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MAX22213

36V, 3.8A Quad Half H-Bridge Drivers with Integrated Current Sense

General Description

The MAX22213 provides four individually controllable 36V, $3.8A_{MAX}$ half H-bridge drivers. It can be used to drive four solenoids, two brushed DC motors, one single stepper motor, or a combination of different loads.

The power FETs have very low impedance resulting in high driving efficiency and low heat generated. The typical total R_{ON} (high side plus low side) is 0.25Ω (typ). Each half bridge can be individually PWM controlled by mean of two logic inputs (DIN_, EN_).

The MAX22213 integrates non-dissipative current sensing, which eliminates the bulky external power resistors normally required for this function, resulting in dramatic space and power saving compared with mainstream applications based on an external sense resistor. A current proportional to the internally-sensed load current is output to the external current-monitor pins (ISEN_). By connecting an external resistor to these pins, a voltage proportional to the motor current is generated. The voltage drop across the external resistors can be input into the controller ADC whenever the control algorithm requires the current/torque information.

The maximum output current per half H-bridge is I_{MAX} = 3.8A and is limited by the overcurrent protection (OCP) circuit. This current can be driven for very short transients and aims to effectively drive small capacitive loads.

The maximum RMS current per H-bridge is I_{RMS} = 2A assuming a 4-layer PCB at room temperature. Since this current is limited by thermal considerations, the actual maximum RMS current depends on the thermal characteristic of the application (PCB ground planes, heatsinks, forced air ventilation etc.).

In applications in which the requirement of the maximum current is less than 1.5A and high-sensing accuracy is desired, the half full-scale (HFS) logic input pin can be set high to halve the current ratings and double the low-side FET R_{ON}. This results in better current-monitor accuracy in the bottom end of the current range.

The MAX22213 features OCP, thermal shutdown (TSD), and undervoltage lockout (UVLO). An open-drain, active-low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During TSD and UVLO events, the driver outputs are three-stated until normal operations are restored.

The MAX22213 is available into a small 5mm x 5mm, 32-pin TQFN and 4.4mm x 9.7mm, 28-pin TSSOP package.

Applications

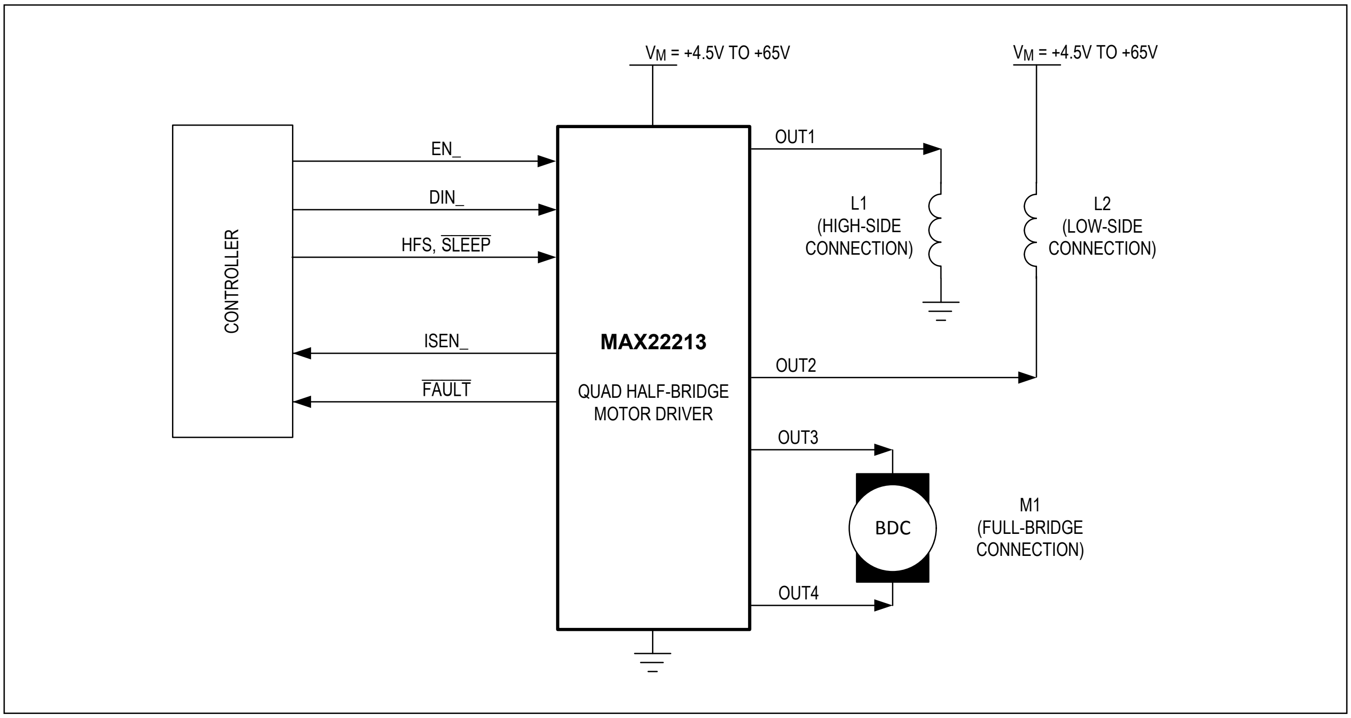
- Stepper-Motor Driver
- Brushed DC Motor Driver
- Solenoid Driver
- Latched Valves

Benefits and Features

- Four Independent Half H-Bridge Drivers
  - 36V Maximum Operating Voltage
  - 0.25Ω R_{ON} (High Side + Low Side) at T_A = +25°C
  - Fully Independent Half Bridge Control
- Current Ratings per H-Bridge (T_A= +25°C):
  - I_{MAX} = 3.8A (Impulsive Current for Driving Capacitive Loads)
  - I_{RMS} = 2A
- Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Half Full-Scale (HFS) Pin to Improve Current-Control Accuracy in the Low-Current Range
- Current-Sense Output Monitor
- Fault Indicator Pin ($\overline{FAULT}$)
- Protections
  - Overcurrent Protection for Each Individual Channel (OCP)
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown T_{SD} = +165°C
- 5mm x 5mm, 32-Pin TQFN and 4.4mm x 9.7mm, 28-Pin TSSOP Packages

Ordering Information appears at end of data sheet.

Simplified Block Diagram



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Absolute Maximum Ratings

V_M to GND .... -0.3V to +42V
V_{DD} to GND........ -0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND .... -0.3V to +0.3V
OUT_ .... -0.3 to (V_M + 0.3)V
V_{CP} to GND........ (V_M - 0.3V) to min (+42V, V_M + 6V)
C_{P2} to GND .... -0.3V to min (+42V, V_M + 0.3V)
C_{P1} to GND .... (V_M - 0.3V) to min (+42V, V_M + 6V)
$\overline{\text{FAULT}}$ to GND .... -0.3V to +6V
ISEN_ to GND .... -0.3V to min (+2.2V, V_{DD} + 0.3V)
DIN_ to GND .... -0.3V to +6V
EN_ to GND .... -0.3V to +6V
HFS to GND .... -0.3V to +6V
$\overline{\text{SLEEP}}$ to GND .... -0.3V to min (+42V, V_M + 0.3V)
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +160°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN—5mm x 5mm

Package Code	T3255-8C
Outline Number	21-0140
Land Pattern Number	90-0013
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	1.7°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

28-Pin TSSOP—4.4mm x 9.7mm

Package Code	U28E+5C
Outline Number	21-0108
Land Pattern Number	90-0147
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	24.65°C/W
Junction to Case (θ_{JC})	1.52°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_M = +4.5V to +36V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply-Voltage Range	V_M		4.5		36	V
Sleep-Mode Current Consumption	I_{VM}	$\overline{\text{SLEEP}}$ = logic low		4	11	µA

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high		2	4	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = internal consumption	1.74	1.8	1.86	V
V_{DD} Current Limit	$I_{V18(LIM)}$		20			mA
V_{DD} UVLO Rising	$UVLOV18_R$	V_{DD} rising	1.59	1.65	1.69	V
V_{DD} UVLO Falling	$UVLOV18_F$	V_{DD} falling	1.535	1.58	1.635	V
Charge-Pump Voltage	V_{CP}			V_M + 2.7		V
LOGIC LEVEL INPUTS/OUTPUTS						
Input Voltage Level—High	V_{IH}		1.2			V
Input Voltage Level—Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pull-Down Current	I_{PD}	To GND	16	34	50	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.2	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = 3.3V	-1		+1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pull-Down Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output On-Resistance Low-Side	$R_{ON(LS)}$	HFS = logic low		0.125	0.22	Ω
		HFS = logic high		0.22	0.42	
Output On-Resistance High-Side	$R_{ON(HS)}$			0.125	0.22	Ω
Output Leakage	I_{LEAK}	Driver off	-5		+5	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			200		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	I_{OCP}		3.8			A
Overcurrent Protection Blanking Time	t_{OCP}		1	2.2	3.2	µs
Autoretry OCP Time	t_{RETRY}			3		ms
UVLO Threshold on V_M	V_{UVLO}	V_M rising	3.85	4	4.15	V
UVLO Threshold on V_M Hysteresis	$UVLO_{HYS}$			0.12		V

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.)

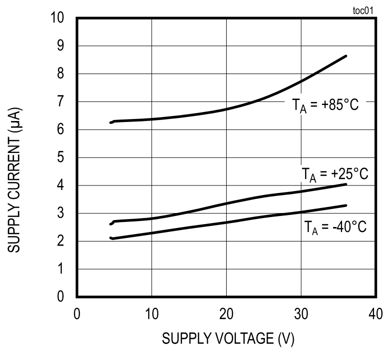
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Protection Threshold Temperature	TSD				+165		°C
Thermal Protection Temperature Hysteresis	TSD_{HYS}				20		°C
CURRENT-SENSE MONITOR							
ISEN_ Voltage Range	ISEN	Voltage range at ISEN_ pins		0		1.1	V
Current-Monitor Scaling Factor	K_{ISEN}	HFS = logic low. See the I_{SEN} output-current equation in the Current-Sense Output (ISEN_)—Current Monitor section.			7500		A/A
		HFS = logic high. See the I_{SEN} output-current equation in the Current-Sense Output (ISEN_)—Current Monitor section.			3840		
Current-Monitor Accuracy	$DKISEN_1$	(Note 1)	HFS = logic low, I_{OUT} = 0.7A to 3A	-5	0.4	+5	%
			HFS = logic high, I_{OUT} = 0.35A to 1.5A	-5	0.4	+5	
	$DKISEN_2$		HFS = logic low, I_{OUT} = 0.4A to 0.7A	-10	0.6	+10	
			HFS = logic high, I_{OUT} = 0.2A to 0.35A	-10	0.6	+10	
Current-Sense Output -3dB Small-Signal Bandwidth	BW				400		KHz
FUNCTIONAL TIMING							
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = logic 1 to logic 0 for OUT_ to become three-state				150	µs
Wake-Up Time from Sleep	t_{WAKE}	$\overline{SLEEP}$ = logic 0 to logic 1 to resume normal operation				3	ms
Enable Time	t_{EN}	Time from EN_ pin rising edge to driver on				0.4	µs
Disable Time	t_{DIS}	Time from EN_ pin falling edge to driver off				0.6	µs

Note 1: Guaranteed by design, not production tested.

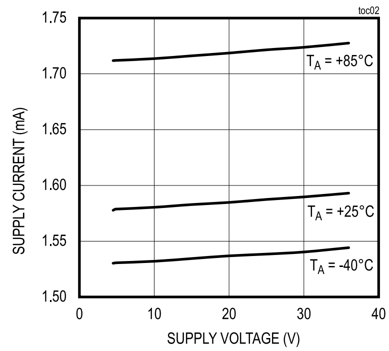
Typical Operating Characteristics

(V_M = +4.5V to +36V; T_A = 25°C unless otherwise noted.)

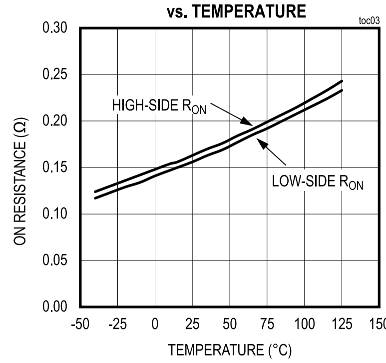
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



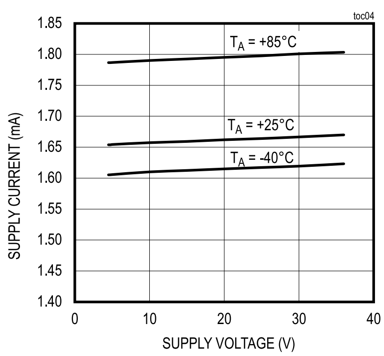
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



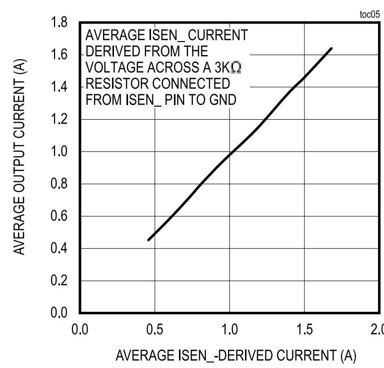
ON RESISTANCE vs. TEMPERATURE



NO LOAD SWITCHING SUPPLY CURRENT vs. SUPPLY VOLTAGE

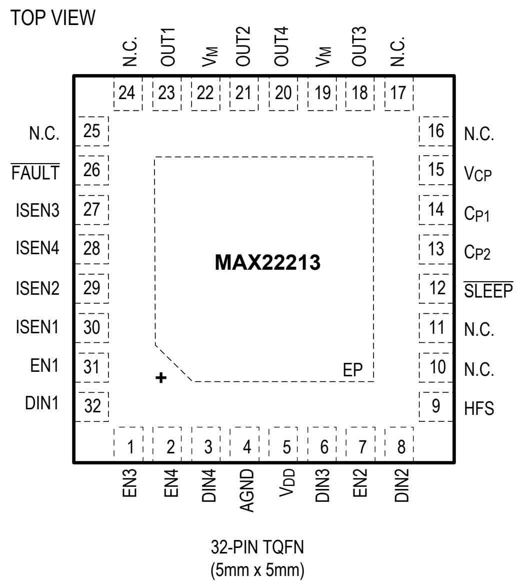


AVERAGE OUTPUT CURRENT vs. AVERAGE ISEN_-DERIVED CURRENT

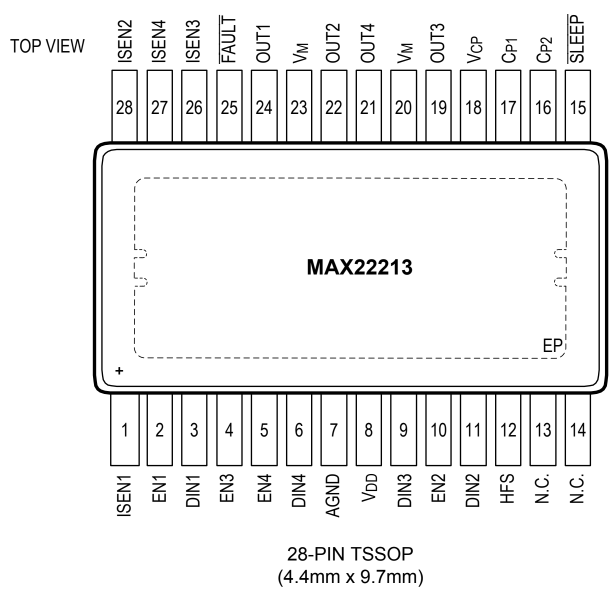


Pin Configurations

TQFN Pin Configuration



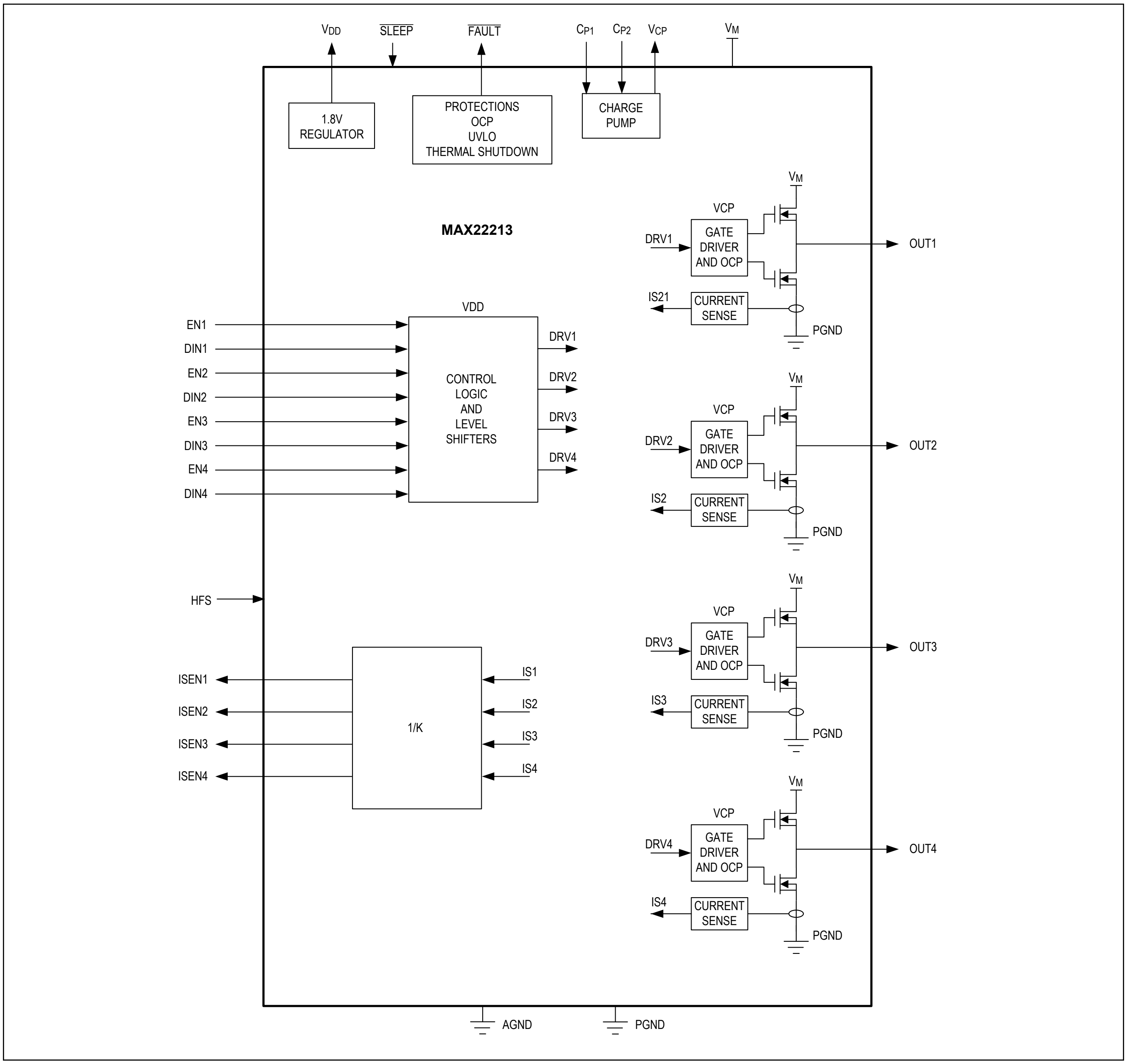
TSSOP Pin Configuration



Pin Description

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
26	25	$\overline{FAULT}$	Active-Low, Open-Drain, Output Fault Indicator. $\overline{FAULT}$ goes low to indicate that one or more of the protection mechanisms has been activated. Connect a pull-up resistor from $\overline{FAULT}$ to the microcontroller supply voltage.	Open Drain Output
4	7	AGND	Analog Ground. Connect to ground plane.	GND
19, 22	20, 23	V_M	Supply Voltage Input. Connect a V_M-rated 1µF (minimum) surface-mounted device capacitor from V_M to GND close to the device, and a 10µF (minimum) electrolytic bypass capacitor from V_M to GND. Higher values can be considered depending on application requirements.	Supply
5	8	V_{DD}	1.8V Linear Regulator Output. Bypass V_{DD} with a 2.2µF capacitor connected close to the device.	Output
23, 21, 18, 20	24, 22, 19, 21	OUT1 to OUT4, respectively	Driver Outputs	Output
30, 29, 27, 28	1, 28, 26, 27	ISEN1 to ISEN4, respectively	Current-Sense Output Monitor. Connect a resistor to GND to monitor the voltage generated with an external ADC (see the *Current-Sense Output (ISEN_)—Current Monitor* section).	Output
32, 8, 6, 3	3, 11, 9, 6	DIN1 to DIN4, respectively	CMOS PWM Inputs	Logic Input
31, 7, 1, 2	2, 10, 4, 5	EN1 to EN4, respectively	Enable Pin. Assert high to enable output drivers.	Logic Input
15	18	V_{CP}	Charge-Pump Output. Connect a 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
14	17	C_{P1}	Charge-Pump Flying Capacitor Pin 1. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
13	16	C_{P2}	Charge-Pump Flying Capacitor Pin 2. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
12	15	$\overline{SLEEP}$	Active-Low Sleep Pin	Logic Input
9	12	HFS	Set Output Current Full Scale. HFS = 0 coefficient is 100%. HFS = 1 coefficient is 50%.	Logic Input
10, 11, 16, 17, 24, 25	13, 14	N.C.	No Connection	—
EP	EP	PGND	Power GND. Connect to ground plane. The thermal exposed pad (EP) is also the electrical power GND pin and must be properly connected to GND.	GND

Functional Diagrams



Detailed Description

The MAX22213 provides four individually controllable 36V, $3.8A_{MAX}$ half H-bridge drivers. It can be used to drive four solenoids, two bushed DC motors, a single stepper motor, or a combination of different loads. The power FETs have very low impedance resulting in high driving efficiency and low heat generation. The typical total R_{ON} (high side plus low side) is 0.25Ω (typ). Each half bridge can be PWM controlled by two logic inputs (DIN_ and EN_). The MAX22213 integrates non-dissipative current sensing which eliminates the bulky external power-sense resistors to reduce space and save power. The internally sensed current is scaled and output to the external current monitor pins (ISEN_), which generate a voltage proportional to the load current when a resistor is connected from the ISEN_ pins to GND. This voltage can be monitored by a microcontroller ADC to get load current and torque information. To improve accuracy for a maximum load current of less than 1.5A, the half full-scale (HFS) logic input can be driven high to halve the maximum current rating and double the low-side FET R_{ON}. The maximum transient output current for each half bridge is I_{MAX} = 3.8A and is limited by overcurrent protection (OCP). This current can be tolerated for short intervals and is aimed to drive small capacitive loads. The maximum RMS current per H-Bridge is I_{RMS} = 2A and is limited by the thermal characteristics of the application such as package and die temperature, PCB ground planes and routing, heatsinks, forced air ventilation, etc.

Sleep Mode ($\overline{\text{SLEEP}}$ Pin)

The $\overline{\text{SLEEP}}$ pin can be driven low to place the device into the lowest power-consumption mode possible, with all outputs three-stated, the internal circuits biased off, and the charge pump disabled. A pull-down resistor should be connected between $\overline{\text{SLEEP}}$ and GND to ensure the part is disabled whenever this pin is not actively driven. Driving the $\overline{\text{SLEEP}}$ pin high wakes up the device and returns it to normal mode. t_{WAKE} is 3ms (max).

PWM Control

When a half-bridge is enabled (EN_ = logic high), the average output voltage is controlled by the corresponding DIN_ logic input. PWM techniques can be used to control the output duty cycle and hence to implement motor speed or solenoid current control.

Setting the EN_ pin at logic low forces the corresponding OUT_ driver pin to enter a high-impedance mode. The EN_ input pin should not be used for PWM control.

Each half-bridge (OUT_) is controlled by two logic inputs (DIN_, EN_). Table 1 shows the control truth table.

Table 1. MAX22213 Truth Table

EN_	IN_	OUT_	DESCRIPTION
0	X	High-Impedance	Half H-bridge is disabled.
1	0	Low	Low-side FET is driven.
1	1	High	High-side FET is driven.

Current-Sense Output (ISEN_)—Current Monitor

A current proportional to the internally-sensed motor current for each OUT_ is output to the ISEN_ pins for each individual half H-bridge. The integrated current sense is unipolar and the current is sensed on the low-side (LS) FET only. Therefore, the current information is meaningful when the LSFET is on and operates in forward mode.

Under this condition, the following ISEN Output Current equation applies:

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Where K_{ISEN} represents the current scaling factor between the output current and its replica at the ISEN_ pins. K_{ISEN} is typically 7.5KA/A (with HFS logic low). For example, if the instantaneous output current is 2A, the current sourced at ISEN_ is 266μA.

When the LS FET is in on in reverse mode or when the HS FET is on, the ISEN_ current monitor outputs a zero current.

Connecting an external signal resistor, R_{ISEN}, between ISEN_ and GND generates a voltage proportional to the motor current. The voltage drop across R_{ISEN} can be input into the ADC of an external controller in applications in which the motor-control algorithm requires the current/torque information. The R_{ISEN} value should be chosen so that the peak voltage meets both the ADC full-scale requirement and does not exceed V_{ISEN} (max). The following equation shows the design formula to calculate R_{ISEN} once the ADC full-scale voltage (V_{FS}) and the maximum operating current (I_{MAX}) are known.

$$R_{ISEN}(\Omega) = K_{ISEN} \times \frac{V_{FS}(V)}{I_{MAX}(A)}$$

For example, if the ADC operates up to 1V FS and the maximum operating output current is 2A, then R_{ISEN} is 7500 x 1V/2A = 3.75KΩ.

The R_{ISEN} value also sets the output impedance of the current-sense output circuit (ISEN_ output impedance). Normally, the input impedance of the ADC is much higher than R_{ISEN}, enabling a direct connection to the ISEN_ pin without attenuation. if a low-input-impedance ADC is used, a pre-amplifier (buffer) can be required.

The current-sense-output circuit bandwidth and step response performances (see the Current-Sense Monitor specifications in the *Electrical Characteristics* section) ensure the current monitor tracks the driver current in motor-drive applications.

Half Full Scale (HFS)

The HFS depends on the status of the logic input pin HFS. When HFS is set logic low, the scalar coefficient is 100% and the power FETs' R_{ON} have a typical value of 0.25Ω (high side plus low side). When the HFS is set logic high, the scalar coefficient is 50% and the power FETs' R_{ON} have a typical value higher of 0.345Ω (high side plus low side). This setting is recommended for applications in which the maximum current does not exceed 1.5A and higher accuracy at low current is desirable.

Table 2 summarizes the HFS settings.

Table 2. HFS Truth Table

HFS	MAXIMUM OUTPUT CURRENT (A)	TYPICAL R_{ON} (HIGH SIDE + LOW SIDE) (Ω)	NOTES
0	3	0.25	Optimized efficiency and extended operating range up to $3.0A_{FS}$.
1	1.5	0.345	Reduced operating range up to $1.5A_{FS}$. Improved current accuracy control at the bottom end of the current range.

Fault Protection

Over Current Protection—(OCP)

OCP protects the device against OUT_ short circuits to the rails (supply voltage and ground) or excessive load currents.

The OCP threshold is set at 3.8A minimum. If the output current is greater than the OCP threshold for longer than the deglitch time (OCP blanking time), an OCP event is detected, the half H-bridge is set to high-impedance mode and the $\overline{FAULT}$ output is driven low to indicate to external circuitry that a fault condition has been detected. The half H-bridge is kept in high-impedance mode for 3ms (typ) (t_{RETRY} specification) before autoretry is initiated when the OUT_ H-bridge is re-enabled according to its current state as defined by EN_and DIN_. If the overcurrent event or short circuit is still present, this cycle repeats. Otherwise, normal operation resumes. The external circuitry monitoring $\overline{FAULT}$ should take action to avoid prolonged operation under the overcurrent mode as a prolonged OCP autoretry could affect the device reliability.

Thermal-Shutdown Protection

If the die temperature exceeds T_{SD} = +165°C (typ), all output pins (OUT1–OUT4) are three-stated and the $\overline{FAULT}$ pin is driven low. The $\overline{FAULT}$ pin remains low and the outputs are placed in three-state mode until the die temperature falls by the hysteresis amount of 20°C (typ), after which the $\overline{FAULT}$ pin is driven high and the outputs are re-enabled.

Undervoltage-Lockout Protection

When the V_M supply voltage is below the UVLO threshold, all OUT_ outputs are three-stated and the $\overline{\text{FAULT}}$ pin is driven low. The OUT_ outputs automatically return to their current state (defined by EN_ and DIN_) when the V_M supply voltage exceeds the OVLO threshold (max) and $\overline{\text{FAULT}}$ is driven high.

Applications Information

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1. Place supply and charge-pump bypass capacitors close to the IC.
2. Ensure a good connection from the exposed pad to the GND plane by using vias and ground pours to help to provide an adequate current path and heat dissipation.
3. Keep the power traces and load connections short and wide. This practice is essential for high efficiency. Use thick copper PCBs (2oz or 1oz vs. 0.5oz) to enhance full-load efficiency and thermal dissipation.
4. Use precision resistors (1% or better) for better accuracy.

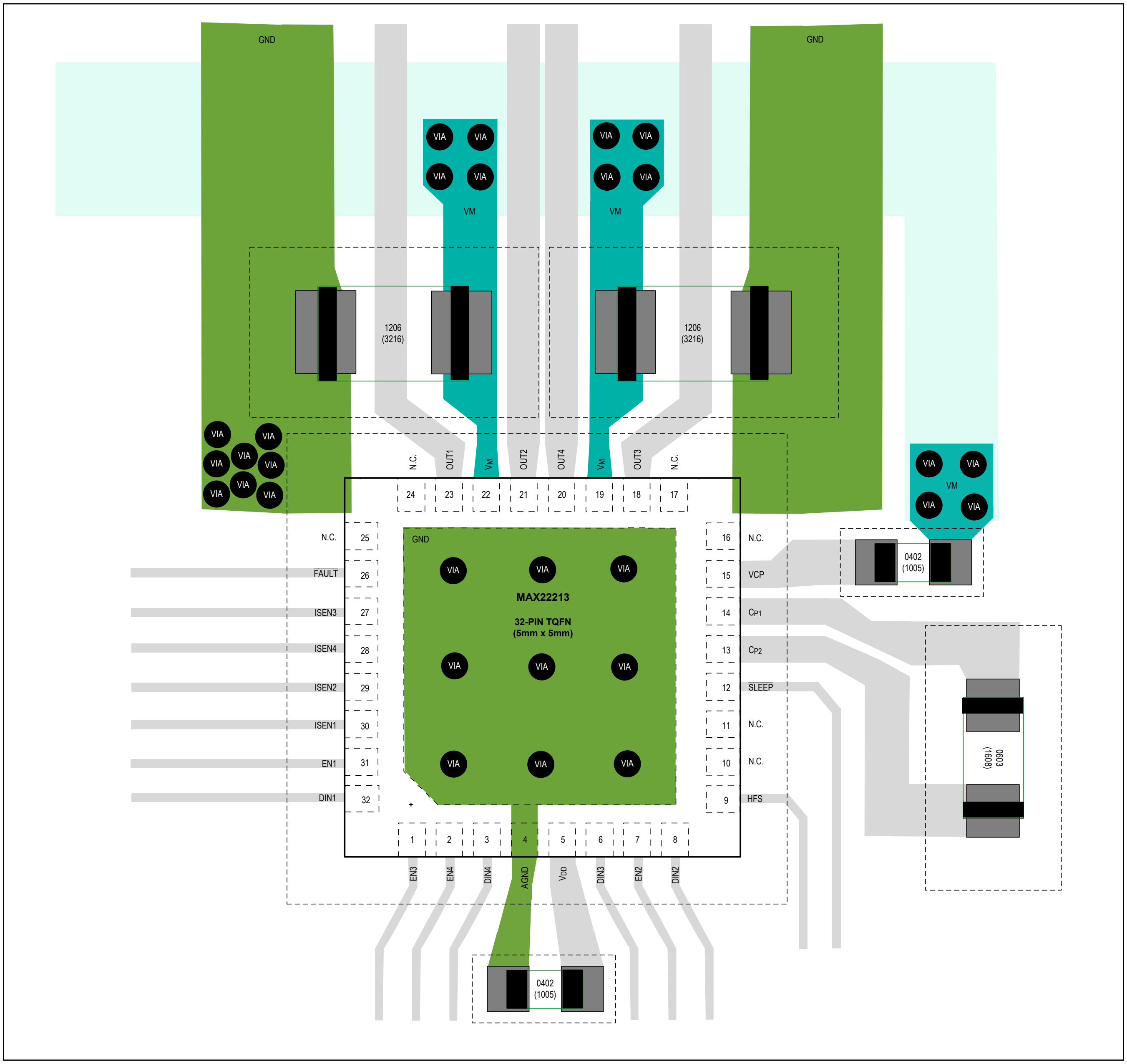
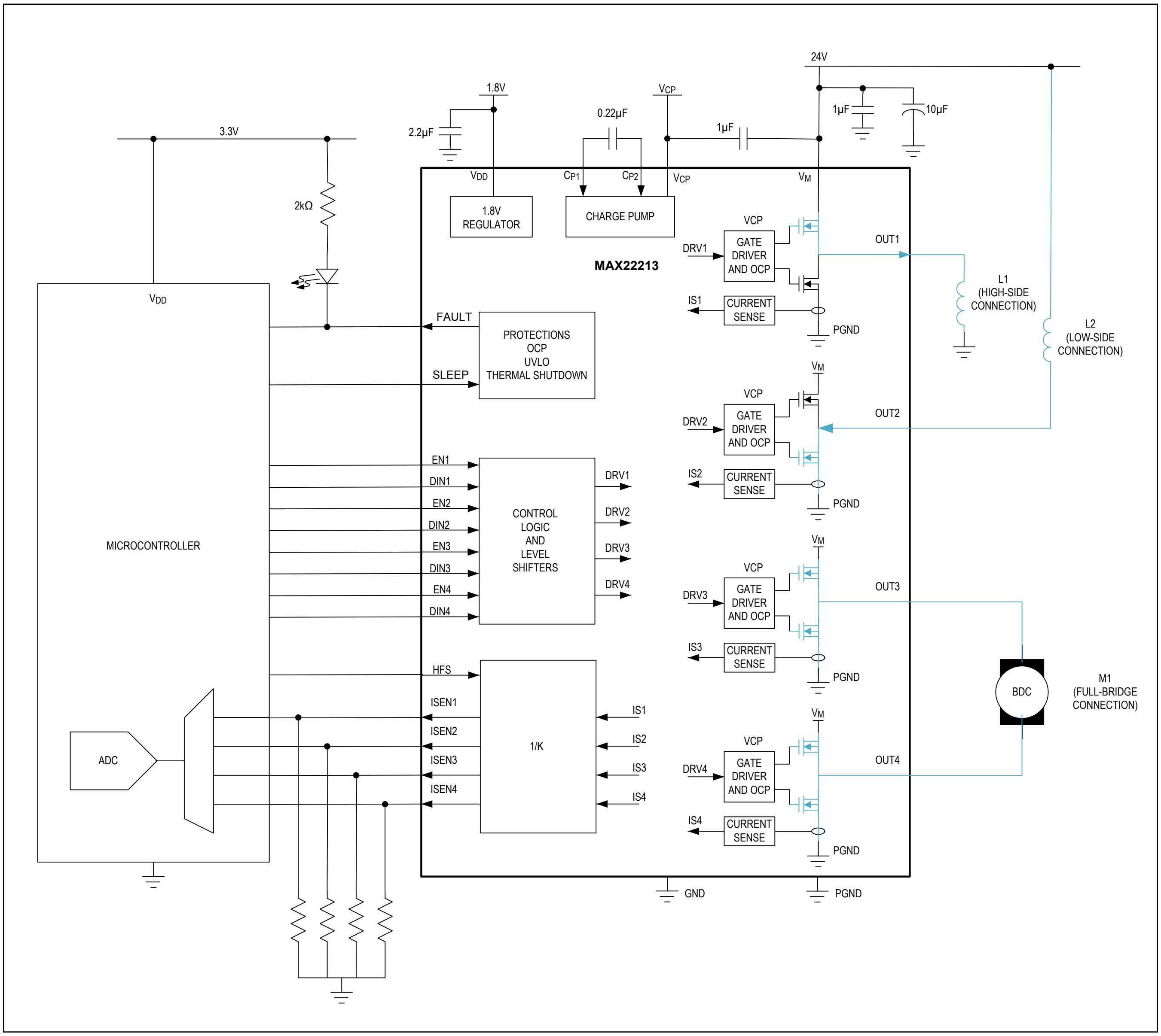


Figure 1. MAX22213 Recommended Layout

Typical Application Circuits

Application Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22213ATJ+	-40°C to +125°C	32 TQFN-EP*
MAX22213ATJ+T	-40°C to +125°C	32 TQFN-EP*
MAX22213AUI+T**	-40°C to +125°C	28 TSSOP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/23	Initial release	—