MAX20402/MAX20403

Automotive 36V, 2.5A/3.5A, Fully Integrated Synchronous Silent Switcher Buck Converters

General Description

The MAX20402/MAX20403 ICs are tiny, low-EMI emission, synchronous Silent Switcher® buck converters with integrated high-side and low-side switches. The MAX20402/MAX20403 deliver up to 2.5A/3.5A over a wide 3V to 36V input voltage range. Voltage quality can be monitored by observing the PGOOD signal. These ICs can operate in dropout by running at 99% duty cycle, making them ideal for automotive and industrial applications.

The MAX20402/MAX20403 offer externally programmable or internally fixed output voltages of 5V and 3.3V. Fixed internal frequency options of 3MHz/2.1MHz/400kHz are available, which allow for small external components and reduced output ripple, and also guarantee no AM interference.

When SYNC is low, the MAX20402/MAX20403 automatically enter skip mode at light loads with an ultra-low quiescent current of 10µA at no load. A pin-selectable, forced-PWM mode is also available, which helps improve EMI performance. The devices have a spread-spectrum frequency modulation option designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX20402/MAX20403 are available in a small, 3mm x 3mm FC2QFN package and use very few external components.

Applications

- Automotive Applications
  - ADAS Systems
  - Radar Modules
  - Infotainment
- Industrial Applications
- High-Voltage DC-DC Converters

Benefits and Features

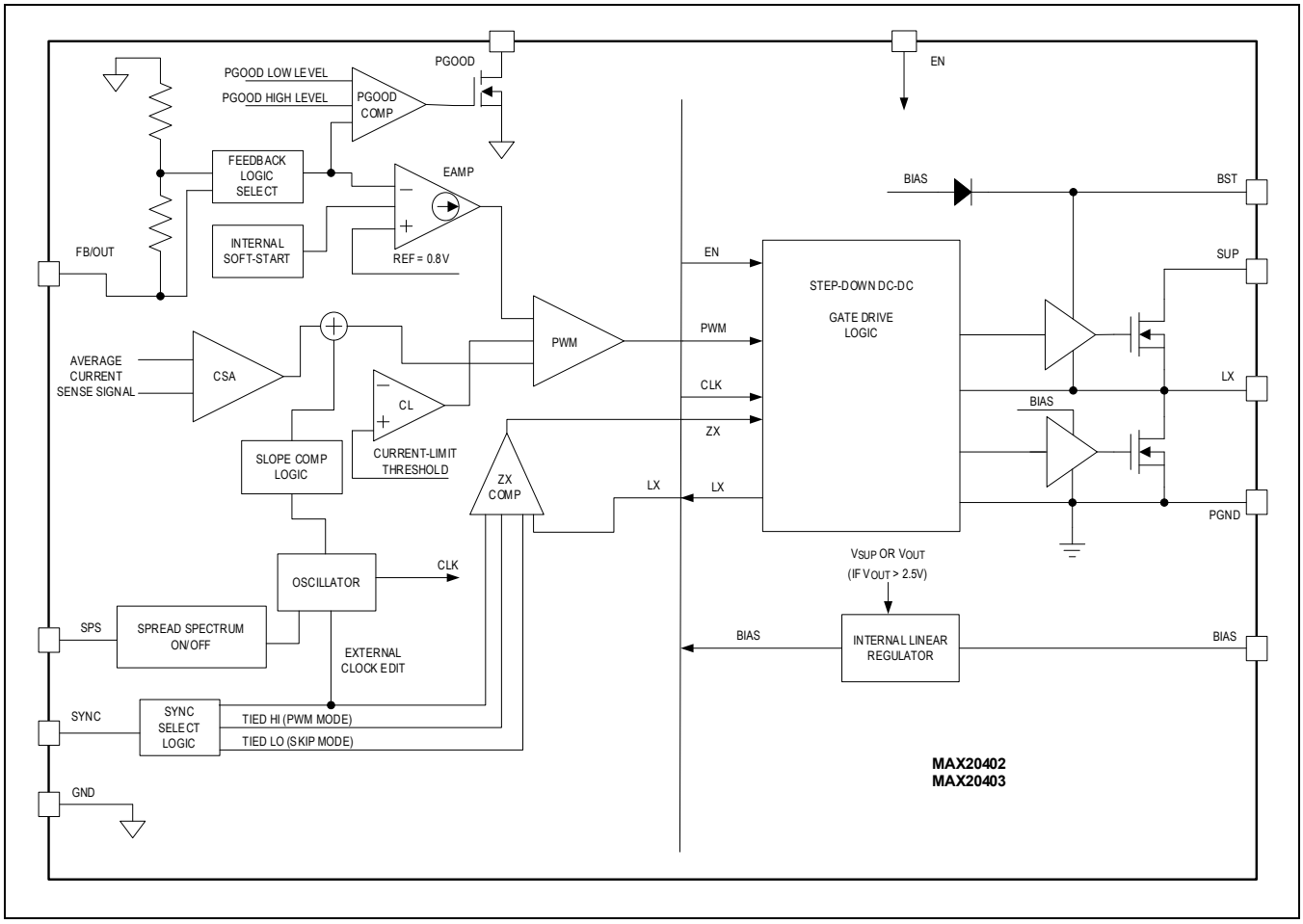
- Silent Switcher
  - Enables Compact, Efficient, Low-EMI Solution
  - Spread-Spectrum Frequency Modulation
  - Symmetrical Package Offers Superior EMI Performance
  - CISPR 25 Class 5-Compliant EV Kit
- Multiple Functions for Small Size
  - Operating Input Voltage Range: 3V to 36V
  - Synchronous DC-DC Converter with Integrated FETs up to 2.5A/3.5A
  - 10µA Quiescent Current in Skip Mode
  - 3MHz/2.1MHz/400kHz Switching Frequency
  - Spread-Spectrum Option
  - Fixed 2.5ms Internal Soft-Start
  - Programmable 0.8V to 12V Output Voltage Range or Fixed 5V/3.3V Options Available
  - 99% Duty Cycle Operation with Low Dropout
- High Precision for Safety Critical Applications
  - ±1.5% Output Voltage Accuracy in FPWM
  - Precision Enable Thresholds for Fully Programmable UVLO Thresholds
  - Accurate Windowed PGOOD
- Robust for the Automotive Environment
  - Average Current-Mode, Forced-PWM, and Skip Operation
  - Overtemperature, Overvoltage, and Short-Circuit Protection
  - 3mm x 3mm FC2QFN
  - -40°C to +125°C Operating Temperature Range
  - 42V Load-Dump Tolerant
  - AEC-Q100 Qualified

Silent Switcher is a registered trademark of Analog Devices, Inc.

***Ordering Information* appears at end of data sheet.**

19-101442; Rev 10; 10/23

Simplified Block Diagram



Absolute Maximum Ratings

SUP ..... -0.3V to +42V
EN ..... -0.3V to +42V
BST to LX ..... -0.3V to +2.2V
BST ..... -0.3V to +44V
LX ..... -0.3V to SUP+0.3V
SYNC ..... -0.3V to +6V
FB/OUT ..... -0.3V to +16V
PGOOD ..... -0.3V to +6V
BIAS ..... -0.3V to +2.2V
SPS ..... -0.3V to +2.2V
PGND to AGND ..... -0.3V to +0.3V
ESD Protection Human Body Model ..... ±2kV
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 25mW/°C above +70°C.) 2000mW
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (Soldering 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	F153B3FY+1	
Outline Number	*21-100532*	
Land Pattern Number	*90-100188*	
THERMAL PARAMETERS	**4-LAYER JEDEC BOARD**	**4-LAYER EV KIT**
Junction-to-Ambient Thermal Resistance (θ_{JA})	51.1°C/W	40.6°C/W
Junction-to-Case (top) Thermal Resistance (θ_{JCt})	32.7°C/W	—
Junction-to-Case (bottom) Thermal Resistance (θ_{JCb})	21.4°C/W	15.6°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	23.3°C/W	11.7°C/W
Junction-to-Top Characterization Parameter (Ψ_{JT})	1.9°C/W	1.8°C/W
Junction-to-Board Characterization Parameter (Ψ_{JB})	25.5°C/W	17.9°C/W

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using JEDEC and the evaluation kit. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1* and *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3		36	V
		t < 1s			42	
Supply Current	I_{SUP_SHDN}	V_{EN} = 0, T_A = +25°C		2.75	5.00	μA
	I_{SUP}	V_{EN} = high, V_{OUT} = 3.3V, fixed output voltage, no load, switching, T_A = +25°C		10		
SUP Undervoltage Lockout	$V_{SUP\_UVLO\_RISE}$	SUP voltage rising	2.900	3.025	3.150	V
	$V_{SUP\_UVLO\_FALL}$	SUP voltage falling	2.600	2.725	2.850	
BIAS Voltage	V_{BIAS}			1.8		V
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	BIAS voltage rising	1.58	1.63	1.68	V

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1* and *Note 2*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS Undervoltage Lockout Hysteresis	$V_{BIAS\_UVLO\_HYS}$	BIAS UVLO hysteresis (*Note 3*)			65		mV
BUCK CONVERTER							
Output Voltage Accuracy 5V	$V_{OUT\_SKIP\_5V}$	T_A = -40°C to +125°C	V_{OUT} = 5V, skip mode, no load	4.92	5.00	5.07	V
	$V_{OUT\_PWM\_5V}$	T_A = -40°C to +125°C	V_{OUT} = 5V, PWM mode, no load	4.94	5.00	5.06	
Output Voltage Accuracy 3.3V	$V_{OUT\_SKIP\_3.3V}$	T_A = -40°C to +125°C	V_{OUT} = 3.3V, skip mode, no load	3.24	3.30	3.36	V
	$V_{OUT\_PWM\_3.3V}$	T_A = -40°C to +125°C	V_{OUT} = 3.3V, PWM mode, no load	3.254	3.300	3.346	
Output Voltage Adjustable Range	V_{OUT}			0.8		12	V
Feedback Voltage Accuracy	V_{FB_PWM}	V_{FB} = 0.8V, PWM mode, no load, T_A = -40°C to +125°C		7.88	0.800	0.812	V
Feedback Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C				100	nA
High-Side DMOS On-Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 0.5A			95	165	mΩ
Low-Side DMOS On-Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 0.5A			45	85	mΩ
High-Side DMOS Current-Limit Threshold	I_{LIM}	MAX20402		3.3	4.0	4.7	A
		MAX20403		4.375	5.300	6.200	
LX Leakage	I_{LX_LKG}	V_{SUP} = 36V, V_{LX} = 0V, or V_{LX} = 36V, T_A = +25°C				1	µA
Soft-Start Ramp Time	t_{SS}				2.5		ms
Minimum On-Time	t_{ON}				35	55	ns
Maximum Duty Cycle	D_{MAX}	Dropout mode		98	99		%
SWITCHING FREQUENCY							
PWM Switching Frequency	f_{SW}	f_{SW} = 400kHz		360	400	440	kHz
		f_{SW} = 2.1MHz		1.925	2.100	2.275	MHz
		f_{SW} = 3.0MHz		2.7	3.0	3.3	
SYNC External Clock Frequency	f_{SYNC}	f_{SW} = 400kHz		300		600	kHz
		f_{SW} = 2.1MHz		1.7		2.6	MHz
		f_{SW} = 3MHz		2.6		3.4	
Spread Spectrum	SPS	Percentage of f_{SW}			±6		%
PGOOD OUTPUT							
PGOOD UV Threshold	$V_{PGOOD\_UV\_THR}$	V_{OUT} rising		91.75	94.00	96.25	%
	$V_{PGOOD\_UV\_THF}$	V_{OUT} falling		90.75	93.00	95.25	
PGOOD OV Threshold	$V_{PGOOD\_OV\_THR}$	V_{OUT} rising		102.75	105.00	107.25	%
	$V_{PGOOD\_OV\_THF}$	V_{OUT} falling		101.75	104.00	106.25	
PGOOD Debounce Time	t_{DEB_rising}	PWM mode	UV rising, OV falling		100		µs

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1* and *Note 2*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	$t_{DEB\_falling}$	PWM mode	UV falling, OV rising		50		
PGOOD Leakage Current	I_{PGOOD_LKG}					1	µA
PGOOD Low Voltage Level	V_{PGOOD_LOW}	Sinking 1mA				0.4	V
LOGIC LEVELS							
EN High Voltage Level	V_{EN_HIGH}			0.825	0.900	0.975	V
EN Low Voltage Level	V_{EN_LOW}			0.625	0.700	0.775	V
EN Hysteresis		(*Note 3*)			200		mV
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 36V, T_A = +25°C				1	µA
SYNC High-Voltage Level	V_{SYNC_HIGH}			1.4			V
SYNC Low-Voltage Level	V_{SYNC_LOW}					0.4	V
SPS High-Voltage Level	V_{SPS_HIGH}			1.4			V
SPS Low-Voltage Level	V_{SPS_LOW}					0.4	V
THERMAL PROTECTION							
Thermal Shutdown	T_{SHDN}				175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}				15		°C

Note 1: Limits are 100% tested at T_A = +125°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

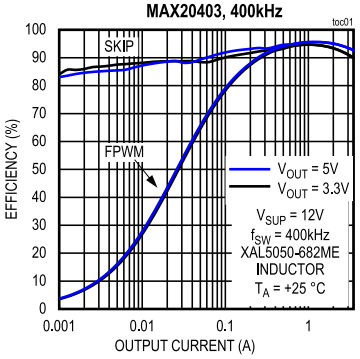
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 3: Guaranteed by design; not production tested.

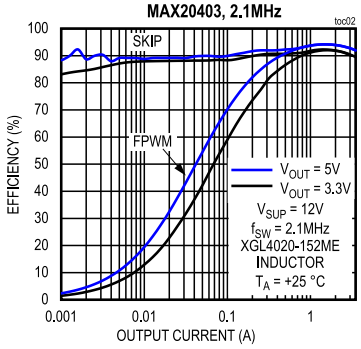
Typical Operating Characteristics

(T_A = +25°C unless otherwise noted.)

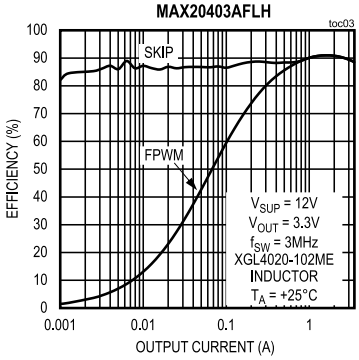
EFFICIENCY vs. OUTPUT CURRENT
MAX20403, 400kHz



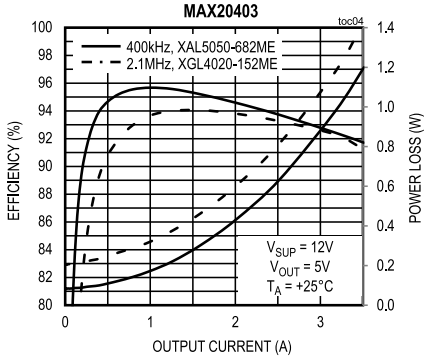
EFFICIENCY vs. OUTPUT CURRENT
MAX20403, 2.1MHz



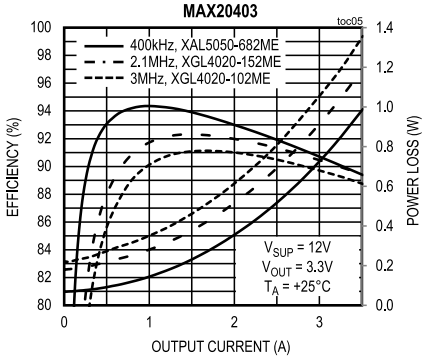
EFFICIENCY vs. OUTPUT CURRENT
MAX20403AFLH



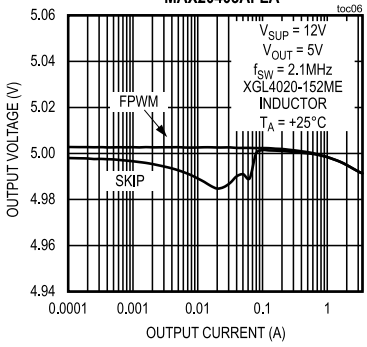
EFFICIENCY AND POWER LOSS
vs. OUTPUT CURRENT
MAX20403



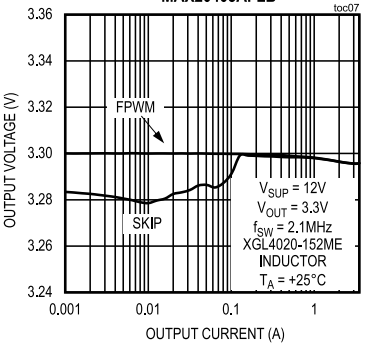
EFFICIENCY AND POWER LOSS
vs. OUTPUT CURRENT
MAX20403



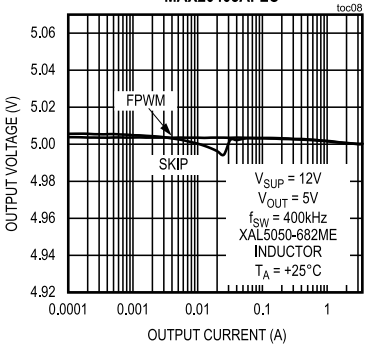
OUTPUT LOAD REGULATION
MAX20403AFLA



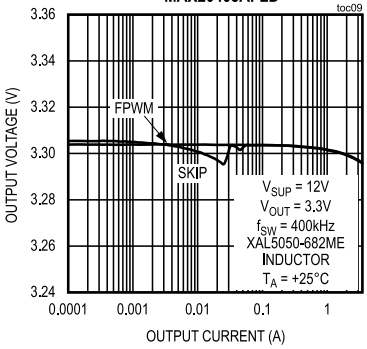
OUTPUT LOAD REGULATION
MAX20403AFLB



OUTPUT LOAD REGULATION
MAX20403AFLC

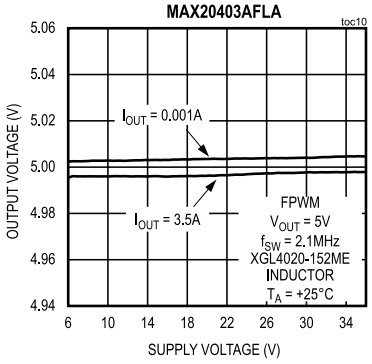


OUTPUT LOAD REGULATION
MAX20403AFLD

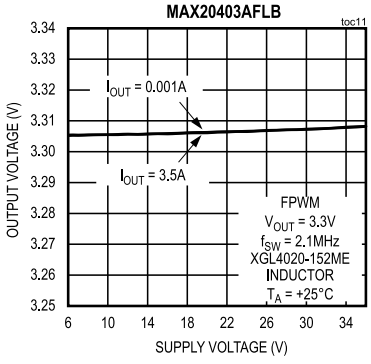


(T_A = +25°C unless otherwise noted.)

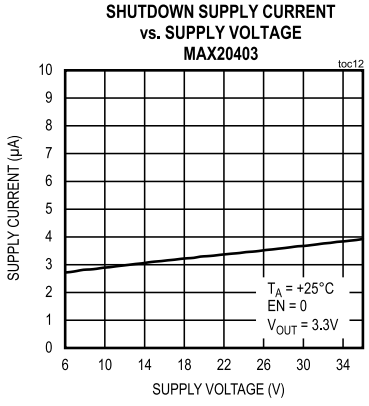
OUTPUT LINE REGULATION MAX20403AFLA



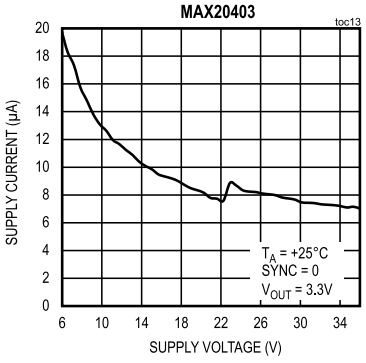
OUTPUT LINE REGULATION MAX20403AFLB



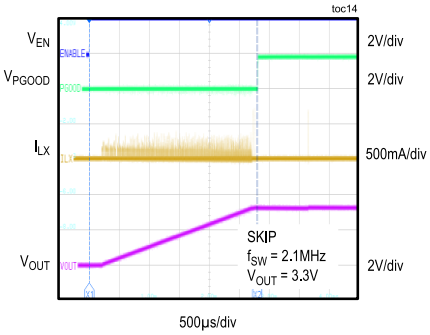
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE MAX20403



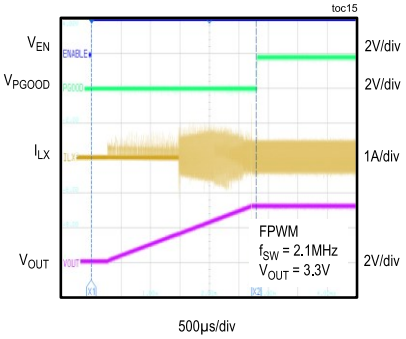
QUIESCENT CURRENT vs. SUPPLY VOLTAGE MAX20403



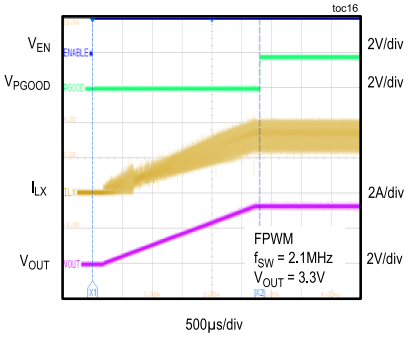
STARTUP INTO NO LOAD



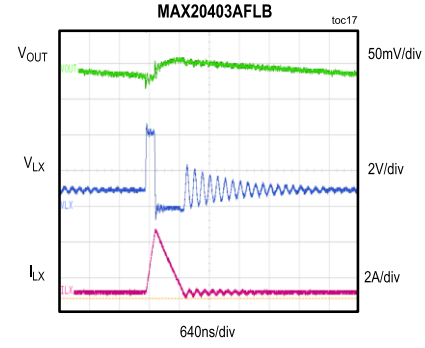
STARTUP INTO NO LOAD



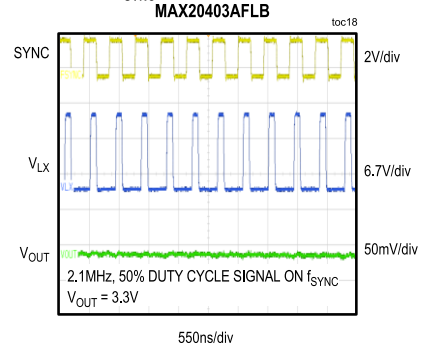
STARTUP INTO FULL LOAD



SKIP-MODE OPERATION MAX20403AFLB

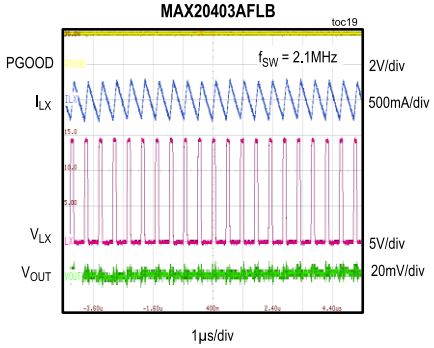


f_{SYNC} SYNCHRONIZATION MAX20403AFLB

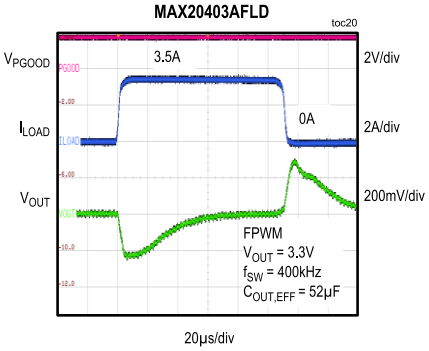


(T_A = +25°C unless otherwise noted.)

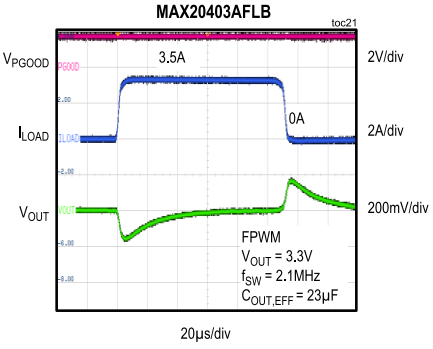
STEADY-STATE SWITCHING WAVEFORM
MAX20403AFLB



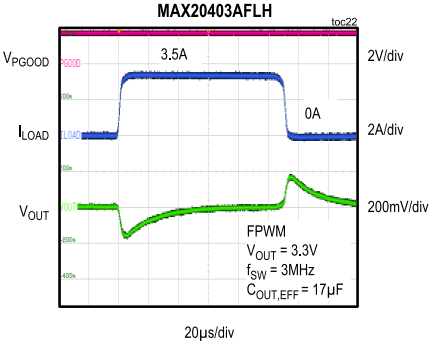
LOAD-TRANSIENT RESPONSE
MAX20403AFLD



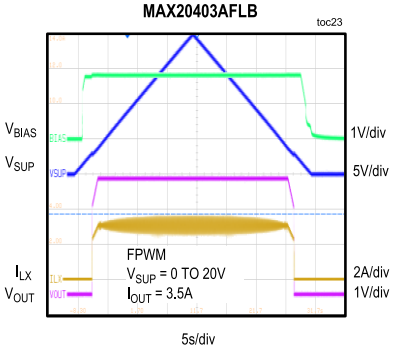
LOAD-TRANSIENT RESPONSE
MAX20403AFLB



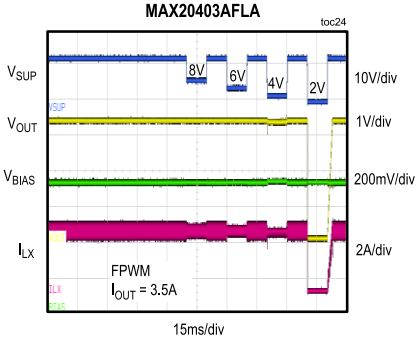
LOAD-TRANSIENT RESPONSE
MAX20403AFLH



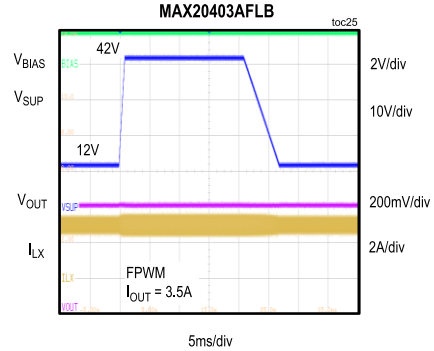
SLOW INPUT VOLTAGE RISING
MAX20403AFLB



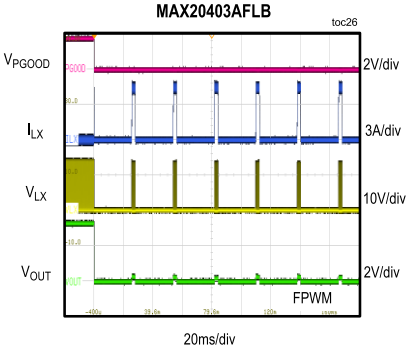
DIPS AND DROPS
MAX20403AFLA



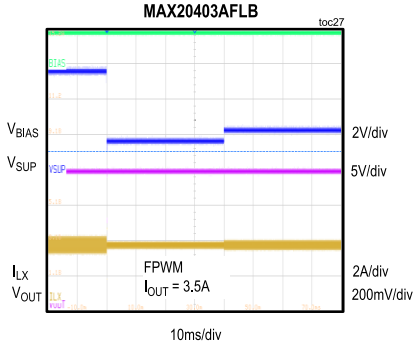
LOAD DUMP
MAX20403AFLB



OUTPUT SHORT TO GROUND
MAX20403AFLB

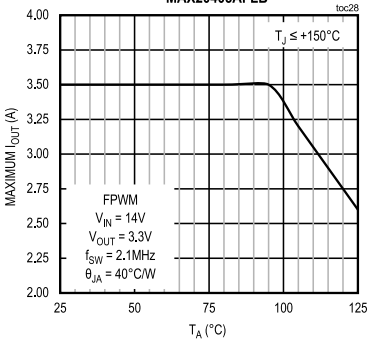


COLD CRANK
MAX20403AFLB

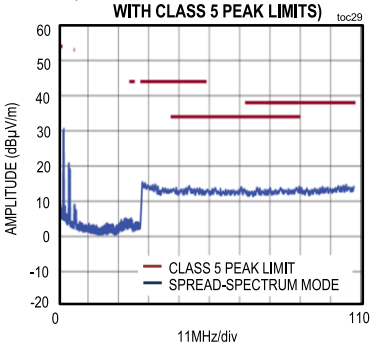


(T_A = +25°C unless otherwise noted.)

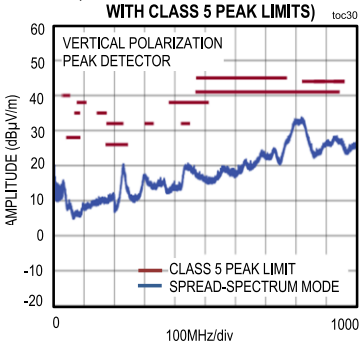
MAXIMUM I_{OUT} (AVE)
MAX20403AFLB



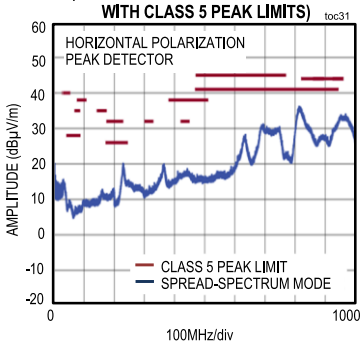
CONDUCTED EMI PERFORMANCE
(CISPR25 CONDUCTED EMISSION TEST
WITH CLASS 5 PEAK LIMITS)



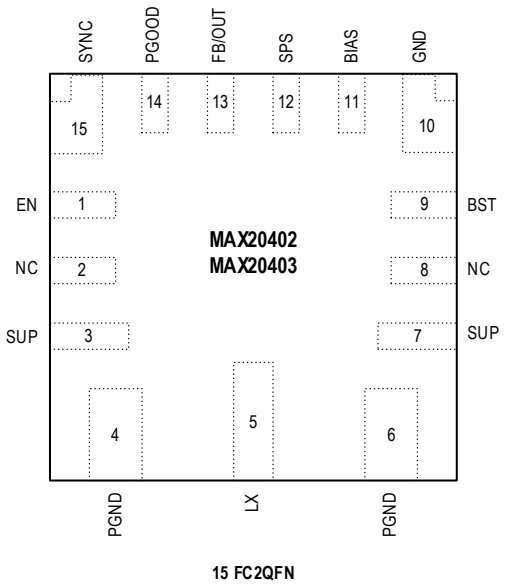
RADIATED EMI PERFORMANCE
(CISPR25 RADIATED EMISSION TEST
WITH CLASS 5 PEAK LIMITS)



RADIATED EMI PERFORMANCE
(CISPR25 RADIATED EMISSION TEST
WITH CLASS 5 PEAK LIMITS)



Pin Configurations



15 FC2QFN

Pin Descriptions

PIN	NAME	FUNCTION
1	EN	High-Voltage-Tolerant, Active-High Digital Enable Input. Drive EN high to enable buck converter.
2, 8	NC	Not Connected
3, 7	SUP	Internal High-Side Supply Input. SUP provides power to the internal switch and LDO. Bypass SUP to PGND with 0.1µF and 2.2µF ceramic capacitors. Place the 0.1µF capacitor as close to the SUP and PGND pins as possible, followed by the 2.2µF capacitor.
4, 6	PGND	Power Ground
5	LX	Inductor Connection. Connect LX to the switched side of the inductor.
9	BST	Boost Flying Capacitor Connection for High-Side FET Gate Voltage. Connect a 0.1µF ceramic capacitor between BST and LX.
10	GND	Quiet Analog Ground
11	BIAS	1.8V Internal BIAS Supply. Connect a minimum of 2.2µF ceramic capacitor from BIAS to PGND.
12	SPS	Spread-Spectrum Enable. Connect logic-high to enable spread spectrum of the internal oscillator or logic-low to disable spread spectrum.
13	FB/OUT	Feedback/Output Sense Input. For the adjustable-output-voltage IC, it acts as an output voltage feedback input (FB). Connect an external resistor-divider between OUT, FB, and AGND to set the output voltage. For the fixed-output-voltage IC, it acts as an output voltage sense pin (OUT). Connect OUT to the buck output to sense the output voltage.
13	OUT	Output Sense Input. Connect OUT to the buck output to sense the output voltage.
14	PGOOD	Open-Drain, Power-Good Output. Connect PGOOD to BIAS or an external positive power supply with a pullup resistor.
15	SYNC	External Clock Synchronization Input. Connect an external clock in the given frequency range to enable external clock synchronization. Connect SYNC to low to enable skip mode. Connect SYNC to high to enable FPWM mode.

Detailed Description

The MAX20402/MAX20403 are small, synchronous buck converters with integrated high-side and low-side switches. These devices are designed to deliver up to 2.5A/3.5A for input voltages of 3V to 36V. They offer fixed output voltage options of 5V and 3.3V, or adjustable output voltage options from 0.8V to 12V. Output voltage quality can be monitored by observing the PGOOD signal. The devices can operate in dropout by running at 99% duty cycle, making them ideal for automotive and industrial applications.

Frequency is internally fixed at 3MHz/2.1MHz/400kHz, which allows for small external components and reduced output ripple, and guarantees no AM interference. These converters automatically enter skip mode at light loads with ultra-low quiescent current of 10µA (typ) at no load when SYNC is pulled low. They feature spread-spectrum frequency modulation to minimize EMI-radiated emissions. The average current-mode architecture allows much better noise rejection of the current loop and very short minimum on-time.

Linear Regulator Output (BIAS)

The devices include a 1.8V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to GND. For the internal feedback version, the bias regulator draws power from the SUP input during startup and switches over to the output after the startup is complete.

System Enable (EN)

An enable control input (EN) activates the device from low-power shutdown mode. EN is compatible with inputs from the automotive battery level down to 3V. Drive EN high to turn on the internal linear BIAS LDO. Once V_{BIAS} is above the internal lockout threshold of 1.63V (typ), the converter is enabled and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During shutdown, the BIAS regulator and gate drivers turn off, and the quiescent current is reduced to 2.75µA (typ).

Synchronization Input (SYNC)

SYNC is a logic-level input used for operation-mode selection and frequency control. Connect SYNC to BIAS to enable forced fixed-frequency operation (FPWM) or to GND to enable automatic skip-mode operation for light load efficiency.

SYNC can also be connected to an external clock, enabling forced-frequency operation. The device synchronizes to an external clock in two cycles, synchronizing at the rising edge of the signal applied. See the external clock frequency limits specified in the *Electrical Characteristics* table. When the external clock signal at SYNC is absent for more than two clock cycles, the IC switches to use the internal clock.

Soft-Start

The devices include a fixed, internal soft-start time. Soft-start time limits start-up inrush current by forcing the output voltage to ramp up towards its regulation point. The soft-start ramp rate is set at 2.5ms (typ).

Power-Good Output (PGOOD)

The MAX20402/MAX20403 feature an open-drain, power-good output (PGOOD) to monitor output voltage quality. PGOOD is an active-high output signal that pulls low when V_{OUT} falls below 93% (typ) of its nominal value or rises above 105% (typ) of its nominal value. Connect a 20kΩ (typ) pull-up resistor to an external supply or to the on-chip BIAS output.

Spread Spectrum

The devices feature a spread-spectrum option. When the SPS pin is pulled high, the spread-spectrum feature is enabled and the internal operating frequency is varied by ±6% relative to the internally generated operating frequency. The modulation signal is a triangular wave with a period of 1.25ms at 400kHz (200µs at 2.1MHz). Spread spectrum is disabled if the device is synchronized to an external clock.

Overcurrent and Short-Circuit Protection

The MAX20402/MAX20403 feature a current limit that protects them against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side switch remains on until the inductor current reaches the specified LX current-limit threshold. The converter then turns the high-side switch off and the low-side switch on to allow the inductor current to ramp down. Once the inductor current crosses below the low-side valley current-limit threshold, the converter turns on the high-side switch again. This cycle repeats until the short-circuit or overload condition is removed.

A short circuit is detected when the output voltage falls below 50% of the regulation voltage while in current limit. If this occurs, hiccup mode activates, and the output turns off for 25ms (10 x 2.5ms) and then attempts to restart. This repeats indefinitely while the short-circuit condition is present. Hiccup mode is disabled during soft-start.

Thermal Shutdown

Thermal shutdown protects the devices from excessive operating temperature. When the junction temperature exceeds +175°C, an internal sensor shuts down the step-down converter, allowing the IC to cool. The sensor turns the IC on again after the junction temperature cools by 15°C.

Overvoltage Protection

The ICs feature overvoltage protection for the output. In case of an overvoltage event in skip mode, the high-side switch is turned OFF and the low-side switch is turned ON until the inductor current reaches a fixed negative value. Once this value is reached, the low-side switch is turned OFF and turns ON again in the next cycle until the output falls below the OV falling threshold. This way, the output is quickly discharged and brought back to regulation.

Applications Information

Setting the Output Voltage

The MAX20402/MAX20403 are available as fixed-output-voltage versions or adjustable-output-voltage versions. The fixed-output-voltage ICs have an internally-fixed output of 5V/3.3V. For the adjustable-output-voltage ICs, the output voltage can be adjusted between 0.8V and 12V using an external resistor-divider. Connect a resistor-divider from the buck output to FB to AGND and a feed-forward capacitor from buck output to FB (see the Adjustable-Output IC diagram in the *Typical Application Circuits* section). Select $R_{FB2} \leq 50k\Omega$. Calculate R_{FB1} with the following equation:

Equation 1:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$ where $V_{FB} = 0.8V$.

Table 1 provides component selection recommendations for each output voltage range. The feed-forward capacitor (CFF) is recommended based on $R_{FB1} = 50k\Omega$.

Table 1. Recommended Components for Adjustable Output

PART NUMBER	FREQUENCY	V_{OUT} (V)	INDUCTOR (µH)	EFFECTIVE C_{OUT} (µF)	CFF (pF)
MAX20402	400kHz	0.8 to 1.5	3.3	120	—
		1.5 to 3	4.7	63	33
		3 to 6	6.8	40	33
		6 to 12	8.2	30	22
	2.1MHz	0.8 to 1.5	1.5	120	—
		1.5 to 3	1.5	46	33
		3 to 6	2.2	25	33
		6 to 12	3.3	18	22
MAX20403	400kHz	0.8 to 1.5	3.3	130	—
		1.5 to 3	3.3	70	33
		3 to 6	6.8	50	33
		6 to 12	8.2	40	22
	2.1MHz	0.8 to 1.5	1.0	120	—
		1.5 to 3	1.0	46	33
		3 to 6	1.5	25	33
		6 to 12	2.2	18	22

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The MAX20402/MAX20403 incorporate a symmetrical pinout to improve EMI performance. It is recommended to split the input capacitors symmetrically between the two SUP pins. Connect a 2.2µF (min) ceramic capacitor on each SUP pin for low-input voltage ripple. For additional noise immunity, a high-frequency 0603 or smaller capacitor can be added on each SUP pin. A bulk capacitor is typically required to provide the remaining capacitance needed to minimize input voltage ripple and to improve load transient response.

Output Capacitor

The output capacitor is selected to meet output voltage ripple, load-transient response, and loop stability requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-change requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. Output capacitance also affects the control-loop stability.

The optimal phase margin for the fixed-output IC is achieved by using the effective output capacitance shown in *Table 2*.

Table 2. Recommended Output Capacitance for Fixed-Output-Voltage Versions

PART NUMBER	FREQUENCY	EFFECTIVE C_{OUT} (µF)	
		TYP	MIN
MAX20402	400kHz	42	34
	2.1MHz	23	18
	3MHz	18	16
MAX20403	400kHz	42	34
	2.1MHz	23	18
	3MHz	18	16

Inductor Selection

Inductor design is a compromise between the size, efficiency, control-loop bandwidth, and stability of the converter. Insufficient inductance increases the inductor current ripple, causing higher conduction losses and higher output voltage ripple. Since the slope compensation is fixed internally for MAX20402/MAX20403, it might also cause current-mode-control instability. A large inductor reduces the ripple, but increases the size and cost of the solution and slows the response. *Table 3* provides optimized inductor values for the respective switching frequency of the fixed-output IC.

Table 3. Recommended Inductor for Fixed-Output-Voltage Versions

PART NUMBER	FREQUENCY	INDUCTANCE (µH)		
		TYP	MIN	MAX
MAX20402	400kHz	8.2	6.8	10
	2.1MHz	2.2	1.5	3.3
	3MHz	1.5	1	2.2
MAX20403	400kHz	6.8	4.7	8.2
	2.1MHz	1.5	1.0	2.2
	3MHz	1.0	0.8	1.5

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching-power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. The package for the MAX20402/MAX20403 offers a unique symmetrical design, which helps cancel the magnetic field generated in the opposite direction. See *Figure 1* for an example layout figure and the following guidelines for good PCB layout:

Place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.

Place the input capacitors in a symmetrical configuration, with a 2.2µF (min) input capacitor on each SUP pin, close to the device. For additional noise immunity, when adding a high-frequency ceramic input-bypass capacitor (CBP) on each SUP pin, first place the high-frequency capacitor as close to the pin as possible, followed by the 2.2µF capacitor. Place the ceramic capacitors as close as possible to the SUP and PGND pins on both sides of the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. The CBP should be located closest to the IC and should have very good high-frequency performance (small package size and high capacitance). This will provide the best EMI rejection and minimize internal noise on the device, which can degrade performance.

Connect PGND and GND pins directly under the IC. This ensures the shortest connection path between GND and PGND.

Place the BIAS capacitor as close to the IC BIAS pin as possible to reduce the bias current loop. This helps to reduce noise on BIAS for smooth operation.

Place the bootstrap capacitor C_{BST} close to the IC and use short, wide traces to minimize the loop area in order to minimize the parasitic inductance. Use the nearest layer for a return trace (C_{BST} to LX) to minimize the inductance further. Refer to the layout in the EV kit for optimum design. High parasitic inductance can impact switching speed (increase switching losses) and cause high dv/dt noise.

Place the inductor as close to the IC LX pin as possible and minimize the area of the LX node.

Place the output capacitors in a symmetrical configuration on opposite sides of the inductor for best noise immunity. Place the output capacitors (C_{OUT}) near the inductor so that the ground side of C_{OUT} is near the C_{IN} ground connection to minimize the current-loop area. Add vias on the capacitor ground to minimize the inductance. For additional noise immunity, place a high-frequency capacitor on each side of the inductor, followed by the output capacitors to further reduce the radiated noise.

Place the inductor, output capacitors, bootstrap capacitor, and BIAS capacitor in such a way as to minimize the area enclosed by the current loops. Keep the power traces and load connections short. This practice is essential for high efficiency. Use a thick copper PCB to enhance full-load efficiency and power-dissipation capability.

Use internal PCB layers as ground planes to help improve the EMI, as ground planes act as a shield against radiated noise. Spread multiple vias around the board, especially near the ground connections.

Use a continuous copper GND plane on the layer next to the IC to shield the entire circuit. The GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias at the GND terminals of the IC and input/output/bypass capacitors. Do not separate or isolate PGND and GND connections with separate planes or areas.

Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor and LX node and other noisy signals.

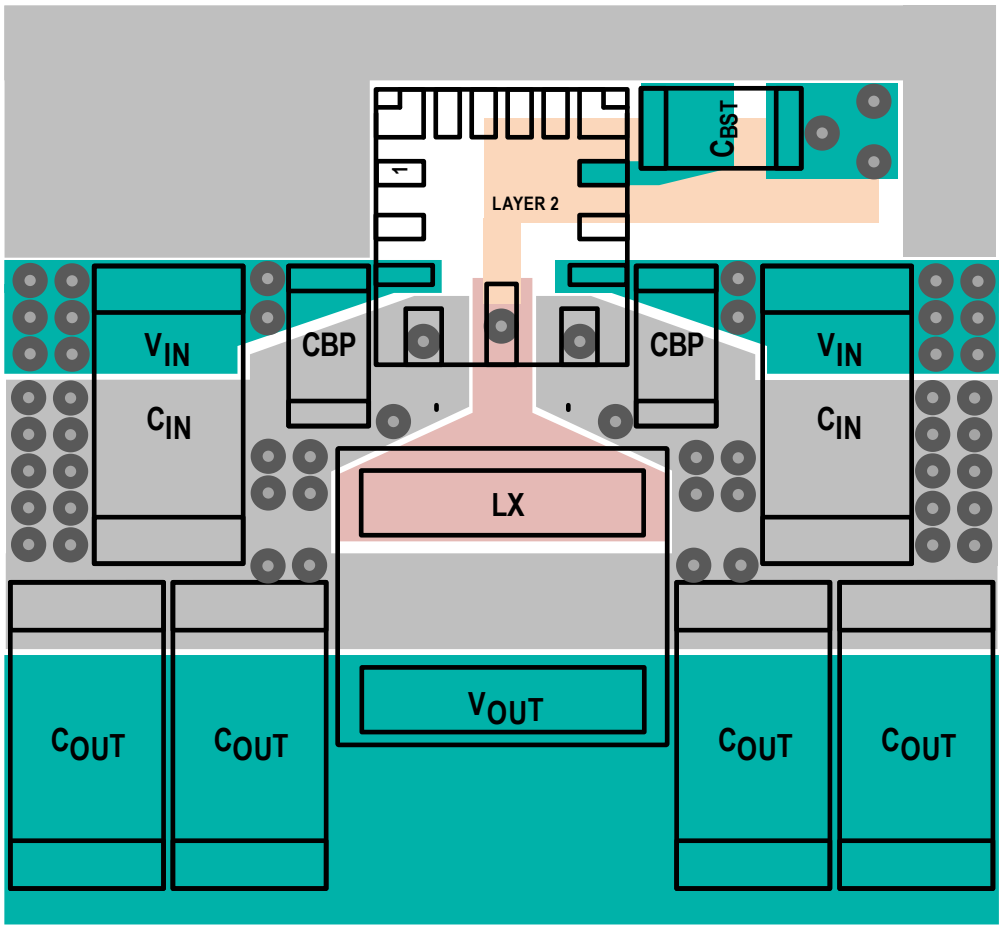
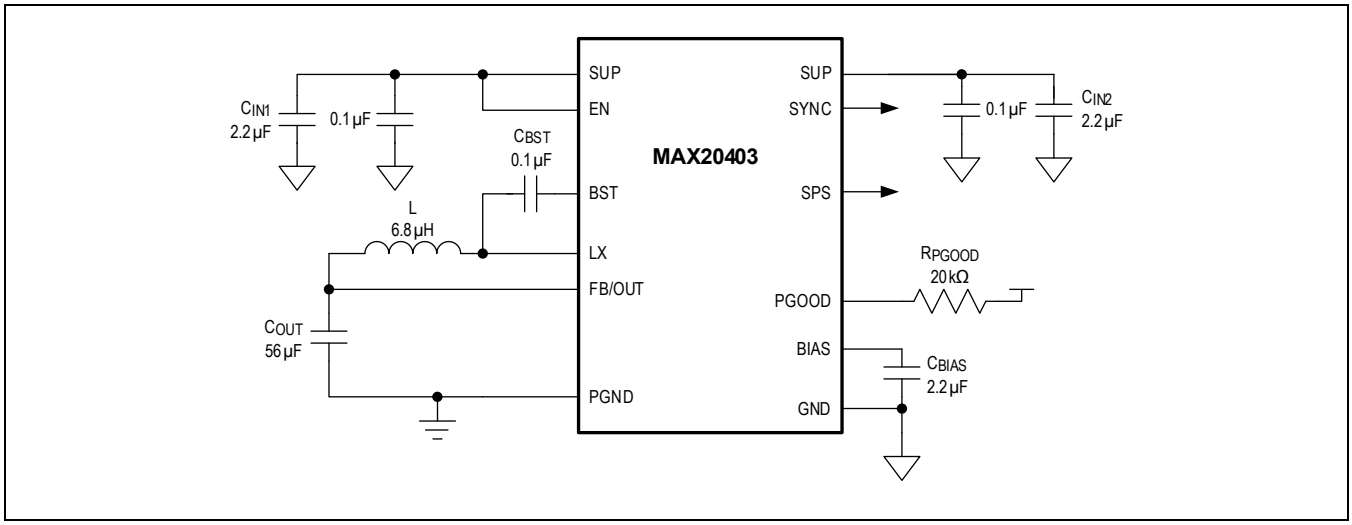


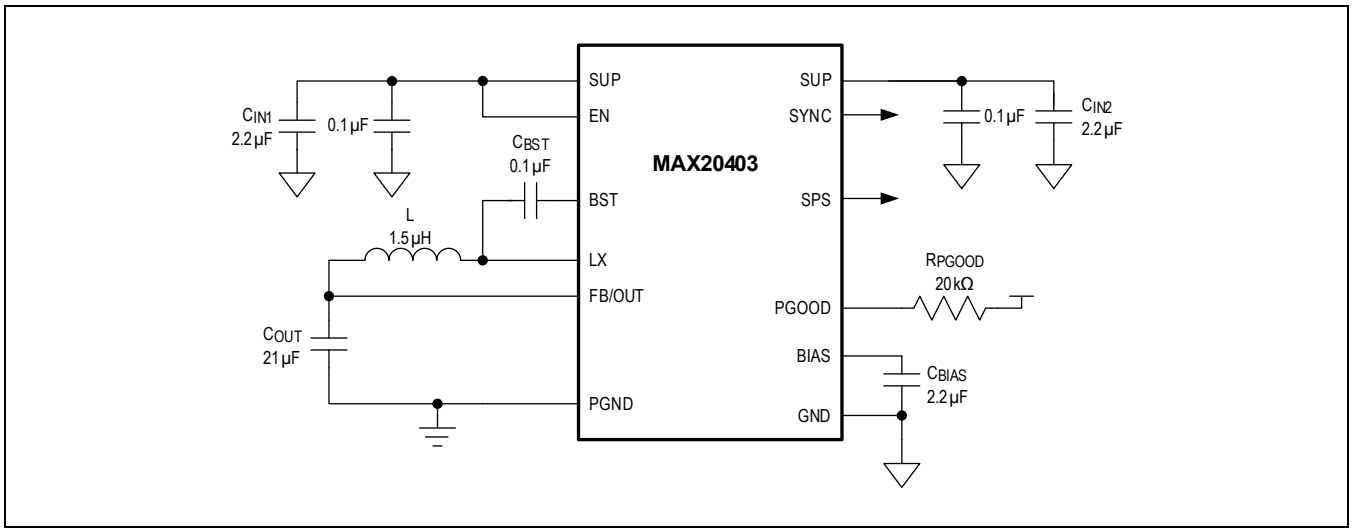
Figure 1. PCB Layout Example

Typical Application Circuits

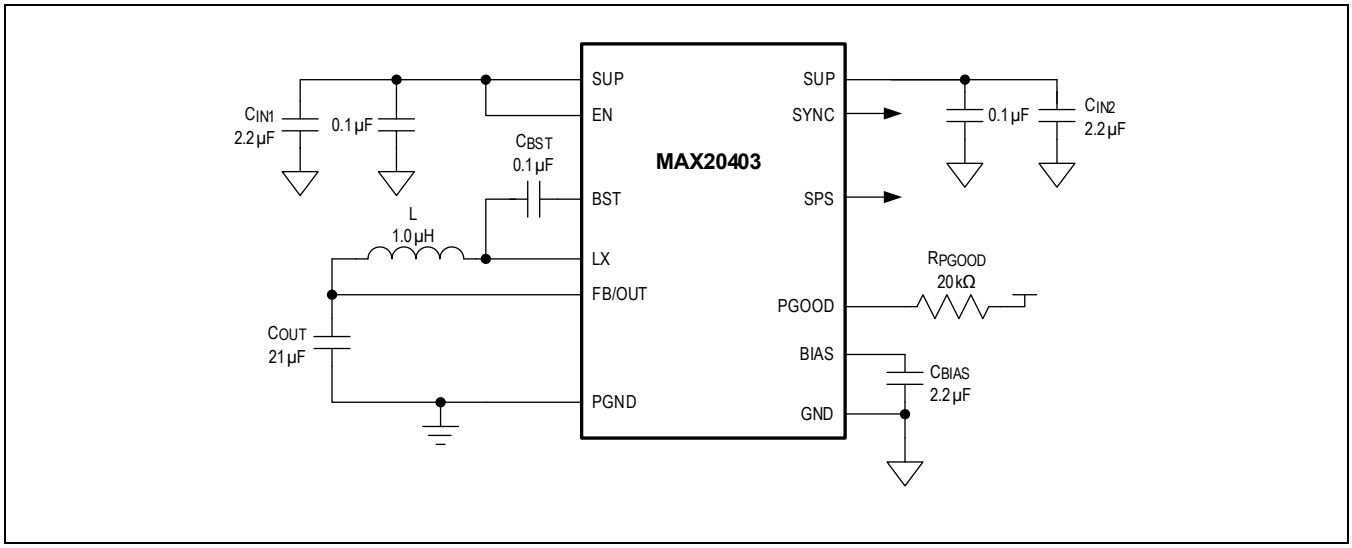
400kHz



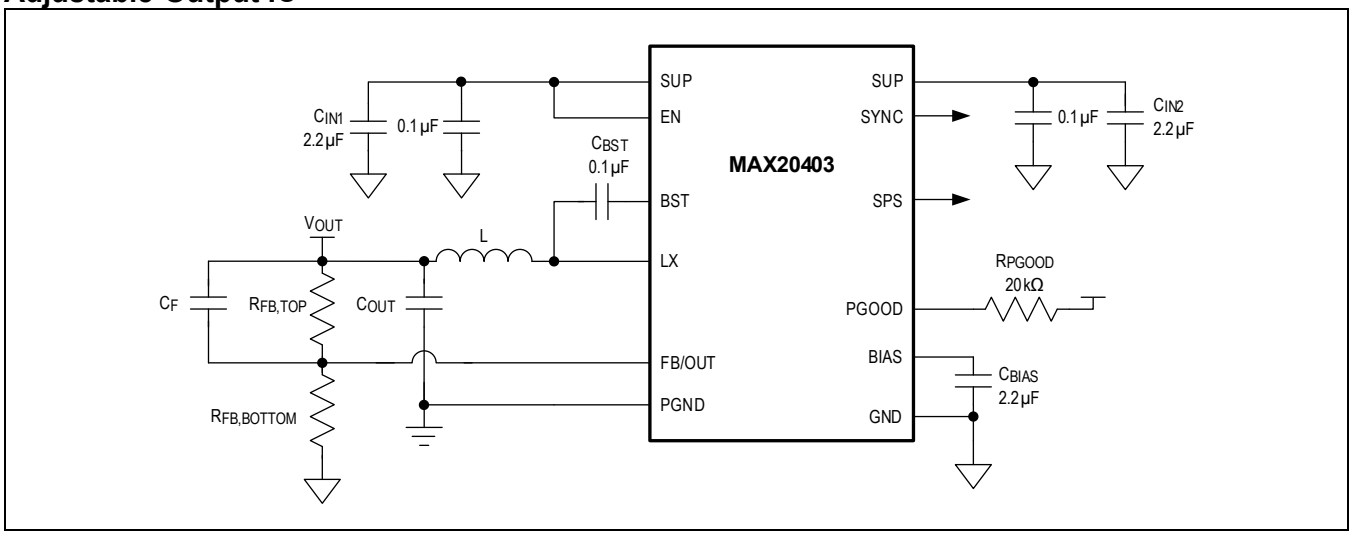
2.1MHz



3MHz



Adjustable-Output IC



Ordering Information

PART NUMBER	V_{OUT} (V)	MAXIMUM LOAD CURRENT (A)	SWITCHING FREQUENCY	SPREAD SPECTRUM (%)
MAX20402AFLA/VY+	5	2.5	2.1MHz	±6
MAX20402AFLB/VY+	3.3	2.5	2.1MHz	±6
MAX20402AFLC/VY+	5	2.5	400kHz	±6
MAX20402AFLD/VY+	3.3	2.5	400kHz	±6
MAX20402AFLE/VY+	Adjustable 0.8V to 12V	2.5	2.1MHz	±6
MAX20402AFLF/VY+	Adjustable 0.8V to 12V	2.5	400kHz	±6
MAX20403AFLA/VY+	5	3.5	2.1MHz	±6

MAX20403AFLB/VY+	3.3	3.5	2.1MHz	±6
MAX20403AFLC/VY+*	5	3.5	400kHz	±6
MAX20403AFLD/VY+*	3.3	3.5	400kHz	±6
MAX20403AFLE/VY+	Adjustable 0.8V to 12V	3.5	2.1MHz	±6
MAX20403AFLH/VY+*	3.3	3.5	3MHz	±6

** Future part—contact factory for availability.*
+ Denotes a lead(Pb)-free/RoHS-compliant package.
T Denotes tape-and-reel.

/VY+ Denotes a side-wettable, automotive-qualified package.
Contact factory for options that are not included.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/22	Initial release	—
1	4/22	Updated Absolute Maximum Ratings, Applications Information, and Ordering Information	3, 13, 14, 18
2	5/22	Updated Ordering Information	18
3	6/22	Updated Ordering Information	18
4	7/22	Updated Ordering Information	18
5	9/22	Updated Ordering Information	18
6	11/22	Updated Simplified Block Diagram, Electrical Characteristics, Typical Operating Characteristics, Detailed Description, and Ordering Information	2, 4, 6, 13, 19
7	3/23	Updated Ordering Information	19
8	4/23	Updated Ordering Information	19
9	7/23	Updated Package Information and Typical Operating Characteristics	3, 9
10	10/23	Updated title, General Description, and Benefits and Features	1

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Analog Devices Inc.:

MAX20402AFLC/VY+ MAX20402AFLC/VY+T MAX20402AFLD/VY+ MAX20402AFLD/VY+T

Other:

MAX20402AFLE/VY+ MAX20402AFLE/VY+T MAX20402AFLF/VY+ MAX20402AFLF/VY+T MAX20402AFLB/VY+ MAX20402AFLA/VY+T MAX20402AFLA/VY+ MAX20402AFLB/VY+T