MAX20356

Wearable Power-Management Solution

General Description

The MAX20356 is a highly integrated and programmable power-management solution designed for ultra-low-power wearable applications. It is optimized for size and efficiency to enhance the value of the end product by extending battery life and shrinking the overall solution size. A flexible set of power-optimized voltage regulators including multiple buck converters, a buck-boost converter, and linear regulators provide a high level of integration and the ability to create a fully optimized power architecture. The quiescent current of each regulator is ultra-low to extend battery life in always-on applications.

The MAX20356 includes a complete battery-management solution with battery seal, charger, power path, and fuel gauge. Both thermal management and input protection are built into the charger. The device also includes a factory-programmable button controller with multiple inputs that are customizable to fit specific product user requirements.

A low-noise, 1.5W buck-boost converter provides highly efficient and clean power conversion required for the LEDs used in optical heart-rate systems such as PPG and SPO_2 measurements. The MAX20356 is also equipped with a nano I_Q fast transient LDO, optimized for use in analog front-end (AFE) sensors. The MAX20356 is configurable through an I^2C interface that allows for programming various functions and reading the device status, including the ability to read temperature and supply voltages through the monitor multiplexer.

The MAX20356 is available in a 63-bump, 0.5mm pitch, 3.71mm x 4.48mm, wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- Wearable Devices
- IoT

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Bluetooth is a registered trademark of Bluetooth SIG, Inc.

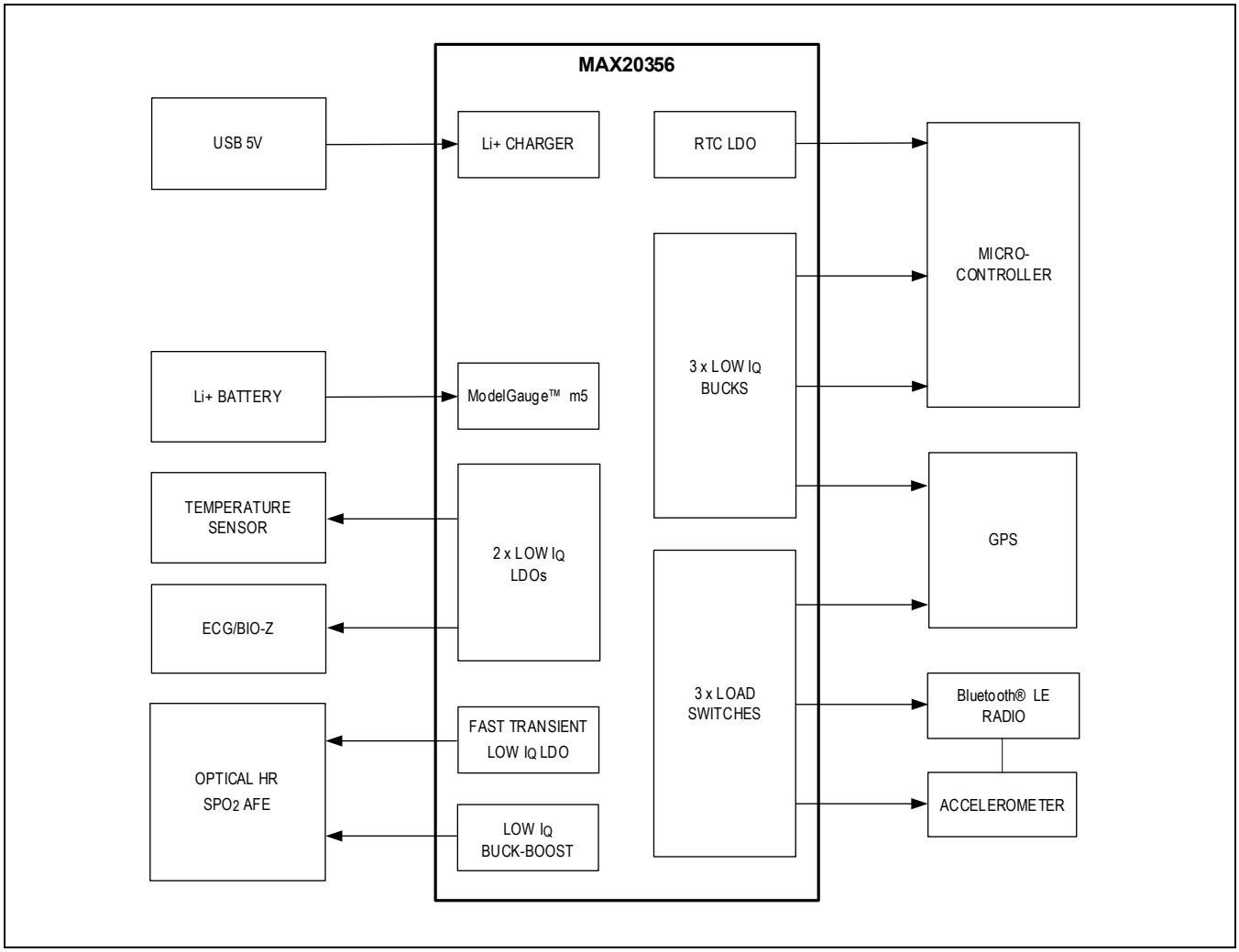
Benefits and Features

- Extend Time Between Charges
  - 3 x Nano-I_Q, 400mA Buck Regulators (I_Q = 400nA typ)
    - 0.500V to 1.130V in 10mV Steps
    - 0.500V to 2.075V in 25mV Steps
    - 0.500V to 3.650V in 50mV Steps
  - 2 x Micro-I_Q LDO/Load Switches (I_Q = 1µA typ)
    - 1.71V to 5.5V Input-Voltage Range
    - 100mA Output-Current Capability
    - 0.900V to 4.0V in 100mV Steps
  - Nano-I_Q Fast Transient LDO (I_Q = 820nA typ)
    - Optimized for use with Sensor AFEs
    - 1.71V to 5.5V Input-Voltage Range
    - 100mA Output-Current Capability
    - 0.900V to 4.075V in 25mV Steps
  - Nano-I_Q Real-Time Clock LDO (I_Q = 200nA typ)
    - Always-On Configurable for RTCs in µC Timers
    - 1.2V [+25mV, +50mV] and 1.8V [+25mV, +50mV]
  - Micro-I_Q Buck-Boost Regulator (I_Q = 2µA typ)
    - 1.5W Output
    - 2.6V to 5.5V in 50mV Steps
    - Dynamic Voltage Scaling
  - 3 x Nano-I_Q, Low On-Resistance Load Switches (I_Q = 260nA typ)
    - Low 0.25Ω (typ) On-Resistance
    - Short-Circuit Protection
    - Soft-Start Feature
- Easy-to-Implement Li+ Battery Charging
  - Wide Fast Charge Current Range: 4mA to 500mA
  - +28V/-5.5V Tolerant Input
  - Programmable JEITA Current/Voltage Profiles
  - Programmable Automatic Step-Charging
- Seamless Interaction with MAX20361 Solar Energy Harvester
- Multiple-Purpose Control Pins are Provided for Flexible Control
- Minimize Solution Footprint Through High Integration
  - Programmable Push-Button Controller
  - Programmable Supply Sequencing
  - Battery Seal Shipping Mode
  - On-Chip Voltage/Charge Current Monitor Mux

Ordering Information ***appears at end of data sheet.***

19-101659; Rev 2; 6/24

Simplified Block Diagram



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Absolute Maximum Ratings

CHGIN ..... -6.0V to +30.0V

CHGIN (factory mode) .....0V to +6V

SYSBK_, SYSBB, SYS, CHGOUT, SDA, SCL, IVMON, $\overline{RST}$, $\overline{INT}$, PFN_, L_IN, LSW_IN, BBOUT, BAT ..... -0.3V to +6.0V

MPC_ .....-0.3V to min(6V, V_{BK1OUT} + 0.3V)

THM ..... -0.3V to +2.2V

$\overline{ALRT}$ ..... -0.3V to +17.0V

CAP ..... -0.3V to min ($|V_{CHGIN}|$ + 0.3V, +6.0V)

VDIG, RTC_LDO..... -0.3V to +2.2V

BK_LX, BK_OUT..... -0.3V to min (6V, $V_{SYSBK\_}$ + 0.3V)

BBLVLX..... -0.3V to min (6V, V_{SYSBB} + 0.3V)

BBHVLX ..... -0.3V to min (V_{BBOUT} + 0.3V, +6.0V)

L_OUT..... -0.3V to min (6V, V_{L_IN} +0.3V)

LSW_OUT..... -0.3 to min (6V, V_{LSW_IN} + 0.3V)

BK_GND, BBGND, AGND, DGND, GSUB ..... -0.3V to +0.3V

RSN/CSN, CSP/FG_TST, RSP, RSP_S-0.3V to min (6V, V_{BAT} + 0.3V)

Continuous Current into BAT, RSN/CSN, RSP (DC current,100% utilization)..... 0.76A

Continuous Current into BAT, RSN/CSN, RSP (DC current, 10% utilization) 1.7A

Continuous Current into RSP_S.....-100mA to +100mA

Continuous Current into BK_OUT, BK_LX, BBLVLX, BBHVLX, BBOUT..... ±560mA

Continuous Current into L_IN, L_OUT ..... ±250mA

Continuous Current into LSW_IN, LSW_OUT..... ±140mA

Continuous Current into SYS, CHGIN, CHGOUT 1.52A

Continuous Current into Any Other Terminal ..... ±100mA

Continuous Power Dissipation (multilayer board) (T_A = +70°C, derate 31.41mW/°C above +70°C)..... 2513mW

Operating Temperature Range..... -40°C to +85°C

Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +150°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

63 WLP

Package Code	W633A4+1
Outline Number	*21-100616*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	31.83°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL SUPPLY CURRENT						
CHGIN Input Current	I_{CHGIN}	V_{CHGIN} = 5V, on mode, charger enabled, ChgAutoStop = 0, I_{CHGOUT} = 0, I_{SYS} = 0, THM monitoring disabled, RTC LDO enabled, all other rails disabled		0.54		mA
		Factory mode 1, CHGIN = 5V, all regulators and load switches off		440		µA
		Factory mode 2, CHGIN = 5V, all regulators and load switches off		75.0		
BAT Input Current	I_{BAT}	Seal mode, RTC LDO disabled		0.28		µA
		Off mode, RTC LDO enabled, fuel gauge shutdown		1.26		
		Battery recovery (BR) mode, RTC LDO enabled, fuel gauge shutdown		1.51		µA
		V_{CHGIN} = 0V, on mode, RTC LDO enabled, all other rails disabled, fuel gauge shutdown		1.67		µA
		V_{CHGIN} = 0V, on mode, RTC LDO enabled, Buck1 enabled, fuel gauge shutdown		2.00		
		V_{CHGIN} = 0V, on mode, RTC LDO enabled, Buck1 and Buck2 enabled, fuel gauge shutdown		2.30		
		V_{CHGIN} = 0V, on mode, RTC LDO enabled, Buck1, Buck2, and Buck3 enabled, fuel gauge shutdown		2.61		
INTERNAL SUPPLIES, UVLOS, AND BAT OCP						
V_{CCINT} OTP OK Threshold/Start-Up Voltage	$V_{CCINT\_OTP\_OK}$	V_{CCINT} falling (*Note 2*)	2.60	2.90		V
		V_{CCINT} rising (*Note 2*)		2.92	3.25	
V_{DIG} OTP OK Threshold	$V_{DIG\_OTP\_OK}$	V_{DIG} falling	1.41	1.51		V
		V_{DIG} rising		1.52	1.62	
V_{CCINT} UVLO Threshold (POR)	V_{CCINT_UVLO}	V_{CCINT} falling (*Note 2*)	2.15	2.40	2.7	V
		V_{CCINT} rising (*Note 2*)	2.2	2.45	2.75	
V_{CCINT} UVLO Threshold (POR) Hysteresis	$V_{CCINT\_UVLO\_H}$	(*Note 2*)		50		mV
BAT UVLO Threshold	$V_{BAT\_UVLO\_R}$	V_{BAT} rising, valid only when CHGIN is present		2.25	2.28	V
	$V_{BAT\_UVLO\_F}$	V_{BAT} falling, valid only when CHGIN is present	2.16	2.22		
BAT Pull-Down Resistance	R_{BAT_PD}	BattPullDown = 1		15		kΩ
Internal V_{DIG} Regulator	V_{DIG}		1.71	1.80	1.89	V
V_{DIG} UVLO Threshold	V_{DIG_UVLO}	V_{DIG} falling	1.51		1.61	V

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		V_{DIG} rising		1.59		1.73	
V_{DIG} UVLO Threshold Hysteresis	$V_{DIG\_UVLO\_H}$				100		mV
Internal CAP Regulator	V_{CAP}	V_{CHGIN} = 4.3V to 28.0V		3.75	4.10	4.55	V
CAP Detect Threshold	V_{CAP_DET}	V_{CHGIN} = V_{CAP} falling		2.60	2.80	3.00	V
		V_{CHGIN} = V_{CAP} rising		3.15	3.4	3.6	
CAP Detect Threshold Hysteresis	$V_{CAP\_DET\_H}$				600		mV
CHGIN Detect Threshold	V_{CHGIN_DET}	V_{CHGIN} rising		4.00	4.15	4.30	V
		V_{CHGIN} falling		3.20	3.30	3.40	
CHGIN Detect Threshold Hysteresis	$V_{CHGIN\_DET\_H}$				850		mV
CHGIN Detection Debounce Time	t_{CHGIN_DET}	CHGIN detachment			100		ms
		CHGIN insertion			108		
SYS UVLO Threshold	V_{SYS_UVLO}	V_{SYS} rising, SysUVLOThSel = 00		2.65	2.75	2.85	V
		V_{SYS} falling, SysUVLOThSel = 00		2.60	2.70	2.80	
		V_{SYS} falling, SysUVLOThSel = 01		2.80	2.90	3.00	
		V_{SYS} falling, SysUVLOThSel = 10		2.90	3.00	3.10	
		V_{SYS} falling, SysUVLOThSel = 11		3.10	3.20	3.30	
SYS UVLO Threshold Hysteresis	$V_{SYS\_UVLO\_H}$				50		mV
SYS UVLO Falling Debounce Time	$t_{SYS\_UVLO\_FD}$	V_{SYS} falling			20		µs
BAT OCP Threshold	I_{BAT_OCP}	I_{SYS} rising	IBatOc = 000		200		mA
			IBatOc = 001		400		
			IBatOc = 010		600		
			IBatOc = 011	480	800	1120	
			IBatOc = 100	600	1000	1400	
			IBatOc = 101	720	1200	1680	
			IBatOc = 110	840	1400	1960	
			IBatOc = 111	960	1600	2240	
BAT OCP Threshold Hysteresis	$I_{BAT\_OCP\_H}$				15		%
BAT OCP Rising Debounce Time	$t_{BAT\_OCP\_RD}$	I_{SYS} rising			50		ms
SYS Pull-Down Resistance	R_{SYS_PD}	Enabled for t_{SYS_PD} when transitioning towards battery recovery (BR) mode			10		Ω
SYS Pull-Down Time	t_{SYS_PD}	R_{SYS_PD} is enabled on SYS for this time when transitioning towards battery recovery (BR) mode			30		ms
OVP AND INPUT CURRENT LIMITER							
CHGIN Overvoltage Threshold	V_{CHGIN_OV}	V_{CHGIN} rising		7.2	7.5	7.8	V

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_H}$				200		mV
CHGIN-SYS Valid Trip Point	$V_{CHGIN\_SYS\_TP}$	V_{CHGIN} - V_{SYS} rising		30	145	290	mV
CHGIN-SYS Valid Trip Point Hysteresis	$V_{CHGIN\_SYS\_TP\_H}$				275		mV
Input Current Limit	I_{LIM}	ILimCntl = 000			90		mA
		ILimCntl = 001			150		
		ILimCntl = 010			200		
		ILimCntl = 011			300		
		ILimCntl = 100			400		
		ILimCntl = 101		400	450	500	
		ILimCntl = 110			1000		
		ILimCntl = 111			1500		
Input Overcurrent Max Limit	I_{LIM_MAX}	t < t_{ILIM_BLANK}, ILimMax = 000			90		mA
		t < t_{ILIM_BLANK}, ILimMax = 001			150		
		t < t_{ILIM_BLANK}, ILimMax = 010			200		
		t < t_{ILIM_BLANK}, ILimMax = 011			300		
		t < t_{ILIM_BLANK}, ILimMax = 100			400		
		t < t_{ILIM_BLANK}, ILimMax = 101		400	450	500	
		t < t_{ILIM_BLANK}, ILimMax =110			1000		
		t < t_{ILIM_BLANK}, ILimMax = 111			1500		
Input Current-Limit Blanking Time	t_{ILIM_BLANK}	ILimBlank = 00			50		µs
		ILimBlank = 01			0.5		ms
		ILimBlank = 10			1.0		
		ILimBlank = 11			10		
SYS Regulation-Voltage Dropout	$V_{CHGIN\_SYS\_REG}$				70		mV
SYS Regulation Voltage	V_{SYSMIN_REG}	V_{BAT} < SysMinVlt[3:0] - SYSDrp[1:0] - SysOVD[1:0] and SysMinVlt[3:0] = 0000 to 1111			3.3 to 4.8, step 0.1		V
	$V_{SYS-CHGOUT\_REG}$	V_{BAT} > SysMinVlt[3:0] - SYSDrp[1:0] - SysOVD[1:0]			SYSDrp[1:0] + SysOVD[1:0]		
SYS Regulation Voltage Overhead	V_{SYS_OVHD}	Additional to SYSDrp[2:0]	SysOVD[1:0] = 00		175		mV
			SysOVD[1:0] = 01		200		
			SysOVD[1:0] = 10		225		
			SysOVD[1:0] = 11		250		
CHGIN to SYS On Resistance	R_{CHGIN_SYS}	CHGIN = 5V, I_{SYS} = 200mA			0.16	0.28	Ω

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current Soft-Start Time	t_{ILIM_SFT}				1		ms
Thermal-Shutdown Temperature	T_{CHG_SHDN}	40°C + 5°C x ChgThrmLim[3:0]	ChgThrmLim = 0000		40		°C
		ChgThrmLim = 1111			115		
CHGIN Boot Retry Timeout	$t_{CHG\_RETRY\_TMO}$	ChgAlwTry = 1, (see *Table 6*)			0.5		s
BATTERY CHARGER							
SYS to CHGOUT On Resistance	R_{CHG}	V_{CHGOUT} = 4.35V, I_{CHGOUT} = 1000mA			50	75	mΩ
SYS to CHGOUT Charge Current Reduction Threshold	$V_{SYS\_CHGOUT\_LIM}$	Measured as V_{SYS} - V_{CHGOUT}, V_{CHGOUT} = 3.6V	SYSDrp[2:0] = 000		25		mV
			SYSDrp[2:0] = 001		37.5		
			SYSDrp[2:0] = 010		50		
			SYSDrp[2:0] = 011		62.5		
			SYSDrp[2:0] = 100		75		
			SYSDrp[2:0] = 101		87.5		
			SYSDrp[2:0] = 110		100		
			SYSDrp[2:0] = 111		112.5		
Precharge Current	I_{PCHG}	IPChg = 00			0.05 x I_{FCHG2}		mA
		IPChg = 01		0.0795 x I_{FCHG2}	0.10 x I_{FCHG2}	0.1075 x I_{FCHG2}	
		IPChg = 10			0.20 x I_{FCHG2}		
		IPChg = 11			0.30 x I_{FCHG2}		
Precharge Threshold	V_{BAT_PCHG}	V_{BAT} rising	VPChg = 000		2.7		V
			VPChg = 001		2.8		
			VPChg = 010		2.9		
			VPChg = 011		3		
			VPChg = 100		3.1		
			VPChg = 101		3.2		
			VPChg = 110		3.3		
			VPChg = 111		3.4		
Precharge Threshold Hysteresis	$V_{BAT\_PCHG\_H}$				100		mV
Step Charge Threshold	V_{BAT_STPCHG}	V_{BAT} rising	ChgStepRise = 0000		3.80		V
			ChgStepRise = 0001		3.85		
			ChgStepRise = 0010		3.90		
			ChgStepRise = 0011		3.95		

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			ChgStepRise = 0100		4.00		
			ChgStepRise = 0101		4.05		
			ChgStepRise = 0110		4.1		
			ChgStepRise = 0111		4.15		
			ChgStepRise = 1000		4.2		
			ChgStepRise = 1001		4.25		
			ChgStepRise = 1010		4.3		
			ChgStepRise = 1011		4.35		
			ChgStepRise = 1100		4.4		
			ChgStepRise = 1101		4.45		
			ChgStepRise = 1110		4.5		
			ChgStepRise = 1111		4.55		
Step Charge Threshold Hysteresis	$V_{BAT\_STPCHG\_H}$	ChgStepHyst = 000			100		mV
		ChgStepHyst = 001			200		
		ChgStepHyst = 010			300		
		ChgStepHyst = 011			400		
		ChgStepHyst = 100			500		
		ChgStepHyst = 101			600		
		ChgStepHyst = 110			600		
		ChgStepHyst = 111			600		
Fast Charge Current Zone 1	I_{FCHG1}	V_{SYS} - V_{BAT} = 1.5V			4 to 130, step 2		mA
		V_{SYS} - V_{BAT} = 1.5V			140 to 500, step 10		
Fast Charge Current Zone 2	I_{FCHG2}	V_{SYS} - V_{BAT} = 1.5V			4 to 130, step 2		mA
		V_{SYS} - V_{BAT} = 1.5V			140 to 500, step 10		
Battery Regulation Voltage Accuracy	$V_{BAT\_REG\_ACC}$	ChgBatReg = 000000 to 111111		-0.5%		+0.5%	V
Battery Recharge Threshold	V_{BAT_RECHG}	Charger recharge threshold in relation to ChgBatReg[5:0].	BatReChg = 00		V_{BAT_REG} - 50		mV
			BatReChg = 01		V_{BAT_REG} - 100		

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			BatReChg = 10		V_{BAT_REG} - 150		
			BatReChg = 11		V_{BAT_REG} - 200		
Maximum Precharge Time	t_{PCHG}	PChgTmr = 00			30		min
		PChgTmr = 01			60		
		PChgTmr = 10			120		
		PChgTmr = 11			240		
Maximum Fast Charge Zone 1 Time	t_{FCHG1}	CC1FChgTmr = 00			30		min
		CC1FChgTmr = 01			60		
		CC1FChgTmr = 10			120		
		CC1FChgTmr = 11			240		
Global Charge Time	t_{CHG}	ChgTmr = 00			75		min
		ChgTmr = 01			150		
		ChgTmr = 10			300		
		ChgTmr = 11			600		
Charge Done Qualification	I_{CHG_DONE}	IChgDone = 00			0.025 x I_{FCHG2}		mA
		IChgDone = 01			0.050 x I_{FCHG2}		
		IChgDone = 10		0.095323 x I_{FCHG2}	0.100 x I_{FCHG2}	0.105357 x I_{FCHG2}	
		IChgDone = 11			0.200 x I_{FCHG2}		
Maximum Maintain Charge Time	t_{MTCHG}	MtChgTmr = 00			0		min
		MtChgTmr = 01			15		
		MtChgTmr = 10			30		
		MtChgTmr = 11			60		
Timer Accuracy	t_{CHG_ACC}			-10		+10	%
Fast-Charge Timer Extend Current Threshold	I_{FCHG_TEXT}	*Figure 29*			50		% $I_{FCHG1,2}$
Fast-Charge Timer Suspend Current Threshold	I_{FCHG_TSUS}	*Figure 29*			20		% $I_{FCHG1,2}$
Battery Regulation Voltage Reduction Due to Thermistor Temperature	$V_{BAT\_REG\_JTA}$	Chg_BatReg = 00			V_{BAT_REG} - 0.15		V
		Chg_BatReg = 01			V_{BAT_REG} - 0.1		
		Chg_BatReg = 10			V_{BAT_REG} - 0.05		
		Chg_BatReg = 11			V_{BAT_REG}		

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fast-Charge Current Reduction Due to Thermistor Temperature	I_{FCHG_JTA}	$I_{FCHG\_}$ = I_{FCHG1} or I_{FCHG2} based on step charge comparator status	Chg_CC_IFChg = 000		0.20 x $I_{FCHG\_}$		mA
			Chg_CC_IFChg = 001		0.30 x $I_{FCHG\_}$		
			Chg_CC_IFChg = 010		0.40 x $I_{FCHG\_}$		
			Chg_CC_IFChg = 011		0.50 x $I_{FCHG\_}$		
			Chg_CC_IFChg = 100		0.60 x $I_{FCHG\_}$		
			Chg_CC_IFChg = 101		0.70 x $I_{FCHG\_}$		
			Chg_CC_IFChg = 110		0.80 x $I_{FCHG\_}$		
			Chg_CC_IFChg = 111		$I_{FCHG\_}$		
POWER PATH (CHGOUT to SYS)							
CHGOUT to SYS On Resistance	R_{PP}	V_{CHGOUT} = 4.35V, I_{SYS} = 1000mA, LDO disabled			50	75	mΩ
CHGOUT to SYS On Threshold	$V_{CHGOUT\_SYS\_ON}$	V_{CHGOUT} = 4.35V, I_{SYS} = 10mA, measured as V_{CHGOUT} - V_{SYS}, PPDrp[1:0] = 00			25		mV
		V_{CHGOUT} = 4.35V, I_{SYS} = 10mA, measured as V_{CHGOUT} - V_{SYS}, PPDrp[1:0] = 01			37.5		
		V_{CHGOUT} = 4.35V, I_{SYS} = 10mA, measured as V_{CHGOUT} - V_{SYS}, PPDrp[1:0] = 10			50		
		V_{CHGOUT} = 4.35V, I_{SYS} = 10mA, measured as V_{CHGOUT} - V_{SYS}, PPDrp[1:0] = 11			62.5		
THERMISTOR MONITOR							
THM Hot Threshold	V_{THM_HOT1}	V_{THM} falling (+70ºC)		16.36	18.36	20.36	$\%V_{DIG}$
	V_{THM_HOT2}	V_{THM} falling (+65ºC)		18.7	20.7	22.7	
	V_{THM_HOT3}	V_{THM} falling (+60ºC)		21.44	23.44	25.44	
	V_{THM_HOT4}	V_{THM} falling (+55ºC)		24.17	26.17	28.17	
	V_{THM_HOT5}	V_{THM} falling (+50ºC)		27.3	29.3	31.3	
	V_{THM_HOT6}	V_{THM} falling (+45ºC)		30.81	32.81	34.81	
	V_{THM_HOT7}	V_{THM} falling (+40ºC)		34.72	36.72	38.72	
	V_{THM_HOT8}	V_{THM} falling (+35ºC)		39.02	41.02	43.02	
THM Warm Threshold	V_{THM_WARM1}	V_{THM} falling (+55ºC)		24.17	26.17	28.17	$\%V_{DIG}$
	V_{THM_WARM2}	V_{THM} falling (+50ºC)		27.3	29.3	31.3	
	V_{THM_WARM3}	V_{THM} falling (+45ºC)		30.81	32.81	34.81	
	V_{THM_WARM4}	V_{THM} falling (+40ºC)		34.72	36.72	38.72	
	V_{THM_WARM5}	V_{THM} falling (+35ºC)		39.02	41.02	43.02	

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	V_{THM_WARM6}	V_{THM} falling (+30ºC)	43.31	45.31	47.31	
	V_{THM_WARM7}	V_{THM} falling (+25ºC)	48	50	52	
	V_{THM_WARM8}	V_{THM} falling (+20ºC)	52.69	54.69	56.69	
THM Cool Threshold	V_{THM_COOL1}	V_{THM} rising (+25ºC)	48	50	52	$\%V_{DIG}$
	V_{THM_COOL2}	V_{THM} rising (+20ºC)	52.69	54.69	56.69	
	V_{THM_COOL3}	V_{THM} rising (+15ºC)	57.77	59.77	61.77	
	V_{THM_COOL4}	V_{THM} rising (+10ºC)	62.45	64.45	66.45	
	V_{THM_COOL5}	V_{THM} rising (+5ºC)	67.14	69.14	71.14	
	V_{THM_COOL6}	V_{THM} rising (0ºC)	71.83	73.83	75.83	
	V_{THM_COOL7}	V_{THM} rising (-5ºC)	76.13	78.13	80.13	
	V_{THM_COOL8}	V_{THM} rising (-10ºC)	80.03	82.03	84.03	
THM Cold Threshold	V_{THM_COLD1}	V_{THM} rising (+15ºC)	57.77	59.77	61.77	$\%V_{DIG}$
	V_{THM_COLD2}	V_{THM} rising (+10ºC)	62.45	64.45	66.45	
	V_{THM_COLD3}	V_{THM} rising (+5ºC)	67.14	69.14	71.14	
	V_{THM_COLD4}	V_{THM} rising (0ºC)	71.83	73.83	75.83	
	V_{THM_COLD5}	V_{THM} rising (-5ºC)	76.13	78.13	80.13	
	V_{THM_COLD6}	V_{THM} rising (-10ºC)	80.03	82.03	84.03	
	V_{THM_COLD7}	V_{THM} rising (-15ºC)	83.16	85.16	87.16	
	V_{THM_COLD8}	V_{THM} rising (-20ºC)	86.28	88.28	90.28	
THM Disable Threshold	V_{THM_DIS}	V_{THM} rising	91.75	93.75	95.75	$\%V_{DIG}$
THM Threshold Hysteresis	V_{THM_H}			60		mV
THM Input Leakage	I_{THM_LK}	V_{THM} = 0V to 5.5V, JEITA disabled	-1		+1	µA
HARVESTER INTERACTION						
Harvester Interaction Ideal CHGOUT to SYS Diode Quiescent Current	$I_{HARV\_CHGOUT\_SYS\_DIO\_Q}$	V_{CHGOUT} = 4.35V, I_{SYS} = 0µA		0.65		µA
		V_{CHGOUT} = 4.35V, I_{SYS} = 10mA		12		
Harvester Interaction SYS to CHGOUT Diode Drop In POR/Seal Mode	$V_{HARV\_SYS\_CHGOUT\_DIO\_PORSEAL}$	POR condition, V_{CHGOUT} = 2.1V, I_{SYS} = -20mA		0.6		V
Harvester Interaction Ideal CHGOUT-to-SYS Diode Regulation	$V_{HARV\_CHGOUT\_SYS\_DIO\_REG}$	V_{CHGOUT} = 4.35V, I_{SYS} = 100mA, measured as V_{CHGOUT} - V_{SYS}		28		mV
Harvester Interaction Ideal CHGOUT-to-SYS Diode Load Transient	$V_{HARV\_CHGOUT\_SYS\_DIO\_LOADTRAN}$	V_{CHGOUT} = 4.35V, I_{SYS} from -20mA to 1A in 1µs, measured as V_{CHGOUT} - V_{SYS}		165		mV
Harvester Interaction Ideal CHGOUT-to-SYS Diode Release Delay	$t_{HARV\_CHGOUT\_SYS\_DIO\_REL}$	V_{CHGOUT} = 4.35V, I_{SYS} = from 1A to -1mA in 1µs, measured as the time from when I_{CHGOUT} goes negative to when it rises above -50µA		110		µs
IVMON MULTIPLEXER						

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IVMON Multiplexer Output Ratio	$V_{IVMON\_DIV\_RT}$	No load on IVMON pin. Inputs: charger current, BAT, SYS, THM, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, RTC_LDO, BBOUT (*Note 3*)	MONRatioCfg = 00		100.0		%
		No load on IVMON pin. Inputs: charger current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, RTC_LDO, BBOUT	MONRatioCfg = 01		50.0		
			MONRatioCfg = 10		33.3		
			MONRatioCfg = 11		25.0		
IVMON Multiplexer Output Impedance	R_{IVMON_DIV}	Inputs charger current, BAT, SYS, BK1OUT, BK2OUT, BK3OUT, L1OUT, L2OUT, L3OUT, RTC_LDO, BBOUT,1µA load on IVMON pin	MONRatioCfg = 00		5.5		kΩ
			MONRatioCfg = 01		31.0		
			MONRatioCfg = 10		28.0		
			MONRatioCfg = 11		24.0		
IVMON Input Leakage	I_{IVMON_LK}	IVMON multiplexer disabled, pull-down resistance disabled, V_{IVMON} = 0V to 5.5V		-1		+1	µA
IVMON Multiplexer Off-State Pull-Down Resistance	R_{IVMON_OFF}	IVMON multiplexer disabled, pull-down resistance enabled			59.0		kΩ
BUCK1, BUCK2, AND BUCK3							
Input-Voltage Range	V_{IN}	Input voltage = V_{SYS}		2.7		5.5	V
Output-Voltage Range	V_{BK_OUT}	10mV step resolution		0.500		1.130	V
		25mV step resolution		0.500		2.075	
		50mV step resolution		0.500		3.650	
Quiescent-Supply Current	I_{Q_BK}	I_{BK_OUT} = 0, V_{SYS} = 3.7V, V_{BK_OUT} = 1.2V, Buck_VStep = 25mV, Buck_FPWM = 0, L = 2.2µH, Buck_ISet = 175mA			0.40	0.70	µA
	$I_{Q\_BK\_PWM}$	I_{BK_OUT} = 0, V_{SYS} = 3.7V, V_{BK_OUT} = 1.2V, Buck_VStep = 25mV, Buck_FPWM = 1, L = 2.2µH, Buck_ISet = 175mA			2.00		mA
Output Average Voltage Accuracy	ACC_BK	Buck_EnbINTGR = 0, CCM operation, V_{BK_OUT} ≤ 3.4V		-2.5		+2.5	%
Peak-to-Peak Voltage Ripple	V_{RPP_BK}	$C_{BK\_OUT\_EFF}$ ≥ 4µF, I_{BK_OUT} = 1mA, L = 2.2µH, Buck_Iset = 150mA, V_{OUT} = 1.2V, V_{SYS} = 3.7V			10		mV
Nominal Peak Current Set Range	I_{PSET_BK}	25mA step resolution		0		375	mA

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Transient Response	$V_{LOAD\_TRANS\_BK}$	10µA to 300mA at 1A/µs, C_{BK_EFF} = 9µF, V_{BK_OUT} = 1.2V		77		mV
Load Regulation Error	$V_{LOAD\_REG\_BK\_}$	Buck_EnbIADPT = 0, Buck_EnbINTGR = 0, I_{BK_OUT} = 500mA		-0.55		%
Line Regulation Error	$V_{LINE\_REG\_BK\_}$	V_{BK_OUT} = 1.2V, V_{SYS} from 2.7V to 5.5V, I_{BK_OUT} = 200mA, C_{BK_OUT} > 9µF		±5.5		mV
Maximum Operative Output Current	I_{BK_MAX}	Load regulation error = -5%, Buck_EnbINTGR = 0	400			mA
Valley Current Limit During Short-Circuit to GND	I_{SHRT_BK}	V_{BK_OUT} = 0V		0.7		A
Valley Current Limit During Start-Up	$I_{VLY\_BK\_STUP}$	During start-up before PGOOD = 1 condition is achieved		125		mA
BKLX Leakage Current	I_{LK_BKLX}	Buck_ disabled	-1		+1	µA
Active Discharge Current	I_{ACTD_BK}	V_{BK_OUT} = 0.7V	8	16	28	mA
Passive Discharge Resistance	R_{PSV_BK}		5	10	15.5	kΩ
Full Turn-On Time	t_{ON_BK}	Time from enable to PGOOD and full current capability, no load		10		ms
Efficiency	EFFIC_BK	Buck_VSet = 1.2V, I_{BK_OUT} = 10mA, Inductor: Murata DFE201610E-2R2M		86		%
BKLX Rising/Falling Slew Rate	SLW_BK	Buck_LowEMI = 0		3.0		V/ns
	SLW_BK_L	Buck_LowEMI = 1		0.6		
Thermal-Shutdown Threshold	T_{SHDN_BK}	I_{LOAD} > 20mA		140		°C
PGOOD Threshold % Shift vs. Nominal Regulation Point	V_{TH_PGOOD}		-7	-5	-3	%
LDO1, LDO2 (TYPICAL VALUES ARE AT V_{L_IN} = +3.7V, V_{L_OUT} = +3V)						
Input Voltage	$V_{IN\_LDO\_}$	LDO mode	1.71		5.5	V
Input Voltage	$V_{IN\_LDO\_}$	Switch mode	1.2		5.5	V
Quiescent-Supply Current	$I_{Q\_LDO\_}$	LDO_ enabled, I_{L_OUT} = 0µA		1.0	1.9	µA
Quiescent Supply Current Room Temperature	$I_{Q\_LDO\_27C}$	LDO_ enabled, I_{L_OUT} = 0µA, T_A = +27ºC		1	1.4	µA
Quiescent-Supply Current	$I_{Q\_LDO\_SW\_}$	LDO_ enabled, I_{L_OUT} = 0µA, switch mode		0.35	0.9	µA
Quiescent-Supply Current in Dropout	$I_{Q\_LDO\_D\_}$	I_{L_OUT} = 0µA, V_{L_IN} = 2.9V, LDO_VSet = +3V		1.9	3.7	µA
Maximum Output Current	$I_{L\_OUT\_MAX}$	V_{L_IN} > 1.8V	100			mA
		V_{L_IN} ≤ 1.8V	50			
Maximum Output Current When Supplied From V_{CCINT}	$I_{LDO1\_MAX\_VCCINT}$	LDO1 only, V_{BAT} > 3.2V, V_{L1OUT} = 1.8V, LDO1INT_SUP = 1 (internal)	100			µA

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Internal Supply Switch	R_{ON_L1IN}	LDO1INT_SUP = 1 (internal), switch between V_{CCINT} and L1IN		4.5	7.3	12	kΩ
Output-Voltage Range	V_{L_OUT}	100mV step resolution		0.9		4	V
Output-Voltage Accuracy	ACCLDO_	V_{L_IN} = max(V_{L_OUT} + 0.5V, 1.71V) or higher, I_{L_OUT} = 1mA		-2.5		+2.5	%
Dropout Voltage	$V_{DROP\_LDO\_}$	V_{L_IN} = 1.85V, LDO_VSet = 1.9V, I_{L_OUT} = 100mA				130	mV
		V_{L_IN} = 3V, LDO_VSet = 3.1V, I_{L_OUT} = 100mA				100	
Line-Regulation Error	$V_{LINEREG\_LDO\_}$	V_{L_IN} = (V_{L_OUT} + 0.5V) to 5.5V, V_{L_IN} ≥ 1.8V, I_{L_OUT} = 100mA		-0.4		0.4	%/V
Load-Regulation Error	$V_{LOADREG\_LDO\_}$	1.8V ≤ V_{L_IN} ≤5.5V, I_{L_OUT} = 100µA to 100mA			0.002	0.007	%/mA
Line Transient	$V_{LINETRAN\_LDO\_}$	V_{L_IN} = 4V to 5V, 1µs rise time			±25		mV
		V_{L_IN} = 4V to 5V, 200ns rise time			±35		
Load Transient	$V_{LOADTRAN\_LDO\_}$	200ns rise time	I_{L_OUT} = 0mA to 10mA		100		mV
			I_{L_OUT} = 0mA to 100mA		200		
Passive Discharge Resistance	$R_{PD\_LDO\_}$			5	10	16	kΩ
Active Discharge Current	$I_{AD\_LDO\_}$	V_{L_IN} = 3.7V		8	22	40	mA
Switch-Mode Resistance	$R_{ON\_LDO\_SW\_}$	I_{L_OUT} = 5mA, switch mode	V_{L_IN} = 1.2V		1.5	2.3	Ω
	$R_{ON\_LDO\_SW\_1p8}$	I_{L_OUT} = 100mA, switch mode	V_{L_IN} = 1.8V		0.65	1	
	R_{ON_LDO}	I_{L_OUT} = 100mA, switch mode	V_{L_IN} = 2.7V		0.4	0.7	
Turn-On Time	$t_{ON\_LDO\_}$	I_{L_OUT} = 0mA, time from 10% to 95% of final value	LDO mode		1.5		ms
	$t_{ON\_LDO\_SW}$	I_{L_OUT} = 0mA, time from 10% to 95% of final value	Switch mode		0.26		
Short-Circuit Current Limit	$I_{SHRT\_LDO\_}$	V_{L_OUT} = GND	V_{L_IN} = 2.7V, Switch mode	210	350	540	mA
			V_{L_IN} = 5.5V	225	460	690	
Thermal-Shutdown Temperature	$T_{SHDN\_LDO\_}$				150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_LDO\_H}$				20		°C
L_IN UVLO	$V_{UVLO\_LDO\_}$	V_{L_IN} rising			1.36	1.71	V
		V_{L_IN} falling		1.05	1.35		
Output Leakage	$I_{LK\_L\_OUT}$	V_{L_OUT} = GND, LDO_ disabled		-1		+1	µA
Output-Voltage Noise	$V_{NOISE\_LDO\_}$	BW = 10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 3.3V			150		$µV_{RMS}$

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		BW = 10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 2.5V			125		
		BW = 10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 1.2V			90		
		BW = 10Hz to 100kHz, V_{L_IN} = 5V , V_{L_OUT} = 0.8V			80		
LDO3 (FAST TRANSIENT LDO)							
Input Voltage	V_{IN_LDO3}	LDO mode		1.71		5.5	V
Quiescent Supply Current	I_{Q_LDO3}	LDO3 enabled, I_{L3OUT} = 0µA, V_{L3IN} > V_{L3OUT} + 100mV			820	2400	nA
Quiescent Supply Current Room Temperature Only	$I_{Q\_LDO3\_27C}$	LDO enabled, I_{L3OUT} = 0µA, V_{L3IN} > V_{L3OUT} + 100mV, +27ºC			820	1400	nA
Quiescent Supply Current in Fast Mode	I_{q_FST}	LDO3 enabled, LDO3_FRC_HIC = 1, I_{L3OUT} = 0, V_{L3IN} > V_{L3OUT} +100mV			3.2	6	µA
Quiescent Supply Current in Dropout	$I_{Q\_LDO3\_D}$	I_{L3OUT} = 0µA, V_{L3IN} = 2.9V, LDO3VSet = +3V			16		µA
Maximum Output Current	I_{LOUT3_MAX}	V_{L3IN} > 2.0V, V_{L3IN} = (V_{L3OUT} + 0.1V) or higher		100			mA
		1.8V < V_{L3IN} < 2V, V_{L3IN} = (V_{L3OUT} + 0.1V) or higher		70			
		1.71V < V_{L3IN} ≤ 1.8V, V_{L3IN} = (V_{L3OUT} + 0.1V) or higher		40			
Output-Voltage Range	V_{L_OUT3}	25mV step resolution		0.9		4.075	V
Output-Voltage Accuracy	ACCLDO3	V_{L3IN} = (V_{L3OUT} + 0.5V) or higher, I_{L3OUT} = 5mA		-2.1		+2.1	%
Dropout Voltage	V_{DROP_LDO3}	V_{L3IN} = 1.8V, LDO3VSet = 1.9V, I_{L3OUT} = 70mA		24	54	84	mV
		V_{L3IN} = 2.9V, LDO3VSet = 3V, I_{L3OUT} = 100mA		20	41	60	
L3IN to L3OUT Dropout DRPLDO3 Bit Threshold	V_{THDRP}	LDO3VSET = 3V, I_{L3OUT} = 100mA, L3IN falling			42		mV
Line-Regulation Error	$V_{LINEREG\_LDO3}$	V_{L3IN} = (V_{L3OUT} + 0.5V) to 5.5V, V_{L3IN} ≥ 2.0V			20		m%/V
Load-Regulation Error	$V_{LOADREG\_LDO3}$	V_{L3IN} = V_{L3OUT} + 0.5V, I_{L3OUT} = 100µA to 100mA			0.001		%/mA
Line Transient	$V_{LINETRAN\_LDO3}$	V_{L3IN} = 4V to 5V, V_{L3OUT} = 1.8V, 1µs rise time			20		mV
		V_{L3IN} = 4V to 5V, 200ns rise time			25		
Load Transient	$V_{LOADTRAN\_LDO3}$	200ns rise time	I_{L3OUT} = 0mA to 10mA, C_{L3OUT} = 1µF, 1.8V output voltage		44		mV
			I_{L3OUT} = 0mA to 100mA, C_{L3OUT} = 1µF, 1.8V output voltage		168		

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load-Transient Recovery Time	$t_{Recovery}$	I_{L3OUT} from 0 to 2mA, t_{rise} = 1µs, C_{L3OUT} = 1µF, V_{L3OUT} = 1.8V, time to rise back to 0.2% of final regulation voltage (*Note 4*)		50	100	µs
		I_{L3OUT} from 0 to 100mA, rise time =1µs, C_{L3OUT} = 1µF, V_{L3OUT} = 1.8V, time to rise back to 0.2% of final regulation voltage		12		
Passive Discharge Resistance	R_{PD_LDO3}		5	10	16	kΩ
Active Discharge Current	I_{AD_LDO3}	V_{L3IN} = 3.7V	8	22	40	mA
Turn-On Time	t_{ON_LDO3}	I_{L3OUT} = 0mA, time from enable to 95% of final value and full output current capability, LDO3VSet = 1.8V, LDO mode		5		ms
L3OUT Start-Up Slew Rate	SLEW_LDO3		0.4	2.35	7	V/ms
Short-Circuit Current Hiccup Threshold	I_{SHRT_LDO3}	V_{L3IN} - V_{L3OUT} ≥ 1V	219	580	942	mA
Thermal-Shutdown Temperature	T_{SHDN_LDO3}			+140		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_LDO3\_H}$			20		°C
L3IN UVLO	V_{UVLO_LDO3}	V_{L3IN} rising			1.75	V
		V_{L3IN} falling	1.26		1.67	
Output Leakage	$I_{LK\_L\_OUT3}$	V_{L3OUT} = GND, LDO3 disabled	-1		+1	µA
Power-Supply Rejection Ratio	PSRR	f = 1kHz, I_{L3OUT} = 30mA		70		dB
Output-Voltage Noise	V_{NOISE_LDO3}	BW = 10Hz to 100kHz, V_{L3OUT} = 0.9V, I_{L3OUT} = 30mA		64		µV RMS
RTC_LDO						
Input Voltage	V_{IN_RTC}		2.7		5.5	V
Quiescent Current	I_{Q_RTC}			200	410	nA
Max Output Current	I_{MAX_RTC}	V_{RTC_LDO} = 80% of the nominal value	2			mA
Output Voltage	V_{OUT_RTC}	LDO4VSet = 1.2V, LDO4Vinc = 00		1.2		V
		LDO4VSet = 1.8V, LDO4Vinc = 00		1.8		
Output-Voltage Accuracy	ACC_RTC	I_{RTC_LDO} = 1mA	-2.5		+2.5	%
Line Regulation	$V_{LINE\_REG\_RTC}$	V_{CHGOUT} from 2.7V to 3.7V	-0.26	0.04	+0.26	%/V
Load Regulation Error	$V_{LOADREG\_RTC}$	I_{RTC_LDO} from 2µA to 2mA	-0.5	0.1	+0.5	%/mA
Line Transient	$V_{LINETRAN\_RTC}$	CHGOUT from 2.7V to 3.7V in 1µs rise/fall time, C_{OUT_EFF} = 1µF		±6		mV
Load Transient	$V_{LOAD\_TRAN\_RTC}$	I_{RTC_LDO} from 0 to 2mA in 100ns, C_{OUT_EFF} = 1µF		30		mV
Output Leakage	I_{LK_RTC}	RTC_LDO disabled, V_{RTC_LDO} = 0V			1	µA

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time	t_{ON_RTC}	I_{RTC_LDO} = 0mA, time from 10% to 90% of final value		1.5		ms
Passive Discharge Resistance	R_{PD_RTC}		5	10	15	kΩ
BUCK-BOOST						
Input Voltage	V_{BBIN}	Input voltage = V_{SYS}	2.7		5.5	V
Output-Voltage Set Range	V_{BBOUT}	50mV step resolution, do not exceed the valid voltage range	2.6		5.5	V
Quiescent Supply Current	I_{Q_BB}	I_{BBOUT} = 0, V_{BBOUT} = 5V		2	4	µA
Maximum Output Operative Power	P_{MAX_BBOUT}	BBstIpPadPEnb = 0, V_{SYS} ≥ 3.2V, V_{BBOUT} ≥ 3.2V, 7.5% load regulation, BBZCCmpEnB = 0 (*Note 4*)	1.5			W
Load-Regulation Error	LOAD_REG_ERR	BBstIpPadPEnb = 0, BBstVSet > 3.3V, P_{OUT} = 1.5W		-3.5		%
Average Output-Voltage Accuracy	ACC_BBOUT	I_{BBOUT} = 1mA, C_{BBOUT_EFF} ≥ 5µF	-2.7		+2.7	%
Maximum Output Current During Start-Up	$I_{LOAD\_MAX\_STUP}$	V_{SYS} > 3V, BBstIpPadPEnb = 0	85			mA
Start-Up Time	t_{STUP}	I_{LOAD} < $I_{LOAD\_MAX\_STUP}$, time from V_{BBOUT} = 0V to final value		13		ms
Input-Supply Current During Start-Up	I_{BBIN_STUP}	V_{SYS} = 3.6V, V_{BBOUT} = 5V, C_{BBOUT_EFF} = 10µF, I_{BBOUT} = 0		10		mA
Output UVLO Threshold	V_{BBOUT_UVLO}	Falling edge (50mV hysteresis)		1.85	2.46	V
HVLX Leakage Current	I_{LK_BBHVLX}		-1		+1	µA
LVLX Leakage Current	I_{LK_BBLVLX}		-1		+1	µA
Passive Discharge Resistance	R_{PSV_BB}		5	10	17	kΩ
Active Discharge Current	I_{ACTD_BB}	V_{BBOUT} = 2.5V	5	20	50	mA
BBOUT Pull-Down Current	$I_{PD\_BB\_E}$	BBst enabled, BBOUT = BBstVSet + 0.1V		300		nA
Thermal-Shutdown Temperature	T_{SHDN_BB}	I_{LOAD} > 20mA		+150		°C
LOAD SWITCHES 1, 2, AND 3						
Input Voltage	V_{SW_IN}		0.65		5.50	V
Quiescent-Supply Current	$I_{Q\_SW\_}$	Load switch on, voltage protection disabled		0.26	0.53	µA
		Load switch on, voltage protection enabled, V_{LSW_IN} = 1.2V		0.75	1.20	µA
On-Resistance	$R_{SW\_}$	V_{SYS} = 3V, V_{LSW_IN} = 1.2V, I_{LSW_OUT} = 50mA		0.25	0.50	Ω
Start-Up Current	I_{SW_START}	V_{LSW_IN} = 1.2V, V_{LSW_OUT} = 0V initially		50	108	mA
Voltage Protection Threshold	V_{SW_PROT}	Falling	10	120		mV
		Rising		130	260	
Turn-On Time	$t_{ON\_SW\_}$	V_{LSW_IN} = 1.2V, 1µF output capacitance, 10% to 90% of output		15		µs

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Start-Up Time-Out Time	t_{STUP_LSW}			5		ms
Start-Up Retry Time	$t_{RETRY\_LSW\_}$			5		ms
Passive Discharge Resistance	$R_{PSV\_LSW\_}$			10		kΩ
Active Discharge Current	$I_{ACTD\_LSW\_}$			20		mA
Output Leakage	$I_{LK\_LSW\_}$	LSW_OUT = GND, load switch disabled			1	µA
FUEL GAUGE (SEE THE *FUEL GAUGE* SECTION FOR MORE DETAILS)						
Internal Sense Resistor	R_{SNS}	T_A = +25°C		50		mΩ
FUEL-GAUGE POWER SUPPLY						
Shutdown Supply Current	I_{DD0}			0.5		µA
Hibernate Supply Current	I_{DD1}	Average current		5.5		µA
Active Supply Current	I_{DD2}	Average current not including thermistor measurement current		12.5		µA
Start-Up Voltage	$V_{FGBATSU}$				3.05	V
FUEL-GAUGE ANALOG-TO-DIGITAL CONVERSION						
BAT Measurement Error	V_{GERR}	T_A = +25°C	-7.5		+7.5	mV
		-40°C ≤ T_A ≤ +85°C	-20		+20	
BAT Measurement Resolution	V_{LSB}			78.125		µV
BAT Measurement Range	V_{FS}		2.7		4.9	V
Current-Measurement External R_{SNS} Offset Error	I_{OERR_E}	Long-term average without load current		±1.5		µV
Current-Measurement External R_{SNS} Error	I_{ERR_E}		-1		+1	% of Reading
Current-Measurement External R_{SNS} Resolution	I_{LSB_E}			1.5625		µV
Current-Measurement External R_{SNS} Range	I_{FS_E}		-51.2		+51.2	mV
Current Measurement Internal R_{SNS} Offset Error	I_{OERR_I}	Zero current, long-term average, R_{SENSE} = 50mΩ		±0.03		mA
Current Measurement Internal R_{SNS} Resolution	I_{LSB_I}			31.25		µA
Current Measurement Internal R_{SNS} Gain Error	I_{GERR}	(*Note 4*)		±2.5		% of Reading
Current Measurement Internal R_{SNS} Error	I_{ERR_I}	0.1A and 0.2A (*Note 4*)	-3.5		+3.5	% of Reading
Internal Temperature-Measurement Error	T_{I_GERR}	-40°C ≤ T_A ≤ +85°C		±1		°C

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Temperature-Measurement Resolution	T_{I_LSB}			0.00391		°C
FUEL-GAUGE INPUT/OUTPUT						
External Thermal Resistance	R_{EXT10}	Config.R100 = 0		10		kΩ
	R_{EXT100}	Config.R100 = 1		100		
Output Drive Low, $\overline{ALRT}$	V_{OL}	I_{OL} = 4mA, V_{BAT} = 2.3V			0.4	V
Input Logic High, $\overline{ALRT}$	V_{IH}		1.5			V
Input Logic Low, $\overline{ALRT}$	V_{IL}				0.5	V
Battery-Detach Detection Threshold	V_{DET}	Measured as a fraction of V_{BAT} on THM rising	91.0	96.2	99.0	%
Battery-Detach Detection Threshold Hysteresis	$V_{DET-HYS}$	Measured as a fraction of V_{BAT} on THM falling		1.6		%
Battery-Detach Comparator Delay	t_{OFF}	THM step from 70% to 100% of V_{BAT} (Alrtp = 0, EnAIN = 1, FTHRM = 1)			100	µs
FUEL-GAUGE LEAKAGE						
Leakage Current, CSN, CSP/FG_TST, $\overline{ALRT}$	I_{LEAK}	$V_{\overline{ALRT}}$ < 15V	-1		+1	µA
FUEL-GAUGE TIMING						
Time-Base Accuracy	t_{ERR}	T_A = +25°C	-1		+1	%
THM Precharge Time	t_{PRE}		8.48			ms
DIGITAL						
SDA, SCL, MPC_, PFN_, $\overline{RST}$, $\overline{INT}$ Input-Leakage Current	I_{LK_IO}	Input pull-up/pull-down resistances disabled, V_{IO} = 0V to 5.5V	-1		+1	µA
SDA, SCL, MPC_ Input-Logic High	V_{IO_IH}		1.4			V
SDA, SCL, MPC_ Input-Logic Low	V_{IO_IL}				0.4	V
PFN_ Input-Logic High	$V_{PFN\_IH\_C}$	Off/seal mode		0.7 x V_{CCINT}		V
PFN_ Input-Logic Low	$V_{PFN\_IL\_C}$	Off/seal mode		0.3 x V_{CCINT}		V
PFN_ Input-Logic-High	$V_{PFN\_IH\_T}$	On mode	1.4			V
PFN_ Input-Logic-Low	$V_{PFN\_IL\_T}$	On mode			0.4	V
MPC_, PFN_ Input-Pull-Up Resistance	R_{IO_PU}	Pull-up resistance to V_{CCINT} (*Note 2*)		170		kΩ
MPC_, PFN_ Input-Pull-Down Resistance	R_{IO_PD}			170		kΩ
MPC_ Output Logic-High	V_{IO_OH}	I_{OH} = 1mA, MPC_ configured as push-pull output, pull-up voltage is V_{BK1OUT}	V_{BK1OUT} - 0.4			V
SDA, MPC_, PFN2, $\overline{RST}$, $\overline{INT}$ Output Logic Low	V_{IO_OL}	I_{OL} = 4mA			0.4	V

(V_{BAT} = V_{CHGOUT} = V_{SYS_UVLO} (falling) to +4.9V, V_{CHGIN} = unconnected or V_{CHGIN_DET} to V_{CHGIN_OV}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{BAT} = 3.7V, V_{CHGIN} = 5.0V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH. ())

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MPC6 Harvester Disable Pull-Up Resistor	$R_{MPC6\_HARV\_DIS\_RPU}$	Harvester interaction enabled, pull-up resistor to V_{CCINT} (*Note 2*)		4		kΩ
SCL Clock Frequency	f_{SCL}	(*Note 5*)	0		400	kHz
Bus Free-Time Between Stop and Start Condition	t_{BUF}		1.3			µs
Hold Time for a Repeated Start Condition	t_{HD_STA}		0.6			µs
Setup Time for a Repeated Start Condition	t_{SU_STA}		0.6			µs
Low Period of SCL Clock	t_{LOW}	(*Note 6*)	1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data-Hold Time	t_{HD_DAT}	(*Note 7* and *Note 8*)	0		0.9	µs
Data-Setup Time	t_{SU_DAT}		100			ns
Setup Time for Stop Condition	t_{SU_STO}		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(*Note 9*)	50			ns
SPI						
SCLK Frequency	f_{SCLK}				10	MHz
Setup Time	t_{CS}		10			ns
Hold Time	t_{CH}		100			ns
Pulse-Width High	t_{IDLE}			60		ns
DIN Setup Time	t_{DS}		10			ns
DIN Hold Time	t_{DH}		20			ns
SCLK Pulse-Width Low	t_{LOW_SPI}		20			ns
SCLK Pulse-Width High	t_{HIGH_SPI}		20			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: V_{CCINT} is an internal supply generated from either BAT or CAP. Its voltage is determined by the following:
IF: [(V_{CHGIN} > V_{CHGIN_DET} AND V_{CAP} > V_{CAP_DET}) OR V_{CAP} > (V_{BAT} + $V_{THSWOVER}$)]
THEN: V_{CCINT} = V_{CAP}
ELSE: V_{CCINT} = V_{BAT}
where $V_{THSWOVER}$ = 0mV - 300mV

Note 3: If the fuel gauge is permanently disabled (FG_OTP_ENA = 0), avoid using IVMON ratio 1:1 on THM.

Note 4: Guaranteed by design, not production tested.

Note 5: Timing must be fast enough to prevent the fuel gauge from entering shutdown mode due to bus low for a period greater than the shutdown timer setting.

Note 6: The SCL waveform must meet the minimum clock low time plus the rise/fall times.

Note 7: The maximum t_{HD_DAT} has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

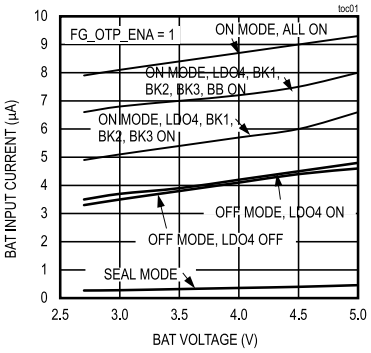
Note 8: This device internally provides a hold time of at least 100ns for the SDA signal (see the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 9: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

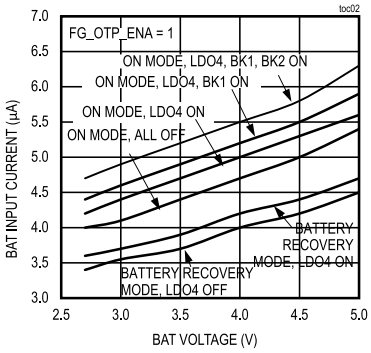
Typical Operating Characteristics

(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25˚C, unless otherwise noted.)

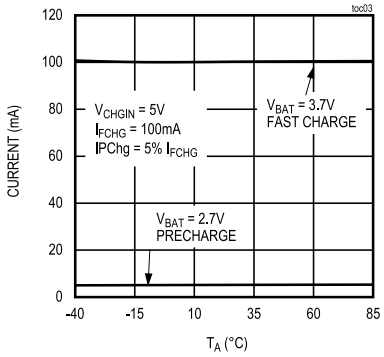
BAT INPUT CURRENT vs. BAT VOLTAGE



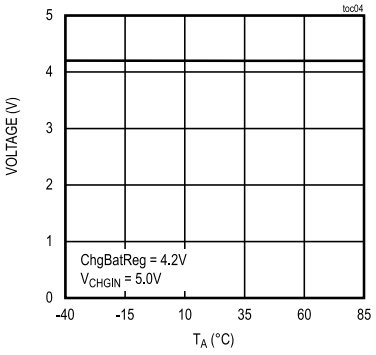
BAT INPUT CURRENT vs. BAT VOLTAGE



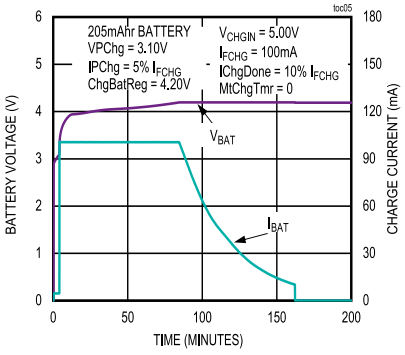
CHARGER CURRENT vs. TEMPERATURE



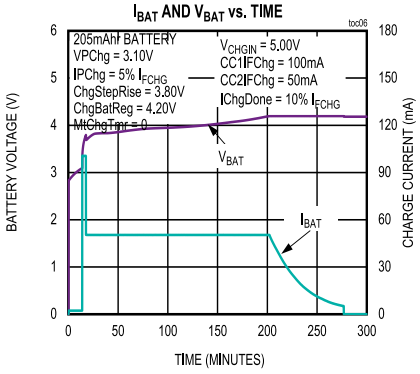
CHARGER VOLTAGE vs. TEMPERATURE



CHARGER PROFILE
I_{BAT} AND V_{BAT} vs. TIME

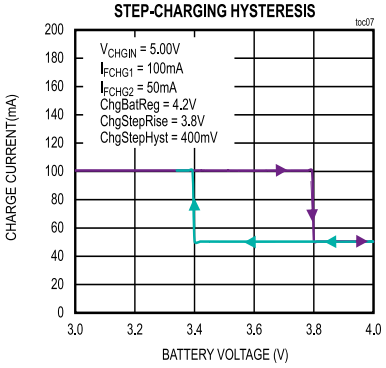


STEP-CHARGING CHARGER PROFILE
I_{BAT} AND V_{BAT} vs. TIME

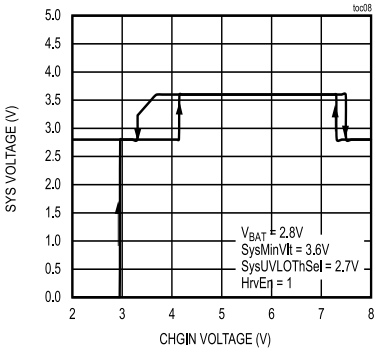


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

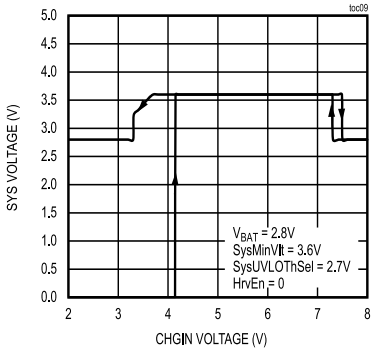
STEP-CHARGING HYSTERESIS



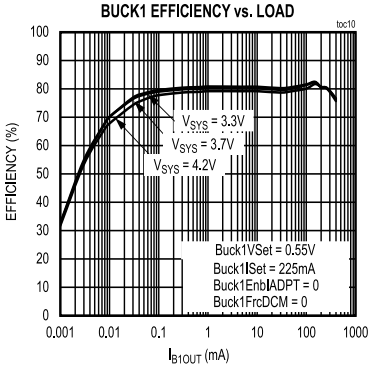
SYS VOLTAGE vs. CHGIN VOLTAGE



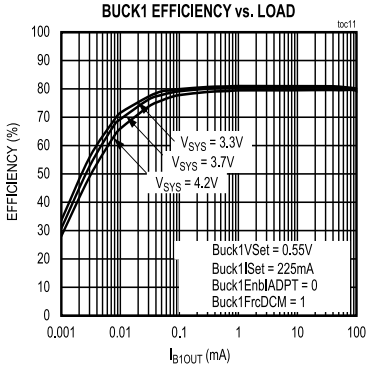
SYS VOLTAGE vs. CHGIN VOLTAGE



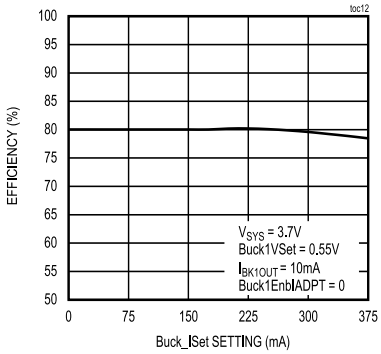
BUCK1 EFFICIENCY vs. LOAD



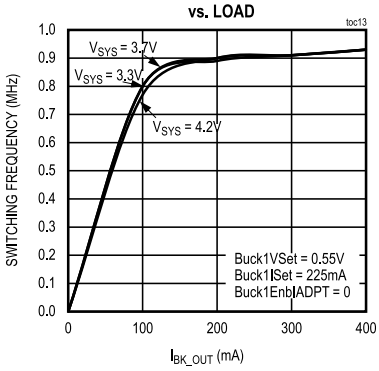
BUCK1 EFFICIENCY vs. LOAD



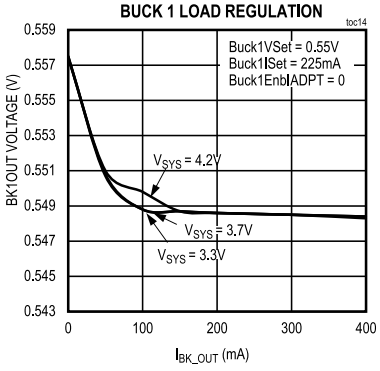
BUCK1 EFFICIENCY vs. Buck_ISet SETTING



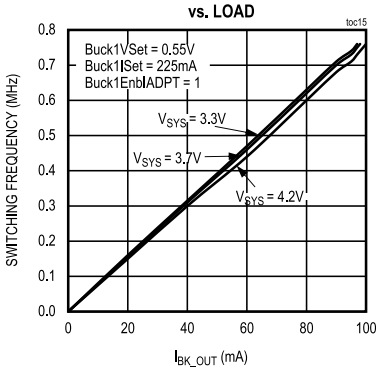
BUCK 1 SWITCHING FREQUENCY vs. LOAD



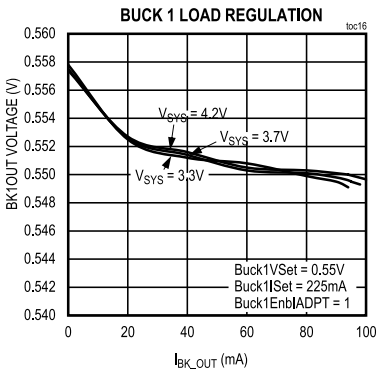
BUCK 1 LOAD REGULATION

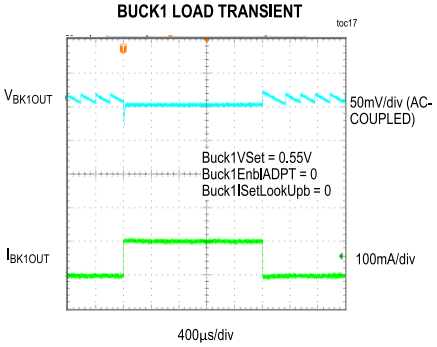


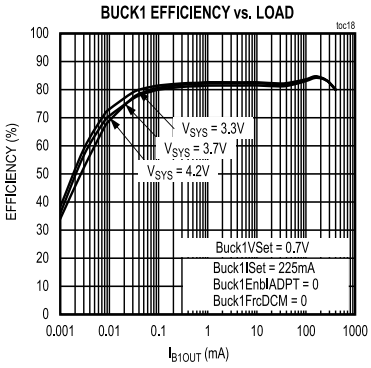
BUCK 1 SWITCHING FREQUENCY vs. LOAD

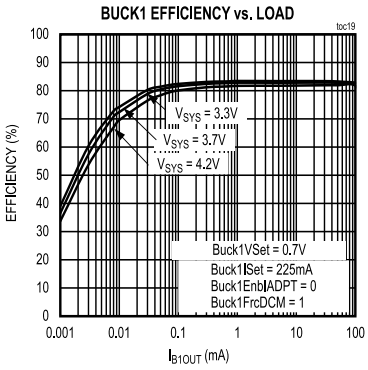


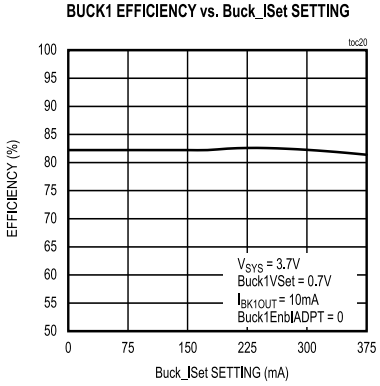
(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

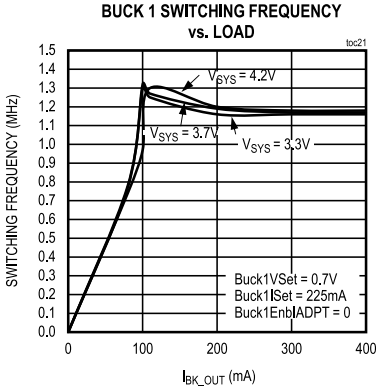


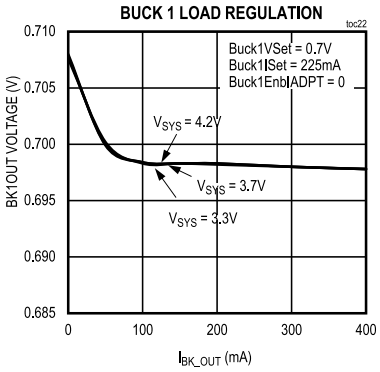


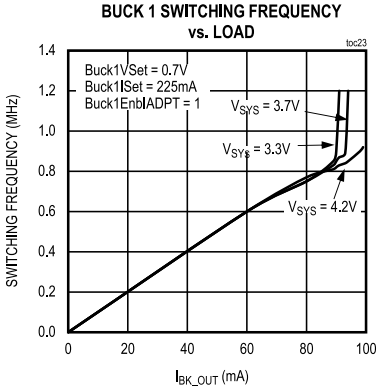


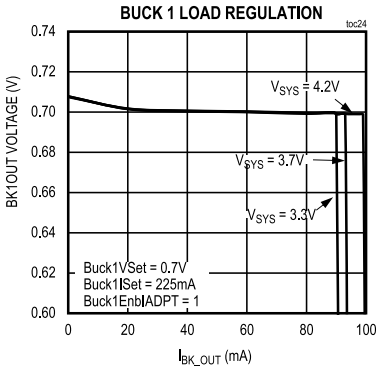












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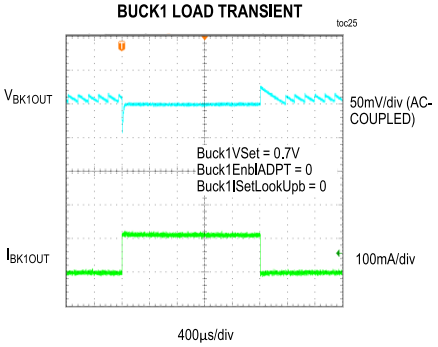
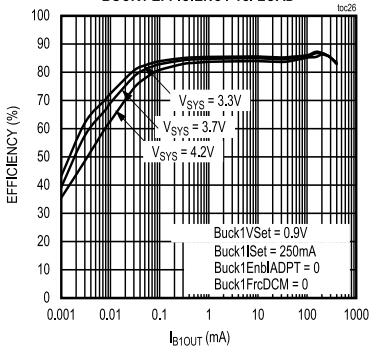
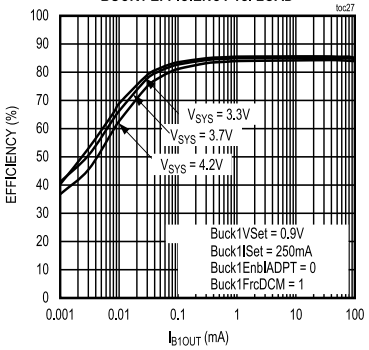
BUCK1 LOAD TRANSIENT



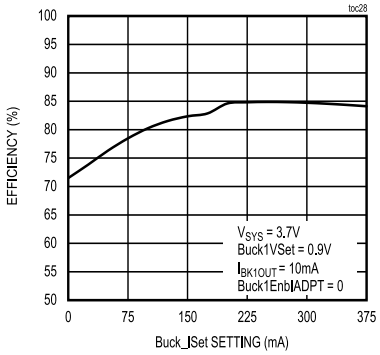
BUCK1 EFFICIENCY vs. LOAD



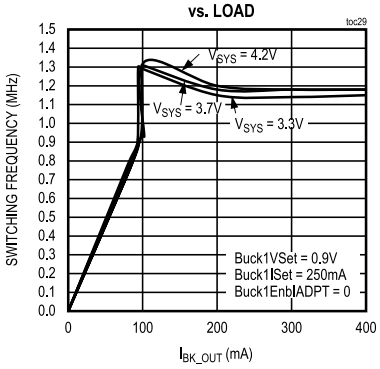
BUCK1 EFFICIENCY vs. LOAD



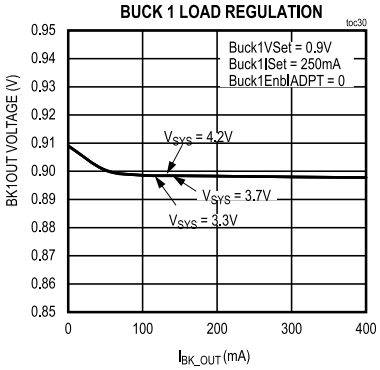
BUCK1 EFFICIENCY vs. Buck_ISet SETTING



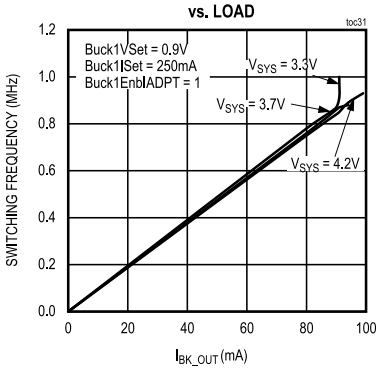
BUCK 1 SWITCHING FREQUENCY vs. LOAD



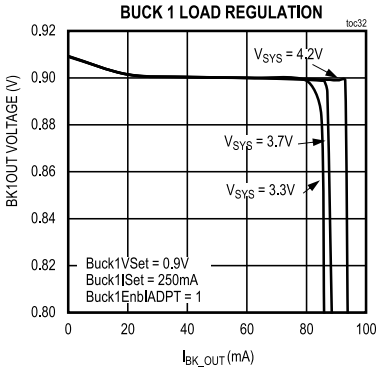
BUCK 1 LOAD REGULATION



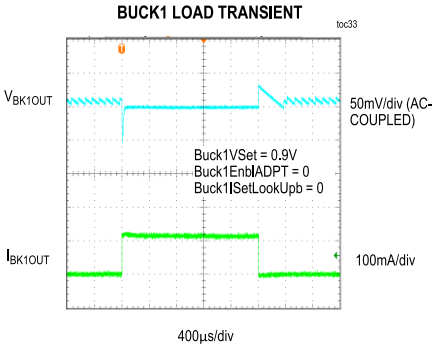
BUCK 1 SWITCHING FREQUENCY vs. LOAD



BUCK 1 LOAD REGULATION



BUCK1 LOAD TRANSIENT



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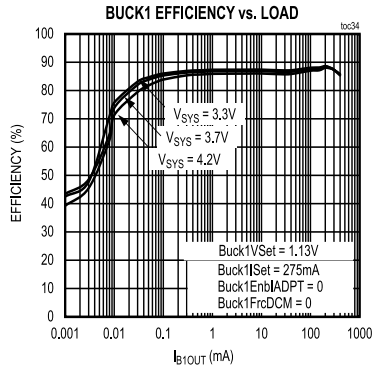

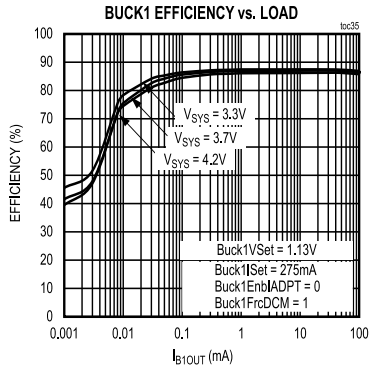

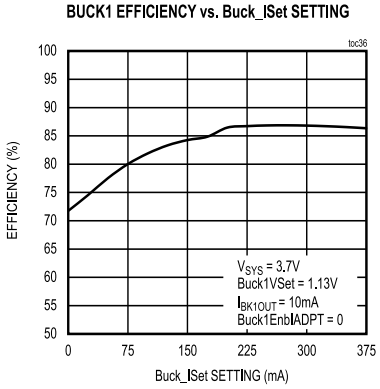

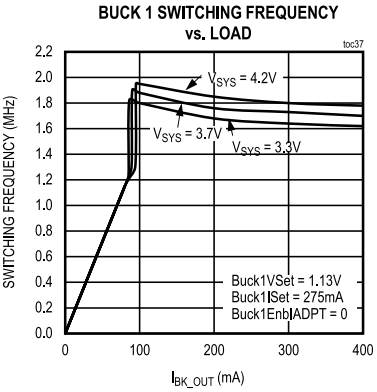

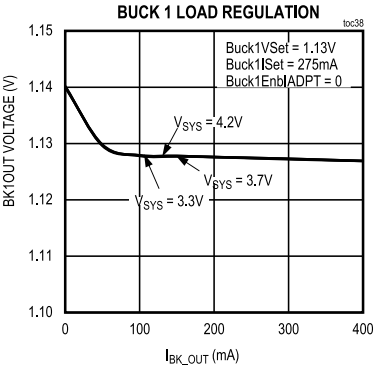

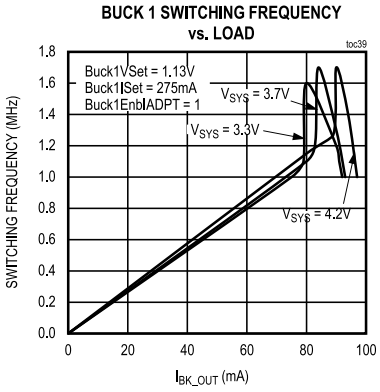

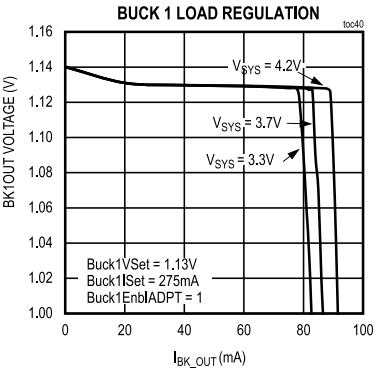

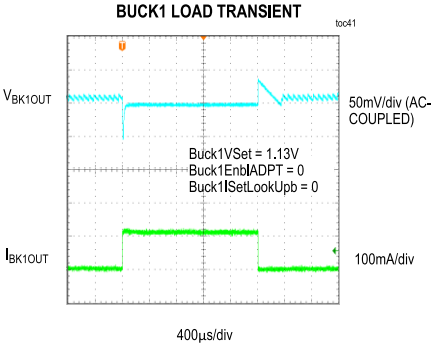

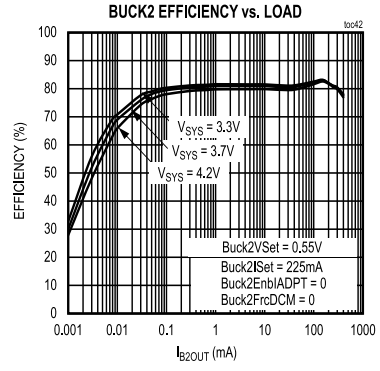

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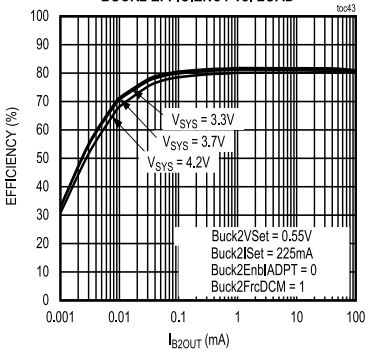
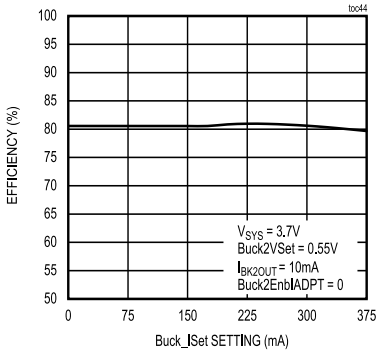
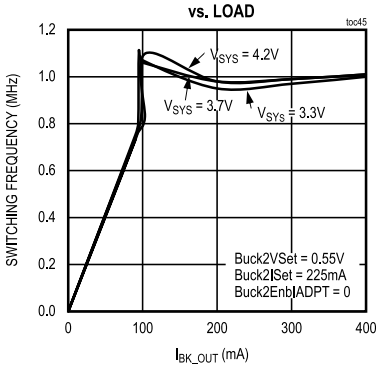
BUCK2 EFFICIENCY vs. LOAD



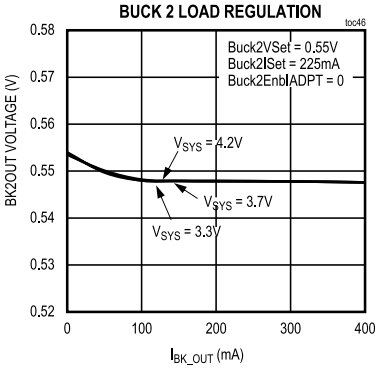
BUCK2 EFFICIENCY vs. Buck_ISet SETTING



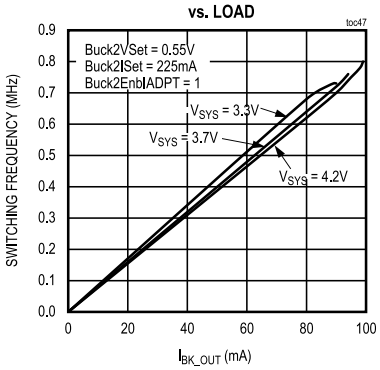
BUCK 2 SWITCHING FREQUENCY vs. LOAD



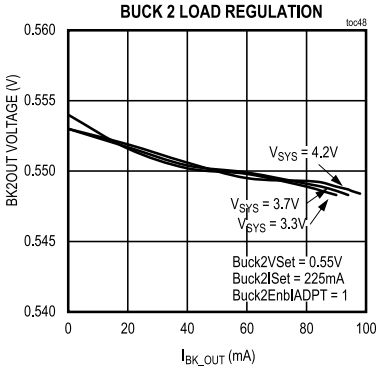
BUCK 2 LOAD REGULATION



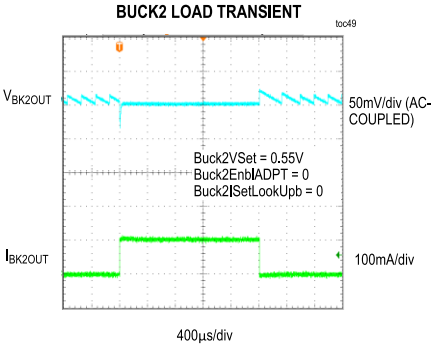
BUCK 2 SWITCHING FREQUENCY vs. LOAD



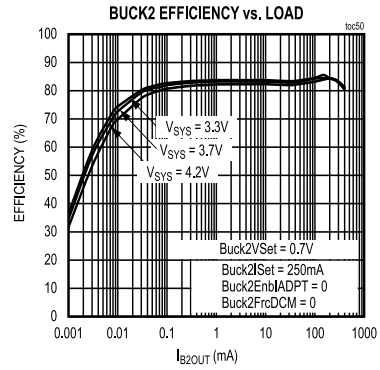
BUCK 2 LOAD REGULATION



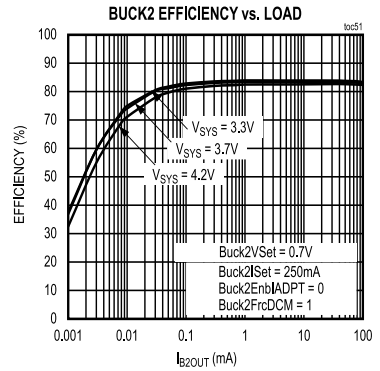
BUCK2 LOAD TRANSIENT



BUCK2 EFFICIENCY vs. LOAD



BUCK2 EFFICIENCY vs. LOAD



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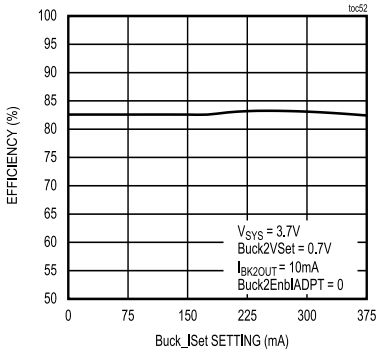
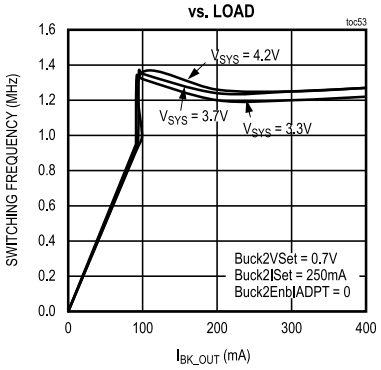
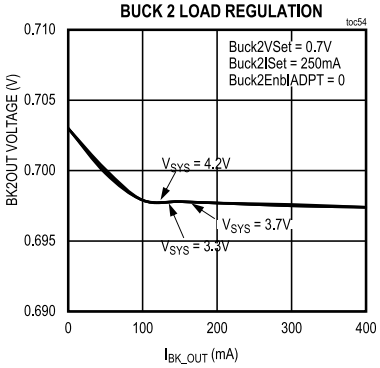
BUCK2 EFFICIENCY vs. Buck_ISet SETTING



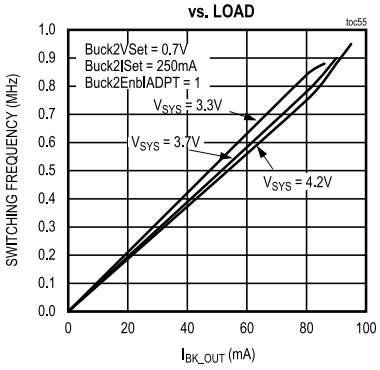
BUCK 2 SWITCHING FREQUENCY vs. LOAD



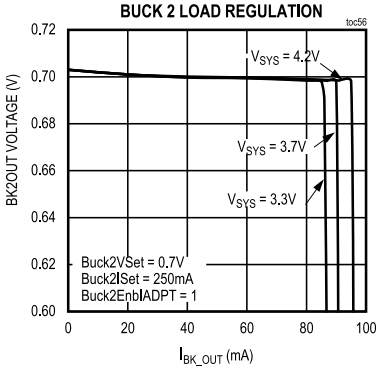
BUCK 2 LOAD REGULATION



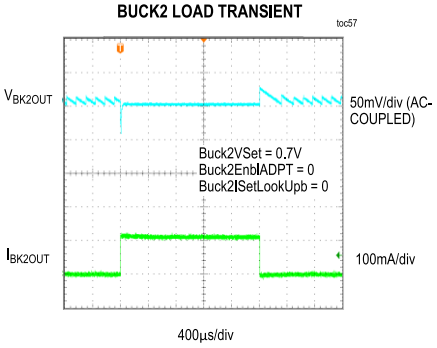
BUCK 2 SWITCHING FREQUENCY vs. LOAD



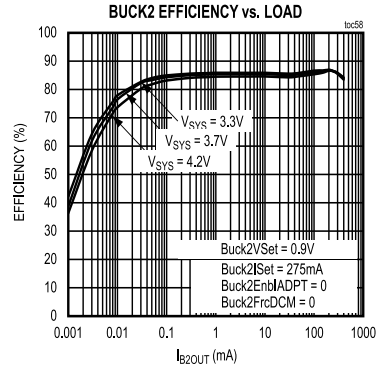
BUCK 2 LOAD REGULATION



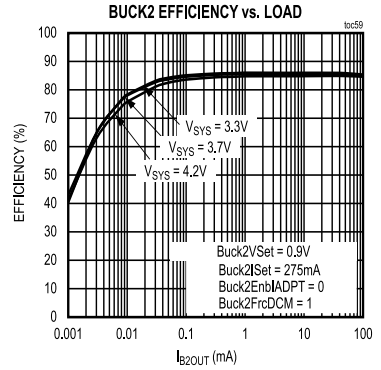
BUCK2 LOAD TRANSIENT



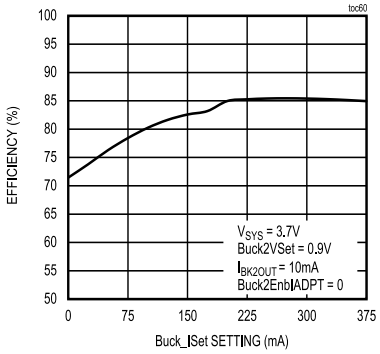
BUCK2 EFFICIENCY vs. LOAD



BUCK2 EFFICIENCY vs. LOAD

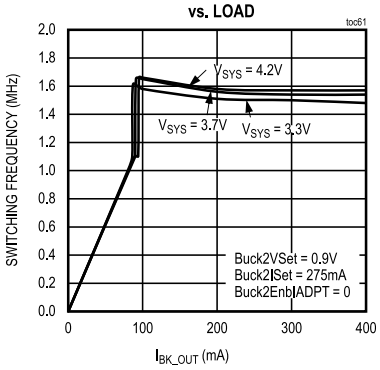


BUCK2 EFFICIENCY vs. Buck_ISet SETTING

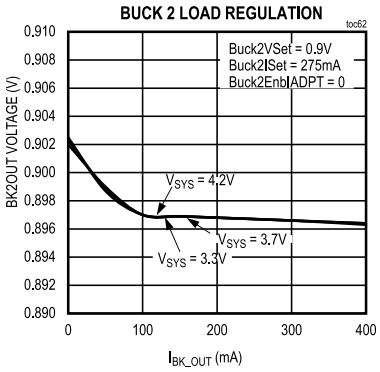


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

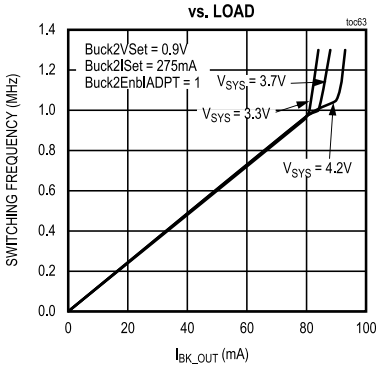
BUCK 2 SWITCHING FREQUENCY vs. LOAD



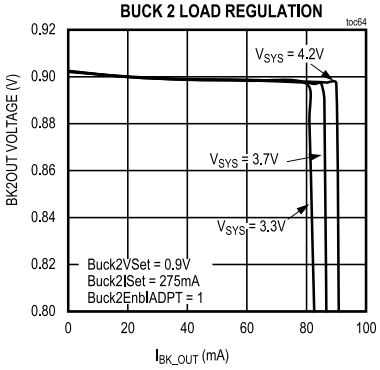
BUCK 2 LOAD REGULATION



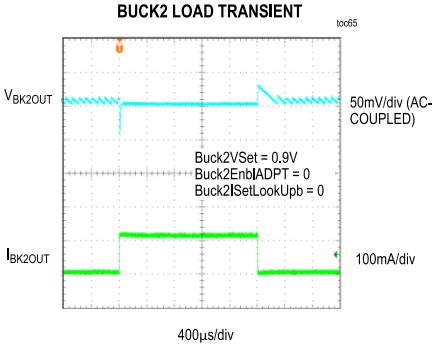
BUCK 2 SWITCHING FREQUENCY vs. LOAD



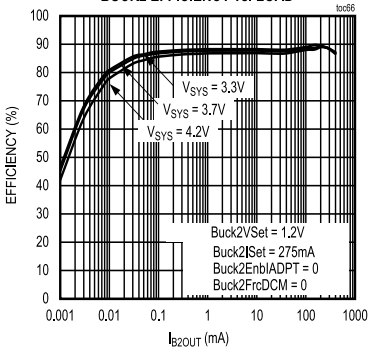
BUCK 2 LOAD REGULATION



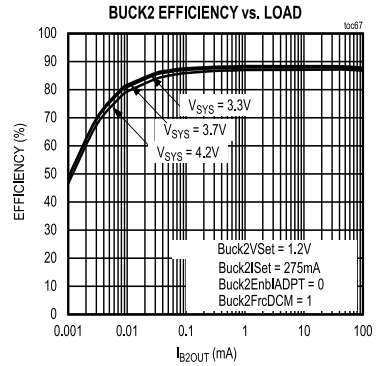
BUCK2 LOAD TRANSIENT



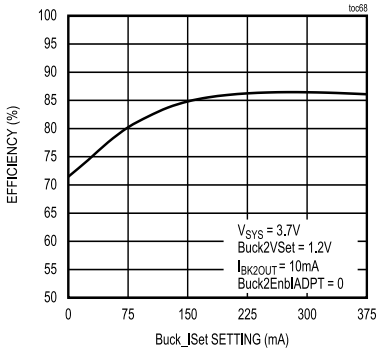
BUCK2 EFFICIENCY vs. LOAD



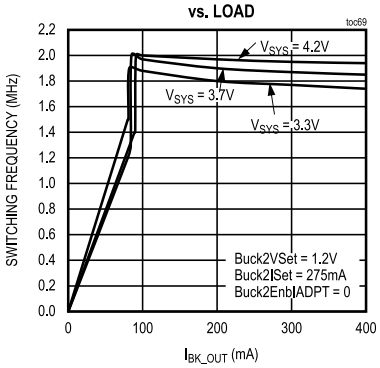
BUCK2 EFFICIENCY vs. LOAD



BUCK2 EFFICIENCY vs. Buck_ISet SETTING



BUCK 2 SWITCHING FREQUENCY vs. LOAD



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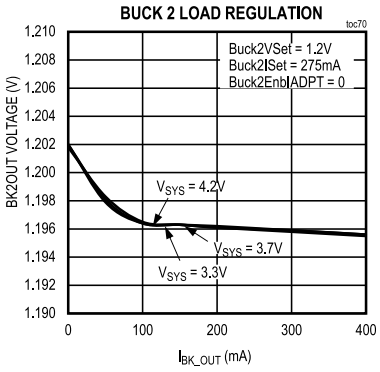

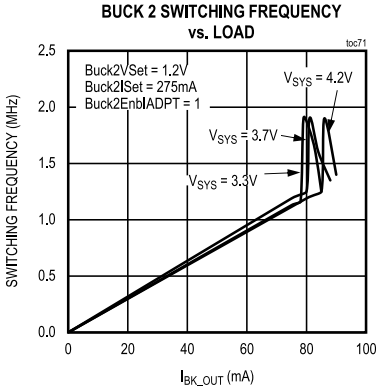

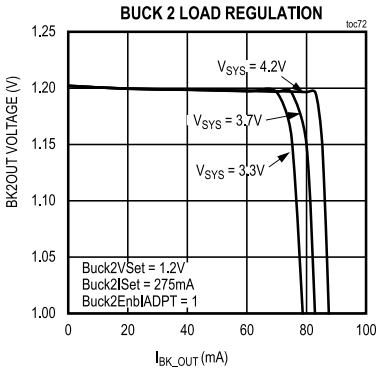

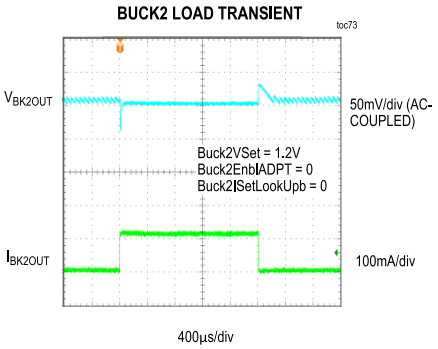

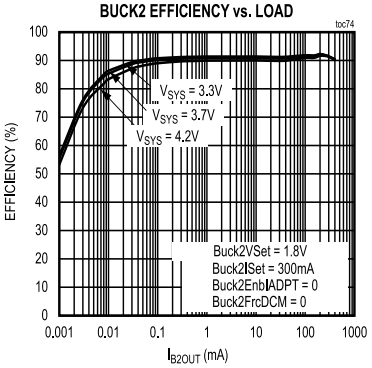

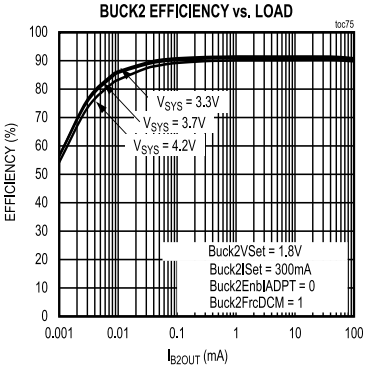

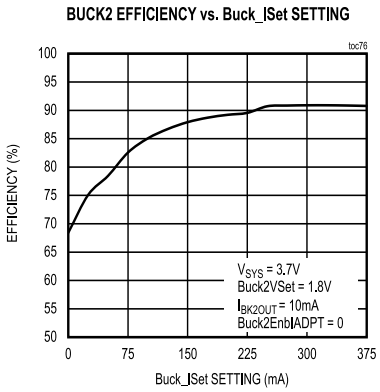

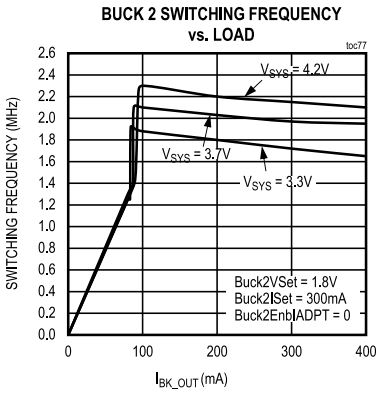

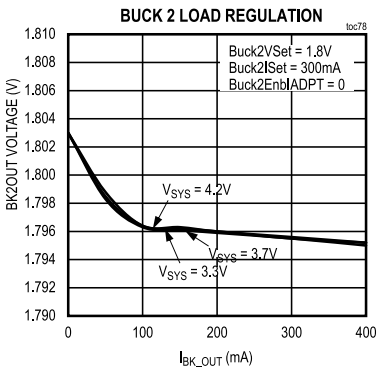

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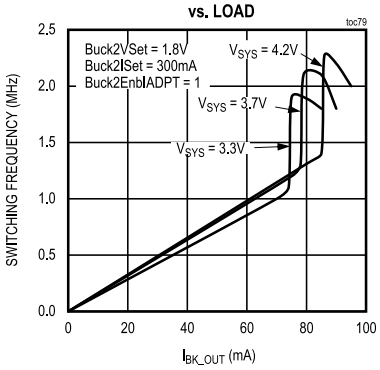
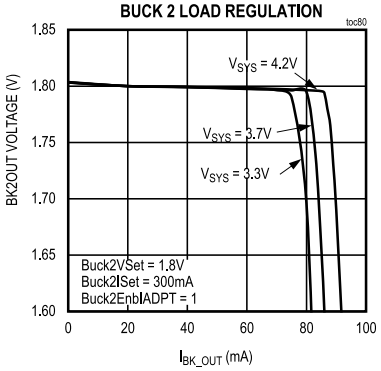
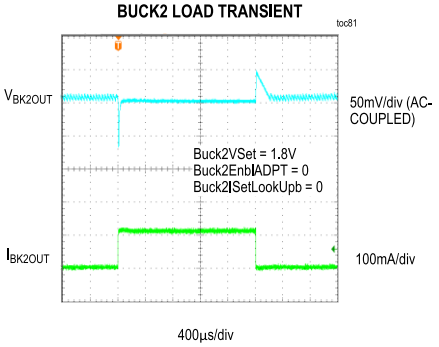
BUCK 2 SWITCHING FREQUENCY vs. LOAD



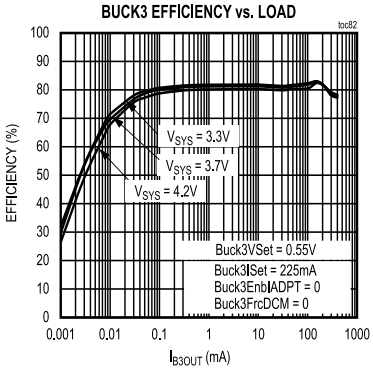
BUCK 2 LOAD REGULATION



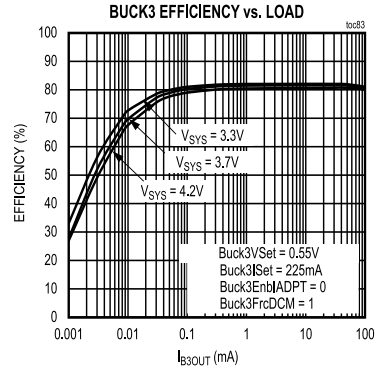
BUCK2 LOAD TRANSIENT



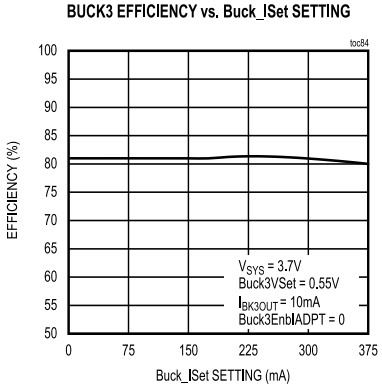
BUCK3 EFFICIENCY vs. LOAD



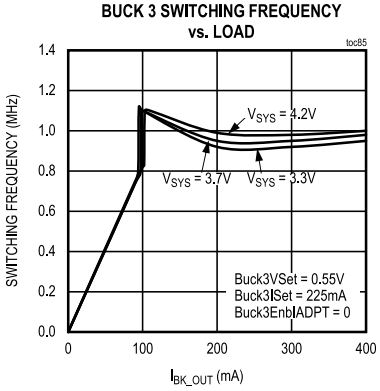
BUCK3 EFFICIENCY vs. LOAD



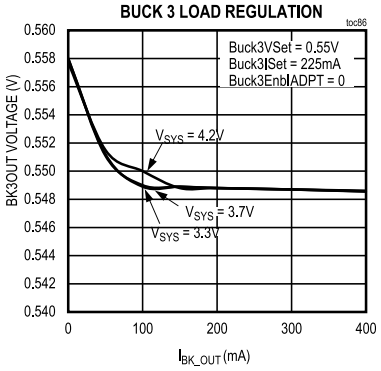
BUCK3 EFFICIENCY vs. Buck_ISet SETTING



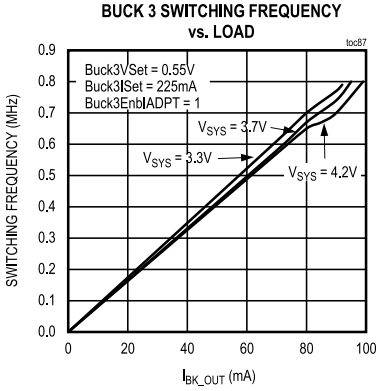
BUCK 3 SWITCHING FREQUENCY vs. LOAD



BUCK 3 LOAD REGULATION



BUCK 3 SWITCHING FREQUENCY vs. LOAD



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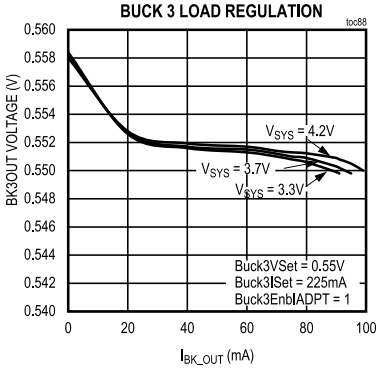
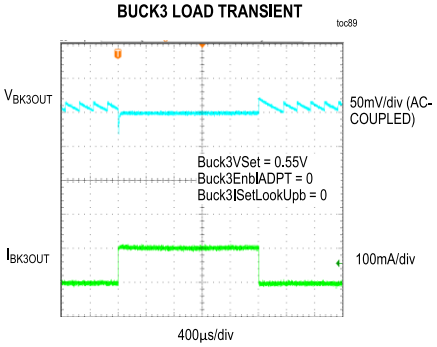
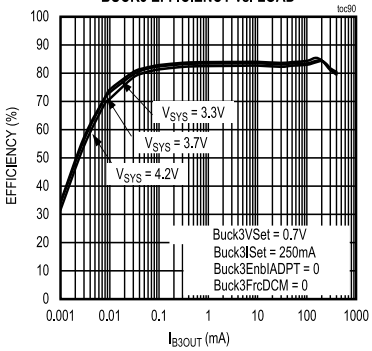
BUCK 3 LOAD REGULATION



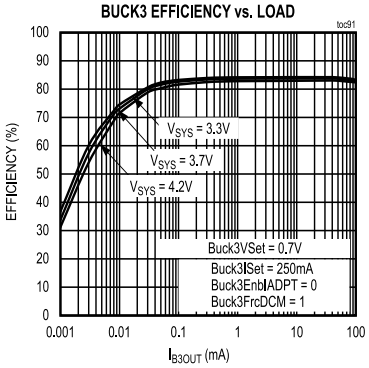
BUCK3 LOAD TRANSIENT



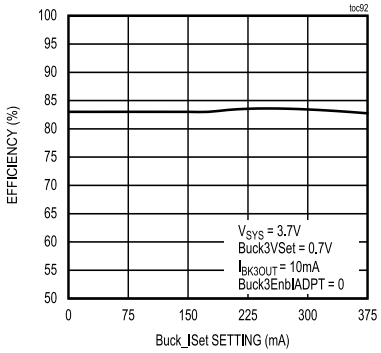
BUCK3 EFFICIENCY vs. LOAD



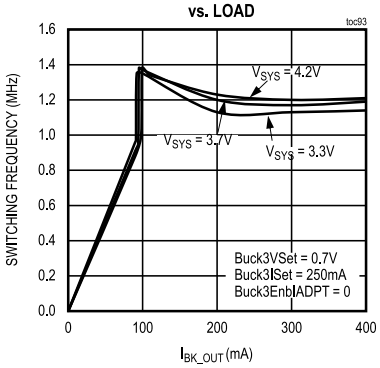
BUCK3 EFFICIENCY vs. LOAD



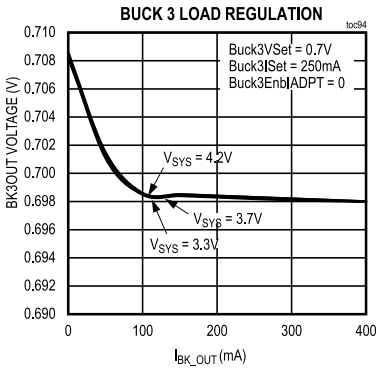
BUCK3 EFFICIENCY vs. Buck_ISet SETTING



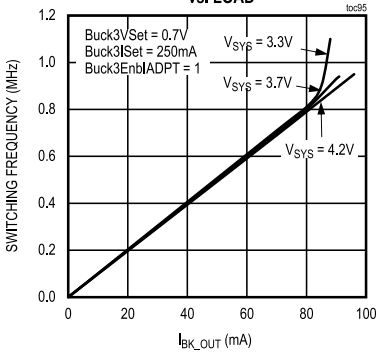
BUCK 3 SWITCHING FREQUENCY vs. LOAD



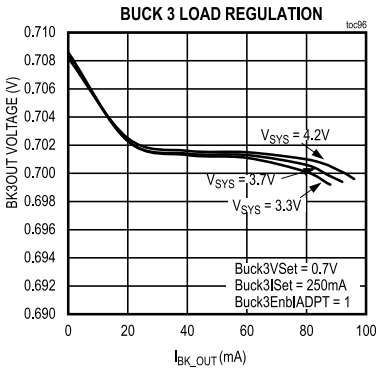
BUCK 3 LOAD REGULATION



BUCK 3 SWITCHING FREQUENCY vs. LOAD



BUCK 3 LOAD REGULATION



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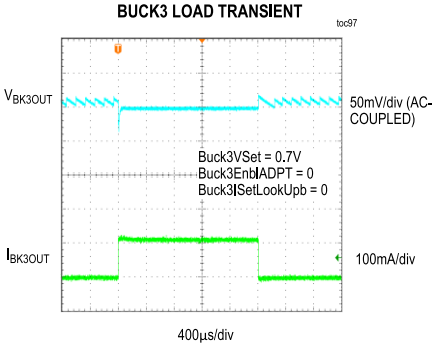
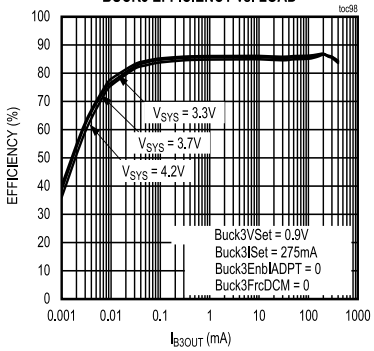
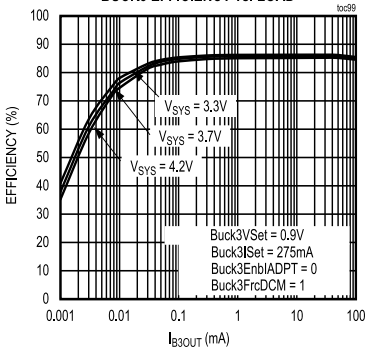
BUCK3 LOAD TRANSIENT



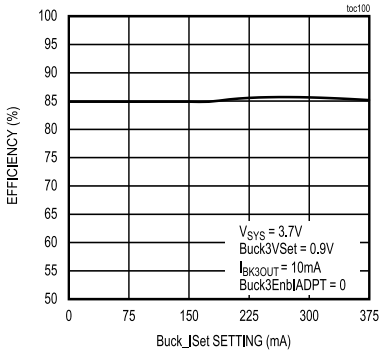
BUCK3 EFFICIENCY vs. LOAD



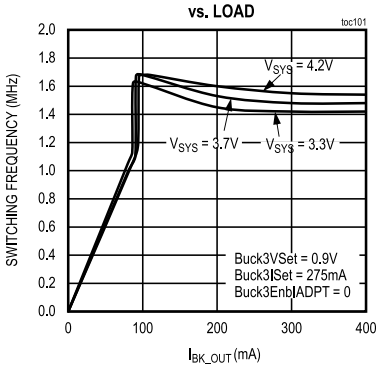
BUCK3 EFFICIENCY vs. LOAD



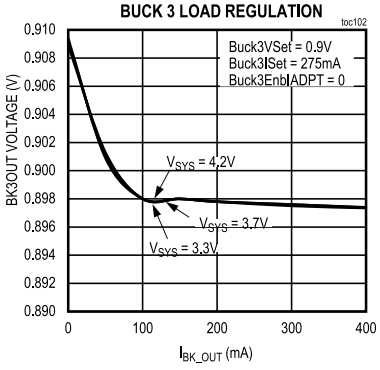
BUCK3 EFFICIENCY vs. Buck_ISet SETTING



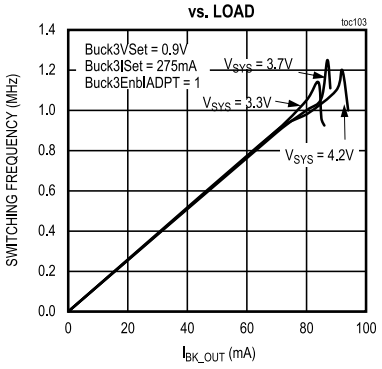
BUCK 3 SWITCHING FREQUENCY vs. LOAD



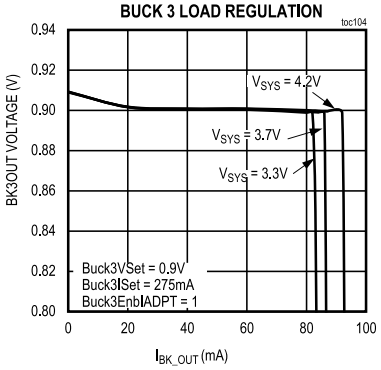
BUCK 3 LOAD REGULATION



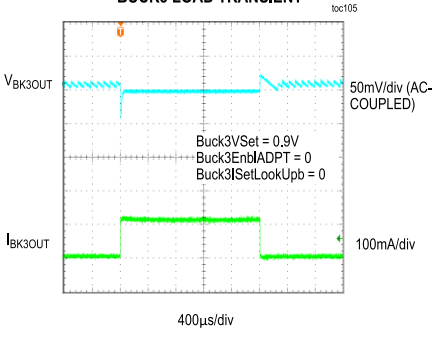
BUCK 3 SWITCHING FREQUENCY vs. LOAD



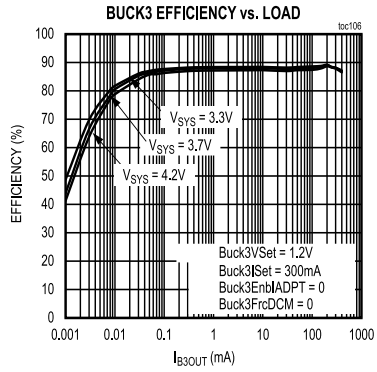
BUCK 3 LOAD REGULATION

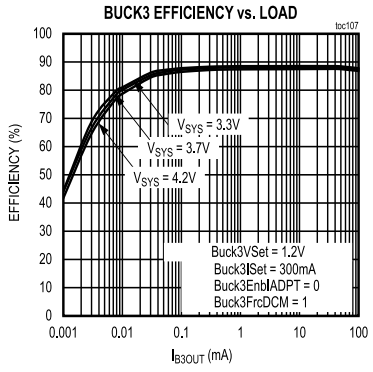


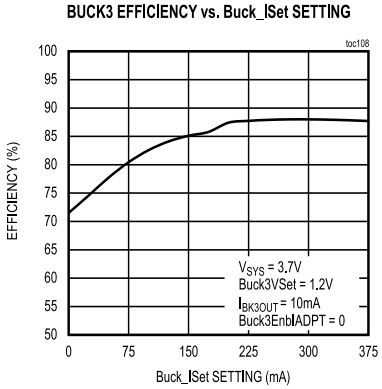
BUCK3 LOAD TRANSIENT

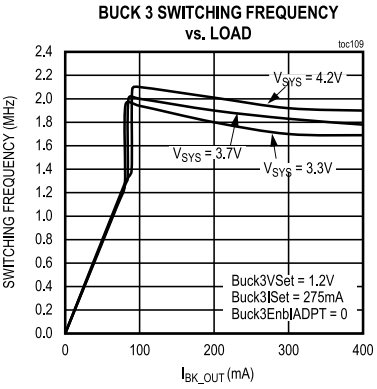


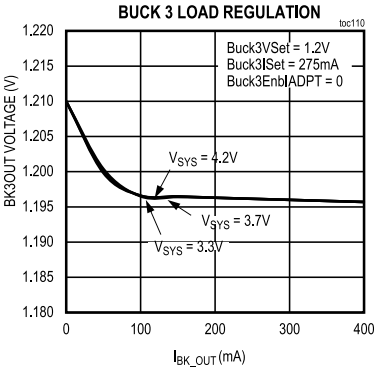
(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

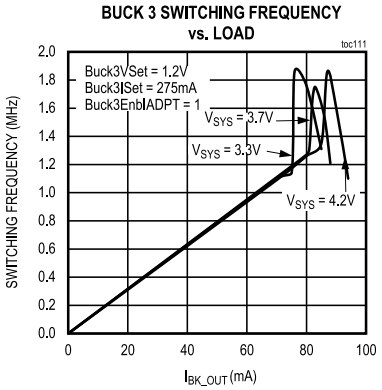


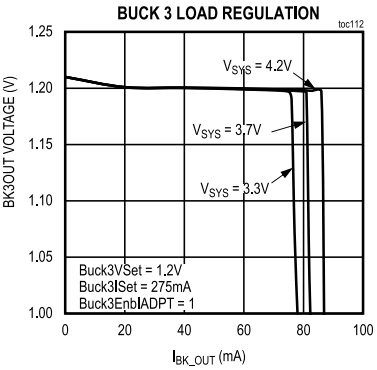


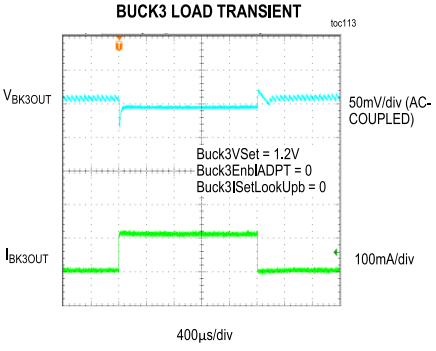


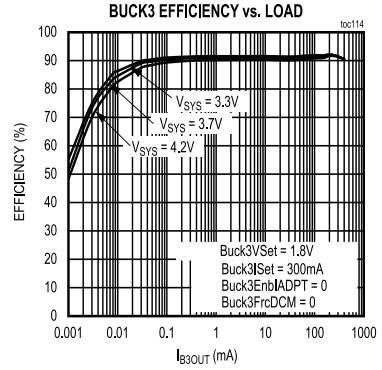






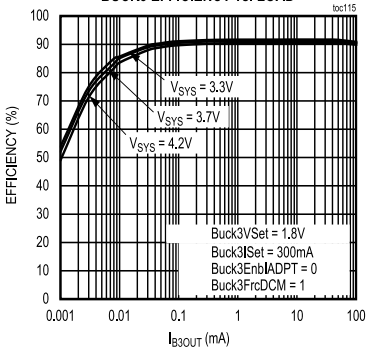




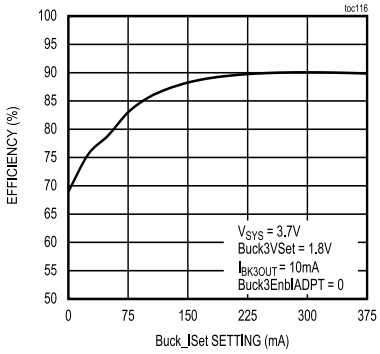


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

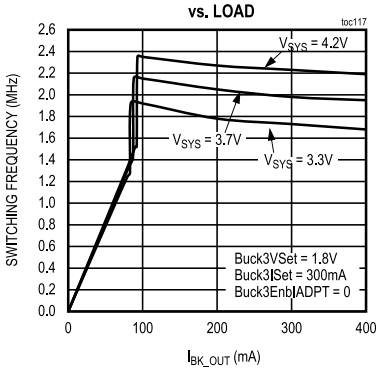
BUCK3 EFFICIENCY vs. LOAD



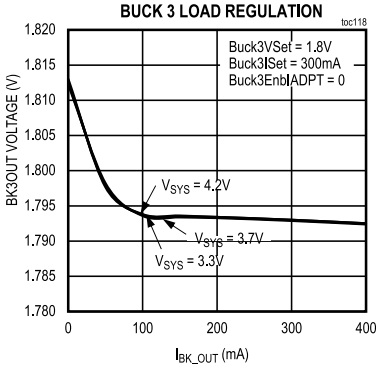
BUCK3 EFFICIENCY vs. Buck_ISet SETTING



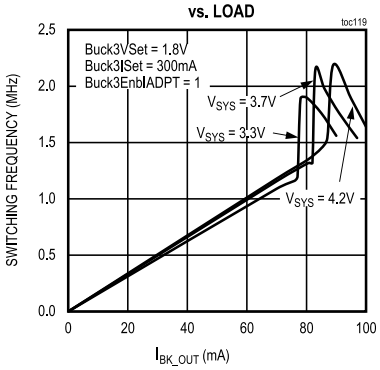
BUCK 3 SWITCHING FREQUENCY vs. LOAD



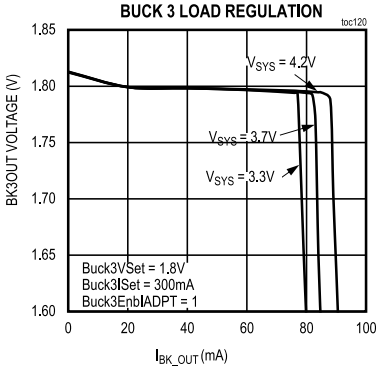
BUCK 3 LOAD REGULATION



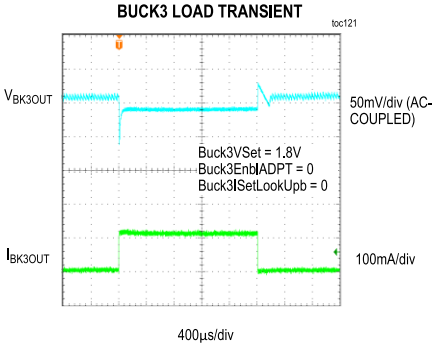
BUCK 3 SWITCHING FREQUENCY vs. LOAD



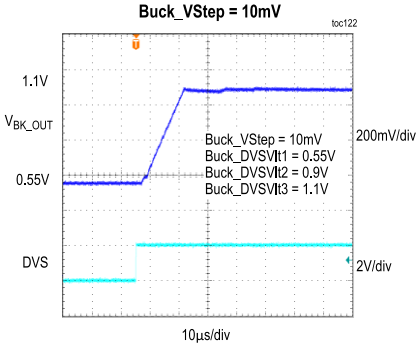
BUCK 3 LOAD REGULATION



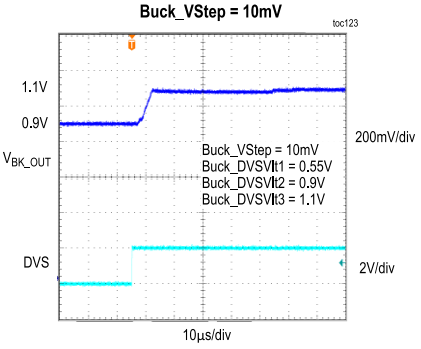
BUCK3 LOAD TRANSIENT



BUCK DVS MODE 1 TRANSITION
Buck_VStep = 10mV

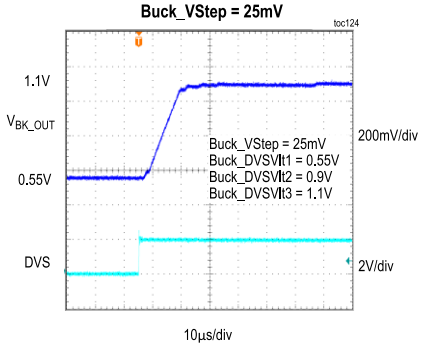


BUCK DVS MODE 1 TRANSITION
Buck_VStep = 10mV

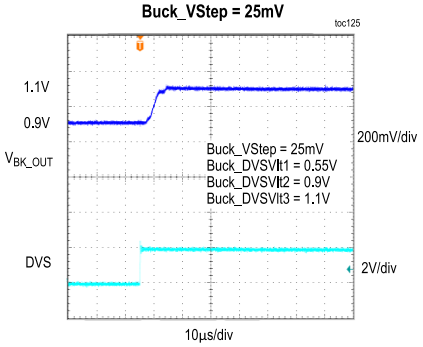


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

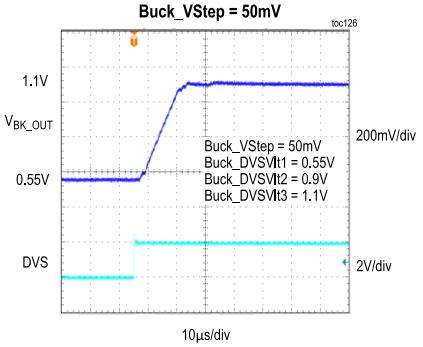
BUCK DVS MODE 1 TRANSITION
Buck_VStep = 25mV



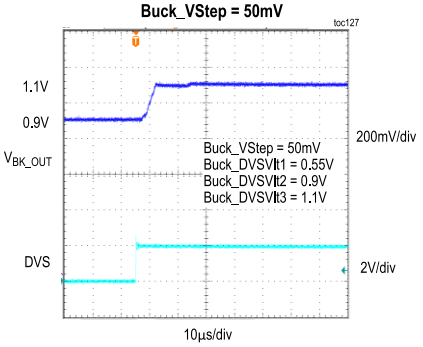
BUCK DVS MODE 1 TRANSITION
Buck_VStep = 25mV



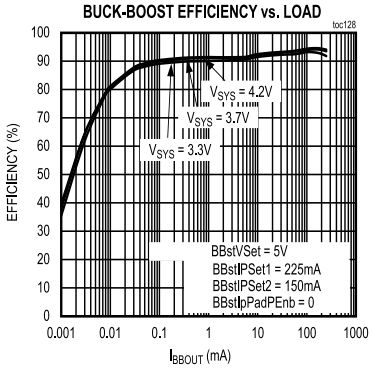
BUCK DVS MODE 1 TRANSITION
Buck_VStep = 50mV



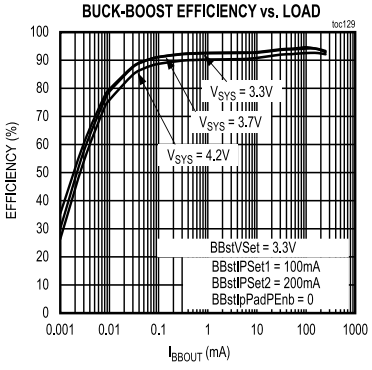
BUCK DVS MODE 1 TRANSITION
Buck_VStep = 50mV



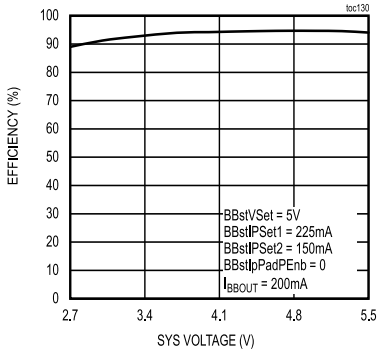
BUCK-BOOST EFFICIENCY vs. LOAD



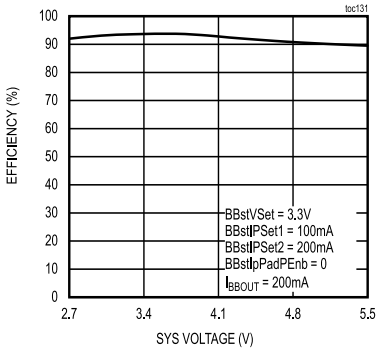
BUCK-BOOST EFFICIENCY vs. LOAD



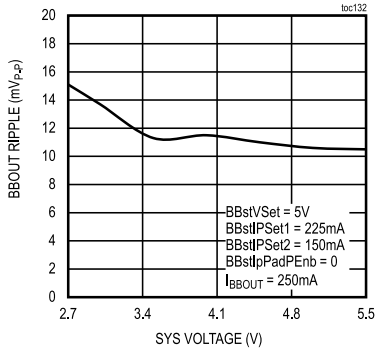
BUCK-BOOST EFFICIENCY vs. SYS VOLTAGE



BUCK-BOOST EFFICIENCY vs. SYS VOLTAGE

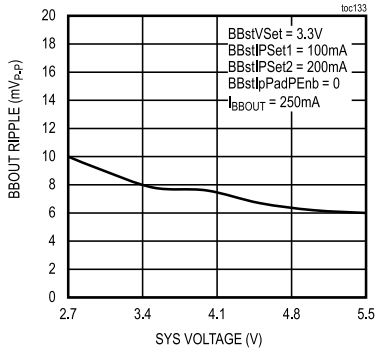


BUCK-BOOST RIPPLE vs. SYS VOLTAGE

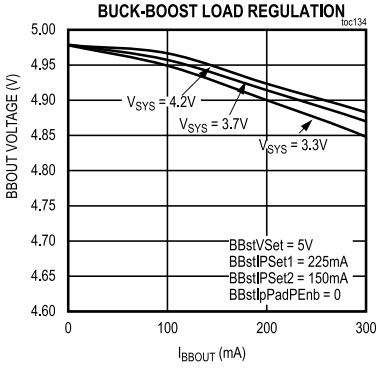


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

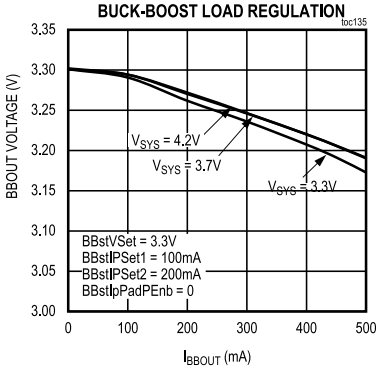
BUCK-BOOST RIPPLE vs. SYS VOLTAGE



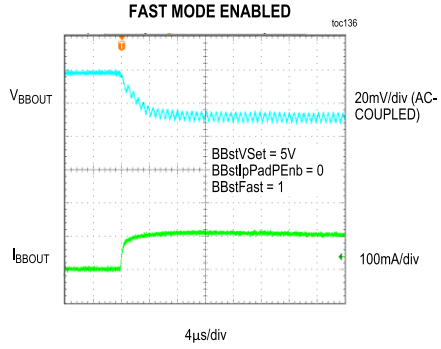
BUCK-BOOST LOAD REGULATION



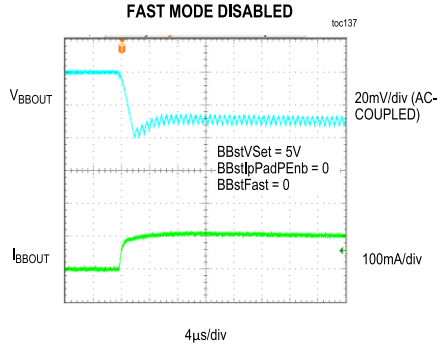
BUCK-BOOST LOAD REGULATION



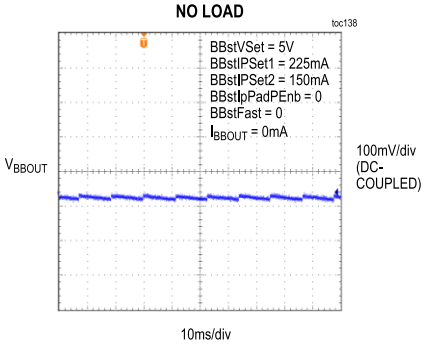
BUCK-BOOST LOAD TRANSIENT FAST MODE ENABLED



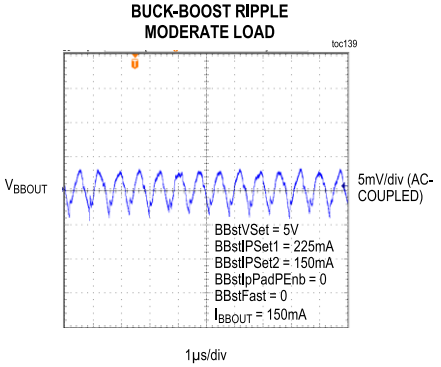
BUCK-BOOST LOAD TRANSIENT FAST MODE DISABLED



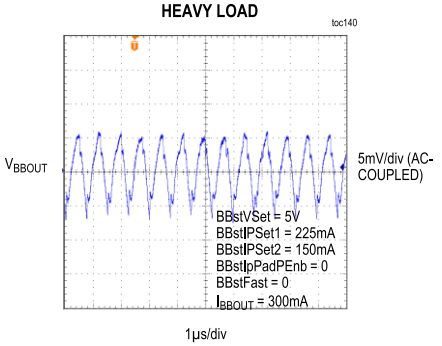
BUCK-BOOST RIPPLE NO LOAD



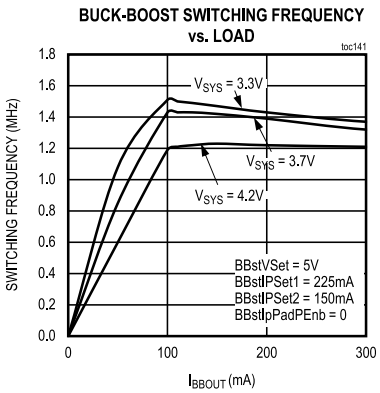
BUCK-BOOST RIPPLE MODERATE LOAD



BUCK-BOOST RIPPLE HEAVY LOAD

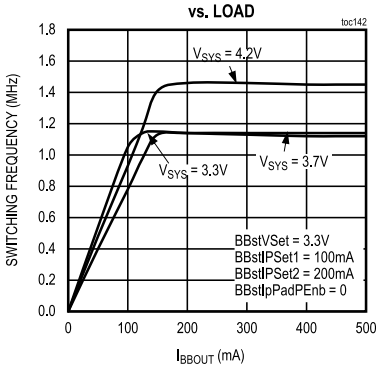


BUCK-BOOST SWITCHING FREQUENCY vs. LOAD

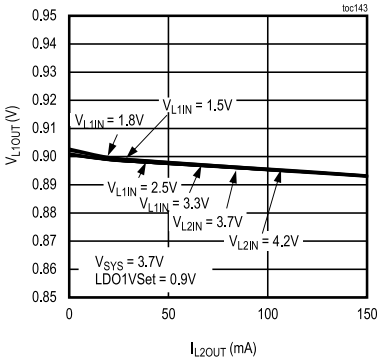


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

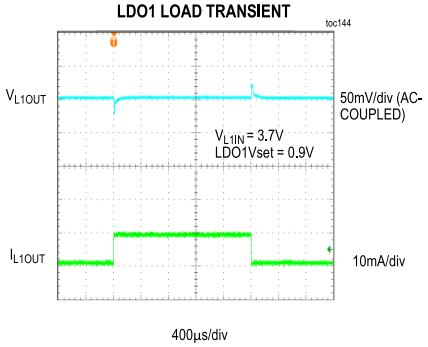
BUCK-BOOST SWITCHING FREQUENCY vs. LOAD



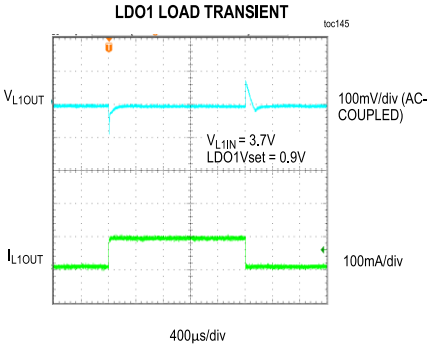
LDO1 LOAD REGULATION



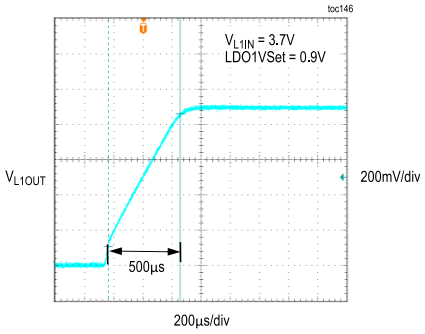
LDO1 LOAD TRANSIENT



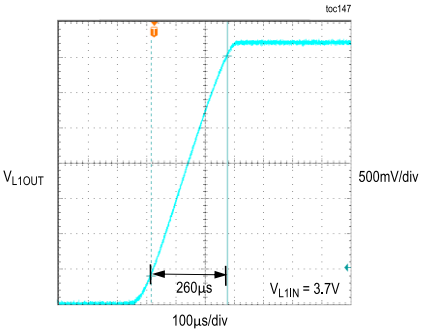
LDO1 LOAD TRANSIENT



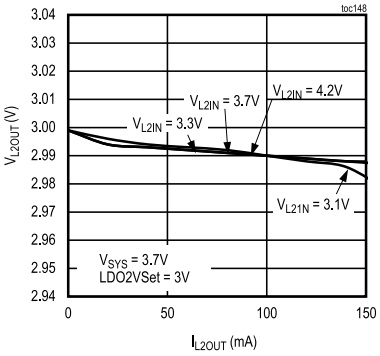
LDO1 LDO MODE TURN-ON TIME



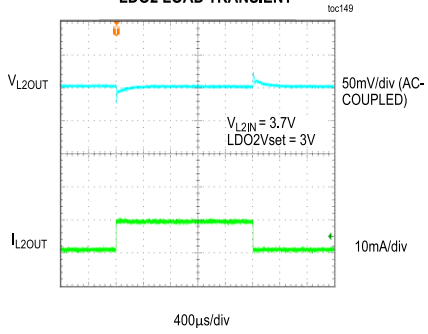
LDO1 SWITCH MODE TURN-ON TIME



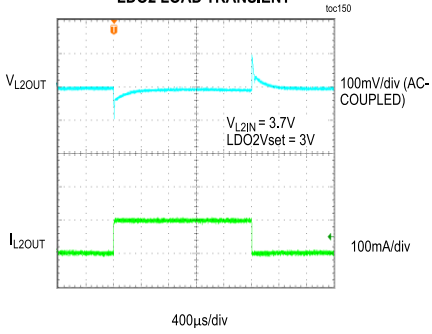
LDO2 LOAD REGULATION



LDO2 LOAD TRANSIENT

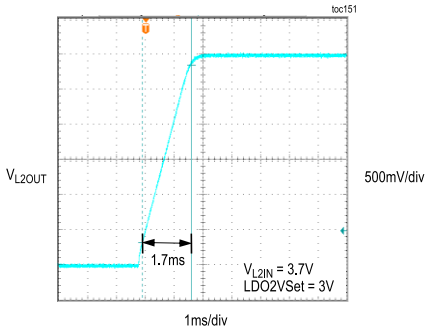


LDO2 LOAD TRANSIENT

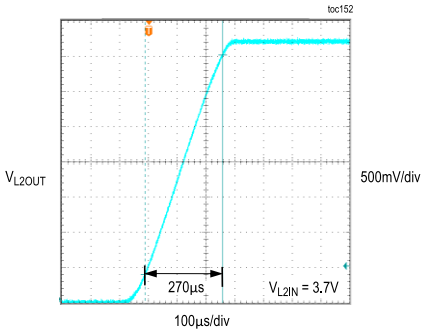


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

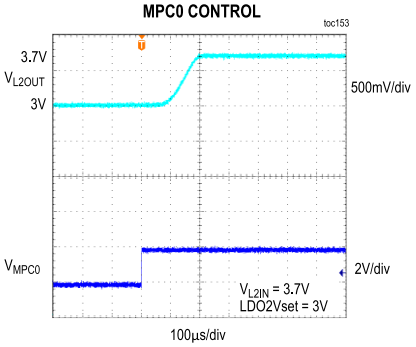
LDO2 LDO MODE TURN-ON TIME



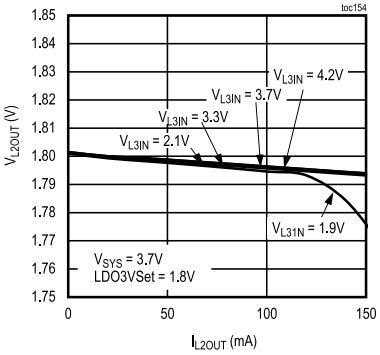
LDO2 SWITCH MODE TURN-ON TIME



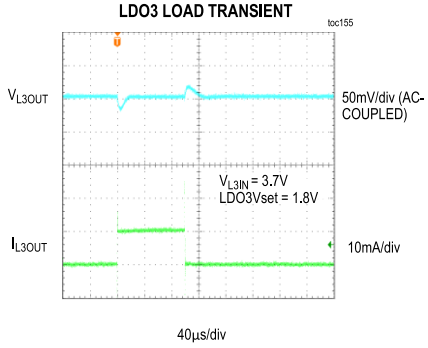
LDO2 LDO MODE TO SWITCH MODE MPC0 CONTROL



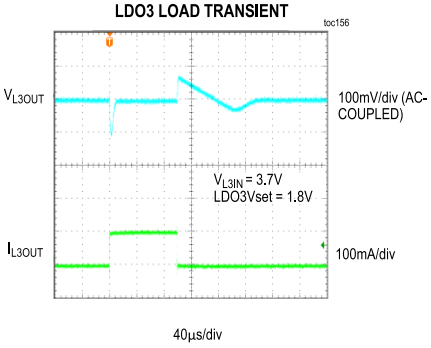
LDO3 LOAD REGULATION



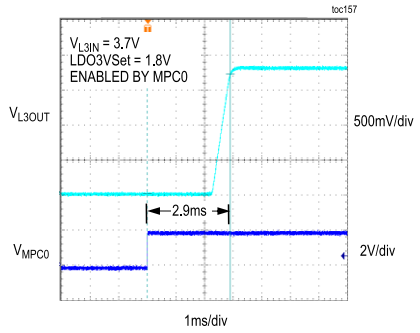
LDO3 LOAD TRANSIENT



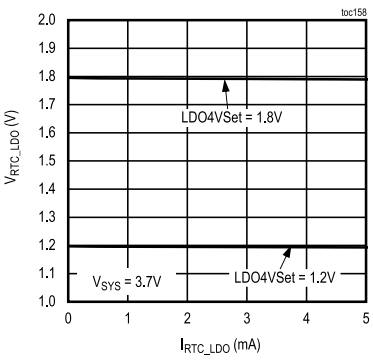
LDO3 LOAD TRANSIENT



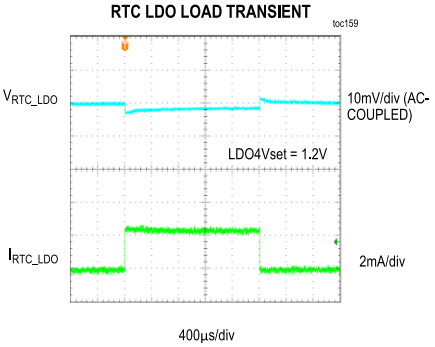
LDO3 TURN-ON TIME



RTC LDO LOAD REGULATION

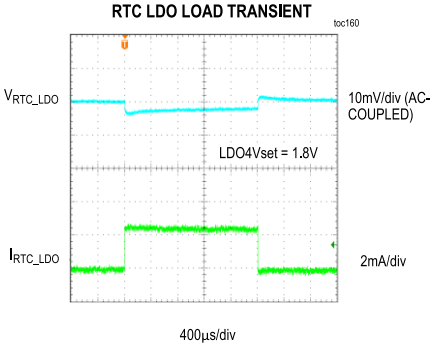


RTC LDO LOAD TRANSIENT

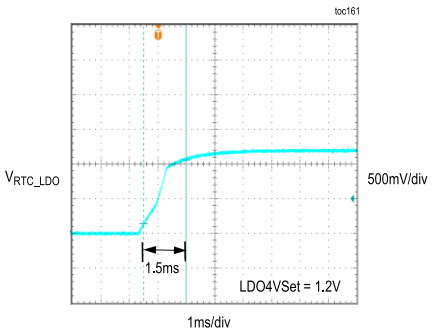


(V_{BAT} = V_{CHGOUT} = 3.7V, C_{CHGIN_EFF} = 1µF, C_{VDIG_EFF} = 1µF, C_{CAP_EFF} = 1µF, C_{SYS_EFF} = 10µF, C_{BAT_EFF} = 1µF, C_{CHGOUT_EFF} = 0.1µF, $C_{BK\_OUT\_EFF}$ = 10µF, $C_{L\_IN\_EFF}$ = 1µF, $C_{L\_OUT\_EFF}$ = 1µF, C_{BBOUT_EFF} = 10µF, L_{BK_OUT} = 2.2µH, L_{BBOUT} = 2.2µH, T_A = +25°C, unless otherwise noted.)

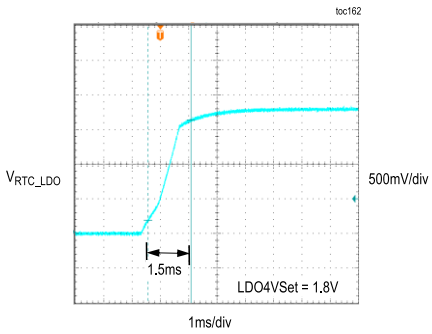
RTC LDO LOAD TRANSIENT



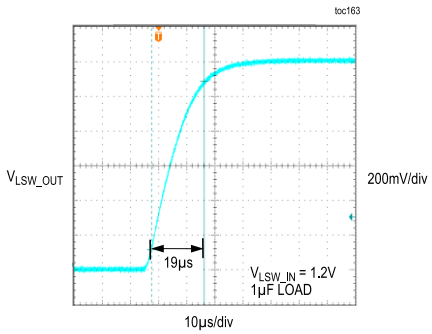
RTC LDO TURN-ON TIME



RTC LDO TURN-ON TIME

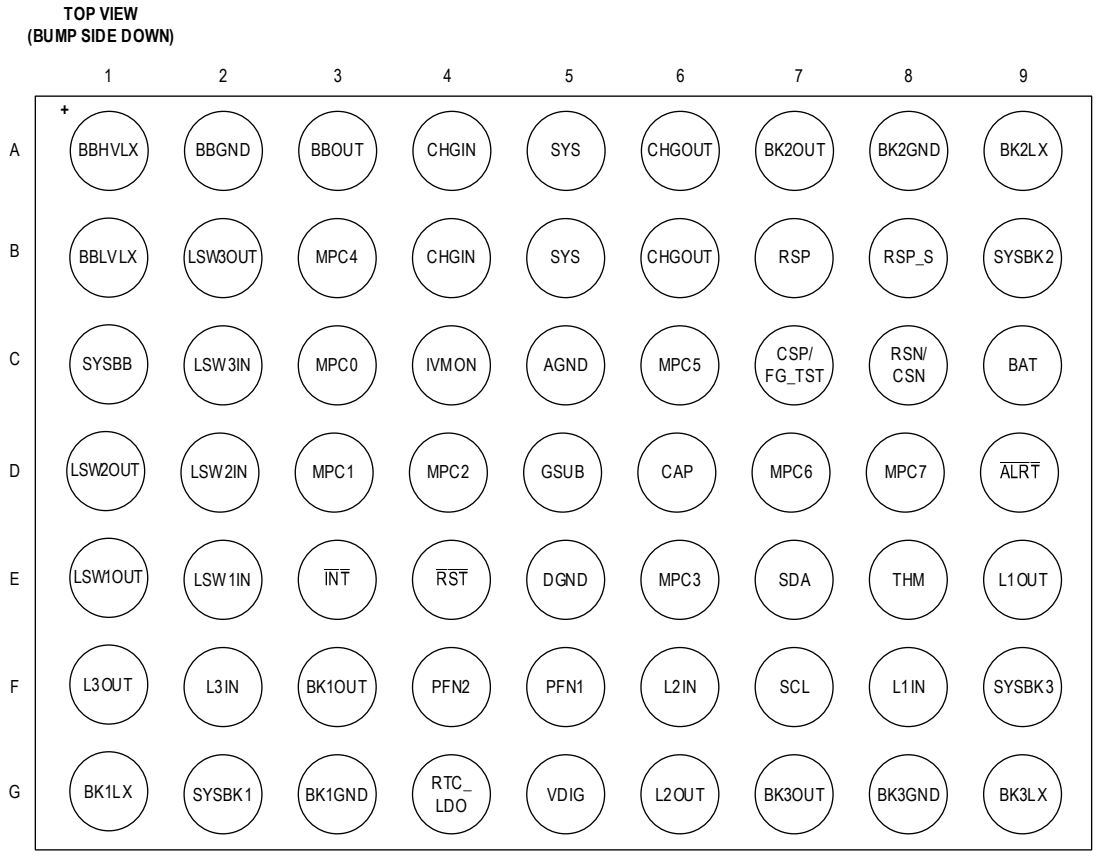


LOAD SWITCH TURN-ON TIME



Pin Configuration

MAX20356



Pin Description

PIN	NAME	FUNCTION
G1	BK1LX	Buck1 Switching LX Node. Connect a 2.2µH inductor to BK1OUT.
F1	L3OUT	LDO3 Output. Bypass with 1µF effective capacitance to ground.
E1	LSW1OUT	Load Switch 1 Output.
D1	LSW2OUT	Load Switch 2 Output.
C1	SYSBB	Buck Boost Power SYS. Connect all SYS pins by means of a SYS plane and bypass with 10µF effective capacitance to ground.
B1	BBLVLX	Buck Boost Switching Node 1. Connect 2.2µH inductance to BBHVLX.
A1	BBHVLX	Buck Boost Switching Node 2. Connect 2.2µH inductance to BBLVLX.
G2	SYSBK1	Buck1 Power SYS. Connect all SYS pins by means of a SYS plane and bypass with 10µF effective capacitance to ground.
F2	L3IN	LDO3 Input. Bypass with 1µF to ground.
E2	LSW1IN	Load Switch 1 Input.

D2	LSW2IN	Load Switch 2 Input.
C2	LSW3IN	Load Switch 3 Input.
B2	LSW3OUT	Load Switch 3 Output.
A2	BBGND	Buck Boost Power Ground. Connect all ground pins with a ground plane.
G3	BK1GND	Buck1 Power Ground. Connect all the ground pins with a ground plane.
F3	BK1OUT	Buck1 Regulator Sensing Output. Bypass to GND according to the *Buck Output Capacitor Selection* section.
E3	$\overline{INT}$	Interrupt Open-Drain Active-Low Output.
D3	MPC1	Multipurpose I/O 1.
C3	MPC0	Multipurpose I/O 0.
B3	MPC4	Multipurpose Pin 6.
A3	BBOUT	Buck Boost Regulator Output. Bypass to ground according to the *Buck-Boost Output Capacitor Selection* section.
G4	RTC_LDO	RTC LDO Output. Bypass RTC_LDO with 1µF effective capacitance to ground.
F4	PFN2	Configurable Power-Mode Control Pin (e.g., $\overline{KOUT}$).
E4	$\overline{RST}$	Reset Open-Drain Output.
D4	MPC2	Multipurpose I/O 2.
C4	IVMON	Voltages and Charging Current Monitor Mux Output.
A4, B4	CHGIN	+28V/-5.5V Protected Charger Input. Bypass with 1µF to ground.
G5	VDIG	Internal 1.8V Reference. Bypass with 1µF to ground.
F5	PFN1	Configurable Power-Mode Control Pin (e.g., $\overline{KIN}$).
E5	DGND	Digital Ground. Connect all the ground pins with a ground plane.
D5	GSUB	Substrate Ground. Connect all the ground pins with a ground plane.
C5	AGND	Analog Ground. Connect all the ground pins with a ground plane.
A5, B5	SYS	System Load Connection. Connect all SYS pins by means of a SYS plane and bypass with 10µF effective capacitance to ground.
G6	L2OUT	LDO2 Output. Bypass with 1µF effective capacitance to ground.
F6	L2IN	LDO2 Input. Bypass with 1µF to ground.
E6	MPC3	Multipurpose I/O 3.
D6	CAP	Internal Reference Supply. Bypass with 1µF real capacitance (after derating) to GND.
C6	MPC5	Multipurpose I/O 5.
A6, B6	CHGOUT	Charger Output. Bypass with 0.1µF effective capacitance to ground. Connect to BAT through the FG sense resistor (external or integrated) or directly.
G7	BK3OUT	Buck3 Regulator Sensing Output. Bypass BK3OUT to ground according to the *Buck Output Capacitor Selection* section.
F7	SCL	I^2C Serial Input Clock.
E7	SDA	I^2C Serial Data Input/Open-Drain Output.
D7	MPC6	Multipurpose I/O 6.
C7	CSP/FG_TST	Fuel Gauge Sensing Resistor Positive Point. Kelvin connect to sense resistor.
B7	RSP	Internal Sense Resistor Forcing Positive Pin.
A7	BK2OUT	Buck2 Regulator Sensing Output. Bypass to ground according to the *Buck Output Capacitor Selection* section.
G8	BK3GND	Buck3 Power Ground. All ground pins must be connected on the PCB using a low-impedance trace, or on the GND plane.
F8	L1IN	LDO1 Input. Bypass with 1µF to ground.

E8	THM	Battery Thermistor Connection.
D8	MPC7	Multipurpose I/O 7.
C8	RSN/CSN	Internal Sense Resistor Negative Forcing Pin/Fuel Gauge Current Negative Sensing Point. Kelvin connect to external sense resistor.
B8	RSP_S	Internal Sense Resistance Positive Sensing Point.
A8	BK2GND	Buck2 Power Ground. Connect all the ground pins with a ground plane.
G9	BK3LX	Buck3 Switching LX Node. Connect 2.2µH to BK3OUT.
F9	SYSBK3	Buck3 Power SYS. All SYS pins must be connected on the PCB using a low-impedance trace or SYS plane. Bypass the common node with a minimum 10µF real capacitance (after derating) to GND.
E9	L1OUT	LDO1 Output. Bypass with 1µF effective capacitance to ground.
D9	$\overline{\text{ALRT}}$	Alert Output. Open-drain active-low which indicates fuel gauge alert. Connect to ground if not used.
C9	BAT	Power Supply and Battery Voltage Sensing Input. Connect to positive battery terminal and bypass with 1µF effective capacitance.
B9	SYSBK2	Buck2 Power SYS. All SYS pins must be connected on the PCB using a low-impedance trace or SYS plane. Bypass the common node with a minimum 10µF real capacitance (after derating) to GND.
A9	BK2LX	Buck2 Switching LX Node. Connect 2.2µH to BK2OUT.

Detailed Description

The MAX20356 is a highly integrated and programmable power-management solution designed for ultra-low-power wearable applications. It is optimized for size and efficiency to enhance the value of the end product by extending battery life and shrinking the overall solution size. A flexible set of power-optimized voltage regulators including multiple buck converters, a buck-boost converter, and linear regulators provide a high level of integration and the ability to create a fully optimized power architecture. The quiescent current of each regulator is ultra-low, targeted at extending battery life in always-on applications.

The MAX20356 includes a complete battery-management solution with battery seal, charger, power path, and fuel gauge. Both thermal management and input protection are built into the charger. The device also includes a factory-programmable button controller with multiple inputs that are customizable to fit specific product user requirements. A low noise, 1.5W buck-boost converter provides highly efficient, low noise power conversion required for the LEDs used in optical heart-rate systems. The device is configurable through an I^2C interface that allows for programming various functions and reading the device status, including the ability to read temperature and supply voltages through the monitor multiplexer.

This device is available in a 63-bump, 0.5mm pitch, 3.71mm x 4.48mm, wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Power Regulation

The MAX20356 features three high-efficiency, low-quiescent current buck regulators (see the *Buck Regulators* section), a buck-boost regulator (see the *Buck-Boost Regulator* section), three low-quiescent current, low-dropout linear regulators (LDOs) (see the *LDOs* section), one low-quiescent current RTC low-dropout linear regulator, and three dedicated load switches (see the *Load Switches* section). Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The buck and buck-boost can operate in a fixed peak current mode for low-current applications or an adaptive peak-current mode to improve load regulation, extend the high-efficiency range, and minimize capacitor size when more current is required.

Dynamic Voltage Scaling

All of the MAX20356 regulators (except fast transient LDO3) feature dynamic voltage scaling (DVS) to scale the output voltage without disabling the converter. The regulator output voltages are set by direct I^2C writes to the corresponding VSet register. In addition to I^2C DVS, the buck regulators feature two additional control methods for applications where timing is critical: GPIO DVS and SPI DVS. Note that the output-voltage slew rate remains the same in all DVS modes.

Buck DVS transitions maximize the output-voltage slew rate while controlling inrush current for devices that require fast voltage transitions. The other regulators minimize inrush current by limiting the output-voltage slew rate. A typical DVS transition on a buck regulator has a rise time of 10µs.

DVS Mode 0 (I^2C DVS Mode)

DVS Mode 0 configures the regulator outputs to be controlled by I^2C. If Buck_DvsCfg = 00000 (see the Buck1DvsCfg, Buck2DvsCfg, and Buck3DvsCfg bits), the output voltage of that regulator is controlled by I^2C writes to the Buck_VSet bitfield (see the Buck1VSet, Buck2VSet, and Buck3VSet bits). Note that a regulator in I^2C DVS mode must be unlocked before modifying the output voltage. Regulators are unlocked by setting their lock mask bit to 0 in LockMsk1 (see the LockMsk1 bit) and writing the unlock password 0x55 to the LockUnlock1 register (see the LockUnlock1 register).

DVS Mode 1 (GPIO DVS Mode)

In DVS Mode 1, two MPC inputs select the regulator output from four programmed values. To configure a regulator output for GPIO mode, set the corresponding Buck_DvsCfg bits (see the Buck1DvsCfg, Buck2DvsCfg, and Buck3DvsCfg bits) to any value between 00001 and 11100. Each code selects a different pair of MPC_ pins to control the regulator. See the Buck_DvsCfg register descriptions (see the Buck1DvsCfg, Buck2DvsCfg, and Buck3DvsCfg bits) for details on which MPC inputs are used for a code. In each case, the first MPC listed controls the lower bit and the second MPC controls the higher bit.

The four Buck_DvsVlt_ bitfields (see the Buck1DvsVlt0, Buck1DvsVlt1, Buck1DvsVlt2, Buck1DvsVlt3, Buck2DvsVlt0, Buck2DvsVlt1, Buck2DvsVlt2, Buck2DvsVlt3, Buck3DvsVlt0, Buck3DvsVlt1, Buck3DvsVlt2, and Buck3DvsVlt3 bits) are loaded with the corresponding regulator's factory-default voltage when the MAX20356 first powers on. After the start-up process, each 6-bit output-voltage level can be programmed using the I^2C for each converter in the Buck_DvsVlt_

bitfields. As the MPC inputs change, the regulator output adjusts to the newly selected level as shown in *Figure 1*. Voltage levels are selected as shown in *Table 1*.

Table 1. DVS Mode 1 Voltage Selection

GPIO1	GPIO0	DVS VOLTAGE
0	0	Vlt0
0	1	Vlt1
1	0	Vlt2
1	1	Vlt3

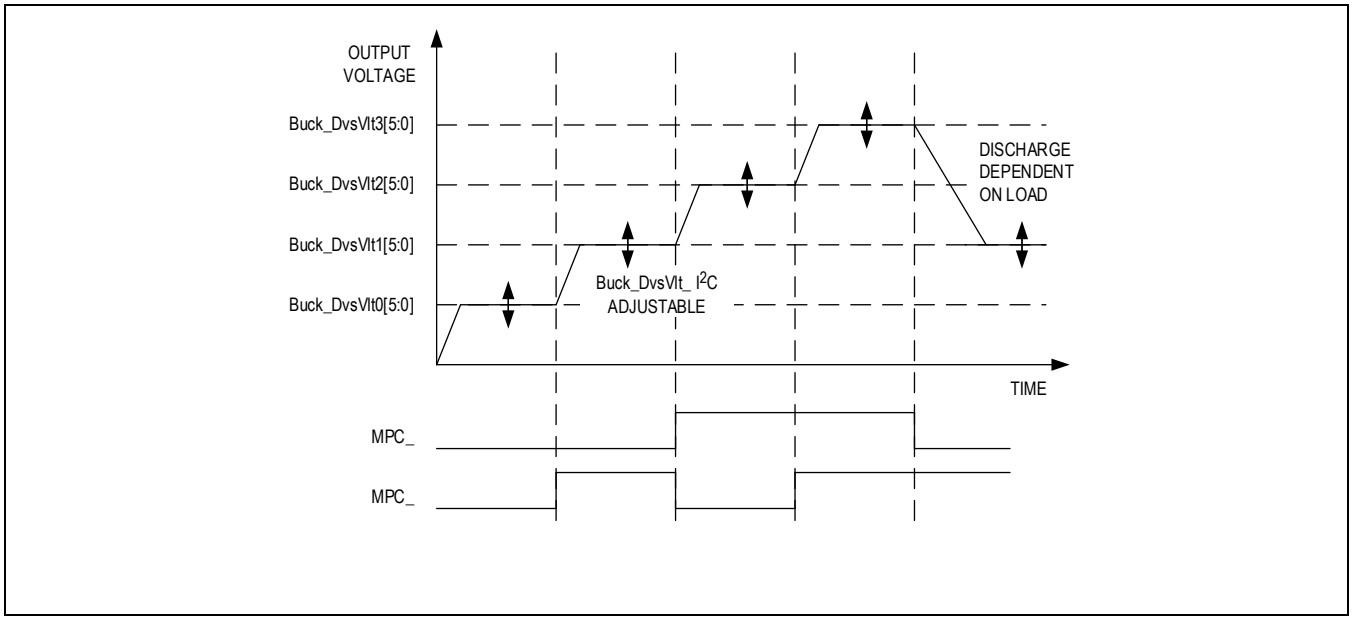


Figure 1. DVS Mode 1, GPIO Control

SPI DVS Mode (DVS Mode 2)

In DVS Mode 2, the regulator voltages are changed by writing command bytes to a 3-wire SPI interface. The SPI interface uses the MPC0, MPC1, and MPC2 pins. MPC0 becomes the active-low chip select pin $\overline{CS}$, MPC1 becomes the clock SCLK with polarity 0, and MPC2 becomes the data input pin DIN. Data is clocked in on the SCLK rising edge. The maximum SPI clock frequency is 8MHz. A command byte comprises two address bits (ADD[1:0]) that select the regulator and six voltage bits (VLT[5:0]) that set the voltage. *Figure 2* shows how data is clocked in SPI mode.

The output voltage is latched on the 8th rising edge of the clock. Note that voltages set by the SPI interface are mirrored in the Buck_SPIVlt bitfields for each converter and readback must be done over I^2C. *Figure 3* shows two regulators controlled in DVS Mode 2.

The DVS SPI interface supports single-byte and burst-mode data transfer. In single-byte mode, $\overline{CS}$ goes high after each command byte is transferred. In burst-mode, all command bytes are written to the MAX20356 before $\overline{CS}$ returns high. *Figure 4* shows how data is written in both modes.

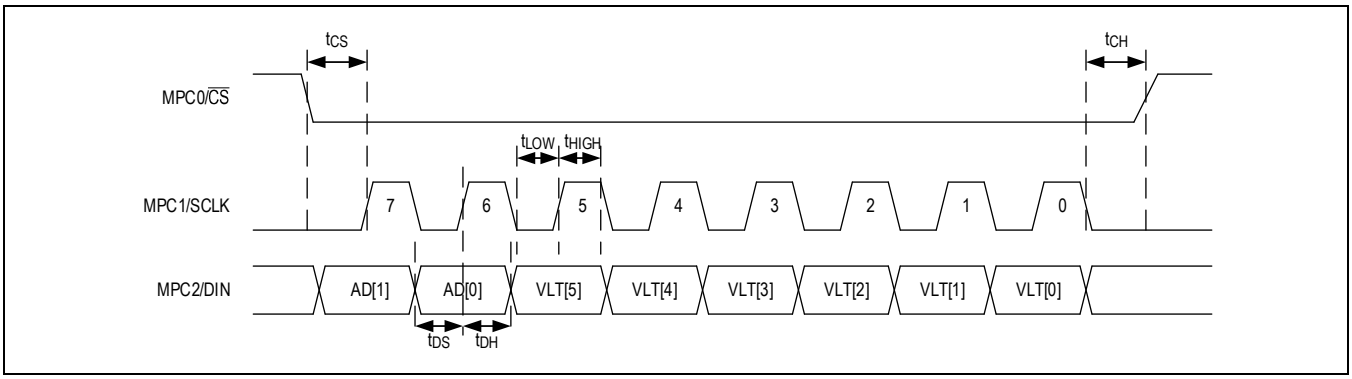


Figure 2. DVS Mode 2, SPI Timing

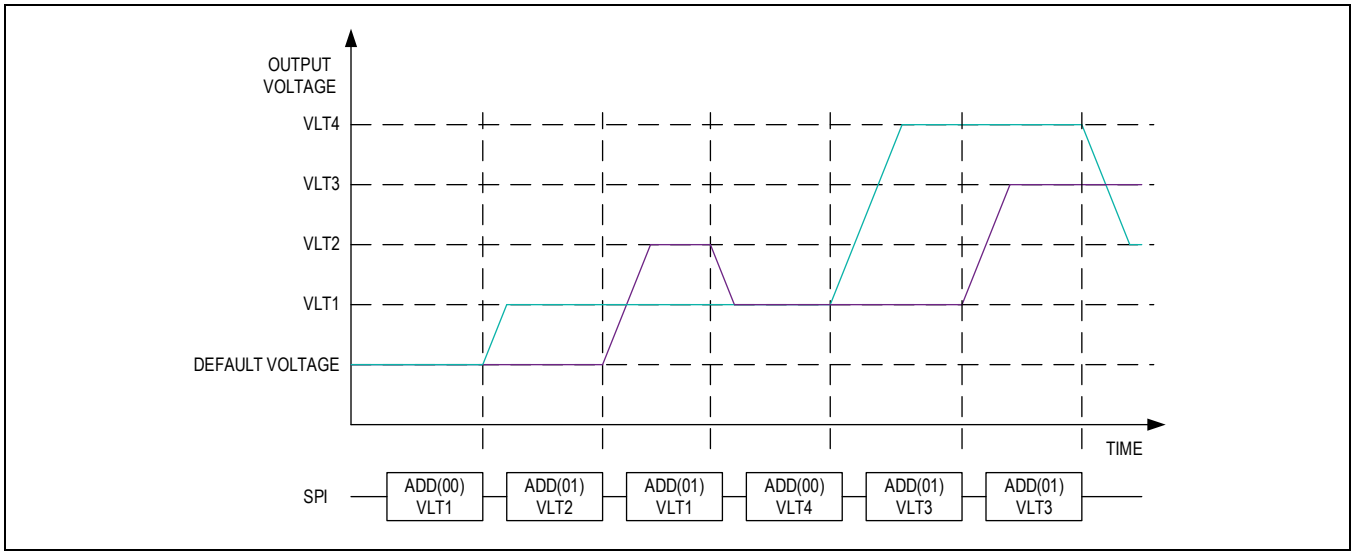


Figure 3. DVS Mode 2, SPI Control

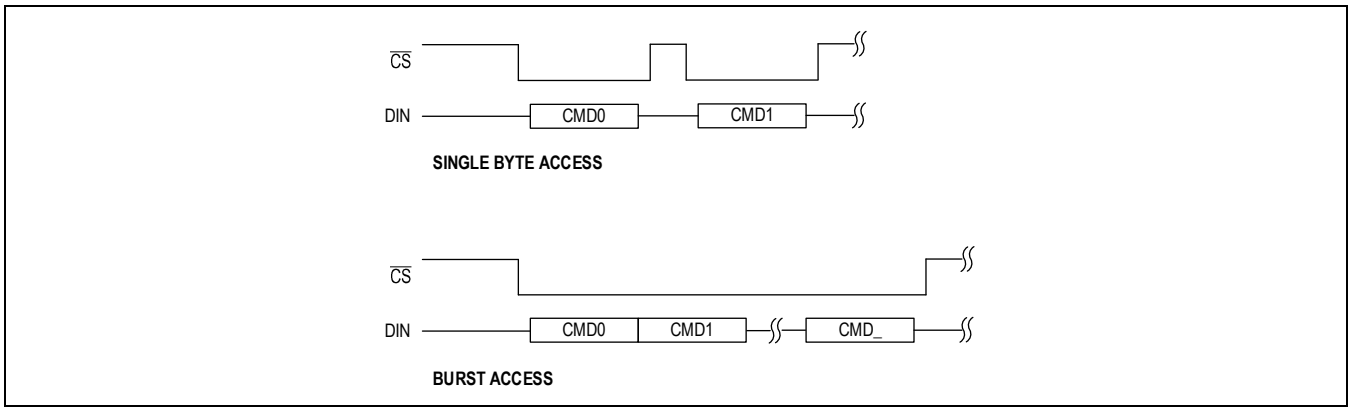


Figure 4. Single-Byte and Burst-Mode SPI Access

Dedicated DVS Interrupts

To quickly alert a host processor when a DVS transition is complete, the MAX20356 features the option to configure the MPC0–MPC6 pins as dedicated PGOOD interrupts. To configure the dedicated interrupt, write the desired BK_MPC_Sel bit(s) in registers 0x7B–0x7D. Additionally, interrupts signalling changes in the ADC, and USBOk statuses are available as dedicated MPC interrupts as well.

Buck Converter DVS Options

The MAX20356 buck converters feature two DVS valley current settings that can be selected using the Buck_DVSCur bits. Both 500mA and 1A settings are available. The 500mA valley-current setting offers a slightly slower transition time while minimizing the voltage overshoot that can occur due to demagnetization of the inductor at the end of the transition. The 1A valley-current setting offers the fastest DVS transition time, but can exhibit overshoot due to inductor demagnetization. Care should be taken that the overshoot is not potentially damaging to downstream devices.

LDOs

The MAX20356 features four integrated LDOs:

- LDO1 and LDO2 are standard low quiescent current LDOs.
- LDO3 is a low quiescent current LDO with ultra-fast transient response that is optimized for use in biosensing applications.
- The RTC LDO is a low quiescent current LDO that is optimized to supply power for a real time clock or dedicated always-on power supply to a microcontroller at either 1.2V or 1.8V. See the *Electrical Characteristics* section for detailed specifications on each LDO.

LDO Output Capacitance Selection

The LDOs on MAX20356 are designed to operate with a minimum of 1µF of effective capacitance on the output. Capacitance derating with DC voltage bias and other factors should be taken into consideration when making the capacitor selection.

LDO2 MPC0 Control

LDO2 can be enabled using an MPC input and are configurable as load switches. Setting the LDO2_MPC0CNT (see bit: LDO2_MPC0CNT) bit to 1 configures LDO2 to be controlled by MPC0 based on the state of LDO2_MPC0CNF (see bit: LDO2_MPC0CNF). If LDO2_MPC0CNF = 0, MPC0 changes LDO2 between LDO mode and switch mode. If LDO2_MPC0CNF = 1, then MPC0 enables or disables LDO2 in switch mode. See *Table 2* for LDO2 MPC0 control detail. Using this MPC control allows the state of LDO2 to be changed much more quickly than through I^2C writes on the order of microseconds. Rapid control of LDO2 supports applications that require minimal delays. For example, quickly increasing the LDO2 output voltage by changing from LDO mode to switch mode reduces the time required for an application processor to transition from a low-power sleep mode to a higher-voltage active state.

Table 2. LDO2 MPC0 Control

LDO2En	LDO2_MPC0CNF	LDO2_MPC0CNT	MPC0 CONTROL
00	1	1	MPC0 control switch mode on/off
01	0	1	MPC0 control LDO mode or switch mode
	1	1	
10	1	1	MPC0 control switch mode on/off
11	1	1	MPC0 control switch mode on/off

Internal Switchover for LDO1 Always-On Power

To power LDO1 when no battery voltage is present, an internal switchover circuit is available. This switchover circuit requires that the LDO be bypassed at the L1IN node by 1µF of capacitance. The L1IN node must otherwise be left unconnected. The switchover circuit automatically powers the LDO from a regulated voltage off of CHGIN so that it is powered even if no battery is present. This option can be enabled by default at the factory or left disabled by default. Either way, the behavior is programmable by I^2C after startup. This function is intended to support an output voltage of 1.8V or lower and a load current of 100µA (max) or smaller. The R_{ON_L1IN} specification in the *Electrical Characteristics* section is used to generate the worst-case output-power capability based on the minimum input voltage from V_{CCINT} (see *Note 2*), maximum output voltage of LDO1, and the maximum on-resistance. LDO1 can be always-on if the LDO1Seq is 001 in OTP.

Fast Transient LDO

The MAX20356 is equipped with a fast transient LDO3 for use of AFE sensors. If any LDO3 fault occurs, the LDO3 autoretry after 1 second.

RTC LDO

The MAX20356 features a new RTC LDO which can be configured as an always-on regulator. To have RTC LDO enabled as always on, register bits MiscFunc[1] and LDO4Seq bits must be set to 0 and 001.

To use RTC LDO always-on feature, the MiscFunc[1] needs to be set to 0 by OTP and also 0 when entering different mode. Otherwise, if the MiscFunc[1] is 1 by OTP, the LDO4 state gets reset to default when enter off/hard-reset/soft-reset (if SftRstCfg=Reset Regs)/battery recovery mode. If MiscFunc[1] is 0 by OTP, the LDO4 state is kept when enter off/hard-reset/soft-reset/battery recovery mode.

Load Switches

The MAX20356 load switches allow a system to disconnect loads when inactive to reduce quiescent current. To limit inrush on enabled, each load switch initially behaves as a constant current source with the I_{SW_START} value. Current mode remains until the switch output is charged to meet the condition V_{SW_IN} - V_{SW_OUT} < V_{SW_PROT}. Once the condition is met, the switch turns fully on and connects LSW_IN to LSW_OUT. If this condition is not met within the startup time-out t_{STUP_LSW}, the switch attempts to turn on after a retry delay t_{RETRY_LSW}.

Both switches feature optional voltage protection to prevent overcurrent. A protection comparator monitors the difference between the input and output voltages. If the difference exceeds V_{SW_PROT}, the switch is opened to protect downstream circuitry. The comparator can be disabled with the LSW_LowIq bit to reduce quiescent current if the upstream power supply has its own overcurrent protection. Be aware that by disabling the protection comparator, the current during a short circuit to GND could be 6A typical.

Buck-Boost Regulator

The MAX20356 buck-boost regulator provides a low-ripple voltage rail that can be used for voltage regulation near or above the battery voltage. The buck-boost is sized to be ideal in powering LEDs used in photoplethysmography (PPG) systems. This includes PPG systems with short wavelength LEDs that require large forward voltage drops. The buck-boost topology as well as the dynamic voltage scaling capabilities allow the user to adjust the output voltage to accommodate as little headroom on the LED current sink as possible to maximize efficiency.

Several other controls help to optimize the efficiency and output noise of the regulator. These include peak current control and automatic peak and valley current adjustment. Additionally, the buck-boost regulator can operate in buck-only mode to increase efficiency when V_{BBOUT} is much lower than V_{SYS}.

Buck-Boost Inductor Selection

Inductor selection for the MAX20356 should be optimized for the intended application. A 2.2µH inductor value is required for this buck-boost. Aside from the inductor value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L\_MAX} = \frac{V_{OUT\_MAX} \times I_{OUT\_MAX}}{\eta \times V_{IN\_MIN}}$$

Where:

V_{OUT_MAX} = Maximum expected operating voltage.

I_{OUT_MAX} = Maximum expected output current.

V_{IN_MIN} = Minimum expected operating input voltage.

η = Expected worst-case efficiency in the minimum input voltage and maximum output power case (see the *Typical Operating Characteristics* section for help in estimating efficiency).

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. To determine the required inductor saturation current, the peak current must be calculated. The worst case peak current for this converter can be calculated as the higher value of:

$$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times (BBstIPSet1 + BBstIPSet2)}{2} + 100mA$$

and

$$I_{L\_PEAK\_DCM} = 1.15 \times (BBstIPSet1 + BBstIPSet2) + 100mA$$

If I_{L_PEAK} is expected to occur when V_{IN} is lower than V_{OUT} by at least 100mV, a less pessimistic assumption can be taken as the lower of:

$$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times BBstIPSet1}{2} + 100mA$$

and

$$I_{L\_PEAK\_DCM} = 1.15 \times BBstIPSet1 + 100mA$$

Where:

BBstIPSet1 and BBstIPSet2 are the peak current settings.

When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally, magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, ferrite inductors should be avoided as they tend to exhibit poor AC characteristics, especially in DCM. See *Table 3* for inductor recommendations for a given optimization parameter.

Table 3. Recommended Inductors

OPTIMIZATION PARAMETERS	VENDOR	PART NUMBER
Efficiency	Murata	DFE201610E-2R2M
Size	Murata	DFE18SBN2R2MEL

Buck-Boost Output Capacitor Selection

The buck-boost is designed to be compatible with small case-size ceramic capacitors. As such, the device has low output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) case-size capacitors. The sample derating curve in *Figure 5* shows the required minimum capacitance for the BBOUT node.

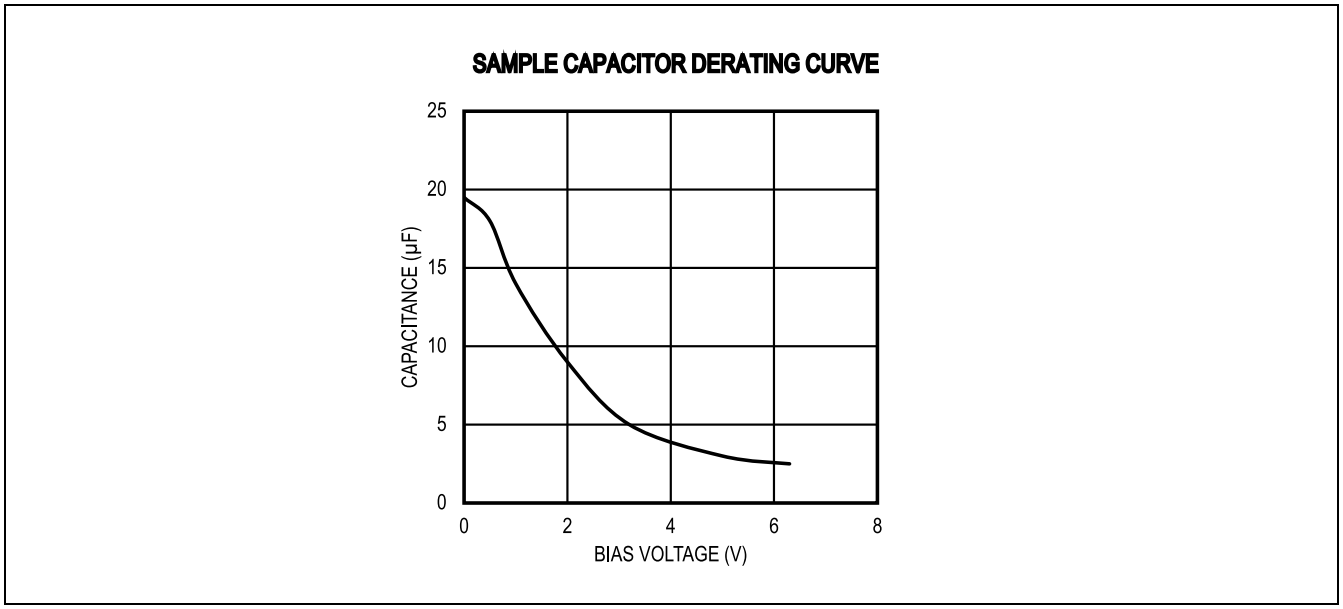


Figure 5. Buck-Boost Required Minimum Output Capacitance

Architecture and Switching Phases

The buck-boost comprises a typical noninverting buck-boost topology. *Figure 6* illustrates the regulator's basic structure with arrows showing the current flow in each switching phase. Depending on the register settings and input-to-output voltage relationship, the buck-boost sequences through the switching phases below in a particular order to deliver charge to the output. At most, two switches are on in any given phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.
- Phase 3: MN1 on, MP2 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

The buck-boost features a frequency comparator to monitor its switching frequency. Switching frequency increases as the load current increases. Under light loads, the buck-boost optimizes its feedback loop for low quiescent current. When load requirements increase the switching frequency to the f_{HIGH} threshold, the low-quiescent current mode is disabled to improve response time. The transition above this threshold generates a discontinuity in the output-voltage ripple. If the transition occurs at a sensitive current causing noise on the output at a critical frequency, adjustment of the f_{HIGH} threshold is recommended with the trade-off of a slight decrease in light load efficiency. The f_{HIGH} threshold is set by the BBFHighSh setting in the BBstCfg1 register (see the BBstCfg1 register). Hysteresis prevents the buck-boost regulator from resuming the low-quiescent current mode until the switch frequency decreases to $f_{HIGH}/4$.

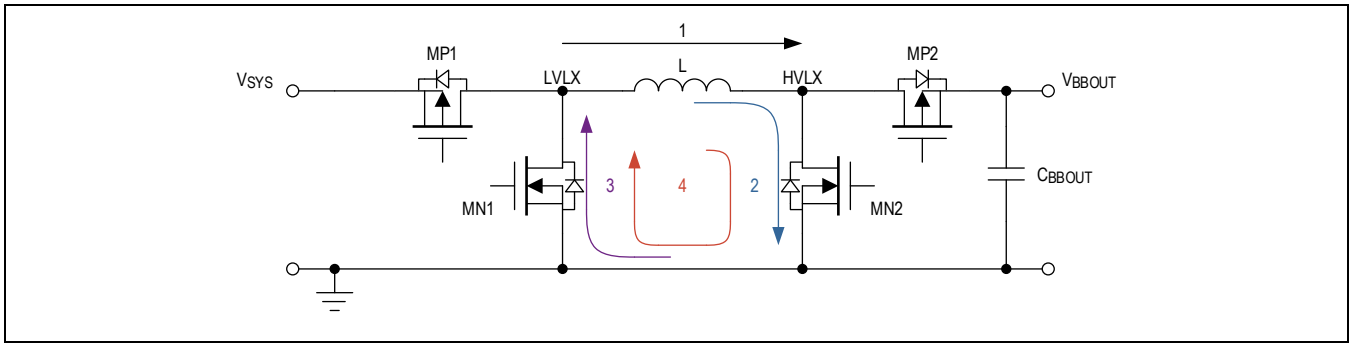


Figure 6. Buck-Boost Regulator and Switching Phases

Buck-Boost Mode

When BBstMode (register 0x55[1]) is 0, the regulator operates in buck-boost mode. The inductor charges in phase 2 up to BBstIPSet1 (register 0x57[3:0]). This minimizes noise when V_{SYS} is close to V_{BBOUT}. The buck-boost then transitions to phase 1. If $V_{SYS} > V_{BBOUT}$, the inductor continues charging until either the current reaches BBstIPSet1 + BBstIPSet2 (register 0x57[7:4]) or after a 500ns delay. If $V_{SYS} \leq V_{BBOUT}$, the buck-boost waits for the 500ns delay to elapse or until the current drops to the valley limit. Next, the regulator enters phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters phase 4 for approximately 30ns if BBZCCmpEnb = 1. The buck-boost skips phase 4 when operating in CCM and BBZCCmpEnb = 0. The valley behavior is determined by BBZCCmpEnb (register 0x58[4]). *Figure 7* shows the inductor current in buck-boost mode.

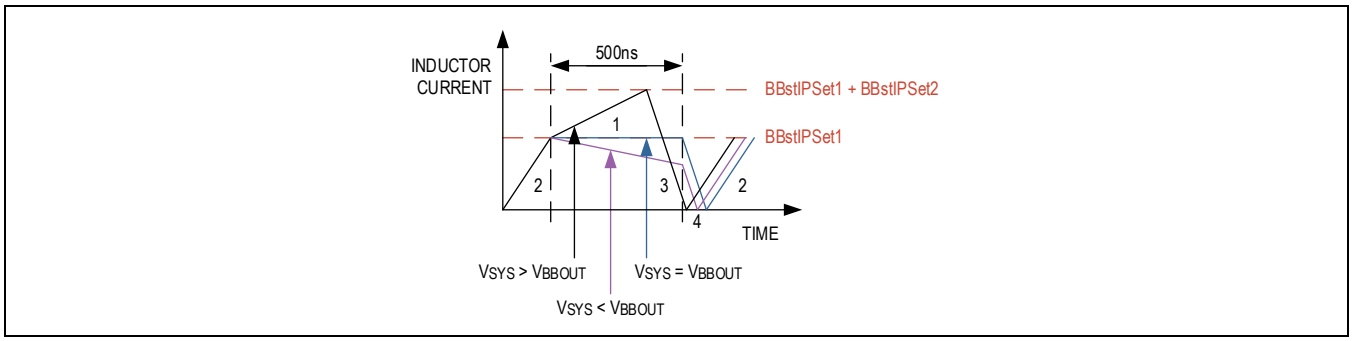


Figure 7. Buck-Boost Inductor Current in Buck-Boost Mode

Buck-Only Mode

To maximize efficiency when $V_{SYS} > V_{BBOUT}$, the buck-boost regulator has a buck-only mode. When BBstMode = 1, the regulator behaves as a synchronous buck regulator. The inductor charges in phase 1 until the inductor current reaches BBstIPSet1. The regulator then transitions to phase 3 to provide a path to deliver the inductor current to the output. *Figure 8* shows the inductor current in buck-only mode.

Buck-only mode reduces switching losses present in buck-boost mode. Buck-only mode should be used when V_{BBOUT} is always less than V_{SYS} to maximize efficiency.

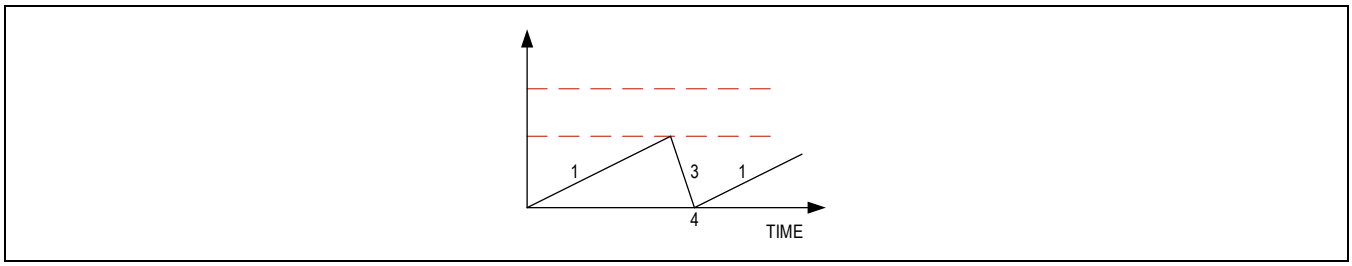


Figure 8. Buck-Boost Inductor Current in Buck-Only Mode

Buck-Boost Inductor Peak and Valley Current Limits

The buck-boost regulator monitors the maximum and minimum values of the inductor current. Peak and valley currents can be fixed to the values in BBstIPSet_ and 0mA, respectively (see the BBstIPSet1 and BBstIPSet2 bits), or allowed to change based on load requirements if BBstIpPadPEnb = 0 (see the BBstIpPadPEnb bit).

Peak currents are set in the BBstISet register (see the BBstISet register). BBstIPSet1 controls the peak current when $V_{SYS} < V_{BBOUT}$ and when the regulator is in buck-only mode. BBstIPSet2 sets a secondary current limit when $V_{SYS} > V_{BBOUT}$ in buck-boost mode. The total inductor current limit when $V_{SYS} > V_{BBOUT}$ is BBstIPSet1 + BBstIPSet2. The buck-boost regulator transitions from phase 1 to phase 3 if the inductor current reaches BBstIPSet1 + BBstIPSet2 or if the 500ns timeout has elapsed. Minimizing the difference between BBstIPSet1 and BBstIPSet2 reduces the output ripple, but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. *Figure 9* presents the safe operating area of BBstIPSet2 with respect to BBstIPSet1. Selecting values lower than those of *Figure 9* for a given value can reduce efficiency and increase output ripple. *Figure 10* is a graphical guide to selecting combinations of BBstPSet1 and BBstIPSet2 to maximize efficiency for specific BBstVSet values.

To maximize the ease of implementation, the peak current settings of the buck-boost regulator are automatically adjusted to the settings shown in *Figure 10* for a given output voltage when BBstIPSetLookUpb = 0. If a different peak current setting is desired, the BBstIPSetLookUpb = 1 setting must be selected. Only then will BBstIPSet1 and BBstIPSet2 have an effect (see the BBstIPSetLookUpb bit). When BBstIpPadPEnb = 0 (see the BBstIpPadPEnb bit), the regulator automatically increases the peak current limits when the load increases to improve load regulation and efficiency at high loads. When BBZCCmpEnB = 1 (see the BBZCCmpEnB bit), the buck-boost operates with peak and valley current limits. In discontinuous conduction mode (DCM), the valley limit is 0mA and it acts as a zero crossing. In CCM, the peak and valley limits are automatically adjusted by the voltage loop if BBstIpPadPEnb = 0 (see the BBstIpPadPEnb bit). However, when BBZCCmpEnB = 0 (see the BBZCCmpEnB bit), the buck-boost operates with peak, valley, and zero crossing

current limits. The zero crossing limit is fixed at 0mA while the peak and valley limits are adjusted by the voltage loop if BBstIpPadPEnb = 0 (see the BBstIpPadPEnb bit).

In DCM, the valley current limit is negative so the end of phase 1 or 3 is determined by the zero-crossing current. In CCM, the valley current limit is ≥ 0mA if BBZCCmpEnB = 0 (see the BBZCCmpEnB bit). The end of phase 1 or 3 is therefore determined by the valley current comparator.

Disabling the zero current crossing comparator reduces the buck-boost output ripple. Enabling the comparator improves EMI in CCM by removing the phase 4 stage in CCM mode that is otherwise present when BBZCCmpEnB = 1 (see the BBZCCmpEnB bit).

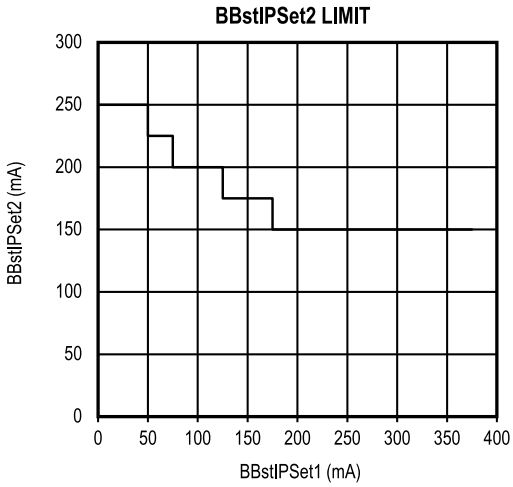


Figure 9. Minimum BBstIPSet2 Limit for a Given BBstIPSet1 Setting

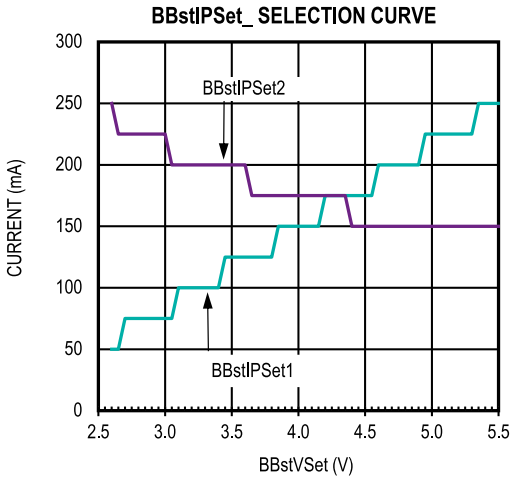


Figure 10. Recommended BBstIPSet1 and BBstIPSet2 Settings

Buck Regulators

The MAX20356 includes three low-power 400mA buck regulators. All of the buck regulators operate in a pulse-frequency modulation (PFM) scheme with peak and valley current control. At light loads, the buck converters operate in discontinuous conduction mode (DCM) to maximize efficiency. The buck regulators have minimum and maximum capacitance requirements. The effective output capacitance of each buck should fall within these limits to guarantee stable operation. *Figure 11* illustrates the minimum and maximum capacitance for each output-voltage setting.

Buck Inductor Selection

Inductor selection for the MAX20356 should be optimized for the intended application. A 2.2µH inductor value is strongly preferred for these buck converters. A 1µH inductor is acceptable, but results in decreased efficiency with only marginal load transient response benefits. Aside from the inductor-value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is simply equal to the maximum output current expected in the application.

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. To determine the required inductor saturation current, the peak current must be calculated. The peak current for this converter can be calculated as the higher value of the following equations:

$$I_{L\_PEAK\_CCM} = I_{L\_MAX} + \frac{1.15 \times Buck\_ISet}{2} + 100mA$$

and

$$I_{L\_PEAK\_DCM} = 1.15 \times Buck\_ISet + 100mA$$

Where:

Buck_ISet is the peak current setting for the relevant buck converter and I_{L_MAX} is the maximum expected load current on the converter.

When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally, magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, ferrite inductors should be avoided as they tend to exhibit poor AC characteristics, especially in DCM. See *Table 4* for inductor recommendations for a given optimization parameter.

Table 4. Recommended Inductors Buck

OPTIMIZATION PARAMETERS	VENDOR	PART NUMBER
Efficiency	Murata	DFE201610E-2R2M
Size	Murata	DFE18SBN2R2MEL

Buck Output Capacitor Selection

The bucks are designed to be compatible with small case-size ceramic capacitors. Therefore, the device has low output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) case-size capacitors. Additionally, there is a maximum output capacitance requirement to maintain stability. The required minimum and maximum capacitance requirements in *Figure 11* show the required capacitance for the BK_OUT node.

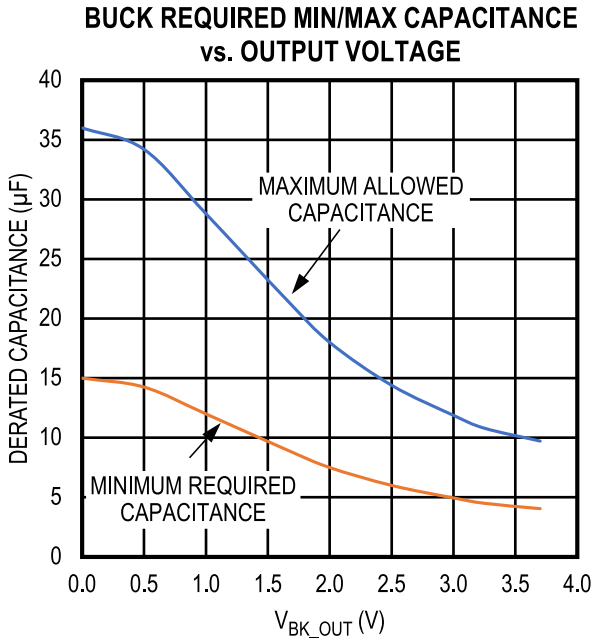


Figure 11. Buck Required Minimum and Maximum Capacitance to Guarantee Stability

Buck Inductor Peak and Valley Current Limits

When a buck regulator is in DCM, the inductor's minimum current threshold (I_{VALLEY}) is 0mA and the inductor's peak current threshold (I_{PEAK}) is set automatically to the optimal value (as shown in *Figure 12*) by the regulator's automatic look-up table or by the Buck_ISet register (see the Buck1ISet, Buck2ISet, and Buck3ISet bits) if Buck_ISetLookUpb = 1 (see the Buck1ISetLookUpb, Buck2ISetLookUpb, and Buck3ISetLookUpb bits). In this mode, as the load increases the switching frequency also increases in accordance with the PFM control scheme.

As the load continues to increase, the switching frequency of the buck regulator eventually reaches approximately 1.1MHz. At this point, if the buck regulator adaptive current setting is enabled (Buck_EnbIADPT = 0) (see the Buck1EnbIADPT, Buck2EnbIADPT, and Buck3EnbIADPT bits) I_{PEAK} and I_{VALLEY} shift upward maintaining a roughly constant offset between themselves (set by the inductor peak current setting described in the first paragraph above). Once the valley current begins to increase, the regulator is operating in continuous conduction mode (CCM) as the inductor is no longer discharged completely to 0mA. The slope of the switching frequency flattens and rises only marginally for the remainder of the load range. This control scheme seeks to balance both the ohmic losses arising from the peak current level and the switching losses incurred by driving the gates of the FETs, extending load regulation and high efficiency over a wider range of loads.

If the adaptive current setting is disabled (Buck_EnbIADPT = 1) (see the Buck1EnbIADPT, Buck2EnbIADPT, and Buck3EnbIADPT bits), the switching frequency continues to rise until the regulator reaches critical conduction mode. As the load increases past critical conduction mode, the switching frequency saturates and the buck regulator behaves as a current source. This results in increased load regulation error at the output of the regulator.

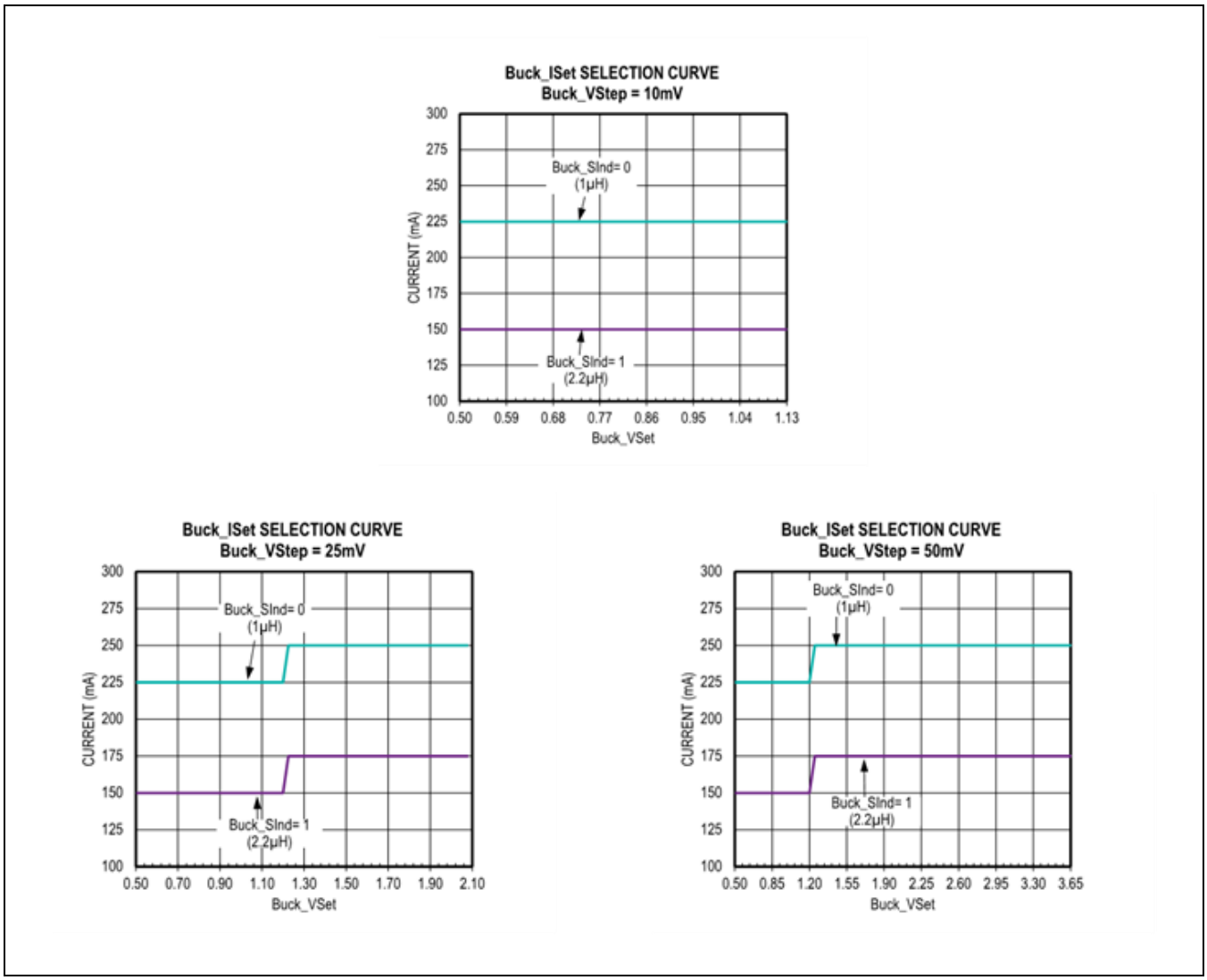


Figure 12. Optimal Peak Current Setting vs. Output Voltage

Adjustments to Manipulate Buck Switching Frequency

In some applications, the buck output-voltage ripple can generate noise at frequencies that interfere with sensitive analog circuitry. The adjustable peak current of the MAX20356 provides the flexibility to shift the ripple frequency out of the sensitive frequency ranges when the regulator is in DCM mode. Increasing the peak current delivers more charge to the output capacitor in a switching cycle, thereby decreasing the number of times the output capacitor requires charging to supply the same load. In this case, the output ripple frequency decreases for a given load current and shifts below sensitive, high-frequency ranges. Conversely, decreasing the peak current increases the switching frequency for a given load current to prevent injecting noise in sensitive, low-frequency ranges.

Note that increasing the peak current results in higher ohmic losses, which can lower efficiency and increased output-voltage ripple amplitude. Decreasing the peak current incurs higher switching losses, which can lower the efficiency. See the *Typical Operating Characteristics* section.

To maximize the ease of implementation, the peak current settings of the buck regulator can be automatically adjusted to the optimal settings for a given output voltage. When Buck_ISetLookUpb = 0 (see the Buck1ISetLookUpb, Buck2ISetLookUpb, and Buck3ISetLookUpb bits), the MAX20356 updates the peak current settings when the output voltage of the buck regulator is changed in any DVS mode. If an application requires independent peak current control, the Buck_ISetLookUpb = 1 setting (see the Buck1ISetLookUpb, Buck2ISetLookUpb, and Buck3ISetLookUpb bits) disables the automatic update function.

Power Switch and Reset Control

The MAX20356 features a power switch that provides the ability to execute a reset sequence or to turn off the main system power and enter off or seal mode to extend battery life. In off mode, the SYS node and all PMIC outputs are turned off except LDO4 (RTC LDO) when it is configured as always on (MiscFunc[1]=0 by OTP), either by the LDO4Seq (see the LDO4Seq bit) or when it is kept on before entering off mode. The LDO1 can be always on if the LDO1Seq (see the LDO1Seq bit) is set to always on by OTP. In seal mode, all regulators and the SYS node are turned off. Seal mode is the lowest-quiescent current mode of the MAX20356 and maximizes battery life when a product cannot be used for an extended period, such as when shipping from the factory to a retailer. More details on the power modes can be found in the *PMIC Power Modes* section.

Shutdown and reset events are triggered by an external control using the power function (PFN) control inputs, I^2C commands, or if other conditions are met. The behavior of the PFN pins is preconfigured to support one of the multiple types of wearable application cases. *Table 5* describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg bits (see PwrRstCfg in *Table 5*), while *Figure 13* through *Figure 21* show the state diagrams associated with each mode.

A soft-reset sends a 10ms pulse on $\overline{RST}$ and either leaves register settings unchanged or resets them to their default values depending on the device version (see the SftRstCfg bit). A hard reset on any device initiates a complete power-on reset (POR) sequence.

Devices with HrvEn = 0 enter seal mode on cold boot (battery attach with no CHGIN present). Devices with HrvEn = 1 enter battery recovery (BR) mode on cold boot. When the MAX20356 is in on mode, it enters off/seal/BR mode after receiving the PWR_OFF_CMD/PWR_SEAL_CMD/PWR_BR_CMD I^2C command in the PwrCmd register (see the PwrCmd register), respectively. When the device detects a valid PFN signal it enters off mode or BR mode based on the PwrRstCfg and HrvEn setting.

The MAX20356 exits off/seal mode and turns the main power back on when there is a qualified PFN1 signal for PwrRstCfg settings where PFN1 is $\overline{KIN}$, or when a valid voltage is applied to CHGIN. In the powered-on state, the SYS node is enabled and other functions can be controlled through the I^2C registers. *Figure 22* and *Figure 23* illustrate a complete boot sequence coming out of off/seal mode.

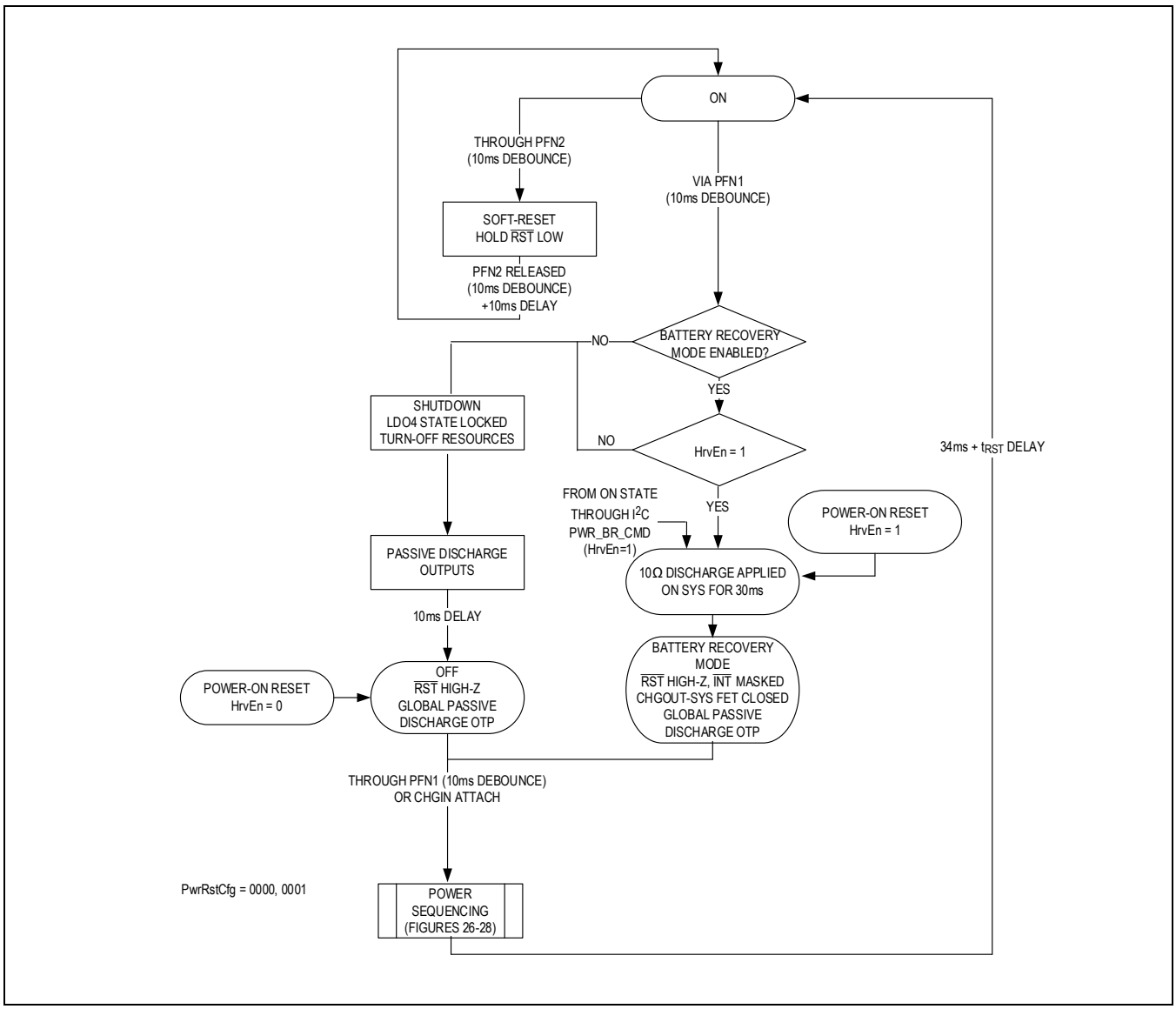


Figure 13. PwrRstCfg 0000, 0001

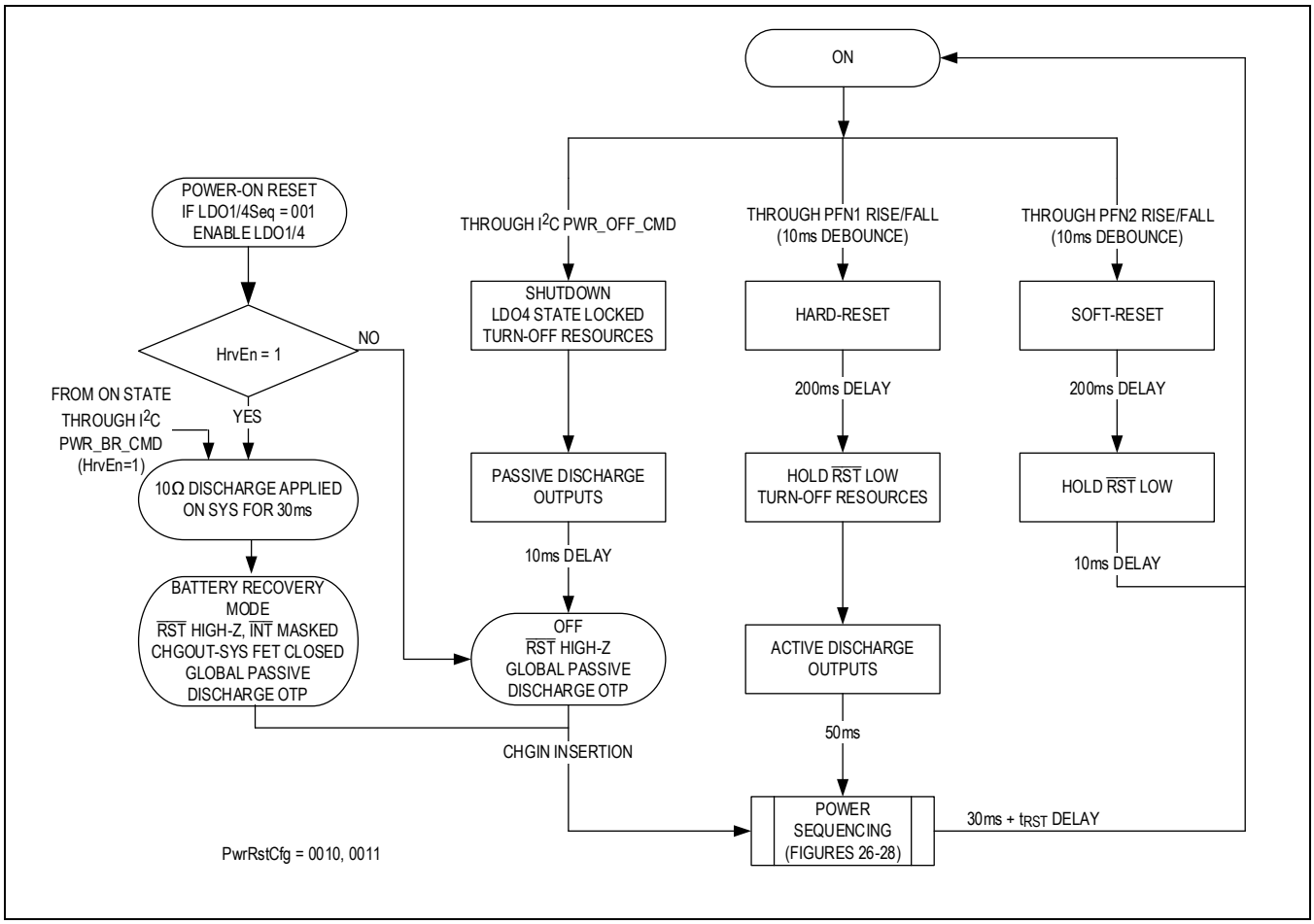


Figure 14. PwrRstCfg 0010, 0011

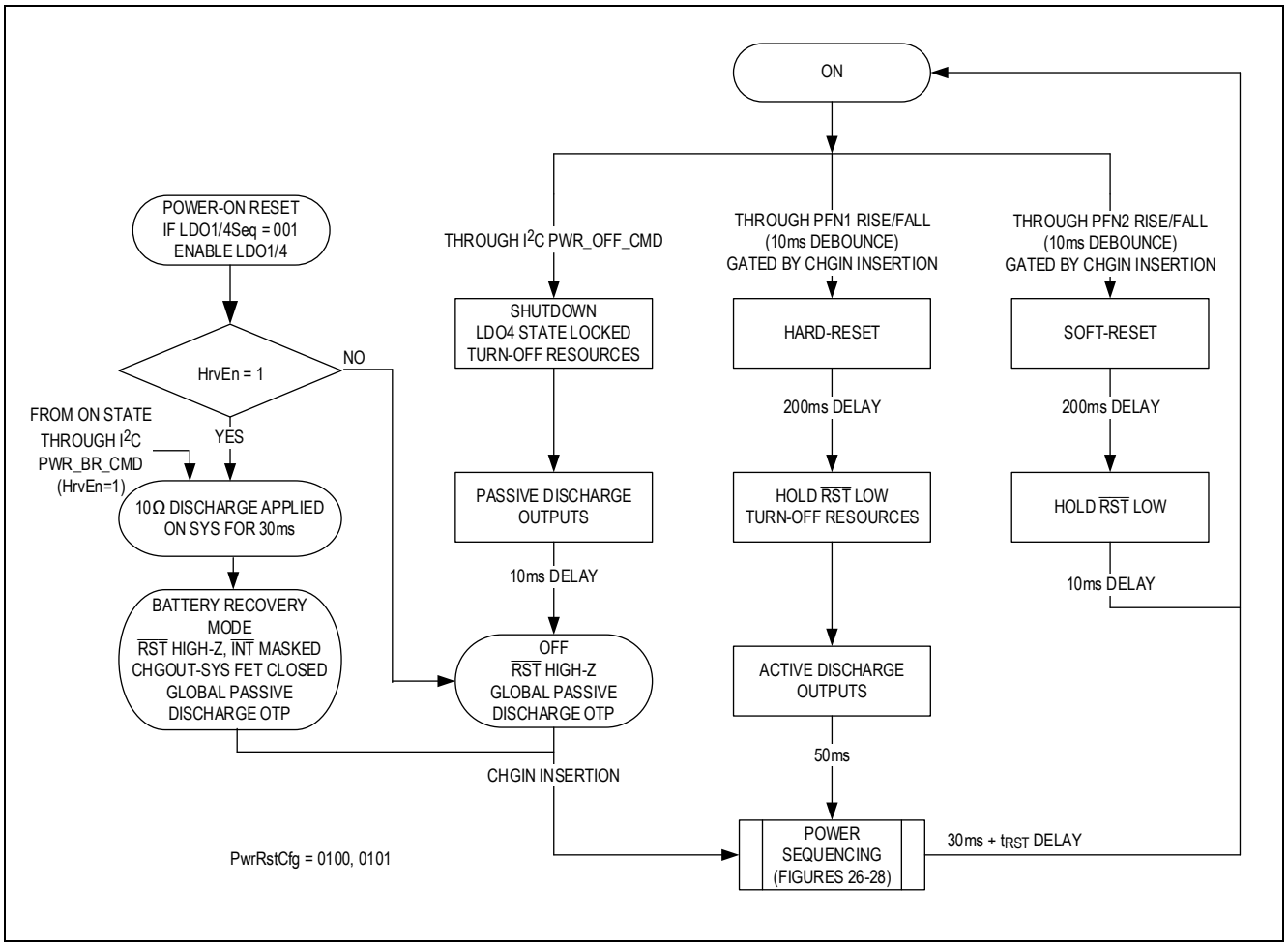


Figure 15. PwrRstCfg 0100, 0101

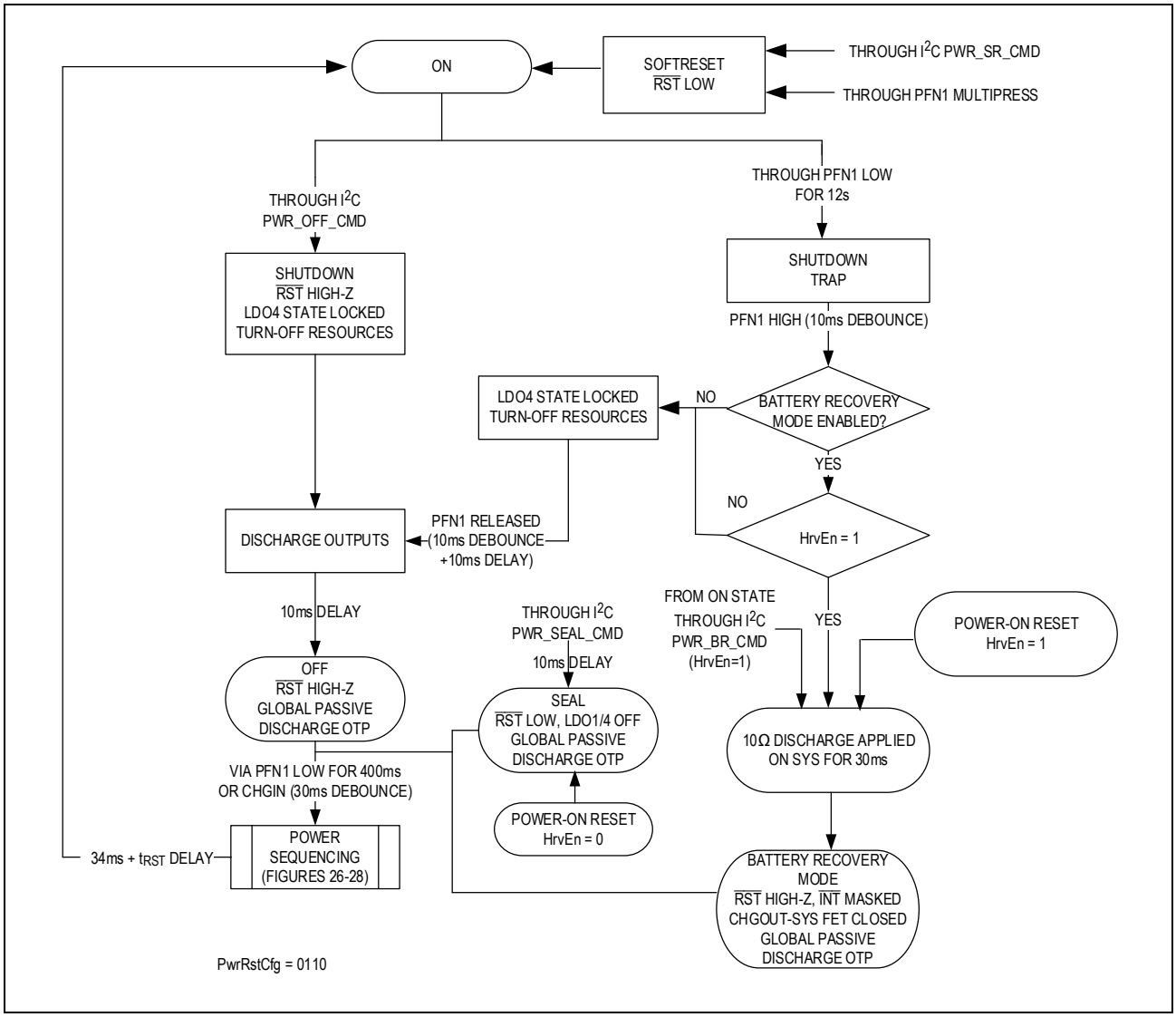


Figure 16. PwrRstCfg 0110

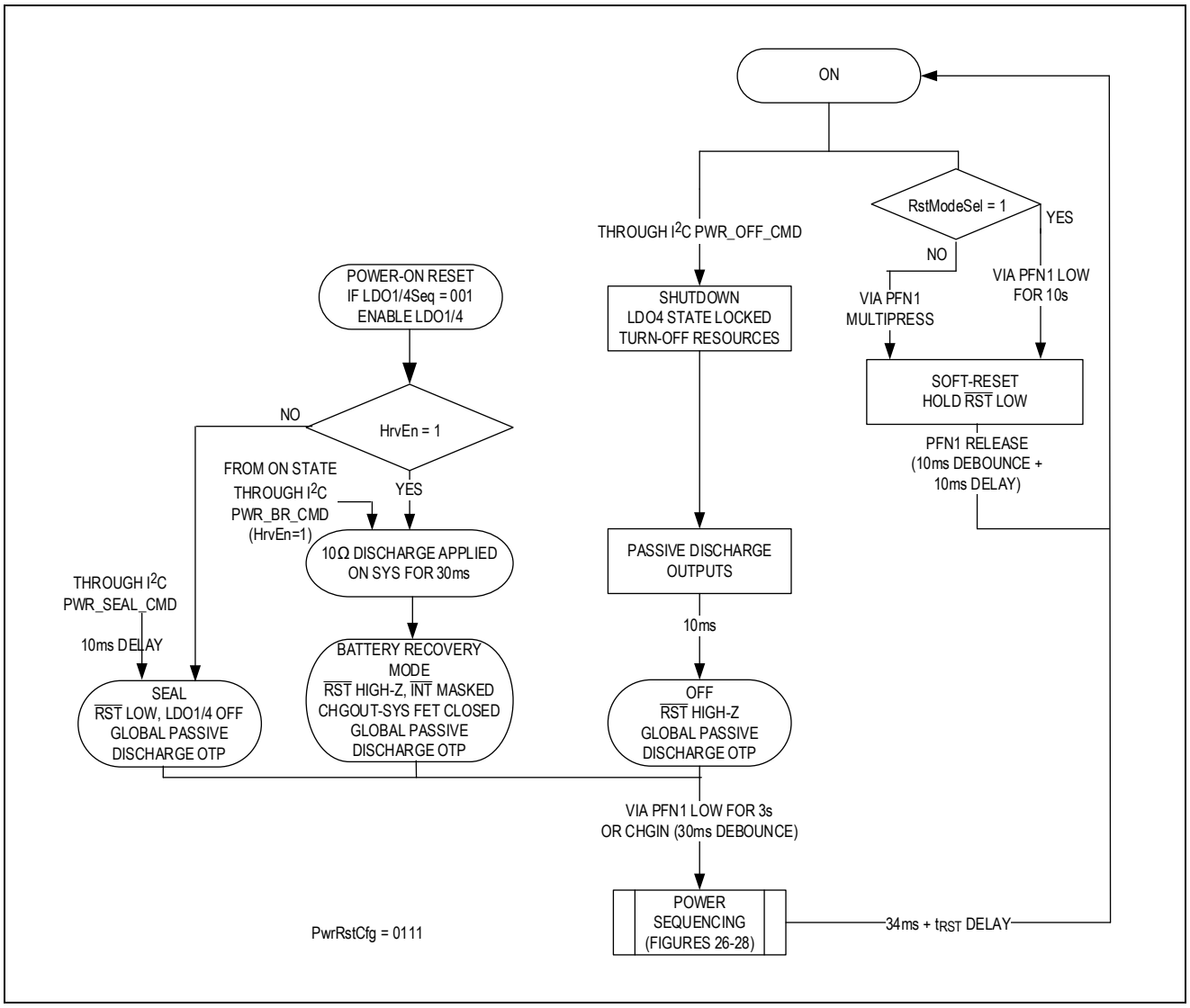


Figure 17. PwrRstCfg 0111

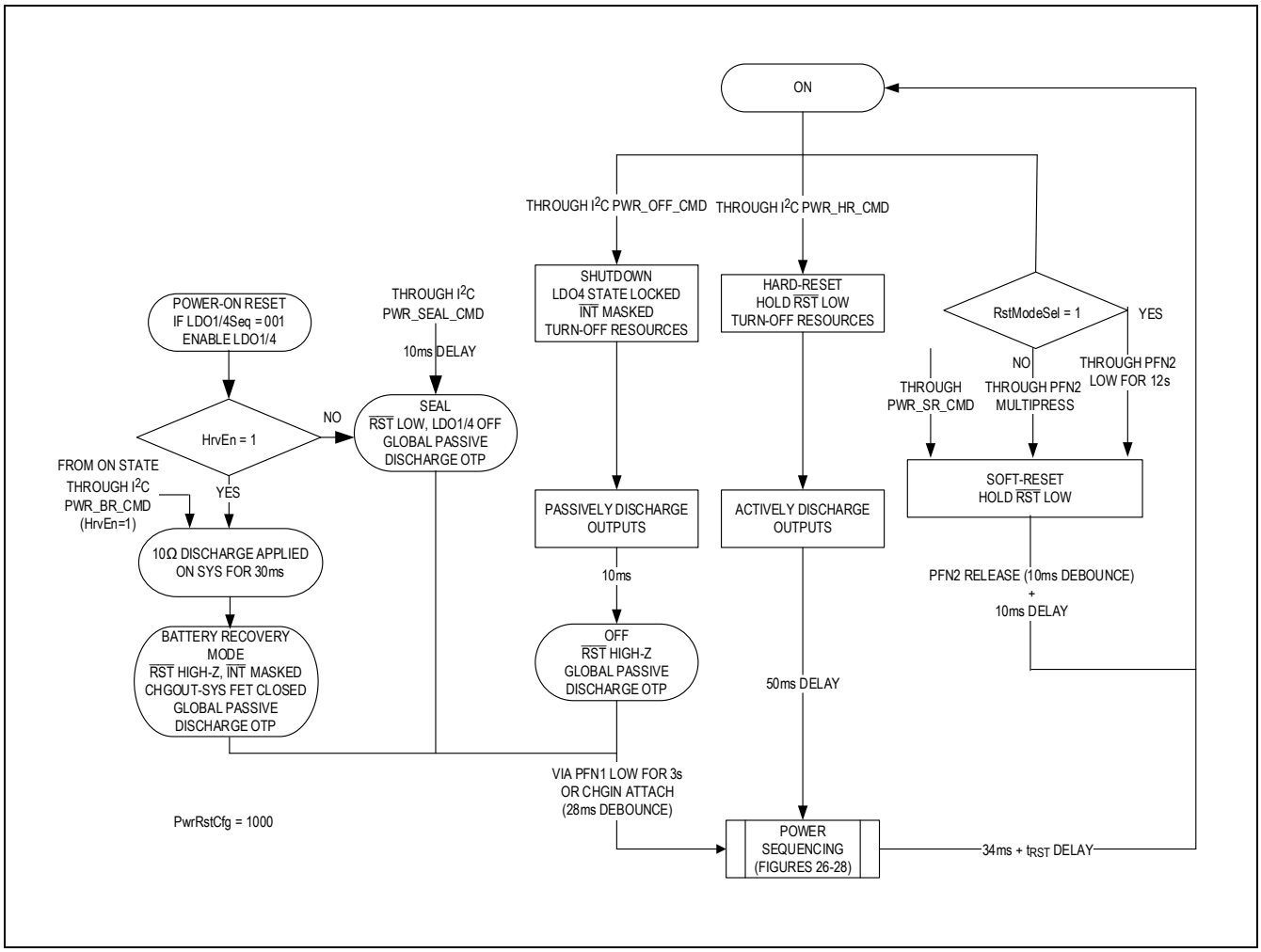


Figure 18. PwrRstCfg 1000

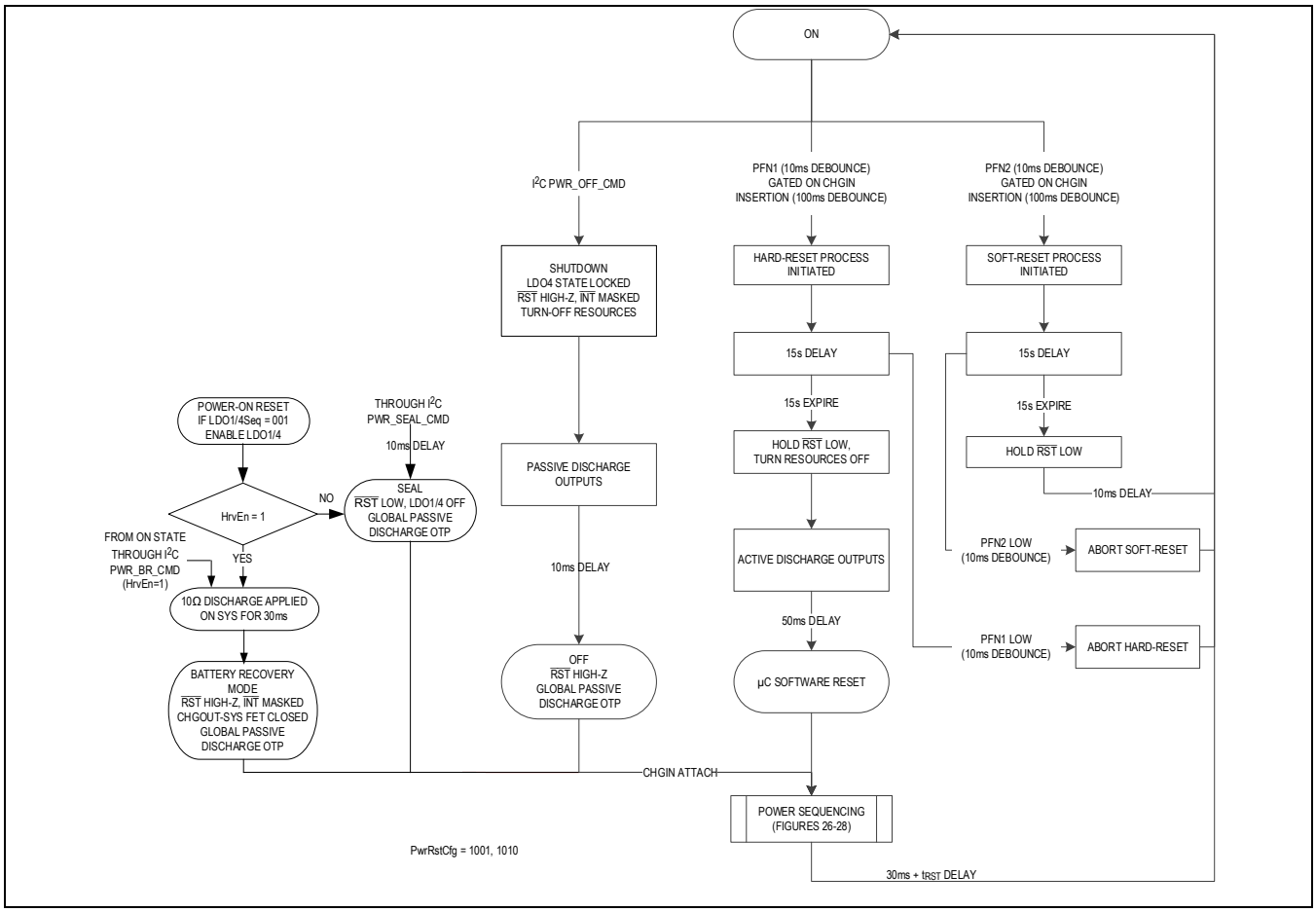


Figure 19. PwrRstCfg 1001, 1010

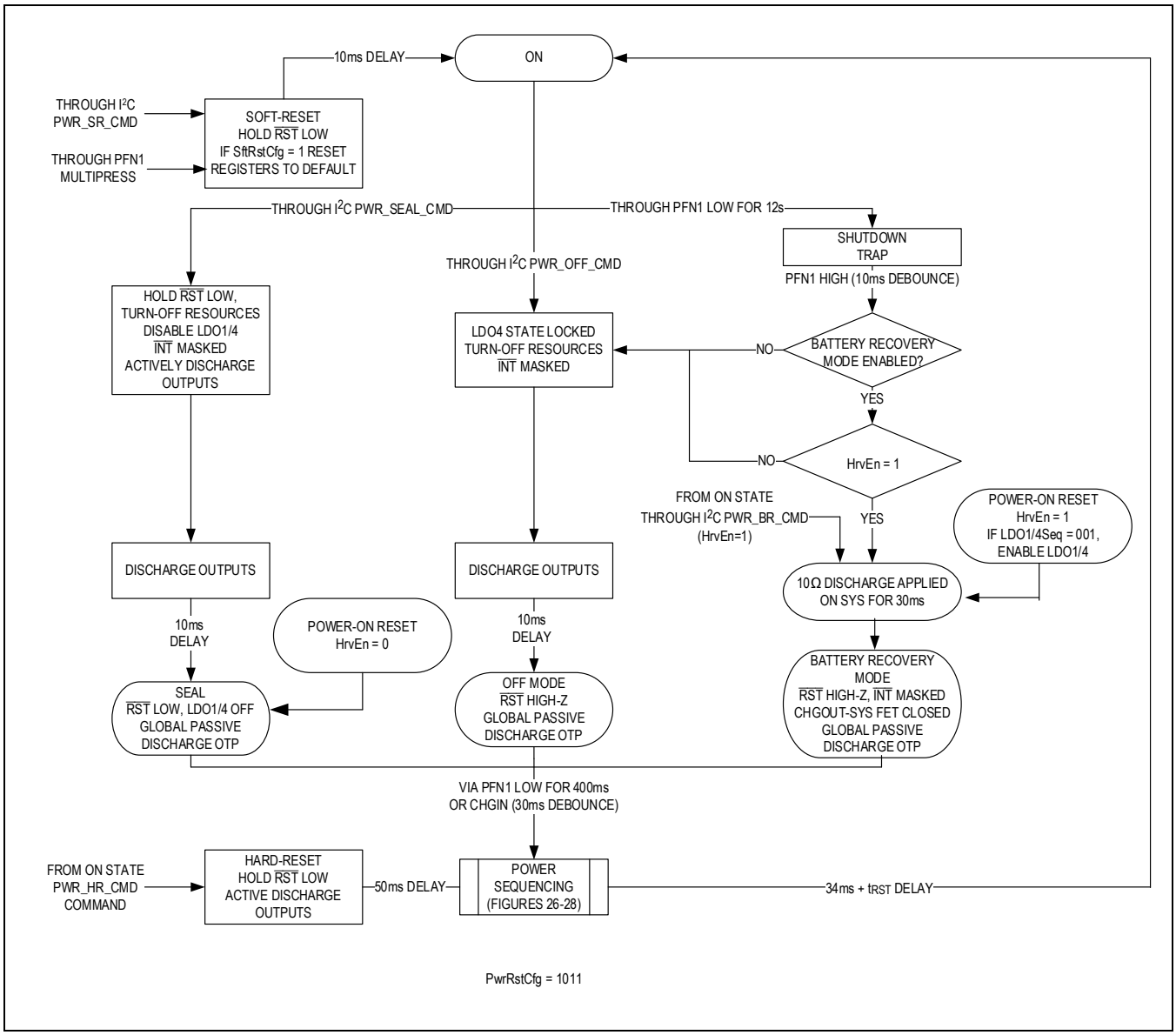


Figure 20. PwrRstCfg 1011

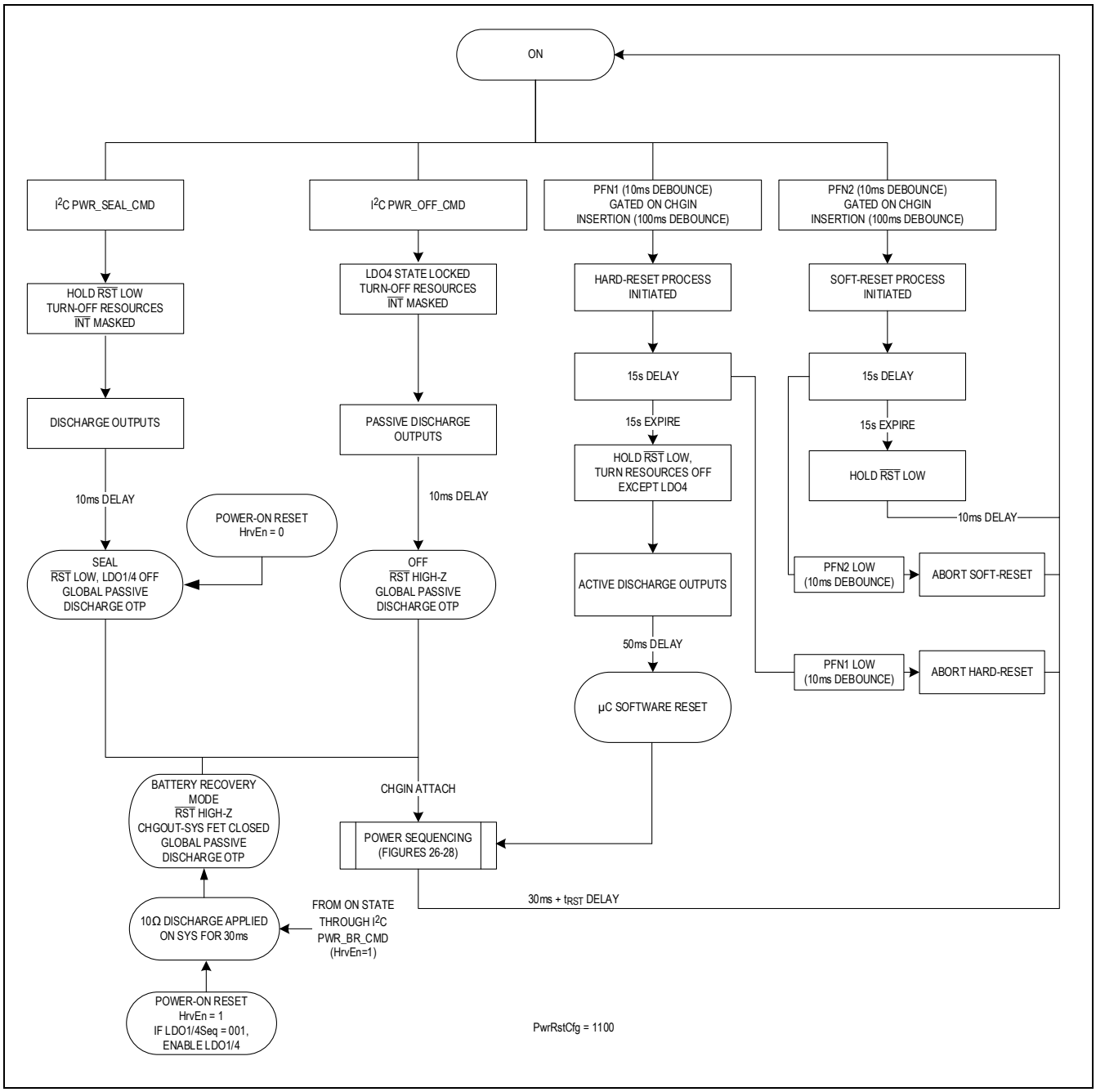


Figure 21. PwrRstCfg 1100

Table 5. PwrRstCfg Settings

PwrRstCfg[3:0]	FIGURE	MODE NAME	BEHAVIOR
0000	*Figure 13*	On/Off	On/off mode with 10ms debounce. PFN1 is the active-high on/off control input. PFN2 is the active-low soft-reset input.
0001	*Figure 13*	On/Off	On/off mode with 10ms debounce. PFN1 is the active-low on/off control input. PFN2 is the active-low soft-reset input.
0010	*Figure 14*	AON	Always-on mode. A rising edge on PFN1 generates a hard-reset after a 200ms delay. A rising edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0011	*Figure 14*	AON	Always-on mode. A falling edge on PFN1 generates a hard-reset after a 200ms delay. A falling edge on PFN2 generates a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0100	*Figure 15*	CR High	Always-on mode. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 high during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0101	*Figure 15*	CR Low	Always-on mode. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 200ms delay. Holding PFN2 low during a CHGIN insertion triggers a soft-reset after a 200ms delay. The device can only enter the off state by writing to the PwrCmd register.
0110	*Figure 16*	$\overline{KIN}$	On/off through key presses. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain $\overline{KOUT}$ output, which buffers the $\overline{KIN}$ input. The device enters on mode through a short (400ms) $\overline{KIN}$ press or a CHGIN insertion. The device enters off mode through a long (> 12s) $\overline{KIN}$ press or through the PwrCmd register.
0111	*Figure 17*	CSR1	On/reset through key presses. PFN1 is the active-low $\overline{KIN}$ button. PFN2 is the open-drain $\overline{KOUT}$ output, which buffers the $\overline{KIN}$ input. The device enters on mode through a long (> 3s) $\overline{KIN}$ press or a CHGIN insertion. A long (> 10s) $\overline{KIN}$ press generates a soft-reset. The device can only enter the off state by writing to the PwrCmd register.
1000	*Figure 18*	CSR2	On/reset through key presses. PFN1 is the active-low $\overline{KIN}$ button. The device enters on mode through a long (> 3s) $\overline{KIN}$ press or a CHGIN insertion. A long (> 12s) PFN2 press generates a soft-reset. The device can only enter the off-state by writing to the PwrCmd register.
1001	*Figure 19*	Custom CR High	Always-on mode. The device can only enter the on state through a CHGIN insertion. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought low during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 high during a CHGIN insertion generates a soft-reset after a 15 second delay. If PFN2 is brought low during this delay (10ms debounce), the hard-reset is aborted.
1010	*Figure 19*	Custom CR Low	Always-on mode. The device can only enter the on state through a CHGIN insertion. Holding PFN1 low during a CHGIN insertion generates a hard-reset after a 15 second delay. If PFN1 is brought high during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 low during a CHGIN insertion generates a soft-reset

			after a 15 second delay. If PFN2 is brought high during this delay (10ms debounce), the hard-reset is aborted.
1011	*Figure 20*	$\overline{\text{KIN}}$ with Off/Seal	On/off through key presses with off/seal. PFN1 is the active-low $\overline{\text{KIN}}$ button. PFN2 is the open-drain $\overline{\text{KOUT}}$ output, which buffers the $\overline{\text{KIN}}$ input. The device enters on mode through a short (400ms) $\overline{\text{KIN}}$ press or a CHGIN insertion. The device enters off mode through a long (> 12s) press or through the PwrCmd register.
1100	*Figure 21*	Custom CR High with Off/Seal	Always-on mode with off/seal. The device can only enter the on-state through a CHGIN insertion. Holding PFN1 high during a CHGIN insertion generates a hard-reset after a 15-second delay. If PFN1 is brought low during this delay (10ms debounce), the hard-reset is aborted. Holding PFN2 high during a CHGIN insertion generates a soft-reset after a 15-second delay. If PFN2 is brought low during this delay (10ms debounce), the hard-reset is aborted.
1101–1111	—	RFU	—

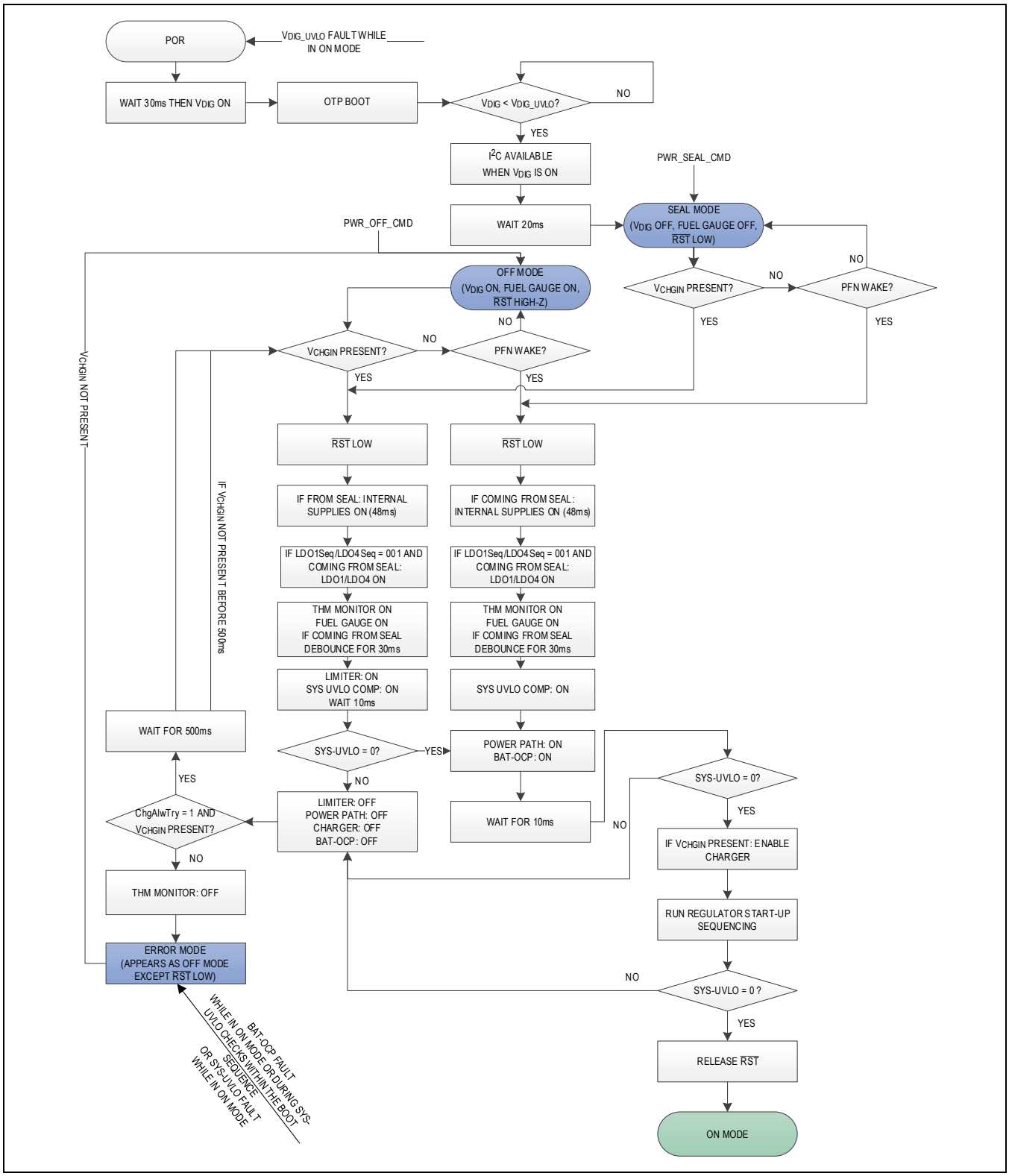


Figure 22. Boot Sequence—Harvester Mode Disabled

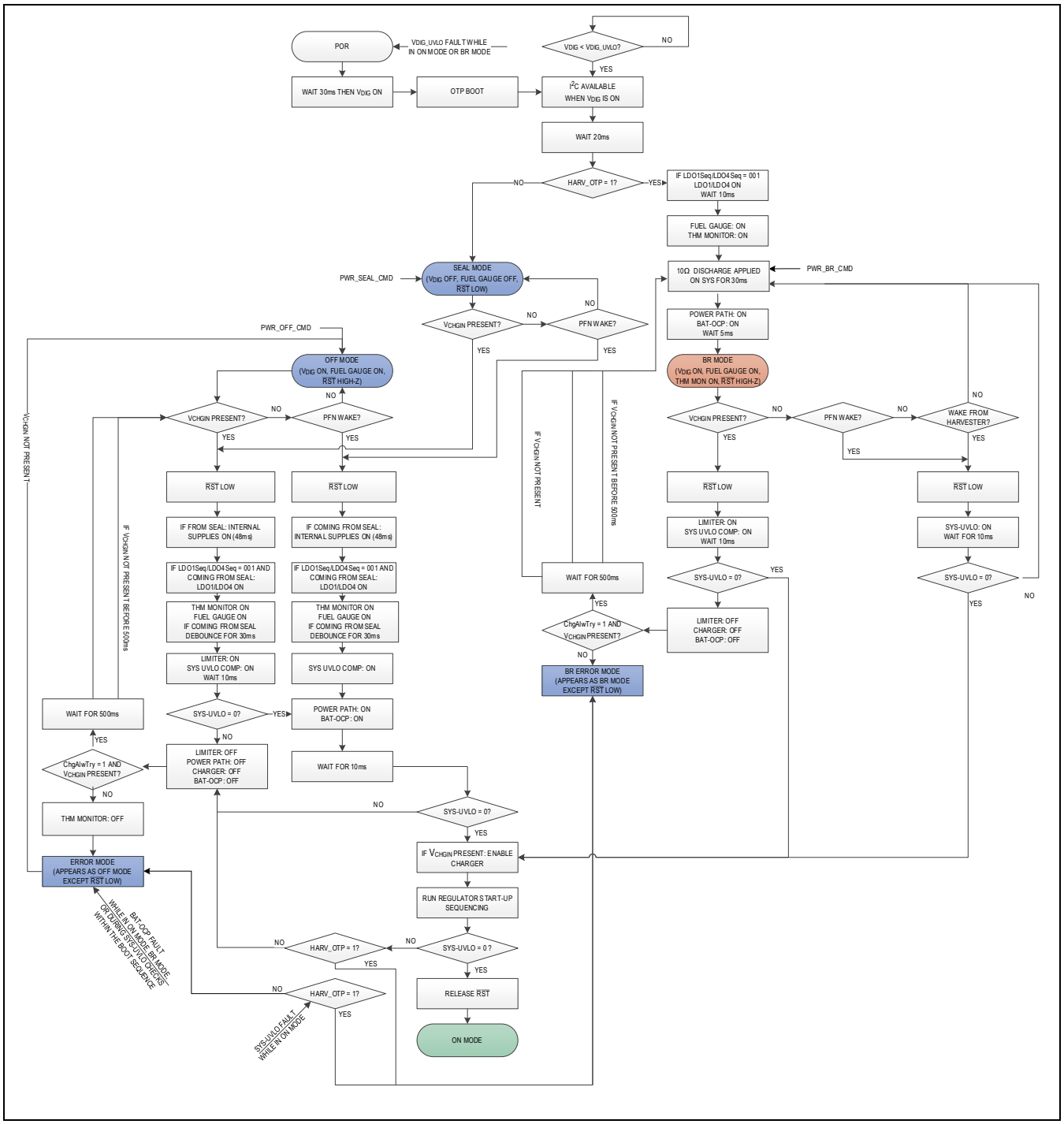


Figure 23. Boot Sequence—Harvester Mode Enabled

PMIC Power Modes

The following sections describe the basic operating modes of the MAX20356.

Seal Mode

Seal mode is the lowest-quiescent current mode on the MAX20356. In this mode, all resources are off except the button monitor and the V_{CHGIN} insertion detection circuitry.

Off Mode

The MAX20356 must, in some cases, power a real time clock (RTC). Off mode is the lowest quiescent current mode in which the fuel gauge and the RTC_LDO are powered. In this mode, the V_{DIG} supply, the button and V_{CHGIN} monitor circuits, and the fuel gauge are on. If RTC_LDO was on before entering off mode and MiscFunc[1] = 0 by OTP, RTC_LDO is also on in off mode.

On Mode (Versions with HrvEn = 0)

On mode is the most common operating mode. In on mode, all regulators are or can be enabled, the fuel gauge is on, and all features are accessible.

Battery Recovery (BR) Mode (Versions with HrvEn = 1)

On versions of the MAX20356 with HrvEn = 1, MPC7 and MPC6 are reconfigured as wake input (from the harvester) and disable output (to harvester, high-side open-drain to V_{CCINT}), respectively, according to the HrvFreeMPC setting of HrvBatCfg register (see the PMIC registers in the Register Map section) .

When the harvester mode is enabled (HrvEn = 1), and HrvFreeMPC =0, the MPC6 and MPC7 pins on the MAX20356 are captive to the harvester function. When the harvester mode is enabled (HrvEn = 1), and HrvFreeMPC = 1, the MPC6 and MPC7 pins are free to be used and are no longer captive to the harvester function.

If the device has SysPDEn enabled, SYS node is discharged through a 10Ω resistor for 30ms before entering battery recovery node. In battery recovery mode, the part is in the same operating condition as off mode. However, in addition the switch between SYS and BAT is closed to allow a charging path for recovery from a dead battery situation and the battery thermistor is actively monitored to ensure safe operating conditions. As soon as the battery reaches a threshold which is programmed on the MAX20361 harvester, the MAX20361 sends a wake signal, bringing the part into on mode (versions with HrvEn = 1) as described below. In situations where the THM monitor detects an out-of-bound condition and the charging is considered unsafe, a disable signal is sent to the harvester to halt charging. Refer to the *MAX20361 data sheet* for more information.

On Mode (Versions with HrvEn = 1)

On mode with HrvEn = 1 is very similar to on mode with HrvEn = 0 as described above with the exception that harvester functionality is enabled. In this mode, an ideal diode can be applied to the CHGOUT-SYS relationship. In the default operation, the harvester supplies SYS directly until it is unable to further support the output at which point the battery supplements the supply. This mode also includes the rest of the harvester interaction functionality described in the *MAX20361 Harvester Interaction* section. This behavior can be modified by the HrvBatSys, HrvThmEn, and HrvThmDis bit fields (see the HrvBatSys, HrvThmEn, and HrvThmDis bits).

Factory Mode

The MAX20356 features two integrated factory modes which can be enabled by an I^2C command or via push button sequence when valid CHGIN voltage is present. Factory mode can be set to on or off mode by the MiscFunc[2] bit. When MiscFunc[2] = 0, factory mode is active. MiscFunc[2] = 1 deactivates this feature. Once factory mode feature is on, factory mode 1 and factory mode 2 are selectable by FactModeSel[1:0] OTP. Once in the factory mode, do not use the I^2C burst write operation.

Factory Mode 1

To enable factory mode 1, set OTP bit FactModeSel[1:0] = 00. The charger input voltage (V_{CHGIN}) must be higher than the charger input detect threshold (V_{CHGIN_DET}) and lower than the CHGIN overvoltage threshold ($V_{CHGIN\_DET} < V_{CHGIN} < V_{CHGIN\_OV}$ or UsbOVP[0] = 0 and UsbOk[0] = 1). The following are true when factory mode 1 is enabled.

1. The power path (CHGOUT-SYS) is enabled as an ideal diode. Note that when the power path is active, the charger is disabled.

2. The CHGIN-SYS path is enabled and the input current limiter is on and set to the maximum current limit of 1500mA ($V_{CHGIN} \neq V_{SYS}$).
3. The fuel gauge remains in functional mode.
4. The watchdog timer is disabled.
5. The battery overcurrent protection events are reported to system status but not asserted.
6. The system fault is masked.
7. SYSUVLO is masked.

Factory Mode 2

Factory mode 2 is configured when OTP bit FactModeSel[1:0] = 11. The charger input (CHGIN) must be higher than the charger input detect threshold (V_{CHGIN_DET}) and lower than the CHGIN overvoltage threshold ($V_{CHGIN\_DET} < V_{CHGIN} < V_{CHGIN\_OV}$ or UsbOVP[0] = 0 and UsbOk[0] = 1). The following are true when factory mode 2 is enabled.

1. The power path (CHGOUT-SYS) is disabled.
2. The CHGIN-SYS path is enabled. The input current limiter and overvoltage protection are disabled ($V_{CHGIN} = V_{SYS}$).
3. $V_{CAP} = V_{CHGIN}$.
4. The charger and JEITA monitoring are disabled.
5. The fuel gauge is off.
6. The watchdog timer is disabled.
7. The battery overcurrent protection events are reported to system status but not asserted.
8. The system fault is masked.
9. SYSUVLO is masked.

Enter/Exit Factory Mode by the PFN_ Push button

Once the proper factory mode (factory mode 1 or 2) is selected by the OTP bits, the MAX20356 can also enter the factory mode by utilizing the PFN_ push button sequence. The factory mode with key press is added to the PwrRstCfg[3:0] and it can be enabled or disabled by the OTP bits. The push button sequence is valid in the following PwrRstCfg[3:0] settings:

PwrRstCfg[3:0] = 0100: through PFN1.

PwrRstCfg[3:0] = 0101: through PFN1.

PwrRstCfg[3:0] = 0110: through PFN1.

PwrRstCfg[3:0] = 0111: through PFN1.

PwrRstCfg[3:0] = 1000: through PFN2.

PwrRstCfg[3:0] = 1011: through PFN1.

The MAX20356 enters factory mode when the PFN_ push button is pressed five times. A debounce time of t_{HIGH} and t_{LOW} is 10ms typical. If the push button is pressed quickly and does not stay low for t_{LOW} > 10ms or the button is released faster than t_{HIGH} > 10ms, the device does not register a button press. Once the debounce time for each t_{LOW} and t_{HIGH} is met, pressing the PFN_ button five times enters the part in factory mode after 8 seconds.

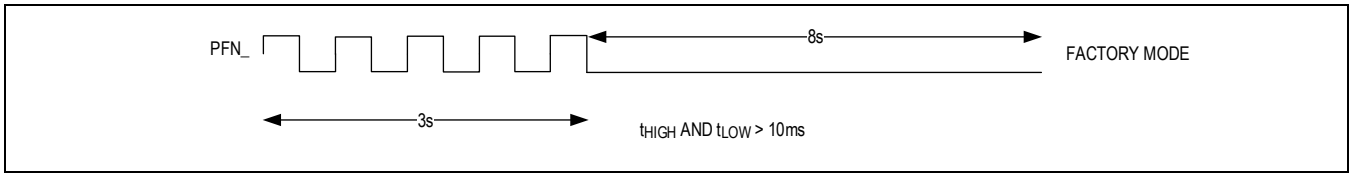


*Figure 24. Entering Factory Mode by PFN_*

The MAX20356 exits factory mode with the I²C command, PFN_ push button, or removal of the CHGIN signal. Exiting from the factory mode reboots the device including all switching regulators and always-on and RTC regulators.

Enter/Exit Factory Mode Through I²C

Factory mode 1 and 2 are available for all PwrRstCfg configurations. To enter or exit factory mode through the I²C, set PwrCmd[0:7] = 0x52. (See the Register Map section.)

New Reset/Key Press/Multipress Feature

For specific power reset sequences, an alternative button sequence is available for soft reset. This push button sequence is intended to provide more robust protection against accidental resets. For PwrRstCfg[3:0] 0110 and 1011, this feature is enabled.

For PwrRstCfg[3:0] 0111 and 1000, this feature can be enabled or disabled by the RstModeSel OTP bit. If RstModeSel = 0, the reset feature is enabled and when RstModeSel = 1, the reset function is disabled.

The multipress reset is valid in the following PwrRstCfg[3:0] settings:

PwrRstCfg[3:0] = 0110: through PFN1.

PwrRstCfg[3:0] = 0111: through PFN1.

PwrRstCfg[3:0] = 1000: through PFN2.

PwrRstCfg[3:0] = 1011: through PFN1.

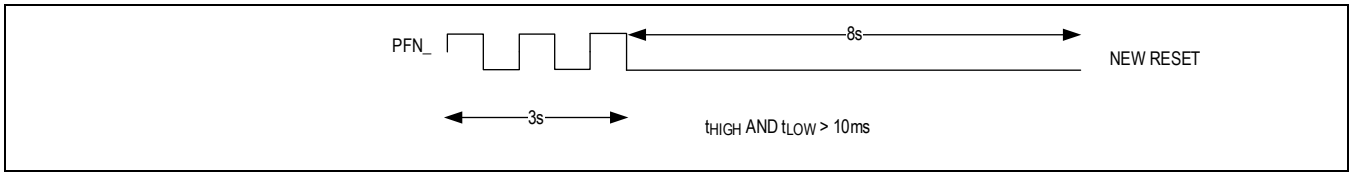


*Figure 25. Reset via PFN_*

The MAX20356 enters the multipress reset when the PFN_ push button is pressed three times. A debounce time of t_{HIGH} and t_{LOW} is 10ms typical. If the push button is pressed quickly and does not stay low for t_{LOW} > 10ms or the button is released faster than t_{HIGH} > 10ms, the device does not register a button press. Once the debounce time for each t_{LOW} and t_{HIGH} is met, pressing the PFN_ button three times performs a soft reset.

Interrupt

The $\overline{INT}$ output of the MAX20356 is driven low when any one of the unmasked interrupts is triggered by the corresponding status change. The $\overline{INT}$ output is held low until the unmasked and triggered interrupt register bits are read by the user. The interrupt bits are cleared on read. The interrupt registers consist of Int0 to Int5 while the interrupt mask registers consist of IntMask0 to IntMask5.

Power Sequencing

The sequencing of the switching regulators, load switches, and LDOs during power-on is configurable. See the sequencing bits of each function for details. Regulators and switches can turn on at one of three points during the power-on process: 0% of $t_{\overline{RST}}$ time after the power-on event, at the time the $\overline{RST}$ signal is released, or at two points in between. The two points between 0% of $t_{\overline{RST}}$ time delay and the $\overline{RST}$ rising edge are fixed proportionally to the duration of the power-on reset (POR) process boot delay ($t_{\overline{RST}}$). The value of the $t_{\overline{RST}}$ delay ranges from 80ms to 420ms and is stored in the BootDly bits (see the BootDly bits). The timing relationship is presented graphically in in *Figure 26*, *Figure 27*, and *Figure 28*.

Alternatively, the regulators and switches can remain off by default and turn on manually with an I^2C command after $\overline{RST}$ is released. LDO1 and RTC_LDO can be configured to be always on.

The SYS voltage is monitored during the power-on sequence. If V_{SYS} falls below V_{SYS_UVLO} during the sequencing process with a valid voltage at CHGIN and ChgAlwTry = 1, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the off state to avoid draining the battery. Power is also turned off if BAT experiences a current greater than I_{BAT_OCP} for more than $t_{BAT\_OCP\_RD}$.

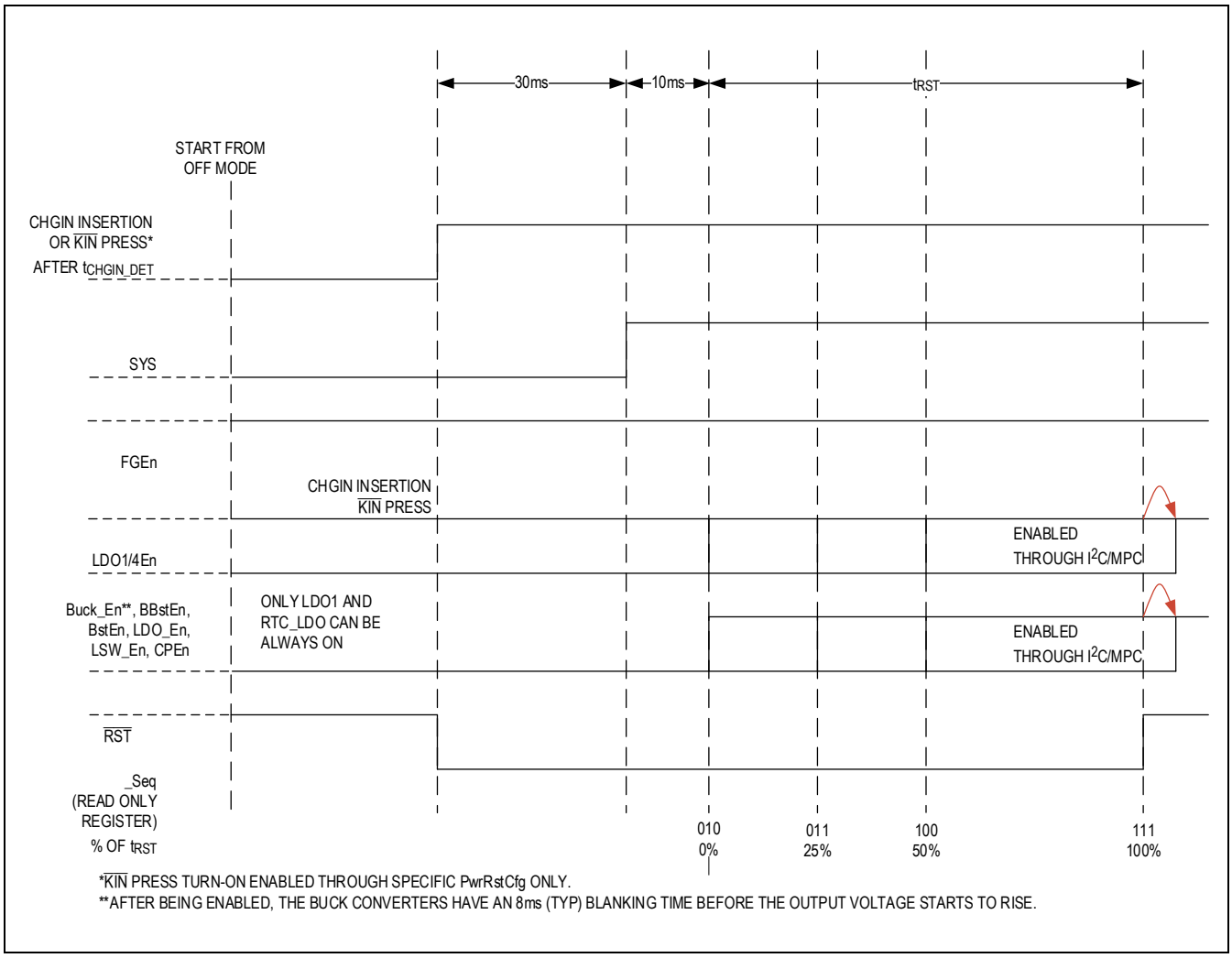


Figure 26. Power Sequencing—HrvEn = 0 from Off Mode

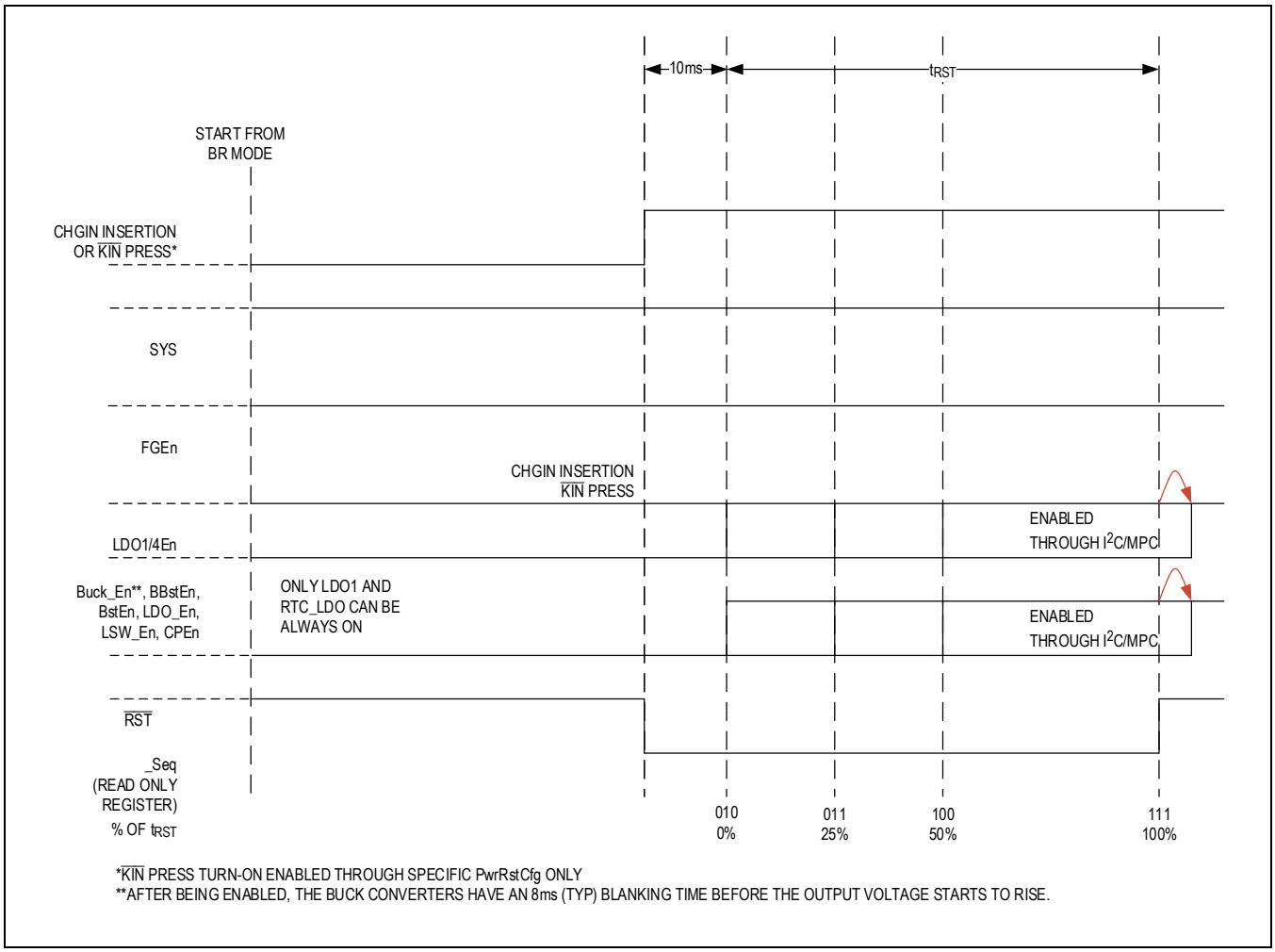


Figure 27. Power Sequencing—HrvEn = 1 from BR Mode

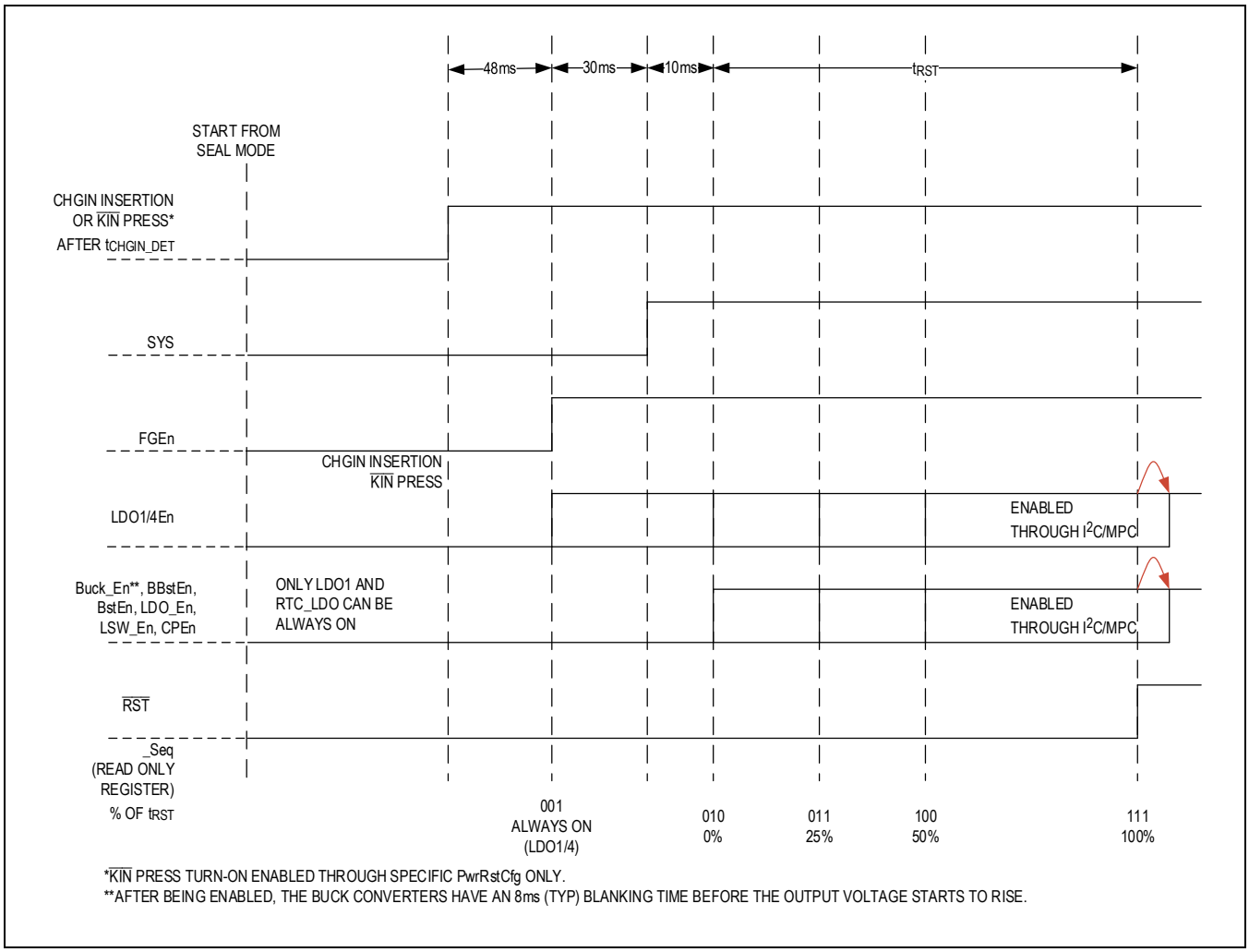


Figure 28. Power Sequencing from Seal Mode

System Load Switch

An internal 50mΩ (typ) MOSFET connects CHGOUT to SYS when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-CHGOUT switch also prevents V_{SYS} from falling below V_{CHGOUT} when the system load exceeds the input current limit. If V_{SYS} drops to V_{CHGOUT} due to the current limit (I_{LIM}), the SYS-to-CHGOUT switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit, the battery is not charged. This is useful for handling loads that are nominally below the input current limit, but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges.

Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the CHGOUT and SYS nodes. With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input-current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input-current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no input-current limit, the system is powered from the battery.

Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power.

Invalid CHGIN Voltage Protection

If CHGIN is above the overvoltage threshold V_{CHGIN_OV}, the device enters overvoltage lockout (OVLO). OVLO protects the MAX20356 and downstream circuitry from high-voltage stress up to +28V. During OVLO, the internal circuit remains powered and an interrupt is sent to the host. The negative voltage protection down to -5.5V disconnects CHGIN and the device is powered only by BAT. The charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V_{BAT}, or less than the V_{CHGIN_DET} threshold. With an invalid input voltage, the SYS-to-BAT load switch closes and allows the battery to power SYS.

CHGIN Input Current Limit

The CHGIN input current is limited to prevent input overload. The input current limit I_{LIM} is I^2C-controlled through the ILimCntl parameter (see the ILimCntl bit). To accommodate systems with a high inrush current, the limiter includes a blanking time t_{ILIM_BLANK} (I^2C-programmable through the ILimBlank parameter (see the ILimBlank bit)), during which the input current limit increases to I_{LIM_MAX}. If I_{LIM_MAX} is set lower than ILimCntl, the more stringent value of I_{LIM_MAX} is forced also for ILimCntl.

Thermal Limiting

In case the die temperature exceeds T_{CHG_LIM}, the MAX20356 attempts to limit temperature increases by reducing the input current from CHGIN. In particular, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T_{CHG_SHDN}), no input current is drawn from CHGIN and the battery powers the entire system load.

Battery Charger

Battery Charger State Diagram

The battery charger-state diagram is shown in *Figure 29.* The user can read the ChgStat bits (see the ChgStat bits) to know the status of the charger. The MAX20356 battery charger is a fully featured lithium-ion charger offering I^2C programmable voltage thresholds through charging phases: pre-charge voltage VPChg, step charging voltage ChgStepRise, charge termination voltage ChgBatReg, and top off current IChgDone. The MAX20356 also features safety timers, JEITA charging profile with thermistor and overtemperature protection with die temperature sensor. It starts charging from the precharge stage if the battery voltage is lower than the precharge voltage VPChg. The step charging feature allows higher charge rate at the beginning of the charge cycle during CC1. Once the battery voltage rises to step charge threshold ChgStepRise, the charger transitions to CC2 at a lower charge rate. If the battery voltage is charged up close to ChgBatReg, in CV mode, the BAT pin voltage is regulated at ChgBatReg and charging current naturally reduces as the battery charges up. The charging current options for precharge, CC1 and CC2 can be found in IPChg, CC1IFChg, and CC2IFChg. The voltage threshold from precharge to CC1, from CC1 to CC2, and charge termination voltage can be found in VPChg, ChgStepRise, and ChgBatReg. The top-off current threshold can be found in IChgDone. *Figure 29* shows the battery charger-state diagram.

There are also independently programmable temperature thresholds, which allow the user to select in which temperature ranges precharge, CC1, CC2, and battery regulation voltage may operate. Different JEITA-compliant temperature operation strategies are I^2C programmable. The timeout function for precharge, CC1, and full charge cycle is also designed to prevent overcharge of the battery. Detailed charger operation is shown in *Figure 29*.

Some charger bits are reset to default value upon CHGIN rising/falling edge based on UsbOkselect option (see *Table 6* for UsbOkselect value). The bits that are reset on the CHGIN edge are denoted by an asterisk * in the register map.

Charger-Off State

As shown in *Figure 29*, when CHGIN is not present or is below the CHGIN_DET threshold, the MAX20356 charger is in charger off state (ChgStat = 0b0000). After CHGIN is connected, the charger transitions from charger off state to charger idle state (ChgStat = 0b0001).

Charger Idle State

As shown in *Figure 29*, the following events cause the charger to enter charger idle state.

- A CHGIN connection event. The charger transitions from charger off state to charger idle state when the MAX20356 detects a CHGIN connection event and ChgEn is 1.
- CHGIN > CHGIN_DET and ChgEn goes from low to high.

Charger Boot State

The charger exits charger idle state and starts boot sequence when one the following conditions are met:

- ChgFresh = 1.
- ChgFresh = 0, $V_{BAT} < V_{BAT\_RECHG}$ (recharge threshold).

When the charger enters charger boot state, all charger timers reset.

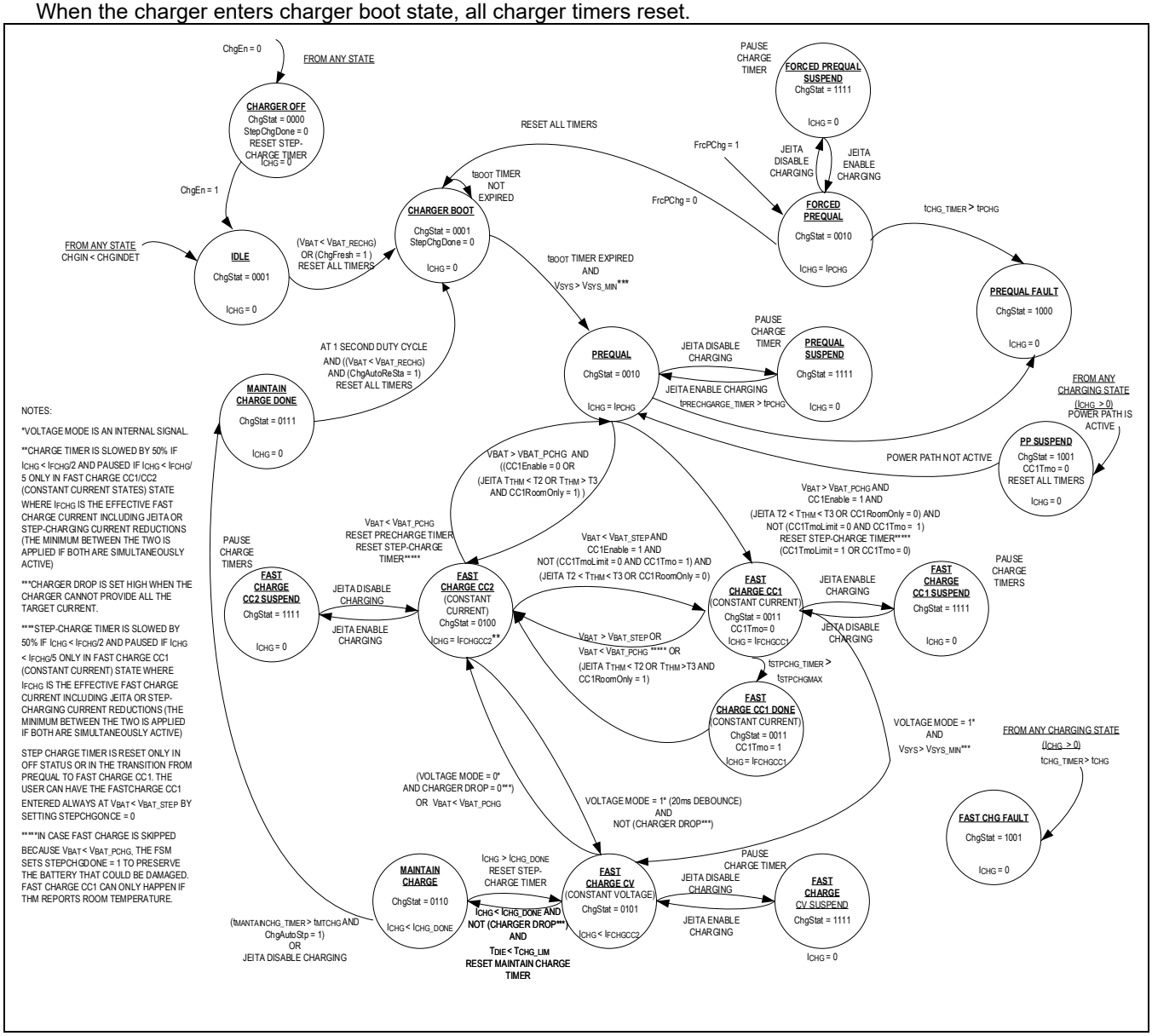


Figure 29. Battery Charger-State Diagram

Prequal State

As shown in *Figure 29,* the charger enters the precharge state (ChgStat = 0b0010) after the charger boot sequence is completed and the SYS pin voltage is regulated higher than or equal to the minimum system voltage SysMinVlt. If the battery voltage is lower than VPChg, or if FrcPChg = 1, the charger remains in the prequal state. In the prequal state, the battery charging current is IPChg.

The following events cause the charger to exit prequal state:

- The battery voltage rises above VPChg. If step charging is enabled (CC1Enable = 1), CC1 is not configured to run at room temperature only (CC1RoomOnly = 0) or CC1 is configured to run at room temperature only (CC1RoomOnly = 1) and the thermistor monitoring reports room temperature and the charger enters fast-charge constant current mode 1 (CC1) state. By default, step charging is enabled (CC1Enable = 1) and CC1 is configured to run at any temperature (CC1RoomOnly = 0).
- The battery voltage rises above VPChg. If step charging is disabled (CC1Enable = 0) or if CC1Enable = 1 and CC1 is configured to run at room temperature only (CC1RoomOnly = 1) but the battery is in the cool or warm temperature zone, the charger enters fast-charge constant current mode 2 (CC2) state.
- Prequal (precharge) timeout. If the charger remains in this state for longer than the charger precharge timer (PChgTmr), the charger enters charger fault-precharge timer PChgTmr expired state (ChgStat = 0b1000) and suspends charging.
- Charger safety timeout. If the charger safety timer (ChgTmr[1:0]) expires while in precharge state, the charger enters charger fault-safety timer ChgTmr[1:0] expired state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The charger suspends charging due to temperature. See the *JEITA Monitoring with Charger Control* section for a detailed description.
- Forced precharge. The charger can be forced to operate with precharge current IPChg in the force precharge state by setting FrcPChg = 1. The charger transitions to the charger boot sequence when disable forced precharge FrcPChg = 0.

Fast-Charge Current Setting

The fast-charge current IFCHG is set by the I^2C interface through bits CC1IFChg (Register 0x17) and CC2IFChg (Register 0x18). The precharge (I_{PCHG}) and charge-done ($I_{CHGDONE}$) currents are I^2C programmed using bits IPChg and IChgDone (Register 0x1B), respectively, as a percentage of CC2IFChg.

Fast-Charge Constant Current CC1 State

Once the battery voltage rises above the precharge threshold VPChg, the charger allows a higher charge rate CC1IFChg at the beginning of the charge cycle during fast-charge constant current mode 1 (CC1) state. Set register bit CC1Enable = 0 to disable the step-charging feature, and the charger transits from the precharge state directly to the CC2 state. In the JEITA-compliant thermistor temperature monitoring control, CC1 can be configured to run at room temperature only by setting CC1RoomOnly = 1. In the CC1 state, the charge current is regulated less than or equal to CC1FChg.

The following events cause the charger state machine to exit CC1 state:

- The battery voltage rises to ChgStepRise. The charger enters CC2 state.
- The battery voltage drops below VPChg. The charger goes through fast-charge CC1 done and CC2 state and eventually goes back to precharge state. During this process, the charge marks internal signal StepChgDone = 1. If the battery voltage rises above VPChg again, it skips CC1 state to protect the battery.
- CC1 timeout. If the step-charge timer is enabled (CC1TmoLimit = 1) and the charger remains in this state for longer than specified by CC1FChgTmr, it enters CC2 state.
- Charger safety timeout. If the charger safety timer (ChgTmr[1:0]) expires while in CC1 state, the charger enters charger fault-safety timer ChgTmr[1:0] expired state (ChgStat = 0b1001) and suspends charging.
- The temperature measured from THM is out of room temperature zone and CC1 is allowed to operate in room temperature only. If CC1RoomOnly = 1 and the battery temperature transitions from room to cool or warm, the charger enters CC2 state.
- JEITA disable charging. The charger suspends charging due to temperature. See the *JEITA Monitoring with Charger Control* section for a detailed description.

The battery charger dissipates the most power in the fast-charge constant current mode, which causes the die temperature to rise. If the die temperature reaches 3°C below ChgThrmLim, the charge current is linearly reduced to limit further temperature increase.

Fast-Charge Constant Current CC2 State

The step-charge feature is enabled by default on the MAX20356. Once the battery voltage rises above the step-charge threshold ChgStepRise, the charger enters fast-charge constant current mode 2 (CC2) state with a lower charge rate CC2IFChg to avoid lithium plating and prolong the lifetime of the battery. The ChgStepHys field sets the hysteresis for the step-charge function to avoid hopping between the CC1 state and CC2 state caused by high voltage drop from current reduction. In the CC2 state, the charge current is regulated less than or equal to CC2IFChg.

The following events cause the charger state machine to exit CC2 state:

- The battery voltage rises to ChgBatReg. The charger enters fast-charge constant voltage (CV) state.
- The battery voltage drops below ChgStepRise - ChgStepHys. The charger goes back to the CC1 state.
- The battery voltage drops below VPChg. The charger goes back to prequal state.
- Charger safety timeout. If the charger safety timer ChgTmr[1:0] expires while in the CC2 state, the charger enters charger fault-safety timer ChgTmr[1:0] expired state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The charger suspends charging due to temperature. See the *JEITA Monitoring with Charger Control* section for a detailed description.

Step Charging

Lithium-ion batteries suffer capacity degradation over their lifetimes. One of the primary causes of degradation over the lifetime of a battery is due to an effect called lithium plating, which is the formation of metallic lithium on the anode of the battery. Lithium plating has many causes, but one of the most common is when the battery is charged at high rates relative to the capacity of the battery when the battery is at a high state of charge (SOC). To combat this effect, the MAX20356 includes a step-charge function. This function allows the user to select a voltage threshold at which the charge current can be reduced to avoid lithium plating and prolong the lifetime of the battery. The settings of this function can be found in the ChgCfg0 and ChgCur0 registers. The ChgStepRise field allows the setting of the rising voltage V_{BAT_STPCHG} at which the charge current should be reduced. The CC1IFChg field sets the percentage I_{FCHG_CC1} of the full fast-charge current to which the charger should be set when the battery is above the V_{BAT_STPCHG} value specified with ChgStepRise. Lastly, the ChgStepHys field sets the $V_{BAT\_STPCHG\_H}$ hysteresis for the step-charge function to avoid oscillations in case a high battery impedance causes the voltage to fall a large amount upon reduction of the battery current.

A safety timeout controlled by CC1FChgTmr is available to ensure the step charge function is allowed only for a limited amount of time. If the safety timeout of the step-charger function is not desirable, set the CC1TmoLim setting to 0 to disable it. For more details on ChgCfg0, ChgCur0, ChgStepRise, CC1IFChg, ChgStepHys, and CC1FChgTmr, see the PMIC registers in the Register Map section.

If the overall step-charger function is not desirable, set the CC1Enable setting to 0 to disable it.

In case both JEITA and step-charging related fast-charge current reductions are active, the minimum between the two is selected and applied.

Adaptive Battery Charging

While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V_{SYS} from collapsing below the maximum between the V_{SYS_LIM} value (I^2C-programmable through the SysMinVlt parameter (see the SysMinVlt bit)) and $V_{SYS\_BAT\_REG}$ value. When the charge current is reduced below 50% (I_{FCHG_TEXT} threshold) due to V_{SYS_LIM}/$V_{SYS\_BAT\_REG}$ or T_{CHG_LIM} limits, the timer clock operates at half speed. When the charge current is reduced below 20% (I_{FCHG_TSUS} threshold) due to V_{SYS_LIM}/$V_{SYS\_BAT\_REG}$ or T_{CHG_LIM} limits, the timer clock pauses.

JEITA Monitoring with Charger Control

To enhance safety when charging lithium-ion batteries, the MAX20356 includes a JEITA-compliant temperature monitoring. A resistive divider is formed on THM connecting the thermistor of a battery pack. THM is internally connected to V_{DIG} through an I^2C-selectable 10kΩ/100kΩ pull-up resistor. The divider output on THM is read by internal comparators when JEITA monitoring is enabled and the resulting temperature measurement places the battery into one of five temperature zones: cold, cool, room, warm, and hot. Charging is always inhibited in cold and hot regions or if the thermistor is not detected while charging behavior is configurable in warm, room, and cool regions using the I^2C-controlled

ThmEn parameter (see the ThmEn bit) as shown in *Figure 30–Figure 33*. In particular, the battery regulation voltage can be reduced to the $V_{BAT\_REG\_JTA}$ value using the I²C-programmed ChgCool/Room/WarmBatReg[1:0] parameters (see the ChgCoolCC_IFChg, ChgRoomCC_IFChg, and ChgWarmCC_IFChg bits) while the fast-charge current can be reduced to the I_{FCHG_JTA} value using the I²C-programmed ChgCool/Room/WarmCC_IFChg parameters (see the ChgCoolCC_IFChg, ChgRoomCC_IFChg, and ChgWarmCC_IFChg bits). Charging can also be inhibited in cool and warm regions using ThmEn (see the ThmEn bit).

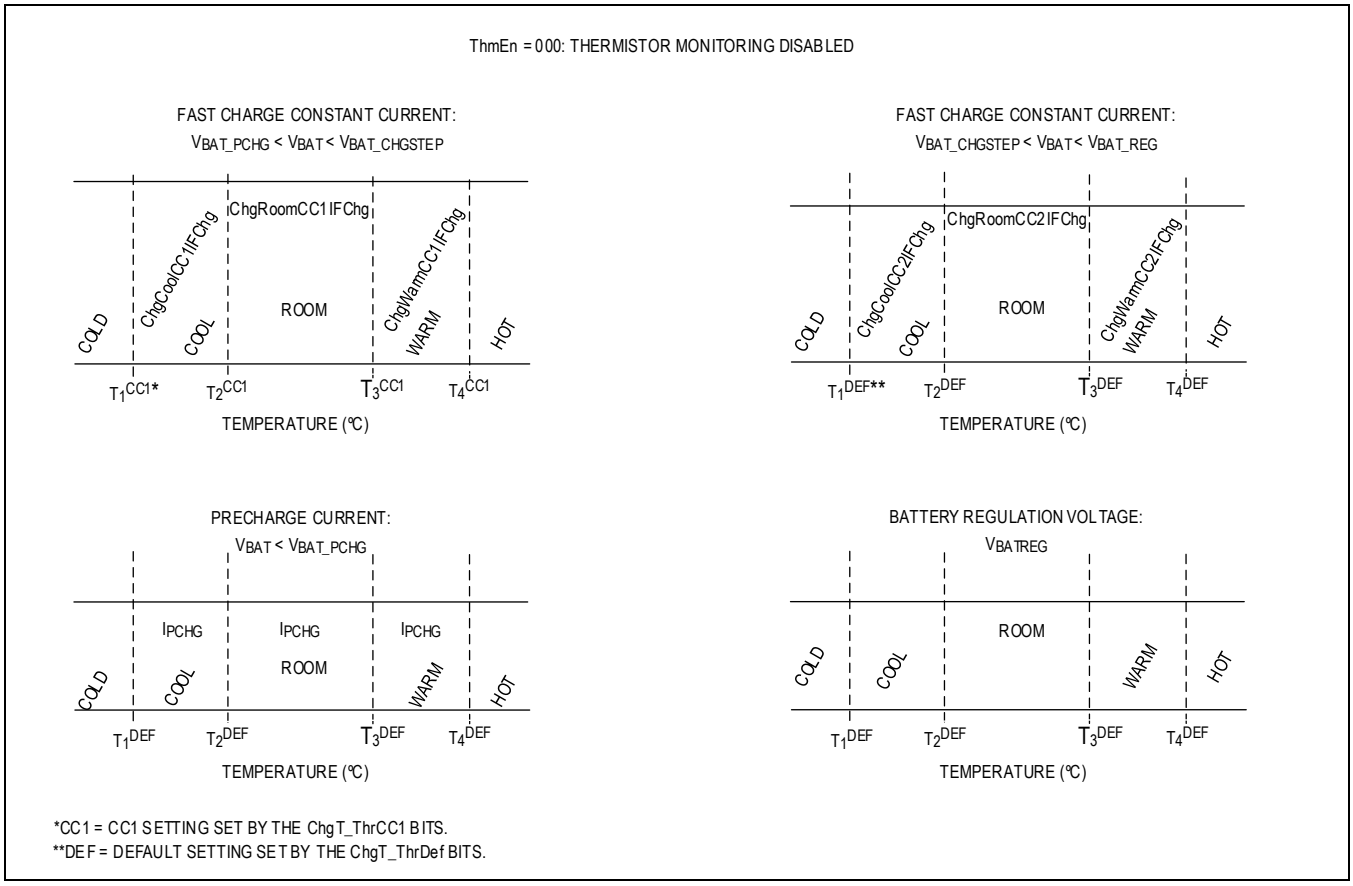


Figure 30. Temperature Monitoring Disabled

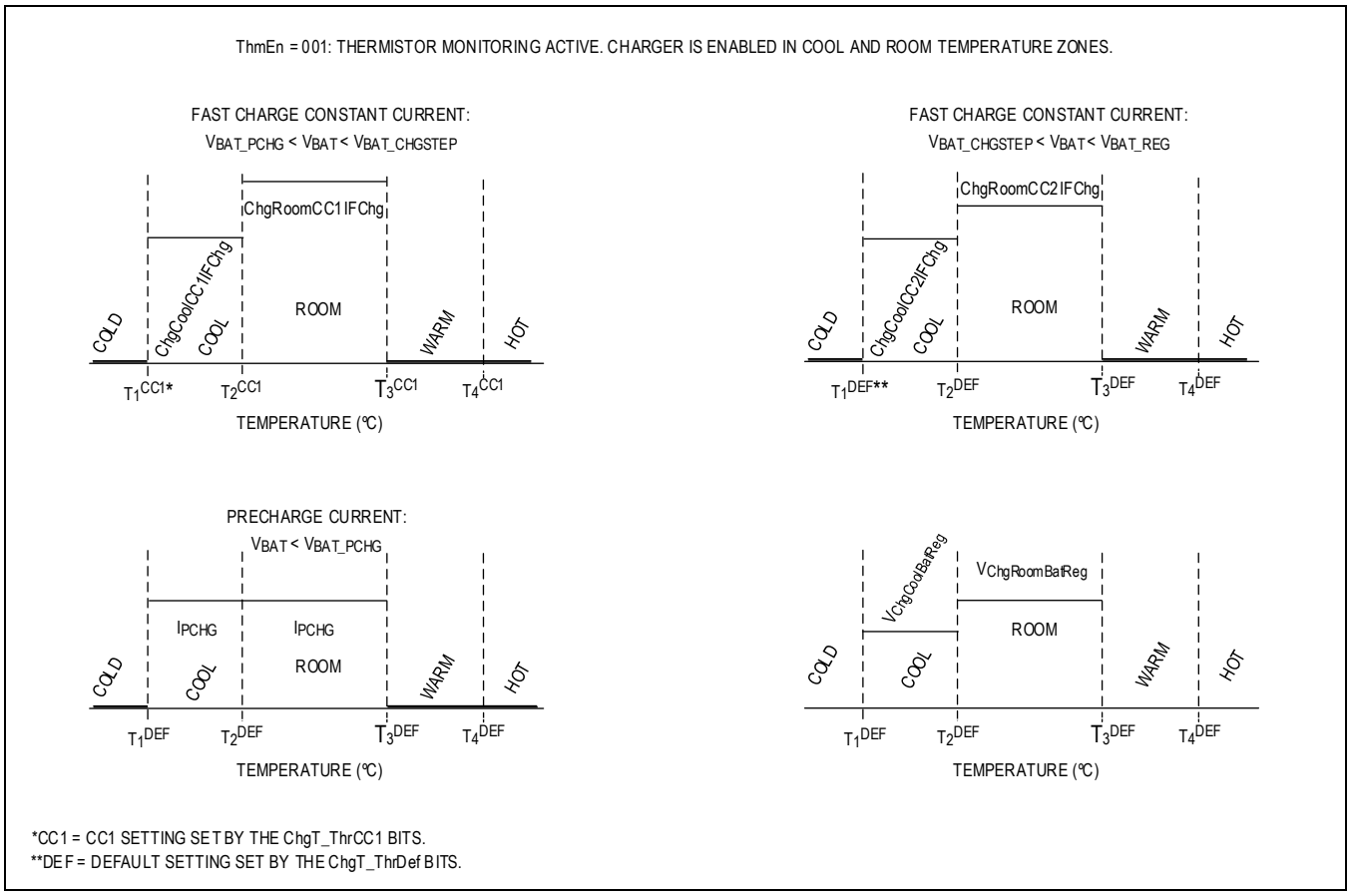


Figure 31. Charging Enabled in Cool and Room Regions

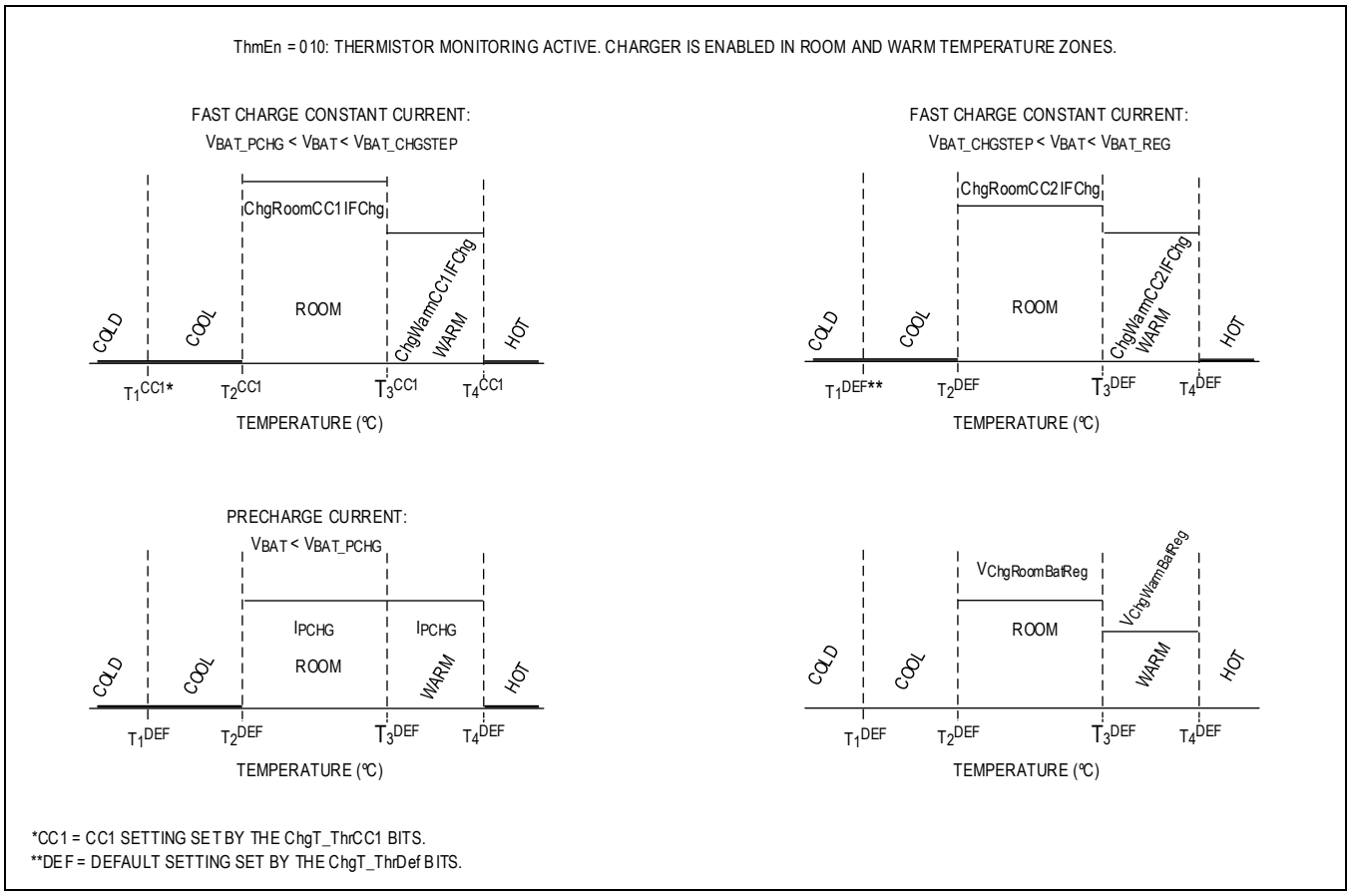


Figure 32. Charging Enabled in Room and Warm Regions

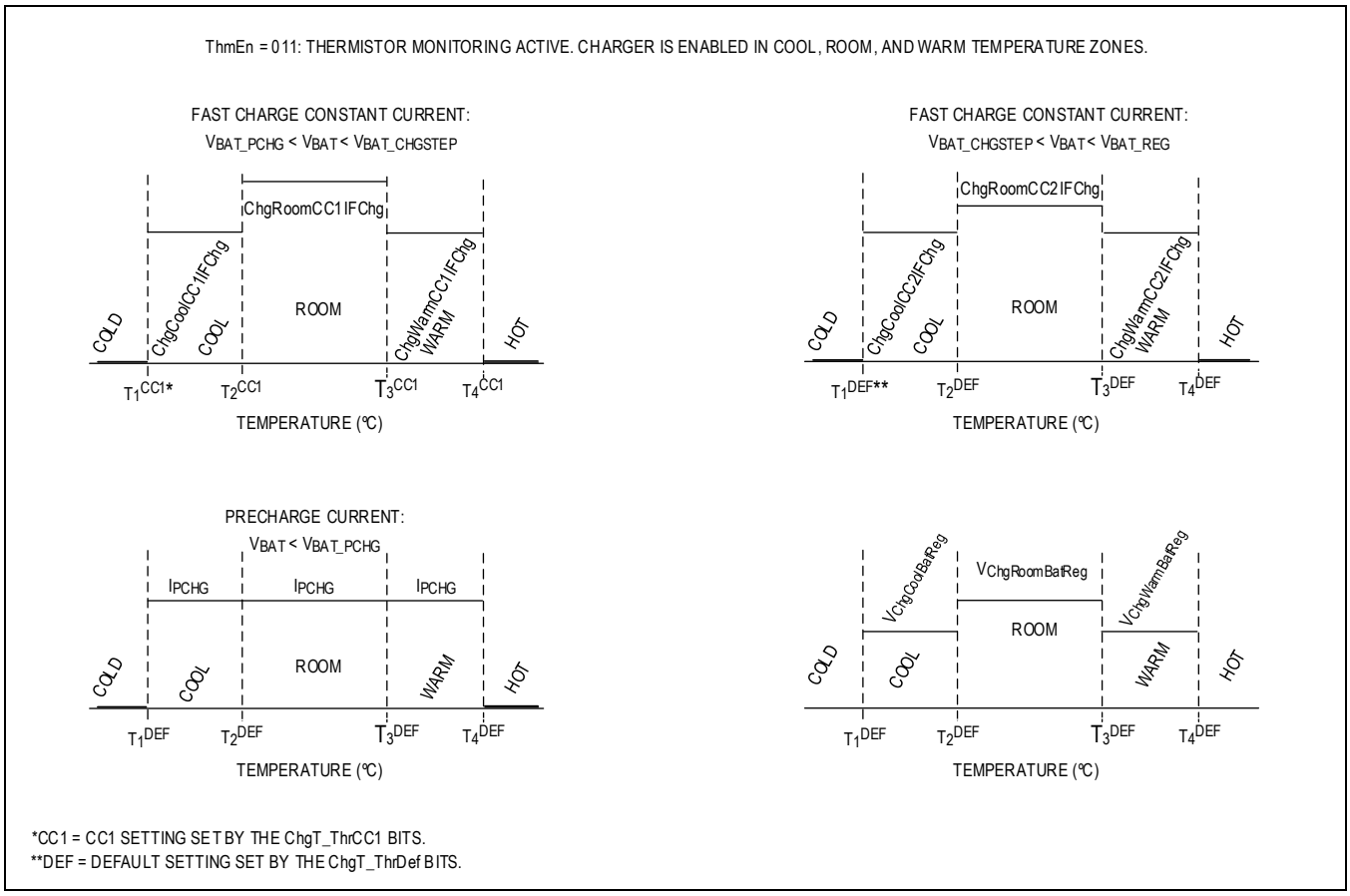


Figure 33. Charging Enabled in Cool, Room, and Warm Regions

Battery or Pack Protector Presence Detection

When pack protectors open due to a discharge-related fault, the pack protector turns off the discharge FET, placing a reverse-biased body diode in the discharge path and preventing further discharge. In this state, the system designer can decide that the battery has been damaged and that they would like to prevent a full charge cycle in the future. Even if the system designer does decide that the battery can be recovered, they can have concerns that the diode drop of the pack protector can cause the charger to presume that the battery is above the precharge voltage threshold, which would mean that the fast charge current is applied.

In this scenario, it is useful for the system to understand before starting a full charge cycle whether a pack is present on the BAT node (with an open protector) or if the battery has simply been removed. The MAX20356 contains all of the necessary circuitry to allow the system designer to implement such a check.

One example of a simple algorithm to check for such a condition is to always run the check below before starting a battery charging cycle:

After receiving a UsbOkInt interrupt (see the UsbOkInt bit) and before enabling the charger, enable the BAT pull-down resistor by writing BattPullDown = 1 (see the BattPullDown bit), wait enough time for any BAT capacitance to discharge, then check the BatUvlob status (see the BatUvlob bit) and disable the BAT pull-down resistor. If BatUvlob = 1 (see the BatUvlob bit), then the battery is present and charging can resume. If BatUvlob = 0 (see the BatUvlob bit) indicating that the BAT voltage is below the UVLO threshold either:

1) The battery is not present.

or

2) The pack protector is open.

Now turn the charger on in a forced precharge mode by writing FrcPChg = 1 and ChgEn = 1 simultaneously (see the FrcPChg and ChgEn bits) and check ChgVoltMode (see the ChgVoltMode bit). If ChgVoltMode = 1 meaning that $V_{BAT} \geq V_{BAT\_REG}$, then the battery is not present. If the battery was present, the BAT voltage would only be allowed to rise one diode drop above the actual battery voltage. If instead ChgVoltMode = 0, the battery must be present and forced precharge mode should be maintained at least long enough to unlock the pack protector.

Monitor Mux

The MAX20356 includes a voltage monitor multiplexer that can be used to multiplex the voltage of various resources onto a single external pin (IVMON). The IVMON is controlled using I^2C through the MONCfg register.

The thermistor (THM) monitoring is disabled with fuel gauge enabled (FG_OTP_ENA = 1). The FG_OTP_ENA bit is not available through I^2C and can only be changed through OTP configuration. This bit is set to 1 by default.

If the fuel gauge is permanently disabled by the OTP bit (FG_OTP_ENA = 0), THM monitoring is available. However, the user must avoid a IVMON ratio (MONRatioCfg) of 1:1.

Watchdog Timer

The MAX20356 features an integrated, programmable, watchdog timer that can be used to reset charger registers or generate soft or hard resets based on the WDCntl register. Note that the watchdog timer is active only in the on mode. When active, the application processor must read the WDTmr before the watchdog timer expires to avoid a watchdog reset. The watchdog timer interval is selected by the WDTmrSel register field. Every time the watchdog is switched on or a reset happens, the first pulse reset is skipped and the time selected in WDTmrSel is doubled for the initial timer countdown.

Fuel Gauge

The MAX20356 integrates ModelGauge m5 EZ with high-side current sensing. Refer to the *MAX17260 data sheet* for external current sensing and the *MAX17262 data sheet* for internal current sensing fuel gauge. For more details about the ModelGauge m5 algorithm, a link to the ModelGauge m5 EZ User Guide/software implementation guide, etc., refer to the Documentation and Resources tab at the *MAX17260 product page*, and see the Register Map in the *MAX17620 data sheet*.

MAX20361 Harvester Interaction

The MAX20356 implements features that allow it to seamlessly interact with the *MAX20361* solar-energy harvester chip. Register HrvBatCfg0 offers some settings for how the harvester-PMIC interaction takes place. Thresholds set on the PMIC for battery full-charge voltage and a restart threshold (see the HrvModCfg bits) set the conditions for the behavior of the PMIC described in the HrvModCfg register setting (see the HrvModCfg, HrvThmEn, and HrvThmDio bits). Interactions between the charger and harvester are intended to be seamless and system intervention should not be necessary (see the HrvFreeMPC bit).

Harvester Thermistor Monitoring

The MAX20356 harvester uses the fuel gauge thermistor to determine the temperature region such as cold, cool, room, warm, and hot to charge the battery. For additional flexibility, register HrvBatCfg0 (see the HrvBatCfg0 register) also allows behavior in the various charging temperature regions to be defined.

DC-DC/LDO/Load Switch System Faults

A system fault status is asserted in case a fault related to a DC/DC, LDO, or load switch that has been turned on automatically during the boot sequence (Buck_Seq, BBstSeq, LDO_Seq, LSW_Seq = 001, 010,011,100) occurs, and the OTP setting indicates DC/DC, LDO, or load switch as a high priority resource (register setting BCK_FltHP, BBFltHP, LDO_FltHP, LSW_FltHP = 1). A system fault is handled by the boot sequence FSM in the same way as a SysUVLO.

Register Map

PMIC Registers - Peripheral Address: 0x50/0x51

ADDRESS	NAME	MSB							LSB
USER-INTERRUPT									
0x00	RevID[7:0]	RevID[7:0]							
0x01	Status0[7:0]	ThmStat[2:0]			CC1Tmo	ChgStat[3:0]			
0x02	Status1[7:0]	SysBatLim	ChgSysLim	ILim	UsbOVP	UsbOk	ChgJEITASD	ChgJEITAReg	ThmSD
0x03	Status2[7:0]	DRPLDO3	SCLDO3	UVLOLDO3	ThmLDO3	UVLOLDO2	ThmLDO2	UVLOLDO1	ThmLDO1
0x04	Status3[7:0]	BBstFault	ThmLSW	LSW3Tmo	LSW2Tmo	LSW1Tmo	ThmBk3	ThmBk2	ThmBk1
0x05	Status4[7:0]	BatUvlob	StepChg	ChgVoltMode	ChgReStart	HrvBatCmp	–	–	–
0x07	Int0[7:0]	ThmStatInt	–	–	CC1TmoInt	–	–	–	ChgStatInt
0x08	Int1[7:0]	SysBatLimInt	ChgSysLimInt	ILimInt	UsbOVPInt	UsbOkInt	ChgJEITASDInt	ChgJEITARegInt	ThmSDInt
0x09	Int2[7:0]	DRPLDO3Int	SCLDO3Int	UVLOLDO3Int	ThmLDO3Int	UVLOLDO2Int	ThmLDO2Int	UVLOLDO1Int	ThmLDO1Int
0x0A	Int3[7:0]	BBstFaultInt	ThmLSWInt	LSW3TmoInt	LSW2TmoInt	LSW1TmoInt	ThmBk3Int	ThmBk2Int	ThmBk1Int
0x0B	Int4[7:0]	BatUvlobInt	StepChgInt	ChgVoltModeInt	ChgRestartInt	HrvBatCmpInt	–	–	–
0x0C	Int5[7:0]	WDTmr	–	–	–	–	–	–	I2cTmoInt
0x0D	IntMask0[7:0]	ThmStatIntM	–	–	CC1TmoIntM	–	–	–	ChgStatIntM
0x0E	IntMask1[7:0]	SysBatLimIntM	ChgSysLimIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgJEITASDIntM	ChgJEITARegIntM	ThmSDIntM
0x0F	IntMask2[7:0]	DRPLDO3IntM	SCLDO3IntM	UVLOLDO3IntM	ThmLDO3IntM	UVLOLDO2IntM	ThmLDO2IntM	UVLOLDO1IntM	ThmLDO1IntM
0x10	IntMask3[7:0]	BBstFaultIntM	ThmLSWIntM	LSW3TmoIntM	LSW2TmoIntM	LSW1TmoIntM	ThmBk3IntM	ThmBk2IntM	ThmBk1IntM
0x11	IntMask4[7:0]	BatUvlobIntM	StepChgIntM	ChgVoltModeM	ChgRestartM	HrvBatCmpM	–	–	–
0x12	IntMask5[7:0]	WDTmrM	–	–	–	–	–	–	I2cTmoIntM

ADDRESS	NAME	MSB							LSB
USER-LIMITER									
0x13	ILimCtrl1[7:0]	ILimBlank*[1:0]		ILimMax*[2:0]			ILimCntl*[2:0]		
0x14	ILimCtrl2[7:0]	–	–	SysDSCEn*	–	SysMinVlt*[3:0]			
USER-GMDROP									
0x16	DropCtrl[7:0]	SysUVLOThSel*[1:0]		–	–	–	–	–	–
USER-CHARGER									
0x17	ChgCur0[7:0]	–	CC1IFChg*[6:0]						
0x18	ChgCur1[7:0]	–	CC2IFChg*[6:0]						
0x19	ChgCntl0[7:0]	ChgEn*	ChgAutoStop*	ChgAutoReSta*	–	FrcRchgMonEn*	CC1RoomOnly*	CC1TmoLimit*	CC1Enable*
0x1A	ChgCntl1[7:0]	BatReChg*[1:0]		ChgBatReg*[5:0]					
0x1B	ChgCntl2[7:0]	–	VPChg*[2:0]			IPChg*[1:0]		IChgDone*[1:0]	
0x1C	ChgTmr[7:0]	MtChgTmr*[1:0]		PChgTmr*[1:0]		CC1FChgTmr*[1:0]		ChgTmr*[1:0]	
0x1D	ChgCfg0[7:0]	–	ChgStepHyst*[2:0]			ChgStepRise*[3:0]			
0x1E	ThmCfg0[7:0]	ChgCoolCC1IFChg*[2:0]			ChgCoolBatReg*[1:0]		ChgCoolCC2IFChg*[2:0]		
0x1F	ThmCfg1[7:0]	ChgRoomCC1IFChg*[2:0]			ChgRoomBatReg*[1:0]		ChgRoomCC2IFChg*[2:0]		
0x20	ThmCfg2[7:0]	ChgWarmCC1IFChg*[2:0]			ChgWarmBatReg*[1:0]		ChgWarmCC2IFChg*[2:0]		
0x21	ThmCfg3[7:0]	–	–	ChgT1ThrDef*[2:0]			ChgT1ThrCC1*[2:0]		
0x22	ThmCfg4[7:0]	–	–	ChgT2ThrDef*[2:0]			ChgT2ThrCC1*[2:0]		
0x23	ThmCfg5[7:0]	–	–	ChgT3ThrDef*[2:0]			ChgT3ThrCC1*[2:0]		
0x24	ThmCfg6[7:0]	–	–	ChgT4ThrDef*[2:0]			ChgT4ThrCC1*[2:0]		
0x25	ThmCfg7[7:0]	ChgThrmLim*[3:0]				ThmPUSel*	ThmEn*[2:0]		
0x26	ChgCtr1[7:0]	ChgFresh*	–	–	–	–	–	–	–
0x27	ChgCtr2[7:0]	–	BattPullDown*	FrcPChg*	–	–	–	–	–
0x28	HrvBatCfg0[7:0]	HrvModCfg*[1:0]		HrvThmEn*[1:0]		–	–	HrvThmDio*	HrvFreeMPC

ADDRESS	NAME	MSB							LSB
USER-MON									
0x29	MONCfg[7:0]	–	MONRatioCfg[1:0]		MONHiZ	MONCtr[3:0]			
USER-WD									
0x2A	WDCntl[7:0]	–	–	–	–	WDRstType[1:0]		WDTmrSel[1:0]	
USER-BUCK1									
0x30	Buck1Ena[7:0]	Buck1Seq[2:0]			–	–	–	Buck1En[1:0]	
0x31	Buck1Cfg0[7:0]	Buck1EnbINTGR	Buck1PGOODena	Buck1Fast	Buck1PsvDsc	Buck1ActDsc	Buck1LowEMI	Buck1FET	Buck1EnLxSns
0x32	Buck1Cfg1[7:0]	Buck1LowBW	Buck1FrcDCM	Buck1MPCFast	Buck1FPWM	Buck1EnbIADPT	–	–	–
0x33	Buck1Iset[7:0]	Buck1ISetLookUpb	–	–	–	Buck1ISet[3:0]			
0x34	Buck1VSet[7:0]	–	–	Buck1Vset[5:0]					
0x35	Buck1Ctr[7:0]	Buck1MPC7	Buck1MPC6	Buck1MPC5	Buck1MPC4	Buck1MPC3	Buck1MPC2	Buck1MPC1	Buck1MPC0
0x36	Buck1DvsCfg0[7:0]	Buck1DvsCur	–	Buck1DvsIpMax	Buck1DvsCfg[4:0]				
0x37	Buck1DvsCfg1[7:0]	–	–	Buck1DvsVlt0[5:0]					
0x38	Buck1DvsCfg2[7:0]	–	–	Buck1DvsVlt1[5:0]					
0x39	Buck1DvsCfg3[7:0]	–	–	Buck1DvsVlt2[5:0]					
0x3A	Buck1DvsCfg4[7:0]	–	–	Buck1DvsVlt3[5:0]					
0x3B	Buck1DvsSpi[7:0]	–	–	Buck1SpiVlt[5:0]					
USER-BUCK2									
0x3C	Buck2Ena[7:0]	Buck2Seq[2:0]			–	–	–	Buck2En[1:0]	

ADDRESS	NAME	MSB							LSB
0x3D	Buck2Cfg[7:0]	Buck2EnbINTGR	Buck2PGOODena	Buck2Fast	Buck2PsvDsc	Buck2ActDsc	Buck2LowEMI	Buck2FET	Buck2EnLxSns
0x3E	Buck2Cfg1[7:0]	Buck2LowBW	Buck2FrcDCM	Buck2MPCFast	Buck2FPWM	Buck2EnbIADPT	–	–	–
0x3F	Buck2Iset[7:0]	Buck2ISetLookUpb	–	–	–	Buck2ISet[3:0]			
0x40	Buck2VSet[7:0]	–	–	Buck2Vset[5:0]					
0x41	Buck2Ctr[7:0]	Buck2MPC7	Buck2MPC6	Buck2MPC5	Buck2MPC4	Buck2MPC3	Buck2MPC2	Buck2MPC1	Buck2MPC0
0x42	Buck2DvsCfg0[7:0]	Buck2DvsCur	–	Buck2DvsIpMax	Buck2DvsCfg[4:0]				
0x43	Buck2DvsCfg1[7:0]	–	–	Buck2DvsVlt0[5:0]					
0x44	Buck2DvsCfg2[7:0]	–	–	Buck2DvsVlt1[5:0]					
0x45	Buck2DvsCfg3[7:0]	–	–	Buck2DvsVlt2[5:0]					
0x46	Buck2DvsCfg4[7:0]	–	–	Buck2DvsVlt3[5:0]					
0x47	Buck2DvsSpi[7:0]	–	–	Buck2SpiVlt[5:0]					
USER-BUCK3									
0x48	Buck3Ena[7:0]	Buck3Seq[2:0]			–	–	–	Buck3En[1:0]	
0x49	Buck3Cfg[7:0]	Buck3EnbINTGR	Buck3PGOODena	Buck3Fast	Buck3PsvDsc	Buck3ActDsc	Buck3LowEMI	Buck3FET	Buck3EnLxSns
0x4A	Buck3Cfg1[7:0]	Buck3LowBW	Buck3FrcDCM	Buck3MPCFast	Buck3FPWM	Buck3EnbIADPT	–	–	–
0x4B	Buck3Iset[7:0]	Buck3ISetLookUpb	–	–	–	Buck3ISet[3:0]			
0x4C	Buck3VSet[7:0]	–	–	Buck3Vset[5:0]					

ADDRESS	NAME	MSB							LSB
0x4D	Buck3Ctr[7:0]	Buck3MPC7	Buck3MPC6	Buck3MPC5	Buck3MPC4	Buck3MPC3	Buck3MPC2	Buck3MPC1	Buck3MPC0
0x4E	Buck3DvsCfg0[7:0]	Buck3DvsCur	–	Buck3DvsIpMax	Buck3DvsCfg[4:0]				
0x4F	Buck3DvsCfg1[7:0]	–	–	Buck3DvsVlt0[5:0]					
0x50	Buck3DvsCfg2[7:0]	–	–	Buck3DvsVlt1[5:0]					
0x51	Buck3DvsCfg3[7:0]	–	–	Buck3DvsVlt2[5:0]					
0x52	Buck3DvsCfg4[7:0]	–	–	Buck3DvsVlt3[5:0]					
0x53	Buck3DvsSpi[7:0]	–	–	Buck3SpiVlt[5:0]					
USER-BUCKBOOST									
0x54	BBstEna[7:0]	BBstSeq[2:0]			–	–	–	BBstEn[1:0]	
0x55	BBstCfg[7:0]	BBstIPSetLookUpb	–	–	BBstLowEMI	BBstActDsc	BBstRampEna	BBstMode	BBstPsvDisc
0x56	BBstVSet[7:0]	–	–	BBstVSet[5:0]					
0x57	BBstISet[7:0]	BBstIPSet2[3:0]				BBstIPSet1[3:0]			
0x58	BBstCfg1[7:0]	–	BBstIpPadPEnb	BBstFast	BBZCCmpEnB	BBstFFET	BBstMPC1FCT	BBFHighSh[1:0]	
0x59	BBstCtr0[7:0]	BBstMPC7	BBstMPC6	BBstMPC5	BBstMPC4	BBstMPC3	BBstMPC2	BBstMPC1	BBstMPC0
USER-LDO1									
0x5A	LDO1Ena[7:0]	LDO1Seq[2:0]			–	–	–	LDO1En[1:0]	
0x5B	LDO1Cfg[7:0]	–	–	–	–	LDO1IntSup	LDO1ActDsc	LDO1Mode	LDO1PsvDsc
0x5C	LDO1VSet[7:0]	–	–	–	LDO1VSet[4:0]				
0x5D	LDO1Ctr[7:0]	LDO1MPC7	LDO1MPC6	LDO1MPC5	LDO1MPC4	LDO1MPC3	LDO1MPC2	LDO1MPC1	LDO1MPC0
USER-LDO2									

ADDRESS	NAME	MSB							LSB
0x5E	LDO2Ena[7:0]	LDO2Seq[2:0]			–	–	–	LDO2En[1:0]	
0x5F	LDO2Cfg[7:0]	–	–	–	LDO2_MPC0CNF	LDO2_MPC0CNT	LDO2ActDsc	LDO2Mode	LDO2PsvDsc
0x60	LDO2VSet[7:0]	–	–	–	LDO2VSet[4:0]				
0x61	LDO2Ctr[7:0]	LDO2MPC7	LDO2MPC6	LDO2MPC5	LDO2MPC4	LDO2MPC3	LDO2MPC2	LDO2MPC1	LDO2MPC0
USER-LDO3									
0x62	LDO3Ena[7:0]	LDO3Seq[2:0]			–	–	–	LDO3En[1:0]	
0x63	LDO3Cfg[7:0]	–	LDO3_MPC_CNF	LDO3_NOCLP	LDO3_HICOUT	LDO3_FRC_HIC	LDO3ActDsc	LDO3_PMOD	LDO3PsvDsc
0x64	LDO3VSet[7:0]	–	LDO3VSet[6:0]						
0x65	LDO3Ctr[7:0]	LDO3MPC7	LDO3MPC6	LDO3MPC5	LDO3MPC4	LDO3MPC3	LDO3MPC2	LDO3MPC1	LDO3MPC0
USER-LDO4									
0x66	LDO4Ena[7:0]	LDO4Seq[2:0]			–	–	–	LDO4En[1:0]	
0x67	LDO4Cfg[7:0]	–	–	–	–	LDO4VInc[1:0]		LDO4VSet	LDO4PsvDsc
0x68	LDO4Ctr[7:0]	LDO4MPC7	LDO4MPC6	LDO4MPC5	LDO4MPC4	LDO4MPC3	LDO4MPC2	LDO4MPC1	LDO4MPC0
USER-LSW1									
0x69	LSW1Ena[7:0]	LSW1Seq[2:0]			–	–	–	LSW1En[1:0]	
0x6A	LSW1Cfg[7:0]	–	–	–	–	–	LSW1ActDsc	LSW1Lowlq	LSW1PsvDsc
0x6B	LSW1Ctr[7:0]	LSW1MPC7	LSW1MPC6	LSW1MPC5	LSW1MPC4	LSW1MPC3	LSW1MPC2	LSW1MPC1	LSW1MPC0
USER-LSW2									
0x6C	LSW2Ena[7:0]	LSW2Seq[2:0]			–	–	–	LSW2En[1:0]	
0x6D	LSW2Cfg[7:0]	–	–	–	–	–	LSW2ActDsc	LSW2Lowlq	LSW2PsvDsc

ADDRESS	NAME	MSB							LSB
0x6E	LSW2Ctr[7:0]	LSW2MPC7	LSW2MPC6	LSW2MPC5	LSW2MPC4	LSW2MPC3	LSW2MPC2	LSW2MPC1	LSW2MPC0
USER-LSW3									
0x6F	LSW3Ena[7:0]	LSW3Seq[2:0]			–	–	–	LSW3En[1:0]	
0x70	LSW3Cfg[7:0]	–	–	–	–	–	LSW3ActDsc	LSW3LowIq	LSW3PsvDsc
0x71	LSW3Ctr[7:0]	LSW3MPC7	LSW3MPC6	LSW3MPC5	LSW3MPC4	LSW3MPC3	LSW3MPC2	LSW3MPC1	LSW3MPC0
USER-MPC_CONTROL									
0x72	MPC0Cfg[7:0]	MPC0Pin	–	–	MPC0Out	MPC0OD	MPC0HiZB	MPC0Res	MPC0Pup
0x73	MPC1Cfg[7:0]	MPC1Pin	–	–	MPC1Out	MPC1OD	MPC1HiZB	MPC1Res	MPC1Pup
0x74	MPC2Cfg[7:0]	MPC2Pin	–	–	MPC2Out	MPC2OD	MPC2HiZB	MPC2Res	MPC2Pup
0x75	MPC3Cfg[7:0]	MPC3Pin	–	–	MPC3Out	MPC3OD	MPC3HiZB	MPC3Res	MPC3Pup
0x76	MPC4Cfg[7:0]	MPC4Pin	–	–	MPC4Out	MPC4OD	MPC4HiZB	MPC4Res	MPC4Pup
0x77	MPC5Cfg[7:0]	MPC5Pin	–	–	MPC5Out	MPC5OD	MPC5HiZB	MPC5Res	MPC5Pup
0x78	MPC6Cfg[7:0]	MPC6Pin	–	–	MPC6Out	MPC6OD	MPC6HiZB	MPC6Res	MPC6Pup
0x79	MPC7Cfg[7:0]	MPC7Pin	–	–	MPC7Out	MPC7OD	MPC7HiZB	MPC7Res	MPC7Pup
0x7A	MPCItrSts[7:0]	–	–	–	–	USBOkMPCSts	BK3PgMPCSts	BK2PgMPCSts	BK1PgMPCSts
0x7B	BK1ItrCfg[7:0]	BK1PgMPCInt	BK1MPC6Sel	BK1MPC5Sel	BK1MPC4Sel	BK1MPC3Sel	BK1MPC2Sel	BK1MPC1Sel	BK1MPC0Sel
0x7C	BK2ItrCfg[7:0]	BK2PgMPCInt	BK2MPC6Sel	BK2MPC5Sel	BK2MPC4Sel	BK2MPC3Sel	BK2MPC2Sel	BK2MPC1Sel	BK2MPC0Sel
0x7D	BK3ItrCfg[7:0]	BK3PgMPCInt	BK3MPC6Sel	BK3MPC5Sel	BK3MPC4Sel	BK3MPC3Sel	BK3MPC2Sel	BK3MPC1Sel	BK3MPC0Sel

ADDRESS	NAME	MSB							LSB
0x7E	USBOkItrCfg[7:0]	USBOkMPCInt	USBOkMPC6Sel	USBOkMPC5Sel	USBOkMPC4Sel	USBOkMPC3Sel	USBOkMPC2Sel	USBOkMPC1Sel	USBOkMPC0Sel
USER-BOOT									
0x80	PFN[7:0]	–	–	–	–	–	–	PFN2Pin	PFN1Pin
0x81	BootCfg[7:0]	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		ChgAlwTry
USER-COMMAND									
0x82	PwrCfg[7:0]	–	INTBootMsk	–	–	–	–	–	StayOn
0x83	PwrCmd[7:0]	PwrCmd[7:0]							
0x84	MiscFunctions[7:0]	–	–	–	–	MiscFunc[3:0]			
0x86	LockMsk1[7:0]	LD4Lck	LD3Lck	LD2Lck	LD1Lck	BBLck	BK3Lck	BK2Lck	BK1Lck
0x87	LockMsk2[7:0]	LD4SeqLck	LD3SeqLck	LD2SeqLck	LD1SeqLck	BBSeqLck	BK3SeqLck	BK2SeqLck	BK1SeqLck
0x89	LockMsk3[7:0]	LSW3SeqLck	LSW2SeqLck	LSW1SeqLck	–	WDLck	GMDrpLck	LimLck	ChgLck
0x8A	LockUnlock1[7:0]	PASSWD1[7:0]							
0x8B	LockUnlock2[7:0]	PASSWD2[7:0]							
0x8C	LockUnlock3[7:0]	PASSWD3[7:0]							
USER-OTP									
0x8D	I2C_OTPADD[7:0]	OTPDIG__ADD[7:0]							
0x8E	I2C_OTPDAT[7:0]	OTPDIG__DAT[7:0]							

Register Details

RevID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	RevID[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RevID	7:0	RevID[7:0] bits show information about the hardware revision of the MAX20356.

Status0 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	ThmStat[2:0]			CC1Tmo	ChgStat[3:0]			
Reset	0b000			0b0	0x0			
Access Type	Read Only			Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
ThmStat	7:5	Status of Thermistor Monitoring.	000: Cold zone (V_{THM_COLD} < V_{THM} < V_{THM_DIS}). 001: Cool zone(V_{THM_COOL} < V_{THM} < V_{THM_COLD}). 010: Room zone (V_{THM_WARM} < V_{THM} < V_{THM_COOL}). 011: Warm zone (V_{THM_HOT} < V_{THM} < V_{THM_WARM}). 100: Hot zone (V_{THM} < V_{THM_HOT}) 101: No thermistor detected (V_{THM} > V_{THM_DIS}). 110: Thermistor monitoring disabled because CHGIN input voltage is present and ThmEn[1:0] = 00 or because CHGIN input voltage is not present and ThmEn[1:0] = HrvThmEn[1:0] = 00. 111: Thermistor monitoring disabled because CHGIN input voltage is not present, ThmEn[1:0] is not equal to 00 and HrvThmEn[1:0] = 00.
CC1Tmo	4	Status of CC1 Timeout (Based on CC1FChgTmr).	0: CC1 timeout not expired. 1: CC1 timeout expired.
ChgStat	3:0	Status of Charger.	0000: Charger off 0001: Charger IDLE mode 0010: Pre-charge in progress 0011: Fast-charge Constant Current mode 1 (CC1) in progress 0100: Fast-charge Constant current mode 2 (CC2) in progress 0101: Fast-charge Constant Voltage mode (CV) in progress 0110: Maintain charge in progress 0111: Maintain charger timer done 1000: Charger Fault - PChgTmr Expired 1001: Charger Fault - Safety Timer ChgTmr Expired 1010: RFU

BITFIELD	BITS	DESCRIPTION	DECODE
			1011: RFU 1100: RFU 1101: RFU 1110: CC Tracking in progress 1111: Charging suspended due to temperature (see battery charger state diagram)

Status1 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	SysBatLim	ChgSysLim	ILim	UsbOVP	UsbOk	ChgJEITASD	ChgJEITAReg	ThmSD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SysBatLim	7	Status of Charger Regulation due to SYS Voltage. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = 01 and charger is enabled.	0: Charge current is not being actively reduced to regulate V_{SYS}. 1: Charge current actively being reduced to regulate V_{SYS} collapse.
ChgSysLim	6	Status of Input Limiter Regulation due to CHGIN Voltage. Valid only when CHGIN input voltage is present and [UsbOVP,UsbOk] = 01.	0: Input limiter current is not being actively reduced to regulate V_{CHGIN}. 1: Input limiter current is actively being reduced to regulate V_{CHGIN} collapse.
ILim	5	Status of CHGIN Input Current Limit. Valid only when CHGIN input voltage is present and [UsbOVP,UsbOk] = 01.	0: CHGIN input current below limit. 1: CHGIN input current limit active.
UsbOVP	4	Status of CHGIN Overvoltage Protection (OVP).	0: CHGIN overvoltage not detected. 1: CHGIN overvoltage detected.
UsbOk	3	Status of CHGIN Input Voltage.	0: CHGIN input voltage not present or outside of valid range. 1: CHGIN input voltage present and valid.
ChgJEITASD	2	Status of Battery Charger Shutdown due to JEITA. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = 01 and charger is enabled.	0: Charger operating normally or disabled. 1: Charger disabled due to JEITA.
ChgJEITAReg	1	Status of Battery Charger Current or Voltage Reduction due to JEITA. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = 01 and charger is enabled.	0: Charger operating normally or disabled. 1: Charger current or voltage being actively reduced due to JEITA.
ThmSD	0	Status of Input Limiter and Charger Thermal Shutdown. Valid only when CHGIN input voltage is present.	0: Input limiter and charger operating normally. 1: Input limiter and charger in thermal shutdown.

Status2 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	DRPLDO3	SCLDO3	UVLOLDO3	ThmLDO3	UVLOLDO2	ThmLDO2	UVLOLDO1	ThmLDO1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DRPLDO3	7	Status of LDO3 Drop Out.	0: LDO3 operating normally. 1: LDO3 DRP active.
SCLDO3	6	Status of LDO3 Short Circuit.	0: LDO3 operating normally. 1: LDO3 short circuit active.
UVLOLDO3	5	Status of LDO3 UVLO.	0: LDO3 operating normally. 1: LDO3 UVLO active.
ThmLDO3	4	Status of LDO3 Thermal Shutdown.	0: LDO3 operating normally. 1: LDO3 in thermal shutdown.
UVLOLDO2	3	Status of LDO2 UVLO.	0: LDO2 operating normally. 1: LDO2 UVLO active.
ThmLDO2	2	Status of LDO2 Thermal Shutdown.	0: LDO2 operating normally. 1: LDO2 in thermal shutdown.
UVLOLDO1	1	Status of LDO1 UVLO.	0: LDO1 operating normally. 1: LDO1 UVLO active.
ThmLDO1	0	Status of LDO1 Thermal Shutdown.	0: LDO1 operating normally. 1: LDO1 in thermal shutdown.

Status3 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	BBstFault	ThmLSW	LSW3Tmo	LSW2Tmo	LSW1Tmo	ThmBk3	ThmBk2	ThmBk1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFault	7	Status of Buck-Boost Fault.	0: Buck-boost operating normally. 1: Buck-boost under fault condition.
ThmLSW	6	Status of LSW1, LSW2, and LSW3 Thermal Shutdown.	0: All the above blocks are operating normally. 1: One of the above blocks is in thermal shutdown.
LSW3Tmo	5	LSW3 Failed to Start Up During the Timeout Period.	
LSW2Tmo	4	LSW2 Failed to Start Up During the Timeout Period.	
LSW1Tmo	3	LSW1 Failed to Start Up During the Timeout Period.	
ThmBk3	2	Status of Buck3 Thermal Shutdown.	0: Buck3 operating normally. 1: Buck3 in thermal shutdown.
ThmBk2	1	Status of Buck2 Thermal Shutdown.	0: Buck2 operating normally. 1: Buck2 in thermal shutdown.

BITFIELD	BITS	DESCRIPTION	DECODE
ThmBk1	0	Status of Buck1 Thermal Shutdown.	0: Buck1 operating normally. 1: Buck1 in thermal shutdown.

Status4 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	BatUvlob	StepChg	ChgVoltMode	ChgReStart	HrvBatCmp	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BatUvlob	7	Status of Charger BatGood Comparator. Valid only when CHGIN input voltage is present and [UsbOVP,UsbOk] = 01.	0: $V_{BAT} < V_{BAT\_UVLO}$. 1: $V_{BAT} > V_{BAT\_UVLO}$ or CHGIN input voltage not present.
StepChg	6	Status of Charger Step-Charge Current Reduction. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = 01 and charger is enabled.	0: Charger step-charge current reduction not active. 1: Charger step-charge current reduction active.
ChgVoltMode	5	Status of Charger BAT Voltage Regulation. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = 01, charger is enabled and SysBatLim = 0.	0: $V_{BAT} < V_{BAT\_REG}$. 1: $V_{BAT} \geq V_{BAT\_REG}$.
ChgReStart	4	Status of Charger BAT Restart Comparator. Valid only when CHGIN input voltage is present, [UsbOVP,UsbOk] = 01, charger is enabled and SysBatLim = 0.	0: $V_{BAT} < V_{BAT\_RECHG}$. 1: $V_{BAT} \geq V_{BAT\_RECHG}$.
HrvBatCmp	3	Status of Harvester BAT Comparator. Valid only when harvester interaction is enabled when HrvEn = 1.	0: $V_{BAT} < V_{BAT\_REG}$. 1: $V_{BAT} > V_{BAT\_REG}$.

Int0 (0x7)

BIT	7	6	5	4	3	2	1	0
Field	ThmStatInt	–	–	CC1TmoInt	–	–	–	ChgStatInt
Reset	0b0	–	–	0b0	–	–	–	0b0
Access Type	Write, Read	–	–	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ThmStatInt	7	Change in ThmStat[2:0] Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
CC1TmoInt	4	Change in CC1 Timeout Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ChgStatInt	0	Change in ChgStat[3:0] Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.

Int1 (0x8)

BIT	7	6	5	4	3	2	1	0
Field	SysBatLimInt	ChgSysLimInt	ILimInt	UsbOVPInt	UsbOkInt	ChgJEITASDInt	ChgJEITARegInt	ThmSDInt
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SysBatLimInt	7	Change in SysBatLim Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ChgSysLimInt	6	Change in ChgSysLim Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ILimInt	5	Change in ILim Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
UsbOVPInt	4	Change in UsbOVP Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
UsbOkInt	3	Change in UsbOk Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ChgJEITASDInt	2	Change in ChgJEITASD Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ChgJEITARegInt	1	Change in ChgJEITAReg Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmSDInt	0	Change in ThmSD Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.

Int2 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	DRPLDO3Int	SCLDO3Int	UVLOLDO3Int	ThmLDO3Int	UVLOLDO2Int	ThmLDO2Int	UVLOLDO1Int	ThmLDO1Int
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DRPLDO3Int	7	Change in DRPLDO3 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.

BITFIELD	BITS	DESCRIPTION	DECODE
SCLDO3Int	6	Change in SCLDO3 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
UVLOLDO3Int	5	Change in UVLOLDO3 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmLDO3Int	4	Change in ThmLDO3 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
UVLOLDO2Int	3	Change in UVLOLDO2 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmLDO2Int	2	Change in ThmLDO2 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
UVLOLDO1Int	1	Change in UVLOLDO1 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmLDO1Int	0	Change in ThmLDO1 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.

Int3 (0xA)

BIT	7	6	5	4	3	2	1	0
Field	BBstFaultInt	ThmLSWInt	LSW3TmoInt	LSW2TmoInt	LSW1TmoInt	ThmBk3Int	ThmBk2Int	ThmBk1Int
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFaultInt	7	Change in BBstFault Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmLSWInt	6	Change in ThmLSW Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
LSW3TmoInt	5	Change in LSW3Tmo Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
LSW2TmoInt	4	Change in LSW2Tmo Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
LSW1TmoInt	3	Change in LSW1Tmo Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmBk3Int	2	Change in ThmBk3 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmBk2Int	1	Change in ThmBk2 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ThmBk1Int	0	Change in ThmBk1 Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.

Int4 (0xB)

BIT	7	6	5	4	3	2	1	0
Field	BatUvlobInt	StepChgInt	ChgVoltModeInt	ChgRestartInt	HrvBatCmpInt	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–

Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BatUvlobInt	7	Change in BatUvlob Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
StepChgInt	6	Change in StepChg Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ChgVoltModeInt	5	Change in ChgVoltMode Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
ChgRestartInt	4	Change Restart Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.
HrvBatCmpInt	3	Change in HrvBatCmp Caused an Interrupt.	0x0: Not triggered since last read. 0x1: Triggered.

Int5 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	WDTmr	–	–	–	–	–	–	I2cTmoInt
Reset	0b0	–	–	–	–	–	–	0b0
Access Type	Write, Read	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDTmr	7	If read, watchdog does not reset the device at internal timer end.	0x0: Bit read: does not reset at the end of the timer. 0x1: Bit not read since last timer end.
I2cTmoInt	0	I^2C watchdog timer expired due to 100ms bus inactivity between start and stop conditions.	0x0: Not triggered since last read. 0x1: Triggered.

IntMask0 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	ThmStatIntM	–	–	CC1TmoIntM	–	–	–	ChgStatIntM
Reset	0b0	–	–	0b0	–	–	–	0b0
Access Type	Write, Read	–	–	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ThmStatIntM	7	ThmStatIntM Masks the ThmStatInt Interrupt in the Int0 Register (0x07).	0: Masked. 1: Not masked.
CC1TmoIntM	4	CC1TmoIntM Masks the CC1TmoInt Interrupt in the Int0 Register (0x07).	0: Masked. 1: Not masked.

BITFIELD	BITS	DESCRIPTION	DECODE
ChgStatIntM	0	ChgStatIntM Masks the ChgStatInt Interrupt in the Int0 Register (0x07).	0: Masked. 1: Not masked.

IntMask1 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	SysBatLimIntM	ChgSysLimIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgJEITASDIntM	ChgJEITARegIntM	ThmSDIntM
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SysBatLimIntM	7	SysBatLimIntM Masks the SysBatLimInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
ChgSysLimIntM	6	ChgSysLimIntM Masks the ChgSysLimInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
ILimIntM	5	ILimIntM Masks the ILimInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
UsbOVPIntM	4	UsbOVPIntM Masks the UsbOVPInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
UsbOkIntM	3	UsbOkIntM Masks the UsbOkInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
ChgJEITASDIntM	2	ChgJEITASDIntM Masks the ChgJEITASDInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
ChgJEITARegIntM	1	ChgJEITARegIntM Masks the ChgJEITARegInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.
ThmSDIntM	0	ThmSDIntM Masks the ThmSDInt Interrupt in the Int1 Register (0x08).	0: Masked. 1: Not masked.

IntMask2 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	DRPLDO3IntM	SCLDO3IntM	UVLOLDO3IntM	ThmLDO3IntM	UVLOLDO2IntM	ThmLDO2IntM	UVLOLDO1IntM	ThmLDO1IntM
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DRPLDO3IntM	7	DRPLDO3IntM Masks the DRPLDO3Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
SCLDO3IntM	6	SCLDO3IntM Masks the SCLDO3Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
UVLOLDO3IntM	5	UVLOLDO3IntM Masks the UVLOLDO3Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
ThmLDO3IntM	4	ThmLDO3IntM Masks the ThmLDO3Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
UVLOLDO2IntM	3	UVLOLDO2IntM Masks the UVLOLDO2Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
ThmLDO2IntM	2	ThmLDO2IntM Masks the ThmLDO2Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
UVLOLDO1IntM	1	UVLOLDO1IntM Masks the UVLOLDO1Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.
ThmLDO1IntM	0	ThmLDO1IntM Masks the ThmLDO1Int Interrupt in the Int2 Register (0x09).	0: Masked. 1: Not masked.

IntMask3 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	BBstFaultIntM	ThmLSWIntM	LSW3TmoIntM	LSW2TmoIntM	LSW1TmoIntM	ThmBk3IntM	ThmBk2IntM	ThmBk1IntM
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFaultIntM	7	BBstFaultIntM Masks the BBstFaultInt Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.
ThmLSWIntM	6	ThmLSWIntM Masks the ThmLSWInt Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.
LSW3TmoIntM	5	LSW3TmoIntM Masks the LSW3TmoInt Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.
LSW2TmoIntM	4	LSW2TmoIntM Masks the LSW2TmoInt Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1TmoIntM	3	LSW1TmoIntM Masks the LSW1TmoInt Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.
ThmBk3IntM	2	ThmBk3IntM Masks the ThmBk3Int Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.
ThmBk2IntM	1	ThmBk2IntM Masks the ThmBk2Int Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.
ThmBk1IntM	0	ThmBk1IntM Masks the ThmBk1Int Interrupt in the Int3 Register (0xA).	0: Masked. 1: Not masked.

IntMask4 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	BatUvlobIntM	StepChgIntM	ChgVoltModeM	ChgRestartM	HrvBatCmpM	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BatUvlobIntM	7	BatUvlobIntM Masks the BatUvlobInt Interrupt in the Int4 Register (0xB).	0: Masked. 1: Not masked.
StepChgIntM	6	StepChgIntM Masks the StepChgInt Interrupt in the Int4 Register (0xB).	0: Masked. 1: Not masked.
ChgVoltModeM	5	ChgVoltModeM Masks the ChgVoltModeInt Interrupt in the Int4 Register (0xB).	0: Masked. 1: Not masked.
ChgRestartM	4	ChgRestartM Masks the ChgRestartInt Interrupt in the Int4 Register (0xB).	0: Masked. 1: Not masked.
HrvBatCmpM	3	HrvBatCmpM Masks the HrvBatCmpInt Interrupt in the Int4 Register (0xB).	0: Masked. 1: Not masked.

IntMask5 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	WDTmrM	–	–	–	–	–	–	I2cTmoIntM
Reset	0b0	–	–	–	–	–	–	0b0
Access Type	Write, Read	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WDTmrM	7	WDTmrM Masks the WDTmr Interrupt in the Int5 Register .	0: Masked. 1: Not masked.
I2cTmoIntM	0	I2cTmoIntM Masks the I2cTmoInt Interrupt in the Int5 Register.	0: Masked. 1: Not masked.

ILimCtrl1 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	ILimBlank*[1:0]		ILimMax*[2:0]			ILimCntl*[2:0]		
Reset	0b00		0b000			0b000		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ILimBlank*	7:6	CHGIN Input Current Limiter Blanking Time (During Which the Current is Limited to I_{LIM_MAX}).	00: No debounce (allow a few clock cycles for resampling). 01: 0.5ms. 10: 1.0ms. 11: 10.0ms.
ILimMax*	5:3	CHGIN Input Current Limiter During Blanking Time (During Which the Current is Limited to I_{LIM_MAX}).	000: 90mA. 001: 150mA. 010: 200mA. 011: 300mA. 100: 400mA. 101: 450mA. 110: 1000mA. 111: 1500mA.
ILimCntl*	2:0	CHGIN Programmable Input Current Limit. In case ILimCntl > ILimMax, then CHGIN current is limited to ILimMax.	000: 90mA. 001: 150mA. 010: 200mA. 011: 300mA. 100: 400mA. 101: 450mA. 110: 1000mA. 111: 1500mA.

ILimCtrl2 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SysDSCEn*	–	SysMinVlt*[3:0]			
Reset	–	–	0b0	–	0x0			
Access Type	–	–	Write, Read	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SysDSCEn*	5	SYS Discharge in Battery Recovery Mode Enable.	0: No SYS discharge. 1: Enable SYS discharge prior to entering battery recovery mode.
SysMinVlt*	3:0	System (SYS) Minimum Regulated Voltage.	0000: 3.3V. 0001: 3.4V. 0010: 3.5V. 0011: 3.6V. 0100: 3.7V. 0101: 3.8V. 0110: 3.9V. 0111: 4.0V. 1000: 4.1V. 1001: 4.2V. 1010: 4.3V. 1011: 4.4V. 1100: 4.5V. 1101: 4.6V. 1110: 4.7V. 1111: 4.8V.

DropCtrl (0x16)

BIT	7	6	5	4	3	2	1	0
Field	SysUVLOThSel*[1:0]		–	–	–	–	–	–
Reset	0b00		–	–	–	–	–	–
Access Type	Write, Read		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SysUVLOThSel*	7:6	SYS UVLO Threshold.	00: 2.7V. 01: 2.9V. 10: 3.0V. 11: 3.2V.

ChgCur0 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	–	CC1IFChg*[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CC1IFChg*	6:0	Fast Charge Constant Current Zone 1 Charge Current Setting. 4mA to 500mA with the steps shown in the decode. Note: accuracy may be worse with settings below 10mA.	0x0: 4. 0x1: 6. 0x2: 8. 0x3: 10. 0x4: 12. 0x5: 14. 0x6: 16.

BITFIELD	BITS	DESCRIPTION	DECODE
			0x7: 18. 0x8: 20. 0x9: 22. 0xA: 24. 0xB: 26. 0xC: 28. 0xD: 30. 0xE: 32. 0xF: 34. 0x10: 36. 0x11: 38. 0x12: 40. 0x13: 42. 0x14: 44. 0x15: 46. 0x16: 48. 0x17: 50. 0x18: 52. 0x19: 54. 0x1A: 56. 0x1B: 58. 0x1C: 60. 0x1D: 62. 0x1E: 64. 0x1F: 66. 0x20: 68. 0x21: 70. 0x22: 72. 0x23: 74. 0x24: 76. 0x25: 78. 0x26: 80. 0x27: 82. 0x28: 84. 0x29: 86. 0x2A: 88. 0x2B: 90. 0x2C: 92. 0x2D: 94. 0x2E: 96. 0x2F: 98. 0x30: 100. 0x31: 102. 0x32: 104. 0x33: 106. 0x34: 108. 0x35: 110. 0x36: 112. 0x37: 114. 0x38: 116. 0x39: 118. 0x3A: 120. 0x3B: 122. 0x3C: 124. 0x3D: 126. 0x3E: 128. 0x3F: 130. 0x40: 140. 0x41: 150. 0x42: 160. 0x43: 170. 0x44: 180. 0x45: 190. 0x46: 200. 0x47: 210. 0x48: 220. 0x49: 230. 0x4A: 240. 0x4B: 250. 0x4C: 260.

BITFIELD	BITS	DESCRIPTION	DECODE
			0x4D: 270. 0x4E: 280. 0x4F: 290. 0x50: 300. 0x51: 310. 0x52: 320. 0x53: 330. 0x54: 340. 0x55: 350. 0x56: 360. 0x57: 370. 0x58: 380. 0x59: 390. 0x5A: 400. 0x5B: 410. 0x5C: 420. 0x5D: 430. 0x5E: 440. 0x5F: 450. 0x60: 460. 0x61: 470. 0x62: 480. 0x63: 490. 0x64: 500. Others: 500.

ChgCur1 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	–	CC2IFChg*[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CC2IFChg*	6:0	Fast Charge Constant Current Zone 2 Charge Current Setting. 4mA to 500mA with the steps shown in the decode. Note: accuracy may be worse with settings below 10mA.	0x0: 4. 0x1: 6. 0x2: 8. 0x3: 10. 0x4: 12. 0x5: 14. 0x6: 16. 0x7: 18. 0x8: 20. 0x9: 22. 0xA: 24. 0xB: 26. 0xC: 28. 0xD: 30. 0xE: 32. 0xF: 34. 0x10: 36. 0x11: 38. 0x12: 40. 0x13: 42. 0x14: 44. 0x15: 46. 0x16: 48. 0x17: 50. 0x18: 52.

BITFIELD	BITS	DESCRIPTION	DECODE
			0x19: 54. 0x1A: 56. 0x1B: 58. 0x1C: 60. 0x1D: 62. 0x1E: 64. 0x1F: 66. 0x20: 68. 0x21: 70. 0x22: 72. 0x23: 74. 0x24: 76. 0x25: 78. 0x26: 80. 0x27: 82. 0x28: 84. 0x29: 86. 0x2A: 88. 0x2B: 90. 0x2C: 92. 0x2D: 94. 0x2E: 96. 0x2F: 98. 0x30: 100. 0x31: 102. 0x32: 104. 0x33: 106. 0x34: 108. 0x35: 110. 0x36: 112. 0x37: 114. 0x38: 116. 0x39: 118. 0x3A: 120. 0x3B: 122. 0x3C: 124. 0x3D: 126. 0x3E: 128. 0x3F: 130. 0x40: 140. 0x41: 150. 0x42: 160. 0x43: 170. 0x44: 180. 0x45: 190. 0x46: 200. 0x47: 210. 0x48: 220. 0x49: 230. 0x4A: 240. 0x4B: 250. 0x4C: 260. 0x4D: 270. 0x4E: 280. 0x4F: 290. 0x50: 300. 0x51: 310. 0x52: 320. 0x53: 330. 0x54: 340. 0x55: 350. 0x56: 360. 0x57: 370. 0x58: 380. 0x59: 390. 0x5A: 400. 0x5B: 410. 0x5C: 420. 0x5D: 430. 0x5E: 440.

BITFIELD	BITS	DESCRIPTION	DECODE
			0x5F: 450. 0x60: 460. 0x61: 470. 0x62: 480. 0x63: 490. 0x64: 500. Others: 500.

ChgCntl0 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	ChgEn*	ChgAutoStop*	ChgAutoReSta*	–	FrcRchgMonEn*	CC1RoomOnly*	CC1TmoLimit*	CC1Enable*
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ChgEn*	7	Charger On/Off Control. Does not affect input limiter and SYS node.	0: Charger disabled. 1: Charger enabled.
ChgAutoStop*	6	Charger Autostop Control. Controls the transition from maintain charge to maintain charge done. See the Battery Charger State Diagram.	0: Autostop disabled. 1: Autostop enabled.
ChgAutoReSta*	5	Charger Auto-Restart Control. See Battery Charger State Diagram.	0: Charger remains in maintain-charge done even when V_{BAT} is less than recharge threshold. 1: Charger automatically restarts when V_{BAT} drops below recharge threshold.
FrcRchgMonEn*	3	Enable Control for the Recharge Battery Threshold Comparator. This control bit is useful when ChgEn = 0 to allow the recharge battery monitor to keep running. When ChgEn = 1 this bit is don't care and the recharge battery monitor is enabled.	0: Recharge Battery monitor disabled. 1: Recharge Battery monitor enabled.
CC1RoomOnly*	2	Sets the Behavior of Step Charging. If set to 1, CC1 fast charge works in room zone only.	0: Run CC1 in any THM temperatrue range based on ThmEn and ThmCfgX regs. 1: Run CC1 at THM room temperature only.
CC1TmoLimit*	1	Sets the Behavior of Step Charging. CC1 fast charge phase runs without timer limitation.	0: Run CC1 phase with no timer. Limitation due to CC1FChgTmr. 1: Run CC1 phase with timer. Limitation set by CC1FChgTmr.
CC1Enable*	0	Enable Control for the CC1 Charging Phase. Allows the unit to step charge the battery by entering the CC1 charging phase. If set to 0, charger only works in CC2 fast charge state and step charging is disabled.	0: CC1 phase disabled (not entered or skipped). 1: CC1 phase enabled.

ChgCntl1 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	BatReChg*[1:0]		ChgBatReg*[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BatReChg*	7:6	Charger Recharge Threshold in Relation to ChgBatReg[5:0].	00: ChgBatReg[5:0] - 50mV. 01: ChgBatReg[5:0] - 100mV. 10: ChgBatReg[5:0] - 150mV. 11: ChgBatReg[5:0] - 220mV.
ChgBatReg*	5:0	Charger Battery Regulation Voltage.	0x0: 4.15V. 0x1: 4.16V. 0x2: 4.17V. 0x3: 4.18V. 0x4: 4.19V. 0x5: 4.20V. 0x6: 4.21V. 0x7: 4.22V. 0x8: 4.23V. 0x9: 4.24V. 0xA: 4.25V. 0xB: 4.26V. 0xC: 4.27V. 0xD: 4.28V. 0xE: 4.29V. 0xF: 4.30V. 0x10: 4.31V. 0x11: 4.32V. 0x12: 4.33V. 0x13: 4.34V. 0x14: 4.35V. 0x15: 4.36V. 0x16: 4.37V. 0x17: 4.38V. 0x18: 4.39V. 0x19: 4.40V. 0x1A: 4.41V. 0x1B: 4.42V. 0x1C: 4.43V. 0x1D: 4.44V. 0x1E: 4.45V. 0x1F: 4.46V. 0x20: 4.47V. 0x21: 4.48V. 0x22: 4.49V. 0x23: 4.50V. 0x24: 4.51V. 0x25: 4.52V. 0x26: 4.53V. 0x27: 4.54V. 0x28: 4.55V. 0x29: 4.56V. 0x2A: 4.57V. 0x2B: 4.58V. 0x2C: 4.59V. 0x2D: 4.60V. 0x2E: 4.61V. 0x2F: 4.62V. 0x30: 4.63V. 0x31: 4.64V. 0x32: 4.65V. 0x33: 4.66V.

BITFIELD	BITS	DESCRIPTION	DECODE
			0x34: 4.67V. 0x35: 4.68V. 0x36: 4.69V. 0x37: 4.70V. 0x38: 4.70V. 0x39: 4.70V. 0x3A: 4.70V. 0x3B: 4.70V. 0x3C: 4.70V. 0x3D: 4.70V. 0x3E: 4.70V. 0x3F: 4.70V.

ChgCntl2 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	–	VPChg*[2:0]			IPChg*[1:0]		IChgDone*[1:0]	
Reset	–	0b000			0b00		0b00	
Access Type	–	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VPChg*	6:4	Charger Precharge Voltage Rising Threshold.	000: 2.70V. 001: 2.80V. 010: 2.90V. 011: 3.00V. 100: 3.10V. 101: 3.20V. 110: 3.30V. 111: 3.40V.
IPChg*	3:2	Charger Precharge Current.	00: 0.05 x I_{FCHG}. 01: 0.10 x I_{FCHG}. 10: 0.20 x I_{FCHG}. 11: 0.30 x I_{FCHG}.
IChgDone*	1:0	Charger Charge-Done Current Threshold.	00: 0.025 x I_{FCHG}. 01: 0.05 x I_{FCHG}. 10: 0.10 x I_{FCHG}. 11: 0.20 x I_{FCHG}.

ChgTmr (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	MtChgTmr*[1:0]		PChgTmr*[1:0]		CC1FChgTmr*[1:0]		ChgTmr*[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MtChgTmr*	7:6	Charger Maintain-Charge Timer.	00: 0min. 01: 15min. 10: 30min. 11: 60min.
PChgTmr*	5:4	Charger Precharge Timer.	00: 30min. 01: 60min. 10: 120min. 11: 240min.
CC1FChgTmr*	3:2	Charger Fast Charge CC1 State Timer.	00: 30min. 01: 60min. 10: 120min. 11: 240min.
ChgTmr*	1:0	Charger Safety Timer. Runs through all charging states.	00: 75min. 01: 150min. 10: 300min. 11: 600min.

ChgCfg0 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	–	ChgStepHyst*[2:0]			ChgStepRise*[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ChgStepHyst*	6:4	Charger Step-Charge Voltage Threshold Hysteresis.	000: 100mV. 001: 200mV. 010: 300mV. 011: 400mV. 100: 500mV. 101: 600mV. 110: Reserved (600mV). 111: Reserved (600mV).
ChgStepRise*	3:0	Charger Step-Charge Voltage Rising Threshold.	0000: 3.80V. 0001: 3.85V. 0010: 3.90V. 0011: 3.95V. 0100: 4.00V. 0101: 4.05V. 0110: 4.10V. 0111: 4.15V. 1000: 4.20V. 1001: 4.25V. 1010: 4.30V. 1011: 4.35V. 1100: 4.40V. 1101: 4.45V. 1110: 4.50V. 1111: 4.55V.

ThmCfg0 (0x1E)

BIT	7	6	5	4	3	2	1	0

Field	ChgCoolCC1IFChg*[2:0]	ChgCoolBatReg*[1:0]	ChgCoolCC2IFChg*[2:0]
Reset	0b111	0b11	0b111
Access Type	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ChgCoolCC1IFChg*	7:5	Charger Cool-Zone Fast-Charge Current Reduction. Sets the modified fast-charge current when the cool temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG}. 001: 0.3 x I_{FCHG}. 010: 0.4 x I_{FCHG}. 011: 0.5 x I_{FCHG}. 100: 0.6 x I_{FCHG}. 101: 0.7 x I_{FCHG}. 110: 0.8 x I_{FCHG}. 111: 1.0 x I_{FCHG}.
ChgCoolBatReg*	4:3	Charger Cool-Zone Battery Regulation Voltage Reduction. Sets the modified battery regulation voltage when the cool temperature zone is entered according to thermistor monitoring.	00: ChgBatReg[5:0] - 150mV. 01: ChgBatReg[5:0] - 100mV. 10: ChgBatReg[5:0] - 50mV. 11: ChgBatReg[5:0].
ChgCoolCC2IFChg*	2:0	Charger Cool-Zone Fast-Charge Current Reduction. Sets the modified fast-charge current when the cool temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG}. 001: 0.3 x I_{FCHG}. 010: 0.4 x I_{FCHG}. 011: 0.5 x I_{FCHG}. 100: 0.6 x I_{FCHG}. 101: 0.7 x I_{FCHG}. 110: 0.8 x I_{FCHG}. 111: 1.0 x I_{FCHG}.

ThmCfg1 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	ChgRoomCC1IFChg*[2:0]			ChgRoomBatReg*[1:0]		ChgRoomCC2IFChg*[2:0]		
Reset	0b111			0b11		0b111		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgRoomCC1IFChg*	7:5	Charger Room-Zone Fast-Charge Current Reduction. Sets the modified fast-charge current when the room temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG}. 001: 0.3 x I_{FCHG}. 010: 0.4 x I_{FCHG}. 011: 0.5 x I_{FCHG}. 100: 0.6 x I_{FCHG}. 101: 0.7 x I_{FCHG}. 110: 0.8 x I_{FCHG}. 111: 1.0 x I_{FCHG}.
ChgRoomBatReg*	4:3	Charger Room-Zone Battery Regulation Voltage Reduction. Sets the modified battery regulation voltage when the room temperature zone is entered according to thermistor monitoring.	00: ChgBatReg[5:0] - 150mV. 01: ChgBatReg[5:0] - 100mV. 10: ChgBatReg[5:0] - 50mV. 11: ChgBatReg[5:0].

BITFIELD	BITS	DESCRIPTION	DECODE
ChgRoomCC2IFChg*	2:0	Charger Room-Zone Fast-Charge Current Reduction. Sets the modified fast-charge current when the room temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG}. 001: 0.3 x I_{FCHG}. 010: 0.4 x I_{FCHG}. 011: 0.5 x I_{FCHG}. 100: 0.6 x I_{FCHG}. 101: 0.7 x I_{FCHG}. 110: 0.8 x I_{FCHG}. 111: 1.0 x I_{FCHG}.

ThmCfg2 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	ChgWarmCC1IFChg*[2:0]			ChgWarmBatReg*[1:0]		ChgWarmCC2IFChg*[2:0]		
Reset	0b111			0b11		0b111		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgWarmCC1IFChg*	7:5	Charger Warm-Zone Fast-Charge Current Reduction. Sets the modified fast-charge current when the warm temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG}. 001: 0.3 x I_{FCHG}. 010: 0.4 x I_{FCHG}. 011: 0.5 x I_{FCHG}. 100: 0.6 x I_{FCHG}. 101: 0.7 x I_{FCHG}. 110: 0.8 x I_{FCHG}. 111: 1.0 x I_{FCHG}.
ChgWarmBatReg*	4:3	Charger Warm-Zone Battery Regulation Voltage Reduction. Sets the modified battery regulation voltage when the Warmtemperature zone is entered according to thermistor monitoring.	00: ChgBatReg[5:0] - 150mV. 01: ChgBatReg[5:0] - 100mV. 10: ChgBatReg[5:0] - 50mV. 11: ChgBatReg[5:0].
ChgWarmCC2IFChg*	2:0	Charger Warm-Zone Fast-Charge Current Reduction. Sets the modified fast-charge current when the warm temperature zone is entered according to thermistor monitoring.	000: 0.2 x I_{FCHG}. 001: 0.3 x I_{FCHG}. 010: 0.4 x I_{FCHG}. 011: 0.5 x I_{FCHG}. 100: 0.6 x I_{FCHG}. 101: 0.7 x I_{FCHG}. 110: 0.8 x I_{FCHG}. 111: 1.0 x I_{FCHG}.

ThmCfg3 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT1ThrDef*[2:0]			ChgT1ThrCC1*[2:0]		
Reset	–	–	0b111			0b111		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT1ThrDef*	5:3	JEITA T1 Default Setting.	000: -20°C. 001: -15°C. 010: -10°C. 011: -5°C. 100: 0°C. 101: +5°C. 110: +10°C. 111: +15°C.
ChgT1ThrCC1*	2:0	JEITA T1 CC1 Setting.	000: -20°C. 001: -15°C. 010: -10°C. 011: -5°C. 100: 0°C. 101: +5°C. 110: +10°C. 111: +15°C.

ThmCfg4 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT2ThrDef*[2:0]			ChgT2ThrCC1*[2:0]		
Reset	–	–	0b111			0b111		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT2ThrDef*	5:3	JEITA T2 Default Setting.	000: -10°C. 001: -5°C. 010: 0°C. 011: +5°C. 100: +10°C. 101: +15C. 110: +20°C. 111: +25°C.
ChgT2ThrCC1*	2:0	JEITA T2 CC1 Setting.	000: -10°C. 001: -5°C. 010: 0°C. 011: +5°C. 100: +10°C. 101: +15°C. 110: +20°C. 111: +25°C.

ThmCfg5 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT3ThrDef*[2:0]			ChgT3ThrCC1*[2:0]		
Reset	–	–	0b111			0b111		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT3ThrDef*	5:3	JEITA T3 Default Setting.	000: +20°C. 001: +25°C. 010: +30°C. 011: +35°C. 100: +40°C. 101: +45°C. 110: +50°C. 111: +55°C.
ChgT3ThrCC1*	2:0	JEITA T3 CC1 Setting.	000: +20°C. 001: +25°C. 010: +30°C. 011: +35°C. 100: +40°C. 101: +45°C. 110: +50°C. 111: +55°C.

ThmCfg6 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ChgT4ThrDef*[2:0]			ChgT4ThrCC1*[2:0]		
Reset	–	–	0b111			0b111		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgT4ThrDef*	5:3	JEITA T4 Default Setting.	000: +35°C. 001: +40°C. 010: +45°C. 011: +50°C. 100: +55°C. 101: +60°C. 110: +65°C. 111: +70°C.
ChgT4ThrCC1*	2:0	JEITA T4 CC1 Setting.	000: +35°C. 001: +40°C. 010: +45°C. 011: +50°C. 100: +55°C. 101: +60°C. 110: +65°C. 111: +70°C.

ThmCfg7 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	ChgThrmLim*[3:0]				ThmPUSel*	ThmEn*[2:0]		
Reset	0x0				0b0	0b000		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ChgThrmLim*	7:4	Setting of the Thermal Threshold.	0x0: +40°C. 0x1: +45°C. 0x2: +50°C. 0x3: +55°C. 0x4: +60°C. 0x5: +65°C. 0x6: +70°C. 0x7: +75°C. 0x8: +80°C. 0x9: +85°C. 0xA: +90°C. 0xB: +95°C. 0xC: +100°C. 0xD: +105°C. 0xE: +110°C. 0xF: +115°C.
ThmPUSel*	3	THM Internal Pull-Up Selection.	0: 10kΩ THM pull-up. 1: 100kΩ THM pull-up.
ThmEn*	2:0	Charger Thermistor Monitoring Related Control. Valid only when CHGIN input voltage is present.	000: Thermistor monitoring disabled. 001: Thermistor monitoring enabled when CHGIN is present. Because of JEITA, battery is charged only in the cool and room temperature zones. 010: Thermistor monitoring enabled when CHGIN is present. Because of JEITA, battery is charged only in the room and warm temperature zones. 011: Thermistor monitoring enabled when CHGIN is present. Because of JEITA, battery is charged only in the cool, room, and warm temperature zones. 100: Thermistor monitoring disabled. 101: Thermistor monitoring enabled, but charger not affected by JEITA. 110: Thermistor monitoring enabled, but charger not affected by JEITA. 111: Thermistor monitoring enabled, but charger not affected by JEITA.

ChgCtr1 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	ChgFresh*	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ChgFresh*	7	Charge Due to VBAT Less Than Recharge Voltage Threshold Control.	0: When CHGIN is inserted, if BAT voltage is greater than V_{BAT_RECHG} recharge threshold, the device stays in idle state. 1: When CHGIN is inserted, the device goes to charger boot state.

ChgCtr2 (0x27)

BIT	7	6	5	4	3	2	1	0

Field	–	BattPullDown*	FrcPChg*	–	–	–	–	–
Reset	–	0b0	0b0	–	–	–	–	–
Access Type	–	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BattPullDown*	6	Pull-Down Resistor Enable on BAT. To probe for battery presence, connect this pull-down to discharge capacitance on the node in case a battery is not present, then check Batuvlob. If BatUvlob is 0, then either no battery is present or the pack protector is open. At this point, forced precharge can be enabled by FrcPchg and the voltage of the battery node can be checked by ChgVoltMode. If ChgVoltMode = 1, then the battery is not present as the capacitor has been quickly charged. If ChgVoltMode = 1, then likely a battery is present but with its pack protector open. Note that if the SysBatLim status is 1, then this bit is not reliable because the limiter is not allowing the charger to force any current into the BAT node.	0: Pull-down resistor disabled. 1: Pull-down resistor enabled.
FrcPChg*	5	Charger Forced Precharge Mode. Valid only if ChgEn = 1. To be used with pack protector detection described in BatPullDown register description.	0: Charger operating normally. 1: Charger current is forced to precharge value.

HrvBatCfg0 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	HrvModCfg*[1:0]		HrvThmEn*[1:0]		–	–	HrvThmDio*	HrvFreeMPC
Reset	0b00		0b00		–	–	0b0	0b0
Access Type	Write, Read		Write, Read		–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HrvModCfg*	7:6	Harvester CHGOUT-SYS FET Control. Valid when CHGIN input voltage is not present and interaction with harvester is enabled when HrvEn = 1. If HrvEn = 0 and CHGIN input voltage is not present, the CHGOUT-SYS FET is fully on (direct-path). If CHGIN input voltage is present, the CHGOUT-SYS FET is controlled by the charger.	00: Direct-path (CHGOUT-SYS FET fully on) forced active. 01: Direct-path active if V_{CHGOUT} < ChgBatReg[5:0] and ideal CHGOUT-to-SYS diode active if V_{CHGOUT} > ChgBatReg[5:0]. Once ideal diode has been activated, a hysteresis equal to BatReChg[1:0] is applied on ChgBatReg[5:0] threshold. 10: Ideal CHGOUT-to-SYS diode (CHGOUT-SYS FET controlled to allow current flowing from CHGOUT to SYS with a low drop and to not allow current flowing from SYS to CHGOUT) forced active. 11: Reserved.

BITFIELD	BITS	DESCRIPTION	DECODE
HrvThmEn*	5:4	Periodic Thermistor Monitoring Related Control. Valid when CHGIN input voltage is not present and interaction with harvester is enabled when HrvEn = 1. If HrvThmEn[1:0] is different from 00, thermistor (V_{THM}) is periodically monitored by exploiting fuel gauge periodic measurements timing.	00: Periodic thermistor monitoring disabled. 01: Periodic thermistor monitoring enabled and harvester charging enabled in the cool and room temperature zones. 10: Periodic thermistor monitoring enabled and harvester charging enabled in the room and warm temperature zones. 11: Periodic thermistor monitoring enabled and harvester charging enabled in the cool, room, and warm temperature zones.
HrvThmDio*	1	Harvester Charging Disabled Condition Control. Valid when CHGIN input voltage is not present, interaction with harvester is enabled by HrvEn = 1, HrvThmEn[1:0] is different from 00 and the temperature is in a zone where charging from harvester is inhibited. If HrvEn = 1 and CHGIN input voltage is present, the harvester is permanently disabled through the MPC6 output.	0: Harvester is disabled through the MPC6 output and the CHGOUT-SYS FET is controlled through HrvModCfg[1:0]. 1: Harvester is not disabled through the MPC6 output and ideal CHGOUT-to-SYS diode is forced active regardless of HrvModCfg[1:0].
HrvFreeMPC	0	When the harvester mode OTP is enabled, the MPC6 and MPC7 pins are captive to the harvester function.	0: MPC6 and MPC7 are used for disable output and wake input for interaction with harvester. 1: MPC6 and MPC7 can be used with other setting.

MONCfg (0x29)

BIT	7	6	5	4	3	2	1	0
Field	–	MONRatioCfg[1:0]		MONHiZ	MONCtr[3:0]			
Reset	–	0b00		0b1	0x0			
Access Type	–	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MONRatioCfg	6:5	IVMON Multiplexer Resistive Partition Selector.	00: 1:1. 01: 2:1. 10: 3:1. 11: 4:1.
MONHiZ	4	IVMON Multiplexer Disabled Condition. Valid when IVMONCntl = 0000.	0: IVMON is pulled low by a 59kΩ (typ) resistor. 1: IVMON is high-impedance.
MONCtr	3:0	IVMON Multiplexer Input Channel Selector.	0000: IVMON multiplexer disabled; high-impedance. 0001: Charger current. 0010: BAT. 0011: SYS. 0100: BK1OUT. 0101: BK2OUT. 0110: BK3OUT. 0111: L1OUT. 1000: L2OUT. 1001: L3OUT. 1010: BBOUT. 1011: THM. 1100: GND. 1101: RTC_LDO.

BITFIELD	BITS	DESCRIPTION	DECODE
			1110: GND. 1111: Reserved.

WDCntl (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	WDRstType[1:0]		WDTmrSel[1:0]	
Reset	–	–	–	–	0b00		0b00	
Access Type	–	–	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WDRstType	3:2	Watchdog Reset Type.	00: Watchdog is off. 01: Charger and limiter registers reset. 11: Soft reset. 11: Hard reset.
WDTmrSel	1:0	Select Watchdog Timer Interval. Set WDRstType = 0 before changing WDTmrSel. After reset or upon activation, the first watchdog timer expiration event is ignored, effectively doubling the time of the first interval.	00: 4s. 01: 8s. 10: 16s. 11: 32s.

Buck1Ena (0x30)

BIT	7	6	5	4	3	2	1	0
Field	Buck1Seq[2:0]			–	–	–	Buck1En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1Seq	7:5	Buck1 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by Buck1En[1:0] after 100% of boot/POR process delay control.
Buck1En	1:0	Buck1 Enable Configuration. (Effective only when Buck1Seq = 111.)	00: Disabled: BK1OUT not actively discharged unless hard-reset/shutdown/off mode. 01: Enabled. 10: Controlled by MPC_ (see the Buck1MPC_ bits). 11: Reserved.

Buck1Cfg0 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	Buck1EnbINTGR	Buck1PGOODena	Buck1Fast	Buck1PsvDsc	Buck1ActDsc	Buck1LowEMI	Buck1FET	Buck1EnLxSns
Reset	0b0	0b1	0b0	0b1	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1EnbINTGR	7	Buck1 Integrator Feedback Disable.	0: Integrator enabled. 1: Integrator disabled—proportional control only.
Buck1PGOODena	6	Buck1 PGOOD Comparator Control.	0: PGOOD comparator disabled during voltage transition after startup. 1: PGOOD comparator enabled during voltage transition after startup.
Buck1Fast	5	Buck1 Pretrigger Mode Setting.	0: Normal, low quiescent current operation. 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30µA.
Buck1PsvDsc	4	Buck1 Passive Discharge Control.	0: Buck1 passively discharged only in hard reset. 1: Buck1 passively discharged in hard reset or enable low.
Buck1ActDsc	3	Buck1 Active Discharge Control.	0: Buck1 actively discharged only in hard reset. 1: Buck1 actively discharged in hard reset or enable low.
Buck1LowEMI	2	Buck1 Low EMI Mode.	0: Normal operation. 1: Slow rise/fall edges on BK1LX by 3x.
Buck1FET	1	Buck1 Force FET Scaling. Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).	0: FET scaling disabled. 1: FET scaling enabled.
Buck1EnLxSns	0	Buck1 LX Sense Control. Selects the condition to turn on freewheeling FET. Keep it to 0 for Buck1Vset ≤ 1.6V.	0: Enter freewheeling mode after inductor current zero-crossing 1: Enter freewheeling mode on V_{LX} high detection after inductor current zero-crossing

Buck1Cfg1 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	Buck1LowBW	Buck1FrcDCM	Buck1MPCFast	Buck1FPWM	Buck1EnbIADPT	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1LowBW	7	Buck1 Low Bandwidth Mode. This mode reduces the amount of capacitance required to minimize jitter when transitioning from DCM to CCM. If this	0: High bandwidth mode. 1: Low bandwidth mode.

BITFIELD	BITS	DESCRIPTION	DECODE
		bit is enabled, the output capacitance requirement is cut in half.	
Buck1FrcDCM	6	Buck1 Forced Discontinuous Conduction Mode (DCM). Improves light load efficiency at the expense of load regulation error at higher loads. This should only be used if the expected maximum load is less than 50mA.	0: Normal operation. 1: Forced DCM operation.
Buck1MPCFast	5	Buck1 Fast Mode by MPC2 Control.	0: Buck1 fast mode control by MPC2 disabled. 1: Buck1 fast mode control by MPC2 enabled.
Buck1FPWM	4	Buck1 Forced PWM Mode Control.	0: Normal operation. 1: Forced PWM mode enabled.
Buck1EnbIADPT	3	Buck1 Adaptive Peak Current Mode Control.	0: Adaptive peak current mode enabled. 1: Peak current fixed at value set in Buck1ISet.

Buck1Iset (0x33)

BIT	7	6	5	4	3	2	1	0
Field	Buck1ISetLookUpb	–	–	–	Buck1ISet[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1ISetLookUpb	7	Buck1 Peak Current Set by Lookup Table Disable.	0: Inductor current setting is set according to look-up table. 1: Inductor current setting is set by Buck1ISet.
Buck1ISet	3:0	Buck1 Inductor Peak Current Setting. Valid only if Buck1ISetLookUpDis is high. For the best efficiency, use between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}.	0000: 0mA. 0001: 25mA. 0010: 50mA. 0011: 75mA. 0100: 100mA. 0101: 125mA. 0110: 150mA. 0111: 175mA. 1000: 200mA. 1001: 225mA. 1010: 250mA. 1011: 275mA. 1100: 300mA. 1101: 325mA. 1110: 350mA. 1111: 375mA.

Buck1VSet (0x34)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1Vset[5:0]					
Reset	–	–	0b000000					

Access Type	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
Buck1Vset	5:0	Buck1 Output Voltage Setting. 0.50V to (63 x Buck1VStep), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.50V. 000001 = 0.51V. … 111111 = 1.13V.

Buck1Ctr (0x35)

BIT	7	6	5	4	3	2	1	0
Field	Buck1MPC7	Buck1MPC6	Buck1MPC5	Buck1MPC4	Buck1MPC3	Buck1MPC2	Buck1MPC1	Buck1MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1MPC7	7	Buck1 MPC7 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC7. 1: Buck1 controlled by MPC7.
Buck1MPC6	6	Buck1 MPC6 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC6. 1: Buck1 controlled by MPC6.
Buck1MPC5	5	Buck1 MPC5 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC5. 1: Buck1 controlled by MPC5.
Buck1MPC4	4	Buck1 MPC4 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC4. 1: Buck1 controlled by MPC4.
Buck1MPC3	3	Buck1 MPC3 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC3. 1: Buck1 controlled by MPC3.
Buck1MPC2	2	Buck1 MPC2 Enable Control. Only valid when Buck1Seq = 111 and Buck1En =	0: Buck1 not controlled by MPC2. 1: Buck1 controlled by MPC2.

BITFIELD	BITS	DESCRIPTION	DECODE
		10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs	
Buck1MPC1	1	Buck1 MPC1 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC1. 1: Buck1 controlled by MPC1.
Buck1MPC0	0	Buck1 MPC0 Enable Control. Only valid when Buck1Seq = 111 and Buck1En = 10. If mutliple MPCs are selected, Buck1 is controlled by the logical OR of the MPCs.	0: Buck1 not controlled by MPC0. 1: Buck1 controlled by MPC0.

Buck1DvsCfg0 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	Buck1DvsCur	–	Buck1DvsIpMax	Buck1DvsCfg[4:0]				
Reset	0b0	–	0b1	0b00000				
Access Type	Write, Read	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
Buck1DvsCur	7	Buck1 DVS Valley Current Selection.	0: 500mA valley current during DVS transition. 1: 1000mA valley current during DVS transition.
Buck1DvsIpMax	5	Buck1 DVS Iset Peak Current Control.	0: IP unchanged during DVS. 1: IP max during DVS.
Buck1DvsCfg	4:0		00000: DVS modes disabled. 00001: MPC0/MPC1. 00010: MPC0/MPC2. 00011: MPC0/MPC3. 00100: MPC0/MPC4. 00101: MPC0/MPC5. 00110: MPC0/MPC6. 00111: MPC0/MPC7. 01000: MPC1/MPC2. 01001: MPC1/MPC3. 01010: MPC1/MPC4. 01011: MPC1/MPC5. 01100: MPC1/MPC6. 01101: MPC1/MPC7. 01110: MPC2/MPC3. 01111: MPC2/MPC4. 10000: MPC2/MPC5. 10001: MPC2/MPC6. 10010: MPC2/MPC7. 10011: MPC3/MPC4. 10100: MPC3/MPC5. 10101: MPC3/MPC6. 10110: MPC3/MPC7. 10111: MPC4/MPC5. 11000: MPC4/MPC6. 11001: MPC4/MPC7. 11010: MPC5/MPC6. 11011: MPC5/MPC7. 11100: MPC6/MPC7.

BITFIELD	BITS	DESCRIPTION	DECODE
			11101: SPI mode. >11101: Reserved.

Buck1DvsCfg1 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DvsVlt0[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DvsVlt0	5:0	Buck1 Alternate Output-Voltage Setting 0 (Controlling MPCs = 00). 0.50V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.50V. 000001 = 0.51V. … 111111 = 1.13V.

Buck1DvsCfg2 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DvsVlt1[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DvsVlt1	5:0	Buck1 Alternate Output-Voltage Setting 1 (Controlling MPCs = 01). 0.50V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.50V. 000001 = 0.51V. … 111111 = 1.13V.

Buck1DvsCfg3 (0x39)

BIT	7	6	5	4	3	2	1	0

Field	–	–	Buck1DvsVlt2[5:0]
Reset	–	–	0b000000
Access Type	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
Buck1DvsVlt2	5:0	Buck1 Alternate Output Voltage Setting 2 (Controlling MPCs = 10). 0.50V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.50V. 000001 = 0.51V. … 111111 = 1.13V.

Buck1DvsCfg4 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1DvsVlt3[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck1DvsVlt3	5:0	Buck1 Alternate Output Voltage Setting 3 (Controlling MPCs = 11). 0.50V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.50V. 000001 = 0.51V. … 111111 = 1.13V.

Buck1DvsSpi (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck1SpiVlt[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck1SpiVlt	5:0	Buck1 SPI DVS Readback. 0.50V to (63 x Bk1Step), linear scale, increments of Bk1Step. e.g., for Bk1Step = 10mV: 000000 = 0.50V. 000001 = 0.51V. … 111111 = 1.13V.

Buck2Ena (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	Buck2Seq[2:0]			–	–	–	Buck2En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2Seq	7:5	Buck2 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by Buck2En[1:0] after 100% of boot/POR process delay control.
Buck2En	1:0	Buck2 Enable Configuration. (Effective only when Buck2Seq = 111.)	00: Disabled: BK2OUT not actively discharged unless hard reset/shutdown/off mode. 01: Enabled. 10: Controlled by MPC_ (see the Buck2MPC_ bits). 11: Reserved.

Buck2Cfg (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	Buck2EnbINTGR	Buck2PGOODena	Buck2Fast	Buck2PsvDsc	Buck2ActDsc	Buck2LowEMI	Buck2FET	Buck2EnLxSns
Reset	0b0	0b1	0b0	0b1	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2EnbINTGR	7	Buck2 Integrator Feedback Disable.	0: Integrator enabled. 1: Integrator disabled—proportional control only.
Buck2PGOODena	6	Buck2 PGOOD Comparator Control.	0: PGOOD comparator disabled during voltage transition after start-up.

BITFIELD	BITS	DESCRIPTION	DECODE
			1: PGOOD comparator enabled during voltage transition after start-up.
Buck2Fast	5	Buck2 Pretrigger Mode Setting.	0: Normal, low quiescent current operation. 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30µA.
Buck2PsvDsc	4	Buck2 Passive Discharge Control.	0: Buck2 passively discharged only in hard reset. 1: Buck2 passively discharged in hard reset or enable low.
Buck2ActDsc	3	Buck2 Active Discharge Control.	0: Buck2 actively discharged only in hard reset. 1: Buck2 actively discharged in hard reset or enable low.
Buck2LowEMI	2	Buck2 Low EMI Mode.	0: Normal operation. 1: Slow rise/fall edges on BK2LX by 3x.
Buck2FET	1	Buck2 FET Scaling Control. Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).	0: FET scaling disabled. 1: FET scaling enabled.
Buck2EnLxSns	0	Buck2 LX Sense Control. Selects the condition to turn on freewheeling FET. Keep it to 0 for Buck2Vset ≤ 1.6V.	0: Enter freewheeling mode after inductor current zero-crossing 1: Enter freewheeling mode on V_{LX} high detection after inductor current zero-crossing

Buck2Cfg1 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	Buck2LowBW	Buck2FrcDCM	Buck2MPCFast	Buck2FPWM	Buck2EnbIADPT	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2LowBW	7	Buck2 Low Bandwidth Mode. This mode reduces the amount of capacitance required to minimize jitter when transitioning from DCM to CCM. If this bit is enabled, the output capacitance requirement is cut in half.	0: High bandwidth mode. 1: Low bandwidth mode.
Buck2FrcDCM	6	Buck2 Forced Discontinuous Conduction Mode (DCM). Improves light load efficiency at the expense of load regulation error at higher loads. This should only be used if the expected maximum load is less than 50mA.	0: Normal operation. 1: Forced DCM operation.
Buck2MPCFast	5	Buck2 Fast Mode by MPC3 Control.	0: Buck2 fast mode control by MPC3 disabled. 1: Buck2 fast mode control by MPC3 enabled.
Buck2FPWM	4	Buck2 Forced PWM Mode Control.	0: Normal operation. 1: Forced PWM mode enabled.
Buck2EnbIADPT	3	Buck2 Adaptive Peak Current Mode Control.	0: Adaptive peak current mode enabled. 1: Peak current fixed at value set in Buck2ISet.

Buck2Iset (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	Buck2ISetLookUpb	–	–	–	Buck2ISet[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2ISetLookUpb	7	Buck2 Peak Current Set by Look-Up Table Disabled.	0: Inductor current setting is set according to look-up table. 1: Inductor current setting is set by Buck2ISet.
Buck2ISet	3:0	Buck2 Inductor Peak Current Setting. Valid only if Buck2ISetLookUpDis is high. For the best efficiency, use between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}.	0000: 0mA. 0001: 25mA. 0010: 50mA. 0011: 75mA. 0100: 100mA. 0101: 125mA. 0110: 150mA. 0111: 175mA. 1000: 200mA. 1001: 225mA. 1010: 250mA. 1011: 275mA. 1100: 300mA. 1101: 325mA. 1110: 350mA. 1111: 375mA.

Buck2VSet (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2Vset[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2Vset	5:0	Buck2 Output-Voltage Setting. 0.50V to (63 x Buck2VStep), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.50V. 000001 = 0.525V. … 111111 = 2.075V.

Buck2Ctr (0x41)

BIT	7	6	5	4	3	2	1	0
Field	Buck2MPC7	Buck2MPC6	Buck2MPC5	Buck2MPC4	Buck2MPC3	Buck2MPC2	Buck2MPC1	Buck2MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2MPC7	7	Buck2 MPC7 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC7. 1: Buck2 controlled by MPC7.
Buck2MPC6	6	Buck2 MPC6 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC6. 1: Buck2 controlled by MPC6.
Buck2MPC5	5	Buck2 MPC5 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC5. 1: Buck2 controlled by MPC5.
Buck2MPC4	4	Buck2 MPC4 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC4. 1: Buck2 controlled by MPC4.
Buck2MPC3	3	Buck2 MPC3 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs	0: Buck2 not controlled by MPC3. 1: Buck2 controlled by MPC3.
Buck2MPC2	2	Buck2 MPC2 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC2. 1: Buck2 controlled by MPC2.
Buck2MPC1	1	Buck2 MPC1 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC1. 1: Buck2 controlled by MPC1.
Buck2MPC0	0	Buck2 MPC0 Enable Control. Only valid when Buck2Seq = 111 and Buck2En = 10. If multiple MPCs are selected, Buck2 is controlled by the logical OR of the MPCs.	0: Buck2 not controlled by MPC0. 1: Buck2 controlled by MPC0.

Buck2DvsCfg0 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	Buck2DvsCur	–	Buck2DvsIpMax	Buck2DvsCfg[4:0]				
Reset	0b0	–	0b1	0b00000				
Access Type	Write, Read	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
Buck2DvsCur	7	Buck2 DVS Valley Current Selection.	0: 500mA valley current during DVS transition. 1: 1000mA valley current during DVS transition.
Buck2DvsIpMax	5	Buck2 DVS Iset Peak Current Control.	0: IP unchanged during DVS. 1: IP max during DVS.
Buck2DvsCfg	4:0		00000: DVS modes disabled. 00001: MPC0/MPC1. 00010: MPC0/MPC2. 00011: MPC0/MPC3. 00100: MPC0/MPC4. 00101: MPC0/MPC5. 00110: MPC0/MPC6. 00111: MPC0/MPC7. 01000: MPC1/MPC2. 01001: MPC1/MPC3. 01010: MPC1/MPC4. 01011: MPC1/MPC5. 01100: MPC1/MPC6. 01101: MPC1/MPC7. 01110: MPC2/MPC3. 01111: MPC2/MPC4. 10000: MPC2/MPC5. 10001: MPC2/MPC6. 10010: MPC2/MPC7. 10011: MPC3/MPC4. 10100: MPC3/MPC5. 10101: MPC3/MPC6. 10110: MPC3/MPC7. 10111: MPC4/MPC5. 11000: MPC4/MPC6. 11001: MPC4/MPC7. 11010: MPC5/MPC6. 11011: MPC5/MPC7. 11100: MPC6/MPC7. 11101: SPI mode. > 11101: Reserved.

Buck2DvsCfg1 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt0[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt0	5:0	Buck2 Alternate Output-Voltage Setting 0 (Controlling MPCs = 00) 0.50V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.50V.. 000001 = 0.525V … 111111 = 2.075V.

Buck2DvsCfg2 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt1[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt1	5:0	Buck2 Alternate Output-Voltage Setting 1 (Controlling MPCs = 01) 0.50V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.50V. 000001 = 0.525V. … 111111 = 2.075V.

Buck2DvsCfg3 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt2[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt2	5:0	Buck2 Alternate Output Voltage Setting 2 (Controlling MPCs = 10) 0.50V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.50V. 000001 = 0.525V. … 111111 = 2.075V.

Buck2DvsCfg4 (0x46)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2DvsVlt3[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck2DvsVlt3	5:0	Buck2 Alternate Output Voltage Setting 3 (Controlling MPCs = 11) 0.50V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.50V. 000001 = 0.525V. … 111111 = 2.075V.

Buck2DvsSpi (0x47)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck2SpiVlt[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck2SpiVlt	5:0	Buck2 SPI DVS Readback. 0.50V to (63 x Bk2Step), linear scale, increments of Bk2Step. e.g., for Bk2Step = 25mV: 000000 = 0.50V. 000001 = 0.525V. … 111111 = 2.075V.

Buck3Ena (0x48)

BIT	7	6	5	4	3	2	1	0
Field	Buck3Seq[2:0]			–	–	–	Buck3En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3Seq	7:5	Buck3 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by Buck3En[1:0] after 100% of boot/POR process delay control.
Buck3En	1:0	Buck3 Enable Configuration. (Effective only when Buck3Seq = 111.)	00: Disabled: BK1OUT not actively discharged unless hard-reset/shutdown/off mode. 01: Enabled. 10: Controlled by MPC_ (see the Buck3MPC_ bits). 11: Reserved.

Buck3Cfg (0x49)

BIT	7	6	5	4	3	2	1	0
Field	Buck3EnbINTGR	Buck3PGOODena	Buck3Fast	Buck3PsvDsc	Buck3ActDsc	Buck3LowEMI	Buck3FET	Buck3EnLxSns
Reset	0b0	0b1	0b0	0b1	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3EnbINTGR	7	Buck3 Integrator Feedback Disable.	0: Integrator enabled. 1: Integrator disabled—proportional control only.
Buck3PGOODena	6	Buck3 PGOOD Comparator Control.	0: PGOOD comparator disabled during voltage transition after startup. 1: PGOOD comparator enabled during voltage transition after startup.
Buck3Fast	5	Buck3 Pretrigger Mode Setting.	0: Normal, low quiescent current operation. 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30µA.
Buck3PsvDsc	4	Buck3 Passive Discharge Control.	0: Buck3 passively discharged only in hard reset. 1: Buck3 passively discharged in hard reset or enable low.
Buck3ActDsc	3	Buck3 Active Discharge Control.	0: Buck3 actively discharged only in hard reset. 1: Buck3 actively discharged in hard reset or enable low.
Buck3LowEMI	2	Buck3 Low EMI Mode.	0: Normal operation. 1: Slow rise/fall edges on BK3LX by 3x.
Buck3FET	1	Buck3 Force FET Scaling. Reduce the FET size by a factor of two. Used to optimize the efficiency when Buck1ISet must be < 100mA (e.g., to mitigate noise at low frequencies).	0: FET scaling disabled. 1: FET scaling enabled.
Buck3EnLxSns	0	Buck3 LX Sense Control. Selects the condition to turn on freewheeling FET. Keep it to 0 for Buck3Vset ≤ 1.6V.	0: Enter freewheeling mode after inductor current zero-crossing. 1: Enter freewheeling mode on V_{LX} high detection after inductor current zero-crossing.

Buck3Cfg1 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	Buck3LowBW	Buck3FrcDCM	Buck3MPCFast	Buck3FPWM	Buck3EnbIADPT	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3LowBW	7	Buck3 Low Bandwidth Mode. This mode reduces the amount of capacitance required to minimize jitter when transitioning from DCM to CCM. If this bit is enabled, the output capacitance requirement is cut in half.	0: High bandwidth mode. 1: Low bandwidth mode.
Buck3FrcDCM	6	Buck3 Forced Discontinuous Conduction Mode (DCM). Improves light load efficiency at the expense of load regulation error at higher loads. This should only be used if the expected maximum load is less than 50mA.	0: Normal operation. 1: Forced DCM operation.
Buck3MPCFast	5	Buck3 Fast Mode by MPC4 Control.	0: Buck3 fast mode control by MPC4 disabled. 1: Buck3 fast mode control by MPC4 enabled.
Buck3FPWM	4	Buck3 Forced PWM Mode Control.	0: Normal operation. 1: Forced PWM mode enabled.
Buck3EnbIADPT	3	Buck3 Adaptive Peak Current Mode Control.	0: Adaptive peak current mode enabled. 1: Peak current fixed at value set in Buck3ISet.

Buck3Iset (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	Buck3ISetLookUpb	–	–	–	Buck3ISet[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3ISetLookUpb	7	Buck3 Peak Current Set by Look-Up Table Disabled.	0: Inductor current setting is set according to look-up table. 1: Inductor current setting is set by Buck3ISet.
Buck3ISet	3:0	Buck3 Inductor Peak Current Setting. Valid only if Buck3ISetLookUpDis is high. For the best efficiency, use between 150mA and 200mA. Linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}.	0000: 0mA. 0001: 25mA. 0010: 50mA. 0011: 75mA. 0100: 100mA. 0101: 125mA. 0110: 150mA. 0111: 175mA. 1000: 200mA. 1001: 225mA.

BITFIELD	BITS	DESCRIPTION	DECODE
			1010: 250mA. 1011: 275mA. 1100: 300mA. 1101: 325mA. 1110: 350mA. 1111: 375mA.

Buck3VSet (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3Vset[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3Vset	5:0	Buck3 Output Voltage Setting. 0.50V to (63 x Buck3VStep), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.50V. 000001 = 0.55V. … 111111 = 3.65V.

Buck3Ctr (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	Buck3MPC7	Buck3MPC6	Buck3MPC5	Buck3MPC4	Buck3MPC3	Buck3MPC2	Buck3MPC1	Buck3MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3MPC7	7	Buck3 MPC7 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC7. 1: Buck3 controlled by MPC7.
Buck3MPC6	6	Buck3 MPC6 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC6. 1: Buck3 controlled by MPC6.

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3MPC5	5	Buck3 MPC5 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC5. 1: Buck3 controlled by MPC5.
Buck3MPC4	4	Buck3 MPC4 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC4. 1: Buck3 controlled by MPC4.
Buck3MPC3	3	Buck3 MPC3 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC3. 1: Buck3 controlled by MPC3.
Buck3MPC2	2	Buck3 MPC2 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC2. 1: Buck3 controlled by MPC2.
Buck3MPC1	1	Buck3 MPC1 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC1. 1: Buck3 controlled by MPC1.
Buck3MPC0	0	Buck3 MPC0 Enable Control. Only valid when Buck3Seq = 111 and Buck3En = 10. If mutliple MPCs are selected, Buck3 is controlled by the logical OR of the MPCs.	0: Buck3 not controlled by MPC0. 1: Buck3 controlled by MPC0.

Buck3DvsCfg0 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	Buck3DvsCur	–	Buck3DvsIpMax	Buck3DvsCfg[4:0]				
Reset	0b0	–	0b1	0b00000				
Access Type	Write, Read	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
Buck3DvsCur	7	Buck3 DVS Valley Current Selection.	0: 500mA valley current during DVS transition. 1: 1000mA valley current during DVS transition.
Buck3DvsIpMax	5	Buck3 DVS Iset Peak Current Control.	0: IP unchanged during DVS. 1: IP max during DVS.
Buck3DvsCfg	4:0		00000: DVS modes disabled. 00001: MPC0/MPC1. 00010: MPC0/MPC2. 00011: MPC0/MPC3. 00100: MPC0/MPC4. 00101: MPC0/MPC5. 00110: MPC0/MPC6. 00111: MPC0/MPC7.

BITFIELD	BITS	DESCRIPTION	DECODE
			01000: MPC1/MPC2. 01001: MPC1/MPC3. 01010: MPC1/MPC4. 01011: MPC1/MPC5. 01100: MPC1/MPC6. 01101: MPC1/MPC7. 01110: MPC2/MPC3. 01111: MPC2/MPC4. 10000: MPC2/MPC5. 10001: MPC2/MPC6. 10010: MPC2/MPC7. 10011: MPC3/MPC4. 10100: MPC3/MPC5. 10101: MPC3/MPC6. 10110: MPC3/MPC7. 10111: MPC4/MPC5. 11000: MPC4/MPC6. 11001: MPC4/MPC7. 11010: MPC5/MPC6. 11011: MPC5/MPC7. 11100: MPC6/MPC7. 11101: SPI mode. >11101: Reserved.

Buck3DvsCfg1 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt0[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt0	5:0	Buck3 Alternate Output-Voltage Setting 0 (Controlling MPCs = 00). 0.50V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.50V. 000001 = 0.55V. … 111111 = 3.65V.

Buck3DvsCfg2 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt1[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt1	5:0	Buck3 Alternate Output Voltage Setting 1 (Controlling MPCs = 01). 0.50V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.50V. 000001 = 0.55V. … 111111 = 3.65V.

Buck3DvsCfg3 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt2[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt2	5:0	Buck3 Alternate Output Voltage Setting 2 (Controlling MPCs = 10). 0.50V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.50V. 000001 = 0.55V. … 111111 = 3.65V.

Buck3DvsCfg4 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3DvsVlt3[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
Buck3DvsVlt3	5:0	Buck3 Alternate Output Voltage Setting 3 (Controlling MPCs = 11). 0.50V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.50V. 000001 = 0.55V. … 111111 = 3.65V.

Buck3DvsSpi (0x53)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Buck3SpiVlt[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
Buck3SpiVlt	5:0	Buck3 SPI DVS Readback. 0.50V to (63 x Bk3Step), linear scale, increments of Bk3Step. e.g., for Bk3Step = 50mV: 000000 = 0.50V. 000001 = 0.55V. … 111111 = 3.65V.

BBstEna (0x54)

BIT	7	6	5	4	3	2	1	0
Field	BBstSeq[2:0]			–	–	–	BBstEn[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BBstSeq	7:5	Buck-Boost Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by BBstEn[1:0] after 100% of boot/POR process delay control.
BBstEn	1:0	Buck-Boost Enable Configuration. (Effective only when BBstSeq = 111.)	00: Disabled: BBOUT not actively discharged unless hard-reset/shutdown/off mode. 01: Enabled. 10: Controlled by MPC_ (see the BBstMPC_ bits). 11: Reserved.

BBstCfg (0x55)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPSetLookUpb	–	–	BBstLowEMI	BBstActDsc	BBstRampEna	BBstMode	BBstPsvDisc

Reset	0b0	–	–	0b0	0b0	0b1	0b0	0b1
Access Type	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIPSetLookUpb	7	Buck-Boost Peak Current Set by Look-Up Table Disable.	0: Inductor current setting is set according to look-up table. 1: Inductor current setting is set by BBstIPSet2 and BBstIPSet1.
BBstLowEMI	4	Buck-Boost Low EMI Mode.	0: Normal operation. 1: Slow rise/fall edges on HVLX/LVLX by 3x.
BBstActDsc	3	Buck-Boost Active Discharge Control.	0: Buck-boost actively discharged only in hard reset. 1: Buck-boost actively discharged in hard reset or enable low.
BBstRampEna	2	Buck-Boost Ramp Enable.	0: Voltage setting transition is performed without intermediate steps. 1: Voltage setting transition to a higher value is performed with incremental steps every 20µs.
BBstMode	1	Buck-Boost Operating Mode.	0: Buck-boost. 1: Buck only.
BBstPsvDisc	0	Buck-Boost Passive Discharge Control.	0: Buck-boost passively discharged only in hard reset. 1: Buck-boost passively discharged in hard reset or enable low.

BBstVSet (0x56)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BBstVSet[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
BBstVSet	5:0	Buck-Boost Output Voltage Setting. 2.5V to 5.5V, linear scale, 50mV increments, codes below 000010 can interfere with V_{BBOUT_UVLO} and are not guaranteed. 000000 = 2.5V. 000001 = 2.55V. … 111100 = 5.5V. > 111100 = Do not use.

BBstISet (0x57)

BIT	7	6	5	4	3	2	1	0
Field	BBstIPSet2[3:0]				BBstIPSet1[3:0]			

Reset	0x0	0x0
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIPSet2	7:4	Buck-Boost Nominal Maximum Peak Current Setting. Valid only if BBstISetLookUpDis is high. See the Buck-Boost Regulator section for a description of the peak current settings. 0mA to 375mA, linear scale, 25mA increments, settings below 75mA can be limited by the minimum t_{ON}. Recommended settings: V_{BBOUT} ≤ 2.65V: 250mA. 2.7V < V_{BBOUT} ≤ 3.05V: 225mA. 3.1V < V_{BBOUT} ≤ 3.6V: 200mA. 3.65V < V_{BBOUT} ≤ 4.35V: 175mA. V_{BBOUT} > 4.4V: 150mA.	0000: BBstIPSet1 + 0mA. 0001: BBstIPSet1 + 25mA. 0010: BBstIPSet1 + 50mA. 0011: BBstIPSet1 + 75mA. 0100: BBstIPSet1 + 100mA. 0101: BBstIPSet1 + 125mA. 0110: BBstIPSet1 + 150mA. 0111: BBstIPSet1 + 175mA. 1000: BBstIPSet1 + 200mA. 1001: BBstIPSet1 + 225mA. 1010: BBstIPSet1 + 250mA. 1011: BBstIPSet1 + 275mA. 1100: BBstIPSet1 + 300mA. 1101: BBstIPSet1 + 325mA. 1110: BBstIPSet1 + 350mA. 1111: BBstIPSet1 + 375mA.
BBstIPSet1	3:0	Buck-Boost Nominal Peak Current Setting. Valid only if BBstISetLookUpDis is high. Nominal peak current when charging inductor between V_{IN} and GND. See the Buck-Boost Regulator section for a description of the peak current settings. 0mA to 375mA, linear scale, 25mA increments, settings below 75mA may be limited by the minimum t_{ON}. Recommended settings: V_{BBOUT} ≤ 2.65V: 50mA. 2.7V < V_{BBOUT} ≤ 3.05V: 75mA. 3.1V < V_{BBOUT} ≤ 3.4V: 100mA. 3.45V < V_{BBOUT} ≤ 3.8V: 125mA. 3.85V < V_{BBOUT} ≤ 4.15V: 150mA. 4.2V < V_{BBOUT} ≤ 4.55V: 175mA. 4.6V < V_{BBOUT} ≤ 4.9V: 200mA. 4.95V < V_{BBOUT} ≤ 5.3V: 225mA. V_{BBOUT} > 5.35V: 250mA.	0000: 0mA. 0001: 25mA. 0010: 50mA. 0011: 75mA. 0100: 100mA. 0101: 125mA. 0110: 150mA. 0111: 175mA. 1000: 200mA. 1001: 225mA. 1010: 250mA. 1011: 275mA. 1100: 300mA. 1101: 325mA. 1110: 350mA. 1111: 375mA.

BBstCfg1 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	–	BBstIpPadPEnb	BBstFast	BBZCCmpEnB	BBstFFET	BBstMPC1FCT	BBFHighSh[1:0]	
Reset	–	0b0	0b0	0b1	0b0	0b0	0b00	
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BBstIpPadPEnb	6	Adaptive Peak/Valley Current Adjustment Enable.	0: Enabled. 1: Disabled, peak current fixed and is set by BBstIPSet1, 2. Valley current is fixed to 0mA.

BITFIELD	BITS	DESCRIPTION	DECODE
BBstFast	5	Buck-Boost Pretrigger Mode Setting.	0: Normal, low quiescent current operation. 1: Increased quiescent mode for fast load transient response. Quiescent current increased to 30µA.
BBZCCmpEnB	4	Buck-Boost Zero-Crossing Comparator Disable.	0: Enable. 1: Disable.
BBstFFET	3	Buck-Boost Force FET Scaling. Reduce the FET size by factor 2 to optimize the efficiency at light loads.	0: FET scaling disabled. 1: FET scaling enabled.
BBstMPC1FCT	2	Buck-Boost Fast Mode Enable by MPC1. Improves interoperability with the MAX86170/MAX86171. Tie MPC1 to INT2 on the MAX86170/MAX86171 if this mode is used.	0: Fast status controlled by BBstFast register. 1: Fast mode controlled by MPC1. MPC1 = 0: Fast disabled MPC1 = 1: Fast enabled, IQ increased by 30µA.
BBFHighSh	1:0	Buck-Boost f_{HIGH} Thresholds. Selects the switching frequency threshold f_{HIGH}. If $f_{SW} > f_{HIGH}$ all the blocks are kept on (I_Q is higher). A small glitch on V_{BBOUT} can be present at the f_{HIGH} crossover.	00: 25kHz/6.125kHz. 01: 35kHz/8.25kHz. 10: 50kHz/12.5kHz. 11: 100kHz/25kHz.

BBstCtr0 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	BBstMPC7	BBstMPC6	BBstMPC5	BBstMPC4	BBstMPC3	BBstMPC2	BBstMPC1	BBstMPC0
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BBstMPC7	7	Buck-Boost MPC7 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC7. 1: Buck-boost controlled by MPC7.
BBstMPC6	6	Buck-Boost MPC6 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC6. 1: Buck-boost controlled by MPC6.
BBstMPC5	5	Buck-Boost MPC5 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC5. 1: Buck-boost controlled by MPC5.
BBstMPC4	4	Buck-Boost MPC4 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC4. 1: Buck-boost controlled by MPC4.

BITFIELD	BITS	DESCRIPTION	DECODE
BBstMPC3	3	Buck-Boost MPC3 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC3. 1: Buck-boost controlled by MPC3.
BBstMPC2	2	Buck-Boost MPC2 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC2. 1: Buck-boost controlled by MPC2.
BBstMPC1	1	Buck-Boost MPC1 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC1. 1: Buck-boost controlled by MPC1.
BBstMPC0	0	Buck-Boost MPC0 Enable Control. Only valid when BBstSeq = 111 and BBstEn = 10. If multiple MPCs are selected, the buck-boost is controlled by the logical OR of the MPCs.	0: Buck-boost not controlled by MPC0. 1: Buck-boost controlled by MPC0.

LDO1Ena (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	LDO1Seq[2:0]			–	–	–	LDO1En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1Seq	7:5	LDO1 Enable Configuration.	000: Disabled. 001: Enabled always when BAT/SYS is present. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: 100 = Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LDO1En[1:0] after 100% of boot/POR process delay control.
LDO1En	1:0	LDO1 Enable Configuration. (Effective only when LDO1Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LDO1Ctr register 0x5D). 11: Reserved.

LDO1Cfg (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDO1IntSup	LDO1ActDsc	LDO1Mode	LDO1PsvDsc

Reset	–	–	–	–	0b0	0b0	0b0	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1IntSup	3	Always On LDO1 Internal Switchover Supply Control.	0: L1IN must be provided externally. 1: L1IN is internally connected to V_{CCINT} with a typ 15kΩ resistor. Bypass L1IN with 1µF.
LDO1ActDsc	2	LDO1 Active Discharge Control.	0: LDO1 output is actively discharged only in hard reset mode. 1: LDO1 output is actively discharged in hard reset mode and also when its enable goes low.
LDO1Mode	1	LDO1 Mode Control. When FET is on, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.	0: Normal LDO operating mode. 1: Load switch mode. FET is either fully on or off depending on state of LDO1En.
LDO1PsvDsc	0	LDO1 Passive Discharge Control.	0: LDO1 output is discharged only entering off and hard reset modes. 1: LDO1 output is discharged only entering off and hard-reset modes and when the enable is low.

LDO1VSet (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO1VSet[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
LDO1VSet	4:0	LDO1 Output Voltage Setting. Limited by input supply. 0.9V to 4.0V, linear scale, 100mV increments. 00000 = 0.9V. 00001 = 1.0V. … 11110 = 3.9V. 11111 = 4.0V.

LDO1Ctr (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	LDO1MPC7	LDO1MPC6	LDO1MPC5	LDO1MPC4	LDO1MPC3	LDO1MPC2	LDO1MPC1	LDO1MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1MPC7	7	LDO1 MPC7 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC7. 1: LDO1 controlled by MPC7.
LDO1MPC6	6	LDO1 MPC6 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC6. 1: LDO1 controlled by MPC6.
LDO1MPC5	5	LDO1 MPC5 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC5. 1: LDO1 controlled by MPC5.
LDO1MPC4	4	LDO1 MPC4 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC4. 1: LDO1 controlled by MPC4.
LDO1MPC3	3	LDO1 MPC3 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC3. 1: LDO1 controlled by MPC3.
LDO1MPC2	2	LDO1 MPC2 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC2. 1: LDO1 controlled by MPC2.
LDO1MPC1	1	LDO1 MPC1 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC1. 1: LDO1 controlled by MPC1.
LDO1MPC0	0	LDO1 MPC0 Enable Control. Only valid when LDO1Seq = 111 and LDO1En = 10. If multiple MPCs are selected, LDO1 is controlled by the logical OR of the MPCs.	0: LDO1 not controlled by MPC0. 1: LDO1 controlled by MPC0.

LDO2Ena (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	LDO2Seq[2:0]			–	–	–	LDO2En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2Seq	7:5	LDO2 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LDO2En[1:0] after 100% of boot/POR process delay control.
LDO2En	1:0	LDO2 Enable Configuration. (Effective only when LDO2Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LDO2Ctr register (0x61)). 11: Reserved.

LDO2Cfg (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO2_MPC0CNF	LDO2_MPC0CNT	LDO2ActDsc	LDO2Mode	LDO2PsvDsc
Reset	–	–	–	0b0	0b0	0b0	0b0	0b1
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2_MPC0CNF	4	MPC0 Configuration Bit.	0: MPC0 controls LDO/SW mode of LDO2 (MPC0 = 0 LDO mode, MPC0 = 1 SW mode). 1: MPC0 controls enabling of LDO2 (MPC0 = 0 disabled, MPC0 = 1 enabled in SW mode).
LDO2_MPC0CNT	3	LDO2 MPC0 Control Bit.	0: MPC0 has no effect on the LDO. 1: LDO2_MPC0CNF is valid and MPC0 function is enabled.
LDO2ActDsc	2	LDO2 active discharge control	0: LDO2 output is actively discharged only in hard-reset mode. 1: LDO2 output is actively discharged in hard-reset mode and also when its enable goes low.
LDO2Mode	1	LDO2 Mode Control. When FET is on, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.	0: Normal LDO operating mode 1: Load switch mode. FET is either fully On or Off depending on state of LDO2En.
LDO2PsvDsc	0	LDO2 Passive Discharge Control.	0: LDO2 output is passively discharged only in hard-reset mode. 1: LDO2 output is passively discharged in hard-reset mode and also when its enable goes low.

LDO2VSet (0x60)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO2VSet[4:0]				

Reset	–	–	–	0b00000
Access Type	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO2VSet	4:0	LDO2 Output-Voltage Setting. Limited by input supply. 0.9V to 4V, linear scale, 100mV increments. 00000 = 0.9V. 00001 = 1.0V. … 11110 = 3.9V. 11111 = 4.0V.

LDO2Ctr (0x61)

BIT	7	6	5	4	3	2	1	0
Field	LDO2MPC7	LDO2MPC6	LDO2MPC5	LDO2MPC4	LDO2MPC3	LDO2MPC2	LDO2MPC1	LDO2MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2MPC7	7	LDO2 MPC7 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC7. 1: LDO2 controlled by MPC7.
LDO2MPC6	6	LDO2 MPC6 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC6. 1: LDO2 controlled by MPC6.
LDO2MPC5	5	LDO2 MPC5 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC5. 1: LDO2 controlled by MPC5.
LDO2MPC4	4	LDO2 MPC4 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC4. 1: LDO2 controlled by MPC4.
LDO2MPC3	3	LDO2 MPC3 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC3. 1: LDO2 controlled by MPC3.

BITFIELD	BITS	DESCRIPTION	DECODE
LDO2MPC2	2	LDO2 MPC2 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC2. 1: LDO2 controlled by MPC2.
LDO2MPC1	1	LDO2 MPC1 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC1. 1: LDO2 controlled by MPC1.
LDO2MPC0	0	LDO2 MPC0 Enable Control. Only valid when LDO2Seq = 111 and LDO2En = 10. If multiple MPCs are selected, LDO2 is controlled by the logical OR of the MPCs.	0: LDO2 not controlled by MPC0. 1: LDO2 controlled by MPC0.

LDO3Ena (0x62)

BIT	7	6	5	4	3	2	1	0
Field	LDO3Seq[2:0]			–	–	–	LDO3En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LDO3Seq	7:5	LDO3 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LDO3En[1:0] after 100% of boot/POR process delay control.
LDO3En	1:0	LDO3 Enable Configuration. (Effective only when LDO3Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LDO3Ctr register 0x65). 11: Reserved.

LDO3Cfg (0x63)

BIT	7	6	5	4	3	2	1	0
Field	–	LDO3_MPC_CNF	LDO3_NOCLP	LDO3_HICOUT	LDO3_FRC_HIC	LDO3ActDsc	LDO3_PMOD	LDO3PsvDsc
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO3_MPC_CNF	6	MPC Configuration Bit.	0: MPC5 does not controls LDO3. 1: MPC5 controls the enabling of FRC_HIQ (MPC5 = 0 disabled, MPC5 = 1 enabled).
LDO3_NOCLP	5	LDO3 No Short-Circuit Protection Trigger On-Clipping	0: Short to GND sensitivity increased. 1: Short to GND robustness increased.
LDO3_HICOUT	4	COUT Selection.	0: Value to be set if C_{OUT} < 4uF. 1: Value to be set if C_{OUT} > 4uF.
LDO3_FRC_HIC	3	LDO3_FRC_HIQ	0: Low quiescent mode, slow response mode. 1: I_Q = ~3uA (typ) , fast response mode.
LDO3ActDsc	2	LDO3 Active Discharge Control.	0: LDO3 output is actively discharged only in hard-reset mode. 1: LDO3 output is actively discharged in hard-reset mode and also when its enable goes low.
LDO3_PMOD	1	LDO3 Proportional Regulation Mode Control.	Reserved. Set this bit to 0.
LDO3PsvDsc	0	LDO3 Passive Discharge Control.	0: LDO3 output is passively discharged only in hard-reset mode. 1: LDO3 output is passively discharged in hard-reset mode and also when its enable goes low.

LDO3VSet (0x64)

BIT	7	6	5	4	3	2	1	0
Field	–	LDO3VSet[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
LDO3VSet	6:0	LDO3 Output-Voltage Setting. Limited by input supply. 0.9V to 4.075V, linear scale, 25mV increments. 0000000 = 0.9V. 0000001 = 0.925V. … 1111110 = 4.05V. 1111111 = 4.075V.

LDO3Ctr (0x65)

BIT	7	6	5	4	3	2	1	0
Field	LDO3MPC7	LDO3MPC6	LDO3MPC5	LDO3MPC4	LDO3MPC3	LDO3MPC2	LDO3MPC1	LDO3MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO3MPC7	7	LDO3 MPC7 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC7. 1: LDO3 controlled by MPC7.
LDO3MPC6	6	LDO3 MPC6 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC6. 1: LDO3 controlled by MPC6.
LDO3MPC5	5	LDO3 MPC5 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC5. 1: LDO3 controlled by MPC5.
LDO3MPC4	4	LDO3 MPC4 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC4. 1: LDO3 controlled by MPC4.
LDO3MPC3	3	LDO3 MPC3 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC3. 1: LDO3 controlled by MPC3.
LDO3MPC2	2	LDO3 MPC2 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC2. 1: LDO3 controlled by MPC2.
LDO3MPC1	1	LDO3 MPC1 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC1. 1: LDO3 controlled by MPC1.
LDO3MPC0	0	LDO3 MPC0 Enable Control. Only valid when LDO3Seq = 111 and LDO3En = 10. If multiple MPCs are selected, LDO3 is controlled by the logical OR of the MPCs.	0: LDO3 not controlled by MPC0. 1: LDO3 controlled by MPC0.

LDO4Ena (0x66)

BIT	7	6	5	4	3	2	1	0
Field	LDO4Seq[2:0]			–	–	–	LDO4En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LDO4Seq	7:5	LDO4 Enable Configuration.	000: Disabled. 001: Enabled always when BAT/SYS is present. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LDO4En[1:0] after 100% of boot/POR process delay control.
LDO4En	1:0	LDO4 Enable Configuration. (Effective only when LDO4Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LDO4Ctr register 0x68). 11: Reserved.

LDO4Cfg (0x67)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LDO4VInc[1:0]		LDO4VSet	LDO4PsvDsc
Reset	–	–	–	–	0b00		0b0	0b1
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO4VInc	3:2	LDO4VInc Provides 25mV Voltage Increment for Each Bit. LDO4VInc = 00: 0mV voltage increment. LDO4VInc = 01: 25mV voltage increment. LDO4VInc =10: 50mV voltage increment. LDO4VInc = 11: 50mV voltage increment.	0x0: 0mV voltage increment. 0x1: 25mV voltage increment. 0x2: 50mV voltage increment. 0x3: 50mV voltage increment.
LDO4VSet	1	LDO4VSet = 0 Sets the Output to 1.2V; LDO4VSet = 1 Sets the Output to 1.8V.	0x0: 1.2V. 0x1: 1.8V.
LDO4PsvDsc	0	LDO4 Passive Discharge Control.	0: LDO4 output is passively discharged only in hard-reset mode. 1: LDO4 output is passively discharged in hard-reset mode and also when its enable goes low.

LDO4Ctr (0x68)

BIT	7	6	5	4	3	2	1	0
Field	LDO4MPC7	LDO4MPC6	LDO4MPC5	LDO4MPC4	LDO4MPC3	LDO4MPC2	LDO4MPC1	LDO4MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LDO4MPC7	7	LDO4 MPC7 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC7. 1: LDO4 controlled by MPC7.
LDO4MPC6	6	LDO4 MPC6 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC6. 1: LDO4 controlled by MPC6.
LDO4MPC5	5	LDO4 MPC5 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC5. 1: LDO4 controlled by MPC5.
LDO4MPC4	4	LDO4 MPC4 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC4. 1: LDO4 controlled by MPC4.
LDO4MPC3	3	LDO4 MPC3 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC3. 1: LDO4 controlled by MPC3.
LDO4MPC2	2	LDO4 MPC2 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC2. 1: LDO4 controlled by MPC2.
LDO4MPC1	1	LDO4 MPC1 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC1. 1: LDO4 controlled by MPC1.
LDO4MPC0	0	LDO4 MPC0 Enable Control. Only valid when LDO4Seq = 111 and LDO4En = 10. If multiple MPCs are selected, LDO4 is controlled by the logical OR of the MPCs.	0: LDO4 not controlled by MPC0. 1: LDO4 controlled by MPC0.

LSW1Ena (0x69)

BIT	7	6	5	4	3	2	1	0
Field	LSW1Seq[2:0]			–	–	–	LSW1En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1Seq	7:5	LSW1 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LSW1En[1:0] after 100% of boot/POR process delay control.
LSW1En	1:0	LSW1 Enable Configuration. (Effective only when LSW1Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LSW1MPC_ bits in register 0x6B). 11: Reserved.

LSW1Cfg (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LSW1ActDsc	LSW1LowIq	LSW1PsvDsc
Reset	–	–	–	–	–	0b0	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1ActDsc	2	LSW1 Active Discharge Control.	0: LSW1 output is actively discharged only in hard-reset mode. 1: LSW1 output is actively discharged in hard-reset mode and also when its enable goes low.
LSW1LowIq	1	LSW1 Low Quiescent Control. Low quiescent mode is achieved by disabling the voltage protection of LSW1.	0: Voltage protection enabled. If V_{SYS} - $V_{LSW1OUT}$ exceeds V_{LSW_PROT}, the output is disabled to protect from overcurrent. 1: Voltage protection disabled and quiescent is reduced.
LSW1PsvDsc	0	LSW1 Passive Discharge Control.	0: LSW1 output is discharged only entering off and hard-reset modes. 1: LSW1 output is discharged only entering off and hard-reset modes and when the enable is low.

LSW1Ctr (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	LSW1MPC7	LSW1MPC6	LSW1MPC5	LSW1MPC4	LSW1MPC3	LSW1MPC2	LSW1MPC1	LSW1MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW1MPC7	7	LSW1 MPC7 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC7. 1: LSW1 controlled by MPC7.
LSW1MPC6	6	LSW1 MPC6 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC6. 1: LSW1 controlled by MPC6.
LSW1MPC5	5	LSW1 MPC5 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC5. 1: LSW1 controlled by MPC5.
LSW1MPC4	4	LSW1 MPC4 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC4. 1: LSW1 controlled by MPC4.
LSW1MPC3	3	LSW1 MPC3 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC3. 1: LSW1 controlled by MPC3.
LSW1MPC2	2	LSW1 MPC2 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC2. 1: LSW1 controlled by MPC2.
LSW1MPC1	1	LSW1 MPC1 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC1. 1: LSW1 controlled by MPC1.
LSW1MPC0	0	LSW1 MPC0 Enable Control. Only valid when LSW1Seq = 111 and LSW1En = 10. If multiple MPCs are selected, LSW1 is controlled by the logical OR of the MPCs.	0: LSW1 not controlled by MPC0. 1: LSW1 controlled by MPC0.

LSW2Ena (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	LSW2Seq[2:0]			–	–	–	LSW2En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2Seq	7:5	LSW2 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LSW2En[1:0] after 100% of boot/POR process delay control.
LSW2En	1:0	LSW2 Enable Configuration. (Effective only when LSW2Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LSW2MPC_ bits in register 0x6E). 11: Reserved.

LSW2Cfg (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LSW2ActDsc	LSW2LowIq	LSW2PsvDsc
Reset	–	–	–	–	–	0b0	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2ActDsc	2	LSW2 Active Discharge Control.	0: LSW2 output is actively discharged only in hard-reset mode. 1: LSW2 output is actively discharged in hard-reset mode and also when its enable goes low.
LSW2LowIq	1	LSW2 Low Quiescent Control. Low quiescent mode is achieved by disabling the voltage protection of LSW2.	0: Voltage protection enabled. If V_{SYS} - $V_{LSW2OUT}$ exceeds V_{LSW_PROT}, the output is disabled to protect from overcurrent. 1: Voltage protection disabled and quiescent is reduced.
LSW2PsvDsc	0	LSW2 Passive Discharge Control.	0: LSW2 output is discharged only entering off and hard-reset modes. 1: LSW2 output is discharged only entering off and hard-reset modes and when the enable is low.

LSW2Ctr (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	LSW2MPC7	LSW2MPC6	LSW2MPC5	LSW2MPC4	LSW2MPC3	LSW2MPC2	LSW2MPC1	LSW2MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW2MPC7	7	LSW2 MPC7 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC7. 1: LSW2 controlled by MPC7.
LSW2MPC6	6	LSW2 MPC6 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC6. 1: LSW2 controlled by MPC6.
LSW2MPC5	5	LSW2 MPC5 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC5. 1: LSW2 controlled by MPC5.
LSW2MPC4	4	LSW2 MPC4 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC4. 1: LSW2 controlled by MPC4.
LSW2MPC3	3	LSW2 MPC3 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC3. 1: LSW2 controlled by MPC3.
LSW2MPC2	2	LSW2 MPC2 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC2. 1: LSW2 controlled by MPC2.
LSW2MPC1	1	LSW2 MPC1 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC1. 1: LSW2 controlled by MPC1.
LSW2MPC0	0	LSW2 MPC0 Enable Control. Only valid when LSW2Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW2 is controlled by the logical OR of the MPCs.	0: LSW2 not controlled by MPC0. 1: LSW2 controlled by MPC0.

LSW3Ena (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	LSW3Seq[2:0]			–	–	–	LSW3En[1:0]	
Reset	0b000			–	–	–	0b00	
Access Type	Write, Read			–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LSW3Seq	7:5	LSW3 Enable Configuration.	000: Disabled. 001: Reserved. 010: Enabled at 0% of boot/POR process delay control. 011: Enabled at 25% of boot/POR process delay control. 100: Enabled at 50% of boot/POR process delay control. 101: Reserved. 110: Reserved. 111: Controlled by LSW3En[1:0] after 100% of boot/POR process delay control.
LSW3En	1:0	LSW3 Enable Configuration (Effective only when LSW3Seq = 111.)	00: Disabled. 01: Enabled. 10: Controlled by MPC_ (see the LSW3MPC_ bits in register 0x71.) 11: Reserved.

LSW3Cfg (0x70)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LSW3ActDsc	LSW3LowIq	LSW3PsvDsc
Reset	–	–	–	–	–	0b0	0b0	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW3ActDsc	2	LSW3 Active Discharge Control.	0: LSW3 output is actively discharged only in hard-reset mode. 1: LSW3 output is actively discharged in hard-reset mode and also when its enable goes low.
LSW3LowIq	1	LSW3 Low Quiescent Control. Low quiescent mode is achieved by disabling the voltage protection of LSW3.	0: Voltage protection enabled. If V_{SYS} - $V_{LSW2OUT}$ exceeds V_{LSW_PROT}, the output is disabled to protect from overcurrent. 1: Voltage protection disabled and quiescent is reduced.
LSW3PsvDsc	0	LSW3 Passive Discharge Control.	0: LSW3 output is discharged only entering off and hard-reset modes. 1: LSW3 output is discharged only entering off and hard-reset modes and when the enable is low.

LSW3Ctr (0x71)

BIT	7	6	5	4	3	2	1	0
Field	LSW3MPC7	LSW3MPC6	LSW3MPC5	LSW3MPC4	LSW3MPC3	LSW3MPC2	LSW3MPC1	LSW3MPC0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW3MPC7	7	LSW3 MPC7 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC7. 1: LSW3 controlled by MPC7.
LSW3MPC6	6	LSW3 MPC6 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC6. 1: LSW3 controlled by MPC6.
LSW3MPC5	5	LSW3 MPC5 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC5. 1: LSW3 controlled by MPC5.
LSW3MPC4	4	LSW3 MPC4 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC4. 1: LSW3 controlled by MPC4.
LSW3MPC3	3	LSW3 MPC3 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC3. 1: LSW3 controlled by MPC3.
LSW3MPC2	2	LSW3 MPC2 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC2. 1: LSW3 controlled by MPC2.
LSW3MPC1	1	LSW3 MPC1 Enable Control. Only valid when LSW3Seq = 111 and LSW2En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC1. 1: LSW3 controlled by MPC1.
LSW3MPC0	0	LSW3 MPC0 Enable Control. Only valid when LSW3Seq = 111 and LSW3En = 10. If multiple MPCs are selected, LSW3 is controlled by the logical OR of the MPCs.	0: LSW3 not controlled by MPC0. 1: LSW3 controlled by MPC0.

MPC0Cfg (0x72)

BIT	7	6	5	4	3	2	1	0
Field	MPC0Pin	–	–	MPC0Out	MPC0OD	MPC0HiZB	MPC0Res	MPC0Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC0Pin	7	MPC0 State.	0: MPC0 low. 1: MPC0 high (if MPC0OD = 0) or high-impedance (if MPC0OD = 1).
MPC0Out	4	MPC0 Output Value. Valid only if MPC0 is configured as output (MPC0HiZB = 1).	0: MPC0 connected to GND. 1: MPC0 open-drain off (MPC0OD = 1) or connected to BK1OUT (MPC0OD = 0).
MPC0OD	3	MPC0 Output Configuration. Valid only if MPC0 is configured as output (MPC0HiZB = 1).	0: MPC0 is push-pull connected to BK1OUT. 1: MPC0 is open drain.
MPC0HiZB	2	MPC0 Direction.	0: MPC0 is high-impedance. Input buffer enabled. 1: MPC0 is not high-impedance. Output buffer enabled.
MPC0Res	1	MPC0 Resistor Presence. Valid only if MPC0 is configured as input (MPC0HiZB = 0).	0: Resistor not connected to MPC0. 1: Resistor connected to MPC0.
MPC0Pup	0	MPC0 Resistor Configuration. Valid only if there is a resistor on MPC0 (MPC0Res = 1).	0: Pull-down connected to MPC0. 1: Pull-up to V_{CCINT} connected MPC0.

MPC1Cfg (0x73)

BIT	7	6	5	4	3	2	1	0
Field	MPC1Pin	–	–	MPC1Out	MPC1OD	MPC1HiZB	MPC1Res	MPC1Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC1Pin	7	MPC1 State.	0: MPC1 low. 1: MPC1 high (if MPC1OD = 0) or high-impedance (if MPC1OD = 1).
MPC1Out	4	MPC1 Output Value. Valid only if MPC1 is configured as output (MPC1HiZB = 1).	0: MPC1 connected to GND. 1: MPC1 open-drain off (MPC1OD = 1) or connected to BK1OUT (MPC1OD = 0).
MPC1OD	3	MPC1 Output Configuration. Valid only if MPC1 is configured as output (MPC1HiZB = 1).	0: MPC1 is push-pull connected to BK1OUT. 1: MPC1 is open drain.
MPC1HiZB	2	MPC1 Direction.	0: MPC1 is high-impedance. Input buffer enabled. 1: MPC1 is not high-impedance. Output buffer enabled.
MPC1Res	1	MPC1 Resistor Presence. Valid only if MPC1 is configured as input (MPC1HiZB = 0).	0: Resistor not connected to MPC1. 1: Resistor connected to MPC1.

BITFIELD	BITS	DESCRIPTION	DECODE
MPC1Pup	0	MPC1 Resistor Configuration. Valid only if there is a resistor on MPC1 (MPC1Res = 1).	0: Pull-down connected to MPC1. 1: Pull-up to V_{CCINT} connected MPC1.

MPC2Cfg (0x74)

BIT	7	6	5	4	3	2	1	0
Field	MPC2Pin	–	–	MPC2Out	MPC2OD	MPC2HiZB	MPC2Res	MPC2Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC2Pin	7	MPC2 State.	0: MPC2 low. 1: MPC2 high (if MPC2OD = 0) or high-impedance (if MPC2OD = 1).
MPC2Out	4	MPC2 Output Value. Valid only if MPC2 is configured as output (MPC2HiZB = 1).	0: MPC2 connected to GND. 1: MPC2 open-drain off (MPC2OD = 1) or connected to BK1OUT (MPC2OD = 0).
MPC2OD	3	MPC2 Output Configuration. Valid only if MPC2 is configured as output (MPC2HiZB = 1).	0: MPC2 is push-pull connected to BK1OUT. 1: MPC2 is open drain.
MPC2HiZB	2	MPC2 Direction.	0: MPC2 is high-impedance. Input buffer enabled. 1: MPC2 is not high-impedance. Output buffer enabled.
MPC2Res	1	MPC2 Resistor Presence. Valid only if MPC2 is configured as input (MPC2HiZB = 0).	0: Resistor not connected to MPC2. 1: Resistor connected to MPC2.
MPC2Pup	0	MPC2 Resistor Configuration. Valid only if there is a resistor on MPC2 (MPC2Res = 1).	0: Pull-down connected to MPC2. 1: Pull-up to V_{CCINT} connected MPC2.

MPC3Cfg (0x75)

BIT	7	6	5	4	3	2	1	0
Field	MPC3Pin	–	–	MPC3Out	MPC3OD	MPC3HiZB	MPC3Res	MPC3Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC3Pin	7	MPC3 State.	0: MPC3 low. 1: MPC3 high (if MPC3OD = 0) or high-impedance (if MPC3OD = 1).
MPC3Out	4	MPC3 Output Value. Valid only if MPC3 is configured as output (MPC3HiZB = 1).	0: MPC3 connected to GND. 1: MPC3 open-drain off (MPC3OD = 1) or connected to BK1OUT (MPC3OD = 0).
MPC3OD	3	MPC3 Output Configuration. Valid only if MPC3 is configured as output (MPC3HiZB = 1).	0: MPC3 is push-pull connected to BK1OUT. 1: MPC3 is open drain.
MPC3HiZB	2	MPC3 Direction.	0: MPC3 is high-impedance. Input buffer enabled. 1: MPC3 is not high-impedance. Output buffer enabled.
MPC3Res	1	MPC3 Resistor Presence. Valid only if MPC3 is configured as input (MPC3HiZB = 0).	0: Resistor not connected to MPC3. 1: Resistor connected to MPC3.
MPC3Pup	0	MPC3 Resistor Configuration. Valid only if there is a resistor on MPC3 (MPC3Res = 1).	0: Pull-down connected to MPC3. 1: Pull-up to V_{CCINT} connected MPC3.

MPC4Cfg (0x76)

BIT	7	6	5	4	3	2	1	0
Field	MPC4Pin	–	–	MPC4Out	MPC4OD	MPC4HiZB	MPC4Res	MPC4Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC4Pin	7	MPC4 State.	0: MPC4 low. 1: MPC4 high (if MPC4OD = 0) or high-impedance (if MPC4OD = 1).
MPC4Out	4	MPC4 Output Value. Valid only if MPC4 is configured as output (MPC4HiZB = 1).	0: MPC4 connected to GND. 1: MPC4 open-drain off (MPC4OD = 1) or connected to BK1OUT (MPC4OD = 0).
MPC4OD	3	MPC4 Output Configuration. Valid only if MPC4 is configured as output (MPC4HiZB = 1).	0: MPC4 is push-pull connected to BK1OUT. 1: MPC4 is open drain.
MPC4HiZB	2	MPC4 Direction.	0: MPC4 is high-impedance. Input buffer enabled. 1: MPC4 is not high-impedance. Output buffer enabled.
MPC4Res	1	MPC4 Resistor Presence. Valid only if MPC4 is configured as input (MPC4HiZB = 0).	0: Resistor not connected to MPC4. 1: Resistor connected to MPC4.
MPC4Pup	0	MPC4 Resistor Configuration. Valid only if there is a resistor on MPC4 (MPC4Res = 1).	0: Pull-down connected to MPC4. 1: Pull-up to V_{CCINT} connected MPC4.

MPC5Cfg (0x77)

BIT	7	6	5	4	3	2	1	0
Field	MPC5Pin	–	–	MPC5Out	MPC5OD	MPC5HiZB	MPC5Res	MPC5Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC5Pin	7	MPC5 State.	0: MPC5 low. 1: MPC5 high (if MPC5OD = 0) or high-impedance (if MPC5OD = 1).
MPC5Out	4	MPC5 Output Value. Valid only if MPC5 is configured as output (MPC5HiZB = 1).	0: MPC5 connected to GND. 1: MPC5 open-drain off (MPC5OD = 1) or connected to BK1OUT (MPC5OD = 0).
MPC5OD	3	MPC5 Output Configuration. Valid only if MPC5 is configured as output (MPC5HiZB = 1).	0: MPC5 is push-pull connected to BK1OUT. 1: MPC5 is open drain.
MPC5HiZB	2	MPC5 Direction.	0: MPC5 is high-impedance. Input buffer enabled. 1: MPC5 is not high-impedance. Output buffer enabled.
MPC5Res	1	MPC5 Resistor Presence. Valid only if MPC5 is configured as input (MPC5HiZB = 0).	0: Resistor not connected to MPC5. 1: Resistor connected to MPC5.
MPC5Pup	0	MPC5 Resistor Configuration. Valid only if there is a resistor on MPC5 (MPC5Res = 1).	0: Pull-down connected to MPC5. 1: Pull-up to V_{CCINT} connected MPC5.

MPC6Cfg (0x78)

BIT	7	6	5	4	3	2	1	0
Field	MPC6Pin	–	–	MPC6Out	MPC6OD	MPC6HiZB	MPC6Res	MPC6Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC6Pin	7	MPC6 State.	0: MPC6 low. 1: MPC6 high (if MPC6OD = 0) or high-impedance (if MPC6OD = 1).
MPC6Out	4	MPC6 Output Value. Valid only if MPC6 is configured as output (MPC6HiZB = 1).	0: MPC6 connected to GND. 1: MPC6 open-drain off (MPC6OD = 1) or connected to BK1OUT (MPC6OD = 0).

BITFIELD	BITS	DESCRIPTION	DECODE
MPC6OD	3	MPC6 Output Configuration. Valid only if MPC6 is configured as output (MPC6HiZB = 1).	0: MPC6 is push-pull connected to BK1OUT. 1: MPC6 is open drain.
MPC6HiZB	2	MPC6 Direction.	0: MPC6 is high-impedance. Input buffer enabled. 1: MPC6 is not high-impedance. Output buffer enabled.
MPC6Res	1	MPC6 Resistor Presence. Valid only if MPC6 is configured as input (MPC6HiZB = 0).	0: Resistor not connected to MPC6. 1: Resistor connected to MPC6.
MPC6Pup	0	MPC6 Resistor Configuration. Valid only if there is a resistor on MPC6 (MPC6Res = 1).	0: Pull-down connected to MPC6. 1: Pull-up to V_{CCINT} connected MPC6.

MPC7Cfg (0x79)

BIT	7	6	5	4	3	2	1	0
Field	MPC7Pin	–	–	MPC7Out	MPC7OD	MPC7HiZB	MPC7Res	MPC7Pup
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MPC7Pin	7	MPC7 State.	0: MPC7 low. 1: MPC7 high (if MPC7OD = 0) or high-impedance (if MPC7OD = 1).
MPC7Out	4	MPC7 Output Value. Valid only if MPC7 is configured as output (MPC7HiZB = 1).	0: MPC7 connected to GND. 1: MPC7 open-drain off (MPC7OD = 1) or connected to BK1OUT (MPC7OD = 0).
MPC7OD	3	MPC7 Output Configuration. Valid only if MPC7 is configured as output (MPC7HiZB = 1).	0: MPC7 is push-pull connected to BK1OUT. 1: MPC7 is open drain.
MPC7HiZB	2	MPC7 Direction.	0: MPC7 is high-impedance. Input buffer enabled. 1: MPC7 is not high-impedance. Output buffer enabled.
MPC7Res	1	MPC7 Resistor Presence. Valid only if MPC7 is configured as input (MPC7HiZB = 0).	0: Resistor not connected to MPC7. 1: Resistor connected to MPC7.
MPC7Pup	0	MPC7 Resistor Configuration. Valid only if there is a resistor on MPC7 (MPC7Res = 1).	0: Pull-down connected to MPC7. 1: Pull-up to V_{CCINT} connected MPC7.

MPCItrSts (0x7A)

BIT	7	6	5	4	3	2	1	0

Field	–	–	–	–	USBOkMPCSts	BK3PgMPCSts	BK2PgMPCSts	BK1PgMPCSts
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
USBOkMPCSts	3	USBOk Dedicated MPC Interrupt Status Bit.	0: USBOk MPC power-good interrupt not active. 1: USBOk MPC power-good interrupt active.
BK3PgMPCSts	2	Buck3 Dedicated MPC Interrupt Status Bit.	0: Buck3 MPC power-good interrupt not active. 1: Buck3 MPC power-good interrupt active.
BK2PgMPCSts	1	Buck2 Dedicated MPC Interrupt Status Bit.	0: Buck2 MPC power-good interrupt not active. 1: Buck2 MPC power-good interrupt active.
BK1PgMPCSts	0	Buck1 Dedicated MPC Interrupt Status Bit.	0: Buck1 MPC power-good interrupt not active. 1: Buck1 MPC power-good interrupt active.

BK1ItrCfg (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	BK1PgMPCInt	BK1MPC6Sel	BK1MPC5Sel	BK1MPC4Sel	BK1MPC3Sel	BK1MPC2Sel	BK1MPC1Sel	BK1MPC0Sel
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BK1PgMPCInt	7	Buck1 Dedicated Power-Good Interrupt.	0: No power-good status change. 1: Buck1 power-good status change caused interrupt.
BK1MPC6Sel	6	Buck1 PGOOD Interrupt MPC6 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC6. 1: Buck1 PGOOD interrupt routed to MPC6
BK1MPC5Sel	5	Buck1 PGOOD Interrupt MPC5 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC5. 1: Buck1 PGOOD interrupt routed to MPC5.
BK1MPC4Sel	4	Buck1 PGOOD Interrupt MPC4 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC4. 1: Buck1 PGOOD interrupt routed to MPC4.
BK1MPC3Sel	3	Buck1 PGOOD Interrupt MPC3 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC3. 1: Buck1 PGOOD interrupt routed to MPC3.
BK1MPC2Sel	2	Buck1 PGOOD Interrupt MPC2 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC2. 1: Buck1 PGOOD interrupt routed to MPC2.
BK1MPC1Sel	1	Buck1 PGOOD Interrupt MPC1 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC1. 1: Buck1 PGOOD interrupt routed to MPC1.
BK1MPC0Sel	0	Buck1 PGOOD Interrupt MPC0 Assignment Control.	0: Buck1 PGOOD interrupt not routed to MPC0. 1: Buck1 PGOOD interrupt routed to MPC0.

BK2ItrCfg (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	BK2PgMPCInt	BK2MPC6Sel	BK2MPC5Sel	BK2MPC4Sel	BK2MPC3Sel	BK2MPC2Sel	BK2MPC1Sel	BK2MPC0Sel
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BK2PgMPCInt	7	Buck2 Dedicated Power-Good Interrupt.	0: No power-good status change. 1: Buck2 power-good status change caused interrupt.
BK2MPC6Sel	6	Buck2 PGOOD Interrupt MPC6 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC6. 1: Buck2 PGOOD interrupt routed to MPC6.
BK2MPC5Sel	5	Buck2 PGOOD Interrupt MPC5 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC5. 1: Buck2 PGOOD interrupt routed to MPC5.
BK2MPC4Sel	4	Buck2 PGOOD Interrupt MPC4 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC4. 1: Buck2 PGOOD interrupt routed to MPC4.
BK2MPC3Sel	3	Buck2 PGOOD Interrupt MPC3 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC3. 1: Buck2 PGOOD interrupt routed to MPC3.
BK2MPC2Sel	2	Buck2 PGOOD Interrupt MPC2 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC2. 1: Buck2 PGOOD interrupt routed to MPC2.
BK2MPC1Sel	1	Buck2 PGOOD Interrupt MPC1 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC1. 1: Buck2 PGOOD interrupt routed to MPC1.
BK2MPC0Sel	0	Buck2 PGOOD Interrupt MPC0 Assignment Control.	0: Buck2 PGOOD interrupt not routed to MPC0. 1: Buck2 PGOOD interrupt routed to MPC0.

BK3ItrCfg (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	BK3PgMPCInt	BK3MPC6Sel	BK3MPC5Sel	BK3MPC4Sel	BK3MPC3Sel	BK3MPC2Sel	BK3MPC1Sel	BK3MPC0Sel
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BK3PgMPCInt	7	Buck3 Dedicated Power-Good Interrupt.	0: No power-good status change. 1: Buck3 power-good status change caused interrupt.
BK3MPC6Sel	6	Buck3 PGOOD Interrupt MPC6 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC6. 1: Buck3 PGOOD interrupt routed to MPC6.
BK3MPC5Sel	5	Buck3 PGOOD Interrupt MPC5 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC5. 1: Buck3 PGOOD interrupt routed to MPC5.

BITFIELD	BITS	DESCRIPTION	DECODE
BK3MPC4Sel	4	Buck3 PGOOD Interrupt MPC4 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC4. 1: Buck3 PGOOD interrupt routed to MPC4.
BK3MPC3Sel	3	Buck3 PGOOD Interrupt MPC3 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC3. 1: Buck3 PGOOD interrupt routed to MPC3.
BK3MPC2Sel	2	Buck3 PGOOD Interrupt MPC2 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC2. 1: Buck3 PGOOD interrupt routed to MPC2.
BK3MPC1Sel	1	Buck3 PGOOD Interrupt MPC1 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC1. 1: Buck3 PGOOD interrupt routed to MPC1.
BK3MPC0Sel	0	Buck3 PGOOD Interrupt MPC0 Assignment Control.	0: Buck3 PGOOD interrupt not routed to MPC0. 1: Buck3 PGOOD interrupt routed to MPC0.

USBOkItrCfg (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	USBOkMPCInt	USBOkMPC6Sel	USBOkMPC5Sel	USBOkMPC4Sel	USBOkMPC3Sel	USBOkMPC2Sel	USBOkMPC1Sel	USBOkMPC0Sel
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
USBOkMPCInt	7	USBOk Dedicated Power-Good Interrupt.	0: No USBOk status change. 1: USBOk status change caused interrupt.
USBOkMPC6Sel	6	USBOk Dedicated Interrupt MPC6 Assignment Control.	0: USBOk interrupt not routed to MPC6. 1: USBOk interrupt routed to MPC6.
USBOkMPC5Sel	5	USBOk Dedicated Interrupt MPC5 Assignment Control.	0: USBOk interrupt not routed to MPC5. 1: USBOk interrupt routed to MPC5.
USBOkMPC4Sel	4	USBOk Dedicated Interrupt MPC4 Assignment Control.	0: USBOk interrupt not routed to MPC4. 1: USBOk interrupt routed to MPC4.
USBOkMPC3Sel	3	USBOk Dedicated Interrupt MPC3 Assignment Control.	0: USBOk interrupt not routed to MPC3. 1: USBOk interrupt routed to MPC3.
USBOkMPC2Sel	2	USBOk Dedicated Interrupt MPC2 Assignment Control.	0: USBOk interrupt not routed to MPC2. 1: USBOk interrupt routed to MPC2.
USBOkMPC1Sel	1	USBOk Dedicated Interrupt MPC1 Assignment Control.	0: USBOk interrupt not routed to MPC1. 1: USBOk interrupt routed to MPC1.
USBOkMPC0Sel	0	USBOk Dedicated Interrupt MPC0 Assignment Control.	0: USBOk interrupt not routed to MPC0. 1: USBOk interrupt routed to MPC0.

PFN (0x80)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PFN2Pin	PFN1Pin
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PFN2Pin	1	Status of PFN2.	0: PFN2 not active. 1: PFN2 active.
PFN1Pin	0	Status of PFN1.	0: PFN1 not active. 1: PFN1 active.

BootCfg (0x81)

BIT	7	6	5	4	3	2	1	0
Field	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		ChgAlwTry
Reset	0x0				0b0	0b00		0b0
Access Type	Read Only				Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PwrRstCfg	7:4	Power Reset Configuration. Determines how the device turns on, off, and enters hard-/soft-reset. See the PwrRstCfg settings in Table 5 for PwrRstCfg values and their associated behaviors.	
SftRstCfg	3	Soft-Reset Configuration. Indicates whether registers are held or reset to default during a soft-reset.	0: Hold register contents. 1: Reset registers to default.
BootDly	2:1	Boot Delay. The boot period when the sequencing engine turns on features with sequence bits 010, 011, and 100.	00: 80ms. 01: 120ms. 10: 220ms. 11: 420ms.
ChgAlwTry	0	SYS UVLO Automatic Retry. Determines what happens when a SYS UVLO event occurs during the boot process with CHGIN present.	0: Part latches off until CHGIN is removed. 1: Part retries to boot after $t_{CHG\_RETRY\_TMO}$ delay if CHGIN is still present.

PwrCfg (0x82)

BIT	7	6	5	4	3	2	1	0

Field	–	INTBootMsk	–	–	–	–	–	StayOn
Reset	–	0b0	–	–	–	–	–	0b0
Access Type	–	Write, Read	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
INTBootMsk	6	Bit Used to Mask INTb During Shutdown to Prevent Application Processor Lock.	0: INTb masked during shutdown. 1: INTb not masked during shutdown.
StayOn	0	Bit Used to Ensure that Processor is Booted Correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set.	0: Shut down 5s after power-on. 1: Stay on.

PwrCmd (0x83)

BIT	7	6	5	4	3	2	1	0
Field	PwrCmd[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PwrCmd	7:0	Power Command Register. Writing the following values issues the command listed. After the written value has been validated by the internal logic, this register is cleared automatically. Any other commands are ignored. See the PwrRstCfg settings in Table 5 for the available PwrCmd for each PwrRstCfg value.	0xB2: PWR_OFF_CMD: places the part in off mode. 0xC3: PWR_HR_CMD: issues a hard-reset (power cycle). 0xD4: PWR_SR_CMD: issues a soft-reset (reset pulse only). 0xE5: PWR_SEAL_CMD: places the part in seal mode. available for PwrRstCfg 0110, 0111, 1000, 1001, 1010, 1011 and 1100 0xF6: PWR_BR_CMD: places the part in battery recovery mode. Available only if HrvEn = 1. 0x52: PWR_FACT_CMD: places the part in factory mode.

MiscFunctions (0x84)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MiscFunc[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MiscFunc	3:0	Multi Function Bit. This bit includes settings for global active discharge, RTC_LDO feature, factory mode, and reserve for future (RFU).	MiscFunc[0] = 0: if active discharge is enabled, output of the block is actively discharged for 50ms while the block is disabled. (default) MiscFunc[0] = 1: if active discharge is enabled, output of the block is actively discharged constantly while the block is disabled. MiscFunc[1] = 0: RTC LDO feature is on. MiscFunc[1] = 1: RTC LDO feature is off. MiscFunc[2] = 0: Factory mode is enabled. MiscFunc[2] = 1: Factory mode is disbaled. MiscFunc[3] = RFU.

LockMsk1 (0x86)

BIT	7	6	5	4	3	2	1	0
Field	LD4Lck	LD3Lck	LD2Lck	LD1Lck	BBLck	BK3Lck	BK2Lck	BK1Lck
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LD4Lck	7	Lock Mask for LDO4 Registers.	0: LDO4 registers not masked from locking/unlocking. 1: LDO4 registers masked from locking/unlocking.
LD3Lck	6	Lock Mask for LDO3 Registers.	0: LDO3 registers not masked from locking/unlocking. 1: LDO3 registers masked from locking/unlocking.
LD2Lck	5	Lock Mask for LDO2 Registers.	0: LDO2 registers not masked from locking/unlocking. 1: LDO2 registers masked from locking/unlocking.
LD1Lck	4	Lock Mask for LDO1 Registers.	0: LDO1 registers not masked from locking/unlocking. 1: LDO1 registers masked from locking/unlocking.
BBLck	3	Lock Mask for Buck-Boost Registers.	0x0: Buck-Boost registers not masked from locking/unlocking. 0x1: Buck-Boost registers masked from locking/unlocking.
BK3Lck	2	Lock Mask for Buck3 Registers.	0x0: Buck3 registers not masked from locking/unlocking. 0x1: Buck3 registers masked from locking/unlocking.
BK2Lck	1	Lock Mask for Buck2 Registers.	0x0: Buck2 registers not masked from locking/unlocking. 0x1: Buck2 registers masked from locking/unlocking.
BK1Lck	0	Lock Mask for Buck1 Registers.	0x0: Buck1 registers not masked from locking/unlocking. 0x1: Buck1 registers masked from locking/unlocking.

LockMsk2 (0x87)

BIT	7	6	5	4	3	2	1	0
Field	LD4SeqLck	LD3SeqLck	LD2SeqLck	LD1SeqLck	BBSeqLck	BK3SeqLck	BK2SeqLck	BK1SeqLck
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1

Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LD4SeqLck	7	Lock Mask for LDO4Seq Registers.	0x0: LDO4Seq registers unlocked (read/write). 0x1: LDO4Seq registers masked from locked (read only).
LD3SeqLck	6	Lock Mask for LDO3Seq Registers.	0x0: LDO2Seq registers unlocked (read/write). 0x1: LDO2Seq registers masked from locked (read only).
LD2SeqLck	5	Lock Mask for LDO2Seq Registers.	0x0: LDO2Seq registers unlocked (read/write). 0x1: LDO2Seq registers masked from locked (read only).
LD1SeqLck	4	Lock Mask for LDO1Seq Registers.	0x0: LDO1Seq registers unlocked (read/write). 0x1: LDO1Seq registers masked from locked (read only).
BBSeqLck	3	Lock Mask for BBseq Registers.	0x0: BBstSeqSeq registers unlocked (read/write). 0x1: BBstSeq registers masked from locked (read only).
BK3SeqLck	2	Lock Mask for Buck3Seq Registers.	0x0: Buck3Seq registers unlocked (read/write). 0x1: Buck3Seq registers masked from locked (read only).
BK2SeqLck	1	Lock Mask for Buck2Seq Registers.	0x0: Buck2Seq registers unlocked (read/write). 0x1: Buck2Seq registers masked from locked (read only).
BK1SeqLck	0	Lock Mask for Buck1Seq Registers.	0x0: Buck1Seq registers unlocked (read/write). 0x1: Buck1Seq registers masked from locked (read only).

LockMsk3 (0x89)

BIT	7	6	5	4	3	2	1	0
Field	LSW3SeqLck	LSW2SeqLck	LSW1SeqLck	–	WDLck	GMDrpLck	LimLck	ChgLck
Reset	0b1	0b1	0b1	–	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LSW3SeqLck	7	Lock Mask for LSW3Seq Registers.	0x0: LSW3Seq registers unlocked (read/write). 0x1: LSW3Seq registers masked from locked (read only).
LSW2SeqLck	6	Lock Mask for LSW2Seq Registers.	0x0: LSW2Seq registers unlocked (read/write). 0x1: LSW2Seq registers masked from locked (read only).
LSW1SeqLck	5	Lock Mask for LSW1Seq Registers.	0x0: LSW1Seq registers unlocked (read/write). 0x1: LSW1Seq registers masked from locked (read only).
WDLck	3	Lock Mask for WatchDog Registers.	0x0: Charger registers not masked from locking/unlocking. 0x1: Charger registers masked from locking/unlocking.
GMDrpLck	2	Lock Mask for Charger Registers.	0x0: Charger registers not masked from locking/unlocking. 0x1: Charger registers masked from locking/unlocking.
LimLck	1	Lock Mask for Charger Registers.	0x0: Charger registers not masked from locking/unlocking. 0x1: Charger registers masked from locking/unlocking.
ChgLck	0	Lock Mask for Charger Registers.	0x0: Charger registers not masked from locking/unlocking. 0x1: Charger registers masked from locking/unlocking.

LockUnlock1 (0x8A)

BIT	7	6	5	4	3	2	1	0
Field	PASSWD1[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PASSWD1	7:0	Lock/Unlock Password. Locks or unlocks all unmasked functions set in the lock mask register, LockMsk1, when the correct password is written. Reading this register returns the current lock state of the functions. Locked functions return 1 and unlocked functions return 0. Functions are organized in the same order as register LockMsk1 .	0x55: Unlock unmasked functions. 0xAA: Lock unmasked functions. All Other Codes: No effect.

LockUnlock2 (0x8B)

BIT	7	6	5	4	3	2	1	0
Field	PASSWD2[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PASSWD2	7:0	Lock/Unlock Password. Locks or unlocks all unmasked functions set in the lock mask register, LockMsk2, when the correct password is written. Reading this register returns the current lock state of the functions. Locked functions return 1 and unlocked functions return 0. Functions are organized in the same order as register LockMsk2 .	0x55: Unlock unmasked functions. 0xAA: Lock unmasked functions. All Other Codes: No effect.

LockUnlock3 (0x8C)

BIT	7	6	5	4	3	2	1	0
Field	PASSWD3[7:0]							
Reset	0xFF							

Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PASSWD3	7:0	Lock/Unlock Password. Locks or unlocks all unmasked functions set in the lock mask register, LockMsk3, when the correct password is written. Reading this register returns the current lock state of the functions. Locked functions return 1 and unlocked functions return 0. Functions are organized in the same order as register LockMsk3.	0x55: Unlock unmasked functions. 0xAA: Lock unmasked functions. All Other Codes: No effect.

I2C_OTP (0x8D)

BIT	7	6	5	4	3	2	1	0
Field	OTPDIG__ADD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
OTPDIG__ADD	7:0	Address of the OTP Reg File for OTP Registers Readback. OTP registers are filled with data from OTP memory block during boot.

I2C_OTP (0x8E)

BIT	7	6	5	4	3	2	1	0
Field	OTPDIG__DAT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTPDIG__DAT	7:0	OTP Data Readback.

Applications Information

I²C Interface

The MAX20356 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The MAX20356 interface supports frequencies up to f_{SCL}. SCL and SDA require pull-up resistors that are connected to a positive supply.

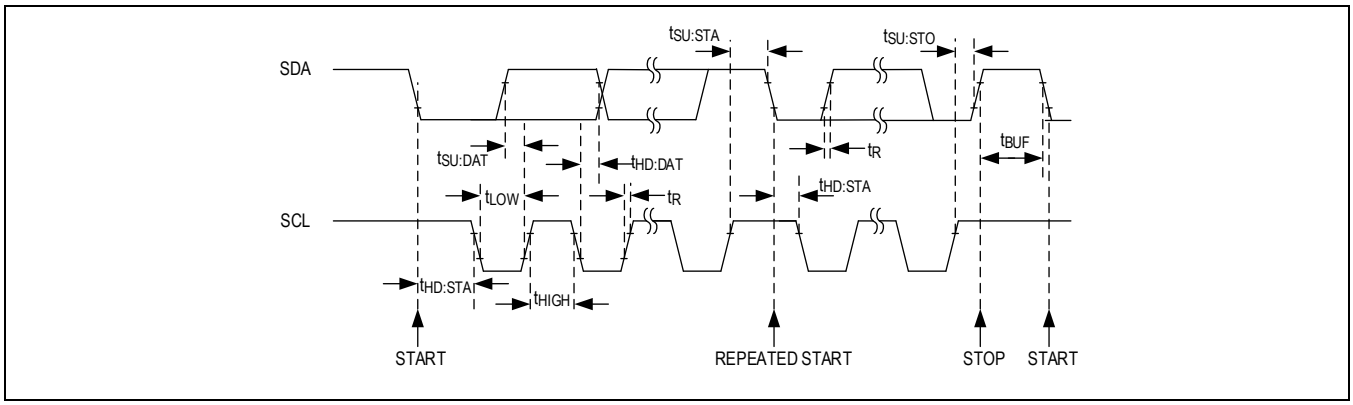


Figure 34. I²C Interface Timing

Peripheral Address

The MAX20356 peripheral address is 0b1010000 (0x50) plus the read/write bit. Set the read/write bit high to configure the MAX20356 to read mode (0x50). Set the read/write bit low to configure the MAX20356 to write mode (0x51). For the fuel gauge, the peripheral address is 0x6C/0x6D.

Start, Stop, and Repeated Start Conditions

When writing to the MAX20356 using the I²C interface, the controller sends a start condition (S) followed by the MAX20356 I²C address. After the address, the controller sends the register address of the register that is to be programmed. The controller then ends communication by issuing a stop condition (P) to relinquish control of the bus, or a repeated start condition (Sr) to communicate to another I²C peripheral.

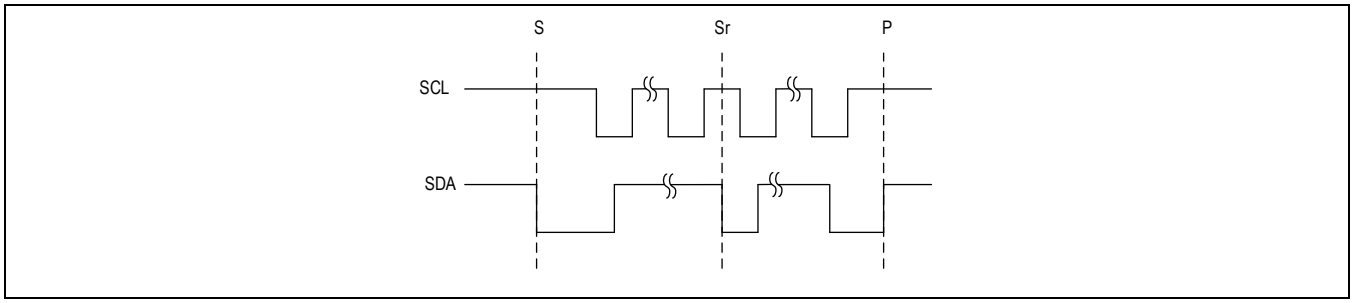


Figure 35. I²C Start, Stop, and Repeated Start Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, and Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the controller sends an address and multiple data bytes to the peripheral device. The following procedure describes the burst write operation:

1. The controller sends a start condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.

4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line only if the address is valid (NAK if not).
6. The controller sends 8 data bits.
7. The peripheral asserts an ACK on the data line.
8. The controller generates a stop condition.

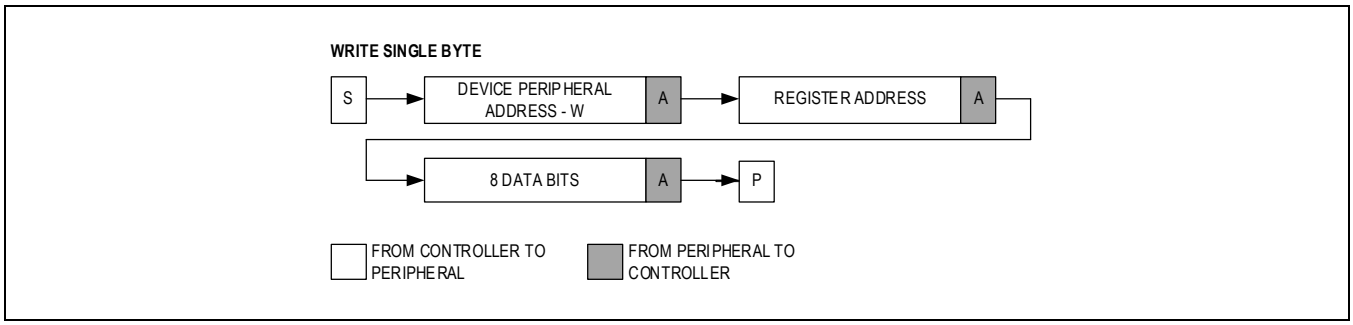


Figure 36. Single-Byte Write Sequence

Burst Write

In this operation, the controller sends an address and multiple data bytes to the peripheral device. The peripheral device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

1. The controller sends a start condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line only if the address is valid (NAK if not).
6. The controller sends 8 data bits.
7. The peripheral asserts an ACK on the data line.
8. Repeat step 6 and step 7 N-1 times.
9. The controller generates a stop condition.

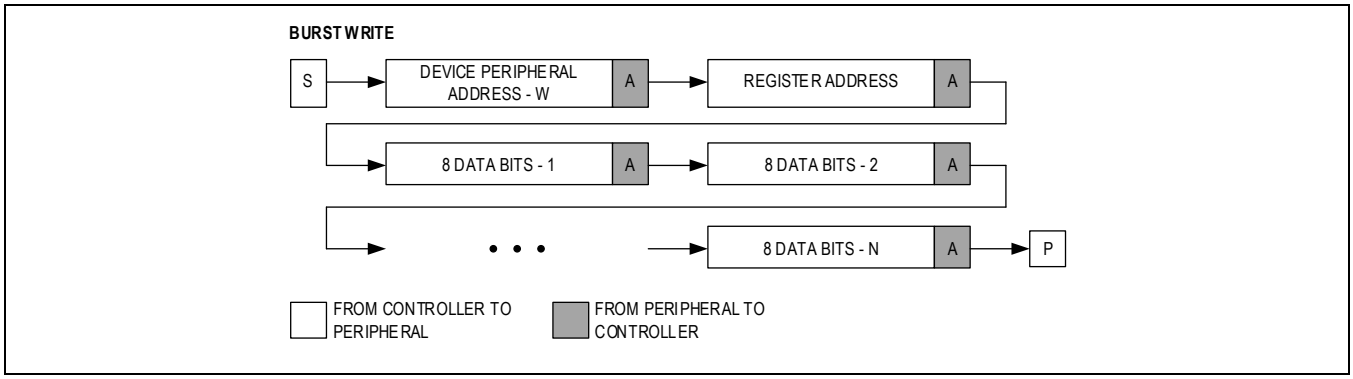


Figure 37. Burst-Write Sequence

Single-Byte Read

In this operation, the controller sends an address plus two data bytes and receives one data byte from the peripheral device. The following procedure describes the single-byte read operation:

1. The controller sends a start condition.

2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line only if the address is valid (NAK if not).
6. The controller sends a repeated start condition.
7. The controller sends the 7-bit peripheral address plus a read bit (high).
8. The addressed peripheral asserts an ACK on the data line.
9. The peripheral sends 8 data bits.
10. The controller asserts a NACK on the data line.
11. The controller generates a stop condition.

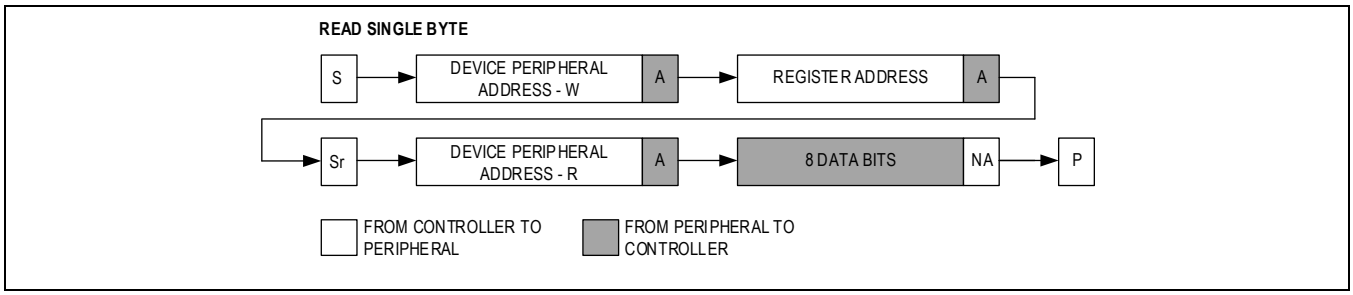


Figure 38. Single-Byte Read Sequence

Burst Read

In this operation, the controller sends an address plus two data bytes and receives multiple data bytes from the peripheral device. The following procedure describes the burst byte read operation:

1. The controller sends a start condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line only if the address is valid (NAK if not).
6. The controller sends a repeated start condition.
7. The controller sends the 7-bit peripheral address plus a read bit (high).
8. The peripheral asserts an ACK on the data line.
9. The peripheral sends 8 data bits.
10. The controller asserts an ACK on the data line.
11. Repeat step 9 and step 10 N-2 times.
12. The peripheral sends the last 8 data bits.
13. The controller asserts a NACK on the data line.
14. The controller generates a stop condition.

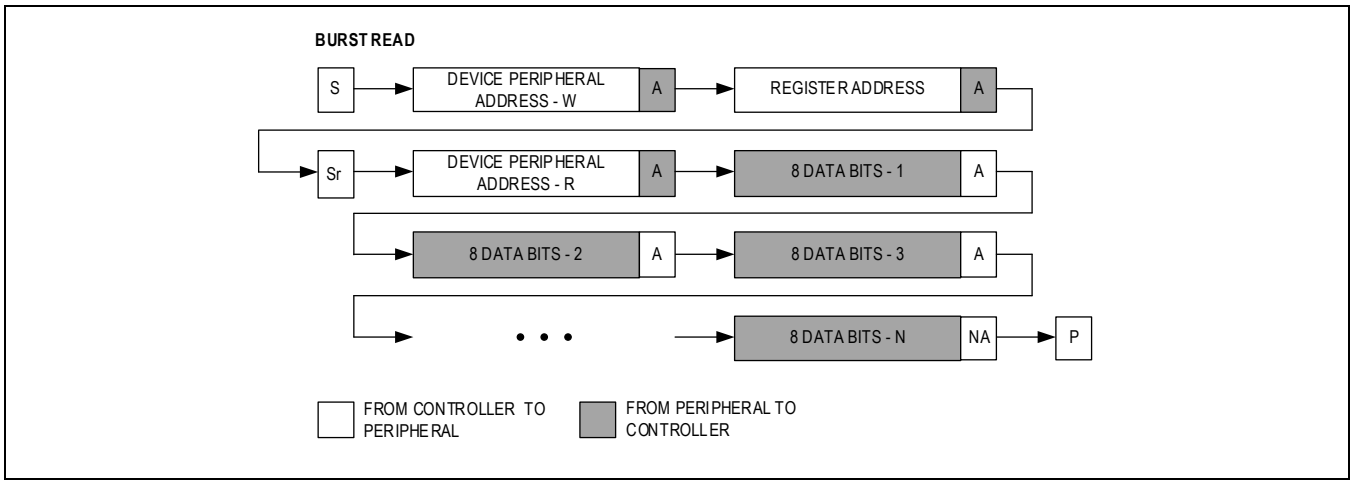


Figure 39. Burst-Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the controller and the MAX2056 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse. To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

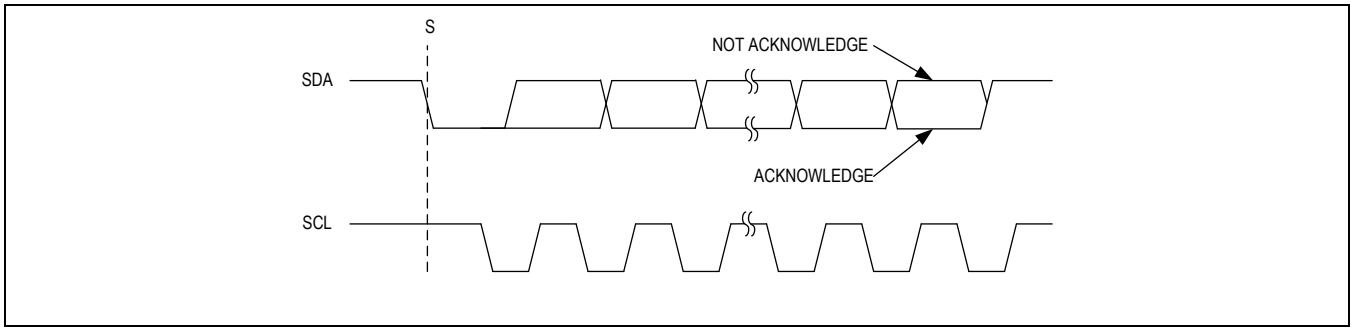


Figure 40. Acknowledge Bits

I²C Security Functions

Function Locking

All regulator voltages and the end-of-charge behavior of the charger can be locked. I²C writes to a locked bitfield have no effect. To lock a function, its lock mask must be removed in the LockMsk1, LockMsk2, and LockMsk3 registers (see the LockMsk1, LockMsk2, and LockMsk3 registers). To remove the lock mask, set the corresponding function mask bit to 0. By writing the lock password 0xAA to the LockUnlock1, LockUnlock2, and LockUnlock3 registers (see the LockUnlock1, LockUnlock2, and LockUnlock3 registers), all unmasked functions are locked. To unlock functions, repeat the mask/unmask process and write the unlock password 0x55 to the LockUnlock1, LockUnlock2, and LockUnlock3 registers. If the function is locked by the OTP PASSWD1, PASSWD2, and PASSWD3, to unlock password, write 0x00 to LockMsk1, LockMsk2, and LockMsk3 registers, and write the unlock password 0x55 to the LockUnlock1, LockUnlock2, and LockUnlock3 registers. The LockUnlock1, LockUnlock2, and LockUnlock3 registers are then 0x00 when read, which means all functions are now unlocked.

Default Bits

Table 6 shows the default settings for different versions. These default values are OTP programmable. Some bits can be changed through the I²C interface after power-up while some bits are set through OTP.

Table 6. Device Default Settings

FIELD	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
ILimBlank	Disabled	Disabled	Disabled	Disabled	Disabled	1ms
ILimMax	1000mA	1000mA	1500mA	1500mA	1500mA	1000mA
ILimCntl	450mA	450mA	450mA	450mA	450mA	1000mA
PPDrp	25mV	25mV	25mV	25mV	25mV	25mV
SysOVD	200mV	200mV	200mV	200mV	200mV	175mV
SysDSCEn	1	1	1	1	1	1
SysMinVlt	3.60V	3.60V	3.60V	3.30V	3.30V	3.40V
CC1IFChg	200mA	200mA	190mA	100mA	100mA	14mA
SysUVLOThSel	2.70V	2.70V	3.00V	3.00V	3.00V	3.00V
SYSDrp	25mV	25mV	25mV	25mV	25mV	25mV
CC2IFChg	200mA	200mA	190mA	100mA	100mA	14mA
CC1RoomOnly	1	1	0	1	1	1
CC1TmoLimit	0	0	1	0	0	0
CC1Enable	0	0	0	0	0	0
ChgBatReg	4.20V	4.20V	4.20V	4.20V	4.20V	4.15V
ChgEn	1	1	1	1	1	1
ChgAutoStop	1	1	1	1	1	1
ChgAutoReSta	1	1	1	1	1	1
VPChg	3.10V	3.10V	3.10V	3.10V	3.00V	3.40V
IPChg	5% I_{FCHG}	5% I_{FCHG}	5% I_{FCHG}	10% I_{FCHG}	10% I_{FCHG}	10% I_{FCHG}
IChgDone	20% I_{FCHG}	20% I_{FCHG}	10% I_{FCHG}	10% I_{FCHG}	10% I_{FCHG}	2.5% I_{FCHG}
BatReChg	ChgBatReg - 100mV	ChgBatReg - 100mV	ChgBatReg - 150mV	ChgBatReg - 150mV	ChgBatReg - 150mV	ChgBatReg - 200mV
PChgTmr	60min	60min	30min	30min	30min	30min
CC1FChgTmr	120min	120min	120min	120min	60min	240min
ChgTmr	300min	300min	300min	300min	150min	300min
ChgStepHyst	400mV	400mV	200mV	200mV	200mV	400mV
ChgStepRise	3.80V	3.80V	3.80V	3.80V	3.80V	3.80V
MtChgTmr	60min	60min	30min	30min	30min	30min
ChgCoolCC1IFChg	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}
ChgCoolBatReg	ChgBatReg	ChgBatReg	ChgBatReg	ChgBatReg	ChgBatReg	ChgBatReg
ChgCoolCC2IFChg	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}
ChgRoomCC1IFChg	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}
ChgRoomBatReg	ChgBatReg	ChgBatReg	ChgBatReg	ChgBatReg	ChgBatReg	ChgBatReg
ChgRoomCC2IFChg	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}	100% I_{FCHG}
ChgWarmCC1IFChg	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	30% I_{FCHG}
ChgWarmBatReg	ChgBatReg - 150mV	ChgBatReg - 150mV	ChgBatReg - 150mV	ChgBatReg - 150mV	ChgBatReg – 150mV	ChgBatReg – 150mV

FIELD	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
ChgWarmCC2IFChg	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	20% I_{FCHG}	50% I_{FCHG}
ChgT2ThrCC1	15°C	15°C	15°C	15°C	15°C	15°C
ChgT1ThrDef	0°C	0°C	0°C	0°C	0°C	0°C
ChgT1ThrCC1	0°C	0°C	0°C	0°C	0°C	0°C
ChgT3ThrCC1	45°C	45°C	45°C	45°C	45°C	45°C
ChgT2ThrDef	15°C	15°C	15°C	15°C	15°C	15°C
ChgT4ThrDef	60°C	60°C	60°C	60°C	60°C	60°C
ChgT4ThrCC1	60°C	60°C	60°C	60°C	60°C	60°C
ChgT3ThrDef	45°C	45°C	45°C	45°C	45°C	45°C
ChgThrmLim	115°C	115°C	115°C	115°C	115°C	60°C
ThmPUSel	10kΩ PU	10kΩ PU	10kΩ PU	10kΩ PU	10kΩ PU	10kΩ PU
ThmEn	001	001	001	001	001	011
HrvFreeMPC	0	0	0	0	0	0
ChgFresh	1	1	1	1	1	1
WdRstType	00	00	00	00	00	00
WDTmrSel	11	11	11	11	11	11
HrvModCfg	00	00	00	00	00	11
HrvThmEn	Cool/Room	Cool/Room	Cool/Room /Warm	Cool/Room /Warm	Cool/Room /Warm	Disabled
HrvThmDio	0	0	0	0	0	1
Buck1FET	0	0	0	0	0	0
Buck1EnLxSns	ZeroCrossing	ZeroCrossing	ZeroCrossing	ZeroCrossing	ZeroCrossing	ZeroCrossing
Buck1Seq	Buck1En After 100%	Buck1En After 100%	Buck1En After 100%	Buck1En After 100%	Buck1En After 100%	Buck1En After 100%
Buck1En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Buck1VStep	10mV	10mV	25mV	50mV	50mV	25mV
Buck1VSet	1.10V	1.10V	1.800V	1.800V	0.700V	1.800V
Buck1LowBW	0	0	0	0	0	0
Buck1FrcDCM	0	0	0	0	0	0
Buck2Seq	Buck2En After 100%	Buck2En After 100%	Buck2En After 100%	50%	50%	Buck2En After 100%
Buck2En	Disabled	Disabled	Disabled	Enabled	Enabled	Disabled
Buck2VStep	25mV	25mV	25mV	25mV	10mV	25mV
Buck2VSet	1.800V	1.800V	1.800V	1.350V	1.050V	1.350V
Buck2LowBW	0	0	0	0	0	0
Buck2FrcDCM	0	0	0	0	0	0
Buck2FET	0	0	0	0	0	0
Buck2EnLxSns	VLX Detection	VLX Detection	ZeroCrossing	ZeroCrossing	ZeroCrossing	ZeroCrossing
Buck3Seq	Buck3En After 100%	Buck3En After 100%	Buck3En After 100%	25%	25%	Buck3En After 100%
Buck3En	Disabled	Disabled	Enabled	Enabled	Enabled	Disabled
Buck3FrcDCM	0	0	0	0	0	0
Buck3FET	0	0	0	0	0	0

FIELD	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
Buck3EnLxSns	VLX Detection	VLX Detection	ZeroCrossing	ZeroCrossing	ZeroCrossing	VLX Detection
BBstEn	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Buck3VStep	50mV	50mV	50mV	50mV	50mV	50mV
Buck3VSet	3.200V	3.200V	3.300V	1.800V	1.850V	3.200V
Buck3LowBW	0	0	0	0	0	0
BBstVSet	5.000V	5.000V	5.000V	5.000V	5.000V	4.500V
BBstMode	BuckBoost	BuckBoost	BuckBoost	BuckBoost	BuckBoost	BuckBoost
BBstSeq	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%
LDO1En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
BBstFast	Low I_Q	Low I_Q	Low I_Q	Low I_Q	Low I_Q	FAST Mode
BBstFFET	0	0	0	0	0	0
BBFHighSh	100kHz/25kHz	100kHz/25kHz	100kHz/25kHz	100kHz/25kHz	100kHz/25kHz	100kHz/25kHz
LDO1VSet	0.90V	0.90V	1.80V	1.80V	1.80V	1.80V
LDO1IntSup	External	External	External	External	External	External
LDO1Mode	LDO	LDO	LDO	Load Switch	Load Switch	LDO
LDO1Seq	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%
LDO2Seq	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%
LDO2En	Disabled	Disabled	Enabled	Disabled	Disabled	Disabled
LDO3En	Disabled	Disabled	Disabled	Disabled	Enabled	Disabled
LDO2VSet	3.00V	3.00V	3.30V	3.30V	1.80V	3.20V
LDO2Mode	LDO	LDO	LDO	LDO	Load Switch	LDO
LDO3_MPC_CNF	0	0	0	0	0	0
LDO3_HICOUT	0	0	0	0	0	1
LDO3_FRC_HIC	0	0	0	0	0	0
LDO3Seq	LDO3En After 100%	LDO3En After 100%	LDO3En After 100%	LDO3En After 100%	LDO3En After 100%	LDO3En After 100%
LDO4En	Disabled	Disabled	Disabled	Disabled	Enabled	Disabled
LDO3VSet	1.800V	1.800V	1.800V	0.900V	3.200V	1.750V
LDO4VInc	0mV	0mV	0mV	0mV	0mV	0mV
LDO4VSet	1.80V	1.80V	1.80V	1.80V	1.80V	1.80V
LDO4Seq	LDO4En After 100%	LDO4En After 100%	LDO4En After 100%	LDO4En After 100%	0%	LDO4En After 100%
LSW2En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
LSW1LowIq	Protected	Protected	Protected	Protected	Protected	Low I_Q
LSW1Seq	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%	LSW1En After 100%
LSW1En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
LSW3Seq	LSW3En After 100%	LSW3En After 100%	LSW3En After 100%	LSW3En After 100%	LSW3En After 100%	LSW3En After 100%
LSW3En	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
LSW2LowIq	Protected	Protected	Protected	Protected	Protected	Low I_Q

FIELD	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
SftRstCfg	Reset Regs	Reset Regs	Reset Regs	Reset Regs	Reset Regs	Reset Regs
LSW2Seq	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%	LSW2En After 100%
BootDly	120ms	120ms	80ms	80ms	80ms	420ms
PwrRstCfg	1011	1011	1011	1011	1011	1000
ChgAlwTry	Retry	Retry	Retry	Retry	Retry	Retry
LSW3LowIq	Protected	Protected	Low I_Q	Low I_Q	Low I_Q	Low I_Q
MiscFunc[2]	1	1	1	1	1	0
MiscFunc[1]	0	0	0	0	1	1
MiscFunc[0]	0	0	0	0	0	0
StayOn	1	1	1	1	1	1
PASSWD1	0x00	0x00	0x55	0x00	0x00	0x00
PASSWD2	0x00	0x00	0x55	0x00	0x00	0x00
PASSWD3	0x00	0x00	0x55	0x00	0x00	0x00
IBatOc	1600mA	1600mA	1000mA	1400mA	1400mA	800mA
USbOkselect	CHGIN Rise	CHGIN Rise	CHGIN Rise	CHGIN Rise	CHGIN Rise	No Reset
Buck1IqMD	400nA	400nA	400nA	700nA	700nA	400nA
Buck1Sind	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH
Buck2IqMD	400nA	400nA	1.1µA	700nA	700nA	400nA
Buck2Sind	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH
Buck3IqMD	400nA	400nA	400nA	700nA	700nA	400nA
Buck3Sind	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH
PFN1PU	Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up
PFN2PU	Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up
PFN1RES	Connect Resistor	Connect Resistor	Connect Resistor	Connect Resistor	Connect Resistor	Connect Resistor
PFN2RES	No Resistor	No Resistor	No Resistor	No Resistor	No Resistor	No Resistor
FG_OTP_ENA	1	1	1	1	1	1
HrvEn	0	1	0	0	0	0
GlbPsvEna	1	1	1	1	1	1
I2cTmoEn	1	1	0	1	1	0
FactModeSel	11	11	11	11	11	00
RstModeSel	1	1	1	1	1	1
LDO2FltHP	0	0	0	0	0	0
LDO1FltHP	0	0	0	0	0	0
LSW3FltHP	0	0	0	0	0	0
LSW2FltHP	0	0	0	0	0	0
LSW1FltHP	0	0	0	0	0	0
BBFltHP	0	0	0	0	0	0
BCK3FltHP	0	0	0	0	0	0
BCK2FltHP	0	0	0	0	0	0
BCK1FltHP	0	0	0	0	0	0

FIELD	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
LDO3FltHP	0	0	0	0	0	0
FGExtSense	Yes	Yes	Yes	No	No	Yes

Register Defaults

Table 7 shows the default values of all the registers.

Table 7. I²C Direct Register Defaults

PERIPHERAL ADDRESS	REGISTER ADDRESS	REGISTER NAME	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
0x50	0x00	RevID	0x02	0x02	0x02	0x02	0x02	0x02
0x50	0x01	Status0	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x02	Status1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x03	Status2	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x04	Status3	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x05	Status4	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x07	Int0	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x08	Int1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x09	Int2	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x0A	Int3	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x0B	Int4	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x0C	Int5	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x0D	IntMask0	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x0E	IntMask1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x0F	IntMask2	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x10	IntMask3	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x11	IntMask4	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x12	IntMask5	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x13	ILimCtrl1	0x35	0x35	0x3D	0x3D	0x3D	0xB6
0x50	0x14	ILimCtrl2	0x63	0x63	0x63	0x60	0x60	0x21
0x50	0x16	DropCtrl	0x00	0x00	0x80	0x80	0x80	0x80
0x50	0x17	ChgCur0	0x46	0x46	0x45	0x30	0x30	0x05
0x50	0x18	ChgCur1	0x46	0x46	0x45	0x30	0x30	0x05
0x50	0x19	ChgCntl0	0xE4	0xE4	0xE2	0xE4	0xE4	0xE4
0x50	0x1A	ChgCntl1	0x45	0x45	0x85	0x85	0x85	0xC0
0x50	0x1B	ChgCntl2	0x43	0x43	0x42	0x46	0x36	0x74
0x50	0x1C	ChgTmr	0xDA	0xDA	0x8A	0x8A	0x85	0x8E
0x50	0x1D	ChgCfg0	0x30	0x30	0x10	0x10	0x10	0x30
0x50	0x1E	ThmCfg0	0x18	0x18	0x18	0x18	0x18	0x18
0x50	0x1F	TmnCfg1	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

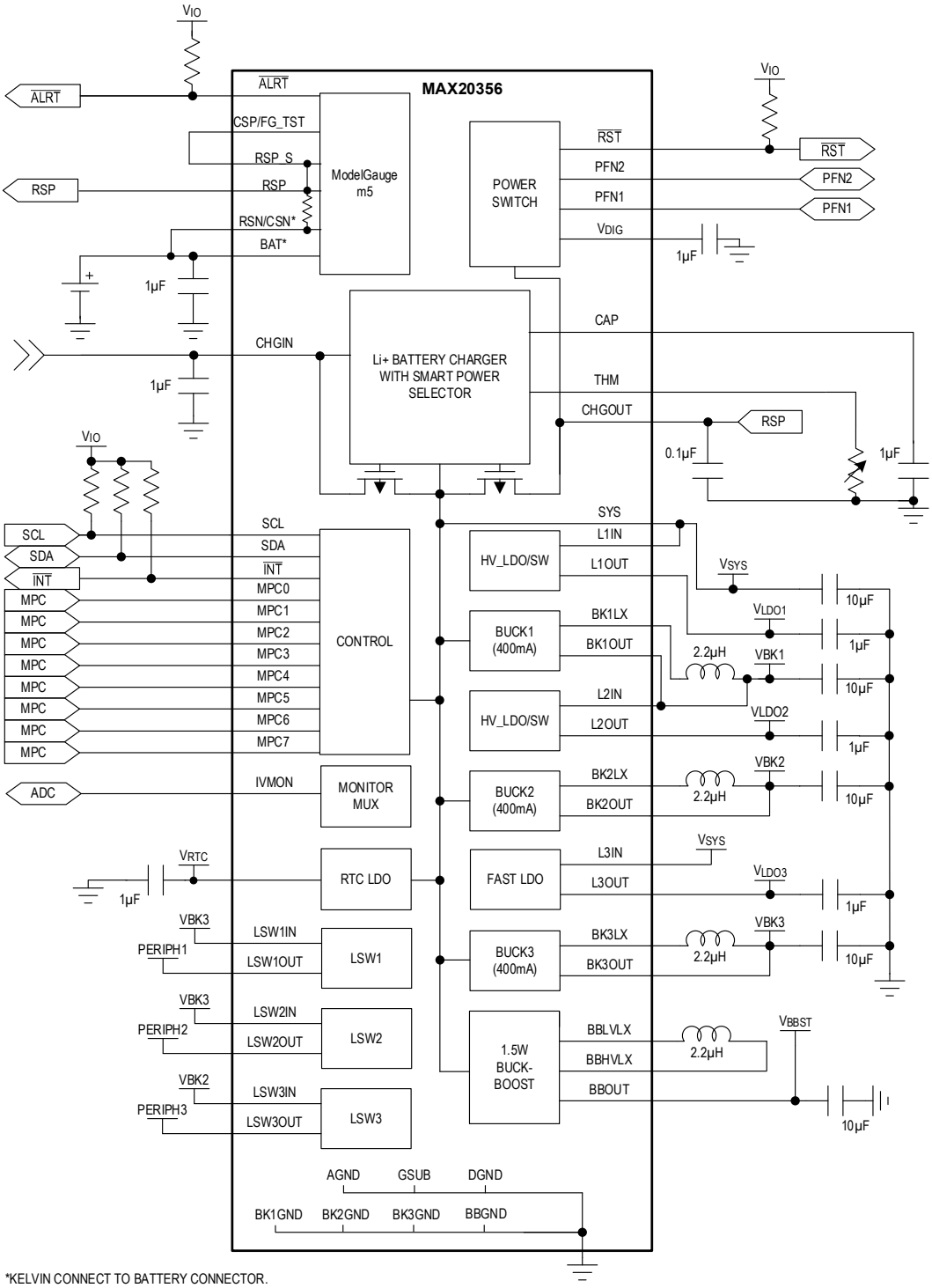
PERIPHERAL ADDRESS	REGISTER ADDRESS	REGISTER NAME	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
0x50	0x20	ThmCfg2	0x00	0x00	0x00	0x00	0x00	0x23
0x50	0x21	ThmCfg3	0x24	0x24	0x24	0x24	0x24	0x24
0x50	0x22	ThmCfg4	0x2D	0x2D	0x2D	0x2D	0x2D	0x2D
0x50	0x23	ThmCfg5	0x2D	0x2D	0x2D	0x2D	0x2D	0x2D
0x50	0x24	ThmCfg6	0x2D	0x2D	0x2D	0x2D	0x2D	0x2D
0x50	0x25	ThmCfg7	0xF1	0xF1	0xF1	0xF1	0xF1	0x43
0x50	0x26	ChgCtr1	0x80	0x80	0x80	0x80	0x80	0x80
0x50	0x27	ChgCtr2	0x01	0x01	0x01	0x01	0x01	0x01
0x50	0x28	HrvBatCfg0	0x10	0x10	0x30	0x30	0x30	0xC2
0x50	0x29	MONCfg	0x10	0x10	0x10	0x10	0x10	0x10
0x50	0x2A	WDCntl	0x03	0x03	0x03	0x03	0x03	0x03
0x50	0x30	Buck1Eba	0xE0	0xE0	0xE0	0xE0	0xE0	0xE0
0x50	0x31	Buck1Cfg0	0x50	0x50	0x50	0x50	0x50	0x50
0x50	0x32	Buck1Cfg1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x33	Buck1Iset	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x34	Buck1VSet	0x3C	0x3C	0x34	0x1A	0x04	0x34
0x50	0x35	Buck1Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x36	Buck1DvsCfg0	0x20	0x20	0x20	0x20	0x20	0x20
0x50	0x37	Buck1DvsCfg1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x38	Buck1DvsCfg2	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x39	Buck1DvsCfg3	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x3A	Buck1DvsCfg4	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x3B	Buck1DvsSpi	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x3C	Buck2Ena	0xE0	0xE0	0xE0	0x81	0x81	0xE0
0x50	0x3D	Buck2Cfg	0x51	0x51	0x50	0x50	0x50	0x50
0x50	0x3E	Buck2Cfg1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x3F	Buck2Iset	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x40	Buck2VSet	0x34	0x34	0x34	0x22	0x37	0x22
0x50	0x41	Buck2Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x42	Buck2DvsCfg0	0x20	0x20	0x20	0x20	0x20	0x20
0x50	0x43	Buck2DvsCfg1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x44	Buck2DvsCfg2	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x45	Buck2DvsCfg3	0x00	0x00	0x00	0x00	0x00	0x00

PERIPHERAL ADDRESS	REGISTER ADDRESS	REGISTER NAME	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
0x50	0x46	Buck2DvsCfg4	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x47	Buck2DvsSpi	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x48	Buck3Ena	0xE0	0xE0	0xE1	0x61	0x61	0xE0
0x50	0x49	Buck3Cfg	0x51	0x51	0x50	0x50	0x50	0x51
0x50	0x4A	Buck3Cfg1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x4B	Buck3Iset	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x4C	Buck3VSet	0x36	0x36	0x38	0x1A	0x1B	0x36
0x50	0x4D	Buck3Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x4E	Buck3DvsCfg0	0x20	0x20	0x20	0x20	0x20	0x20
0x50	0x4F	Buck3DvsCfg1	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x50	Buck3DvsCfg2	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x51	Buck3DvsCfg3	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x52	Buck3DvsCfg4	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x53	Buck3DvsSpi	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x54	BBstEna	0xE0	0xE0	0xE0	0xE0	0xE0	0xE0
0x50	0x55	BBstCfg	0x05	0x05	0x05	0x05	0x05	0x05
0x50	0x56	BBstVSet	0x32	0x32	0x32	0x32	0x32	0x28
0x50	0x57	BBstISet	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x58	BBstCfg1	0x13	0x13	0x13	0x13	0x13	0x33
0x50	0x59	BBstCtr0	0x08	0x08	0x08	0x08	0x08	0x08
0x50	0x5A	LDO1Ena	0xE0	0xE0	0xE0	0xE0	0xE0	0xE0
0x50	0x5B	LDO1Cfg	0x01	0x01	0x01	0x03	0x03	0x01
0x50	0x5C	LDO1VSet	0x00	0x00	0x09	0x09	0x09	0x09
0x50	0x5D	LDO1Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x5E	LDO2Ena	0xE0	0xE0	0xE1	0xE0	0xE0	0xE0
0x50	0x5F	LDO2Cfg	0x01	0x01	0x01	0x01	0x03	0x01
0x50	0x60	LDO2VSet	0x15	0x15	0x18	0x18	0x09	0x17
0x50	0x61	LDO2Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x62	LDO3Ena	0xE0	0xE0	0xE0	0xE0	0xE1	0xE0
0x50	0x63	LDO3Cfg	0x01	0x01	0x01	0x01	0x01	0x11
0x50	0x64	LDO3VSet	0x24	0x24	0x24	0x00	0x5C	0x22
0x50	0x65	LDO3Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x66	LDO4Ena	0xE0	0xE0	0xE0	0xE0	0x41	0xE0
0x50	0x67	LDO4Cfg	0x83	0x83	0x03	0x03	0x03	0x03
0x50	0x68	LDO4Ctr	0x00	0x00	0x00	0x00	0x00	0x00

PERIPHERAL ADDRESS	REGISTER ADDRESS	REGISTER NAME	EV KIT	EV KIT WITH HARVESTER	MAX20356A	MAX20356C	MAX20356D	MAX20356F
0x50	0x69	LSW1Ena	0xE0	0xE0	0xE0	0xE0	0xE0	0xE0
0x50	0x6A	LSW1Cfg	0x01	0x01	0x01	0x01	0x01	0x03
0x50	0x6B	LSW1Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x6C	LSW2Ena	0xE0	0xE0	0xE0	0xE0	0xE0	0xE0
0x50	0x6D	LSW2Cfg	0x01	0x01	0x01	0x01	0x01	0x03
0x50	0x6E	LSW2Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x6F	LSW3Ena	0xE0	0xE0	0xE0	0xE0	0xE0	0xE0
0x50	0x70	LSW3Cfg	0x01	0x01	0x03	0x03	0x03	0x03
0x50	0x71	LSW3Ctr	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x72	MPC0Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x73	MPC1Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x74	MPC2Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x75	MPC3Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x76	MPC4Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x77	MPC5Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x78	MPC6Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x79	MPC7Cfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x7A	MPCItrSts	0x00	0x00	0x04	0x06	0x06	0x00
0x50	0x7B	BK1ItrCfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x7C	BK2ItrCfg	0x00	0x00	0x00	0x80	0x80	0x00
0x50	0x7D	BK3ItrCfg	0x00	0x00	0x80	0x80	0x80	0x00
0x50	0x7E	USBOkItrCfg	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x80	PFN	0x01	0x01	0x01	0x01	0x01	0x01
0x50	0x81	BootCfg	0xBB	0xBB	0xB9	0xB9	0xB9	0x8F
0x50	0x82	PwrCfg	0x01	0x01	0x01	0x01	0x01	0x01
0x50	0x83	PwrCmd	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x84	MiscFunctions	0x04	0x04	0x04	0x04	0x06	0x02
0x50	0x86	LockMsk1	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
0x50	0x87	LockMsk2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
0x50	0x89	LockMsk3	0xEF	0xEF	0xEF	0xEF	0xEF	0xEF
0x50	0x8A	LockUnlock1	0x00	0x00	0x55	0x00	0x00	0x00
0x50	0x8B	LockUnlock2	0x00	0x00	0x55	0x00	0x00	0x00
0x50	0x8C	LockUnlock3	0x00	0x00	0x55	0x00	0x00	0x00
0x50	0x8D	I2C_OTP_ADD	0x00	0x00	0x00	0x00	0x00	0x00
0x50	0x8E	I2C_OTP_DAT	—	—	—	—	—	—

Typical Application Circuits

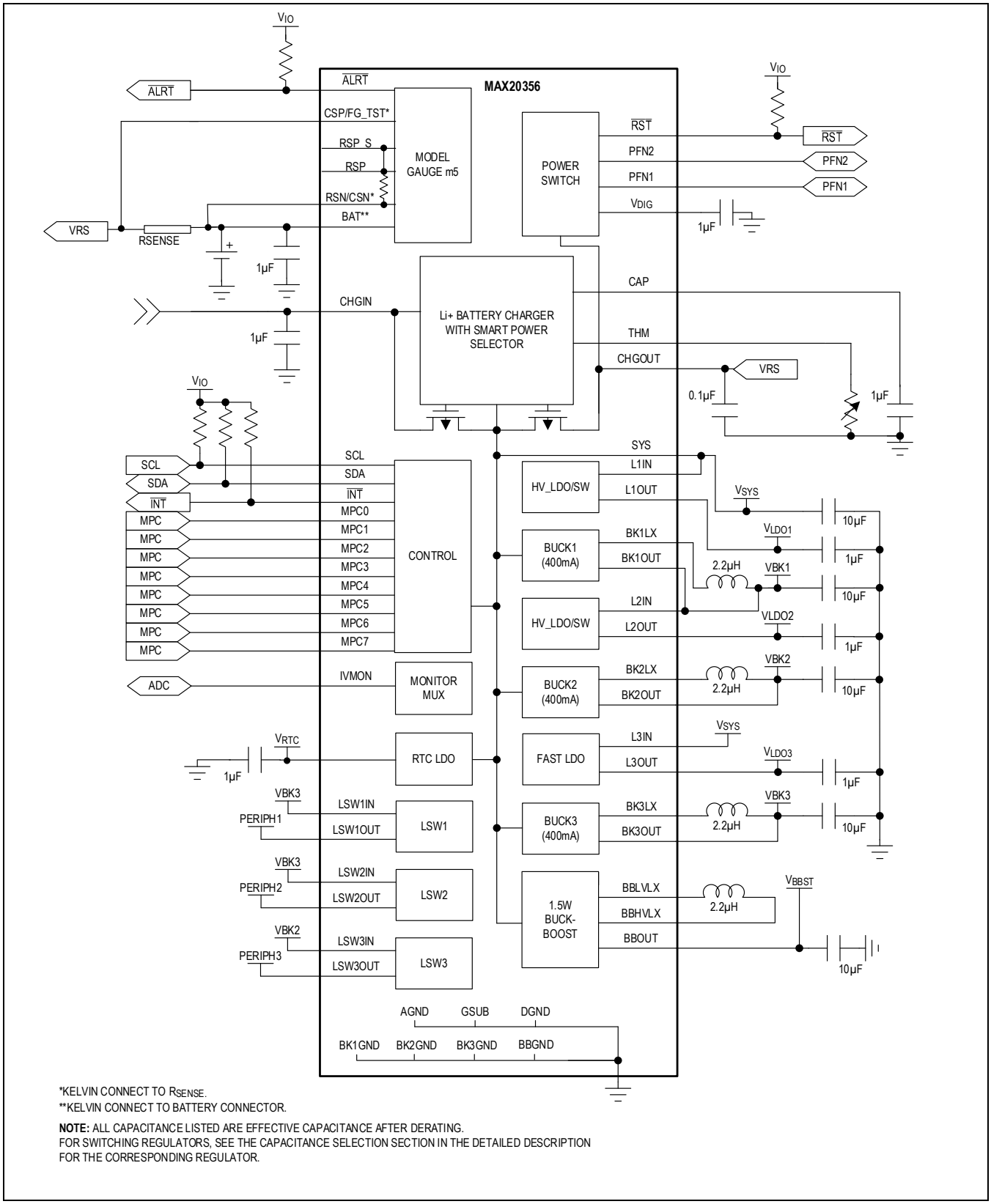
Internal Sense Resistor Case



*KELVIN CONNECT TO BATTERY CONNECTOR.

NOTE: ALL CAPACITANCE LISTED ARE EFFECTIVE CAPACITANCE AFTER DERATING. FOR SWITCHING REGULATORS, SEE THE CAPACITANCE SELECTION SECTION IN THE DETAILED DESCRIPTION FOR THE CORRESPONDING REGULATOR.

External Sense Resistor Case



*KELVIN CONNECT TO R_{SENSE}.
**KELVIN CONNECT TO BATTERY CONNECTOR.

NOTE: ALL CAPACITANCE LISTED ARE EFFECTIVE CAPACITANCE AFTER DERATING.
FOR SWITCHING REGULATORS, SEE THE CAPACITANCE SELECTION SECTION IN THE DETAILED DESCRIPTION FOR THE CORRESPONDING REGULATOR.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20356AEWY+	-40°C to +85°C	63-WLP
MAX20356AEWY+T	-40°C to +85°C	63-WLP
MAX20356CEWY+	-40°C to +85°C	63-WLP
MAX20356CEWY+T	-40°C to +85°C	63-WLP
MAX20356DEWY+	-40°C to +85°C	63-WLP
MAX20356DEWY+T	-40°C to +85°C	63-WLP
MAX20356FEWY+	-40°C to +85°C	63-WLP
MAX20356FEWY+T	-40°C to +85°C	63-WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/23	Initial release	—
1	4/24	Added decription in RTC LDO section. Update BAT-SYS FET to CHGOUT-SYS FET. Update CSR1 10s. Update MiscFunc[2] OTP bit to MiscFunc[2] bit. Update BAT to SYS to CHGOUT to SYS. Update bit name WDTmr in Watchdog Timer section. Updated bits description in register map: SCLDO3, ChgTmr, ThmPUSel, ThmEn, HrvFreeMPC, MONCtr, LDO3_MPC_CNF, PwrCmd, MiscFunc[0], BBLck. Updated MiscFunc[1] values in Table 6. Add MAX20356CEWY+, MAX20356CEWY+T, MAX20356DEWY+, and MAX20356DEWY+T to Table 6, Table 7, and Ordering Information.	52, 61-69, 70, 74, 79, 88, 99, 114, 119, 121, 122, 152, 172, 173, 181-188, 191
2	6/24	Updated Internal Switchover for LDO1 Always-On Power and Fast Transient LDO section. Updated Figure 13-21. Updated NewReset/Key Press Feature section. Add MAX20356FEWY+, and MAX20356FEWY+T to Table 6, Table 7, and Ordering Information.	51, 61-69, 76, 181-188, 191

Mouser Electronics

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Analog Devices Inc.:

MAX20356AEWY+T