

**MAX20094/MAX20095****Backup Battery Charger and Boost Controller****General Description**

The MAX20094/MAX20095 ICs combine a configurable constant-current/constant-voltage (CC/CV) battery charger with a high-efficiency synchronous boost controller to supply critical systems in the event the primary power source is lost. In addition, diagnostic features are available to check battery state-of-health (SOH) and IC functionality. Charging thresholds and the boost output voltage are configurable to support popular battery chemistries and a wide range of cell counts. To support system integration, the ICs have an I<sup>2</sup>C target port through which configuration and status bits can be accessed.

Switching frequency of 2.2MHz also helps to reduce system cost by minimizing inductor size. The ICs also include a precision battery SOH check and have built-in functionality to minimize leakage current out of the backup battery (BUB).

The MAX20094/MAX20095 are available in a 28-pin (5mm x 5mm) side-wettable TQFN package and are AECQ-100 qualified.

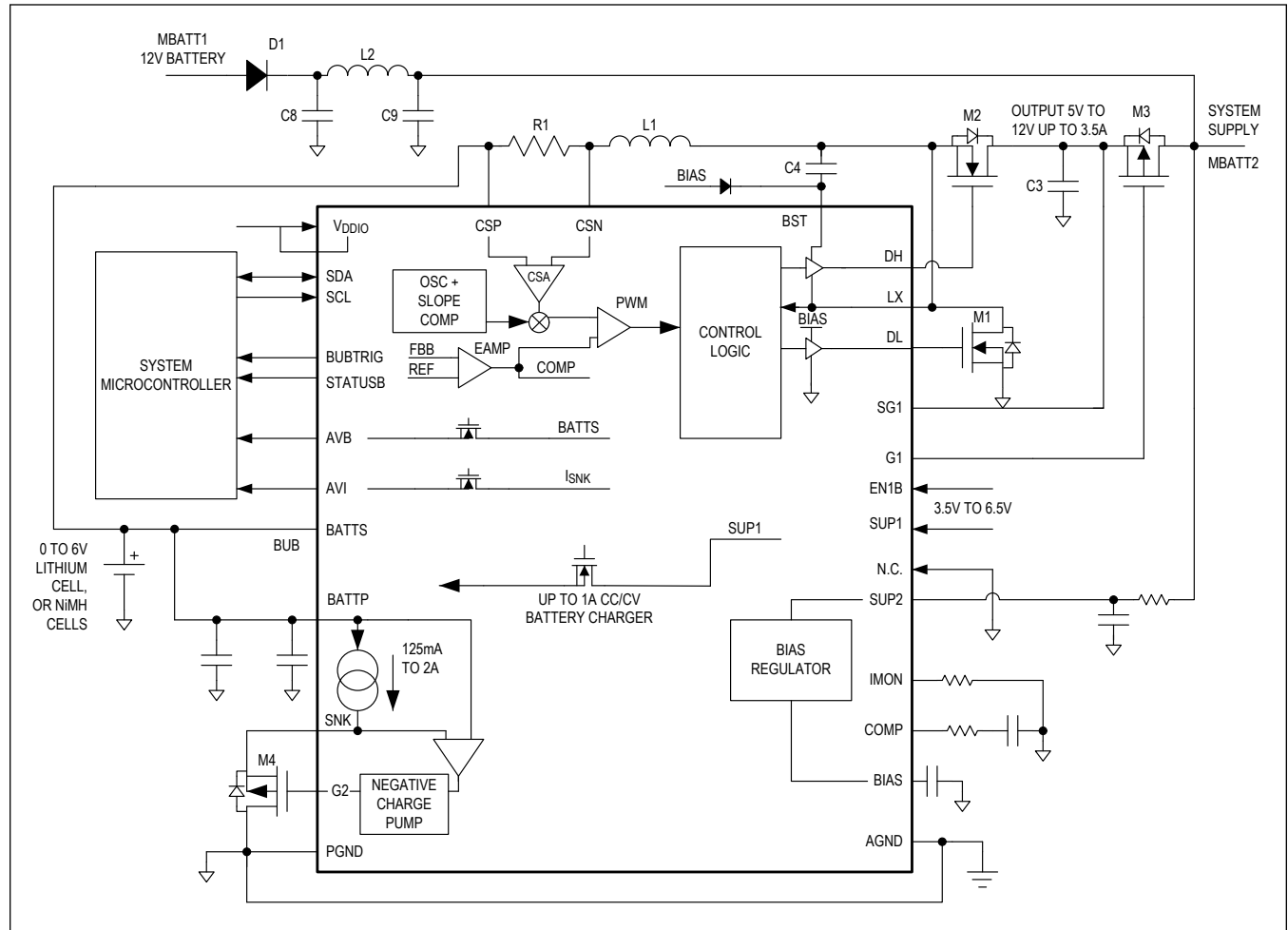
**Applications**

- Automotive Telematics Battery Backup
- Single or Multicell Battery-Backup Systems

**Benefits and Features**

- Efficient Solution
  - Minimum 2V Sync Boost with n-Channel FET Control
  - Skip Mode Guarantees > 50% Efficiency at 1mA
- Multiple Functions to Enable Small Solution Size
  - 3V to 6V CC/CV Battery Charger
  - I<sup>2</sup>C-Settable Charging Current up to 1A
  - I<sup>2</sup>C-Selectable CV Voltage and CC Current Levels
  - Gate-Driver Output for p-Channel Load Disconnect
  - Backup Battery Switchover-Trigger Signal
- State-of-Health for Backup Battery Monitoring
  - I<sup>2</sup>C Interface Diagnostics and Control Interface
  - Accurate Internal Current Sink for Battery Impedance Measurement
  - Analog Readout of Internal Sink Current from Backup Battery
  - Remote Sense for BATT\_ Voltage Measurement
- Robust for Automotive Environment
  - 3.5V to 36V V<sub>IN</sub> (40V Load-Dump Tolerant)
  - < 1μA Leakage for Pins Connected to the Battery
  - -40°C to +125°C Operating Temperature Range
  - 28-Pin, Side-Wettable TQFN Package Enables Optical Inspection

## Simplified Block Diagram



## Absolute Maximum Ratings

SUP2, DH, LX, SG1, CSP, CSN to PGND ..... -0.3V to +40V  
 G1 to SG1 ..... -7.0V to +0.3V  
 BST to LX ..... -0.3V to +6V  
 CSP to CSN ..... -0.3V to +0.3V  
 AVI, BUBTRIG, DL, COMP,  
 IMON to AGND ..... -0.3V to  $V_{BIAS} + 0.3V$   
 SCL, SDA to AGND ..... -0.3V to  $V_{DDIO} + 0.3V$   
 PGND to AGND ..... -0.3V to +0.3V  
 EN1B, BIAS, VDDIO, STATUSB to AGND ..... -0.3V to +6V

BATTP, SNK, BATTs, SUP1 to AGND ..... -0.3V to +7.0V  
 AVB to AGND ..... -0.3V to  $V_{BATTs} + 0.3V$   
 G2 to BATTP ..... -6.0V to +0.3V  
 Operating Temperature Range ..... -40°C to +125°C  
 Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -40°C to +150°C  
 Soldering Temperature (reflow) ..... +260°C  
 ESD Protection - Human Body Model ..... ±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 28-Pin (5mm x 5mm x 0.75mm) Side-Wettable TQFN

Package Code	T2855Y+5C
Outline Number	<a href="#">21-100130</a>
Land Pattern Number	<a href="#">90-0027</a>
<b>THERMAL RESISTANCE, SINGLE-LAYER BOARD</b>	
Junction to Ambient ( $\theta_{JA}$ )	48°C/W
Junction to Case ( $\theta_{JC}$ )	3°C/W
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction to Ambient ( $\theta_{JA}$ )	35°C/W
Junction to Case ( $\theta_{JC}$ )	3°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{SUP1} = 4V$ ,  $V_{SUP2} = 14V$ ,  $V_{BATTP} = V_{BATTs} = 3.5V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BOOST CONTROLLER</b>						
Supply Voltage Range	$V_{SUP2}$	Normal operation	4.5		36	V
		$t < 1s$			40	
Backup Battery Undervoltage-Lockout Threshold	BUB_UVLO	Contact factory for options			2	V
Shutdown Supply Current	$I_{SUP2}$	Boost disabled through I <sup>2</sup> C, $V_{SUP2} = 12V$ , $V_{EN1B} = 0V$			10	μA

## Electrical Characteristics (continued)

( $V_{SUP1} = 4V$ ,  $V_{SUP2} = 14V$ ,  $V_{BATTP} = V_{BATTS} = 3.5V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$I_{SUP2\_STB}$	BOOST I <sup>2</sup> C bit enabled, $V_{EN1B} = 0V$ , $V_{SUP1} = 0$ to $6V$ , $V_{SUP2} = V_{SG1} = 14V$ , no switching		26	55	$\mu A$
Boost Mode Fixed-Output Voltage	$V_{SUP2}$	$V_{SUP2}$ is factory-programmable	6.076	6.2	6.355	V
			6.37	6.5	6.663	
			6.664	6.8	6.97	
			6.958	7.1	7.278	
			5.39	5.5	5.7	
			7.84	8	8.20	
			8.82	9	9.27	
			9.8	10	10.25	
			11.76	12	12.30	
Boost Output Overvoltage - Falling Threshold (Boost Wakes Up Below this Threshold)	$BOOST\_OV\_F$		104	107	110.5	%
Boost Output Overvoltage - Falling Hysteresis				6		%
Boost Output Overvoltage - Rising Threshold (Boost Enters Sleep Mode Above this Threshold)	$V_{SUP2\_R}$		110	113	116	%
Boost Output Undervoltage Lockout	$BST\_UVLO$	Falling		65		%
		Rising		85		
Transconductance (from FBB to COMP)	$g_m$	$V_{BIAS} = 5.5V$ ( <a href="#">Note 2</a> )		250		$\mu S$
G1 Drive Strength	G1	$V_{SG1} = 6.8V$ , G1 not active		1.75		k $\Omega$
G1 Activation Time		5nF MOSFET capacitance from SG1 to G1, OV falling until G1 reaches 4.5V below SG1; boost is ready to run within 10 $\mu s$ (typ) once $BOOST\_OV\_F$ is tripped		10	50	$\mu s$
Dead Time		DL low to DH rising		20		ns
		DH low to DL rising		20		
Minimum On-Time	$t_{ON,MIN}$			120		ns
Minimum Off-Time	$t_{OFF,MIN}$			60		ns
PWM Switching-Frequency Range	$f_{SW}$		1.9	2.1	2.3	MHz
			0.36	0.4	0.44	
CS_ Current Limit	$V_{LIMIT}$	$V_{CSP} - V_{CSN}$	40	50	60	mV
LX Leakage Current		$V_{LX} = V_{PGND}$ or $V_{IN}$ , $T_A = +25^{\circ}C$			1	$\mu A$
DH Pull-Up Resistance		$V_{BIAS} = 5V$ , $I_{DH} = -100mA$		3	6	$\Omega$

**Electrical Characteristics (continued)**

( $V_{SUP1} = 4V$ ,  $V_{SUP2} = 14V$ ,  $V_{BATTP} = V_{BATTS} = 3.5V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH Pull-Down Resistance		V <sub>BIAS</sub> = 5V, I <sub>DH</sub> = 100mA		1.5	3	Ω
DL Pull-Up Resistance		V <sub>BIAS</sub> = 5V, I <sub>DL</sub> = -100mA		3	6	Ω
DL Pull-Down Resistance		V <sub>BIAS</sub> = 5V, I <sub>DL</sub> = 100mA		1.5	3	Ω
INTERNAL LDO BIAS						
Internal BIAS Voltage		V <sub>SUP2</sub> > 6V		5		V
BIAS UVLO Threshold		V <sub>BIAS</sub> rising		3.0	3.25	V
		V <sub>BIAS</sub> falling	2.35	2.5		
BATTERY CHARGER						
Supply Voltage Range	V <sub>SUP1</sub>		0		6.5	V
Supply Undervoltage Threshold, Falling	V <sub>SUP1_UV</sub>		3.3			V
Supply Undervoltage Threshold, Rising	V <sub>SUP1_UV_R</sub>				3.5	V
Supply Leakage Current	I <sub>SUP1</sub>	Charger disabled, T <sub>A</sub> = +25°C			10	μA
SUP1 to BATTP On-Resistance	R <sub>CHG</sub>	V <sub>SUP1</sub> = 3.5V, V <sub>BATTP</sub> = 3.45V		250	500	mΩ
I <sup>2</sup> C Control BUB Voltage Setting	V <sub>CVTHR</sub>	I <sup>2</sup> C control	3.0		6.0	V
BUB Voltage Range	V <sub>BATT_</sub>		0.0		6.0	V
Output-Voltage Accuracy	V <sub>BATT_</sub>	V <sub>CVTHR</sub> = 3.6V	-1.2		+1	%
Fast-Charging Current Setting		I <sup>2</sup> C settable	0.05		1	A
Precharge Current		V <sub>BUB</sub> = 0 to 2.0V	40	50	60	mA
Fast-Charge Current Accuracy		V <sub>SUP1</sub> = 3.5V to 6.5V, 250mA < I <sub>FCHG</sub> < 1A	-10		+10	%
		V <sub>SUP1</sub> = 3.5V to 6.5V, 50mA < I <sub>FCHG</sub> < 250mA	-20		+20	
Charger Restart-Voltage Threshold		Voltage drop below V <sub>CVTHR</sub> for FAST_CHR_CC to resume		200		mV
Soft-Start Time		I <sup>2</sup> C enables the charger, fast-charge current of 90% of final value; EN1B going from high to low automatically enables the charger, as long as the I <sup>2</sup> C register is set			1	ms
BATTP Leakage Current	I <sub>BATTP</sub>	Not boosting, and/or charger disabled, and/or unpowered (V <sub>BATT_</sub> > V <sub>SUP1</sub> ), T <sub>A</sub> = +25°C			1	μA
Fast Shut-Off		V <sub>EN1B</sub> = low to high, overrides I <sup>2</sup> C, fast-charge current of < 50mA			5	μs
Minimum Charger Output Capacitance		Backup battery not present	1			μF

**Electrical Characteristics (continued)**

( $V_{SUP1} = 4V$ ,  $V_{SUP2} = 14V$ ,  $V_{BATTP} = V_{BATTS} = 3.5V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IMON Gain				440		A/A
Thermal-Limit Temperature	$T_{LIM}$	Junction temperature when the charge current is reduced, $T_J$ rising		145		$^{\circ}C$
<b>THERMAL OVERLOAD</b>						
Thermal-Shutdown Temperature		( <a href="#">Note 2</a> )		170		$^{\circ}C$
Thermal-Shutdown Hysteresis		( <a href="#">Note 2</a> )		20		$^{\circ}C$
<b>BATTERY STATE-OF-HEALTH CURRENT SINK</b>						
SNK Current Range	$I_{SNK}$	I <sup>2</sup> C control	0		2	A
SNK Current Accuracy		$I_{SNK} = 0.5A$ , $V_{BATT\_} = 3.3V$	-10		+10	%
SNK Current-Measurement Accuracy	$V_{AVI}$	$I_{SNK} = 0.5A$ , $V_{BATT\_} = 3.3V$	-7.5	1	+7.5	%
Sink Current-Measurement Voltage Range	$V_{AVI}$	$I_{SNK} = 0$ to 2A	0		3	V
BUB Voltage-Measurement Range	$V_{AVB}$	$V_{BATTS} = 0$ to 6V	0		6	V
Resistance of AVB Pass Switch		BATT_ <sub>-</sub> to AVB			10	$\Omega$
G2 Drive-Current Capability	$I_{G2}$		7			$\mu A$
BATTS Leakage Current	$I_{BATTS}$	$T_A = +25^{\circ}C$			1	$\mu A$
SNK Leakage Current	$I_{SNK}$	$T_A = +25^{\circ}C$			1	$\mu A$
G2 Output Low Voltage	$V_{G2\_OL}$	$I_{G2\_SINK} = 5\mu A$			-3	V
BATTS Undervoltage Threshold, Falling					2.5	V
<b>DIGITAL INPUT CHARACTERISTICS (SCL, SDA)</b>						
Input High Threshold	$V_{IH}$	$2.5V \leq V_{DDIO} \leq 5.5V$	$0.7 \times V_{DDIO}$			V
Input Low Threshold	$V_{IL}$	$2.5V \leq V_{DDIO} \leq 5.5V$			$0.3 \times V_{DDIO}$	V
Input Threshold Hysteresis	$V_{HYS}$		0.15			V
Input Leakage Current	$I_{IN}$	$V_{IN} = 0V$ or $V_{DDIO}$ , $T_A = +25^{\circ}C$			1	$\mu A$
Input Capacitance	$C_{IN}$				10	pF
<b>DIGITAL INPUT CHARACTERISTICS (EN1B)</b>						
Input High Threshold	$V_{IH}$	$2.5V \leq V_{BIAS} \leq 5.5V$	1.4			V
Input Low Threshold	$V_{IL}$	$2.5V \leq V_{BIAS} \leq 5.5V$			0.5	V
Input Leakage Current	$I_{IN}$	$V_{IN} = 0V$ or $V_{BIAS}$ , $T_A = +25^{\circ}C$			1	$\mu A$
<b>DIGITAL OUTPUT CHARACTERISTICS (SDA, STATUSB, BUBTRIG)</b>						
Output High Voltage	$V_{OH}$	Applies only to BUBTRIG CMOS output, $I_{SOURCE} = 1mA$	$V_{BIAS} - 0.15$	$V_{BIAS} - 0.06$		V

**Electrical Characteristics (continued)**

( $V_{SUP1} = 4V$ ,  $V_{SUP2} = 14V$ ,  $V_{BATTP} = V_{BATTS} = 3.5V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) ([Note 1](#))

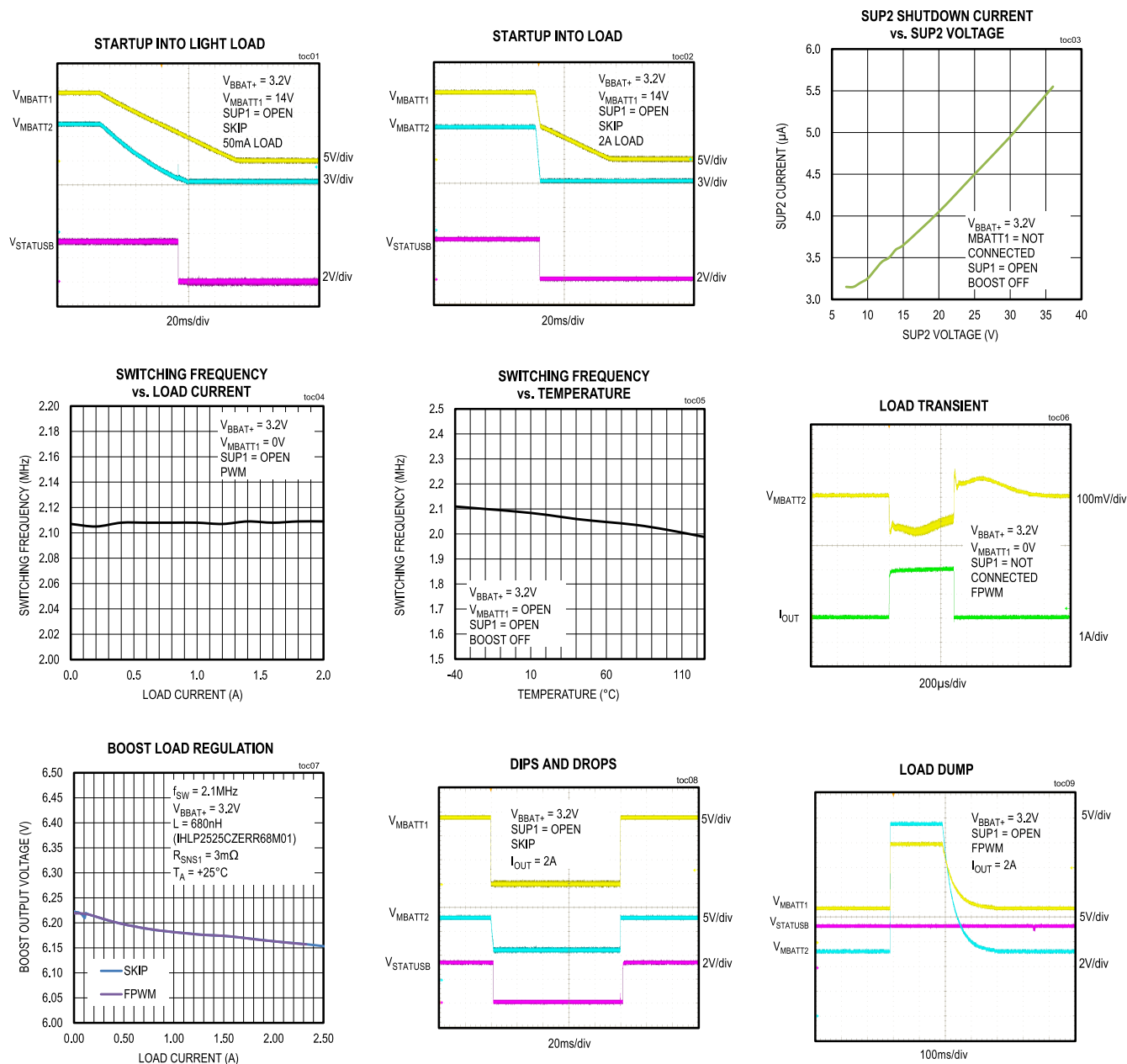
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage	$V_{OL}$	Applies to SDA, STATUSB, and BUBTRIG; $I_{SNK} = 1mA$			0.2	V
Output Inactive-Leakage Current	$I_{OFF}$	Applies only to STATUSB open-drain output (see $I_{IN}$ for SDA)			$\pm 1$	$\mu A$
Output Inactive Capacitance	$C_{OFF}$	Applies only to STATUSB open-drain output (see $C_{IN}$ for SDA)			10	pF
Backup Battery-TriggerPulse Width	$t_{BUBTRIG}$	BOOST enabled and $SUP2 < BOOST\_OV\_F$	180	200	220	ms
<b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS (SCL, SDA)</b>						
SCL Clock Frequency	$f_{SCL}$		0		400	kHz
Bus-Free Time Between a STOP and START Condition	$t_{BUF}$		1.3			$\mu s$
Hold Time for a Repeated START Condition	$t_{HD;STA}$		0.6			$\mu s$
SCL Pulse Width Low	$t_{LOW}$		1.3			$\mu s$
SCL Pulse Width High	$t_{HIGH}$		0.6			$\mu s$
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			$\mu s$
Data Hold Time	$t_{HD;DAT}$		0		900	ns
Data Setup Time	$t_{SU;DAT}$		100			ns
SDA and SCL Receiving Rise Time	$t_R$	Incoming signals (from controller)	$20 + C_B/10$		300	ns
SDA and SCL Receiving Fall Time	$t_F$	Incoming signals (from controller)	$20 + C_B/10$		300	ns
SDA Transmitting Fall Time	$t_F$		$20 + C_B/10$		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			$\mu s$
Bus Capacitance Allowed	$C_B$	$2.5V \leq V_{DDIO} \leq 5.5V$	0		900	pF
Pulse Width of a Suppressed Spike		Width of spikes that must be suppressed by the input filter of both SDA and SCL signals		50		ns

**Note 1:** Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 2:** Guaranteed by design; not production tested.

## Typical Operating Characteristics

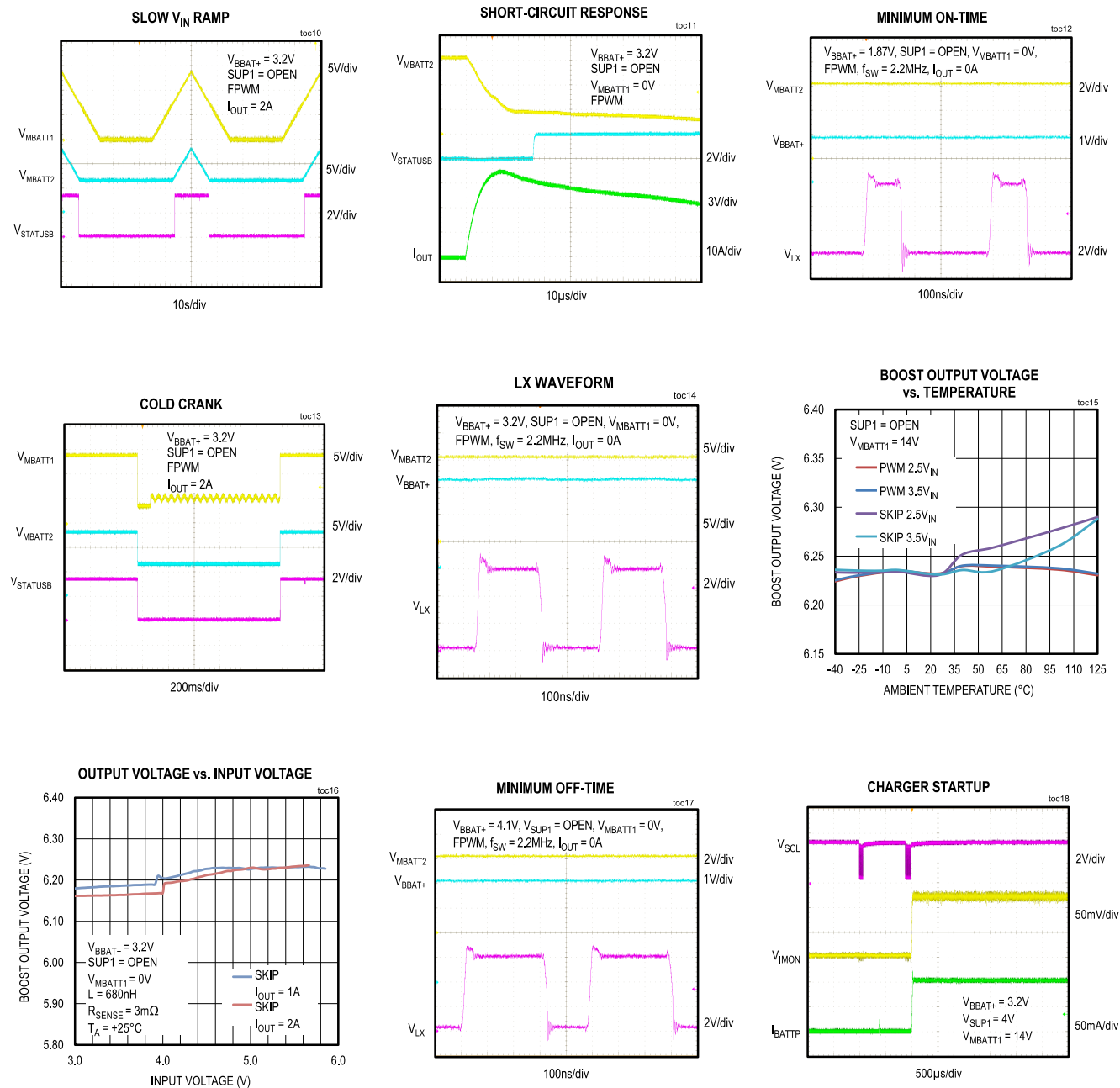
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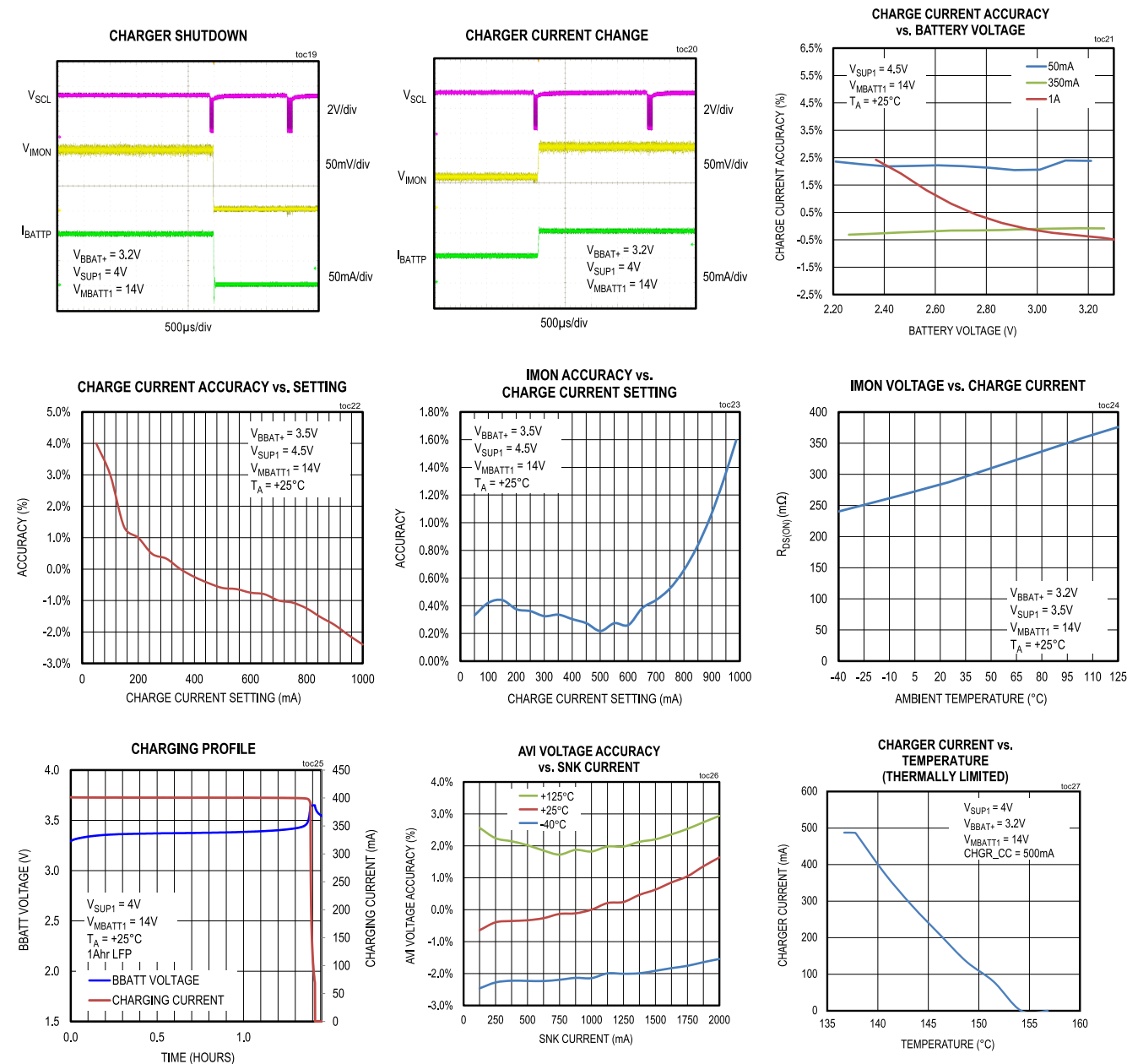
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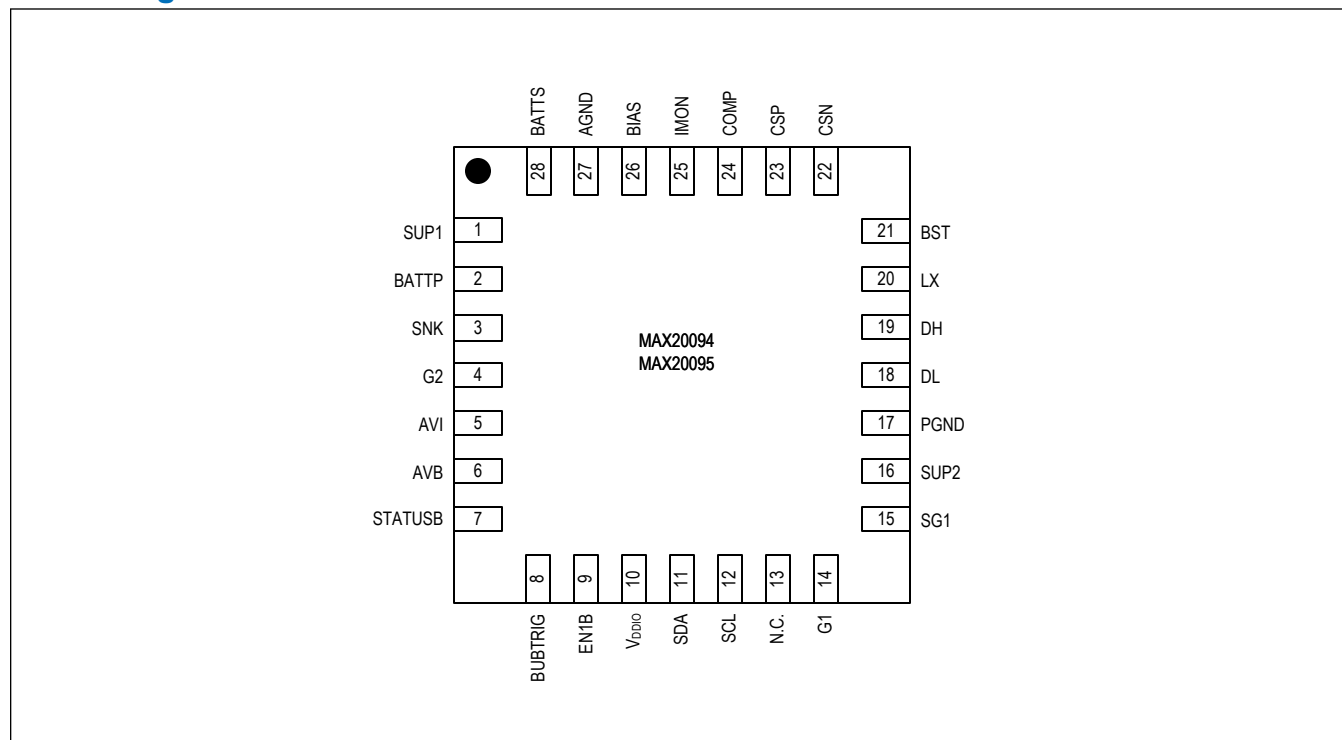


## Typical Operating Characteristics (continued)

( $V_{SUP1} = 4V$ ,  $V_{SUP2} = 14V$ ,  $V_{BATTP} = V_{BATTS} = 3.5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Configuration



## Pin Description

PIN	NAME	FUNCTION
1	SUP1	Input to the CC/CV Charger. Connect a 2.2μF ceramic capacitor from SUP1 to the ground plane.
2	BATTP	Charger Output for the Backup Battery (BUB). BATTP is the current sink for the battery state-of-health (SOH) check. Place a 10μF, 2.2μF, and 0.1μF ceramic capacitor as close as possible to the SUP2 pin. See the <a href="#">PCB Layout Recommendations</a> section for details on trace sizing to BATTP.
3	SNK	Connection for the Source of the External MOSFET (M4) for State-of-Health (SOH) Measurements. The SNK pin sinks the preset current from the BUB to the external MOSFET during SOH measurements.
4	G2	Gate Drive to Turn on the MOSFET (M4) and Sink Current into the IC. This function is controlled by I <sup>2</sup> C. G2 is not connected when the discharger is disabled. When the discharger is enabled, G2 is driven to BATTP for 62μs (typ) before the circuit starts up.
5	AVI	Analog Voltage Measurement for SNK Current Set During SOH Measurement. There is a 30kΩ pull-down resistor when AVI is disabled.
6	AVB	Analog Battery Voltage-Measurement Output During SOH Measurements. There is a 60kΩ pull-down resistor connected 10μs before the AVB switch is turned off through I <sup>2</sup> C.
7	STATUSB	STATUSB (Battery Boost) Default Open-Drain Output. Driven to AGND during boost operation due to loss of primary power; otherwise, high impedance.
8	BUBTRIG	Backup Battery-Active Timed Output. Driven to BIAS for 200ms following backup boost controller start of operation; otherwise, driven to AGND.
9	EN1B	Charger Disable. EN1B is connected to ground during normal operation. If pulled high, the charger is disabled, regardless of the I <sup>2</sup> C register setting.
10	VDDIO	I <sup>2</sup> C Logic Interface Supply Voltage, 2.5V to 5.5V. Connect to the I <sup>2</sup> C bus supply.
11	SDA	I <sup>2</sup> C Data Signal

## Pin Description (continued)

PIN	NAME	FUNCTION
12	SCL	I <sup>2</sup> C Clock Input
13	N.C.	Connect to GND in the Application
14	G1	High-Side p-Channel MOSFET (M3) Driver. There is a 188kΩ resistor between G1 and SG1.
15	SG1	Source of the External p-Channel MOSFET (M3). SG1 and G1 control the gate drive of external MOSFET M3.
16	SUP2	System Supply Voltage Input. High-voltage-tolerant input to the LDO, which generates 5V supply for the IC. Connect a resistor and capacitor filter from the battery-filtered rail and SUP2. See the <a href="#">Applications Information</a> section for more details.
17	PGND	Power Ground Pin. Connect directly to the PCB ground plane.
18	DL	Low-Side MOSFET Driver Output. Connect to the gate of the boost converter's low-side MOSFET.
19	DH	High-Side MOSFET Driver Output. Connect to the boost converter's high-side MOSFET.
20	LX	Switching Node of DC-DC Controller
21	BST	Boosted Supply Voltage for the High-Side Sync MOSFET Gate Drive
22	CSN	Current-Sense Resistor, Inductor-Side Sense Point. Connect CSN as close as possible to the current-sense resistor terminal. See the <a href="#">PCB Layout Recommendations</a> section for details on proper layout.
23	CSP	Current-Sense Resistor Input Pin. Connect CSP as close as possible to the current-sense resistor for accurate current sensing. See the <a href="#">PCB Layout Recommendations</a> section for details on proper layout.
24	COMP	Loop-Compensation Component Connection Pin. COMP is the output of the internal g <sub>m</sub> amplifier. Connect a resistor in series with a capacitor to the AGND pin. The component values are selected according to the data sheet recommendations.
25	IMON	Connect IMON to GND with a 500Ω Resistor. $V_{IMON} = (I_{CHG}/440) \times 500\Omega$ . $Max R_{IMON} = (V_{BATTP(MIN)} - 0.25)/(0.0025I_{CHG}) - 200$ .
26	BIAS	Supply Pin for the Internal IC Circuits. This pin should be decoupled with a 2.2μF capacitor. BIAS is the output of the LDO connected to the V <sub>SUP_</sub> pin, and is used to supply the internal circuitry with 5V.
27	AGND	Analog Ground. Low-noise ground for precision circuit blocks.
28	BATTS	Battery Voltage-Sensing Input. Senses the battery voltage for the voltage-feedback loop and routes to the internal analog switch. Connect BATTS as close as possible to the battery's positive terminal for the most accurate voltage sensing of the battery.
—	EP	Exposed Pad

## Detailed Description

The MAX20094/MAX20095 ICs combine a configurable constant-current/constant-voltage (CC/CV) battery charger, with a high-efficiency synchronous boost controller to supply critical systems in the event the primary power source is lost. In addition, diagnostic features are available to check battery state-of-health (SOH) and IC functionality. Charging thresholds and the boost output voltage are configurable to support popular battery chemistries and a wide range of cell counts. To support system integration, the ICs have an I<sup>2</sup>C target port through which configuration and status bits can be accessed.

### BIAS Linear Regulator

An internal 5V linear regulator (BIAS) generates a bias supply for the internal circuitry. Bypass BIAS with a 2.2μF or greater ceramic capacitor to guarantee stability under the full-load condition.

The BIAS input undervoltage-lockout (UVLO) circuitry inhibits boost operation, charging, or SOH if the 5V bias supply (BIAS) is below its 2.5V (typ) UVLO falling threshold. Once the 5V bias supply (BIAS) rises above its UVLO rising threshold and the block control logic conditions are met, the ICs are functional.

### Block Control Logic

The logic governing the operation of the boost controller, battery charger, and SOH is summarized in [Table 1](#).

**Table 1. Block Control Logic**

BLOCK	COMMENTS
SOH	SOH is enabled when: <ul style="list-style-type: none"> <li>• I<sup>2</sup>C register bit is set</li> <li>• Boost is not regulating</li> <li>• Not in thermal-shutdown condition</li> </ul>
Boost	Boost is enabled/regulating when: <ul style="list-style-type: none"> <li>• I<sup>2</sup>C register bit is set</li> <li>• SUP2 is below OV_F threshold</li> <li>• Not in thermal-shutdown condition</li> </ul> <b>Note:</b> When boost is regulating, SOH and charger functions are disabled.
Charger	Charger is enabled when: <ul style="list-style-type: none"> <li>• I<sup>2</sup>C register bit is set and EN1B pin = 0</li> <li>• Boost is not regulating</li> <li>• Not in thermal-shutdown condition</li> </ul> <b>Note:</b> While enabled, the charger mode progression is controlled by an internal state machine and associated comparators.

## Logic Equations

### STATUSB Pin

The STATUSB pin is an open-drain, active-low nMOS output pin that can be used in a shared-interrupt configuration with a μC controller, and any number of similarly configured target devices (using a wired-OR configuration with an external pull-up resistor to a suitable supply, typically V<sub>DDIO</sub>). Under default conditions, the STATUSB pin is active when the boost is actively regulating SUP2. The function of the STATUSB pin can be changed to provide other types of operation using the I<sup>2</sup>C interface (see the GEN\_STATUS and EN\_INT registers).

### Charger Block

The normal operating mode of the ICs is to maintain charge on the backup battery (BUB). This function is provided by the charger block (see [Figure 1](#)).

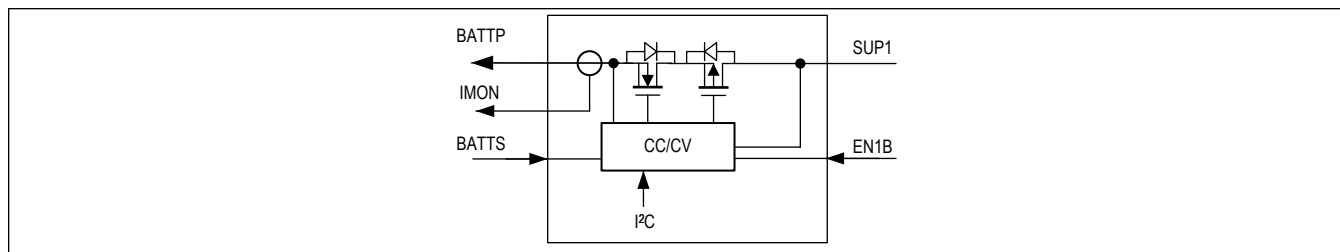


Figure 1. Charger Block Diagram

### Charger State Machine Description

Once enabled, the charger operation is governed by a state machine, described below and detailed in [Figure 2](#). The real-time operation of the charger can be read back using the CHGR\_STATUS (01\h) register.



The charger is held in an OFF state when CONTROL/CHG\_EN=0, or START\_BIASRDY=0, or the die temperature is above the thermal-shutdown threshold. Once CONTROL/CHG\_EN=1, bias has been established (START\_BIASRDY=1) and the die temperature is below the thermal-shutdown threshold (START\_THMSD=0), the charger moves to standby mode, and a 15 $\mu$ s timer is started, allowing the charger's internal biases and comparators to settle.

The charger remains in standby mode until internal biases are established (based on the startup timer) and supply conditions are checked and found to be valid. The charger returns to standby mode in the event of an invalid supply

condition. Supply conditions can be verified in real time using the CHGR\_STATUS (01\h) register. A supply condition alert is also available in GEN\_STATUS (02\h).

### Prequal

The charger next moves to a 50mA current-limited charging mode (PREQUAL). The charger remains in this mode until  $V_{BUB}$  exceeds  $V_{PQVTHR}$ . For  $V_{PQVTHR}$  settings, see the [Ordering Information](#) table.

### Constant-Current (CC)

The charger now begins the fast-charging procedure, beginning in a constant-current mode (FAST\_CHG\_CC). Charge current is programmed using the CHGR\_CC (05\h) register. The charger remains in fast charging until  $V_{BUB}$  exceeds  $V_{CVTHR}$  and returns to FAST\_CHG\_CC if  $V_{BUB}$  falls below  $V_{CVTHR}$ , which is selected using the CHGR\_CV (06\h) register. If 50mA setting is used, first enable the charger, then set CHGR\_CC to 100mA or greater for at least 1ms before switching down to 50mA.

### Constant-Voltage (CV)

When  $V_{BUB}$  exceeds  $V_{CVTHR}$ , the charger continues charging in a constant-voltage mode (FAST\_CHG\_CV). A constant-voltage-mode alert is available in GEN\_STATUS (02\h), notifying the user that charging is nearing completion. Once the charger has moved to FAST\_CHG\_CV mode, the charger current is monitored. If  $I_{CHG}$  falls below 50mA, the fast-charging operation is completed and the charger moves to FAST\_CHG\_DONE mode. The charger remains in this mode until it is disabled by the user (returning to OFF), a supply fault condition occurs (returning to STANDBY), or  $V_{BUB}$  falls below  $V_{CVTHR} - 200mV$  (returning to FAST\_CHG\_CC). After entering the DONE state, a charging-done alert is available in GEN\_STATUS (02\h), notifying the user that charging is completed. If the charger is restarted during CV, set CHGR\_CC to 50mA before enabling the charger. CHGR\_CC can be increased to the desired setting after the charger is enabled.

### Done

If  $V_{SUP1}$  and  $V_{BUB}$  enter dropout, the charge current is reduced due to the  $R_{DS(ON)}$  of the internal MOSFET, and the voltage difference between  $V_{SUP1}$  and the battery. If charge current continues to decrease, the ALRT\_CV and CHGR\_MODE changes to show CV state. Once charge current reduces to 50mA, ALRT\_CV remains 1, ALRT\_DONE=1, and CHGR\_MODE goes to the DONE state. Use the following equation to estimate the amount of headroom required to stay out of dropout at maximum ambient temperature:

$$V_{Drop\_CHG} = 1.15 \times R_{CHG\_MAX} \times I_{FAST\_CHG\_CC}$$

where  $R_{CHG\_MAX}$  is the maximum value of  $R_{CHG}$  from the [Electrical Characteristics](#) table. When CONTROL/CHG\_EN=0, then CHRG\_STATUS/SUP1\_UVLO=1. This default condition is due to internal circuitry being turned off to minimize leakage.

### EN1B Pin

The EN1B pin is an active-low input port that controls the operation of the charger block. When the EN1B pin is held low, the charger operation is controlled by the I<sup>2</sup>C interface registers. When pulled high (usually due to an external system fault), the charger is instantly disabled and its internal state machine reset. The charger resumes normal operation once the pin is returned low.

### Boost Block

The boost block allows the ICs to maintain a regulated supply voltage on the SUP2 pin using the backup battery (BUB) in the event of a main-battery failure.

The boost is a synchronous current-mode controller with a factory-preset output voltage. The switching frequency is capable of greater than 2MHz. To enable longer battery life, the boost utilizes pulse-frequency modulation (PFM) mode at light load and automatically enters ultra-low  $I_Q$  standby mode when output voltage is above the required boost voltage. The boost automatically enters awake mode when the output voltage is at or near the required boost voltage, and sends a discrete signal to the host to indicate it has awakened.

### Standby Current

The ICs have low standby supply current, as mentioned in the [Electrical Characteristics](#) table, but still allow for 250μs (max) quick turn-on time once  $V_{SUP2}$  falls below BST\_OV\_F. I<sup>2</sup>C settings are held during the low-standby mode. In this



The schematic diagram illustrates a power management IC (PMIC) designed for a battery-powered system. The IC is shown as a central block with various pins and internal functional blocks. The external components and their connections are as follows:

- MBATT1 12V BATTERY:** Connected to the input of the PMIC through a diode (D1), inductor (L2), and capacitors (C8, C9).
- BUB (0 TO 6V LITHIUM CELL OR NiMH CELLS):** Connected to the BUB pin of the PMIC.
- COMP, BIAS, AGND:** Pins for the PMIC's internal control logic.
- OSC + SLOPE COMP, FBB REF, EAMP, COMP:** Internal functional blocks within the PMIC.
- CONTROL LOGIC:** The central control block of the PMIC.
- BIAS REGULATOR:** A block within the PMIC that regulates the bias voltage.
- SUP2, G1, SG1:** Pins for the PMIC's internal control logic.
- M1, LX, DL, DH, BST, CSP, CSN:** Pins for the PMIC's internal control logic.
- BIAS:** A pin for the PMIC's internal control logic.
- C4:** A capacitor connected to the BIAS pin.
- M2, C3, M3:** Diodes and capacitors connected to the output of the PMIC.
- MBATT2, SYSTEM SUPPLY:** The output of the PMIC, which can be connected to a 12V battery or a 5V/3.5A output.

### BUBTRIG Pin

### Current Limit

## Skip Operation

Once zero crossing and one cycle of  $t_{ON\_MIN}$  are reached, the controller enters skip mode. Transition back to PWM mode occurs when there is 480ns of  $t_{ON\_MIN}$  and the output voltage stays too low, so PWM control resumes to bring output voltage back into regulation.

The state-of-health (SOH) block (see [Figure 4](#)) allows the ICs to test the backup battery (BUB) under current-load conditions to aid in determining the condition of the BUB based on output impedance. During the test, the output voltage of the battery, as well as a voltage representation of the current applied, are made available for ADC measurements. When  $V_{BUB}$  is less than 2.5V, the SOH discharger is disabled and the SOH\_ILIM status bit is set to 1, indicating that a fault has occurred. The SOH sink current setting is the SOH (07/h) register. SOH is enabled by setting CONTROL/SOH\_EN. Selection between the hardware-default and register-override values are set by CONTROL/SOH\_OVR.



## I<sup>2</sup>C START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A controller initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the controller signals the beginning of a transmission to the device. The controller terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a Repeated START condition is generated instead of a STOP condition; this is often used in combined-format read operations. See [Figure 5](#) for examples that show the generation and proper use of START (S), STOP (P), and Repeated START (Sr) conditions.

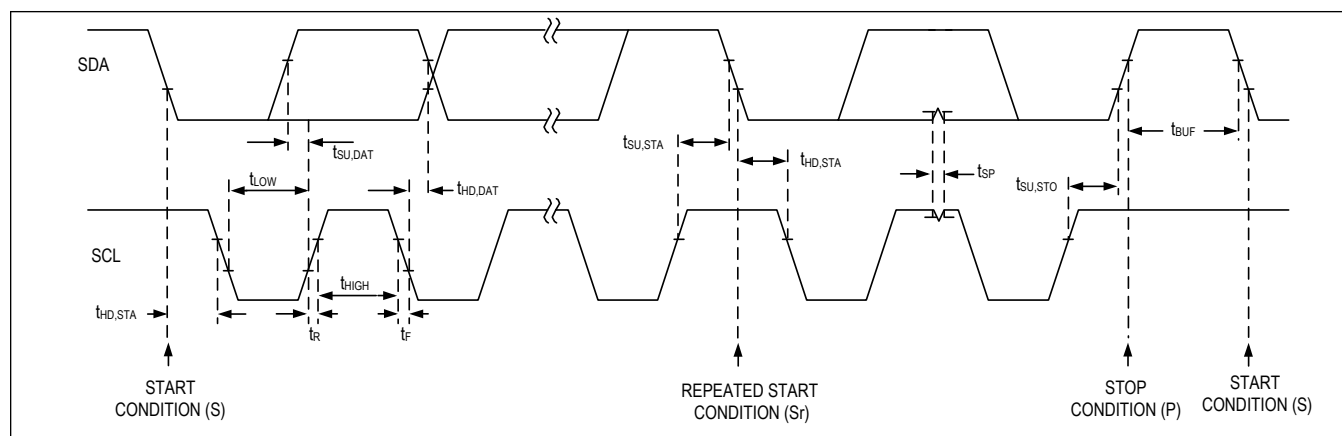


Figure 5. I<sup>2</sup>C Serial-Interface Timing Diagram

## I<sup>2</sup>C Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit the device uses for handshake receipt of each byte of data when in write mode. The device pulls down SDA during the entire controller-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows the detection of unsuccessful data transfers that occur if a receiving device is busy, or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller retries communication. The controller pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the device is in read mode. An acknowledge is sent by the controller after each read byte to allow data transfer to continue. A not-acknowledge (NACK) is sent when the controller reads the final byte of data from the device, followed by a STOP (P) condition.

## I<sup>2</sup>C Command and Data Bytes

A command byte follows the target address. A command byte is typically followed by one or two data bytes unless it is the last byte in the transmission, as would be the case for readback operations (see [Figure 5](#)). If data bytes follow the command byte, the command byte indicates the address of the register that should receive the data bytes that follow. The data bytes are stored in a temporary register and then transferred to the appropriate register during the ACK periods between bytes.

## I<sup>2</sup>C Write Operations

A controller device communicates with the device by transmitting the proper target address, followed by a register/command and data word(s). Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each byte is 8 bits long and is always followed by an acknowledge (ACK) clock pulse, as shown in [Figure 6](#). The first byte contains the address of the device, with R/W = 0 to indicate a write. The second byte contains the register (or command) to be written, and the third byte contains the data to be written.

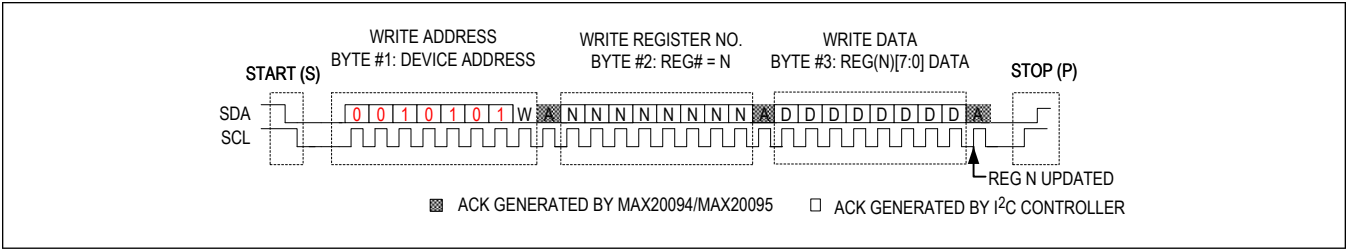


Figure 6. I<sup>2</sup>C Write Sequence

I<sup>2</sup>C Read Operations

The ICs support standard combined-format I<sup>2</sup>C read-mode operations. Each receive sequence is again framed by a START (S) or Repeated START (Sr) condition and a STOP (P). Each byte is 8 bits long and is always followed by an ACK clock pulse, as shown in [Figure 7](#). The first byte contains the address of the device, with R/W = 0 to indicate a write. The second byte contains the register that is to be read back. There is now a Repeated START (Sr) condition, followed by the device address, with R/W = 1 to indicate a read and an acknowledge (ACK) clock. The controller still has control of the SCL line, but the device takes over the SDA line. The fourth byte in the frame contains the register data readback followed by a STOP (P) condition.

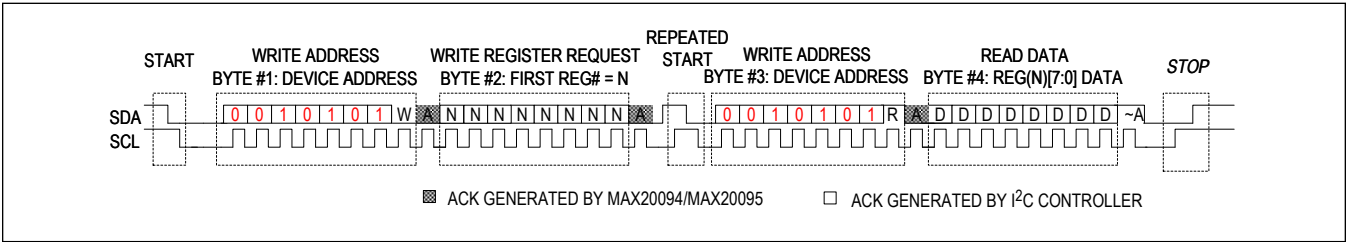


Figure 7. I<sup>2</sup>C Read Sequence

## Register Map

### MAX20094/MAX20095

ADDRESS	NAME	MSB							LSB
USER COMMANDS									
0x00	<a href="#">CHIP_ID[7:0]</a>	DIE_TYPE[7:0]							
0x01	<a href="#">CHGR_STATUS[7:0]</a>	CHGR_EN	CHGR_MODE[2:0]			–	SUP1_UVLO	SUP1_OVP	SUP1_BATT
0x02	<a href="#">GEN_STATUS[7:0]</a>	BOOST	ALRT_BST	ALRT_CV	ALRT_DONE	ALRT_SUP1	THRM_LIM	THRM_SD	SOH_ILIM
0x03	<a href="#">EN_INT[7:0]</a>	EN_BST	EN_ABS_T	EN_ACV	EN_ADN	EN_ASP	EN_TLIM	EN_TSD	EN_SOHI
0x04	<a href="#">CONTROL[7:0]</a>	SOH_EN	SOH_OVR	–	AVB_EN	CHG_EN	CHG_IMON	BST_EN	BST_SKIP
0x05	<a href="#">CHGR_CC[7:0]</a>	–	–	–	FCHG_CUR[4:0]				
0x06	<a href="#">CHGR_CV[7:0]</a>	–	–	–	VCVTHR[4:0]				
0x07	<a href="#">SOH[7:0]</a>	ISINK[3:0]				REG_ISINK[3:0]			
0x08	<a href="#">SW_RST[7:0]</a>	All_Zeros[7:0]							
0xFF	<a href="#">NO_OP[7:0]</a>	Dont_Care[7:0]							

## Register Details

### [CHIP\\_ID \(0x00\)](#)

CHIP\_ID is a read-only register that provides information on the chip and silicon revision.

BIT	7	6	5	4	3	2	1	0
Field	DIE_TYPE[7:0]							
Reset	0x02 for MAX20094 and 0x03 for MAX20095							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DIE_TYPE	7:0	DIE_TYPE provides information on the chip and silicon revision.

### [CHGR\\_STATUS \(0x01\)](#)

CHGR\_STATUS is a read only register that provides information on the Charger operating mode and related Supply1 voltage status.

BIT	7	6	5	4	3	2	1	0
Field	CHGR_EN	CHGR_MODE[2:0]			–	SUP1_UVLO	SUP1_OVP	SUP1_BATT
Reset					–			
Access Type	Read Only	Read Only			–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CHGR_EN	7	0 = Disabled: CONTROL/CHG_EN=0, or BIAS is below UVLO threshold. 1 = Enabled: CONTROL/CHG_EN=1, and BIAS is above UVLO threshold.

BITFIELD	BITS	DESCRIPTION
CHGR_MODE	6:4	0b000 = Disabled/standby 0b010 = Prequalify-Charging Mode: $V_{BATT} < V_{PQVTHR}$ , $I_{CHG} = 50mA$ 0b110 = Fast-Charging Constant Current (CC) Mode: $V_{PQVTHR} \leq V_{BATT} < V_{CVTHR}$ , $I_{CHG} = I_{FCHG\_CUR}$ 0b111 = Fast-Charging Constant Voltage (CV) Mode: $V_{BATT} \geq V_{CVTHR}$ , $I_{CHG} < I_{FCHG\_CUR}$ 0b100 = Fast-Charging Done Mode: $V_{BATT} \geq V_{CVTHR}$ and $I_{CHG} < 50mA$ , $I_{CHG} = 0mA$ <b>Notes:</b> CHGR_MODE[2] = FAST_CHARGE: Indicates charging is controlled by the fast-charge state progression. CHGR_MODE[1] = BATT_CHARGE: Indicates battery is currently being charged. CHGR_MODE[0] = CV_CHARGE: Indicates the fast-charge progression has reached the CV mode. States 001, 011, 101 are not used.
SUP1_UVLO	2	0 = $V_{SUP1} > 3.5V$ 1 = $V_{SUP1} < 3.5V$ <b>Note:</b> 1 when CHG_EN=0.
SUP1_OVP	1	0 = $V_{SUP1} < 7.0V$ 1 = $V_{SUP1} > 7.0V$
SUP1_BATT	0	0 = $V_{SUP1} > (V_{BATT\_} + 100mV)$ 1 = $V_{SUP1} < (V_{BATT\_} + 100mV)$

### GEN\_STATUS (0x02)

GEN\_STATUS is a read-only register that provides information on the status and operation of all internal blocks within the ICs. The contents of the GEN\_STATUS register can be individually selected for inclusion in the STATUS/INTB interrupt term using the EN\_INT register.

BIT	7	6	5	4	3	2	1	0
Field	BOOST	ALRT_BST	ALRT_CV	ALRT_DON E	ALRT_SUP 1	THRM_LIM	THRM_SD	SOH_ILIM
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
BOOST	7	0 = Disabled: CONTROL/BST_EN = 0, or $V_{SUP2} > V_{BOOST\_OV\_F}$ 1 = Enabled: CONTROL/BST_EN = 1 and $V_{SUP2} < V_{BOOST\_OV\_F}$ <b>Note:</b> Boost threshold is set through OTP.
ALRT_BST	6	0 = Boost has not been activated since the last read. 1 = Boost has been activated since last the read. <b>Edge-Set, Clear-on-Read:</b> Once read, this alert is cleared until the boost is deactivated and reactivated. Real-time boost activity can be monitored using D7.
ALRT_CV	5	0 = Charger has not reached fast-charge CV mode since the last read. 1 = Charger has reached fast-charge CV mode since the last read. <b>Edge-Set, Clear-on-Read:</b> Once read, this alert is cleared until the charger exits and reenters the CV state.

BITFIELD	BITS	DESCRIPTION
ALRT_DONE	4	0 = Charger has not reached fast-charge-done mode since the last read. 1 = Charger has reached fast-charge-done mode since the last read. <b>Edge-Set, Clear-on-Read:</b> Once read, this alert is cleared until the charger exits and reenters the done state.
ALRT_SUP1	3	0 = Supply1 conditions allow normal charger operation. 1 = One or more supply status indicators is active. <b>Level-Set, Clear-on-Read:</b> Once read, this alert is cleared if the supply condition has been resolved. Individual supply faults can be read back using CHGR_STATUS.
THRM_LIM	2	0 = Charger is not operating, or is operating normally. 1 = Charger is operating in a thermally limited (reduced-current) mode (> 145°C). <b>Level-Set, Clear-on-Read:</b> Once read, this alert is cleared if the thermal-limit condition has been resolved.
THRM_SD	1	0 = Device is operating normally. 1 = Device thermal protection is engaged (> 170°C). <b>Level-Set, Clear-on-Read:</b> Once read, this alert is cleared if the thermal-shutdown condition has been resolved.
SOH_ILIM	0	0 = SOH is not operating, or is operating normally ( $I_{SNK} < 3A$ , or $V_{BATTP} >$ undervoltage threshold). 1 = SOH is operating in overcurrent condition ( $I_{SNK} \geq 3A$ , or $V_{BATTP} <$ undervoltage threshold when SOH is enabled). <b>Level-Set, Clear-on-Read:</b> Once read, this alert is cleared if the overcurrent condition, or BATTP undervoltage condition has been resolved.

### EN\_INT (0x03)

EN\_INT is a read/write register that governs the operation of the STATUSB output pin. The content of this register determines which interrupt input terms are included in the interrupt output OR term (e.g., a '1' in an EN\_INT register indicates that the corresponding input term is included in the STATUS interrupt output OR term). See the GEN\_STATUS register for detailed descriptions of the interrupt terms.

BIT	7	6	5	4	3	2	1	0
Field	EN_BST	EN_ABST	EN_ACV	EN_ADN	EN_ASP	EN_TLIM	EN_TSD	EN_SOHI
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
EN_BST	7	0 = BOOST status is not included in the STATUS OR term. 1 = BOOST status is included in the STATUS OR term.
EN_ABST	6	0 = ALRT_BST status is not included in the STATUS OR term. 1 = ALRT_BST status is included in the STATUS OR term.
EN_ACV	5	0 = ALRT_CV status is not included in the STATUS OR term. 1 = ALRT_CV status is included in the STATUS OR term.
EN_ADN	4	0 = ALRT_DONE status is not included in the STATUS OR term. 1 = ALRT_DONE status is included in the STATUS OR term.
EN_ASP	3	0 = ALRT_SUP1 status is not included in the STATUS OR term. 1 = ALRT_SUP1 status is included in the STATUS OR term.
EN_TLIM	2	0 = THRM_LIM status is not included in the STATUS OR term. 1 = THRM_LIM status is included in the STATUS OR term.

BITFIELD	BITS	DESCRIPTION
EN_TSD	1	0 = THRM_SD status is not included in the STATUS OR term. 1 = THRM_SD status is included in the STATUS OR term.
EN_SOHI	0	0 = SOH_ILIM status is not included in the STATUS OR term. 1 = SOH_ILIM status is included in the STATUS OR term.

**CONTROL (0x04)**

CONTROL is a read/write register that enables/disables device features.

BIT	7	6	5	4	3	2	1	0
Field	SOH_EN	SOH_OVR	–	AVB_EN	CHG_EN	CHG_IMON	BST_EN	BST_SKIP
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SOH_EN	7	0 = SOH disabled, G2 driven to BATTP. 1 = SOH enabled, G2 driven to achieve $I_{SNK}$ ( $V_{BATTP}$ to AGND - 3V). This will also enable the AVI switch. <b>Notes:</b> This bit is reset to 0 when the boost controller is actively regulating (BST_EN=1 and SUP2 < BST_OV_F threshold). This bit is reset to 0 when SOH current limit is true, or $V_{BATTP}$ is undervoltage.
SOH_OVR	6	0 = Use Hardware default value, $ISINK[3:0] = OTP\_ISINK[3:0]$ . 1 = Use override value, $ISINK[3:0] = REG\_ISINK[3:0]$ . <b>Note:</b> This bit allows toggling between the OTP and REG settings of ISINK.
AVB_EN	4	0 = Switch off. 1 = Switch on.
CHG_EN	3	0 = Charger disabled. 1 = Charger enabled (if EN1B is also low). <b>Notes:</b> The register value is programmed and read back in this location; the AND term showing the charger-enable status is available as CHGR_STATUS/CHGR_EN. This bit is reset to 0 when the boost controller is actively regulating (BST_EN=1 and SUP2 < BST_OV_F threshold).
CHG_IMON	2	0 = Internally shunting current. 1 = Current is sent to the IMON pin (monitoring current externally).
BST_EN	1	0 = Boost controller disabled. 1 = Boost controller enabled. <b>Notes:</b> This bit is reset to 0 if all the following conditions are true: - boost controller is actively regulating (BST_EN=1 and SUP2 < BST_OV_F threshold). - SUP2 < 4.5V (BST_UV threshold).
BST_SKIP	0	0 = Disable boost skip-mode operation. 1 = Enable boost skip-mode operation.

**CHGR\_CC (0x05)**

CHGR\_CC is a read/write register that sets the fast-charge current during constant-current operation.



BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FCHG_CUR[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
FCHG_CUR	4:0	<p>FCHG_CUR sets the fast-charge current between 50mA and 1000mA in 50mA steps</p> <p>0b00000 = 50mA  0b00001 = 100mA  0b00010 = 150mA  ...  0b10001 = 900mA  0b10010 = 950mA  0b10011 = 1000mA  ...  0b11111 = 1000mA</p> <p><b>Notes:</b> Prior to initial write, FCHG_CUR reads back the factory-default setting.  The reset value is determined by OTP (0b00000 = 50mA).</p>

#### [CHGR\\_CV \(0x06\)](#)

CHGR\_CV is a read/write register that sets the charger regulation voltage required to shift to constant-voltage operation.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VCVTHR[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
VCVTHR	4:0	<p>VCVTHR sets the charger regulation between 3.0V and 6.0V in 100mV steps:</p> <p>0b00000 = 3.0V  0b00001 = 3.1V  0b00010 = 3.2V  ...  0b11100 = 5.8V  0b11101 = 5.9V  0b11110 = 6.0V  0b11111 = 7.0V</p> <p><b>Note:</b> The reset value is determined by OTP (0b00110 = 3.6V).</p>

#### [SOH \(0x07\)](#)

SOH is a read/write register that sets the user-programmable sink current during state-of-health (SOH) measurements. Enabling of SOH is accomplished by setting CONTROL/SOH\_EN. Current selection between hardware-default and register-override values is set by CONTROL/SOH\_OVR (Reg03h, D6 and D5, respectively). Writes to this register are only required to modify the register-override value, REG\_ISINK[3:0]. To support dual-current measurements, this register should be written before the override value is used. Readback of the SOH register returns the ISINK[3:0] value currently in use (read only, depending on the value of CONTROL/SOH\_OVR), and the user-programmed value of REG\_ISINK[3:0] (for verification).

BIT	7	6	5	4	3	2	1	0
Field	ISINK[3:0]				REG_ISINK[3:0]			
Reset					0b0000			
Access Type	Read Only				Write, Read			

BITFIELD	BITS	DESCRIPTION
ISINK	7:4	If CONTROL/SOH_OVR = 0, OTP_ISINK[3:0] is returned. If CONTROL/SOH_OVR = 1, REG_ISINK[3:0] is returned. 0b0000 = 125mA.
REG_ISINK	3:0	REG_ISINK sets the discharger's current regulation between 125mA and 2A in 125mA steps: 0b0000 = 125mA 0b0001 = 250mA 0b0010 = 375mA ... 0b1101 = 1.750A 0b1110 = 1.875A 0b1111 = 2A

**SW\_RST (0x08)**

SW\_RST (software reset) is a write-only register/command that resets the entire part to its original default conditions at the end of the I<sup>2</sup>C SW\_RST transaction (i.e., the data-byte ACK). Execution only occurs if DIN[7:0]=0x00. The effect of a SW\_RST is identical to power-cycling the part.

BIT	7	6	5	4	3	2	1	0
Field	All_Zeros[7:0]							
Reset	0b00000000							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
All_Zeros	7:0	

**NO\_OP (0xFF)**

NO\_OP (no-operation register) is a read-write register that has no internal effect on the part. If this register is read back, SDA remains zero for I<sup>2</sup>C readback data. Any attempt to write to this register is ignored, without impact to internal operation.

BIT	7	6	5	4	3	2	1	0
Field	Dont_Care[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
Dont_Care	7:0	

**Register Details**

## Applications Information

### Boost Converter

Boost switching current is sensed by R1 in the [Simplified Block Diagram](#). During large loads, the limits of the CSN, CSP, and the headroom available on the amplifier need to be observed. The  $V_{LIMIT}$  is shown in the [Electrical Characteristics](#) table. For a  $0.003\Omega$  (typ) sense resistor and 40mV (min)  $V_{LIMIT}$ , the peak inductor current is 13.3A. As the BUB is depleted of charge, the CSP pin voltage decreases. When the undervoltage lockout on CSP is disabled, the CSP low voltage for minimum headroom is 1.5V (typ), assuming  $100m\Omega$  battery ESR and  $3.2V_{BUB}$ .

### Inductor Selection

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size; however, if the boost components are used as the input filter components during nonboost operation, low frequency becomes advantageous.

The duty-cycle range of the boost converter depends on the effective input-to-output voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{BUB(MIN)}}{V_{OUT(MAX)}}$$

or including the voltage drops across the inductor, MOSFET ( $V_{ON,FET}$ ):

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{BUB(MIN)} + I_{OUT} \times R}{V_{OUT(MAX)}}$$

where:

$$R = R_{DC} + R_{DS(on),M2} + R_{DS(on),M3}$$

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and elected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{IN} \times D}{f_{SW}[MHz] \times LIR}$$

where:

$$D = (V_{OUT} - V_{IN})/V_{OUT}$$

$V_{IN}$  = Typical input voltage

$V_{OUT}$  = Typical output voltage

$$LIR = 0.3 \times I_{OUT}/1 - D$$

Select the inductor with a saturation current rating higher than the peak-switch current limit of the converter:

$$I_{L, PEAK} > I_{L, MAX} + \frac{\Delta I_{L, RIP, MAX}}{2}$$

Running a boost converter in continuous-conduction mode introduces a right-half-plane zero into the transfer function. To avoid the effect of this right-half-plane zero, the crossover frequency for the control loop should be  $\leq 1/3 \times f_{RHP\_ZERO}$ . If faster bandwidth is required, a smaller inductor and higher switching frequency is recommended.

### MOSFET Selection

The key selection parameters for choosing the n-channel MOSFET used in the boost converter follow.

### Threshold Voltage

The boost's n-channel MOSFET must be a logic-level type with guaranteed on-resistance specifications at  $V_{GS} = 4.5V$ .

### Current Capability

The n-channel MOSFET must deliver the input current ( $I_{IN(MAX)}$ ):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs with the appropriate average current at  $V_{GS} = 4.5V$ .

### Input Capacitor Selection

The BUB provides the voltage on the input and some stability to transients, but can include a wiring harness or series resistance. Add a 10 $\mu$ F, 2.2 $\mu$ F, and 0.1 $\mu$ F X7R ceramic capacitor at the BATTP input of the MAX20094. Review the MAX20094 evaluation kit schematic and PCB layout with the factory to optimize the input capacitors.

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{BUB} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{(V_{BUB} - V_{DB}) \times D}{L \times f_{SW}}$$

$V_{DS}$  is the total voltage drop across the external MOSFET, plus the voltage drop across the inductor ESR.  $\Delta I_L$  is the peak-to-peak inductor ripple current as calculated above.  $\Delta V_Q$  is the portion of input ripple due to the capacitor discharge and  $\Delta V_{ESR}$  is the contribution due to ESR of the capacitor. Assume the input capacitor-ripple contribution due to ESR ( $\Delta V_{ESR}$ ) and capacitor discharge ( $\Delta V_Q$ ) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source, especially at a high output-to-input differential.

### Output Capacitor Selection

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

$I_{OUT}$  is the load current in A,  $f_{SW}$  is in MHz,  $C_{OUT}$  is in  $\mu$ F,  $\Delta V_Q$  is the portion of the ripple due to the capacitor discharge, and  $\Delta V_{ESR}$  is the contribution due to the ESR of the capacitor.  $D_{MAX}$  is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic, and high-value low-cost aluminum capacitors for lower output ripple and noise.

### Shunt Resistor Selection

The current-sense resistor ( $R_{CS\_}$ ), connected between the battery and the inductor, sets the current limit. The CS\_ input has a voltage trip level ( $V_{CS\_}$ ) of 50mV (typ). Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of  $R_{CS\_}$ :

$$R_{CS\_} = \frac{V_{CS\_}}{I_{IN(MAX)}}$$

where  $I_{IN(MAX)}$  is the peak current that flows through the MOSFET at full load and minimum  $V_{IN}$ .

$$I_{IN(MAX)} = \frac{I_{LOAD(MAX)}}{(1 - D_{MAX})}$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

### Input Filter for SUP2

An input filter consisting of a 10µF capacitor and 100mΩ resistor is suggested. SUP2 current is approximately 50mA for boost applications in FPWM mode, 300µA in skip mode, and 26µA in standby mode. For charger and SOH applications, SUP2 current is approximately 1mA.

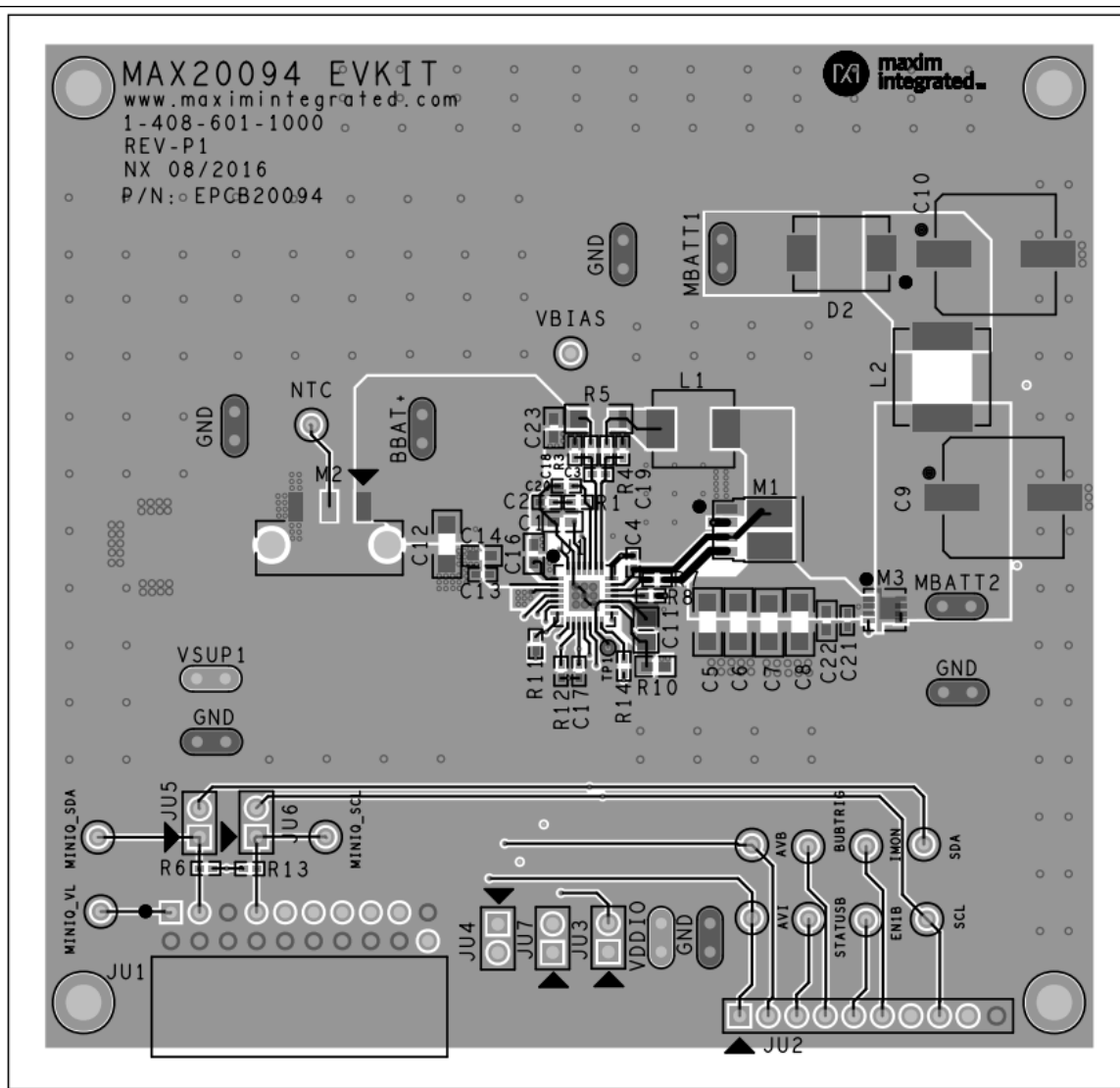
### PCB Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (see [Figure 5](#)). When possible, mount all power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more.
- Minimize current-sensing errors by connecting CSP and CSN. Use Kelvin sensing directly across the current-sense resistor (RCS<sub>+</sub>).
- Route high-speed switching nodes (BST<sub>+</sub>, LX<sub>+</sub>, DH<sub>+</sub>, and DL<sub>+</sub>) away from sensitive analog areas (SUP2, CSP, and CSN).

### PCB Layout Procedure

- Place the power components first, with ground terminals adjacent (low-side FET, C<sub>IN</sub>, C<sub>OUT</sub>, and Schottky). If possible, make all these connections on the top layer with wide, copper-filled areas.
- Mount the controller IC adjacent to the low-side MOSFET (preferably on the back side opposite NL<sub>+</sub> and NH<sub>+</sub>) to keep LX, GND, DH<sub>+</sub>, and the DL<sub>+</sub> gate-drive lines short and wide. To keep the driver impedance low, and for proper adaptive dead-time sensing, the DL<sub>+</sub> and DH<sub>+</sub> gate traces must be short and wide (50 mils to 100 mils), if the MOSFET is 1in from the controller IC.
- Group the gate-drive components (BST<sub>+</sub> diode and capacitor and LDO bypass capacitor, BIAS) together as close as possible to the controller IC. Be aware that gate currents of up to 1A flow from the bootstrap capacitor to BST<sub>+</sub>, from DH<sub>+</sub> to the gate of the external HS switch, and from the LX pin to the inductor. Dimension those traces accordingly.
- Make the DC-DC controller ground connections, as shown in the MAX20094 EV kit component placement guide (see [Figure 8](#)). This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go, and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly under the IC.
- Connect the output power planes directly to the output filter capacitor's positive and negative terminals with multiple vias, and place the entire DC-DC converter circuit as close as possible to the load.



## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	f <sub>sw</sub>	V <sub>OUT</sub>	BUB_UVLO	V <sub>PQVTHR</sub>
MAX20094ATIA/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.2V	On	2.0V
MAX20094ATIB/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.5V	On	2.0V
MAX20094ATIC/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.8V	On	2.0V
MAX20094ATID/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	7.1V	On	2.0V
MAX20094ATIE/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	400kHz	6.2V	On	2.0V
MAX20094ATIF/VY+**	-40°C to +125°C	28 (SW) TQFN-EP*	400kHz	7.1V	On	2.0V
MAX20094ATIJ/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	6.5V	On	3.0V
MAX20095ATIA/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	5.5V	On	2.0V
MAX20095ATIB/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	8V	On	2.0V
MAX20095ATIC/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	9V	On	2.0V
MAX20095ATID/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	10V	On	2.0V
MAX20095ATIE/VY+	-40°C to +125°C	28 (SW) TQFN-EP*	2.2MHz	12V	On	2.0V

/V denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

(SW) = Side-wettable package.

\* EP = Exposed pad.

\*\* Future product—contact factory for availability.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/17	Initial release	—
1	7/17	Updated min and max numbers for Boost Mode Fixed-Output Voltage (VSUP2), deleted Boost Mode Fixed-Output Voltage Accuracy row in <a href="#">Electrical Characteristics</a> ; updated Reset address in CHIP_ID (0x00) register table; removed future product status from MAX20095ATIA/VY+ in <a href="#">Ordering Information</a>	4, 20, 30
2	5/18	Changed package outline number (from 21-100041 to 21-100130) and land pattern number (from 90-0025 to 90-0027), as well as thermal resistances in the Package Information table; removed future product status from MAX20095ATIB/VY+, MAX20095ATIC/VY+, MAX20095ATID/VY+, and MAX20095ATIE/VY+ in the <a href="#">Ordering Information</a> table	3, 30
3	7/19	Updated <a href="#">Simplified Block Diagram</a> , <a href="#">Pin Description</a> , <a href="#">Detailed Description</a> , I <sup>2</sup> C User Command and Register Map, and <a href="#">Ordering Information</a>	2, 11, 16, 17, 20, 24, 26, 27, 30
4	1/20	Updated <a href="#">Simplified Block Diagram</a> , <a href="#">Electrical Characteristics</a> , <a href="#">Detailed Description</a> , Register Map, <a href="#">Applications Information</a> , and <a href="#">Ordering Information</a>	2, 5, 16, 17, 22, 27, 30
5	10/20	Updated <a href="#">Electrical Characteristics</a> , <a href="#">Ordering Information</a> , and register 0x04 CONTROL in Register Map	4, 24, 31
6	5/22	Updated <a href="#">Electrical Characteristics</a> , <a href="#">Detailed Description</a> , <a href="#">Typical Operating Characteristics</a> , register 0x02 GEN_STATUS in Register Map, and <a href="#">Ordering Information</a>	3, 4, 10, 14, 22, 30
7	5/22	Removed future product notation for MAX20094ATIJ/VY+	31



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