Click here to ask an associate for production status of specific part numbers.

MAX17614

4.5V to 60V, 3A, Ideal Diode/Power Source Selector with Current Limit, UV, OV Protection

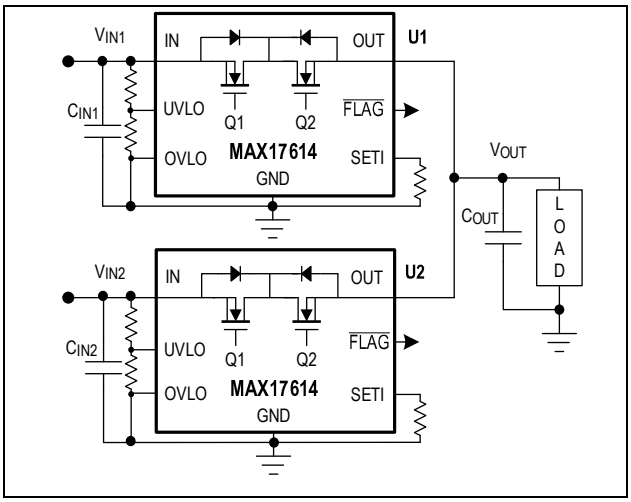
Product Highlights

- Ideal Diode Operation
  - Fast Reverse Current-Blocking Protection(140ns)
  - Seamless Power Source Switchover
- Robust Protection Reduces System Downtime
  - Wide Input Supply Range: +4.5V to +60V
  - Hot Plug-in Tolerant without transient voltage suppressor (TVS) up to 35V Input Supply
  - Negative Input Tolerance to -65V
  - Low R_{ON} 130mΩ (typ)
  - Thermal Shutdown Protection
  - Programmable Startup Blanking Time
  - Extended -40°C to +125°C Temperature Range
- Flexible Design Options Enable Reuse and Less Requalification
  - Adjustable Input Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) Thresholds
  - Programmable Forward-Current Limit: 0.15A to 0.3A with +3.6% and -3.3% Accuracy and 0.3A to 3A with ±3.3% Accuracy Over Full Temperature Range
  - Programmable Current Limit Fault Response: Autoretry, Continuous, and Latch-Off Modes
  - Built-in Fault Indication Signals: UVOV and $\overline{FLAG}$
- Saves Board Space and Reduces External BOM Count
  - 20-Pin, 4mm x 4mm, TQFN-EP Package
  - Integrated Back-to-Back nFETs

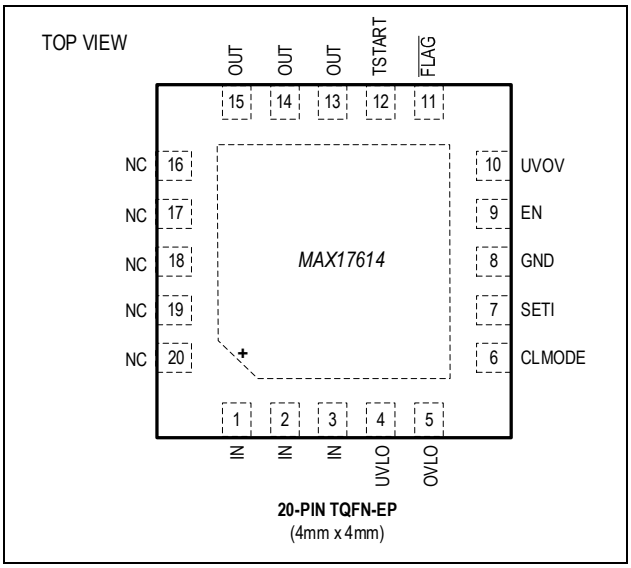
Key Applications

- Small Total Solution Size
  The MAX17614 with its integrated nFETs enables up to 40% smaller solution size in space-constrained equipment. Applications include ideal diode implementations and power source selectors where the end equipment needs to supply the load from more than one power source.
- Faster Response Times
  Faster fault exit response times enable the MAX17614 to reduce output hold-up capacitor size up to 50% in Priority Power Source Selector applications, where the end equipment input supply transitions between a higher priority power source and a backup power source.
- Tight Current Limit Accuracy
  Battery-operated electronics as well as battery chargers need tight current limit accuracy to protect against overcurrent faults. The MAX17614 with its ±3.3% tight current limit accuracy provides robust overcurrent protection in these applications.

Simplified Application Diagram



Pin Description



20-PIN TQFN-EP
(4mm x 4mm)

***Ordering Information* appears at end of data sheet.**

19-101707 Rev 0; 04/23

Absolute Maximum Ratings

IN to GND ..... -70V to +65V

IN to OUT ..... -65V to +65V

OUT to GND ..... -0.3V to +65V

UVLO, OVLO to GND ..... -0.3V to (max(V_{IN}, V_{OUT})+0.3)V

EN, CLMODE, TSTART to GND ..... -0.3V to +6.0V

UVOV, $\overline{FLAG}$ to GND ..... -0.3V to +6.0V

IN Current (DC) 3.3A

SETI to GND (*Note 1*) ..... -0.3V to +1.6V

Continuous Power Dissipation (T_A = +70°C, derate 30.3mW/°C above +70°C) 2424.2mW

Operating Temperature Range (*Note 2*) ..... -40°C to +125°C

Junction Temperature Range ..... -40°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Note 1: The SETI pin is internally clamped. Forcing more than 5mA current into the pin can damage the device.

Note 2: Junction temperature greater than +125°C degrades operating life times.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 20 TQFN	
Package Code	T2044+4C
Outline Number	*21-100172*
Land Pattern Number	*90-0409*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	33°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.

Electrical Characteristics

(V_{IN} = V_{IN} = +4.5V to +60V, V_{UVLO} = 1.8V, V_{OVLO} = 1V, R_{SETI} = 1.5kΩ, C_{IN} = 1µF, C_{OUT} = 0.47µF, EN = TSTART = CLMODE = OUT = $\overline{FLAG}$ = UVOV = Unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C. All voltages are referred to GND, unless otherwise noted. (*Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		4.5		60	V
Shutdown Input Current	I_{SHDN}	V_{EN} = 0V		33	75	µA
Shutdown Output Current	I_{OFF}	V_{EN} = 0V, V_{OUT} = 0V	-10			µA
Reverse Input Current	I_{IN_RVS}	V_{IN} = -60V, V_{OUT} = 0V	-100	-58		µA
Supply Current	I_{IN}	V_{IN} = 24V		1.02	1.35	mA
Internal Undervoltage Trip Level	V_{INT_UVR}	V_{IN} rising	3.46	4.20	4.50	V
	V_{INT_UVF}	V_{IN} falling	3.20	3.46	4.00	
UVLO Threshold	V_{UVR}	V_{UVLO} rising	1.47	1.50	1.53	V
	V_{UVF}	V_{UVLO} falling	1.42	1.45	1.48	

(V_{IN} = V_{IN} = +4.5V to +60V, V_{UVLO} = 1.8V, V_{OVLO} = 1V, R_{SETI} = 1.5kΩ, C_{IN} = 1µF, C_{OUT} = 0.47µF, EN = TSTART = CLMODE = OUT = $\overline{FLAG}$ = UVOV = Unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C. All voltages are referred to GND, unless otherwise noted. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVLO Threshold	V_{OVR}	V_{OVLO} rising	1.47	1.50	1.53	V
	V_{OVF}	V_{OVLO} falling	1.42	1.45	1.48	
UVLO, OVLO Leakage Current	I_{LEAK}	V_{UVLO} = V_{OVLO} = 0 to 2V	-100		+100	nA
OVLO Adjustment Range		(Note 4)	5.5		60	V
UVLO Adjustment Range		(Note 4)	4.5		59	V
INTERNAL FETs						
Internal FETs On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} > 8V, T_J = +25°C		130	155	mΩ
		I_{LOAD} = 100mA, V_{IN} > 8V, T_J = +85°C			200	
		I_{LOAD} = 100mA, V_{IN} > 8V, -40°C ≤T_J ≤ +125°C			230	
Current Limit Adjustment Range	I_{LIM}	(Note 5)	0.15		3	A
Current Limit Accuracy		0.15A ≤ I_{LIM} ≤ 0.3A (Note 7)	-3.3		+3.6	%
		0.3A ≤ I_{LIM} ≤ 3A (Note 7)	-3.3		+3.3	
Overcurrent Protection Threshold	I_{OCP}	(Note 6)	4.0	8.5	15.0	A
$\overline{FLAG}$ Assertion Drop Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V	410	470	550	mV
Slow Reverse Current Blocking Threshold	V_{RIBS}	(V_{IN} - V_{OUT}) (Note 6)	-8.6	-4.5	-0.3	mV
Slow Reverse Current Blocking Debounce Blanking Time	t_{DEBRIB}	(Note 8)	10	17	35	µs
Fast Reverse Current Blocking Threshold	V_{RIBF}	(V_{IN} - V_{OUT}) (Note 8)	-130	-102	-68	mV
Fast Reverse Current Blocking Response Time	t_{RIB}	(Note 6)	90	140	220	ns
Reverse Blocking Exit Threshold	V_{RIB_RISING}	(V_{IN} - V_{OUT}) (Note 8)	67	100	123	mV
Q1 Turn-On Time	t_{Q1_ON}	I_{LOAD} = 3A, ΔV_{OUT} = 150mV		8		µs
Reverse Blocking Supply Current	I_{RBL}	Current into OUT when (V_{OUT} - V_{IN}) > 130mV		1.06	1.40	mA
SETI						
R_{SETI} x I_{LIM}	V_{RI}			1.5		V
Current Mirror Output Ratio	C_{IRATIO}	0.15A ≤ I_{IN} ≤ 0.3A (Note 7)	2952	3032	3117	A/A
		0.3A ≤ I_{IN} ≤ 3A (Note 7)	2964	3032	3128	
Internal SETI Clamp	V_{SETI_MAX}	5mA into SETI	1.6		2.2	V
SETI Leakage Current		V_{SETI} = 1.6V	-0.1		+0.1	µA
LOGIC INPUT						
EN Input Logic High	V_{IH}		1.4			V
EN Input Logic Low	V_{IL}				0.4	V

(V_{IN} = V_{IN} = +4.5V to +60V, V_{UVLO} = 1.8V, V_{OVLO} = 1V, R_{SETI} = 1.5kΩ, C_{IN} = 1µF, C_{OUT} = 0.47µF, EN = TSTART = CLMODE = OUT = $\overline{FLAG}$ = UVOV = Unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C. All voltages are referred to GND, unless otherwise noted. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Pull-Up Voltage		EN pin unconnected. V_{IN} = 60V		1.4	2.0	V
EN Input Current		V_{EN} = 5.5V		13	40	µA
EN Pull-Up Current		V_{EN} = 0.4V	1.0	6.2	15.0	µA
CLMODE Input Logic High			2.0	4.2	4.9	V
CLMODE Input Logic Low			0.25	0.60	0.95	V
CLMODE Pull-Up Input Current			8	10	12	µA
$\overline{FLAG}$, UVOV OUTPUTs						
$\overline{FLAG}$, UVOV Output Logic Low Voltage		I_{SINK} = 1mA			0.4	V
$\overline{FLAG}$, UVOV Output Leakage Current		V_{IN} = $V_{\overline{FLAG}}$ = V_{UVOV} = 5V, $\overline{FLAG}$ and UVOV pins are deasserted			1	µA
TSTART STARTUP						
TSTART Reference Voltage	$V_{TSTART-REF}$		1.43	1.50	1.57	V
TSTART Output Current	I_{START}		4.5	5.0	5.5	µA
TSTART Internal Shunt Discharge Resistance	R_{START}	Discharging Resistance			300	Ω
TSTART Unconnecting Check Time Interval	$t_{START-UNCONNECTED}$			100		µs
TSTART Default Interval	$t_{START-DEFAULT}$		90	100	110	ms
TIMING CHARACTERISTICS						
Q2 Turn-On Delay	$t_{Q2\_ON\_OVLO}$	I_{LOAD} = 3A, From V_{OVLO} < V_{OVF} to I_{OUT} = 95%. (Note 6)		18	26	µs
	$t_{Q2\_ON\_UVLO}$	I_{LOAD} = 3A, From V_{UVLO} > V_{UVR} I_{OUT} = 95%. (Note 6)		1.15	1.80	ms
OVLO Rising Edge Delay	t_{OVR_DLY}	From V_{OVLO} > V_{OVR} to V_{OUT} = 90%; R_{LOAD} = 1kΩ, C_{LOAD} = 0pF. (Note 8)		0.86	1.50	µs
UVLO Falling Edge Delay	t_{UVF_DLY}	From V_{UVLO} < V_{UVF} to V_{OUT} = 90%; R_{LOAD} = 1kΩ, C_{LOAD} = 0pF		10		µs
UVLO Rising Edge Delay	t_{UVR_DLY}	From V_{UVLO} > V_{UVR} to V_{OUT} = 10%; R_{LOAD} = 1kΩ, C_{LOAD} = 0pF		0.77		ms
Overcurrent Protection Response Time	t_{OCP_RES}	I_{LIM} = 3A, C_{LOAD} = 0µF, R_{LOAD} step from 16Ω to 6Ω. Time to regulate I_{OUT} within 10% of current limit value.		32		µs
IN Debounce Time	t_{DEB}	From (V_{IN_UVR} < V_{IN} < V_{IN_OVR}) and (EN = High) to V_{OUT} = 10% of V_{IN}. Elapses only at power-up. V_{IN} = 24V. (Note 6)	0.75	1.25	2.00	ms
Current Limit Blanking Time	t_{BLANK}	(Note 9)	18	20	22	ms
Current Limit Autoretry Time	t_{RETRY}	After blanking time from I_{OUT} > I_{LIM} to $\overline{FLAG}$ deasserted (Note 10)	900	1000	1100	ms
THERMAL PROTECTION						

(V_{IN} = V_{IN} = +4.5V to +60V, V_{UVLO} = 1.8V, V_{OVLO} = 1V, R_{SETI} = 1.5kΩ, C_{IN} = 1µF, C_{OUT} = 0.47µF, EN = TSTART = CLMODE = OUT = $\overline{FLAG}$ = UVOV = Unconnected, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C. All voltages are referred to GND, unless otherwise noted. (*Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown	T_J			155		˚C
Thermal Shutdown Hysteresis	$T_{J(HYS)}$			15		˚C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design; not production tested.

Note 4: User settable. See the *Input Overvoltage Lockout* and *Input Undervoltage Lockout* sections for instructions.

Note 5: The current limit can be set below 150mA with a decreased accuracy.

Note 6: Guaranteed by design, not production tested.

Note 7: Production tested at 600mA. Guaranteed by design over entire range.

Note 8: Production tested at V_{IN} = 24V. Guaranteed by design for V_{IN} = 4.5V to 60V.

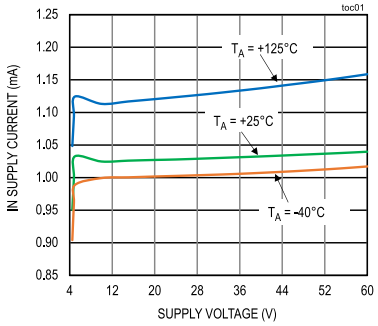
Note 9: During overload and short-circuit conditions, the power dissipation in the device increases. The device enters thermal shutdown protection if the junction temperature exceeds thermal shutdown threshold (T_J).

Note 10: The ratio between autoretry time and blanking time is fixed and equal to 50.

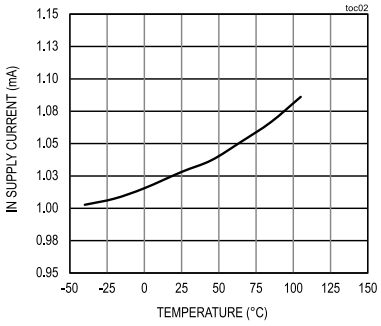
Typical Operating Characteristics

Typical values are at V_{IN} = +24V, V_{IN_UVF} = 4.5V, EN = OPEN, T_A = +25°C, C_{IN} = 1µF, C_{OUT} = 4.7µF, R_{SETI} = 1.5kΩ, unless otherwise noted.

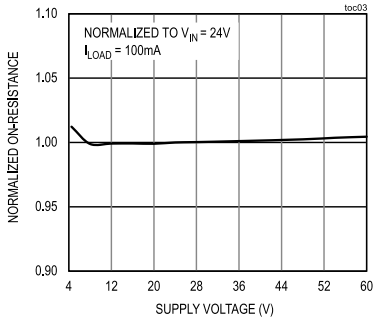
IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



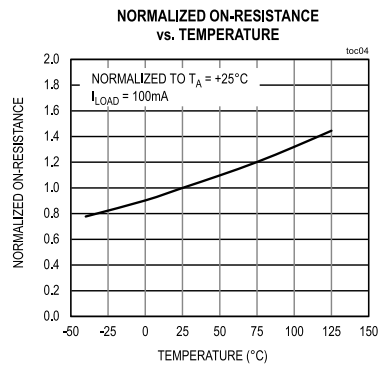
IN SUPPLY CURRENT vs. TEMPERATURE



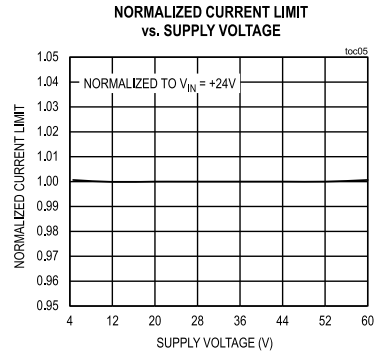
NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



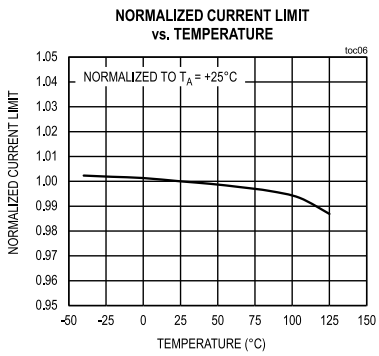
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



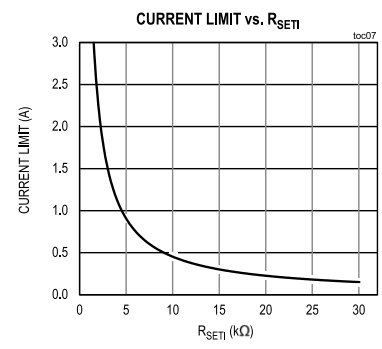
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



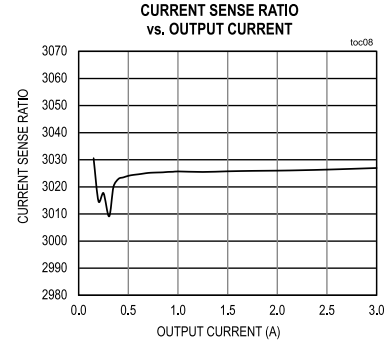
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



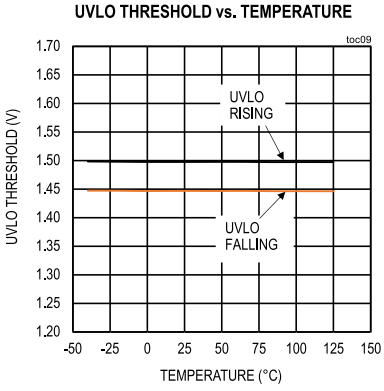
CURRENT LIMIT vs. R_{SETI}



CURRENT SENSE RATIO vs. OUTPUT CURRENT

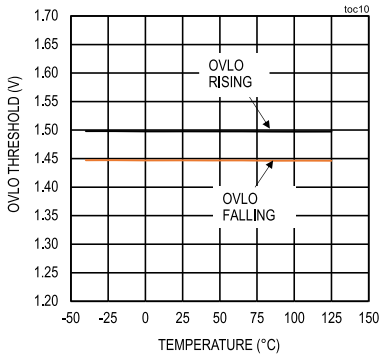


UVLO THRESHOLD vs. TEMPERATURE

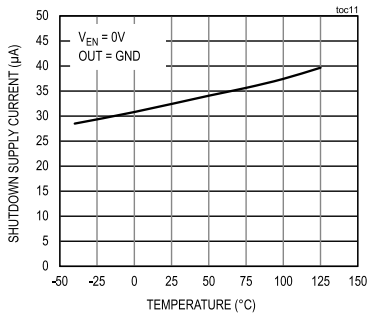


Typical values are at V_{IN} = +24V, V_{IN_UVF} = 4.5V, EN = OPEN, T_A = +25°C, C_{IN} = 1µF, C_{OUT} = 4.7µF, R_{SETI} = 1.5kΩ, unless otherwise noted.

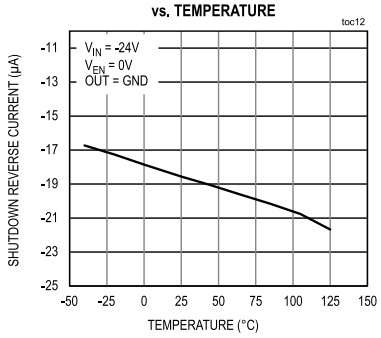
OVLO THRESHOLD vs. TEMPERATURE



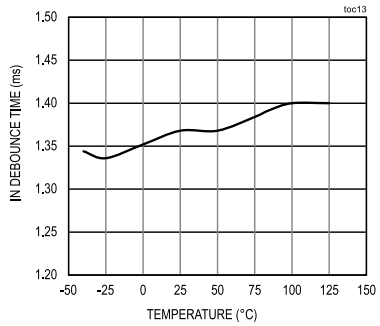
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



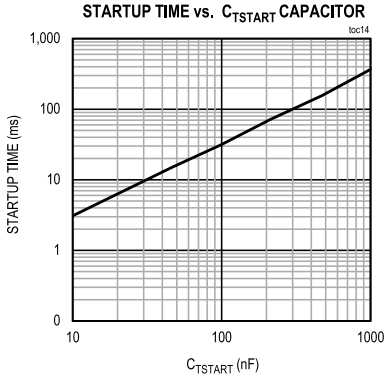
SHUTDOWN REVERSE CURRENT INTO IN PIN vs. TEMPERATURE



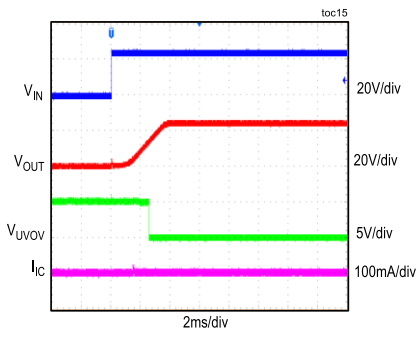
IN DEBOUNCE TIME vs. TEMPERATURE



STARTUP TIME vs. C_{TSTART} CAPACITOR

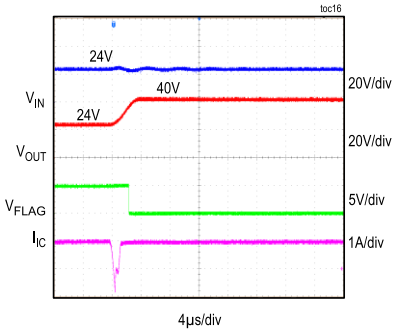


POWER-UP RESPONSE



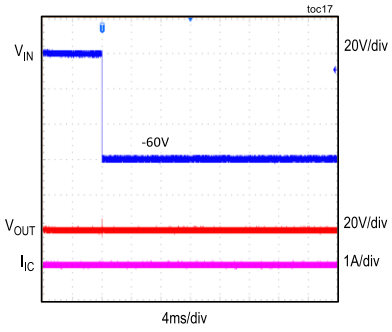
CONDITIONS: UVOV IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

REVERSE-BLOCKING RESPONSE

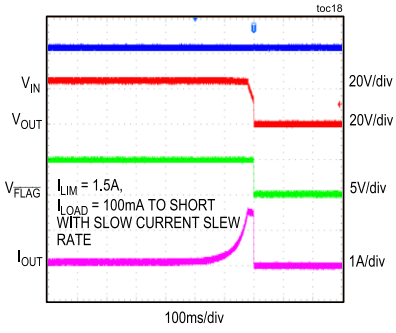


CONDITIONS: $\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

REVERSE INPUT SUPPLY PROTECTION



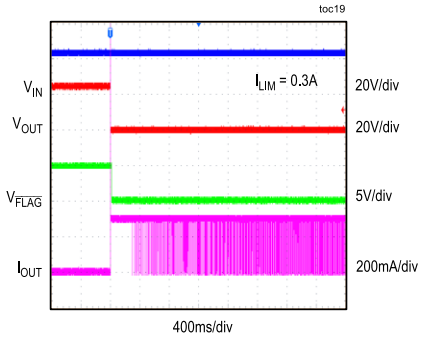
CURRENT-LIMIT RESPONSE



CONDITIONS: $\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

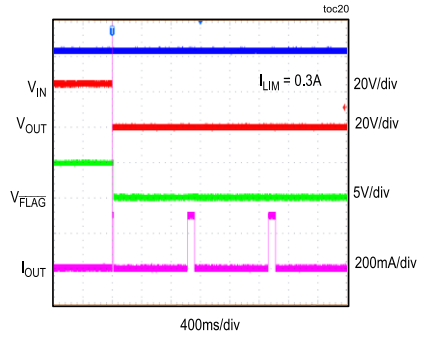
Typical values are at V_{IN} = +24V, V_{IN_UVF} = 4.5V, EN = OPEN, T_A = +25°C, C_{IN} = 1µF, C_{OUT} = 4.7µF, R_{SETI} = 1.5kΩ, unless otherwise noted.

CONTINUOUS CURRENT-LIMIT MODE RESPONSE



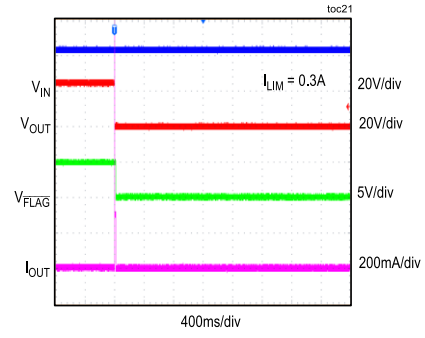
CONDITIONS: $\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

AUTORETRY CURRENT-LIMIT MODE RESPONSE



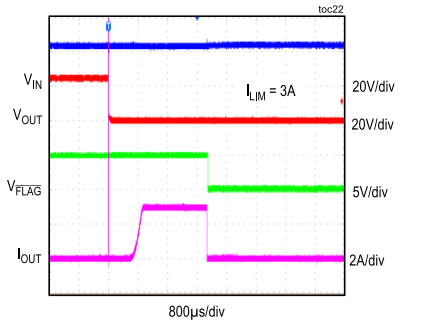
CONDITIONS: $\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

LATCH-OFF CURRENT-LIMIT MODE RESPONSE



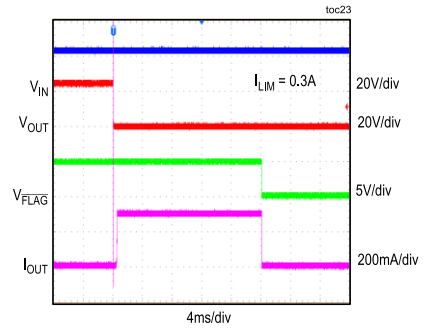
CONDITIONS: $\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

THERMAL SHUTDOWN DUE TO OUTPUT SHORT-CIRCUIT



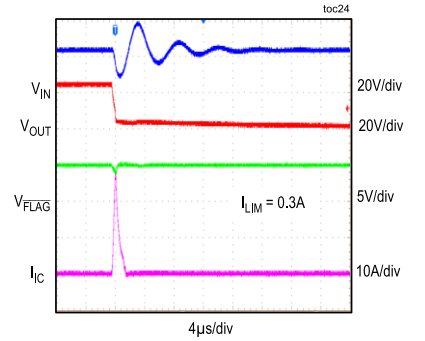
CONDITIONS: CLMODE = OPEN OR CONNECTED TO 150kΩ TO GND
$\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

OUTPUT SHORT-CIRCUIT RESPONSE



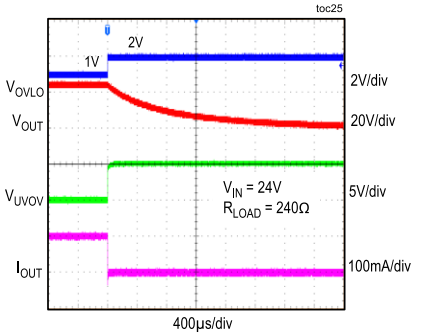
CONDITIONS: CLMODE = OPEN OR CONNECTED TO 150kΩ TO GND
$\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

OUTPUT SHORT-CIRCUIT FAST TRIP RESPONSE



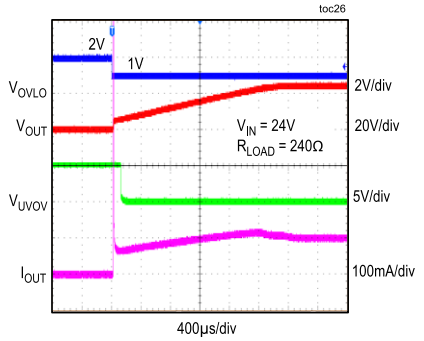
CONDITIONS: $\overline{FLAG}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

OVLO OVERVOLTAGE CUT-OFF RESPONSE



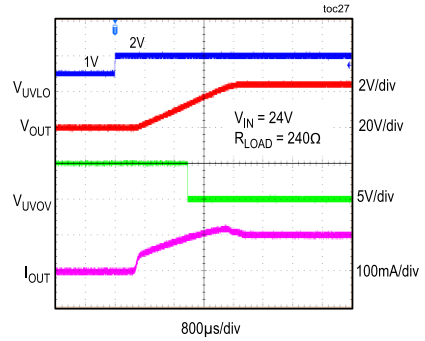
CONDITIONS: UVOV IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

OVLO FALLING RESPONSE



CONDITIONS: UVOV IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

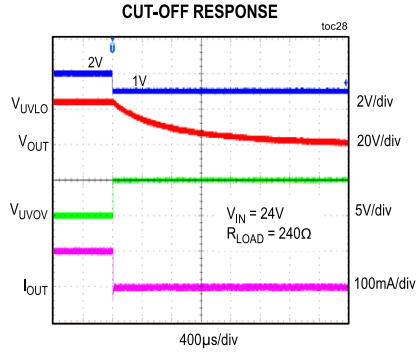
UVLO RISING RESPONSE



CONDITIONS: UVOV IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

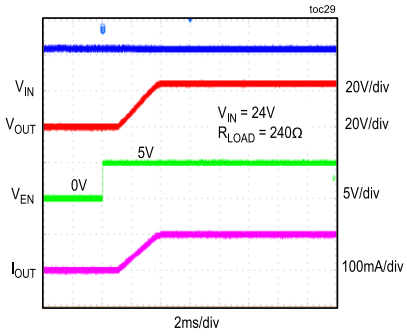
Typical values are at V_{IN} = +24V, V_{IN_UVF} = 4.5V, EN = OPEN, T_A = +25°C, C_{IN} = 1µF, C_{OUT} = 4.7µF, R_{SETI} = 1.5kΩ, unless otherwise noted.

UVLO UNDERVOLTAGE CUT-OFF RESPONSE

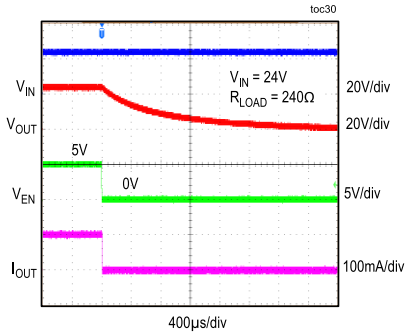


CONDITIONS: UVOV IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

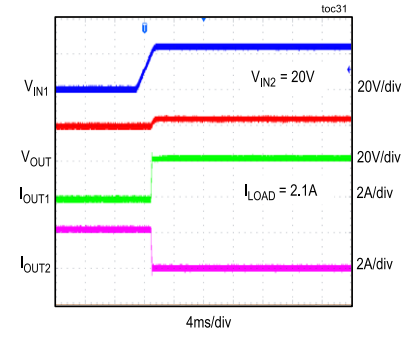
TURN-ON THROUGH EN



TURN-OFF THROUGH EN

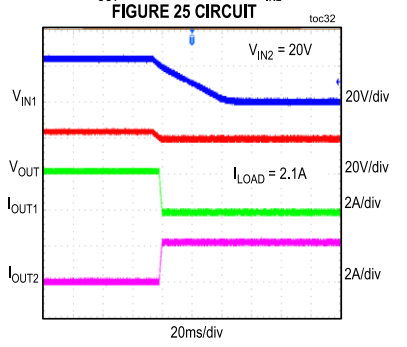


IDEAL DIODE APPLICATION, V_{OUT} SWITCHOVER TO V_{IN1} FIGURE 25 CIRCUIT



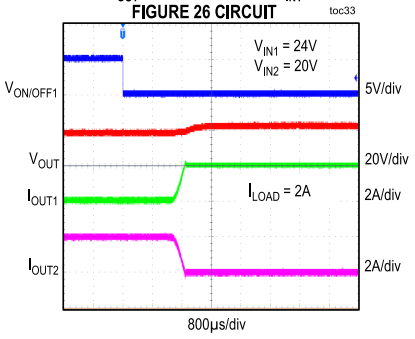
CONDITIONS: V_{IN1} = 0V to 24V

IDEAL DIODE APPLICATION, V_{OUT} SWITCHOVER TO V_{IN2} FIGURE 25 CIRCUIT

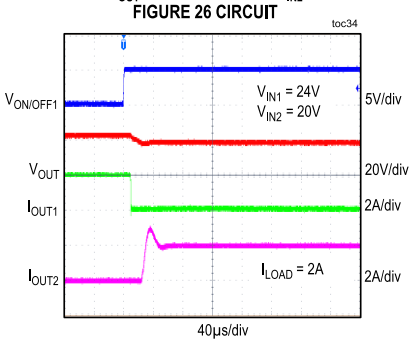


CONDITIONS: V_{IN1} = 24V to 0V

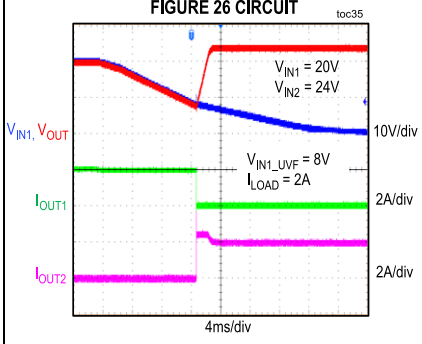
POWER SOURCE SELECTOR, V_{OUT} SWITCHOVER TO V_{IN1} FIGURE 26 CIRCUIT



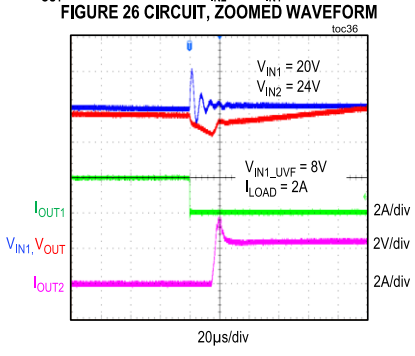
POWER SOURCE SELECTOR, V_{OUT} SWITCHOVER TO V_{IN2} FIGURE 26 CIRCUIT



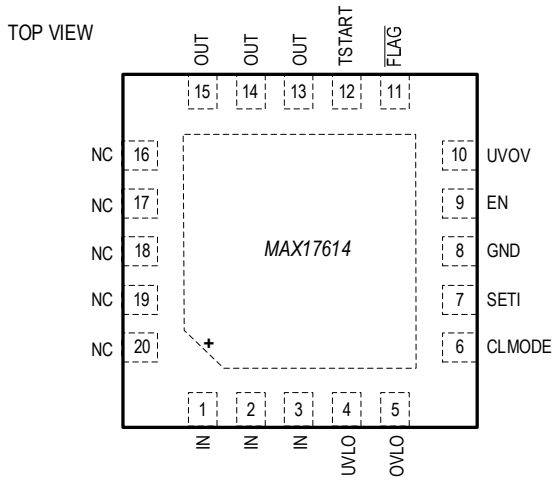
PRIOITIZED POWER SOURCE SELECTOR, V_{OUT} SWITCHOVER TO V_{IN2} AT V_{IN1} FALLING UVLO FIGURE 26 CIRCUIT



PRIOITIZED POWER SOURCE SELECTOR, V_{OUT} SWITCHOVER TO V_{IN2} AT V_{IN1} FALLING UVLO, FIGURE 26 CIRCUIT, ZOOMED WAVEFORM



Pin Configuration

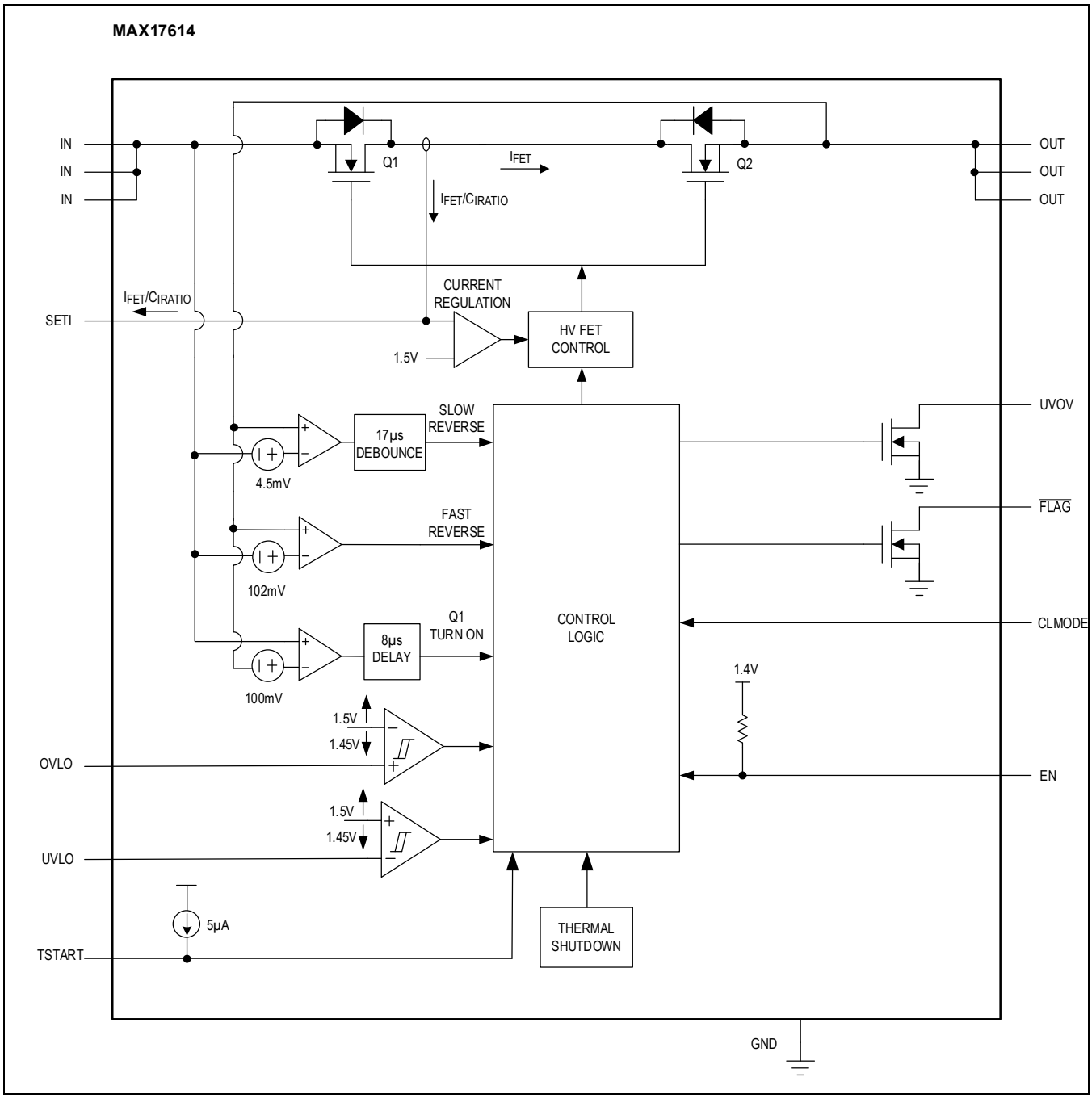


20-PIN TQFN-EP
(4mm x 4mm)

Pin Descriptions

PIN	NAME	FUNCTION
1-3	IN	Input Pins. Connect a low-ESR ceramic capacitor to enhance ESD protection. For Hot Plug-In applications, see the *Applications Information* section.
4	UVLO	Input UVLO Adjustment. Connect UVLO to mid-point of a resistive potential divider from IN to GND to set the Input UVLO threshold.
5	OVLO	Input OVLO Adjustment. Connect OVLO to mid-point of a resistor-divider from IN to GND to set the Input OVLO threshold.
6	CLMODE	Current-Limit Mode Selector. Connect CLMODE to GND for Continuous mode. Connect a 150kΩ resistor between CLMODE and GND for Latch-off mode. Leave CLMODE unconnected for Autoretry mode.
7	SETI	Overcurrent Limit Adjustment Pin and Current Monitoring Output. Connect a resistor from SETI to GND to set the overcurrent limit. See *Setting the Current Limit/Threshold (SETI)* section. Do not connect more than 10pF to SETI.
8	GND	Ground.
9	EN	Active-High Enable Input. Internally pulled-up to 1.4V. Leave unconnected for always ON operation.
10	UVOV	Open-Drain, Fault Indicator Output. UVOV goes high when: • Input voltage falls below UVLO falling threshold. • Input voltage rises above OVLO rising threshold.
11	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low when: • Overcurrent limit duration exceeds the blanking time during normal operation. • Output voltage does not reach (V_{IN}-V_{FA}) within startup blanking time. • Reverse current is detected. • Thermal shutdown is active. • R_{SETI} is less than 1.5kΩ (max).
12	TSTART	Startup Blanking Time Programming Input. Connect a capacitor from TSTART to GND to program the desired startup blanking time. Leave TSTART pin unconnected for a default startup blanking time of 100ms. See *Programming Startup Blanking Time (TSTART)* section for more details.
13-15	OUT	Output Pins. For a long output cable or inductive load, see the *Applications Information* section.
16-20	NC	Not Connected.
-	EP	Exposed Pad. Connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17614 EV kit data sheet for a reference layout design.

Functional Diagram



Detailed Description

The MAX17614 ideal diode/power source selector device offers adjustable protection boundaries for systems against positive and negative input faults up to +60V and -65V, and output load current up to 3A. The device features two internal nFETs connected in series with a low cumulative R_{ON} of 130mΩ (typ) and can be used to implement an ideal diode function to provide reverse input voltage and reverse current protection with improved system efficiency. Input undervoltage protection can be programmed between 4.5V and 59V, while the overvoltage protection can be independently programmed between 5.5V and 60V. Additionally, the device has an internal default UVLO rising threshold set at 4.2V (typ).

The device is enabled or disabled through the EN pin by a main supervisory system. This in turn offers a switch operation to turn on or turn off power delivery to connected loads.

The current through the device is limited by setting a current limit, which is programmed by a resistor connected from SETI to GND. The current limit can be programmed between 0.15A to 3A. When the device current reaches or exceeds the set current limit, the internal nFET Q2 is controlled to limit the current to set limit. The device offers three current-limit modes: Autoretry, Continuous, and Latch-off. The SETI pin also presents a voltage with reference to GND, which under normal operation is proportional to the device current. The voltage appearing on the SETI pin might be read by an analog-to-digital converter or ADC in a monitoring system for recording instantaneous device current.

The device offers $\overline{FLAG}$ and UVOV communication signals to indicate different operational and fault signals. The communication signal pins are open drain in nature and require external pullup resistors to appropriate system interface voltage.

The device offers internal thermal shutdown protection against excessive power dissipation.

Input Undervoltage Lockout

Connect an external resistive divider to the UVLO pin as shown in *Figure 1* to adjust the Input UVLO threshold voltage. Use the following equation to adjust the falling Input UVLO threshold (V_{UVF}). The recommended value of R1 is 2.2MΩ.

$$V_{IN\_UVF} = V_{UVF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{IN_UVF} is the input supply voltage at which the device enters the UVLO condition.

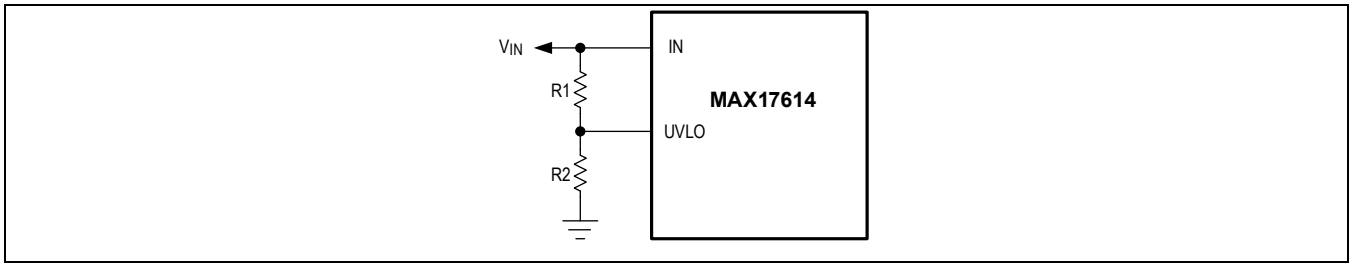


Figure 1. Adjustable Input UVLO

If the voltage at the UVLO pin decreases below V_{UVF}, only the output nFET Q2 is turned off after 10µs (t_{UVF_DLY}) and UVOV is asserted high while the input nFET Q1 is kept ON. When the UVLO condition is removed, the device takes 0.77ms (t_{UVR_DLY}) to start the switch turn-on process. Q2 turns back on within 1.15ms ($t_{Q2\_ON\_UVLO}$) and UVOV is deasserted low. *Figure 2* depicts input undervoltage rising and falling operation.

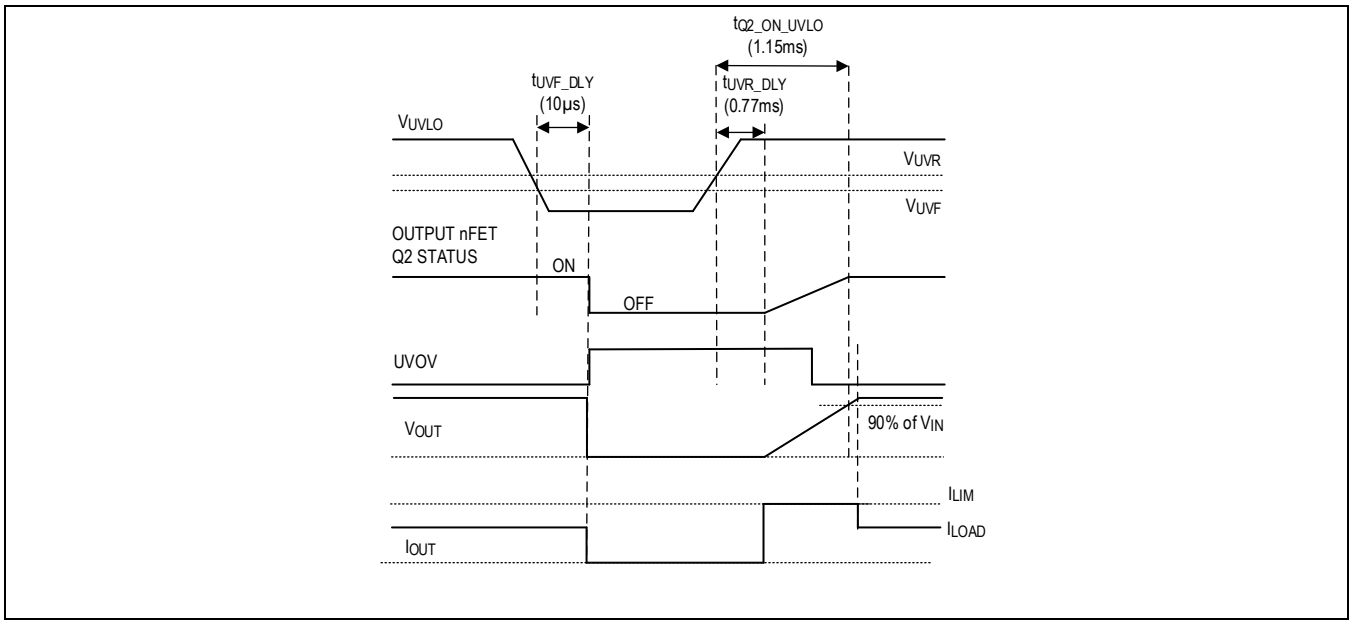


Figure 2. Input Undervoltage Fault Timing Diagram

Input Overvoltage Lockout

Connect an external resistive divider to the OVLO pin as shown in the *Figure 3* to adjust rising input OVLO threshold voltage. Use the following equation to adjust rising input OVLO threshold (V_{OVR}). The recommended value of R3 is 450kΩ–500kΩ.

$$V_{IN\_OVR} = V_{OVR} \times \left(1 + \frac{R3}{R4}\right)$$

where V_{IN_OVR} is the input supply voltage at which the device enters the OVLO condition.

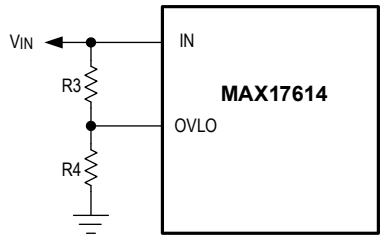


Figure 3. Adjustable Input OVLO

If the voltage at the OVLO pin exceeds V_{OVR}, only the output nFET Q2 is turned off after 0.86µs (t_{OVR_DLY}) and UVOV is asserted high while the input nFET Q1 is kept ON. When the OVLO condition is removed, Q2 turns back on within 18µs ($t_{Q2\_ON\_OVLO}$) and UVOV is deasserted low. *Figure 4* depicts Input overvoltage rising and falling operation.

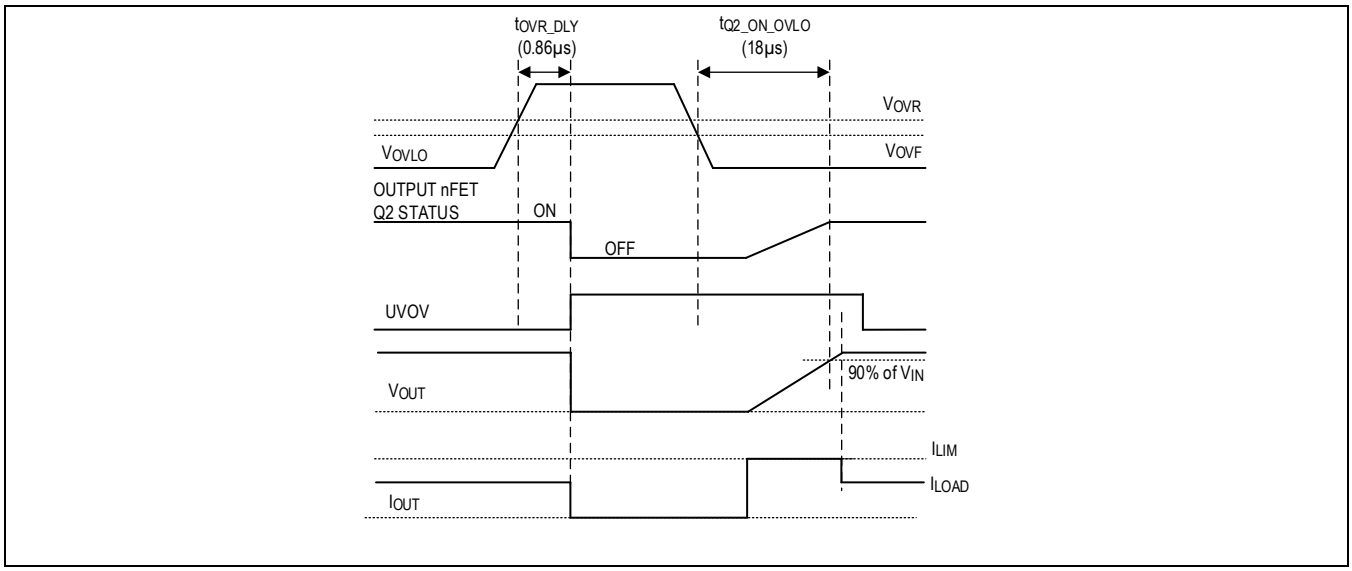


Figure 4. Input Overvoltage Fault Timing Diagram

Input Debounce Protection

The MAX17614 features input debounce protection. The device turns on input nFET Q1 after 200µs (t_{Q1_DLY}) once the input voltage rises above 4.2V (V_{INT_UVR}). The output nFET Q2 is turned on only if the input voltage is higher than the input UVLO threshold for a period greater than 1.25ms (t_{DEB}). The debounce time (t_{DEB}) applies only at power-up of the device. This feature is intended for applications where the EN signal is present when the power supply ramps up. *Figure 5* depicts input debounce timing diagram.

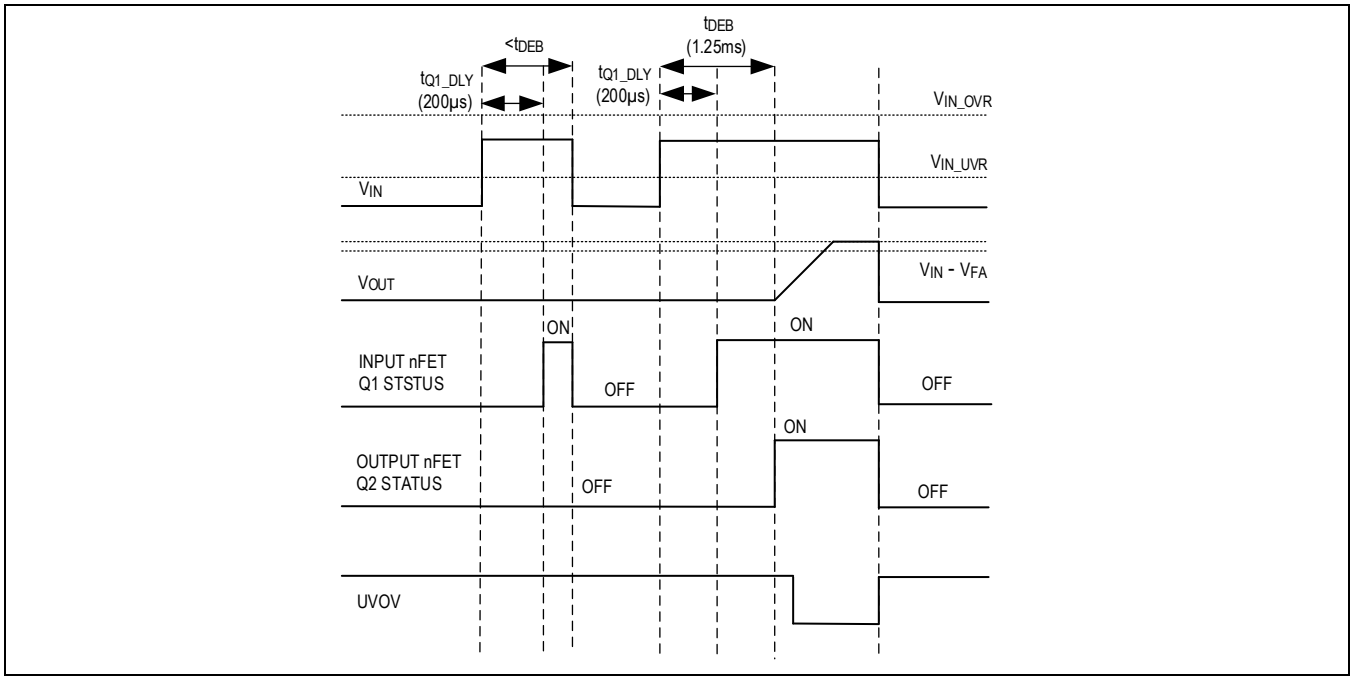


Figure 5. Input Debounce Timing Diagram

Enable (EN)

The MAX17614 is enabled or disabled through the EN pin by driving it above or below EN threshold voltage; as such, the device can be used to turn power delivery to connected loads on or off using the EN pin. The device turns off both internal nFETs when EN is low. In Latch-off mode, toggling the EN pin for at least 5.2µs resets the fault condition, and the device

resumes operation. The EN pin is internally pulled up to 1.4V to have an always ON option when it is left open. Input debounce time (t_{DEB}) is present when the device is turned on through the EN pin.

Setting the Current Limit/Threshold (SETI)

During overload events, the MAX17614 continuously regulates the device current to the current limit (I_{LIM}) programmed by the resistor R_{SETI} connected at the SETI pin. The current limit can be programmed between 0.15A and 3A. Use the following equation to calculate current-limit setting resistor:

$$R_{SETI} = \frac{4548}{I_{LIM}}$$

where I_{LIM} is the desired current limit in mA and R_{SETI} is in kΩ.

The minimum allowed value for R_{SETI} is 1.5kΩ. *Table 1* shows current-limit thresholds for different resistor values.

When the device current reaches the set current limit during overload, short-circuit or when charging large output capacitance during startup, only the internal nFET Q2 is controlled to limit the current to I_{LIM}.

Table 1. Current-Limit Threshold vs. SETI Resistor Values

R_{SETI}(kΩ)	CURRENT LIMIT I_{LIM}(A)
30.10	0.15
15.00	0.3
4.53	1.0
2.26	2.0
1.82	2.5
1.50	3.0

The SETI pin also enables monitoring current flowing from IN to OUT. The IN-to-OUT current is mirrored with a ratio of 3032 (C_{IRATIO}) and flows out through the SETI pin into the external current-limit resistor. The voltage on the SETI pin provides information about the IN-to-OUT current with the following relationship:

$$I_{IN-OUT} = \frac{3.032 \times V_{SETI}}{R_{SETI}}$$

where

I_{IN-OUT} is current flowing from IN-to-OUT in A,

V_{SETI} is SETI pin voltage in V,

R_{SETI} is in kΩ.

Any time SETI is left unconnected, V_{SETI} rises to SETI clamp level (V_{SETI_MAX}) and the device does not allow any current to flow. During startup, this causes the internal nFETs to remain off and $\overline{FLAG}$ to assert after t_{BLANK} elapses**.** During startup, if R_{SETI} is lower than 350Ω, the switches remain off and $\overline{FLAG}$ asserts. For best damped measurement, the capacitance on the SETI pin should be limited to 10pF.

Reverse Current Protection

The MAX17614 reverse current protection feature prevents current flow from the OUT pins to IN pins. The device monitors V_{IN} and V_{OUT} to provide true reverse current blocking. Two reverse current protection features are implemented.

A slow reverse current condition is detected if (V_{IN} - V_{OUT}) < -4.5mV (V_{RIBS}) is present for 17µs (t_{DEBRIB}). During this condition, only the input nFET Q1 turns off and $\overline{FLAG}$ is asserted while the output nFET Q2 is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the part exits reverse current blocking mode, i.e., (V_{IN} - V_{OUT}) > +100mV (V_{RIB_RISING}) has been detected, input nFET Q1 turns back on after 8µs (t_{Q1_ON}) and the $\overline{FLAG}$ pin is deasserted. *Figure 6* depicts slow reverse current blocking operation.

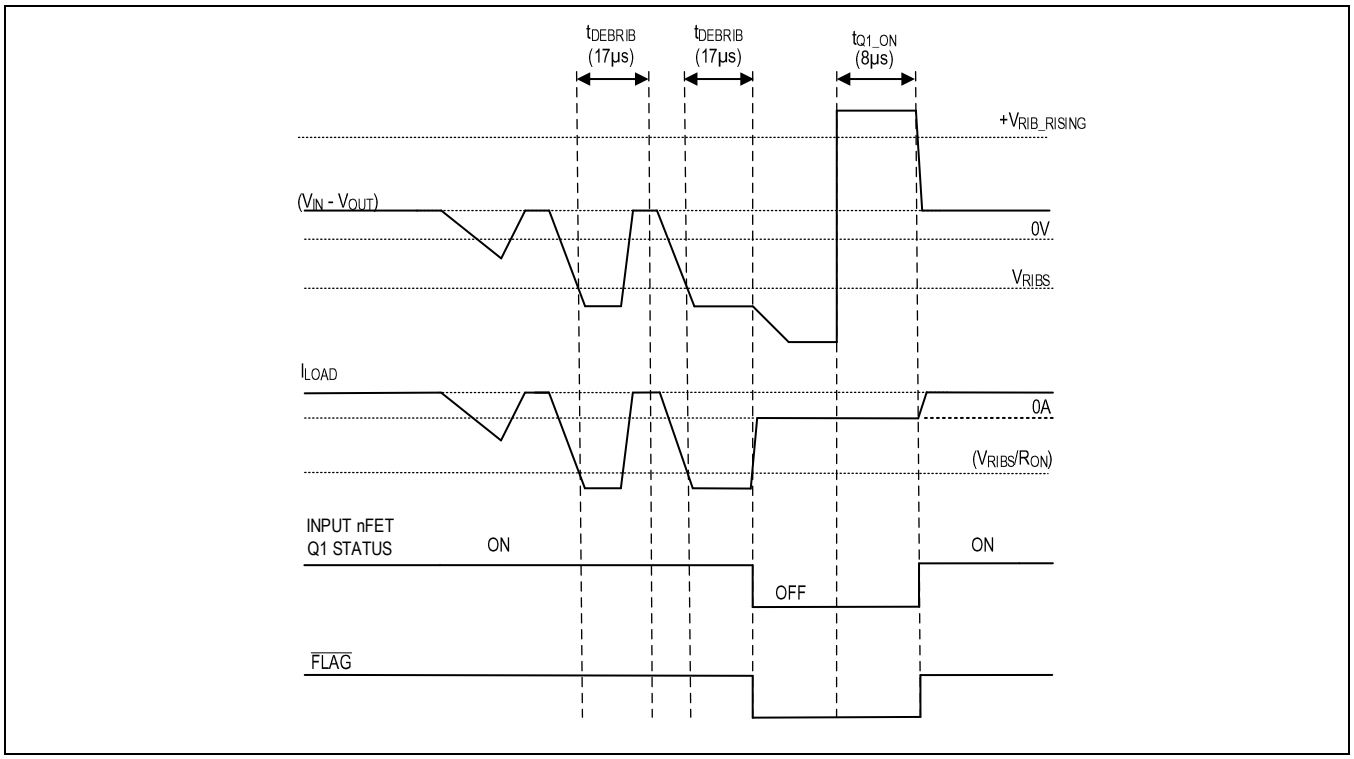


Figure 6. Slow Reverse Current Fault Timing Diagram

For fast reverse current events such as input hard short, the MAX17614 turns off internal nFET Q1 within 140ns (t_{RIB}) after (V_{IN} - V_{OUT}) < -102mV (V_{RIBF}) is detected. During this condition, only the input nFET Q1 turns off and $\overline{FLAG}$ is asserted while the output nFET Q2 is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the part exits reverse current blocking mode, i.e., (V_{IN}-V_{OUT}) > +100mV (V_{RIB_RISING}) has been detected, input nFET Q1 turns back on after 8µs (t_{Q1_ON}) and the $\overline{FLAG}$ pin is deasserted. *Figure 7* depicts fast reverse current blocking operation.

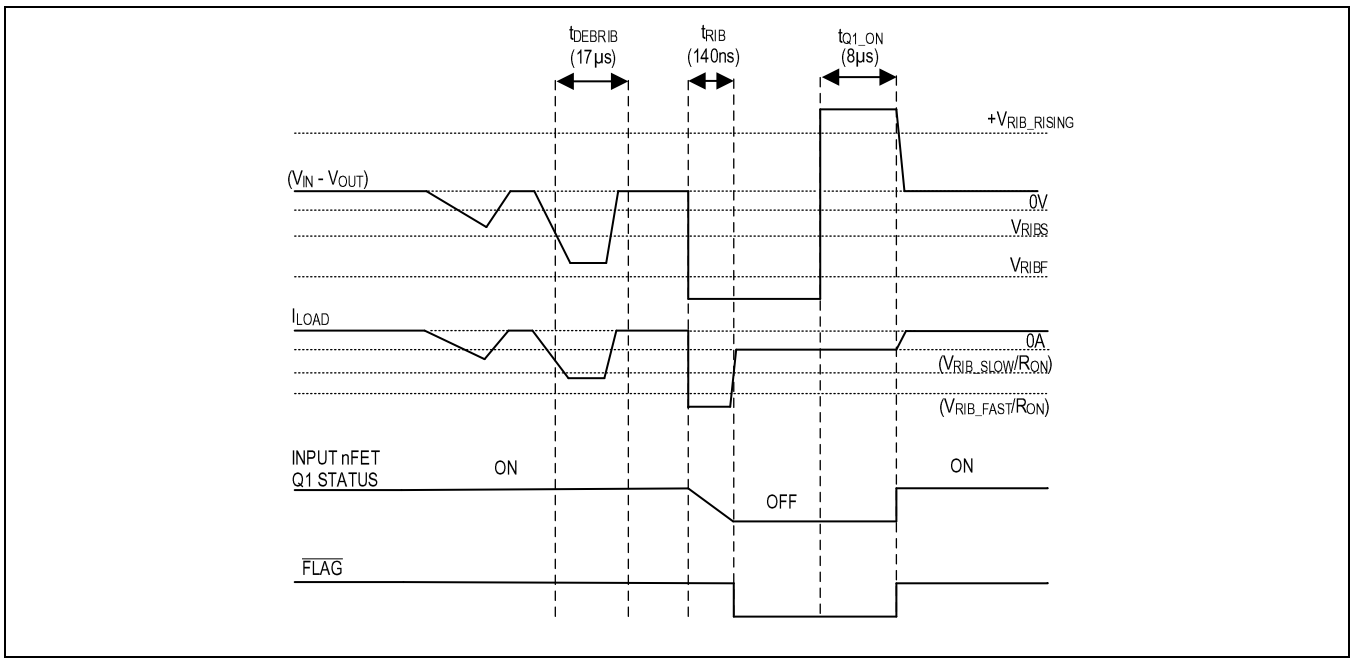


Figure 7. Fast Reverse Current Fault Timing Diagram

Programming Startup Blanking Time (TSTART)

Connecting a capacitor from the TSTART pin to GND programs the startup blanking time. The t_{TSTART} is the time allowed for V_{OUT} to reach the designated value (V_{IN} - V_{FA}) before the device enters fault mode. If the output voltage does not charge to (V_{IN} - V_{FA}) within the programmed time (t_{TSTART}), then the $\overline{FLAG}$ is asserted. When charging large output capacitances, the part may hit thermal shutdown and may cycle ON and OFF as described in *Thermal Shutdown Protection* section. In order to program t_{TSTART}, the capacitor C_{TSTART} connected to the TSTART pin is charged with a constant current of 5µA (typ). When the voltage on the capacitor reaches 1.5V, t_{TSTART} is considered expired and the capacitor is discharged to ground.

$$t_{TSTART} = \frac{C_{TSTART}}{5\mu} \times 1.5$$

The following table presents C_{TSTART} required for different t_{TSTART} durations.

Table 2. C_{TSTART} vs. t_{TSTART}

t_{TSTART} (ms)	C_{TSTART} (nF)
15	50
60	200
300	1000
100	Unconnected

If the TSTART pin is left unconnected or is connected to a very low-value capacitor, then the 1.5V voltage threshold is reached in less than 100µs ($t_{TSTART-UNCONNECTED}$). In this case, the pin is considered unconnected, and the device applies a preset startup time 100ms ($t_{TSTART-DEFAULT}$). *Figure 8* depicts the startup behavior with and without a capacitor at the TSTART pin.

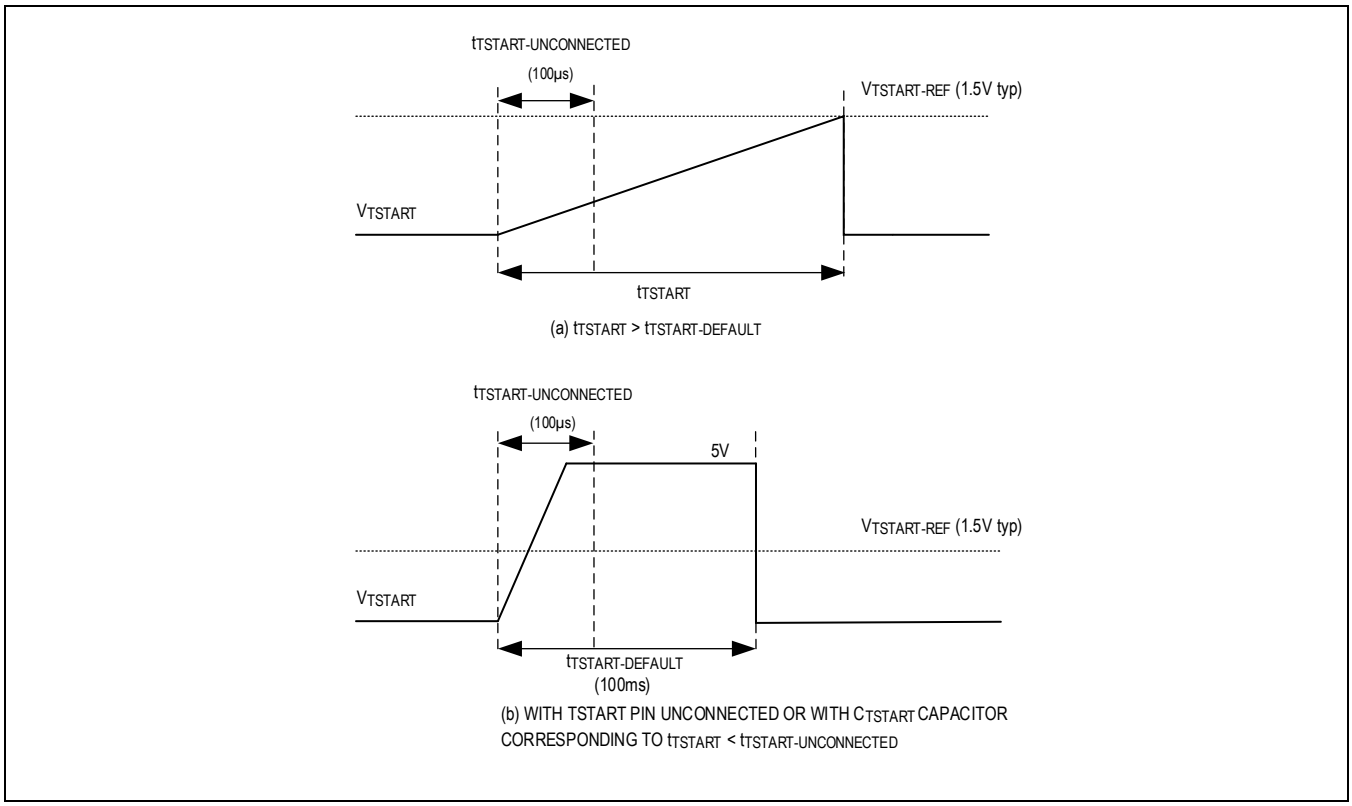


Figure 8. Programming Startup Blanking Time Using C_{TSTART}

Startup Requirements

During startup, the device turns on the internal nFETs after the IN debounce time (t_{DEB}). The output capacitor starts charging with the input current set by SETI resistor current limit. The output capacitor charging profile without output load can be determined by the following equation:

$$V_{OUT}(t) = \frac{I_{LIM} \times t}{C_{OUT}}$$

The charging time for the output capacitance is calculated as follows:

$$t_{charg} = \frac{C_{OUT} \times V_{IN(MAX)}}{I_{LIM}}$$

Figure 9 depicts startup operation for output capacitance without load. Note that the slew rate of V_{OUT} charging is limited to 10V/ms (typ). During startup operation, the part may hit thermal shutdown due to excessive power dissipation and may cycle ON and OFF as described in the *Thermal Shutdown Protection* section.

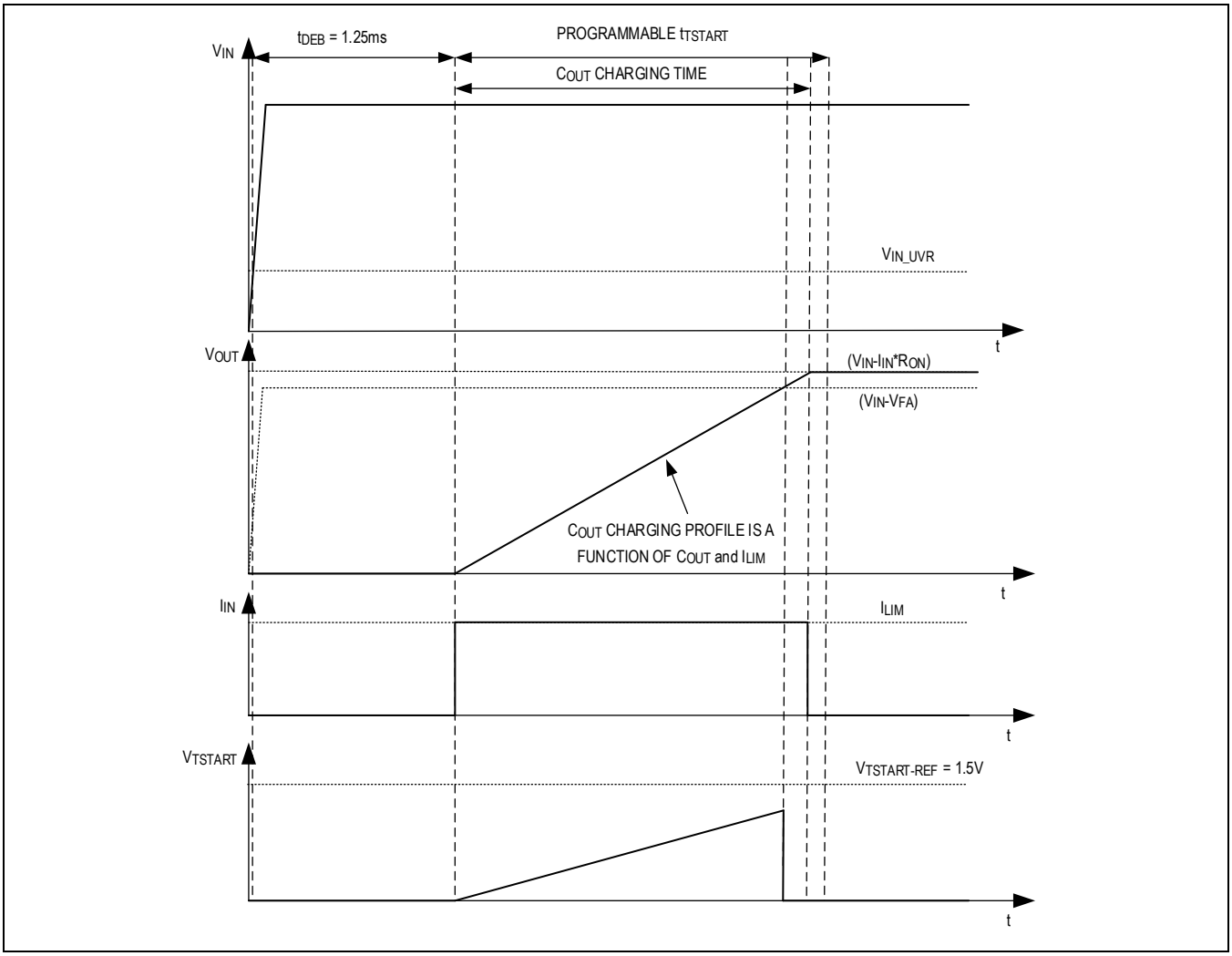


Figure 9. Startup Timing Diagram for Output Capacitance without Load

When the load present is on the output, the output capacitor charging profile with load resistance can be determined by the following equation:

$$V_{OUT}(t) = I_{LIM} \times R_{OUT}\left(1 - e^{-\left(\frac{t}{R_{OUT} * C_{OUT}}\right)}\right)$$

The charging time for the output capacitance is calculated as follows:

$$t_{CHARGE} = R_{OUT} \times C_{OUT} \times \ln\left(\frac{1}{1 - \left(\frac{V_{IN(MAX)}}{I_{LIM} * R_{OUT}}\right)}\right)$$

Figure 10 depicts startup operation for output capacitance with load resistance. Note that the slew rate of V_{OUT} charging is limited to 10V/ms (typ). During startup operation, the part may hit thermal shutdown due to excessive power dissipation and may cycle ON and OFF as described in *Thermal Shutdown Protection* section.

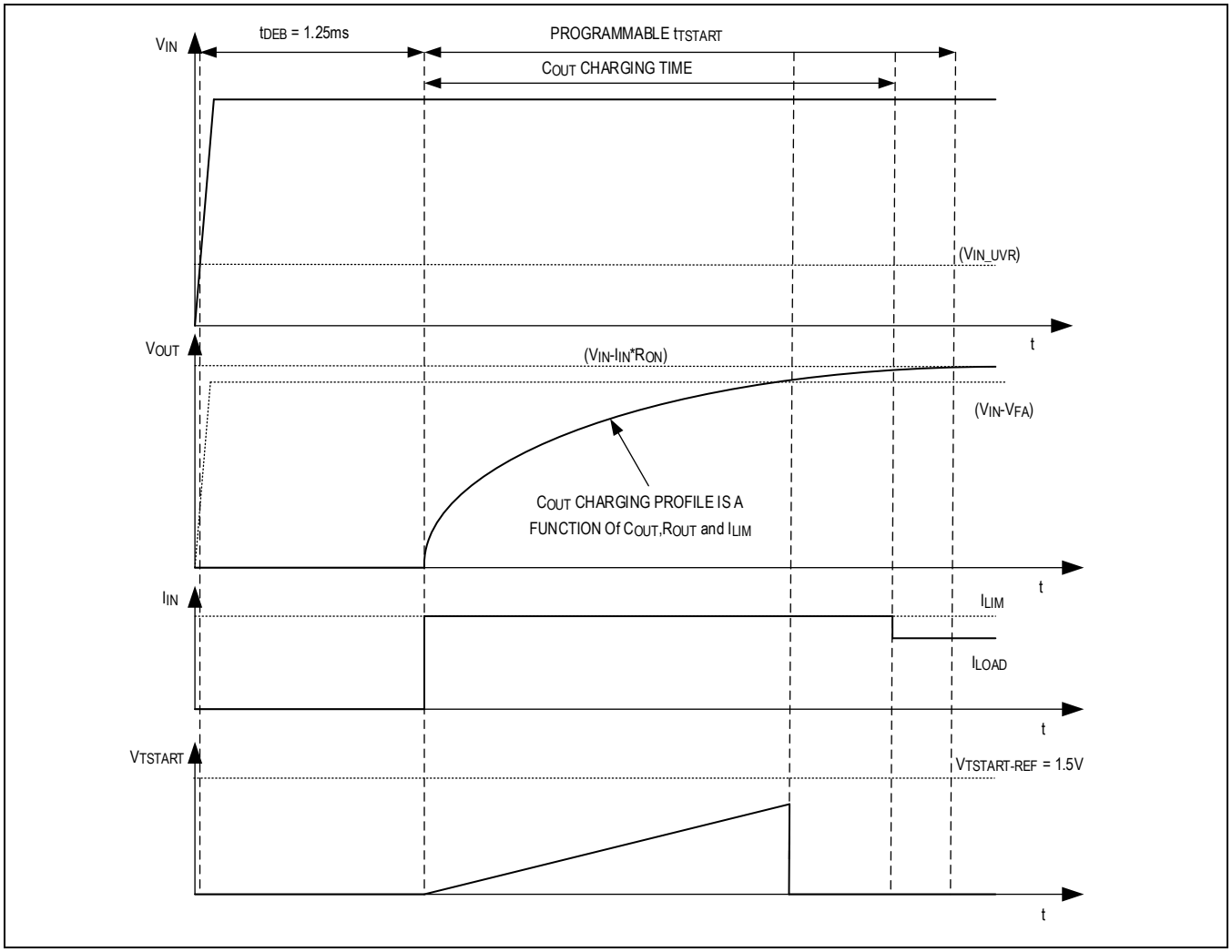


Figure 10. Startup Timing Diagram for Output Capacitance with Load Resistance

To avoid a startup blanking time fault condition, C_{TSTART} should be selected by the following equation:

$$C_{TSTART} \geq 3.3 \times t_{CHARGE}$$

where

C_{TSTART} is in nF,

C_{OUT} is maximum output capacitance in µF,

$V_{IN(MAX)}$ is the maximum input voltage in V,

t_{CHARGE} is in ms.

Once V_{OUT} reaches the designated value (V_{IN} - V_{FA}) within t_{TSTART}, timer t_{START} resets.

To avoid thermal shutdown during startup, the junction temperature of the device must be maintained below the thermal shutdown threshold. The power dissipation of the device during startup is generally greater in magnitude than the steady state power dissipation and is function of input voltage, load resistance, output capacitance, and programmed current limit. The junction temperature of the device during startup is a function of power dissipation during startup, thermal resistance, and thermal capacitance of the device package, assuming that the thermal capacitance of the printed circuit board is much greater. This assumption is usually true in most practical environments. These factors decide the maximum output capacitance that can be placed on the OUT terminals for a given current limit (I_{LIM}) setting.

Current Limit Type Selection (CLMODE)

The CLMODE pin can be used to program the overcurrent limit response of the device in one of the following three current-limit modes:

- Autoretry mode: CLMODE pin is left unconnected
- Continuous mode: CLMODE is connected to GND
- Latch-off mode: a 150kΩ resistor between CLMODE and GND

In all three current-limit modes, if the current through the device reaches the current-limit threshold, the device limits output current to the programmed current limit by controlling the internal nFET Q2. The following sections present the current limit operation of the MAX17614 in each mode during the startup phase and in steady state operation.

Continuous Current-Limit Mode

After the input debounce time (t_{DEB}) is completed, the device starts charging the output capacitor with a current I_{LIM} during startup blanking time (t_{TSTART}). If the output voltage V_{OUT} reaches the designated value (V_{IN} - V_{FA}) within t_{TSTART}, the t_{TSTART} timer resets and the normal operation continues. If the output voltage V_{OUT} does not reach (V_{IN} - V_{FA}) within t_{TSTART} due to overload on the output, the t_{TSTART} timer resets, the $\overline{FLAG}$ pin asserts, and the operation continues. The $\overline{FLAG}$ deasserts after V_{OUT} reaches the designated value (V_{IN} - V_{FA}). *Figure 11* depicts startup behavior in continuous current-limit mode.

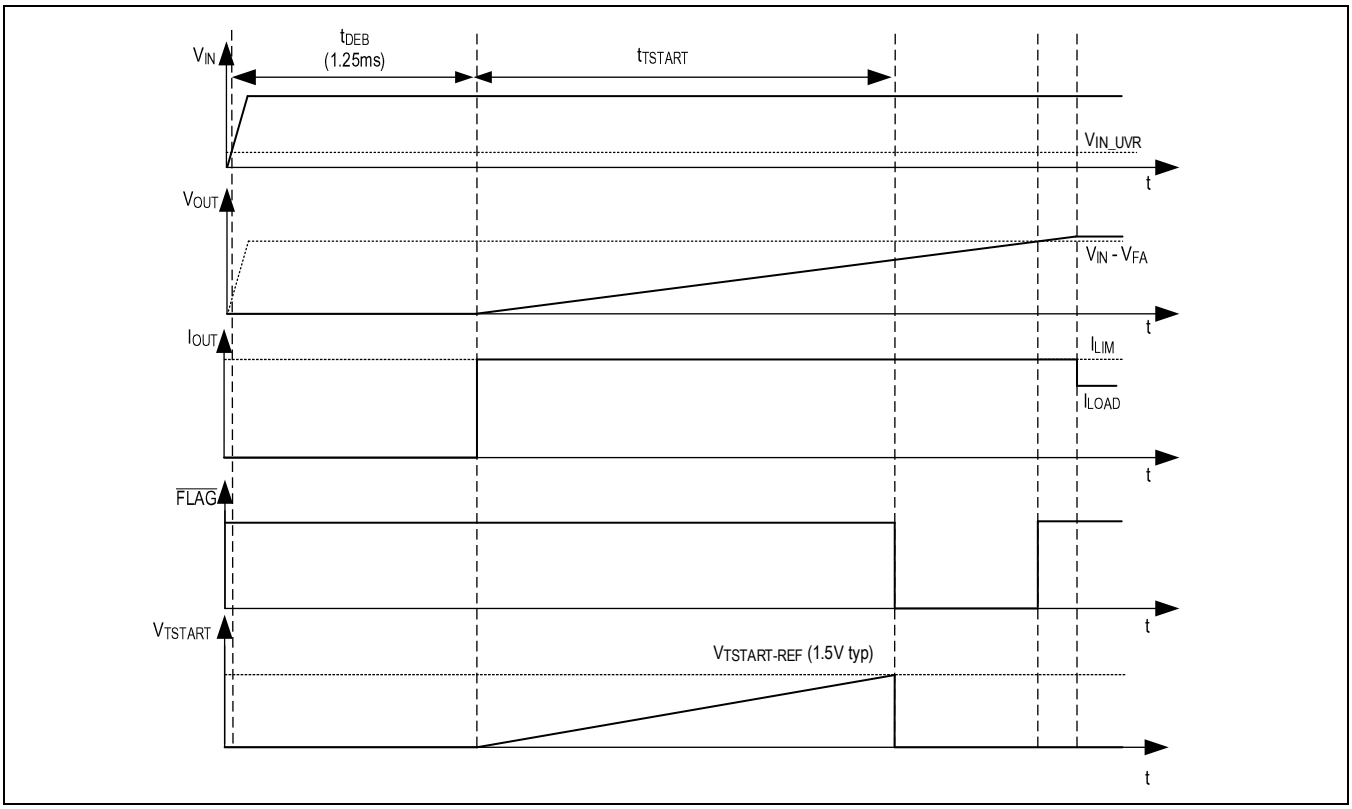


Figure 11. Startup Fault Timing Diagram in Continuous Current-Limit Mode

In continuous current-limit mode, if the device enters current limit condition during normal operation, the t_{BLANK} timer starts. The t_{BLANK} timer resets if the current limit condition resolves before the t_{BLANK} duration has elapsed and the normal operation continues. If the current limit condition exists for the t_{BLANK} duration, the t_{BLANK} timer resets, the $\overline{FLAG}$ pin asserts, and the operation continues. The $\overline{FLAG}$ deasserts after V_{OUT} reaches the designated value (V_{IN} - V_{FA}). *Figure 12* depicts continuous current-limit mode operation during overload event in normal operation.

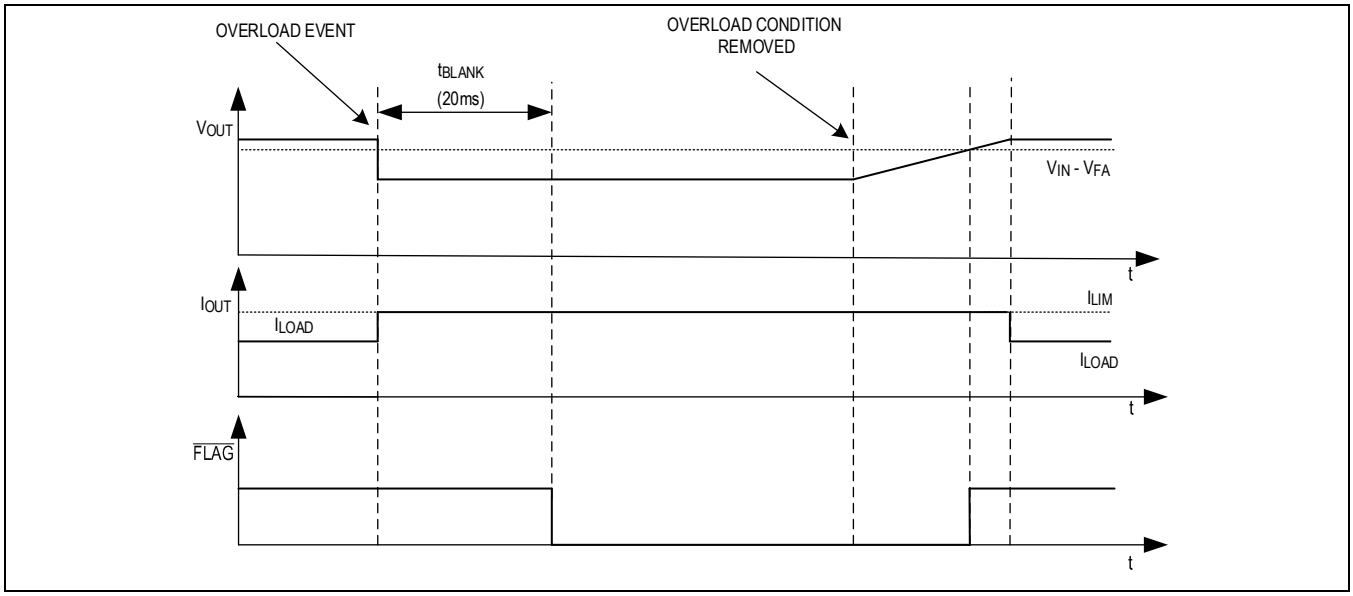


Figure 12. Overload Fault Timing Diagram in Continuous Current-Limit Mode

During current limit condition in startup and steady state operation, the part may hit thermal shutdown due to excessive power dissipation and may cycle ON and OFF as described in *Thermal Shutdown Protection* section.

Autoretry Current-Limit Mode

During startup in autoretry current-limit mode, the device operates in continuous current-limit mode until t_{TSTART}. If the output voltage V_{OUT} does not reach (V_{IN} - V_{FA}) within t_{START} due to overload on the output, then output nFET Q2 is turned off, the timer t_{TSTART} resets, and the $\overline{FLAG}$ pin asserts while the input nFET Q1 is kept ON. A retry time delay (t_{RETRY}) starts after t_{TSTART} has elapsed. During t_{RETRY} time, Q2 remains off. Once the t_{RETRY} time has elapsed, the device reinitiates the startup cycle again. If overload on the output still exists, autoretry startup cycle is repeated and the $\overline{FLAG}$ pin remains asserted. If the overload condition is resolved and the output voltage (V_{OUT}) reaches the designated value (V_{IN} - V_{FA}), Q2 stays on and the $\overline{FLAG}$ pin deasserts. *Figure 13* depicts startup behavior in autoretry current-limit mode.

During normal operation in autoretry current-limit mode, if the part enters current limit condition, then the t_{BLANK} timer starts. The t_{BLANK} timer resets if the current limit condition resolves before the t_{BLANK} duration has elapsed, and normal operation continues. If the current limit condition is present for t_{BLANK}, the output nFET Q2 is turned off, the t_{BLANK} timer resets, and the $\overline{FLAG}$ asserts while the input nFET Q1 is kept on. A t_{RETRY} delay starts after t_{BLANK} has elapsed. During the t_{RETRY} interval, Q2 remains turned off. Once t_{RETRY} has elapsed, the device initiates a startup cycle. *Figure 14* depicts autoretry current-limit mode operation during overload event in normal operation.

During current limit condition in startup and steady state operation, the part may hit thermal shutdown due to excessive power dissipation and may cycle ON and OFF as described in *Thermal Shutdown Protection* section.

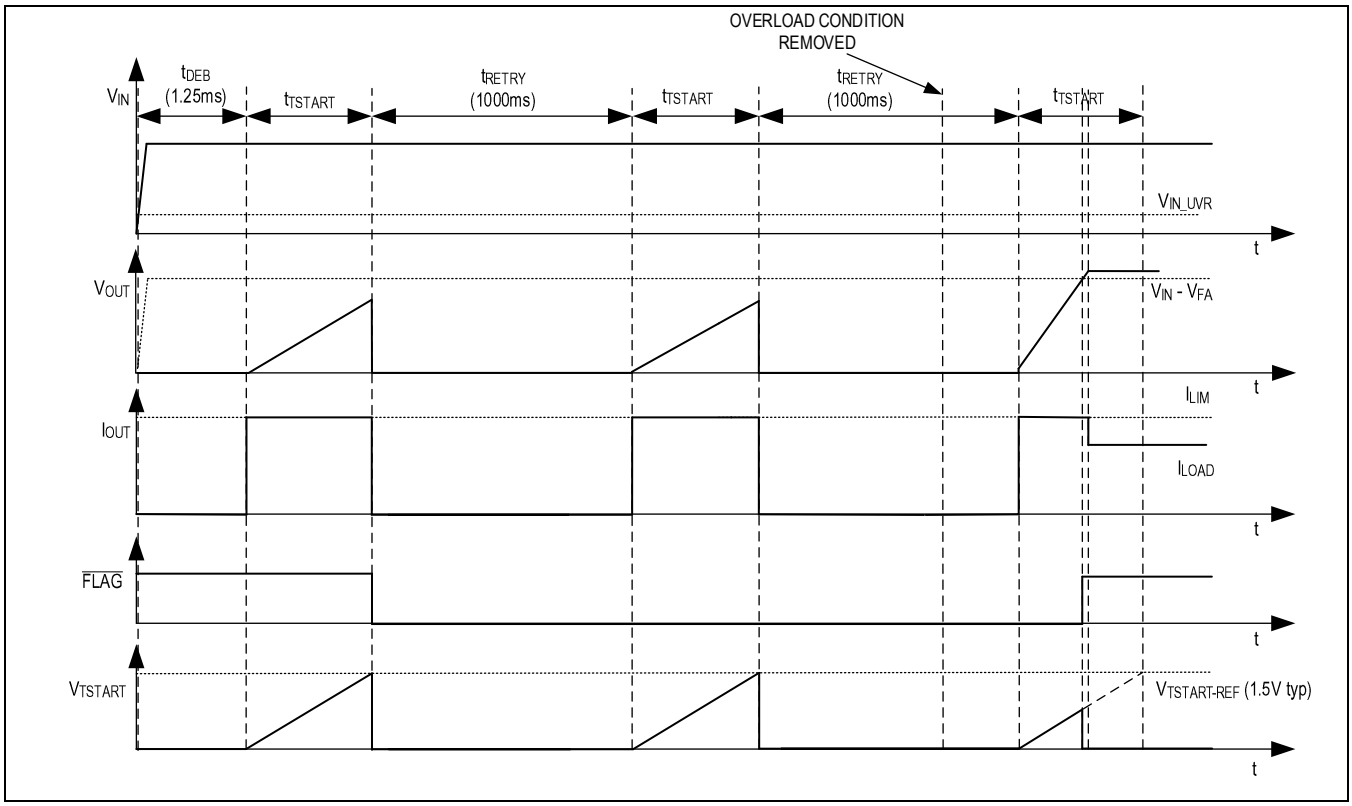


Figure 13. Startup Fault Timing Diagram in Autoretry Current-Limit Mode

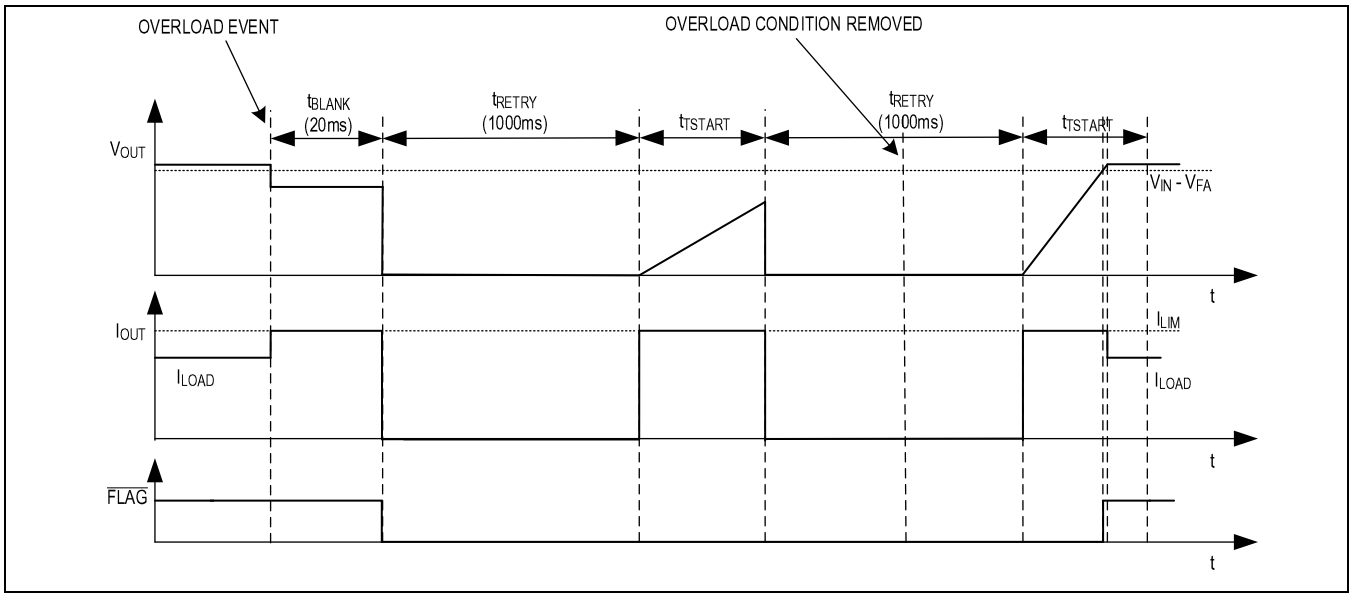


Figure 14. Overload Fault Timing in Autoretry Current-Limit Mode

The autoretry feature reduces system average power dissipation compared to continuous current-limit mode in case of overload or short-circuit conditions. The average power dissipation in the device for an output short-circuit condition can be calculated by the following equation:

$$P_D \cong V_{IN} \times I_{LIM} \times \left[\frac{t_{START}}{t_{START} + t_{RETRY}}\right]$$

For a current-limit threshold setting of 1A, output voltage of 24V, and output capacitance of 100µF, the programmed t_{TSTART} time is 4.5ms. With 1000ms (typ) of t_{RETRY} time, the duty cycle is 0.45%, resulting in an average power dissipation of only 108mW.

Latch-Off Current-Limit Mode

During startup in latch-off current-limit mode, the device operates in continuous current-limit mode until t_{TSTART}. If the output voltage V_{OUT} does not reach (V_{IN} - V_{FA}) within t_{START} due to overload on the output, then output nFET Q2 is turned off and latched, the timer t_{TSTART} resets, and the $\overline{FLAG}$ pin asserts while the input nFET Q1 is kept ON. To reset the device, either toggle the enable control signal (EN) or cycle the input voltage. *Figure 15* depicts startup behavior in latch-off current-limit mode.

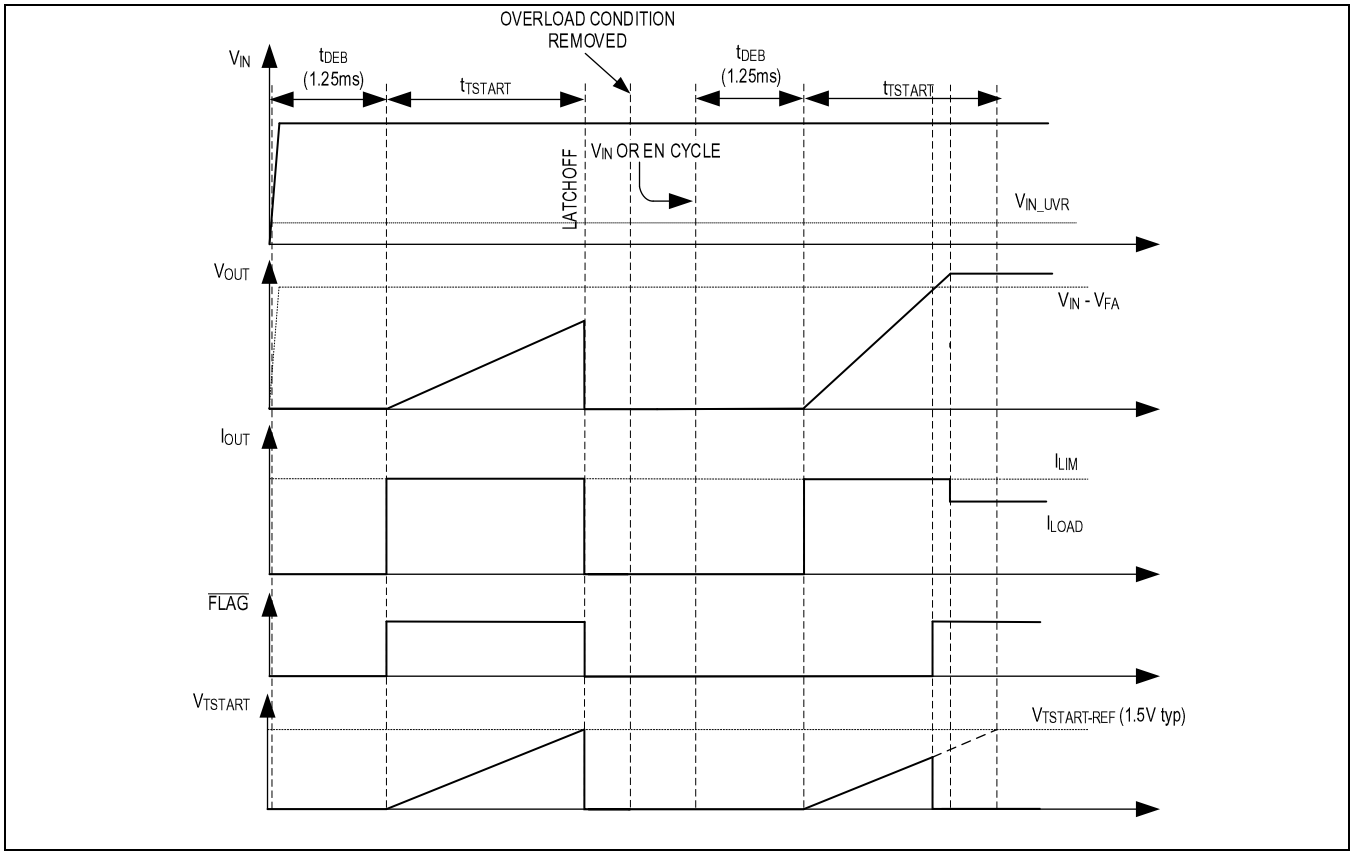


Figure 15. Startup Fault Timing Diagram in Latchoff Current-Limit Mode

In latch-off current-limit mode during normal operation, if the device enters current limit condition, then the t_{BLANK} timer starts. If the current limit condition exists for the t_{BLANK} duration, the output nFET Q2 is turned off and latched, the t_{BLANK} timer resets, and the $\overline{FLAG}$ pin asserts while the input nFET Q1 is kept on. To reset the device, either toggle enable control signal (EN) or cycle the input voltage. *Figure 16* depicts latch-off current-limit mode operation during overload event in normal operation.

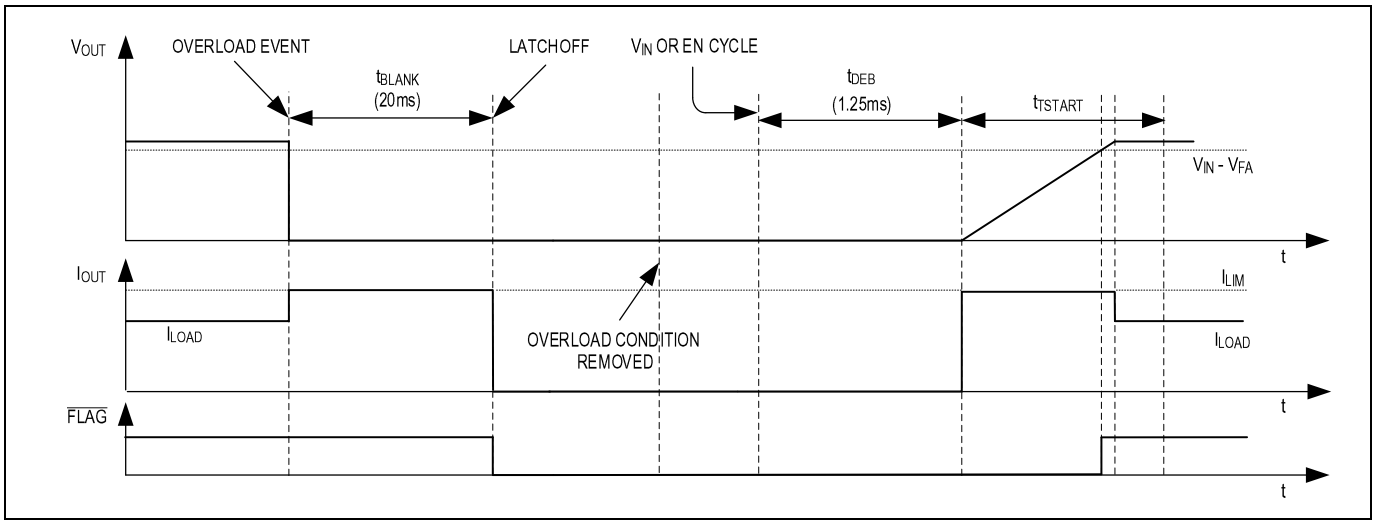


Figure 16. Overload Fault Timing Diagram in Latchoff Current-Limit Mode

During current limit condition in startup and steady state operation, the part may hit thermal shutdown due to excessive power dissipation and may cycle ON and OFF as described in *Thermal Shutdown Protection* section.

Short-Circuit Protection

During a hard output short-circuit event, the current through the device increases very rapidly. The MAX17614 incorporates a fast-trip current comparator to limit the output short-circuit peak current. The fast-trip current comparator turns off only the internal nFET Q2 within 1.5µs (t_{DELAY1}), when the current through the nFET exceeds I_{OCP}. The I_{OCP} is internally set to 8.5A (typ). After a time delay of 580µs (t_{DELAY2}), the device turns back on and limits the output current to programmed current limit within 360µs (t_R) and operates as described in earlier current-limit mode sections. *Figure 17* illustrates the behavior of the system when the current exceeds the I_{OCP} threshold.

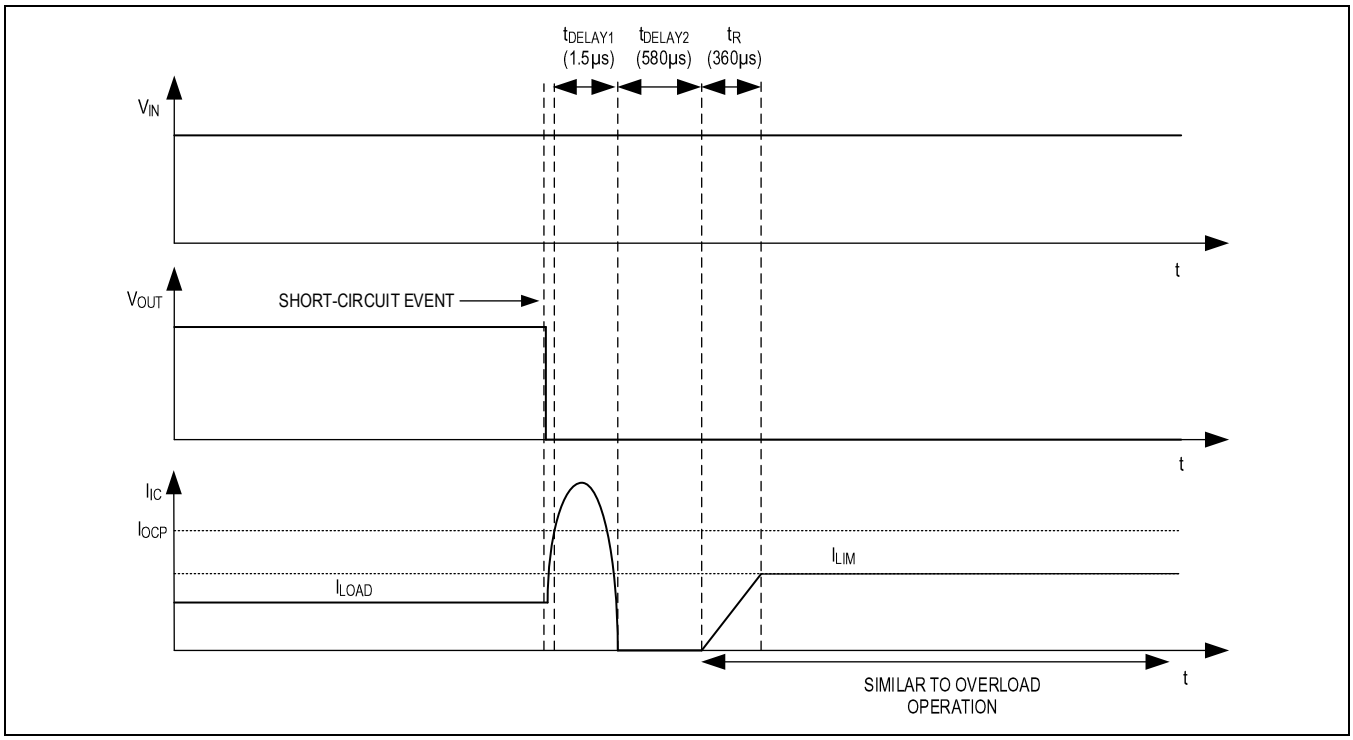


Figure 17. Fast Overcurrent Trip Timing Diagram

When the MAX17614 is started with short-circuit on the output, the device limits the load current to the programmed current limit and behaves similar to overload condition.

Fault Outputs

The MAX17614 device has two open-drain fault outputs, $\overline{FLAG}$ and UVOV. The $\overline{FLAG}$ pin goes low when any of the following conditions occur:

- Current limit duration exceeds blanking time t_{BLANK} during normal operation.
- Output voltage does not reach (V_{IN} - V_{FA}) within startup blanking time (t_{TSTART}) during the startup cycle.
- Reverse current is detected.
- Thermal shutdown is active.
- R_{SETI} is less than 1.5kΩ (max).

See the *Input Undervoltage Lockout* and *Input Overvoltage Lockout* sections for UVOV functionality.

The following table describes the status of the internal nFETs in various fault conditions.

Table 3. Internal FETs Status During Faults

CONDITION	Q1 STATUS	Q2 STATUS	$\overline{FLAG}$ STATUS	UVOV STATUS
No Fault	ON	ON	HIGH	LOW
Input UVLO below V_{UVF}	ON	OFF	HIGH	HIGH
Input OVLO above V_{OVR}	ON	OFF	HIGH	HIGH
Reverse Current Blocking With no other fault	OFF	ON	LOW	LOW
Current limit duration exceeds t_{BLANK} during normal operation	ON	X (*Note 11*)	LOW (*Note 11*)	LOW
Overcurrent Protection (I_{OCP}, 8.5A)	ON	OFF (*Note 12*)	LOW (*Note 12*)	LOW
EN is low	OFF	OFF	HIGH	HIGH
Thermal Shutdown	ON	OFF	LOW	LOW
SETI Grounded (*Note 13*)	OFF	OFF	LOW	LOW
Current limit duration exceeds t_{TSTART} during startup operation	ON	X (*Note 14*)	LOW (*Note 14*)	LOW

Note 11: For continuous current-limit mode: Q2 is on, $\overline{FLAG}$ is pulled low after t_{BLANK}. For latch-off and autoretry current-limit modes: Q2 turns off and $\overline{FLAG}$ is pulled low after t_{BLANK}.

Note 12: For continuous current-limit mode: Q2 is turned off instantly, then turned back on after t_{DELAY2} (580µs) with current limit ramps up in t_R (360µs) duration; $\overline{FLAG}$ is pulled low after t_{BLANK}. For latch-off and autoretry current-limit modes: Q2 is turned off instantly, then turned back on after tDELAY2 (580µs) with current limit ramps up in t_R (360µs) duration; Q2 turns off and $\overline{FLAG}$ is pulled low if overload condition is present beyond t_{BLANK}.

Note 13: This condition is checked only at the power on.

Note 14: For continuous current-limit mode: Q2 is on, $\overline{FLAG}$ is pulled low after t_{TSTART}. For latch-off and autoretry current-limit modes: Q2 turns off and $\overline{FLAG}$ is pulled low after t_{TSTART}.

Thermal Shutdown Protection

The MAX17614 has the thermal shutdown feature to protect against overheating. The device turns off only output nFET Q2 and the $\overline{FLAG}$ pin asserts when the junction temperature exceeds T_J (+155°C typ). The device exits thermal shutdown and resumes operation after the junction temperature cools down by $T_{J(HYS)}$ (15°C typ), except when in latch-off mode, where the device needs either EN or input voltage to be cycled to restart. There is no blanking time for thermal protection. Thermal shutdown may occur during overload, short-circuit, or starting into large output capacitances, when the device experiences high power dissipation.

Applications Information

Ideal Diode/Power MUX Application

The conventional redundant power architecture solution to support a critical load is to “OR” two power sources using Schottky diodes. In this scheme, if one of the Power sources were to fail, switchover to the other source occurs smoothly without interruption of power to the load. However, the Schottky-based solution suffers from power loss and higher temperature rise, while also requiring a large number of discrete components for implementation of other important protection features such as current limit, UVLO, and OVLO.

The MAX17614 device with internal back-to-back nFETs provides a highly integrated, efficient, and reliable ideal diode solution for fast and seamless switchover response while delivering significant reduction in component count and design complexity. *Figure 18* shows an ideal diode implementation with two MAX17614 devices.

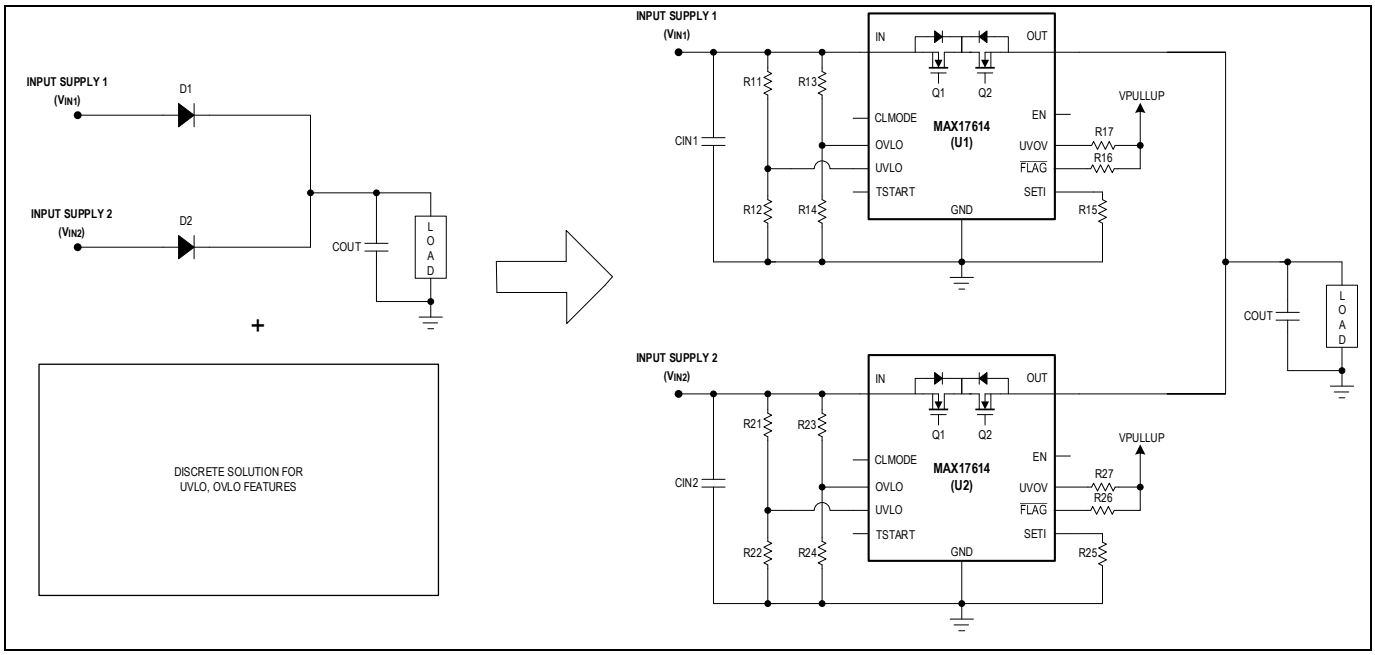


Figure 18. Ideal Diode/Power MUX Implementation Using Two MAX17614s

A fast reverse comparator in the MAX17614 monitors the voltage drop across IN-to-OUT terminals and controls the internal nFET Q1 and turns Q1 ON/OFF with hysteresis as shown in *Figure 19.*

1) The internal nFET Q1 is turned off within 140ns (t_{RIB}) once a fast reverse condition is detected, i.e., (V_{IN} - V_{OUT}) falls below -102 mV.

2) The internal nFET Q1 is turned off after 17µs (t_{DEBRIB}) once a slow reverse condition is detected, i.e., (V_{IN} - V_{OUT}) falls below -4.5 mV.

3) The internal nFET is turned on after 8µs (t_{Q1_ON}) once the reverse current condition has been removed, i.e., (V_{IN} - V_{OUT}) exceeds +100 mV.

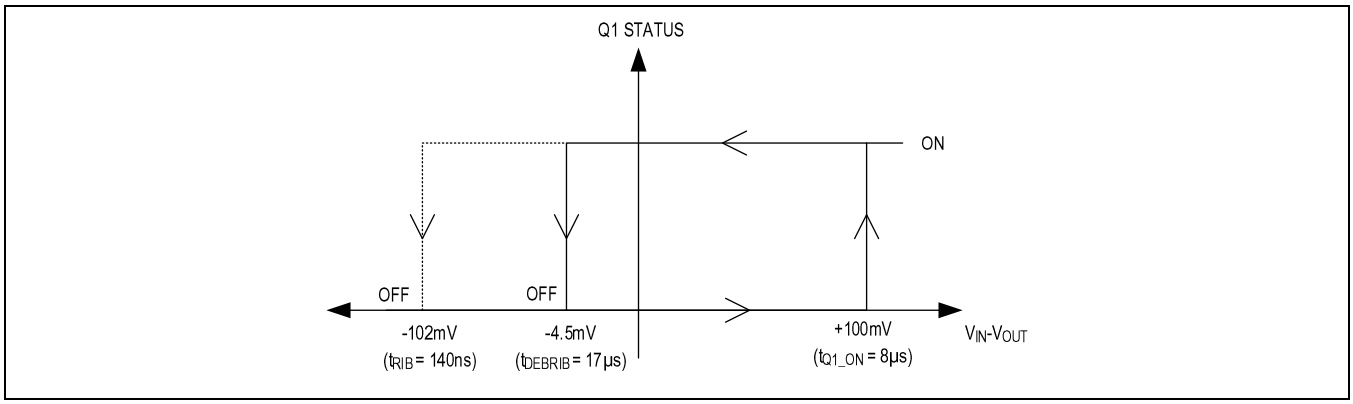


Figure 19. Q1 Turns ON/OFF Status

Figure 20 depicts timing diagram for load switchover from main power source (V_{IN1}) to backup power source (V_{IN2}) for ideal diode implementation using the MAX17614.

The load is initially supported by main power source in steady state since $V_{IN1} > V_{IN2}$. In this state, device U1 is in forward conduction state (both Q1, Q2 are ON) and device U2 is in reverse blocking state (Q1 is OFF, Q2 is ON) since $V_{OUT} > V_{IN2}$. In this state, if V_{IN1} were to ramp down due to failure of power, V_{OUT} follows V_{IN1} by a voltage drop that is equal to the product of internal nFETs ON-resistance and current through U1. When V_{IN1} has fallen to a level such that (V_{IN2} - V_{OUT}) > +100mV, U2 exits its reverse blocking condition and turns ON its internal nFET Q1 after 8µs (t_{Q1_ON}). The V_{IN2} starts supporting the output load since $V_{IN2} > V_{IN1}$. The turn-ON of Q1 in U2 instantaneously raises V_{OUT} by a voltage drop equal to Q1 body diode voltage drop. This causes the fast reverse comparator of U1 to turn off only its internal nFET Q1 within 140ns (t_{RIB}) once (V_{IN1} - V_{OUT}) falls below -102 mV while its Q2 is kept ON. Both U1 and U2 share the load current until the internal nFET Q1 of U1 is turned OFF without interrupting normal operation.

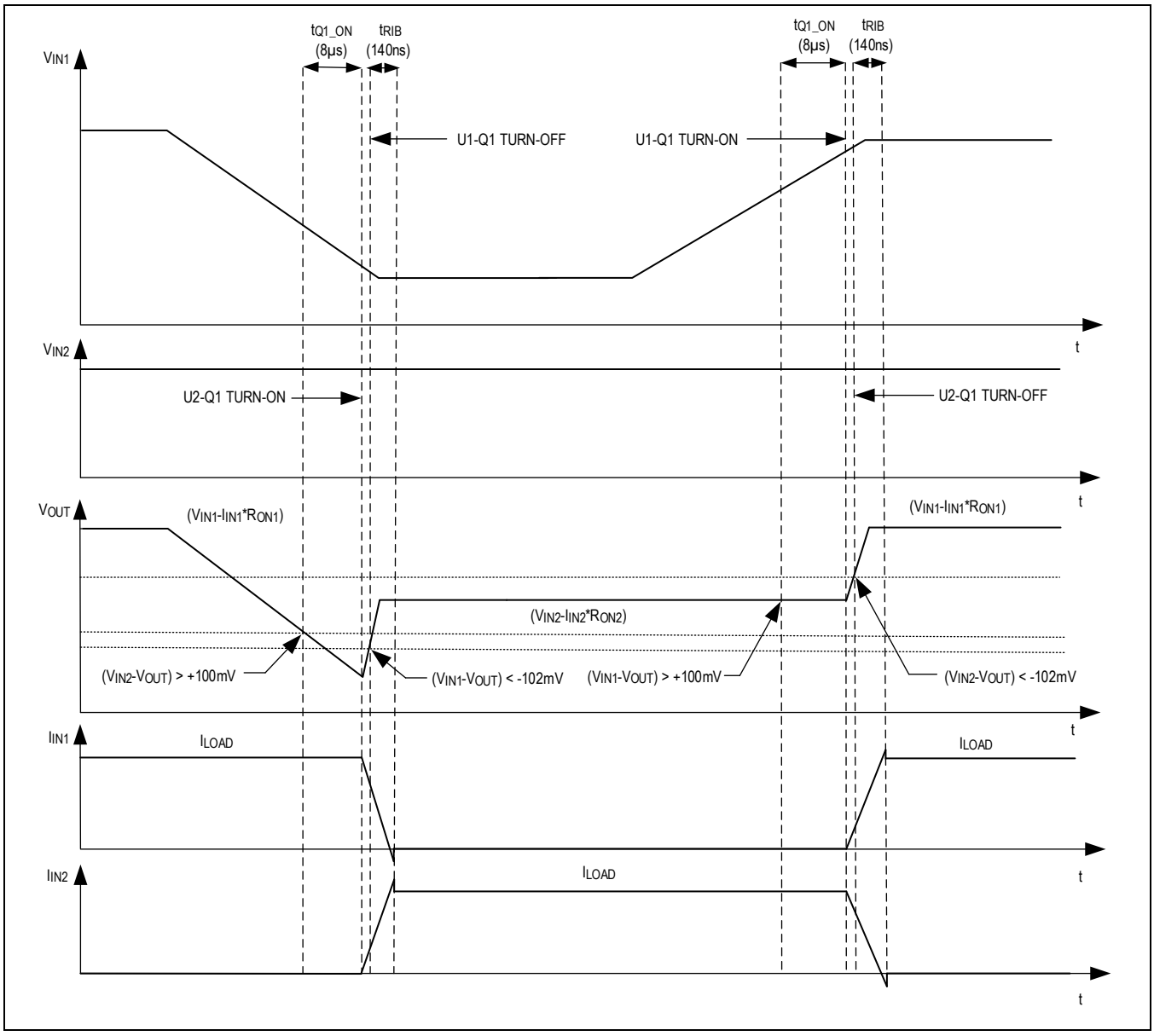


Figure 20. MAX17614 Ideal Diode Implementation Timing Diagram

The output load is now supported by V_{IN2} in steady state since $V_{IN2} > V_{IN1}$: The device U1 is in reverse blocking state (Q1 is OFF, Q2 is ON) and the device U2 is in forward conduction state (both Q1, Q2 are ON). When V_{IN1} recovers and ramps up, U1 turns ON its internal nFET Q1 after 8µs (t_{Q1_ON}) once the reverse condition has been removed, i.e., (V_{IN1} - V_{OUT}) exceeds +100 mV. The V_{IN1} starts supporting the output load since $V_{IN1} > V_{IN2}$. The output voltage starts ramping up until the steady state output is reached, i.e., the output voltage is a function of main supply voltage, U1 internal ON resistance, and load current. The U2 turns off only its internal nFET Q1 within 140ns (t_{RIB}) once (V_{IN2} - V_{OUT}) falls below -102mV while its Q2 is kept ON. Both U1 and U2 share the load current until the internal nFET Q1 of U2 is turned OFF without interrupting normal operation.

Thus, the MAX17614 helps implement an ideal diode OR-ing solution that seamlessly transfers the load from main power (V_{IN1}) to the backup source (V_{IN2}), and then back to V_{IN1}, while providing significant power loss savings compared to a Schottky-based solution.

Power Source Selector

The EN pin of the MAX17614 allows a system microcontroller to turn ON/OFF power to the load, thus enabling the system to select a power source based on operating conditions.

Figure 21 depicts the timing diagram for Power Source Selector implementation using two MAX17614 devices. The output load is initially supported by V_{IN1} in steady state since $V_{IN1} > V_{IN2}$, i.e., the initial output voltage is a function of main supply voltage V_{IN1}, U1 internal ON-resistance, and load current. The device U1 is in forward conduction state (both Q1, Q2 are ON) and the device U2 is in reverse blocking state (Q1 is OFF, Q2 is ON).

When Enable signal (EN1) of U1 goes low, the internal nFETs Q1, Q2 of U1 are turned OFF. The output capacitor starts discharging to support the load. The U2 turns ON its internal Q1 after 8µs (t_{Q1_ON}) once the reverse condition has been removed, i.e., (V_{IN2} - V_{OUT}) exceeds +100 mV. The V_{IN2} starts supporting the load current and the output voltage starts ramping up until the steady state output is reached, i.e., the output voltage is a function of V_{IN2}, U2 internal ON-resistance, and load current.

When Enable signal (EN1) of U1 is restored back, U1 turns on its input nFET Q1 after 200µs (t_{Q1_DLY}) and output nFET Q2 after 1.25ms (t_{DEB}). The V_{IN1} starts supporting the output load since $V_{IN1} > V_{IN2}$. The output voltage is a function of V_{IN1}, U1 internal ON-Resistance, and load current. The U2 turns off only its input nFET Q1 within 140ns (t_{RIB}) once (V_{IN2} - V_{OUT}) falls below -102mV while its output nFET Q2 is kept ON. Both U1 and U2 share the load current until the internal nFET Q1 of U2 is turned OFF without interrupting normal operation.

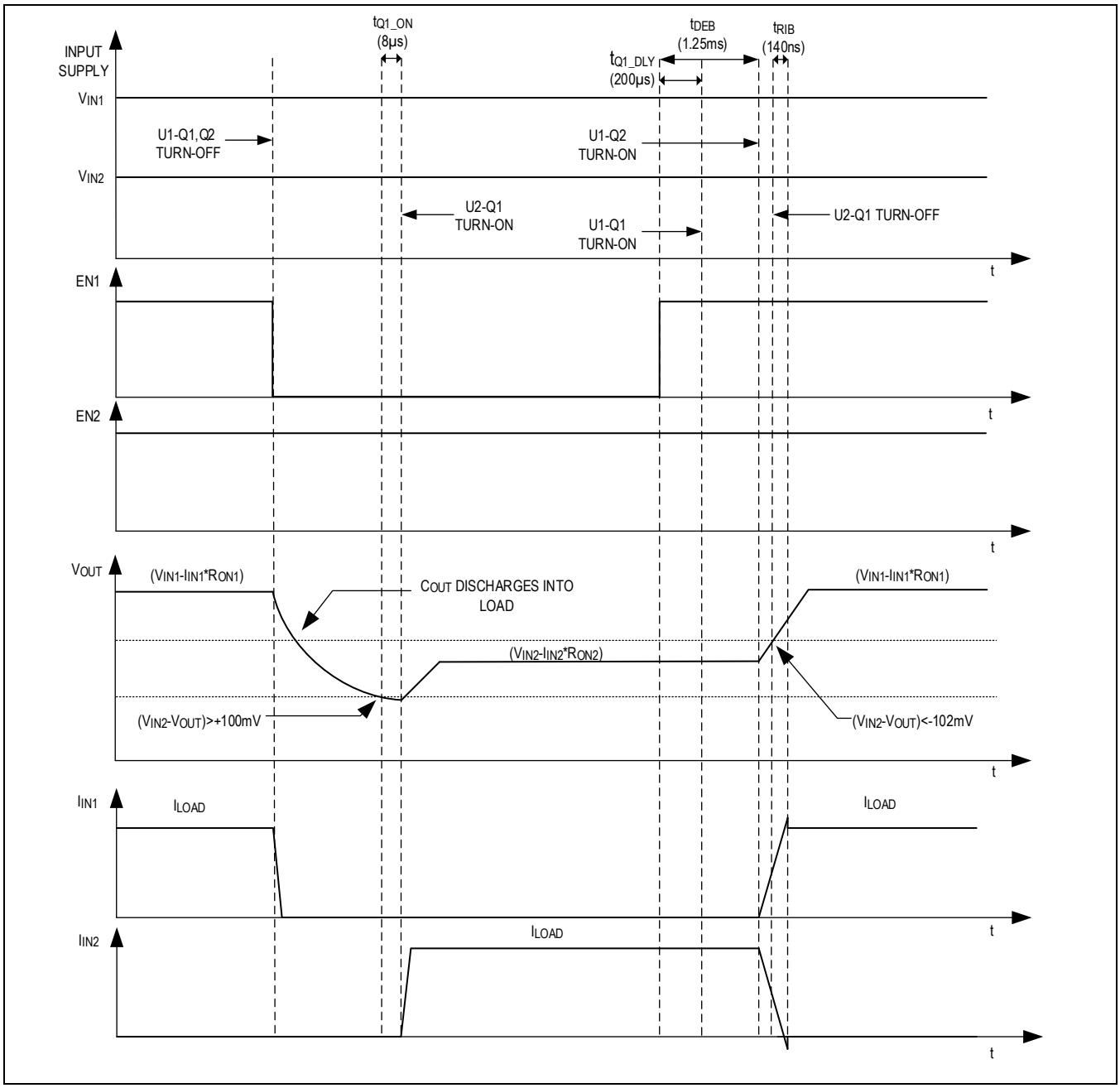


Figure 21. Power Source Selector Timing Diagram

Priority Power Source Selector

The OVLO and UVOV pins of the MAX17614 can be configured for Priority Power Source Selector implementation as shown in Typical Application Circuits *Figure 26*, so that V_{IN2} supports the load only if V_{IN1} falls below falling input undervoltage threshold (V_{IN1_UVF}) even if $V_{IN2} > V_{IN1}$. For example, when priority power source V_{IN1} (10V-30V) is above its rising input undervoltage threshold (V_{IN1_UVR}), only V_{IN1} supports the load irrespective of whether backup power source V_{IN2} (10.8V-13.2V) is greater than or less than V_{IN1}. Once V_{IN1} falls below 8.9V (V_{IN1_UVF}), V_{IN2} supports the load.

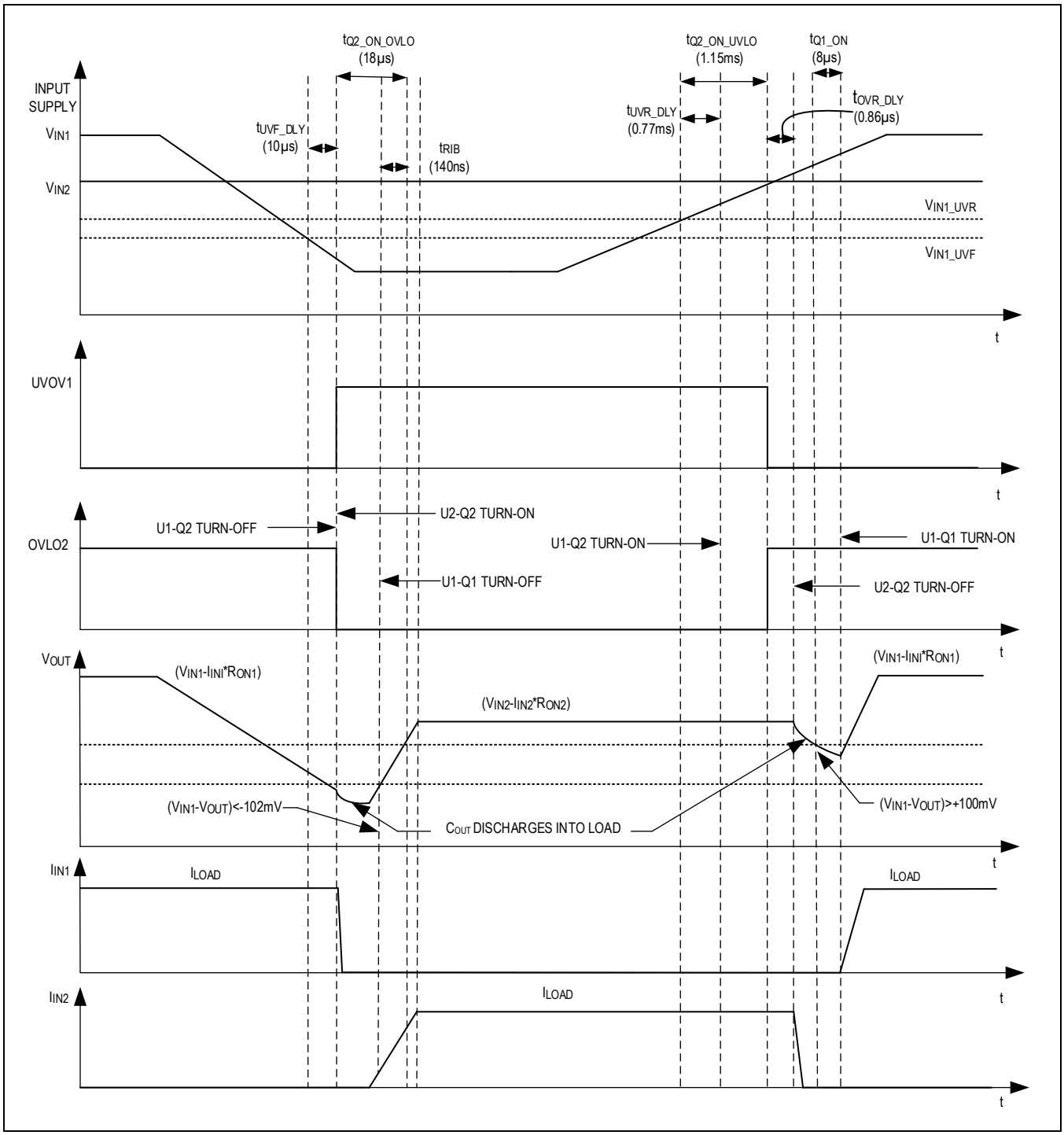


Figure 22. MAX17614 Priority Source Selector Timing Diagram

Figure 22 depicts the timing diagram for Priority Power Source Selector implementation using the MAX17614. The output load is initially supported by V_{IN1} in steady state since $V_{IN1} > V_{IN1\_UVR}$. The U1 is in forward conduction state (both Q1, Q2 are ON). The U2 is in OFF state (Q1 is ON, Q2 is OFF) since its OVLO pin is greater than rising input OVLO threshold.

In this state, if V_{IN1} were to ramp down due to failure of power, V_{OUT} follows V_{IN1} by a voltage drop that is equal to the product of U1 internal ON-resistance and load current. When V_{IN1} falls below V_{IN1_UVF} threshold, only the output nFET Q2 of U1 is turned OFF after 10µs (t_{UVF_DLY}) and UVOV1 is asserted. When UVOV1 is asserted, V_{OVLO2} is pulled

below the V_{OVF} threshold and U2 starts to turn ON Q2. The internal nFET Q2 fully turns on within 18µs ($t_{Q2\_ON\_OVLO}$). The V_{IN2} starts supporting the load current and the output voltage starts ramping up until the steady state output is reached, i.e., the output voltage is a function of V_{IN2}, U2 internal ON-resistance, and load current. During output voltage ramp-up, U1 turns off its internal nFET Q1 within 140ns (t_{RIB}) once (V_{IN1} - V_{OUT}) falls below -102mV.

When V_{IN1} recovers and V_{IN1} rises above V_{IN1_UVR} threshold, U1 starts to turn ON Q2 after 0.77ms (t_{UVR_DLY}). The internal nFET Q2 fully turns back on within 1.15ms ($t_{Q2\_ON\_UVLO}$) and UVOV1 is deasserted. When UVOV1 is deasserted, V_{OVLO2} rises above V_{OVR} threshold and U2 turns OFF its output nFET Q2 after 0.86µs (t_{OVR_DLY}) while its input nFET Q1 is kept ON. The output capacitor starts discharging to support the load. During output capacitor discharge, U1 turns ON its internal nFET Q1 after 8µs (t_{Q1_ON}) once the reverse condition has been removed, i.e., (V_{IN1} - V_{OUT}) exceeds +100mV. The output voltage starts ramping up until the steady state output is reached i.e., the output voltage is a function of V_{IN1}, U1 internal ON-resistance, and load current.

Input Capacitor

A ceramic (0.47µF–1µF) capacitor from the IN pin to GND is recommended.

Hot Plug-In

In many system-powering applications, an input-filtering capacitor is required to lower radiated emission and enhance ESD capability. In hot plug-in applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that is capable of limiting surge voltage to 60V (max) should be placed close to the input terminal for enhanced protection. The maximum allowable slew rate at the IN pins is 100V/µs (max).

Hot Plug-In at OUT Terminal

In some applications, there can be a possibility of applying an external voltage at the OUT terminal of the devices with or without presence of input voltage. During these conditions, the MAX17614 detects any reverse current entering at the OUT pin and flowing out of the IN pin and turns off the internal FETs. Parasitic cable inductance along with input and output capacitors cause overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection devices to see up to twice the applied voltage, which can damage the devices. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the absolute maximum ratings. The maximum allowable slew rate at the OUT pins is 100V/µs (max).

Output Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, a Schottky diode between the OUT terminal and ground is recommended to prevent negative voltage swing on OUT due to inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

Place input and output capacitors as close as possible to the device. The IN and OUT pins must be connected with wide short traces to the power bus. During normal operation, the power dissipation is small and the package temperature change is minimal.

Power dissipation under steady-state normal operation can be calculated as follows:

$$P_{SS} = (I_{OUT}^2) * R_{ON}$$

See the *Electrical Characteristics* and *Typical Operating Characteristics* for R_{ON} values at various operating temperatures. Thermal vias from the exposed pad to the ground plane should be used to provide adequate heatsinking to internal ground planes.

ESD Protection

The devices are specified for ±15kV (HBM) typical ESD resistance on IN when IN is bypassed to ground with a 0.47µF low-ESR ceramic capacitor. No capacitor is required for ±2kV (HBM) typical ESD on IN. All the pins have a ±2kV (HBM) typical ESD protection.

Figure 23 shows the Human Body Model and *Figure 24* shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

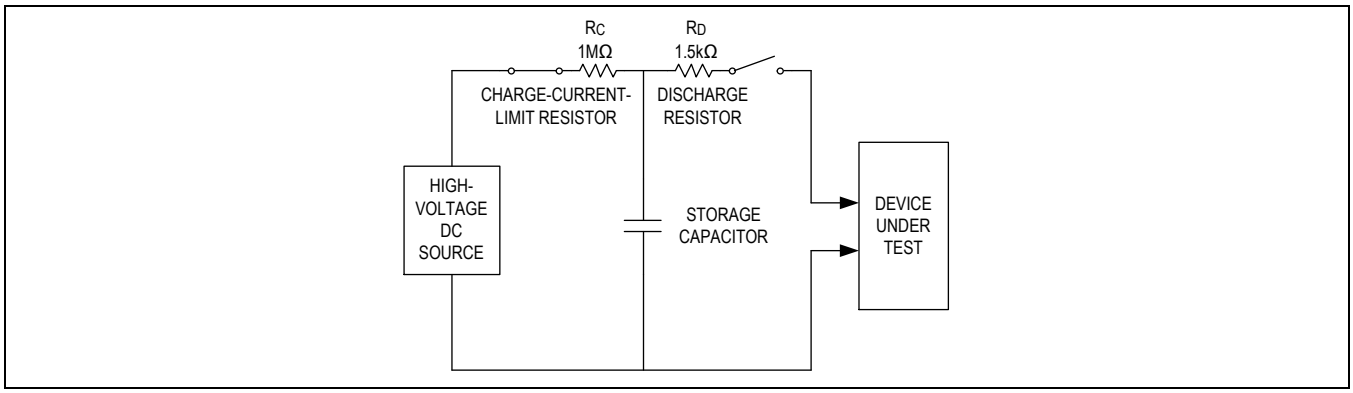


Figure 23. Human Body ESD Test Model

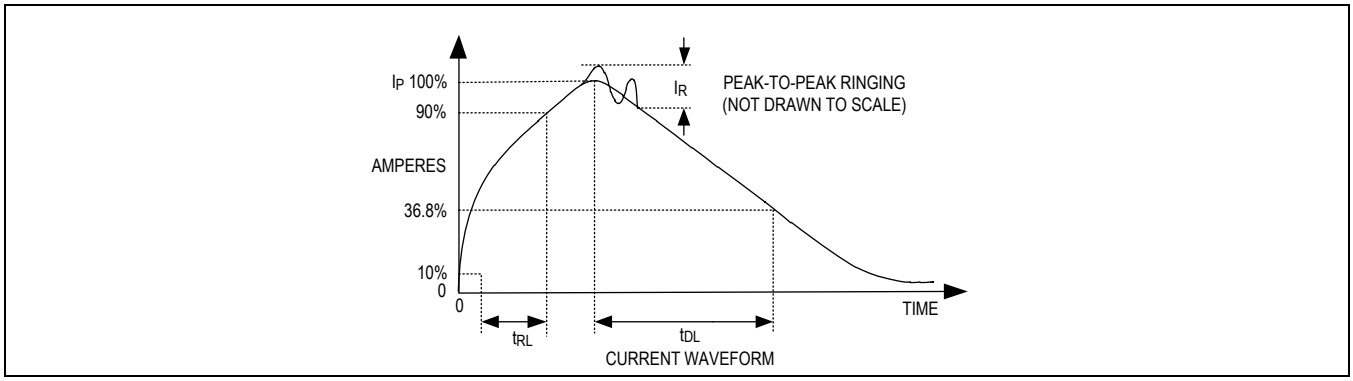


Figure 24. Human Body Current Waveform

Typical Application Circuits

Ideal Diode/Power MUX Application

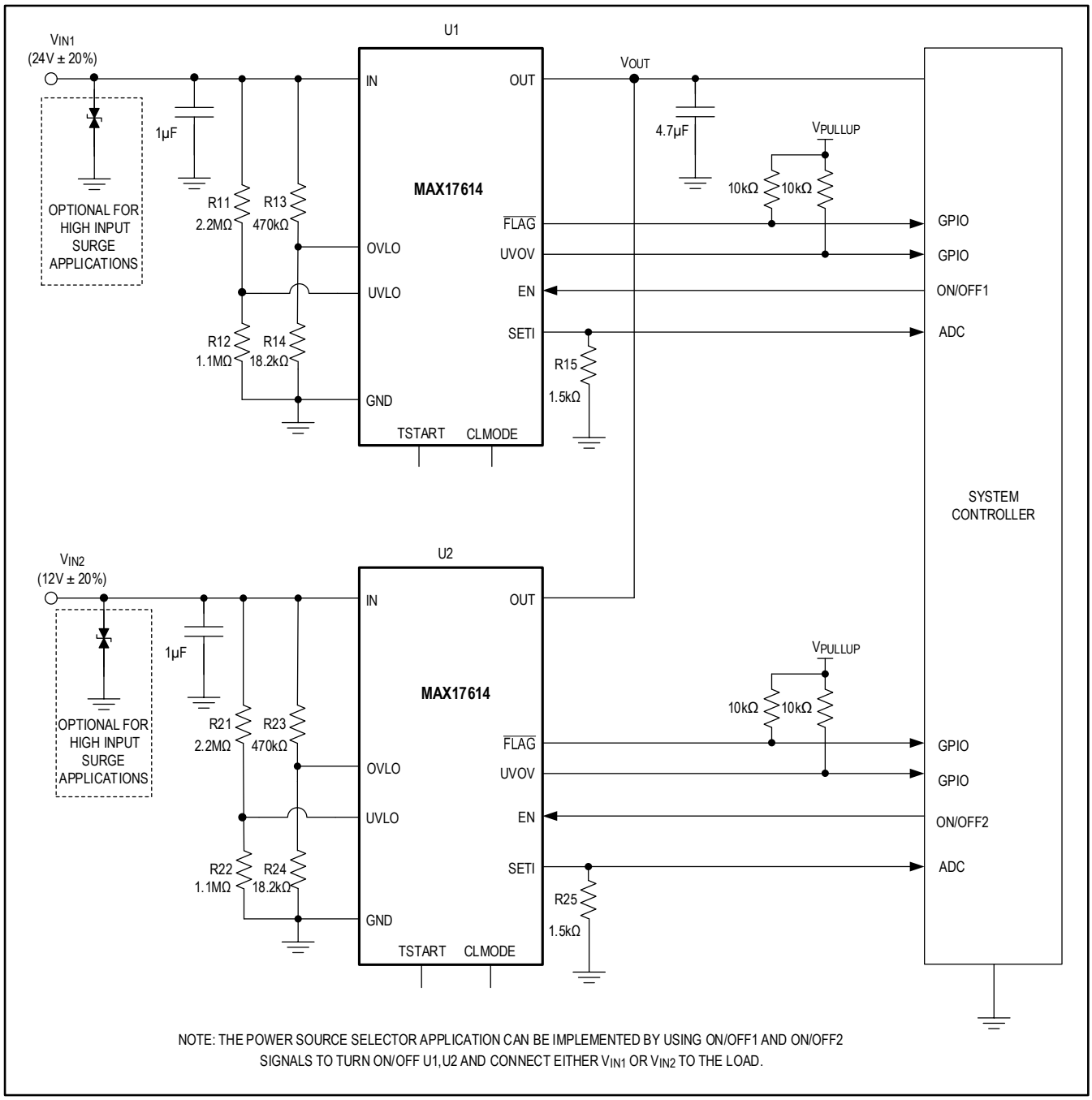


Figure 25. Ideal Diode Application Circuit Using Two MAX17614 ICs

Priority Power Source Selector

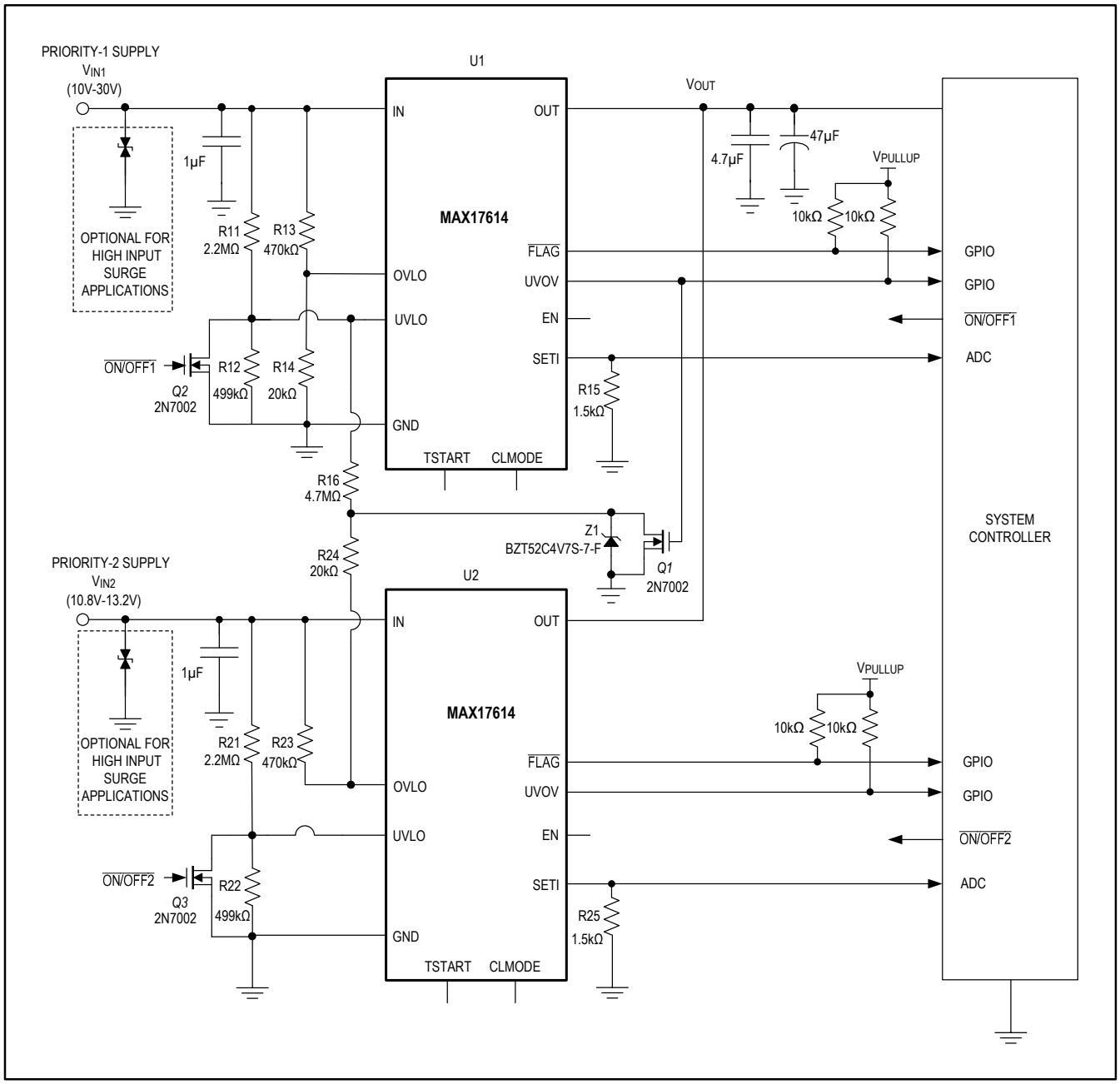


Figure 26. Priority Power Source Selector Application Circuit Using Two MAX17614 ICs

Current Limiter with Reverse Current Blocking

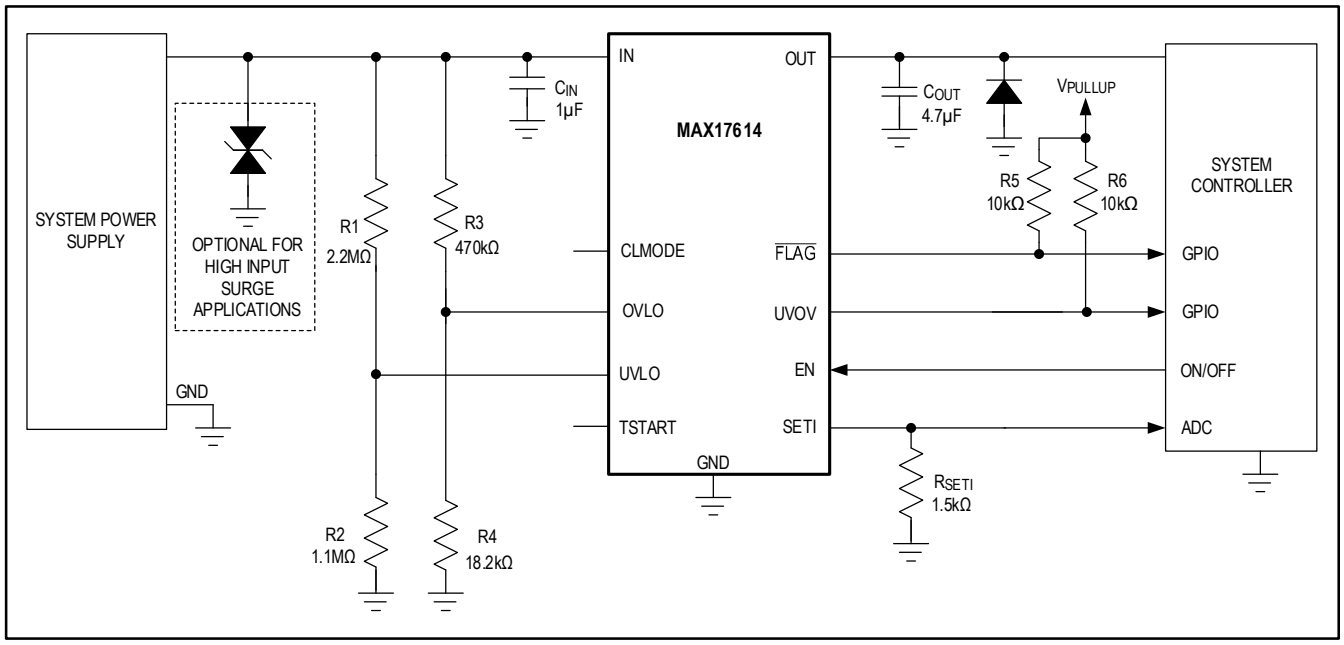


Figure 27. Current Limiter with Reverse Current Blocking Application Circuit Using MAX17614 IC

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX17614ATP+	-40°C to +125°C	20 TQFN-EP*
MAX17614ATP+T	-40°C to +125°C	20 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

*EP = Exposed pad.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/23	Release for Market Intro	—

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX17614ATP+ MAX17614ATP+T