Click here to ask an associate for production status of specific part numbers.

4V to 60V, 1.5A, High-Efficiency, Synchronous Step-Down DC-DC Converter

MAX17571

Product Highlights

- Reduces External Components and Total Cost
  - No Schottky—Synchronous Operation
  - Internal Compensation
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4V to 60V Input-Voltage Range
  - Adjustable Output Voltage Range from 0.9V up to 90% of V_{IN}
  - 400kHz to 2.2MHz Adjustable Switching Frequency with External Clock Synchronization
- Reduces Power Dissipation
  - 94% Peak Efficiency
  - External Bias Input for Improved Efficiency
  - 4.65µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Built-in Hiccup Mode Overload Protection
  - Built-in Output-Voltage Monitoring with $\overline{RESET}$
  - Adjustable Soft-Start
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Output Voltage
  - Overtemperature Protection
  - CISPR 32 Class B Compliant

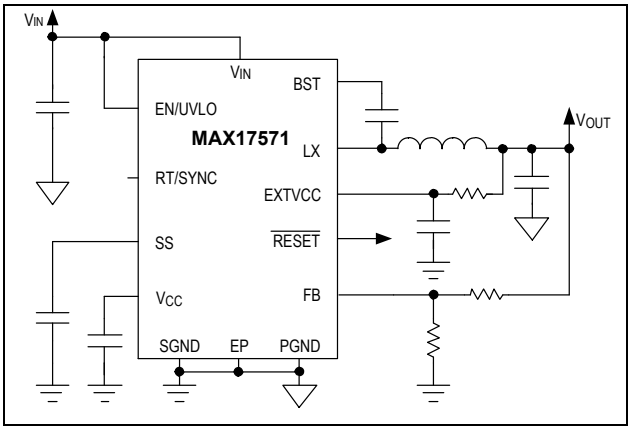
General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17571, a high-efficiency, high-voltage, Himalaya synchronous step-down DC-DC converter with integrated MOSFETs operates over an input voltage range of 4V to 60V. The converter can deliver up to 1.5A current. Output voltage is programmable from 0.9V up to 90% of V_{IN}. The feedback voltage regulation accuracy over -40°C to +125°C is ±1.2%. Built-in compensation across the output voltage range eliminates the need for external compensation components.

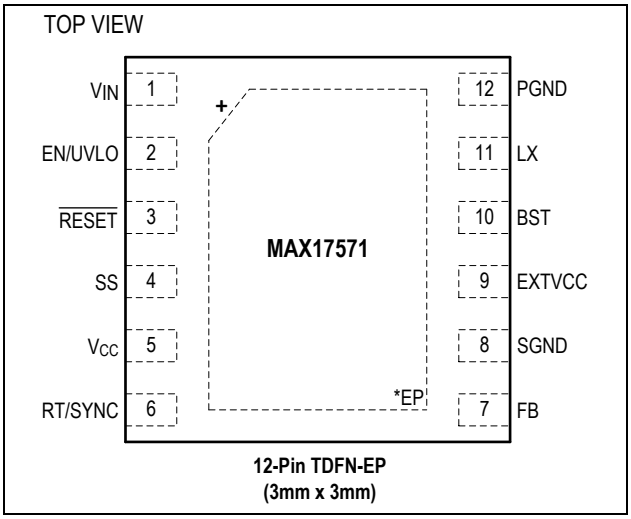
The MAX17571 features peak-current-mode control architecture and operates in fixed frequency forced pulse-width modulation (PWM) mode. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an enable/input undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. The MAX17571 offers a low minimum on time that allows high switching frequencies and a smaller solution size.

The MAX17571 is available in a 12-pin (3mm x 3mm) TDFN-EP package. Simulation models are available.

Simplified Application Diagram



Pin Description



***Ordering Information* appears at end of data sheet.**

19-101589; Rev 0; 7/22

Absolute Maximum Ratings

V_{IN} to PGND ..... -0.3V to +65V

EN/UVLO to SGND ..... -0.3V to (V_{IN} + 0.3V)

EXTVCC to SGND..... -0.3V to +26V

BST to PGND ..... -0.3V to +70V

LX to PGND..... -0.3V to (V_{IN} + 0.3V)

BST to LX..... -0.3V to +6.5V

BST to V_{CC} ..... -0.3V to +65V

$\overline{RESET}$, SS, RT/SYNC to SGND..... -0.3V to +6.5V

PGND to SGND..... -0.3V to +0.3V

FB to SGND ..... -0.3V to +1.5V

V_{CC} to SGND..... -0.3V to +6.5V

LX Total RMS Current..... ±1.6A

Continuous Power Dissipation (T_A = +70°C, derate 24.4mW/°C above +70°C) (Multilayer Board)..... 1951mW

Output Short-Circuit Duration..... Continuous

Operating Temperature Range () ..... -40°C to +125°C

Junction Temperature ..... 150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s)..... 300°C

Soldering Temperature (reflow)..... 260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Type: 12 TDFN	
Package Code	TD1233+1C
Outline Number	*21-0664*
Land Pattern Number	*90-0397*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2kΩ, C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{EXTVCC} = 0V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (Shutdown mode)		4.65	7.25	µA
Input Quiescent Current	I_{Q_PWM}	Normal Switching, V_{FB} = 0.8V		5.2		mA
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.26	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.131	
EN/UVLO Input Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 1.25V, T_A = +25°C	-50	0	+50	nA
LINEAR REGULATORS (IN-LDO, EXT-LDO)						
V_{CC} Output Voltage	V_{CC}	1mA ≤ I_{VCC} ≤ 15mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 60V; I_{VCC} = 1mA	4.75	5	5.25	
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 6.5V	25	54	100	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 15mA			0.35	V
V_{CC} Undervoltage Threshold	V_{CC-UVR}	Rising	3.65	3.8	3.9	V
	V_{CC-UVF}	Falling	3.43	3.58	3.68	
EXTVCC Switchover Threshold	$V_{EXTVCC-UVR}$	EXTVCC rising	4.56	4.7	4.84	V
	$V_{EXTVCC-UVF}$	EXTVCC falling	4.3	4.45	4.6	
EXTVCC Dropout	$EXTVCC_{DO}$	V_{EXTVCC} = 4.75V, I_{VCC} = 15mA			0.3	V
EXTVCC Current Limit	$EXTVCC_{ILIM}$	V_{CC} = 4.5V, EXTVCC = 7V	26.5	60	100	mA
HIGH-SIDE AND LOW-SIDE MOSFETS						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, sourcing		330	620	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A, sinking		170	320	mΩ
LX Leakage Current	I_{LX_LKG}	T_A = 25°C, V_{LX} = (V_{PGND} + 1V) to (V_{IN} - 1V)	-2		+2	µA
SOFT-START (SS)						
Soft-Start Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}		0.889	0.9	0.911	V
FB Input-Bias Current	I_{FB}	0 ≤ V_{FB} ≤ 1V, T_A = +25°C	-50		+50	nA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		2.39	2.79	3.18	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		2.58	3.09	3.48	A
Negative Current-Limit Threshold				1		A
RT/SYNC AND TIMINGS						
Switching Frequency	f_{SW}	$R_{RT/SYNC}$ = 51.1kΩ	370	400	430	kHz
		$R_{RT/SYNC}$ = 40.2kΩ	475	500	525	

(V_{IN} = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2kΩ, C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{EXTVCC} = 0V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

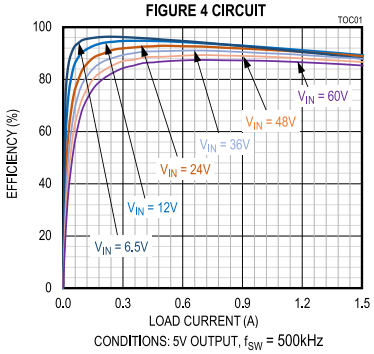
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		$R_{RT/SYNC}$ = 8.06kΩ	1950	2200	2450	
		$R_{RT/SYNC}$ = Open	430	490	550	
V_{FB} Undervoltage Trip Level to Cause HICCUP	$V_{FB-HICF}$		0.56	0.58	0.65	V
HICCUP Timeout				32768		Cycles
Minimum On-Time	t_{ON_MIN}			60	80	ns
Minimum Off-Time	t_{OFF_MIN}			105	125	ns
LX Dead Time				5		ns
SYNC Frequency Capture Range		f_{SW} set by $R_{RT/SYNC}$	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
OUTPUT VOLTAGE STATUS ($\overline{RESET}$)						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output Leakage Current		T_A = T_J = 25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.8	95	97.8	%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.5	92	94.6	%
$\overline{RESET}$ Delay after FB Reaches V_{FB-OKR}				1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		165		°C
Thermal Shutdown Hysteresis				10		°C

Note 2: Electrical specifications are production tested are at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Typical Operating Characteristics

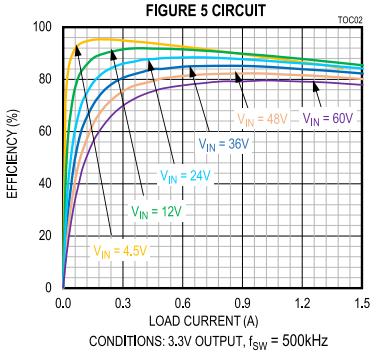
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND.)

EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



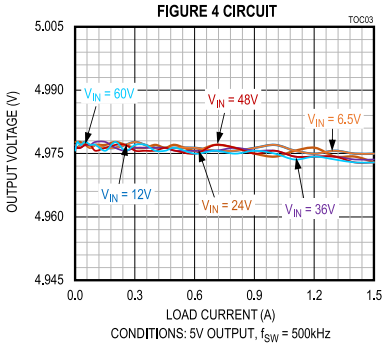
CONDITIONS: 5V OUTPUT, f_{SW} = 500kHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



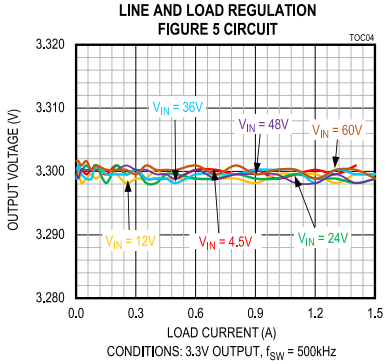
CONDITIONS: 3.3V OUTPUT, f_{SW} = 500kHz

LINE AND LOAD REGULATION
FIGURE 4 CIRCUIT



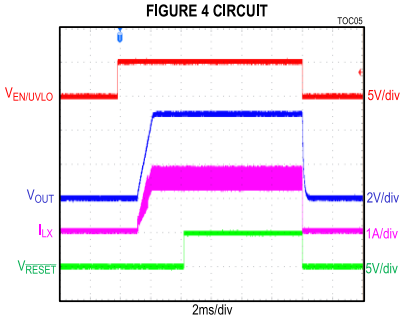
CONDITIONS: 5V OUTPUT, f_{SW} = 500kHz

LINE AND LOAD REGULATION
FIGURE 5 CIRCUIT



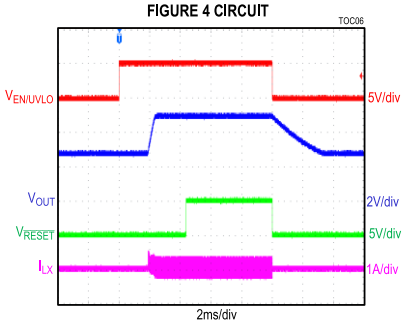
CONDITIONS: 3.3V OUTPUT, f_{SW} = 500kHz

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 4 CIRCUIT



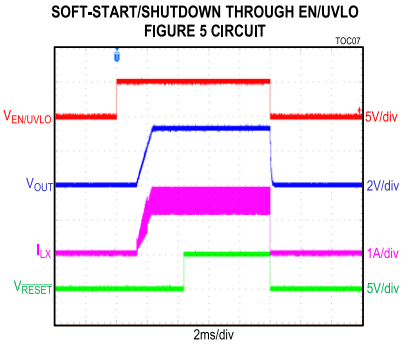
CONDITIONS: 5V OUTPUT, 3.33Ω RESISTIVE LOAD
$\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START WITH PREBIAS VOLTAGE OF 2.5V
FIGURE 4 CIRCUIT



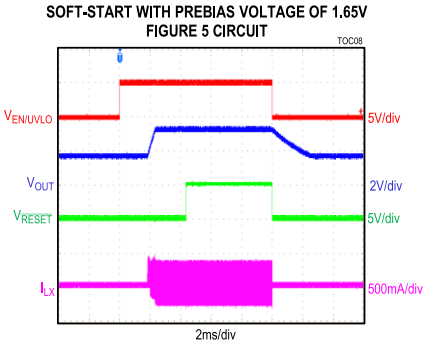
CONDITIONS: 5V OUTPUT, 250Ω RESISTIVE LOAD
$\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 5 CIRCUIT



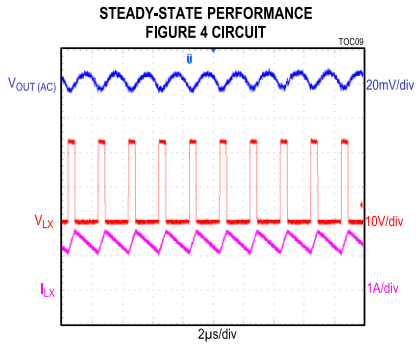
CONDITIONS: 3.3V OUTPUT, 2.2Ω RESISTIVE LOAD
$\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

SOFT-START WITH PREBIAS VOLTAGE OF 1.65V
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 165Ω RESISTIVE LOAD
$\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

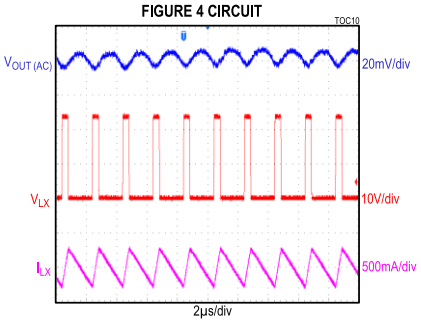
STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, 3.33Ω RESISTIVE LOAD

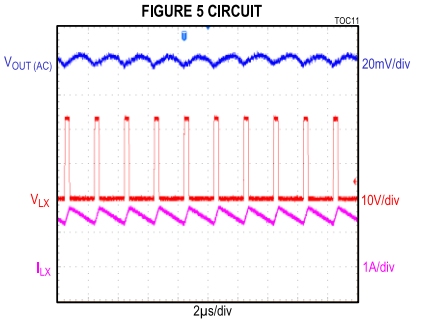
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND.)

STEADY-STATE PERFORMANCE
FIGURE 4 CIRCUIT



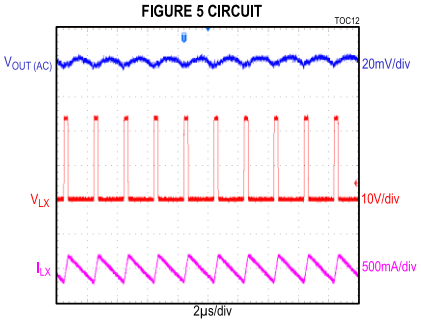
CONDITIONS: 5V OUTPUT, NO LOAD

STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



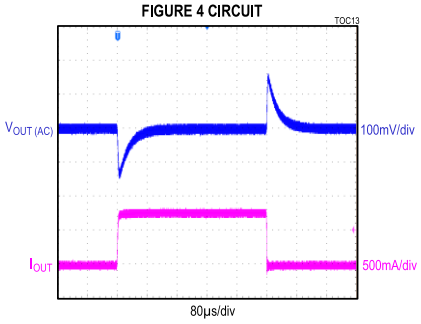
CONDITIONS: 3.3V OUTPUT, 2.2Ω RESISTIVE LOAD

STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



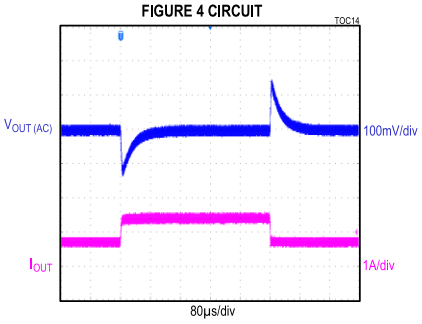
CONDITIONS: 3.3V OUTPUT, NO LOAD

LOAD TRANSIENT BETWEEN 0A AND 0.75A
FIGURE 4 CIRCUIT



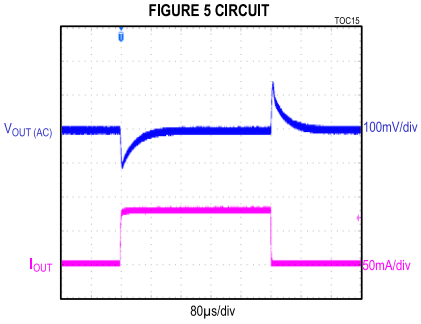
CONDITIONS: 5V OUTPUT

LOAD TRANSIENT BETWEEN 0.75A AND 1.5A
FIGURE 4 CIRCUIT



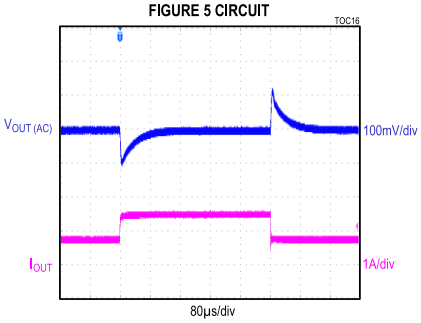
CONDITIONS: 5V OUTPUT

LOAD TRANSIENT BETWEEN 0A AND 0.75A
FIGURE 5 CIRCUIT



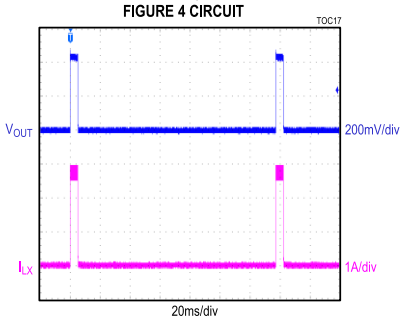
CONDITIONS: 3.3V OUTPUT

LOAD TRANSIENT BETWEEN 0.75A AND 1.5A
FIGURE 5 CIRCUIT



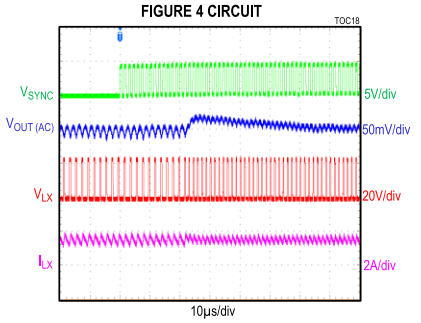
CONDITIONS: 3.3V OUTPUT

OVERLOAD PROTECTION, HICCUP OPERATION
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, 0.15Ω LOAD

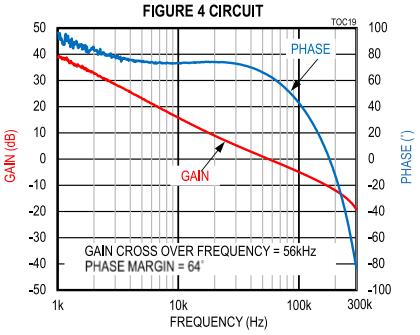
EXTERNAL CLOCK SYNCHRONIZATION
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, 3.33Ω RESISTIVE LOAD, f_{SW} = 500kHz, EXTERNAL CLOCK FREQUENCY = 700kHz

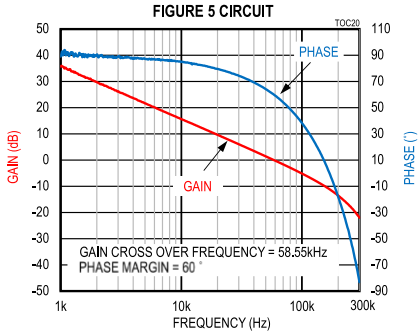
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND.)

BODE PLOT
FIGURE 4 CIRCUIT



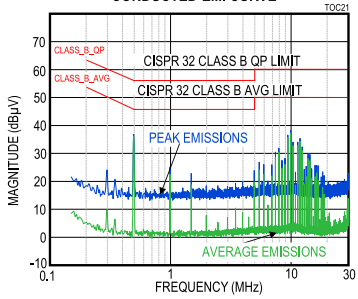
CONDITIONS: 5V OUTPUT, 3.33Ω RESISTIVE LOAD

BODE PLOT
FIGURE 5 CIRCUIT



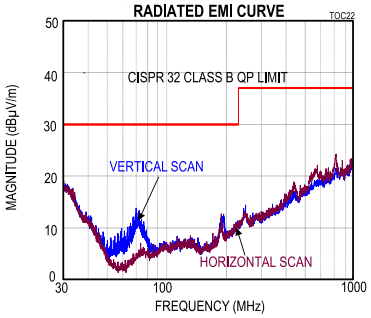
CONDITIONS: 3.3V OUTPUT, 2.2Ω RESISTIVE LOAD

MAX17571, 5V OUTPUT, 1.5A LOAD CURRENT
CONDUCTED EMI CURVE



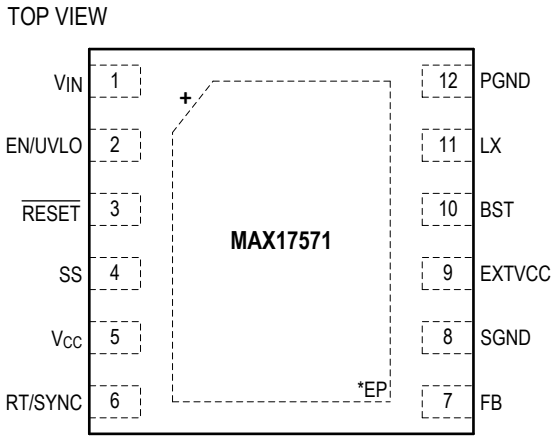
CONDITIONS: MEASURED ON THE MAX17571EVKITB# WITH L201 = 15µH, C201 = 4.7µF/100V/X7R/1206

MAX17571, 5V OUTPUT, 1.5A LOAD CURRENT
RADIATED EMI CURVE



CONDITIONS: MEASURED ON THE MAX17571EVKITB#

Pin Configurations

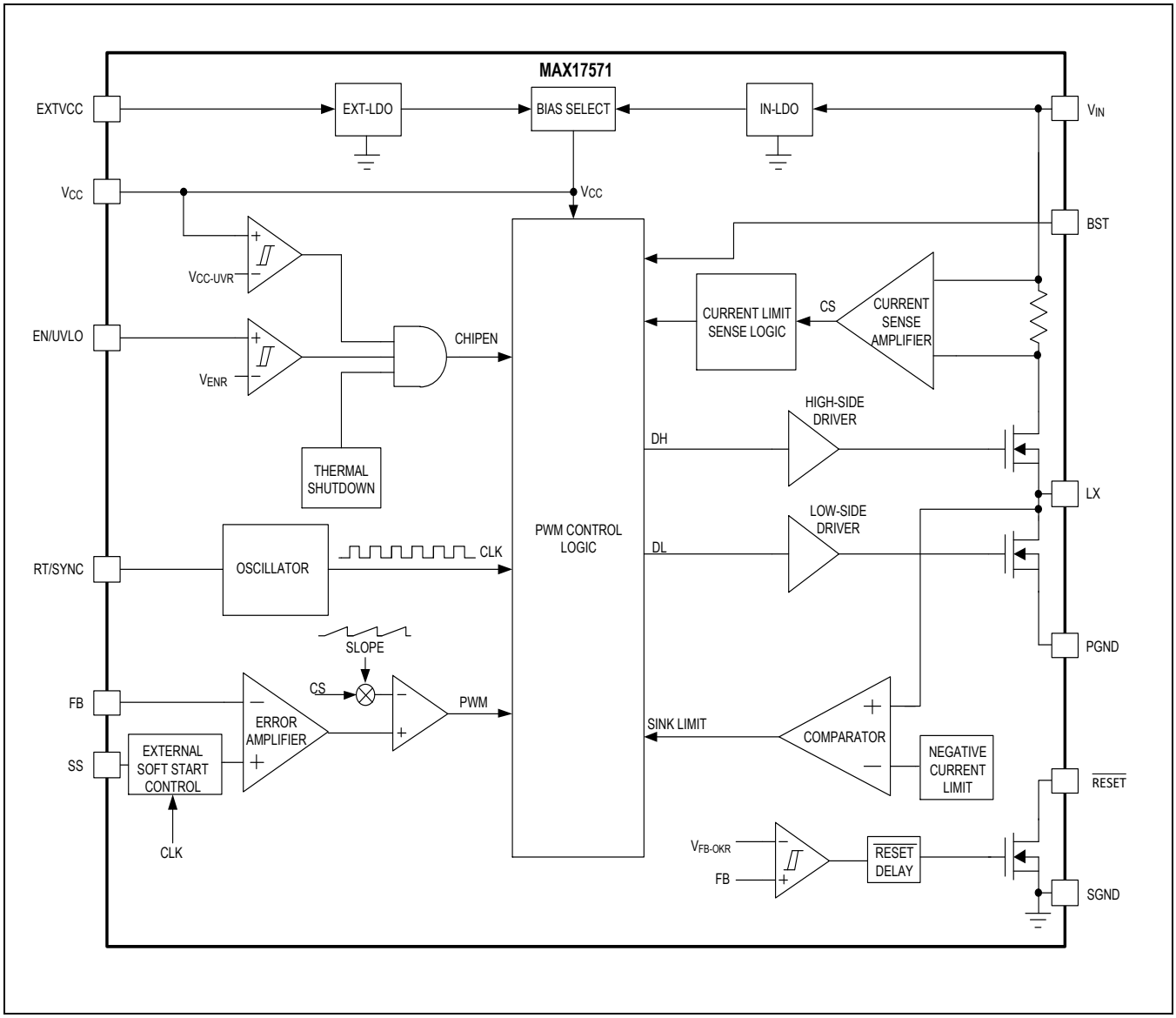


12-Pin TDFN-EP
(3mm x 3mm)

Pin Descriptions

PIN	NAME	FUNCTION
1	V_{IN}	Power Supply Input. The input supply range is from 4V to 60V.
2	EN/UVLO	Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the center node of the resistive divider between V_{IN} and SGND to set the input voltage (undervoltage threshold) at which the device turns on. Pull up to V_{IN} for always-on operation.
3	$\overline{RESET}$	Open-Drain Status Output. Output voltage status can be monitored by connecting the $\overline{RESET}$ pin to V_{CC} through a pullup resistor. The $\overline{RESET}$ output is driven low if FB drops below 92% of its set value. $\overline{RESET}$ goes high 1024 clock cycles after FB rises above 95% of its set value. $\overline{RESET}$ is valid when the device is enabled and V_{IN} is above 4V.
4	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
5	V_{CC}	5V LDO Output. Connect a minimum of 2.2µF/0603, low-ESR ceramic capacitor between V_{CC} to SGND.
6	RT/SYNC	Switching Frequency Programming and External Clock Synchronization Input. Connect a resistor from RT/SYNC to SGND to program the switching frequency from 400kHz to 2.2MHz. The device can be synchronized to an external clock using this pin. See the *Switching Frequency Selection and External Frequency Synchronization* section for details.
7	FB	Feedback Input. Connect FB to the center node of the resistive divider between output voltage and SGND.
8	SGND	Signal Ground.
9	EXTVCC	External Power-Supply Input for the Internal LDO. Applying a voltage between 5V and 24V at the EXTVCC pin bypasses the internal LDO and improve efficiency.
10	BST	Bootstrap Capacitor Pin. Connect a 0.1µF ceramic capacitor between BST and LX.
11	LX	Switching Node Pin. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.
12	PGND	Power Ground. Connect PGND externally to the power ground plane. Connect SGND and PGND pins together on the ground return path of the V_{CC} bypass capacitor.
-	EP	Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large ground plane with several thermal vias for best thermal performance. Refer to the MAX17571 EV kit data sheet for an example of the correct method for EP connection and thermal vias.

Functional Diagram


MAX17571
EXTVCC
EXT-LDO
BIAS SELECT
IN-LDO
VIN
VCC
VCC
BST
VCC-UVR
EN/UVLO
CHIPEN
CURRENT LIMIT SENSE LOGIC
CS
CURRENT SENSE AMPLIFIER
VENR
HIGH-SIDE DRIVER
DH
THERMAL SHUTDOWN
LX
LOW-SIDE DRIVER
PWM CONTROL LOGIC
RT/SYNC
OSCILLATOR
CLK
DL
SLOPE
PGND
FB
CS
PWM
ERROR AMPLIFIER
SINK LIMIT
COMPARATOR
SS
EXTERNAL SOFT START CONTROL
NEGATIVE CURRENT LIMIT
RESET
CLK
VFB-OKR
FB
RESET DELAY
SGND

Detailed Description

The MAX17571 is a high-efficiency, high-voltage, Himalaya synchronous step-down DC-DC converter with integrated MOSFETs that operates over a wide 4V to 60V input-voltage range. The device can deliver up to 1.5A and generates output voltages ranging from 0.9V to 90% of V_{IN}. Built-in compensation across the output-voltage range and switching frequency range eliminates the need for external compensation components. The feedback-voltage regulation accuracy is ±1.2% over the -40°C to +125°C temperature range.

The device features a peak-current-mode control architecture and operates in fixed-frequency forced PWM mode. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up and stores energy in the inductor and provides current to the output. During the rest of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a RT/SYNC pin to program the switching frequency and to synchronize to an external clock. The device also features adjustable-input undervoltage-lockout (EN/UVLO), adjustable soft-start (SS), open-drain $\overline{RESET}$, and external bias input (EXTVCC).

Linear Regulator (V_{CC})

The MAX17571 has two internal low-dropout regulators, IN-LDO and EXT-LDO, that power V_{CC}. IN-LDO is powered from V_{IN} pin and EXT-LDO is powered from the EXTVCC pin. IN-LDO is enabled during V_{IN} and EN/UVLO power up. Only one of these two linear regulators operates depending on the voltage at EXTVCC pin. During power up, the switchover from IN-LDO to EXT-LDO occurs at the end of the programmed soft-start time if EXTVCC pin voltage is greater than 4.7V ($V_{EXTVCC-UVR}$). Powering V_{CC} from EXT-LDO reduces on-chip dissipation and increases efficiency at higher input voltages. Connect the EXTVCC pin to the converter output voltage node for output voltages ranging from 5V to 24V for improved efficiency. The typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks as well as the low-side MOSFET driver, and recharges the external bootstrap capacitor.

The MAX17571 starts switching only when voltage at V_{CC} is greater than 3.8V (V_{CC-UVR}). The device employs an undervoltage lockout circuit that forces the converter off when V_{CC} falls below 3.58V (V_{CC-UVF}). The 220mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck converter output is connected to the EXTVCC pin, if the output is shorted to ground, the transfer from EXT-LDO to IN-LDO happens seamlessly without any impact on the normal functionality. Bypass EXTVCC with a low ESR 0.1µF ceramic capacitor SGND. Also, add a 4.7Ω resistor from the buck converter output node to the EXTVCC pin to limit V_{CC} bypass capacitor discharge current and to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during inductive output short-circuit condition. Connect EXTVCC pin to SGND when not in use.

Switching Frequency Selection and External Frequency Synchronization

The switching frequency of the MAX17571 can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT/SYNC pin to SGND. When a resistor is not used, the frequency is programmed to 490kHz. The switching frequency (f_{SW}) is related to the resistor connected at the RT/SYNC pin ($R_{RT/SYNC}$) by the following equation:

$$R_{RT/SYNC} = \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where $R_{RT/SYNC}$ is in kΩ and f_{SW} is in kHz. See *Table 1* for RT/SYNC resistor values for a few common switching frequencies.

The RT/SYNC pin can be used to synchronize the device internal oscillator to an external system clock. A resistor must be connected from the RT/SYNC pin to SGND to be able to synchronize the MAX17571 to an external clock. The external clock should be coupled to the RT/SYNC pin through a network, as shown in *Figure 1*. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on RT/SYNC setting) after detecting 16 external clock rising edges. The external clock logic-high level should be higher than 2.1V, a logic-low level lower than 0.8V, and the pulse-width of the external clock should be more than 50ns. The RT/SYNC resistor should be selected to set the switching frequency at 10% lower than the external clock frequency.

Table 1. Switching Frequency vs. RT/SYNC Resistor

SWITCHING FREQUENCY (kHz)	RT/SYNC RESISTOR
400	51.1
490	OPEN
1000	19.1
2200	8.06

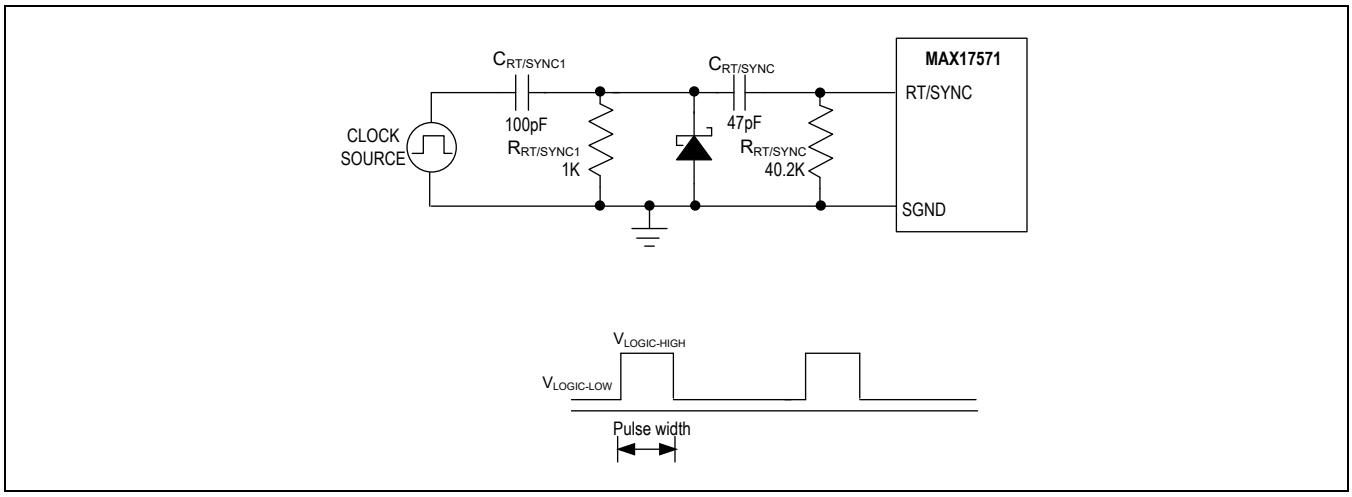


Figure 1. External Clock Synchronization

Operating Input-Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\_ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF\_MIN(MAX)}\right)} + I_{OUT(MAX)} \times \left(R_{DS\_ONH(MAX)} - R_{DS\_ONL(MAX)}\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times 10^3 \times t_{ON\_MIN(MAX)}}$$

where:

$V_{IN(MIN)}$ = Worst-case minimum input voltage

$V_{IN(MAX)}$ = Worst-case maximum input voltage

V_{OUT} = Set nominal output voltage

$I_{OUT(MAX)}$ = Maximum load current

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency in kHz

$t_{OFF\_MIN(MAX)}$ = Worst-case minimum switch off-time (125ns)

$t_{ON\_MIN(MAX)}$ = Worst-case minimum switch on-time (80ns)

$R_{DS\_ONL(MAX)}$ and $R_{DS\_ONH(MAX)}$ = Worst-case on-state resistances of low-side and high-side internal MOSFETs, respectively.

$V_{IN(MIN)}$ is minimum input voltage, above which the output is regulated at V_{OUT} for load currents up to $I_{OUT(MAX)}$. For load currents lower than $I_{OUT(MAX)}$, the required minimum input voltage is lowered correspondingly. When an input voltage lower than $V_{IN(MIN)}$ is applied with $I_{OUT(MAX)}$ load, the output voltage might not be regulated.

$V_{IN(MAX)}$ is maximum input voltage, below which the converter switching frequency is maintained at the programmed value. When an input voltage higher than $V_{IN(MAX)}$ is applied, the switching pulses can skip and reduce the effective switching frequency to regulate the output at V_{OUT}.

Overcurrent Protection

The MAX17571 provides a robust overcurrent protection (OCP) scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET and the low-side MOSFET turns on whenever the high-side switch current exceeds an internal limit of 2.79A ($I_{PEAK-LIMIT}$). A runaway current limit on the high-side switch current at 3.09A ($I_{RUNAWAY-LIMIT}$) protects the device under high input voltage and output short-circuit conditions when there is insufficient output voltage available to restore the inductor current built up during the on period of the step-down converter. One occurrence of runaway current limit triggers a hiccup mode. In addition, if the feedback voltage drops below 0.58V ($V_{FB-HICF}$) any time after soft-start is completed due to any fault, then hiccup mode is activated.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload conditions, if feedback voltage does not exceed $V_{FB-HICF}$, the device continues to switch at half of the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The MAX17571 includes a $\overline{\text{RESET}}$ comparator to monitor the status of the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the feedback voltage (V_{FB}) increases above 95% (V_{FB-OKR}). $\overline{\text{RESET}}$ is pulled low when V_{FB} drops below 92% (V_{FB-OKF}). $\overline{\text{RESET}}$ is also pulled low during thermal shutdown or when EN/UVLO pin goes below V_{ENF}.

Prebiased Output

When the device starts into a prebiased output, both the high-side and low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

The MAX17571 offers internal thermal-shutdown protection to limit the total average power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns on with soft-start after the junction temperature cools down by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection during normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ is the maximum load current.

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times 10^3 \times \Delta V_{IN}}$$

where:

D = V_{OUT}/V_{IN} and is the duty ratio of the converter

f_{SW} = Switching frequency in kHz

ΔV_{IN} = Allowable input voltage ripple

η = Efficiency

Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the input capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

In applications where the source is far from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}) are three key inductor parameters that must be specified for operation with the device. The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{1.6 \times V_{OUT}}{f_{SW} \times 10^3}$$

Where V_{OUT} and f_{SW} are nominal values and f_{SW} is in kHz. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to about 3% of the output voltage. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.33}{f_C}$$

where:

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT}= Allowable output-voltage deviation

f_C = Target closed-loop crossover frequency in Hz

f_{SW} = Switching frequency

Select f_C to be 1/9th of f_{SW}, if the switching frequency is less or equal to 500kHz. If the switching frequency is higher than 500kHz, select f_C to be 55kHz. Actual derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start Capacitor Selection

The MAX17571 implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{OUT_SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} = 56 \times 10^{-6} \times C_{OUT\_SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to SGND. Note that during start-up, the device operates at half the programmed switching frequency until the output voltage reaches 66.7% of the set output nominal voltage.

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see *Figure 2*). Connect the center node of the divider to the FB pin. Use the following procedure to calculate the resistive voltage-divider values:

Calculate resistor R_{FB_TOP} from the output to the FB pin as follows:

$$R_{FB\_TOP} = \frac{110}{f_C \times C_{OUT\_SEL}}$$

where:

R_{FB_TOP} is in kΩ

f_C = Crossover frequency in Hz

C_{OUT_SEL} = Actual capacitance of selected output capacitor at DC-bias voltage in F

Calculate resistor R_{FB_BOT} from the FB pin to SGND as follows:

$$R_{FB\_BOT} = \frac{R_{FB\_TOP} \times 0.9}{(V_{OUT} - 0.9)}$$

R_{FB_BOT} is in kΩ.

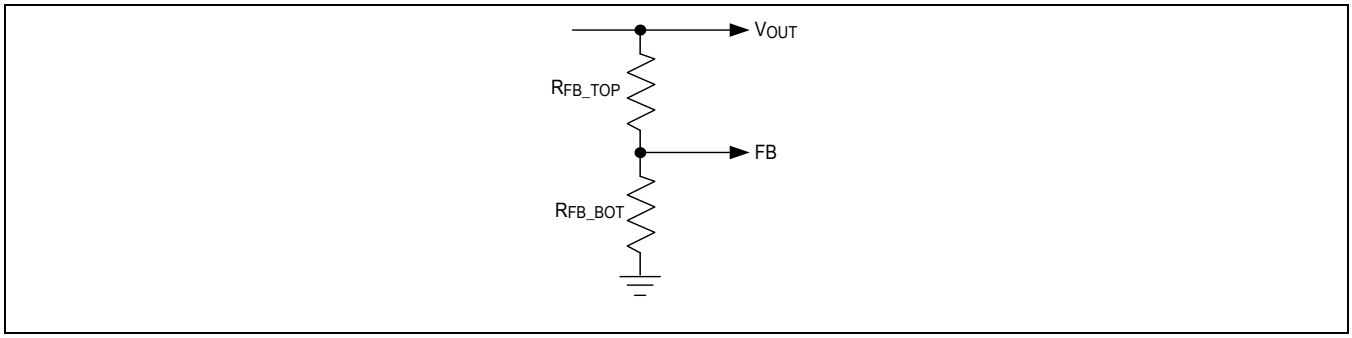


Figure 2. Adjusting Output Voltage

Setting the Undervoltage Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND (*Figure 3*). Connect the center node of the divider to EN/UVLO. Choose R_{UVL_TOP} to be 3.3MΩ and then calculate R_{UVL_BOT} as follows:

$$R_{UVL\_BOT} = \frac{R_{UVL\_TOP} \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccup during slow power-up (slower than soft-start) or power-down.

If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

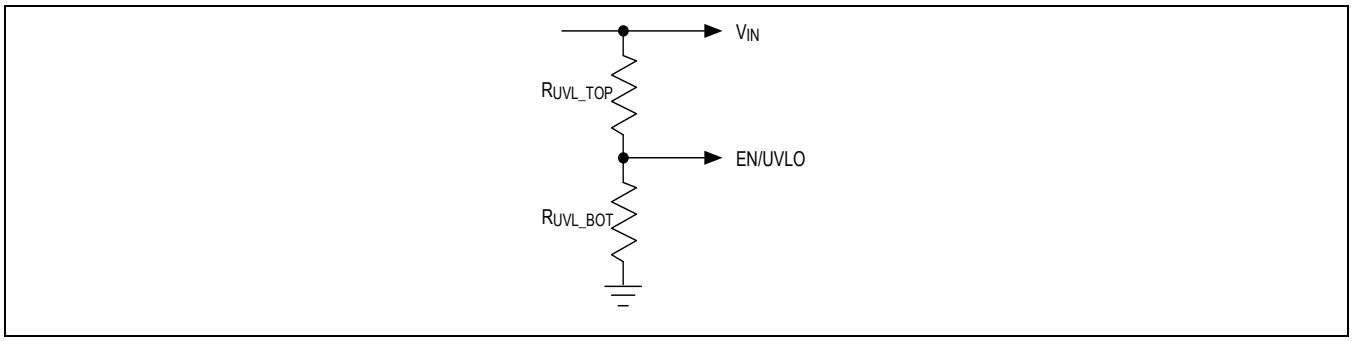


Figure 3. Setting the Input Undervoltage Lockout

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - {I_{OUT}}^2 \times R_{DCR}$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of the converter

R_{DCR} = DC resistance of the inductor

For a typical multilayer board, the thermal performance metrics for the package are given as follows:

$$\theta_{JA} = 41°C/W$$

$$\theta_{JC} = 8.5°C/W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J(MAX)} = T_{EP(MAX)} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these traces must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, inductance is reduced if the loop area is made very small. Additionally, small-current loop areas reduce radiated EMI. When routing the circuitry around the IC, the signal ground (SGND) and the power ground (PGND) for switching currents must be kept separate. PCB layout also affects the thermal performance of the design.

- Place the input capacitor as close as possible to the V_{IN} and PGND pins.
- Connect the V_{CC} capacitor close to the V_{CC} pin and connect the other terminal to the SGND plane.
- Place BST capacitor close to the BST and LX pins.
- Place the inductor as close as possible to the LX pin. Minimize the length and area of the trace connection from the LX pin to the inductor.
- Place the output capacitor as close as possible to non-switching side of the inductor.
- Place the PGND terminals of the input capacitor and output capacitor as close as possible to the PGND pins and connect them to the PGND plane.
- Place the RT/SYNC resistor, SS capacitor, and FB resistors as close as possible to their respective pins. Connect their other terminals to the SGND plane.
- Keep all the power and load connections short to keep inductances at minimum levels.
- Connect the PGND and SGND nodes at a point where the switching activity is at its minimum, at the negative terminal of the V_{CC} bypass capacitor.
- Connect EP to a large ground plane with several thermal vias for best thermal performance.

Refer to the MAX17571 evaluation kit layout available at *www.maximintegrated.com* for recommended PCB layout and routing.

Typical Application Circuits

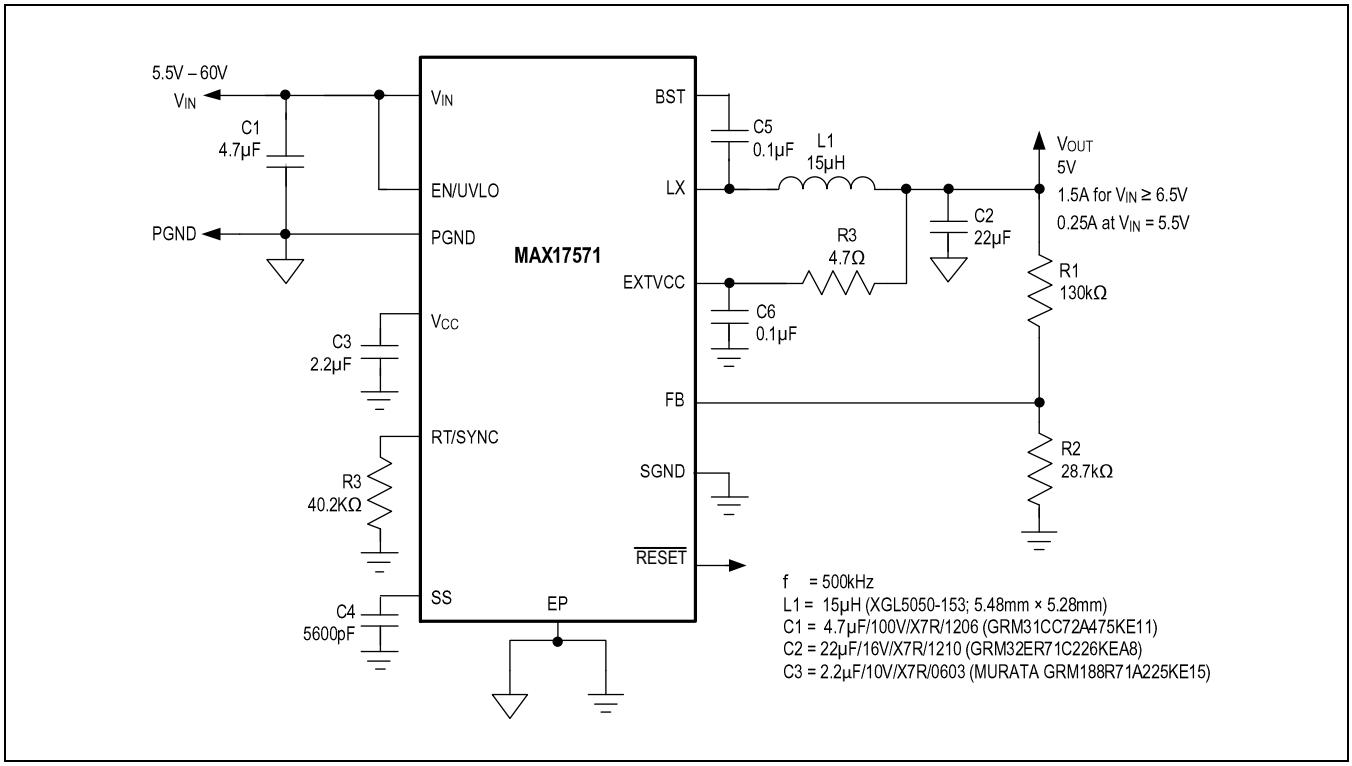


Figure 4. Typical Application Circuit for 5V Output

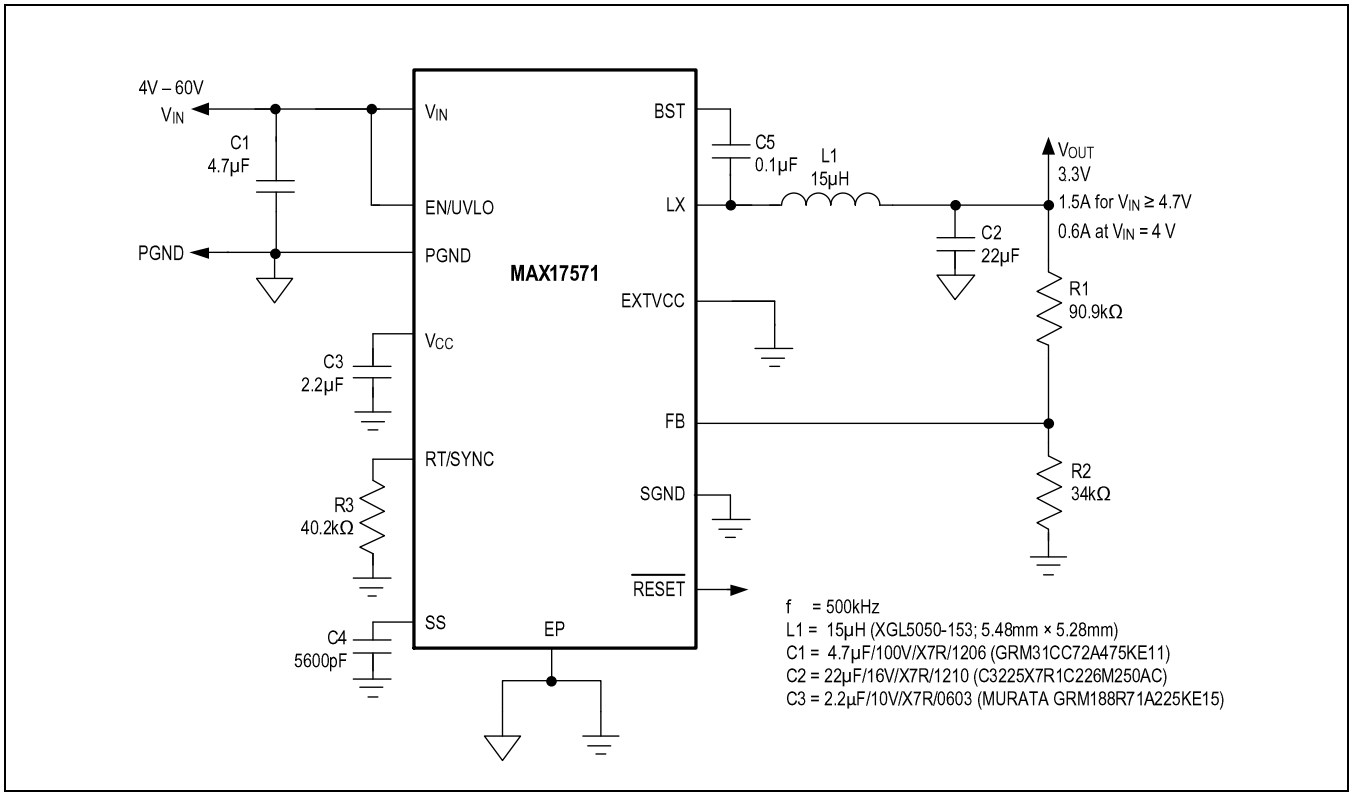


Figure 5. Typical Application Circuit for 3.3V Output

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX17571ATC+	-40°C to 125°C	12 TDFN-EP* 3mm x 3mm
MAX17571ATC+T	-40°C to 125°C	12 TDFN-EP* 3mm x 3mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed Pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/22	Release for Market Intro	—

Mouser Electronics

Authorized Distributor

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