EVALUATION KIT AVAILABLE

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MAX17332

AccuCharge + ModelGauge m5 EZ 1-Cell Charger, Fuel Gauge, and Protector

General Description

The MAX17332 is a 35µA I_Q stand-alone charger, fuel gauge, protector, and battery internal self-discharge detection IC for 1-cell lithium-ion/polymer batteries. When a voltage source is present, the IC regulates charging by modulating the charge N-FET, using AccuCharge™ charger technology. The IC regulates charge voltage, current, and FET temperature. Stand-alone charging is supported by flexible configuration in nonvolatile memory. The IC supports the following applications:

- Low-Power Charging
  - 1mA to 500mA directly from universal 5V USB
  - No USB identification/coordination needed
- High-Power Parallel Packs (>1000mA)
  - Independently charges parallel packs
  - Prevents cross-charging for parallel batteries
  - Coordinates external DC-DC with alerts
  - Minimizes dropout and heat
- Protection and Charging Control—pack or host side

The IC ideal diode circuit supports a quick response to system transients and adapter removal with low voltage drop across the CHG FET.

The IC uses the ModelGauge™ m5 EZ algorithm that combines the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge to provide industry-leading accuracy. The IC automatically compensates for cell aging, temperature, and discharge rate while providing accurate state-of-charge (SOC) in milliampere-hours (mAh) or percentage (%) over a wide range of operating conditions.

The IC monitors the voltage, current, temperature, and state of the battery to provide protection against over/undervoltage, overcurrent, short-circuit, over/undertemperature and overcharge conditions, and internal self-discharge protection using external high-side N-FETs to ensure that the lithium-ion/polymer battery operates under safe conditions which prolongs the life of the battery.

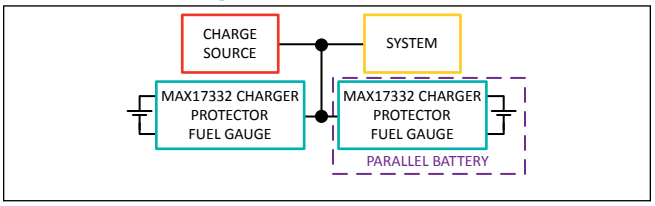
Applications

• USB PPS and Direct Charging • Smart Batteries and Hybrid Supercap Batteries • Dual Screen Smartphones, Tablets • Hearables, Wearables, Smartwatches • Medical Devices, Health, Fitness Monitors • Handheld Radios, Computers, Accessories • Home/Building Automation, Sensors, Cameras • Parallel Battery AR/VR Systems

Benefits and Features

- Non-Volatile Programmable Stand-Alone Charger
  - 1% Charge Current, 256 Current Settings
  - 0.25% Charge Voltage, 2.42V to 4.8V, Configurable
  - Optional Manual Charge Control
  - FET Temperature Limit and Heat Regulation
  - Prequal, SmartFull, and Step-Charging Options
  - JEITA—9 Temperature Regions
- Battery Health + Programmable Safety/Protection
  - Overvoltage/Overcharge Current
    - Temperature Region Dependent
  - Overcharge/Discharge/Short-Circuit Current
  - Over/Under Temperature
  - Zero-Volt or >1.8V Charging Option
  - Undervoltage + SmartEmpty
- Pushbutton Wakeup/Factory Ship Mode (0.5µA)
- ModelGauge m5 EZ Algorithm
  - Percent, Capacity,Time-to-Empty/Full, Age
  - Cycle+™ Age Forecast + Age-Scheduled Charging
- Dynamic Power—Estimates Power Capability
- SHA-256 Authentication to Prevent Cloning
- Precision Measurement Without Calibration
  - Current, Voltage, Power, Time, Cycles
  - Die Temperature and two Thermistors
- History Logging, User Data
- Low Quiescent Current
  - FETs Enabled: 35µA Active, 21µA Hibernate
  - FETs Disabled: 8µA Ship, 0.5µA Shutdown
- 2-Wire (I^2C) and 1-Wire®
- 1.9 mm x 2.5 mm 15-Bump 0.5mm Pitch Wafer-Level Package (WLP)

Simple Charger, Fuel Gauge with Protector Diagram



Ordering Information appears at end of data sheet.

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SMBus is a trademark of Intel Corp.

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

19-101220; Rev 1; 1/23

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Absolute Maximum Ratings

CP to BATT ..... -0.3V to BATT +6V
CHG to BATT ..... -0.3V to CP +0.3V
Continuous Source Current for BATT (during zero-volt charging) 50mA
Continuous Sink Current for SDA, ALRT, PFAIL 20mA
Continuous Source Current for PFAIL 20mA
Continuous Sink Current for ZVC 50mA
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature (soldering 10s) ..... +300°C

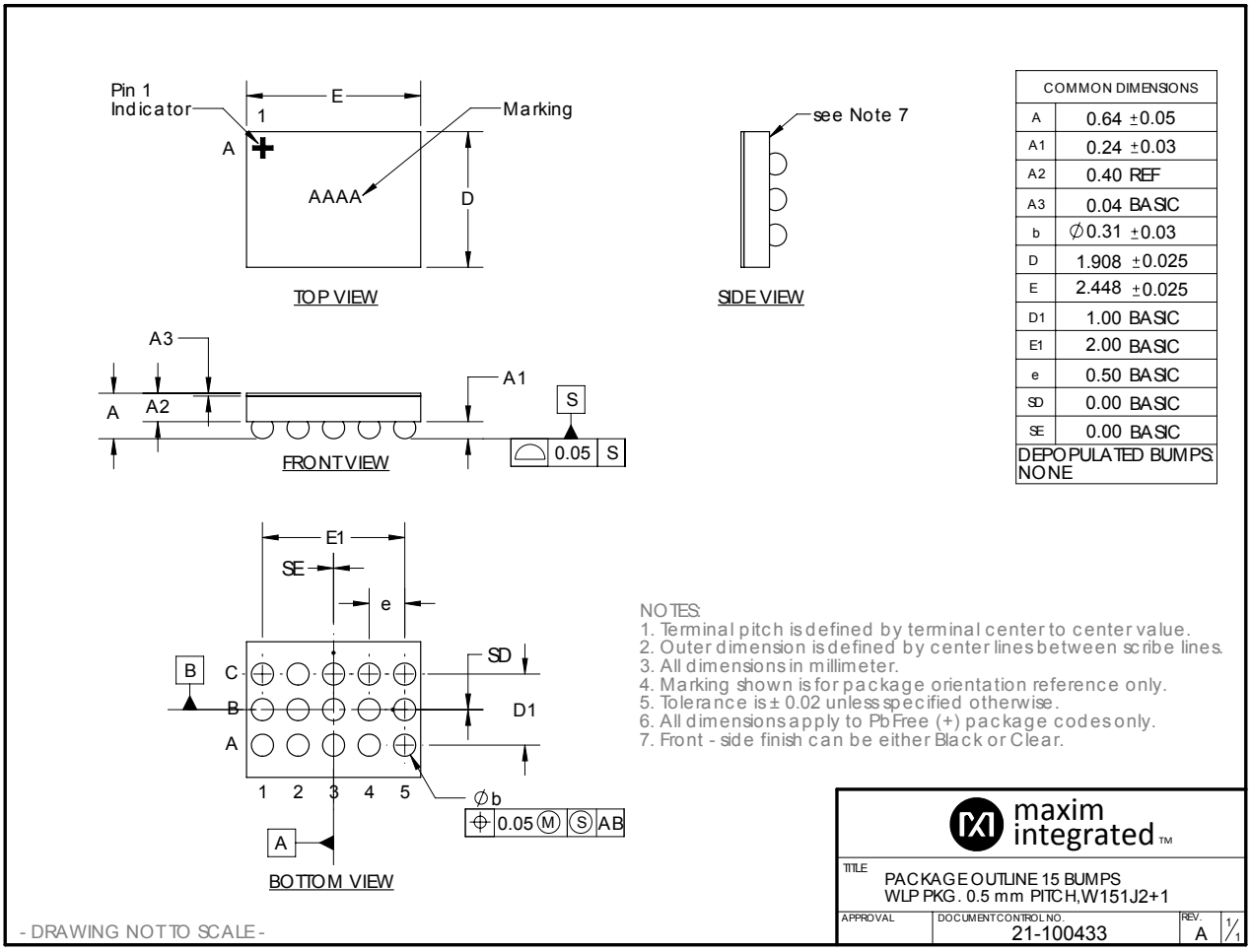
BATT to GND ..... -0.3V to +6V
ALRT to GND ..... -0.3V to +17V
TH, PFAIL to GND ..... -0.3V to BATT +0.3V
ZVC/TH2 to GND ..... -0.3V to +6V
REG to GND ..... -0.3V to +2.2V
CSN to BATT ..... BATT - 0.3V to BATT +0.3V
CSP to BATT ..... BATT - 0.3V to BATT +0.3V
DIS to GND ..... -0.3V to CP +0.3V
PCKP to GND ..... -0.3V to +28V
SDA, SCL to GND ..... -0.3V to +20V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

15 WLP

Package Code	W151J2+1
Outline Number	**21-100433**
Land Pattern Number	Refer to ***Application Note 1891***
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	62°C/W
Junction to Case (θ_{JC})	N/A



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.24 ±0.03
A2	0.40 REF
A3	0.04 BASIC
b	∅0.31 ±0.03
D	1.908 ±0.025
E	2.448 ±0.025
D1	1.00 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to Pb Free (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE	PACKAGE OUTLINE 15 BUMPS WLP PKG. 0.5 mm PITCH,W151J2+1		
APPROVAL	DOCUMENT CONTROL NO. 21-100433	REV. A	1/1

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{BATT} = 2.16V to 4.9V, typical value at 3.6V (Note 1), T_A = -40°C to +85°C, typical values are T_A = +25°C, see the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{BATT}	(Note 1)		2.16		4.9	V
Undervoltage Shutdown Supply Current	I_{DD0}	Undervoltage shutdown			0.5	1.1	µA
DeepShip Supply Current	I_{DD1}	T_A ≤ +50°C, typical at +25°C			0.5	1.1	µA
Ship Supply Current	I_{DD2}	DpShpEn = 0, T_A ≤ +50°C, typical at +25°C, protection FETs off	1.4s updates		11	24	µA
			5.625s updates		8		
Hibernate Supply Current	I_{DD3}	T_A ≤ +50°C, typical at +25°C, average current, CHG and DIS on, 1.4s updates			21	42	µA
Active Supply Current	I_{DD4}	T_A ≤ +50°C, typical at +25°C, average current, not including thermistor measurement current			35	58	µA
Regulation Voltage	V_{REG}				1.8		V
CHARGE ACCURACY							
Charge Voltage Accuracy	V_{GERR}	nVChgCfg1/2 setting, T_A = +25°C		-7.5		+7.5	mV
		nVChgCfg1/2 setting, -40ºC ≤ T_A ≤ +85ºC		-20		+20	
Charge Voltage Range	V_{FS}	nVChgCfg1/2 setting, 5mV resolution		3.56		4.835	V
Charge Current Accuracy	I_{GERR}	nIChgCfg1/2 vs. CSP-CSN, Charge Current set 10mV to 25.6mV		-1.1		+1.1	%
		nIChgCfg1/2 vs. CSP-CSN, Charge Current set 6mV to 10mV		-1.15		+1.15	
	I_{GERR}	nIChgCfg1/2 vs. CSP-CSN, Charge Current from 4mV to 6mV		-1.25		+1.25	% of Reading
	I_{GERR}	nIChgCfg1/2 vs. CSP-CSN, Charge Current from 2.5mV to 4mV		-1.4		+1.4	%
Charge Current Range	I_{FS}	nIChgCfg1/2 setting, 400mA to 2560mA, 10mA steps (with 10mΩ)		2.5		25.6	mV
Charge Heat Regulation Max Setting		nChgCfg1.HeatLim; R_{SENSE} = 10mΩ; multiply R_{SENSE}/10mΩ for other sense resistors			3264		mW
ANALOG-TO-DIGITAL CONVERSION							
Voltage Measurement Error	V_{GERR}	T_A = +25°C, 2.3V ≤ V_{BATT} ≤ 4.9V		-7.5		+7.5	mV
		-40ºC ≤ T_A ≤ +85ºC, 2.3V ≤ V_{BATT} ≤ 4.9V		-20		+20	
Voltage Measurement Resolution	V_{LSB}				78.125		µV
Current Measurement Offset Error	I_{OERR}	CSP = CSN = 3.6V, long-term average (Note 2)			±1.5		µV
Current Measurement Gain Error	I_{GERR}	CSP between CSN-50mV and CSN+50mV		-1		+1	% of Reading

Electrical Characteristics (continued)

(V_{BATT} = 2.16V to 4.9V, typical value at 3.6V (Note 1), T_A = -40°C to +85°C, typical values are T_A = +25°C, see the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current Measurement Resolution	I_{LSB}				1.5625		µV
Current Measurement Range	I_{FS}				±51.2		mV
Internal Temperature Measurement Error	TI_{GERR}				±1		ºC
Internal Temperature Measurement Resolution	TI_{LSB}	TH (Note 2)			0.00391		ºC
Auxiliary Ratiometric Measurement Error	TE_{GERR}			-0.5		+0.5	% of Reading
PCKP Measurement Resolution	VP_{LSB}				312.5		µV
PCKP Measurement Range	VP_{FS}			1.5		BATT + 5.12	V
PCKP Versus BATT Measurement Error	VP2Berr	T_A = +25ºC		-10		+10	mV
PCKP							
PCKP Startup Voltage				3.1			V
PCKP Startup Hysteresis				100	170	220	mV
PCKP Current		BATT = PCKP	T_A < +85°C, typical at T_A = +25°C		1.2	2.5	µA
PCKP Pulldown Resistor	R_{PDPCKP}			24	40	60	kΩ
CHARGE PUMP							
CP Output Voltage	V_{CP}	Battery only	I_{CHG} + I_{DIS} = 1µA	2 x V_{BATT} - 0.4	2 x V_{BATT} - 0.2	2 x V_{BATT}	V
CHG DRIVER							
CHG Output High	V_{OHC}	I_{OH} = -1mA		V_{CP} - 0.4			V
CHG Output Low	V_{OLC}	I_{OL} = 1mA				BATT + 0.4	V
DIS DRIVER							
DIS Output High	V_{OHD}	I_{OH} = -100µA		V_{CP} - 0.4			V
DIS Output Low	V_{OLD}	I_{OL} = 100µA				0.1	V
ZERO-VOLT CHARGE							
Voltage Drop Between ZVC and BATT	$V_{ZVCDROP}$	30mA into ZVC	BATT = 0V		1.4	2	V
			BATT = 2.3V		0.15	0.5	

Electrical Characteristics (continued)

(V_{BATT} = 2.16V to 4.9V, typical value at 3.6V (Note 1), T_A = -40°C to +85°C, typical values are T_A = +25°C, see the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT/OUTPUT						
Output Drive Low, ALRT, SDA, PFAIL	V_{OL}	I_{OL} = 4mA, V_{BATT} = 2.3V	0.01		0.4	V
Output Drive High, PFAIL	V_{OH}	I_{OH} = -1mA, V_{BATT} = 2.3V	V_{BATT} - 0.1			V
Input Logic High, SCL, SDA, PIO	V_{IH}		1.5			V
Input Logic Low, SCL, SDA, PIO	V_{IL}				0.5	V
PIO Wake Debounce	PIO_WD	Ship mode		100		ms
External Thermistance Resistance	R_{EXT10}	nPackCfg.R100 = 0		10		kΩ
	R_{EXT100}	nPackCfg.R100 = 1		100		
RESISTANCE AND LEAKAGE						
Leakage Current, CSN, CSP, ALRT, TH	I_{LEAK}	V_{ALRT} < 15V	-1		+1	µA
Input Pulldown Current	I_{PD}	SDA, SCL pin = 0.4V		0.2	0.5	µA
COMPARATORS						
Overcharge Current Threshold Offset Error	OC_{OE}	OC comparator	-0.8		+0.8	mV
Overdischarge Current Threshold Offset Error	OD_{OE}	OD comparator	-1.5		+1.5	mV
Short-Circuit Threshold Offset Error	SC_{OE}	SC comparator	-2.5		+2.5	mV
Overcurrent Threshold Gain Error	$ODOCSC_{GE}$	OC, OD, or SC comparator	-4.0		+4.0	% of Threshold
Overcurrent Comparator Delay	OC_{DLY}	OD or SC comparator, 20mV minimum input overdrive, delay configured to minimum		2	6	µs
Supplement Mode Comparator Threshold Falling PCKP Versus BATT	$V_{SUP\_TH\_F}$	BATT ≥ 3.4V, PCKP sweep down		30		mV
TIMING						
Time-Base Accuracy	t_{ERR}	T_A = +25°C	-1		+1	%
SHA Calculation Time	t_{SHA}	V_{BATT} > 3V		4.5	10	ms
TH Precharge Time	t_{PRE}	Time between turning on the TH bias and analog-to-digital conversions	8.48			ms
Task Period	t_{TP}			351.5		ms
NONVOLATILE MEMORY						
Nonvolatile Access Voltage	V_{NVM}	For block programming and recalling, applied on BATT	3.0			V
Programming Supply Current	I_{PROG}	Current from BATT at 2.9V for block programming	2	5.5	10	mA

Electrical Characteristics (continued)

(V_{BATT} = 2.16V to 4.9V, typical value at 3.6V (Note 1), T_A = -40°C to +85°C, typical values are T_A = +25°C, see the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Block Programming Time	t_{BLOCK}			368	7360	ms
Page Programming Time	t_{UPDATE}	SHA secret update or learned parameters update		64	1280	ms
Nonvolatile Memory Recall Time	t_{RECALL}				5	ms
Write Capacity, Configuration Memory	n_{CONFIG}	(Notes 2, 3, 4)		7		writes
Write Capacity, SHA Secret	n_{SECRET}	(Notes 2, 3, 4)		5		writes
Write Capacity, Learned Parameters	$n_{LEARNED}$	(Notes 2, 3, 4)		99		writes
Data Retention	t_{NV}	(Note 2)	10			years
1-WIRE INTERFACE, REGULAR SPEED						
Time Slot	t_{SLOT_STD}		60		120	µs
Recovery Time	t_{REC_STD}		1			µs
Write-0 Low Time	t_{LOW0_STD}		60		120	µs
Write-1 Low Time	t_{LOW1_STD}		1		15	µs
Read-Data Valid	t_{RDV_STD}				15	µs
Reset-Time High	t_{RSTH_STD}		480			µs
Reset-Time Low	t_{RSTL_STD}		480		960	µs
Presence-Detect High	t_{PDH_STD}		15		60	µs
Presence-Detect Low	t_{PDL_STD}		60		240	µs
1-WIRE INTERFACE, OVERDRIVE SPEED						
Time Slot	t_{SLOT_OVD}		6		16	µs
Recovery Time	t_{REC_OVD}		1			µs
Write-0 Low Time	t_{LOW0_OVD}		6		16	µs
Write-1 Low Time	t_{LOW1_OVD}		1		2	us
Read-Data Valid	t_{RDV_OVD}				2	µs
Reset-Time High	t_{RSTH_OVD}		48			µs
Reset-Time Low	t_{RSTL_OVD}		48		80	µs
Presence-Detect High	t_{PDH_OVD}		2		6	µs
Presence-Detect Low	t_{PDL_OVD}		8		24	µs
2-WIRE INTERFACE						
SCL Clock Frequency	f_{SCL}	(Note 5)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 6)	0.6			µs

Electrical Characteristics (continued)

(V_{BATT} = 2.16V to 4.9V, typical value at 3.6V (Note 1), T_A = -40°C to +85°C, typical values are T_A = +25°C, see the *Functional Diagram*. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 7, 8)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 7)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		5		300	ns
Fall Time of Both SDA and SCL Signals	t_F		5		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}	(Note 9)			50	ns
Capacitive Load for Each Bus Line	C_B				400	pF
SCL, SDA Input Capacitance	C_{BIN}			6		pF

Note 1: All voltages are referenced to GND.

Note 2: Specification is guaranteed by design (GBD) and not production tested.

Note 3: Write capacity numbers shown have one write subtracted for the initial write performed during manufacturing test to set nonvolatile memory to a known value.

Note 4: Due to the nature of one-time programmable memory, write endurance cannot be production tested. Follow the nonvolatile memory and SHA secret update procedures detailed in the data sheet.

Note 5: Timing must be fast enough to prevent the IC from entering shutdown mode due to bus low for a period greater than the shutdown timer setting.

Note 6: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 7: The maximum $t_{HD:DAT}$ has to only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

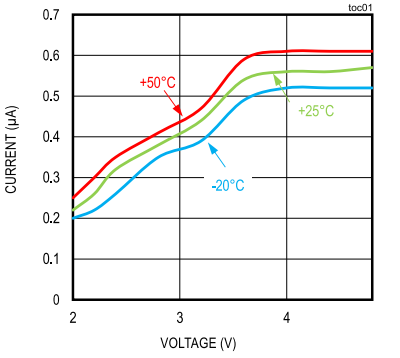
Note 8: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 9: On 10mΩ R_{SENSE}

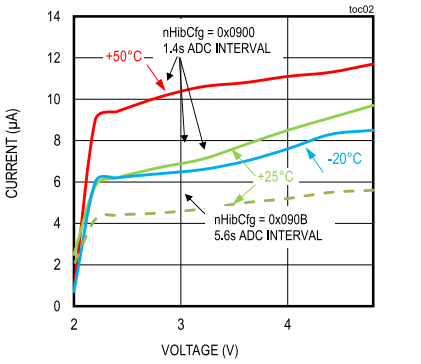
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

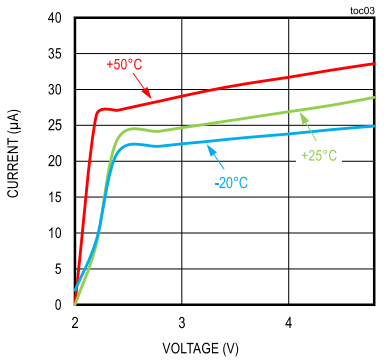
DEEP SHIP MODE CURRENT vs SUPPLY VOLTAGE



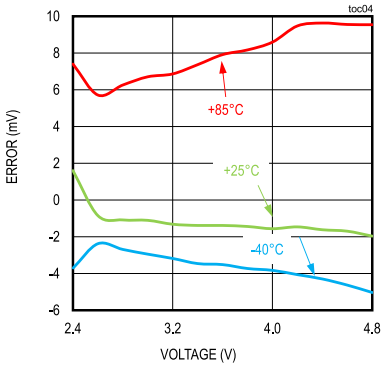
FETS OFF SHIP MODE CURRENT vs SUPPLY VOLTAGE



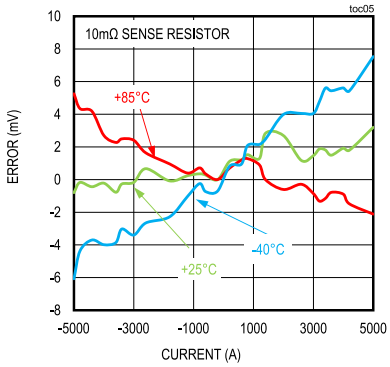
ACTIVE MODE CURRENT vs SUPPLY VOLTAGE



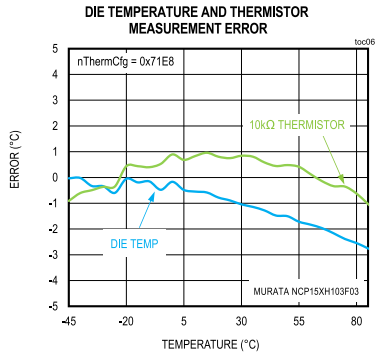
CELL VOLTAGE ADC ERROR



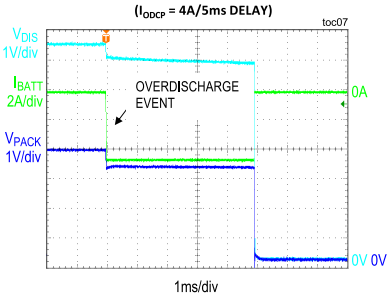
CURRENT ADC ERROR



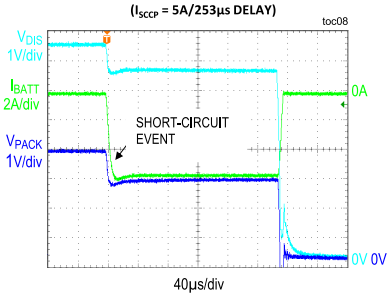
DIE TEMPERATURE AND THERMISTOR MEASUREMENT ERROR



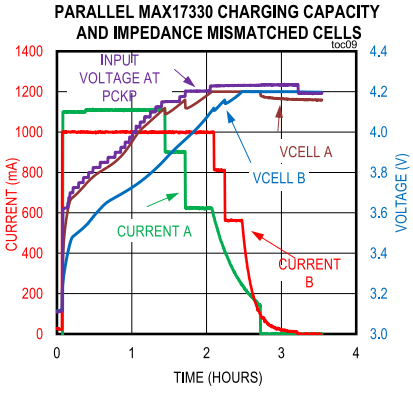
OVERDISCHARGE CURRENT PROTECTION (I_{ODCP} = 4A/5ms DELAY)



SHORT-CIRCUIT PROTECTION (I_{SCCP} = 5A/253µs DELAY)



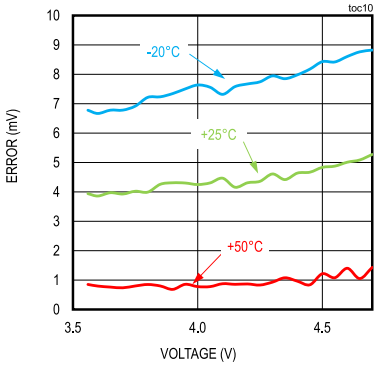
PARALLEL MAX17330 CHARGING CAPACITY AND IMPEDANCE MISMATCHED CELLS



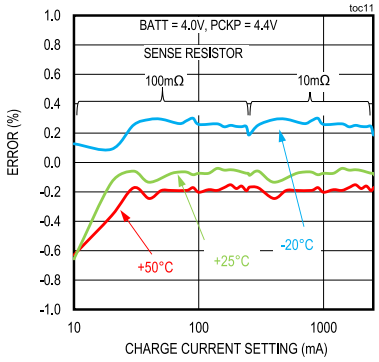
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

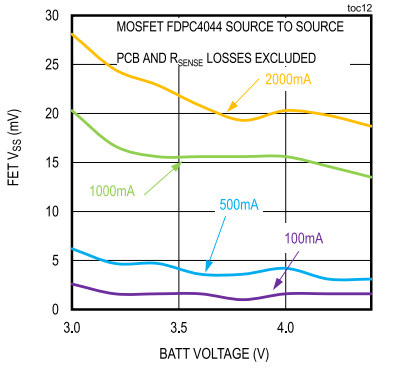
CHARGER VOLTAGE REGULATION ACCURACY



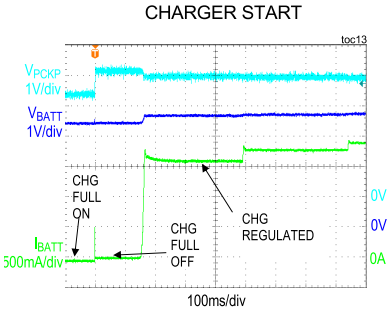
CHARGER CURRENT ACCURACY



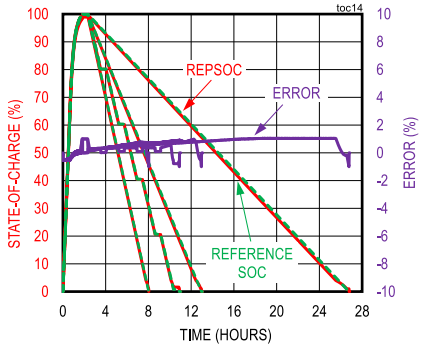
FET HEADROOM VOLTAGE AT DROPOUT DETECTION



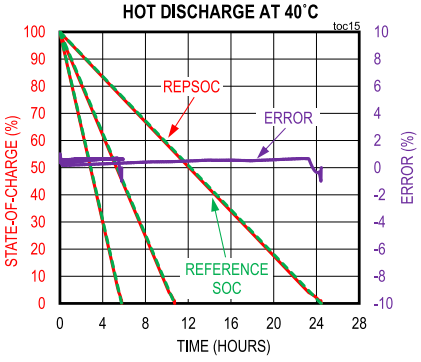
CHARGER START



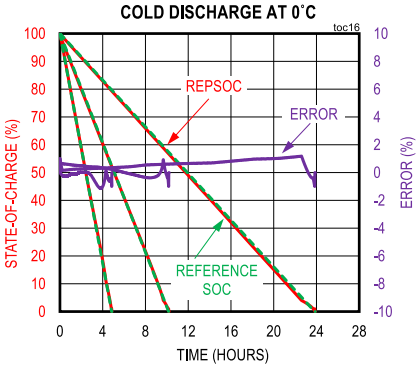
CHARGE AND DISCHARGE AT 25°C



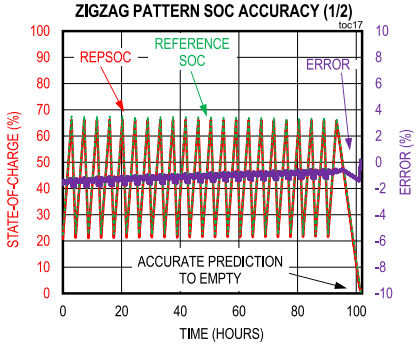
HOT DISCHARGE AT 40°C



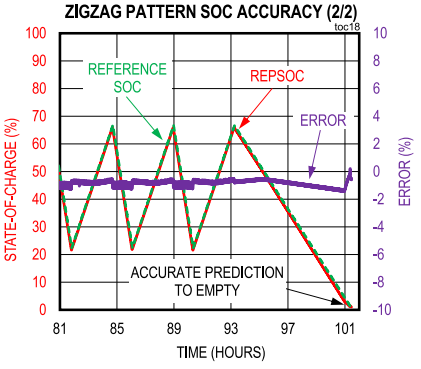
COLD DISCHARGE AT 0°C



ZIGZAG PATTERN SOC ACCURACY (1/2)

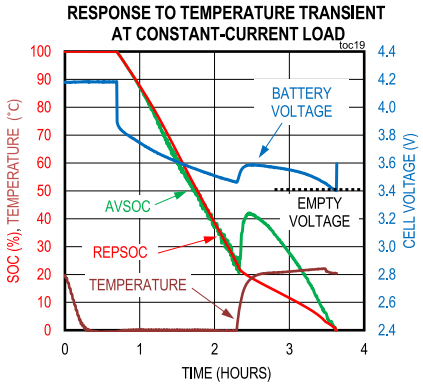


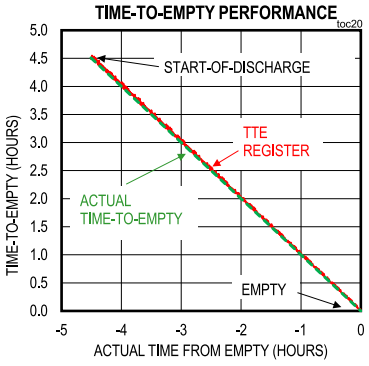
ZIGZAG PATTERN SOC ACCURACY (2/2)

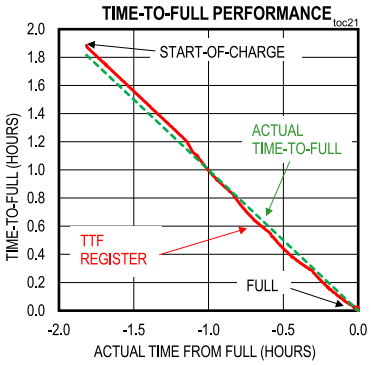


Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

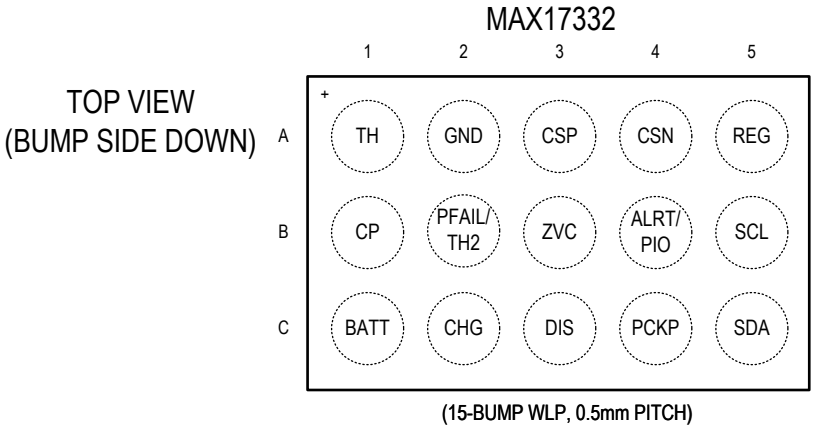






Pin Configuration

WLP 3x5



(15-BUMP WLP, 0.5mm PITCH)

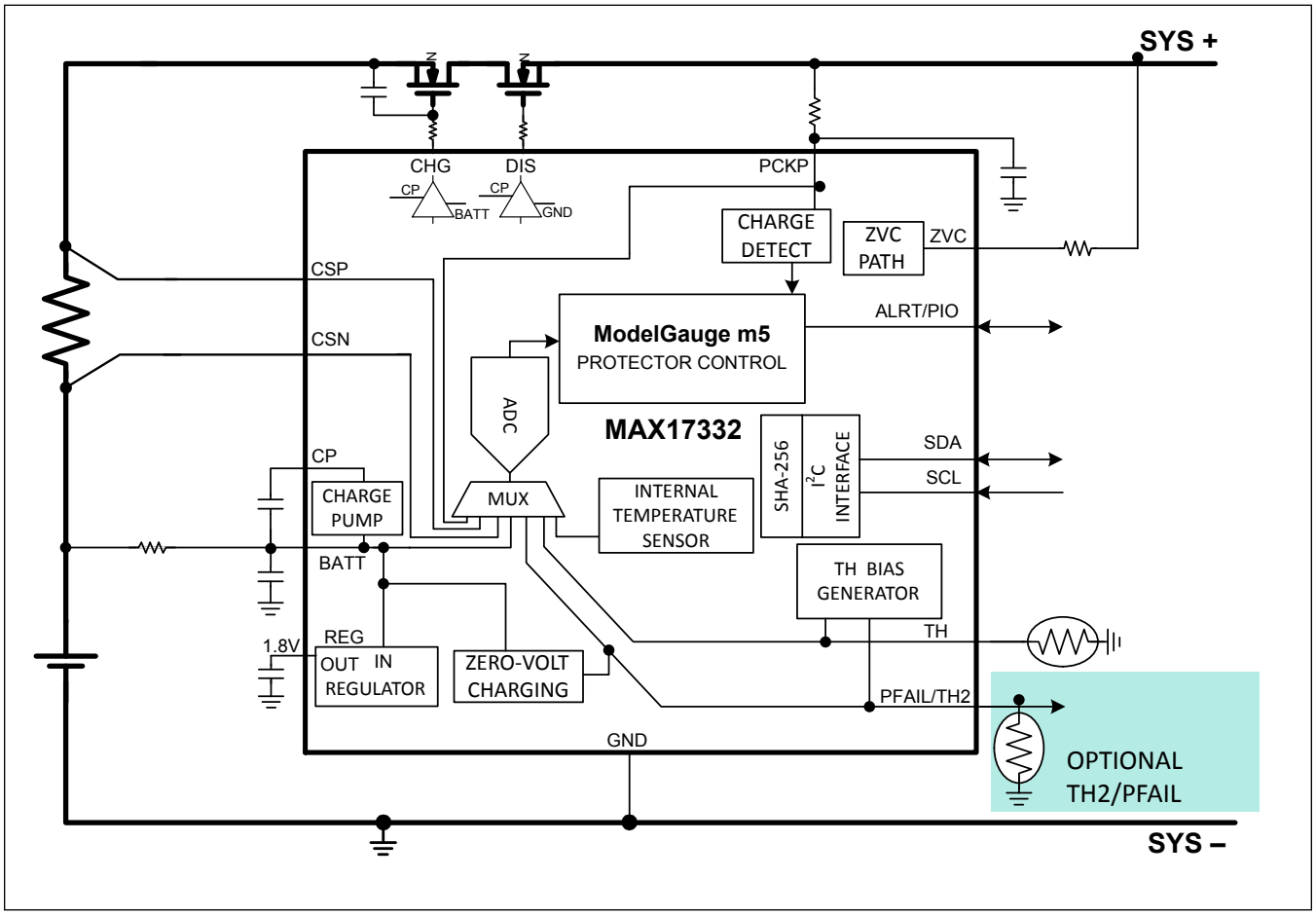
Pin Description

PIN	NAME	FUNCTION
A1	TH	Battery Thermistor Connection. Connect an external 10kΩ or 100kΩ thermistor between TH and GND to measure the battery temperature. Connect to BATT if not used.
B1	CP	Charge Pump Output. CP provides the voltage for driving external charge and discharge protection N-FETs. Connect a bypass 0.1µF capacitor between CP and BATT.
C1	BATT	Battery Connection. The MAX17332 receives power from BATT and measures cell voltage at BATT. Connect BATT to positive terminal of the battery with a 10Ω resistor and bypass with a 0.1µF capacitor to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
B2	PFAIL/TH2	Permanent Failure Indicator/Thermistor 2 (Optional). Connect to secondary protector to take action in case of primary FET failure detection. Alternative function is temperature sense for CHG-FET, connect to Thermistor. Disconnect if not used, or connect to GND with a 1kΩ resistor.
A3	CSP	Current-Sense-Resistor Positive Input. Kelvin-connect to the Pack+ side of the sense resistor.
A4	CSN	Current-Sense Negative Input. Kelvin connect to the cell side of the sense resistor.
A5	REG	1.8V Regulator. REG provides a 1.8V supply for the IC. Bypass with a 0.47µF capacitor between REG and GND.
C5	SDA	Serial Data Input/Output for I^2C Communication Modes. Open-drain output driver. Connect to the DATA terminal of the battery pack. SDA has an internal pulldown (IPD) for sensing pack disconnection.
B5	SCL	Serial Clock Input for I^2C Communication. Input only. For I^2C communication, connect to the clock terminal of the battery pack. SCL has an internal pulldown (IPD) for sensing pack disconnection.
B4	ALRT/PIO	Alert Output. ALRT is open-drain and active-low. Connect an external pullup resistor to indicate alerts. See the *Alerts* section for more details. *Pushbutton Wakeup*. Connect to the host-system's power button to GND without any external pullup since the IC has an internal pullup. The IC wakes up from shutdown mode when the button is pressed.
C4	PCKP	Pack Positive Terminal or System Positive Terminal. PCKP pin is used for charger detection, input voltage measurement, and overcurrent fault removal detection.
C3	DIS	Discharge FET Control. DIS enables/disables battery discharge by driving an external N-FET between CP and GND.
B3	ZVC	Zero-Volt Charge Input Pin. Connect to PCKP through a resistor for ZVC function. Leave disconnected or tie to GND if unused.
C2	CHG	Charge FET Control. CHG blocks/allows battery charge by controlling an external N-FET between CP and BATT.
A2	GND	IC GND

Functional Diagram



Detailed Description

General Description

The MAX17332 is a 35µA I_Q stand-alone charger, fuel gauge IC with protector, and SHA-256 authentication for 1-cell lithium-ion/polymer batteries which implements Maxim's ModelGauge m5 EZ algorithm without requiring host interaction for configuration. This makes the MAX17332 an excellent charger, protector, and fuel gauge. The MAX17332 charges the battery with programmable voltage and current based on measured temperature and battery state using configurable profile of voltage and current based on temperature, and cell voltage. The MAX17332 monitors the voltage, current, temperature, and state of the battery to ensure that the lithium-ion/polymer battery is operating under safe conditions to prolong the life of the battery. The voltage of the battery pack is measured at the BATT connection. Current is measured with an external sense resistor placed between the CSP and CSN pins. Power and average power are also reported. An external NTC thermistor connection allows the IC to measure the temperature of the battery pack by monitoring the TH pin, and optionally calculate the temperature of the FET with the PFAIL/TH2 pin. The TH/TH2 pins provide an internal pull-up for the thermistor that is disabled internally when the temperature is not being measured. The internal die temperature of the IC is also measured and can be a proxy for the protection/charge FET temperature if it is located close to the IC, or used with the TH2 thermistor to calculate the FET temperature if located further from the IC.

The MAX17332 controls charging in current, voltage, temperature, and power limit modes. Each of these limits is set in non-volatile memory, and the battery is charged at the highest rate within these limits. The voltage and current are adjusted over temperature to comply with the 9-zone JEITA temperature settings and with 5-zone step-charging based on the battery voltage. Additional functionality is described in the *Charge Control* section.

The MAX17332 scales the charging current based on the sense resistor, making it well suited to many types of batteries, ranging from <10 mAh in wearable applications, to >10,000 mAh in parallel packs, or large capacity applications.

The MAX17332 provides programmable discharge protection for overdischarge currents (fast, medium, and slow protection), overtemperature, and undervoltage. The IC also provides programmable charge protection for overvoltage, over/undertemperature, overcharge currents (fast and slow), charge done, charger communication timeout, and overcharge capacity fault. The IC provides ideal diode discharge behavior even while a charge fault persists. The IC provides programmable charging current/voltage prescription following JEITA temperature regions as well as step-charging. The MAX17332 provides additional protection to permanently disable the battery by overriding a secondary protector or blowing a fuse in severe fault conditions. This is useful when the IC has detected FET failure and is unable to block charge/discharge any other way. Additional functionality is described in the Protector section.

The ModelGauge m5 EZ algorithm combines the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. Additionally, the algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The MAX17332 automatically compensates for aging, temperature, and discharge rate and provides an accurate state of charge (SOC) in milliampere-hours (mAh) or percentage (%) over a wide range of operating conditions. Fuel gauge error always converges to 0% as the cell approaches empty. Dynamic power functionality provides the instantaneous maximum battery output power which can be delivered to the system without violating the minimum system input voltage. The IC provides accurate estimation of time-to-empty and time-to-full and provides three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer. In addition, age forecasting allows the user to estimate the expected lifespan of the cell.

To prevent battery clones, the IC integrates SHA-256 authentication with a 160-bit secret key. Every IC also incorporates a 64-bit unique identification number (ROM ID). Additionally, up to 122 bytes of user memory (NVM) can be made available to store custom information.

The IC supports three low-power modes: undervoltage shutdown (0.5µA), deepship (0.5µA), and ship (8µA). The IC can enter these low-power modes by command, communication collapsed (if enabled), or undervoltage shutdown. The IC can wake up from these low-power modes by communication, charger detection, or pushbutton wakeup (if enabled and installed). Pushbutton wakeup disconnects the battery from the system during shipping, yet wakes up immediately upon the user pressing the button, not needing the user to plug in a charger.

Communication with the host occurs over a standard I^2C interface. SCL is input from the host, and SDA is an open-drain

I/O pin that requires an external pullup. The ALRT pin is an output that can be used as an external interrupt to the host processor if certain application conditions are detected.

Charge Control

Lithium-ion/polymer batteries are very common in a wide variety of portable electronic devices because they have a very high energy density, minimal memory effect, and low self-discharge. However, care must be taken to avoid overheating or overcharging these batteries to prevent damage to the batteries potentially resulting in dangerous outcomes/explosive results. By operating in safe temperature ranges, at safe voltages, and under safe current levels, the overall safety of the lithium-ion/polymer batteries can be assured throughout the life of the battery.

MAX17332 controls the charging voltage and current dynamically based on the JEITA charge profile, step-charging, battery temperature, and temperature of the charging FET. The charge current is reduced at low battery voltage (prequal), low and high temperature, or when the charging FET is in a temperature or power dissipation limit. Figure 1 shows the typical charge profile through the operating range of a battery. MAX17332 has several regulation and control options, shown in the list below.

- **Autonomous Charger** with non-volatile configuration.
- **Constant Current Regulation**. Configurable from 185mA to 2331mA (with a 10mΩ sense resistor) and step size configurable as described in Table 70, with 1% accuracy. Scalable with a sense resistor for larger or smaller currents and batteries. See Table 13.
- **Constant Voltage Regulation**. Configurable in 5mV steps from 3.56V to 4.835V (or 10mV steps from 2.42V to 4.97V) with 0.25% accuracy.
- **Constant Power Regulation**. The MAX17332 measures the pack and battery voltage and charging current to calculate the power in the FET and sense resistor. The IC regulates heat with a configurable threshold (scalable with a sense resistor).
- **Temperature Regulation**. The IC regulates the FET temperature to a configurable threshold.
- **Supplement Mode** quickly supported with ideal diode.
- **Parallel Cell Management**, including cross-charge blocking.
- **Manual Charge Control**. If enabled, the host can manually override the autonomous control and write the ChargingVoltage and ChargingCurrent registers directly.
- **Age Scheduled Charge Duration.** If enabled, the MAX17332 can derate the ChargingVoltage and ChargingCurrent as the battery ages. See *nAgeChgCfg*.
- **Zero Volt Charging/Blocking** and Battery Prequalification.

Table 1 and Table 2 show an example of the charge profile with step charging and JEITA profile changing the target charge current and charge voltage. See *nICHgCfg1,nICHgCfg2*, *nVChgCfg1,nVChgCfg2*, *nStepCurr*, *nStepVolt*, *nTPrtTh1*, *nTPrtTh2* and *nDesignCap* for configuration details.

Table 1. Charging Current with Step Charging and JEITA

TEMPERATURE	TOO COLD	COLD2	COLD1	COOL	ROOM	WARM	HOT1	HOT2	TOO HOT
	<-10°C	-10°C – 0°C	0°C – 10°C	10°C –20°C	20°C – 40°C	40°C – 45°C	45°C – 50°C	50°C – 55°C	>55°C
Step 4	No Charging	0.438°C	0.484°C	0.531°C	0.609°C	0.547°C	0.500°C	0.453°C	No Charging
Step 3	No Charging	0.484°C	0.547°C	0.594°C	0.688°C	0.625°C	0.578°C	0.516°C	No Charging
Step 2	No Charging	0.547°C	0.609°C	0.656°C	0.766°C	0.703°C	0.641°C	0.578°C	No Charging
Step 1	No Charging	0.594°C	0.672°C	0.734°C	0.844°C	0.766°C	0.703°C	0.641°C	No Charging
Step 0	No Charging	0.719°C	0.797°C	0.875°C	1.000°C	0.922°C	0.844°C	0.766°C	No Charging

Table 2. Charging Voltage with Step Charging and JEITA

TEMPERATURE	TOO COLD	COLD2	COLD1	COOL	ROOM	WARM	HOT1	HOT2	TOO HOT
	<-10°C	-10°C – 0°C	0°C – 10°C	10°C –20°C	20°C – 40°C	40°C – 45°C	45°C – 50°C	50°C – 55°C	>55°C
Step 4	No Charging	4.115V	4.145V	4.175V	4.200V	4.175V	4.145V	4.415V	No Charging
Step 3	No Charging	4.090V	4.120V	4.150V	4.175V	4.150V	4.120V	4.090V	No Charging
Step 2	No Charging	4.065V	4.095V	4.125V	4.150V	4.125V	4.095V	4.095V	No Charging
Step 1	No Charging	4.040V	4.070V	4.100V	4.125V	4.100V	4.070V	4.040V	No Charging
Step 0	No Charging	4.015V	4.045V	4.075V	4.100V	4.075V	4.045V	4.015V	No Charging

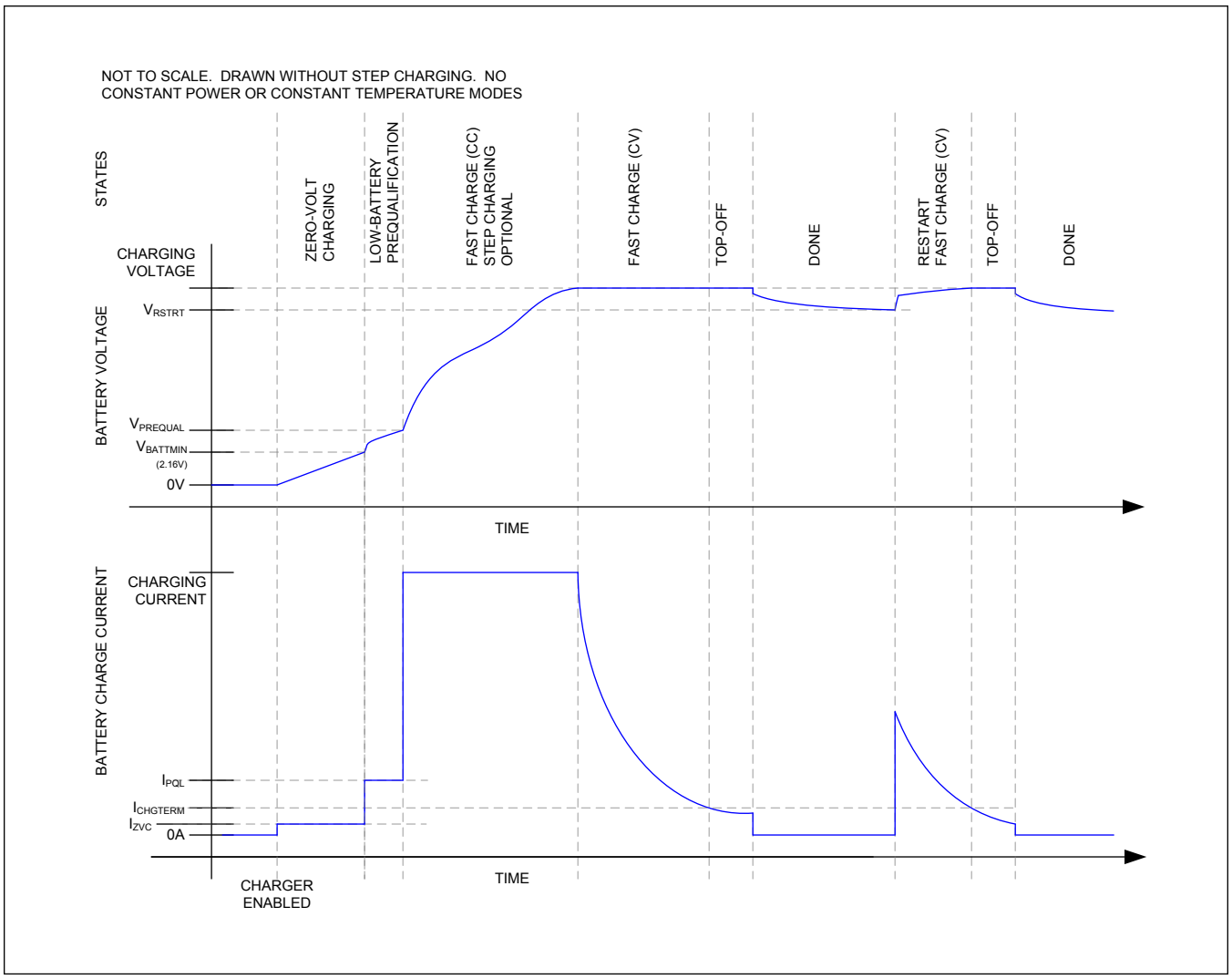


Figure 1. Li+/Li-Poly Charge Profile

$V_{BATTMIN}$: Minimum operating voltage of the MAX17332. If ZVC is used, the battery is charged through the external resistor and ZVC pin until the IC can power on.

$V_{PREQUAL}$: Enabled in nProtCfg. The battery is charged at a limited rate to check if it is safe to charge. Prequal Voltage and Current are set in the nChgCfg0 register.

Charging Voltage: The battery is charged to this terminal voltage. The voltage is set in the nVChgCfg1 and nDesignCap registers for room temperature and other temperatures.

V_{RSTRT}: Once the CHG FET turns off, the cell voltage drops over time. If the cell voltage drops below the restart threshold, the CHG FET turns on and brings the cell voltage up again.

I_{ZVC}: Zero-Volt Charging Current. See the *Zero-Volt Charging* section for details.

$I_{CHGTERM}$: The charger goes into top-off mode after this current is reached. Top off ends based on a programmable timer. Set IChgTerm in the nIChgTerm register.

I_{PQL}: Prequal Charge Current. Set in nChgCfg0.

Charging Current: Fast Charging Current. The current is set in the nIChgCfg1 and nDesignCap registers for room

temperature and other temperatures. In the Fast Charge CC state, the regulation current is adjusted by nStepCurr.

The charging current and voltage are configured by the Charge Configuration registers. See the Charge Configuration section below. The Power Limit, FET Temperature limit, and second thermistor configuration are set in the *nChgCfg1* register.

More details on each register are available in the *Charging Configuration* section.

Charging Calculation

The MAX17332 calculates the safe charging voltage and charging current depending on the state of the battery and the temperature. The ChargingVoltage and ChargingCurrent registers provide the settings according to the knowledge that is installed in the battery under the principle that the battery maker knows the requirements best. This safe voltage and current, along with the power and temperature limits, are used to control the charge current to the battery.

As the temperature of the battery changes significantly above and below room temperature, most cell manufacturers recommend charging at reduced current and lower termination voltage to assure safety and improve lifespan. The MAX17332 can be configured to change its charging when the temperature crosses the TooCold/Cold2/Cold1/Cool/Room/Warm/Hot1/Hot2/TooHot programmable temperature thresholds (see *nTPrtTh1/2*). Both charging current and voltage are updated at Cold2/Cold1/Cool/Room/Warm/Hot1/Hot2 (see *nVChgCfg1/2* and *nIChgCfg1/2*). See Figure 9 and Figure 10.

Additionally, the IC provides step-charging to improve the lifespan of the battery and charge speed by applying a step-charging profile (see the *Step-Charging* section) as shown in Figure 2.

Step Charging

A step-charging profile sets five charge voltages, five corresponding charge currents, and manages a state-machine to transit through the stages as shown in Figure 2. The MAX17332 supports Constant Voltage Step-Charging (CV Step-Charging, shown in Figure 2) and Constant Current Step-Charging (CC Step-Charging).

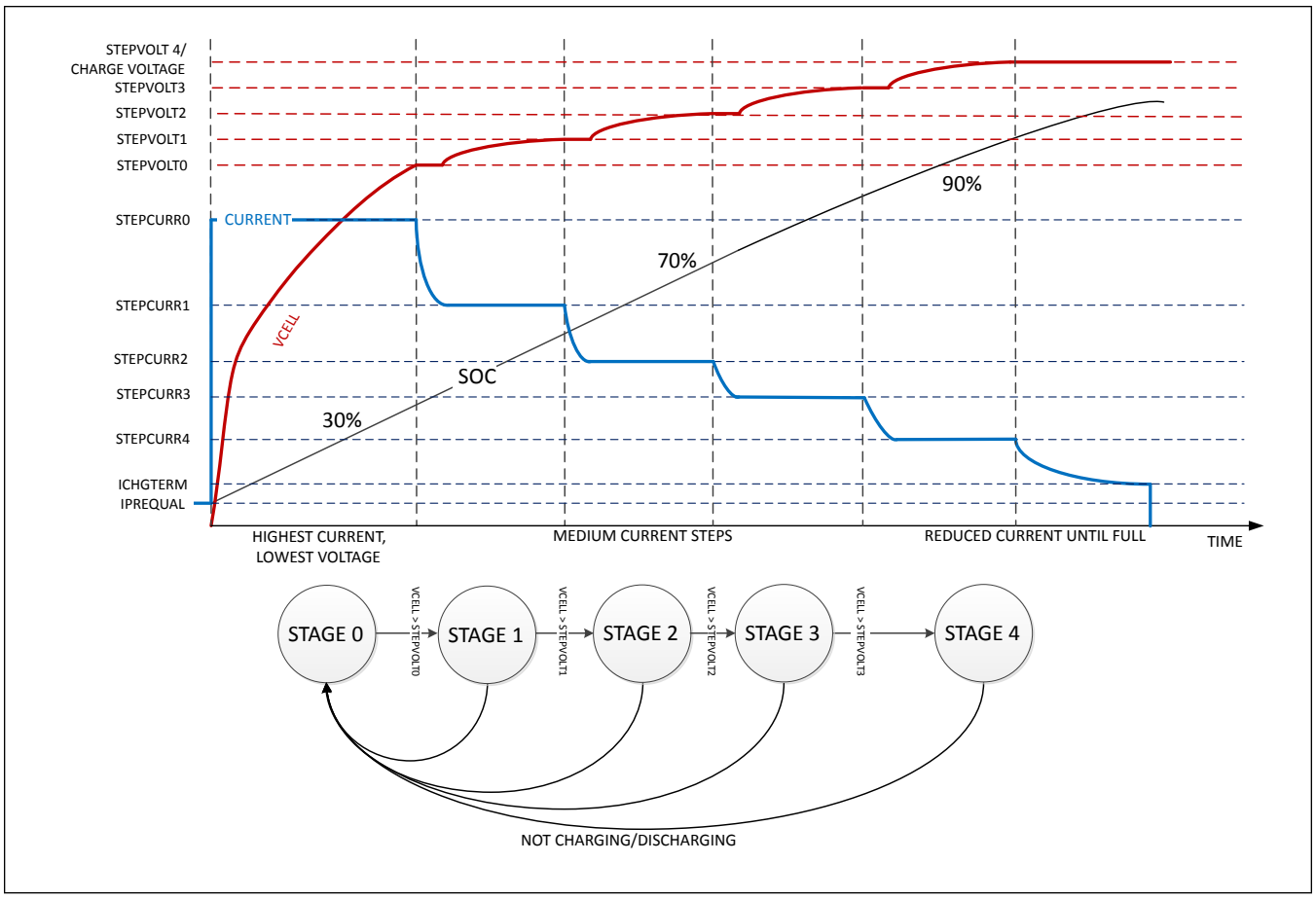


Figure 2. Step-Charging State Machine

This breaks charging into the following five charge stages:

1. **Stage 0:** Highest current, lowest voltage. ChargingCurrent comes from nIChgCfg1/2 (depending on temperature zone) until VCell > StepVolt0. After VCell > StepVolt0, ChargingCurrent becomes defined by Stage 1.
2. **Stage 1:** Step1 Current. ChargingCurrent comes from nIChgCfg1 - StepCurr1 until VCell > StepVolt1. When VCell > StepVolt1, ChargingCurrent becomes defined by Stage 2.
3. **Stage 2:** Step1 Current. ChargingCurrent comes from StepCurr1 - StepCurr2 until VCell > StepVolt2. When VCell > StepVolt2, ChargingCurrent becomes defined by Stage 3.
4. **Stage 3:** Step1 Current. ChargingCurrent comes from StepCurr2 - StepCurr3 until VCell > StepVolt3. When VCell > StepVolt3, ChargingCurrent becomes defined by Stage 4.
5. **Stage 4:** Reduced Current Until Full. ChargingCurrent comes from StepCurr3 - StepCurr.StepCurr4 until full.

Figure 2 is an example of Constant Voltage Step-Charging (CV Step-Charging) where the ChargingVoltage is held constant while the current tapers to the next Step Current when transitioning between charge stages. CV Step-Charging is enabled by setting nChgCfg0.CVStepDis = 0. CC Step-Charging is selected by setting nChgCfg0.CVStepDis = 1, which results in a direct step in the ChargingCurrent when transtioning between charge stages.

For example, a charge can start with a ChargingCurrent of 1280mA until the cell voltage reaches 4.1V. At that point, the ChargingCurrent is reduced to 1080mA until the cell voltage reaches 4.125V. At that point, the ChargingCurrent is reduced to 980mA until the cell voltage reaches 4.15V. At that point, the ChargingCurrent is reduced to 880mA until the cell voltage reaches 4.175V. Then, the ChargingCurrent is further reduced to 680mA where it remains until the current begins to taper off naturally as the cell voltage is regulated at FullChargeVoltage.

Zero-Volt Charging

When in undervoltage protection, the MAX17332 turns both FETs off and then enters a low quiescent state. After a long time in the undervoltage state, it is possible for the battery voltage to fall below the minimum 2.16V operating voltage, making it unable to wakeup by communications or pushbutton. In this situation, an external charge voltage must be applied to the system side positive node of MAX17332 (PCKP, or SYSP) to wake up the IC.

Zero-Volt Charge Recovery

In the ZVC circuit configuration (connect ZVC to PCKP), even a battery at zero volts can be charged by applying a charger at PCKP. If a secondary protector is used, zero-volt charge recovery must be enabled. If a secondary protector is not used, ZVC can be tied to GND.

Zero-Volt Charge current can be calculated as I_{ZVC} = (V_{PCKP} - $V_{ZVCDROP}$)/R_{ZVC} as shown in Figure 3. R_{ZVC} must be selected to keep ZVC current below the 50mA rated limit for the ZVC pin.

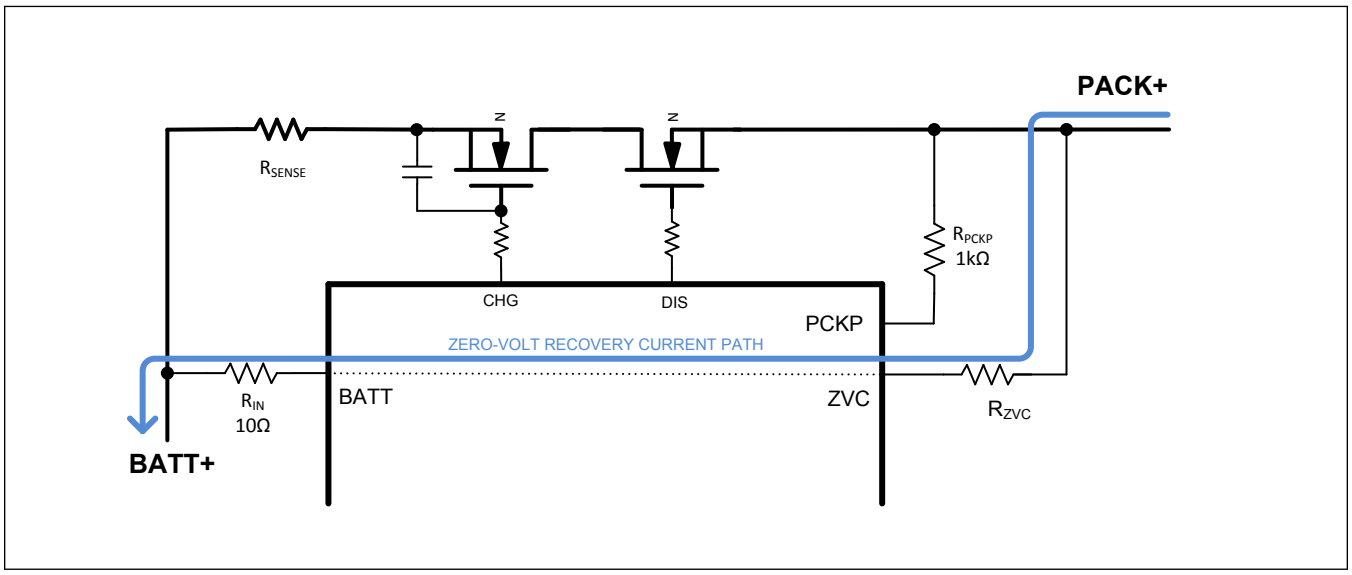


Figure 3. Zero-Volt Charge Recovery

End-of-Charge

The IC stops charging the battery when the current falls below the IChgTerm register value while the *VFOCV* value is above the nFullCfg.FullOCVThr register value. Once the End-of-Charge conditions are met, and nDelayCfg.FullTmr delay is reached, the CHG FET is turned off. The IC rejects false end-of-charge events such as application load spikes or early charge-source removal. When charge termination is detected, the device learns a new FullCapRep register value based on the RepCap register output. If the old FullCapRep value was too high, it is adjusted on a downward slope near the end-of-charge as defined by the MiscCfg.FUS setting until it reaches RepCap. If the old FullCapRep was too low, it is adjusted upward to match RepCap. This prevents the calculated state-of-charge from ever reporting a value greater than 100%. See Figure 4.

Charge termination occurs when all of the following conditions are met:

- VFOCV > FullOCVThr
- Current < IChgTerm
- AvgCurrent < IChgTerm
- FullTimer Expired

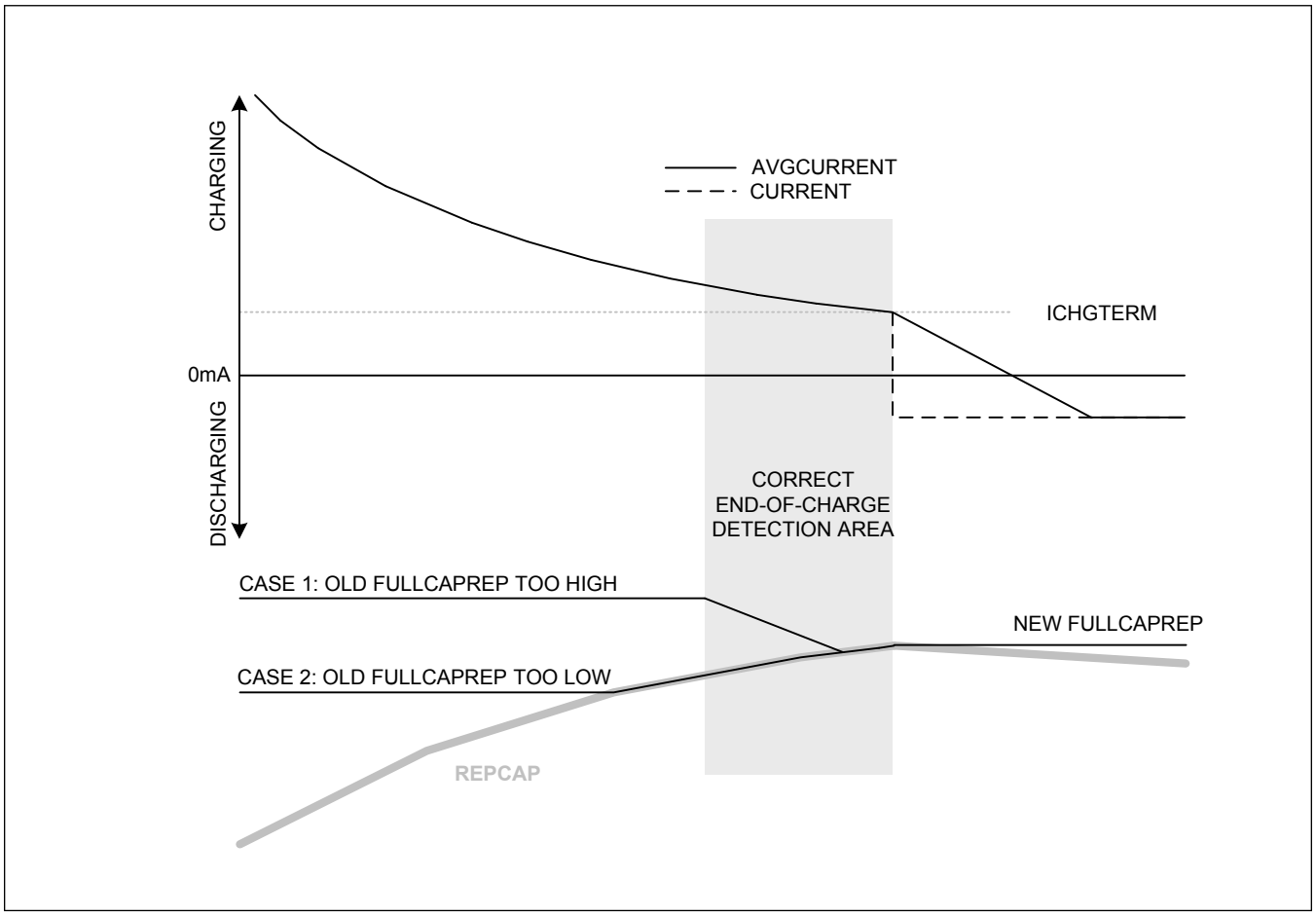


Figure 4. FullCapRep Learning at End-of-Charge

Smart-Full

Smart-full charge termination declares an end-of-charge based on the true state of the battery as determined by the open-circuit voltage (OCV) of the cell. Typical end-of-charge detection is highly variable with temperature and state of the battery. Relying on the OCV of the cell for charge termination is highly reliable as shown in Figure 5.

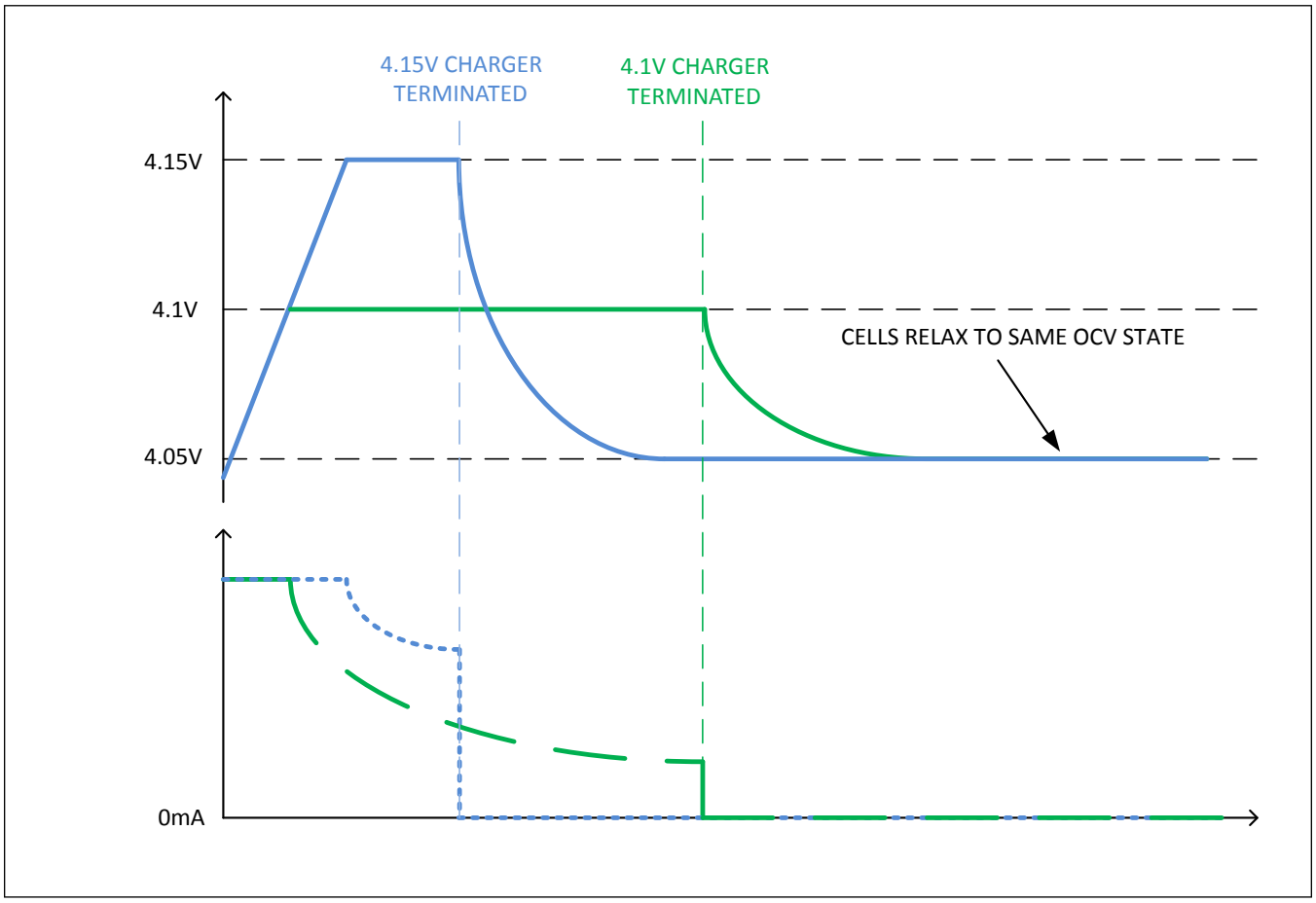


Figure 5. Smart-Full Example

Smart-full enables the following:

- **Lifespan extension combined with faster charging.** Smart-full is an alternative to reduced charging voltage (for example, 4.1V charging) to extend the life of the battery. Smart-full offers an alternative strategy allowing conventional charge voltage (for example, 4.15V). Smart-full controls termination to the same battery state as the reduced charger voltage approach.
- **Faster charging to normal state by charging to higher cell voltage**. Smart-full allows a higher charging voltage to be used, but prevents the OCV of the cell from exceeding the user-defined smart-full threshold.
- **Better normal charge termination**. Better control of charge termination even for normal 4.2V charging. Smart-full is more accurate than the traditional charge-current termination approach. It is especially robust against:
  - Adapter current limit interaction
  - Recharging near full
  - Charge control at hot and cold
  - Aged battery

The MAX17332 supports smart-full charge termination and opens the CHG FET and sets the reported SOC to 100% when the VFOCV (estimated open-circuit voltage) is greater than the smart-full threshold, current has dropped below the charge termination threshold and the *nDelayCfg*. FullTimer expires. See *nFullCfg* for details.

Charger Restart

MAX17332 supports restart charging if the charge-source is plugged in for an extended period. This allows topping off the battery for charge lost due to self discharge. In the Charge-done state, the IC begins charging the battery when VFOCV falls nChgCfg2.ReChgTh below VFOCV at end-of-charge.

Parallel Battery Management

The MAX17332 supports automation to manage parallel charging or discharging of multiple batteries and prevent one battery from charging the other (cross-charging) with the following features and benefits:

- **Converge cell voltages** faster with independent control
  - Priority to charge emptiest battery first
  - Priority to discharge fullest battery first
  - Charge and discharge in parallel once cell voltages converge
- **Prevent cross-charge** to optimize heat and dropout
  - Break-Before-Make Control
    - Charge Source Insertion: Discharge blocking applies before enabling charge.
    - Charger Source Removal: Charge blocking applies before enabling discharge.

Set nPackCfg.ParEn = 1 to enable the Parallel Battery Management functionality. When enabled, a timeout automatically sequences charge/discharge blocking and enabling. The automatic charge-blocking feature allows the host to determine which battery must be charged first and charge only the battery that is selected. Automatic discharge blocking prevents batteries at a higher state from charging batteries at a lower state.

- **To block discharging** while allowing charging, set Config2.BlockDisEn = 1.
- Status.AllowChgB is internally set every 1.4s.

Parallel Applications:

- **Low-Power Parallel Charging** (less than 500mA total). *This application eliminates the USB-charge-controller IC.* A 5V source, such as USB, connects directly (or by USB-switch) to the system as well as both packs. USB detection (such as BC1.2) is often not necessary since all generations of USB provide 500mA. Charging parallel batteries (multiple MAX17332 ICs) with greater than 500mA is not recommended without determining the source capability. The combined charging current should be limited to less than the source capability to prevent oscillations in charging current.

  Example: Two batteries each charging less than 250mA, the CHG FET heat is lower than 350mW across 99% of the charge curve, and less than 200mW for the majority of charging. During charging, a lithium battery exceeds 3.6V for 99% of the charge curve. Heat dissipated = 250mA x (5.0V - 3.6V) = 350mW.
- **High-Power Parallel Charging** (>500mA total). A USB-charger or other configurable DC-DC should deliver voltage about 50mV above the battery voltage. The charging source must operate as a voltage source. By operating near dropout, the MAX17332 has reduced heat in the charge MOSFET. In this application, charge currents beyond 2500mA are achievable.

Host Responsibility (See the *Appendix B: Parallel Cell Management Example*):

- **Declare the presence of charge source**. Only the host has this knowledge. Repeatedly write STATUS = 0xFFDF (AllowChgB = 0). The IC automatically blocks charging if AllowChgB is not cleared repeatedly before the 1.4s timeout. After this timeout, all MAX17332 ICs revert to allow-discharge and block-charge state.
- **Configure to prevent cross-charging.** If cell voltages differ by more than 400mV, configure the higher voltage packs to block discharging. Note that the higher voltage pack resumes discharge when charge-source-presence is no longer indicated.
  - **Determine if emptiest cell can support system load** (3.3V, for example). Until lowest cell charges enough to support system loading, there is a risk of system crash while higher-voltage packs are denied discharge support.

Cross-charging should be allowed/tolerated during the limited time associated with VCell less than 3.3V.

- **Block discharge** on packs identified as cross-charging risk. Set Config2.BlockDis = 1.

- **Manage DC-DC voltage setting** (applications greater than 500mA). Use the dropout-alert and heat-alert of all MAX17332 ICs to decide to step DC-DC voltage up or down.

Table 3. Parallel Management FET Logic

PAREN	BLOCKDIS	ALLOWCHGB	CHG FET	DIS FET
0	x	x	NORMAL	NORMAL
1	0	0	NORMAL	NORMAL
1	0	1 (timeout)	BLOCK READY	NORMAL
1	1	0	NORMAL	BLOCK READY
1	1	1 (timeout)	BLOCK READY	NORMAL

In the BLOCK READY state, the CHG or DIS FET is ready to block and is turned off if charging or discharging current is observed. In the NORMAL case, the CHG/DIS FET is controlled by standard protection and charging control.

Ideal Diode Behavior

While the CHG FET is in the OFF state (CHG fault present) or in regulation mode (Charging), if a discharge current is requested from the battery, the MAX17332 provides automatic control to operate the CHG FET as a 30mV Ideal-Diode using a comparator for fast response.

The CHG FET:

- Quickly turns on upon discharge detection
- Quickly turns off upon charge detection

Upon discharge, the CHG FET is fully enhanced to prevent voltage drop when a comparator detects $V_{PCKP} < V_{BATT}$ - 30mV (typ). This prevents the 600mV voltage drop and associated heat during discharging.

Upon charge, a current-sense comparator detects charging when the sense voltage exceeds 1mV (typ) and turns off the CHG FET. The MAX17332 then decides whether or not to start or resume charging. Charge faults continue to block charging. If there are no faults, the MAX17332 starts or resumes regulated charging. See Figure 6.

The ideal diode operates during discharge as well as charge regulation. During charge regulation, the system can briefly and repeatedly overload the charge source, demanding the battery to briefly support a load pulse. The charging regulation is paused until the load pulse finishes, and the MAX17332 resumes charging regulation.

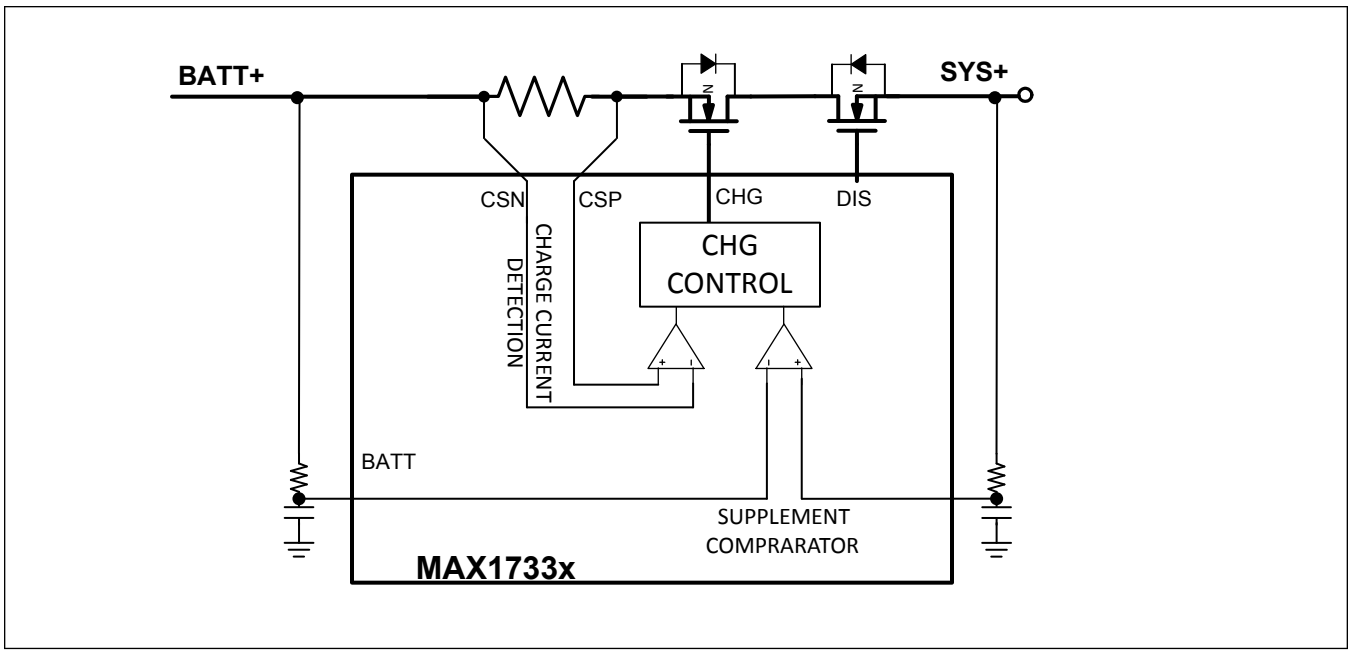


Figure 6. Supplement and Charging Comparators

The IC uses these comparators combined with additional information to detect charger presence and absence. During discharge, any charge faults, such as overvoltage fault or overtemperature fault, are preserved. The CHG FET is turned on fully to allow discharging and returned to the OFF state when a charger is detected. See Figure 7.

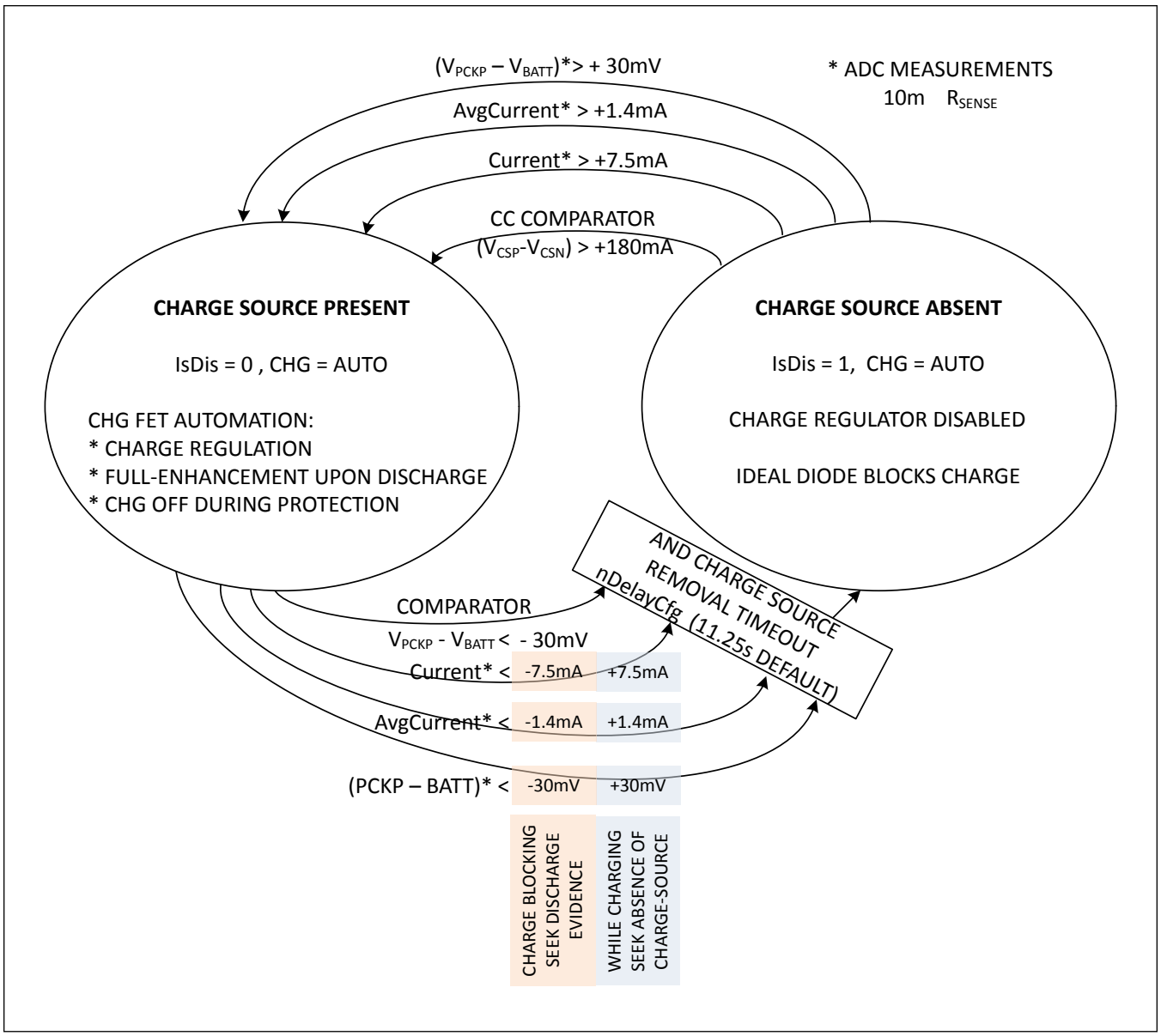


Figure 7. Charging and Discharging States

ADC Measurements corresponding to Current, AvgCurrent, and PCKP enhance the accuracy of charger detection. The charge source removal timeout waits for 11.25s (configurable with nDelayCfg.ChgWDT) of charge source absence before turning off the charge regulation. This allows charging to quickly resume after many seconds of battery-supplement when the system load exceeds charge source current-limit.

nProtMiscTh.CurrDet configures the previous current-detection thresholds, corresponding with ±1.4mA and ±7.5mA (on 10mΩ). Analog Devices recommends these settings which are optimized according to the ADC noise.

Table 4. AvgCurrDet Threshold when using 10mΩ and Default nProtMiscTh.CurrDet = 7.5mA

	AVGCURRENT FILTER CONFIGURATION (nFilterCfg.nCurr)

Table 4. AvgCurrDet Threshold when using 10mΩ and Default nProtMiscTh.CurrDet = 7.5mA (continued)

	1 (0.7s)	2 (1.4s)	3 (2.8s)	4 (5.6s)	5 (11.25s)	6 (22.5s)	7 (45s)	8 (90s)
Active (0.351s)	4.22mA	2.34mA	2.34mA	**1.41mA (default)**	1.41mA	0.94mA	0.94mA	0.7mA
Hibernate (1.4s)	7.5mA	4.2mA	4.2mA	2.3mA	2.3mA	1.4mA	1.4mA	0.94mA
Hibernate (2.8s)	7.5mA	7.5mA	7.5mA	4.2mA	4.2mA	2.3mA	2.3mA	1.4mA

The fast responses in Table 4 correspond with the 0.351s ADC update rate. The more accurate slow responses correspond with the AvgCurrent filter delay configuration.

Protector

Simple protection schemes are available to protect a battery from exceeding the safe levels. These schemes include protection for overdischarge current, short-circuit current, overcharge current, undervoltage and overvoltage. The next level of protection offers smart protection schemes which include protection for under OCV (SmartEmpty), long overdischarge current, overtemperature limits for charge and discharge, undertemperature charge limits, and charge-done protection. The MAX17332 provides all of these simple and smart protection schemes with programmable thresholds and programmable timer delays for each fault.

The MAX17332 provides additional protection functionality beyond these schemes as follows:

Discharging Protection Functionality

- **Overcurrent:** (see *nODSCCfg* and *nODSCTh*)
  - **Fast Short-Circuit (70µs to 985µs):** The short-circuit comparator is programmable from 5.12mV to 158.72mV with delay programmable from 70µs to 985µs.
  - **Medium (1ms to 15ms):** The overdischarge current comparator is programmable from 2.55mV to 79.36mV with delay programmable from 1ms to 15ms.
  - **Slow (351ms to 35s):** Slow overdischarge protection is programmable from 0mV to 51.2mV in 0.2mV steps with delay programmable from 351ms to 35s (see *nDelayCfg* and *nIPrtTh1*).
- **Overtemperature:**
  - **Hot (OTPD—Overtemperature Discharge):** Discharge overtemperature (OTPD, see *nProtMiscTh*) is separately programmable from charge overtemperature (OTPC). OTPD is typically a higher temperature than OTPC, since charging while hot is more hazardous than discharging. OTPD is programmable in 1°C steps, with a programmable timer (see *nDelayCfg*).
  - **Die-Hot:** The MAX17332 measures die temperature as well as a thermistor's temperature. Since the IC is generally located close to the external FETs, the die temperature can indicate when the FETs are overheating. This separately programmable threshold (see *nProtMiscTh*) blocks both charging and discharging.
  - **Permanent-Fail-Hot:** When a severe overtemperature is detected, the fault is recorded into NVM and permanently disables the charge and discharge FETs and blows the three terminal fuse if enabled.
- **Too Cold Discharge:** If enabled, the IC blocks discharging if the cell temperature is too low. It prevents the discharge of a cell when cell impedance due to temperature is too large to support the application load.
- **Undervoltage (UVP):** Undervoltage is protected by three thresholds: UVP (undervoltage protect), UVShdn (undervoltage shutdown), and UOCVP (under OCV protect—*SmartEmpty*). UOCVP provides deep-discharge-state protection that is immune from load and cell impedance/resistance variations.

Charging Protection Functionality:

- **Overvoltage Protection (OVP):** Overvoltage protection is programmable with 10mV resolution (see *nOVPrtTh*). Temperature-region-dependent OVP protection is also provided for cold/room/warm and hot temperature regions (see *nVChgCfg1/2*). OVP detection is debounced with a programmable timer (see *nDelayCfg*). An additional, higher OVP permanent failure threshold is programmable, which records any excessive OVP into NVM and permanently blocks charging.
- **Charge Temperature Protection:** Temperature protection thresholds are debounced with a programmable timer (see *nDelayCfg*).

  - **Hot (OTPC):** Charging temperature protection is programmable with 2.5°C resolution (see *nTPrtTh1*) and 2.5°C hysteresis.
  - **Cold (UTP):** Charging is blocked at cold, programmable with 2.5°C resolution (see *nTPrtTh1*), and no hysteresis.
- **Overcharge-Current Protection:**
  - **Fast:** Overcharge current is detected by a programmable hardware comparator and debounce timer between 0 to 39.375mV and 1ms to 15ms thresholds.
  - **Slow:** A lower and slower overcharge current protection ensures that more moderate high currents do not persist for a long time. With a 10mΩ sense resistor, this is programmable up to 5.12A in 40mA steps, with an additional delay programmable between 0.35s and 22.5s. Additionally, with *nNVCfg1*.enJP = 1, this overcurrent protection threshold is modulated according to temperature region (see *nIChgCfg1/2*).
- **Charge-Done:** If enabled, the IC blocks charge whenever charge termination is detected, until discharging or charger removal is eventually detected.
- **Charger-Communication Timeout:** If enabled, during charging the IC turns off the charge FET if the host has stopped communicating beyond a timeout configurable from 11s to 3 minutes. In systems that consult the battery for prescribing the charge current or charge voltage, especially to apply JEITA thresholds or step-charging, this feature is useful to protect against operating system crash or shutdown.
- **Overcharge-Capacity Alert:** If any charge session delivers more charge (coulombs) to the battery than the expected full design capacity, charging is briefly interrupted and a protection alert is indicated. This threshold is programmable as a percentage (see *nProtMiscTh*.QOvflwTh) beyond the design capacity.

Other Faults:

- **Nonvolatile CheckSum Failure:** If enabled (*nNVCfg1*.enProtChkSm), the MAX17332 blocks charge and discharge when startup checksum of protector NVM does not match the value stored in nProtCfg2.CheckSum.

Other Protection Functionality:

- **Zero-Volt Charging:** The IC can begin charging when the cell has depleted to 2.16V (ZVC disabled) or from 0.0V (ZVC enabled). See the *Zero-Volt Charging* section for more details.
- **Overdischarge-Removal Detection:** Following any overdischarge current fault, after the IC turns off the discharge FET, it tests for load removal by sourcing 30µA into PCKP. Load removal is detected when PCKP exceeds 1V. This low threshold is intentionally below the startup voltage of most ICs in order to allow active loads by external ICs while rejecting passive loads by resistors (short-circuit, failed components, etc.).
- **Charger Removal Detection:** Following any charge fault, after the IC turns off the charge FET, it measures PCKP to detect the removal of the offending charger. Charger removal is detected when PCKP falls below BATT - nIPrtTh2.ChgDetTh or whenever discharge current is detected.
- **Battery Internal Self-Discharge Detection:** The IC measures the internal self-discharge of the battery that might indicate health or safety problems. The IC alerts the system or turns off the charge and discharge FETs when a leakage is detected above the configurable threshold. See the *Battery Internal Self-Discharge* section for more details.
- **Ideal-Diode Control:** During any charge fault, the charge FET turns on when a discharge current is detected. See the *Ideal Diode* section for more details. The discharge FET behaves the same way during discharge faults to block discharging, yet turns on during charging. This ideal diode behavior reduces the heat and voltage drop associated with the body diode during protection faults.

Protection Fault Reporting:

- **Protection Fault Status:** Each charge and discharge fault state is latched in the ProtStatus register. When the fault is cleared, the corresponding bit is cleared.
- **Protection Fault Alerts:** The ProtAlrt register latches the status of any previous faults detected by the device. Once a fault is detected, the corresponding bit remains set until it is cleared by the host. Additionally, the Status.ProtAlrt bit is set when any ProtAlrt bit is set.
- **Protection Fault Logging:** The nFaultLog register also indicates which protection events happened during each history log period.

Charging Regulation Registers: The *ChargingVoltage* and *ChargingCurrent* registers control and display the calculated target charging voltage and current. This includes the following knowledge which generally is associated with a particular battery and can be stored in the battery with the MAX17332.

- **Factory Recommended Charging Current and Voltage:** This is useful when a system involves multiple battery vendors, swappable batteries, aftermarket batteries, or legacy system support.
- **Manual Charge Control:** If enabled, the host can manually override the autonomous control and write to the ChargingVoltage and ChargingCurrent registers directly.
- **Charging Modifications According to Battery Temperature and Age:** Significantly above and below room temperature, most cell manufacturers recommend charging at reduced current and lower termination voltage to assure safety and improve lifespan. The MAX17332 modulates its settings according to TooCold/Cold2/Cold1/Cool/Room/Warm/Hot1/Hot2/TooHot programmable temperature regions (see *nTPrtTh1*/2). Both charging current and voltage are modulated at Cold2/Cold1/Cold/Warm/Hot1/Hot2, targeting lower than Room (see *nVChgCfg1/2* and *nIChgCfg1/2*). If enabled, the MAX17332 can derate the ChargingVoltage and ChargingCurrent as the battery ages. See *nAgeChgCfg*.
- **Step-Charging:** A common practice to balance lifespan and charge speed is to apply step-charging profiles (see the *Step-Charging* section). The MAX17332 supports five programmable steps with programmable charge currents and voltages.

At a high level, the MAX17332 protector has a state machine as shown in Figure 8. Each charge and discharge fault state is latched in the *ProtStatus* register, where each fault obeys a separate instance of the state machine shown in Figure 8. Any single charge fault opens the charge FET to block charge current (charge faults are OR'd together). All charge faults must be released to allow the charge to resume (charge fault release conditions are AND'd together). The behavior is similar for blocking discharge.

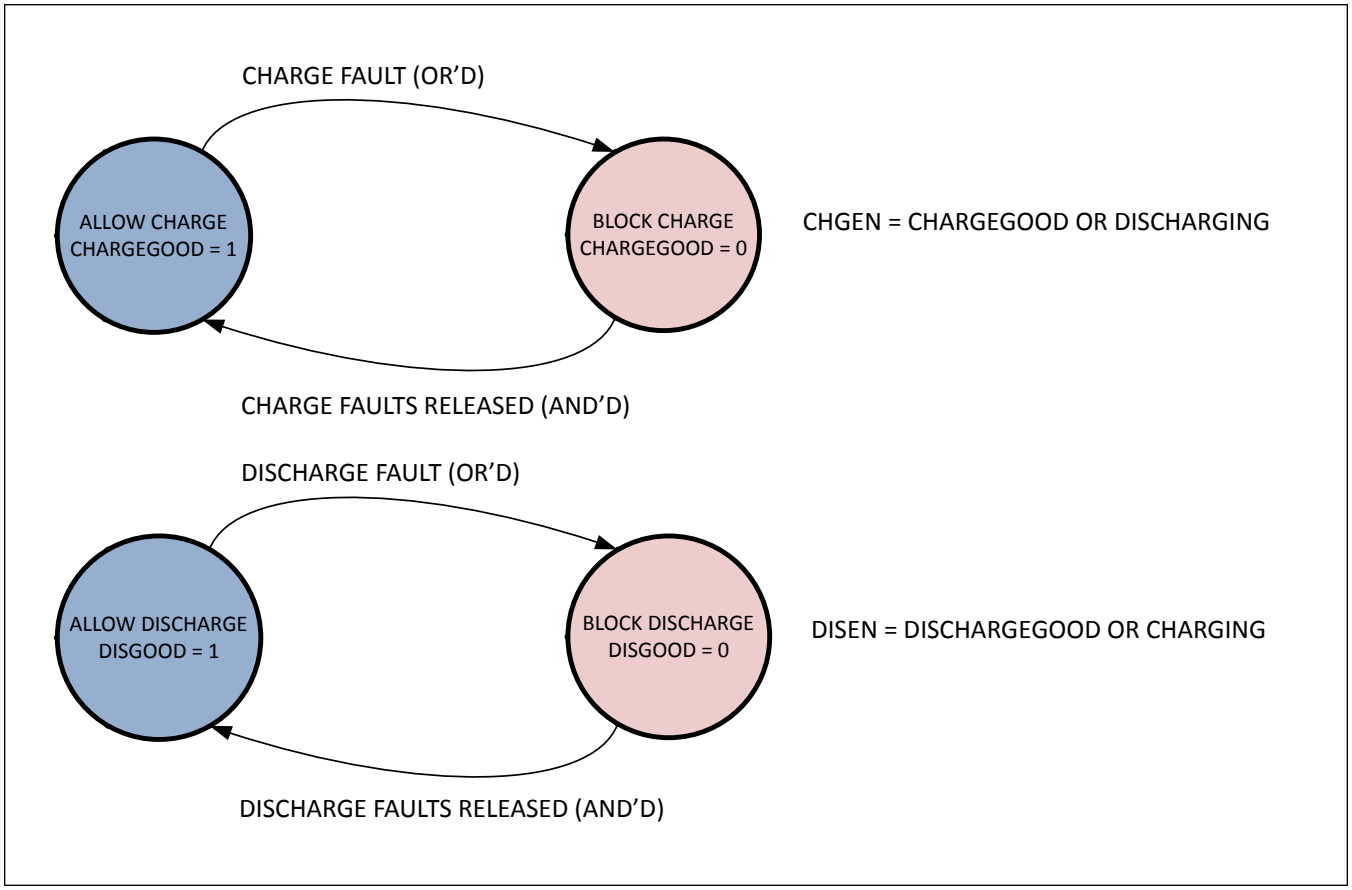


Figure 8. Simplified Protector State Machine

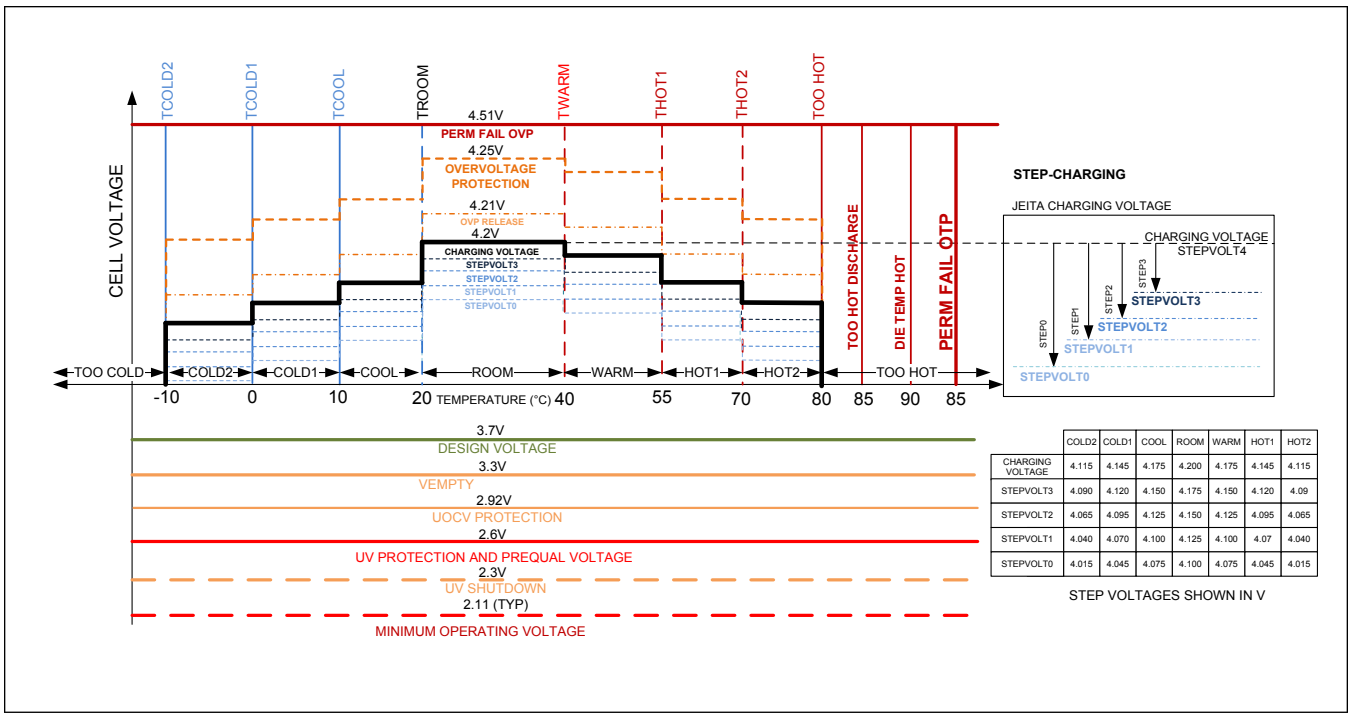
The IC includes a write protection and a permanent locking function. The write protection prevents accidental overwrites of protection parameters. This protection must be cleared before updating any registers and should be set after

configuration changes are made. The permanent locks prevent intentional or malicious tampering and should be enabled after development is completed and the battery pack is ready to ship in production. See the *Memory Locks and Write Protection* section for more details.

The protector registers are summarized by their protection function in Table 5 and are graphically shown across the various temperature ranges in Figure 9 and Figure 10.

Table 5. Summary of Protector Registers by Function

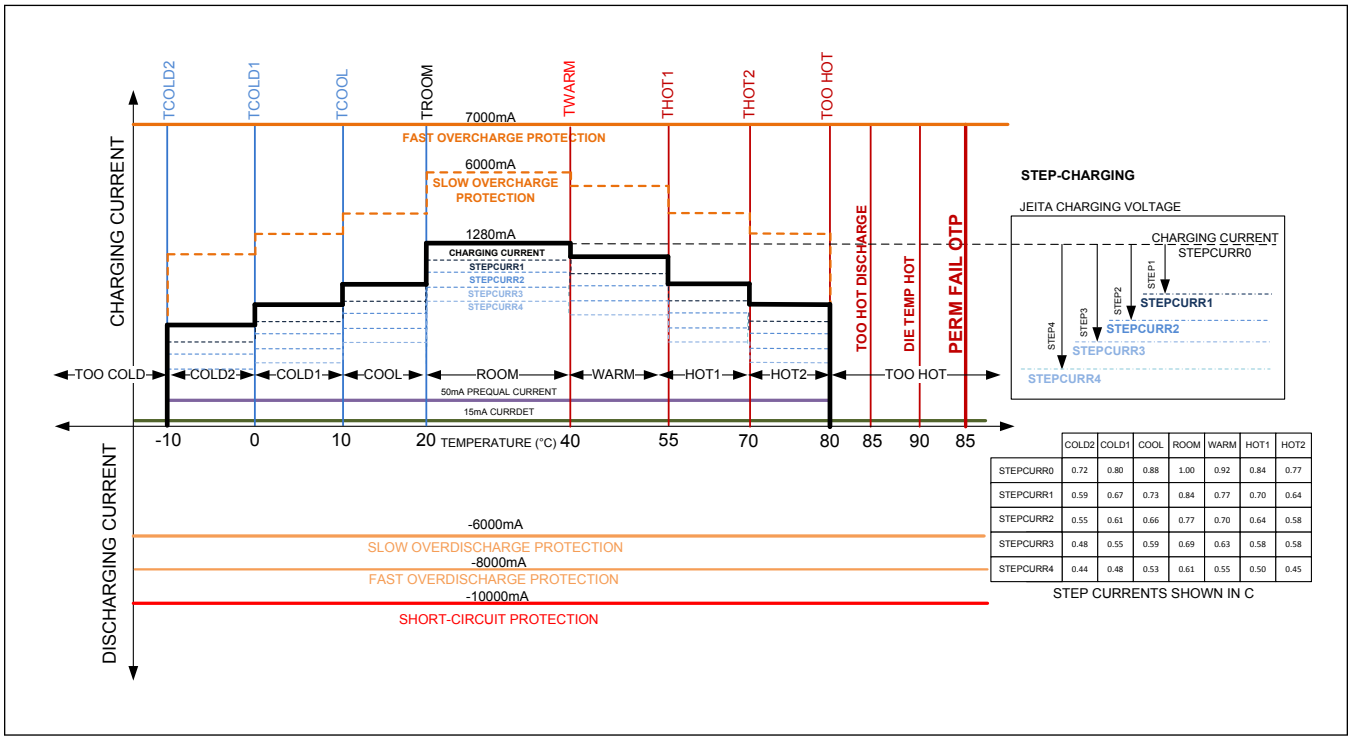
FUNCTION	REGISTER
VOLTAGE THRESHOLDS	
Permanent Fail Overvoltage Protection	nOVPrtTh
Overvoltage Protection	nVChgCfg1/2, nOVPrtTh
Overvoltage Protection Release	nOVPrtTh
UnderOCV Protection	nUVPrtTh
Undervoltage Protection	nUVPrtTh
Undervoltage Shutdown	nUVPrtTh
Prequalification Voltage	nChgCfg0
CURRENT THRESHOLDS	
Fast Overcharge Protection	nODSCTh, nODSCCfg
Slow Overcharge Protection	nIPrtTh1
Slow Overdischarge Protection	nIPrtTh2
Fast Overdischarge Protection	nODSCTh, nODSCCfg
Short-Circuit Protection	nODSCTh, nODSCCfg
Charging Detected	nProtMiscTh
Discharging Detected	nProtMiscTh
Temperature Thresholds	nTPrtTh1, nTPrtTh2, nProtMiscTh
Fault Timers	nDelayCfg
CHARGING REGULATION	
Charging Voltage	nVChgCfg1, nVChgCfg2
Charging Current	nIChgCfg1, nIChgCfg2
Precharge Current	nChgCfg0
Step Charging	nStepCurr, nStepVolt
Protection Status/Configuration	nProtCfg, ProtStatus, nBattStatus



	COLD2	COLD1	COOL	ROOM	WARM	HOT1	HOT2
CHARGING VOLTAGE	4.115	4.145	4.175	4.200	4.175	4.145	4.115
STEPVOLT3	4.090	4.120	4.150	4.175	4.150	4.120	4.09
STEPVOLT2	4.065	4.095	4.125	4.150	4.125	4.095	4.065
STEPVOLT1	4.040	4.070	4.100	4.125	4.100	4.07	4.040
STEPVOLT0	4.015	4.045	4.075	4.100	4.075	4.045	4.015

STEP VOLTAGES SHOWN IN V

Figure 9. Programmable Voltage Thresholds



	COLD2	COLD1	COOL	ROOM	WARM	HOT1	HOT2
STEPCURR0	0.72	0.80	0.88	1.00	0.92	0.84	0.77
STEPCURR1	0.59	0.67	0.73	0.84	0.77	0.70	0.64
STEPCURR2	0.55	0.61	0.66	0.77	0.70	0.64	0.58
STEPCURR3	0.48	0.55	0.59	0.69	0.63	0.58	0.58
STEPCURR4	0.44	0.48	0.53	0.61	0.55	0.50	0.45

STEP CURRENTS SHOWN IN C

Figure 10. Programmable Current Thresholds

Battery Internal Self-Discharge Detection (ISD)

A healthy lithium-ion/polymer battery has a very high coulombic-efficiency, typically greater than 99.9% (defined as discharge mAh vs. charge mAh). Some portion of the charge capacity can be lost by internal self-discharge. This includes natural aging, which is exacerbated if the battery stays at a high temperature and/or high state for long periods of time. However, in a damaged battery, additional capacity can be lost (unavailable for discharge), and some portion of this reflects permanent capacity loss. Unusual self-discharge in a lithium-ion/polymer battery might indicate health or safety problems.

The MAX17332 internal self-discharge (ISD) detection feature measures battery leakage and provides the following functions:

- **Leakage Measurement:** The LeakCurrRep register outputs the milliampere leakage measured across several days and multiple charge termination events.
  - Accurate leakage detection
  - Low ppm false-positive rate at a 3mA threshold
  - Detection during normal use
    - No discharge depth or duration constraints
    - Requires at least four full events, each separated by 20 hours or more
- **Leakage Log:** Leakage measurements are recorded in the battery-life-logging data. This reveals leakage versus time for any returned battery or for managing deployed packs.
- **Leakage Alert:** If enabled, an LDET alert (see *ProtAlrt*) is asserted when LeakCurrRep exceeds the programmable alert threshold.
- **Leakage Fault:** If enabled, the protector disconnects the battery when LeakCurrRep exceeds the programmable fault threshold.

Example of Internal Self-Discharge Detection

Figure 11 shows the current leakage detected by the MAX17332 as a result of placing a 909Ω resistor across a cell to emulate a battery with internal self-discharge over various temperatures.

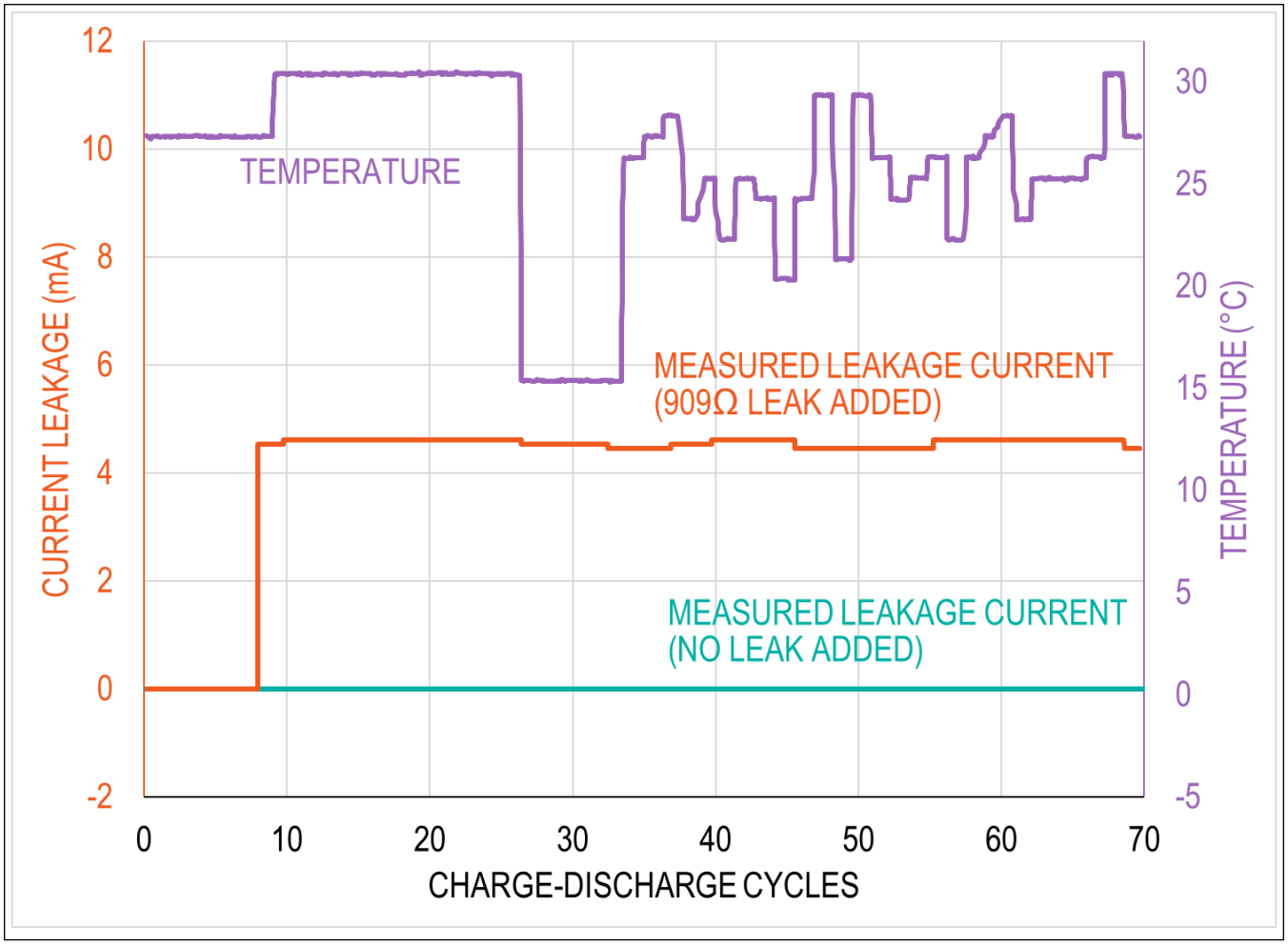


Figure 11. Example of Internal Self-Discharge with Temperature Variation

Configuring ISD

Contact Maxim Integrated for configuring the ISD Feature. See the *Battery Internal Self-Discharge Registers* section for configuration details.

Protector Thresholds

The MAX17332 provides a variety of programmable protector thresholds that are stored in nonvolatile memory. These thresholds include voltage, current, temperature, and timer delays.

Voltage Thresholds Pass

All voltage thresholds of the MAX17332 are shown graphically in Figure 9 and in table form with details of which bits and registers create the various thresholds in Table 6. The description of each register provides additional guidance for the selection of the register value.

Table 6. Voltage Thresholds

NAME	DESCRIPTION	CONFIGURATION REGISTERS	EXAMPLE
Permanent Fail Overvoltage	—	nOVPrtTh.OVPPermFail	4.4V
Overvoltage (with 7xJEITA)	Programmable overvoltage at each JEITA band. Programmable 10mV resolution from 3.9V to 4.88V. Programmable delay.	ChargeVoltage[temp] + nOVPrtTh.dOVP	{4.1V/ 4.20V/4.18/ 4.15V} +50mV
Overvoltage Release	Programmable release hysteresis	Overvoltage - nOVPrtTh.dOVPR	{4.15V/ 4.25V/ 4.23V/ 4.2V} -10mV
ChargeVoltage-Room	ChargingVoltage() output	nVChgCfg1.Room	4.20V
ChargeVoltage-Hot2	ChargingVoltage() output	nVChgCfg2.Hot2	4.115
ChargeVoltage-Hot1	ChargingVoltage() output	nVChgCfg2.Hot1	4.145V
ChargeVoltage-Warm	ChargingVoltage() output	nVChgCfg2.Warm	4.175V
ChargeVoltage-Cool	ChargingVoltage() output	nVChgCfg1.Cool	4.175
ChargeVoltage-Cold1	ChargingVoltage() output	nVChgCfg1.Cold1	4.145V
ChargeVoltage-Cold2	ChargingVoltage() output	nVChgCfg1.Cold2	4.115
DesignVoltage	Just for information, no action	nDesignVolt	3.7V
EmptyVoltage	For fuel gauge only (not related to protection)	nVEmpty	3.0V
Undervoltage Release	Charger applied	—	—
Under OCV Protection (SmartEmpty)	Programmable under-OCV 40mV steps UVP to UVP + 1.28V.	nUVPrtTh.UOCVP	3.2V
Undervoltage Protection	Programmable undervoltage 20mV steps 2.2V to 3.4V. Gauging and communications work until undervoltage shutdown	nUVPrtTh.UVP	2.7V
Undervoltage Shutdown	Gauging and communications work until undervoltage shutdown	nUVPrtTh.UVShdn	2.5V
Undervoltage Lockout	—	—	2.11V typ, 2.16V max
Low-Voltage Charging	—	—	1.8V
Zero-Voltage Charging	—	—	0.0V

Current Thresholds

All of the current thresholds of the MAX17332 are shown graphically in Figure 10 and in table form with details of each threshold in Table 7. The description of each register provides additional guidance for selection of the register value.

Table 7. Current Threshold Summary

CURRENT	ACTION	RELEASE	DETAILS
Overcharge Current (fast)	CHG off	Discharging or charger removal detection	Threshold 5-bit, 1.25mV steps to 38.75mV. Delay programmable 4-bit, 1ms to 15ms in 0.9ms steps.
Overcharge Current (slow with 4xJEITA)	CHG off		Programmable 0.4mV steps to 51.2mV. Delay programmable 351ms to 45s. Separate thresholds for 4 out of 6 JEITA segments.

Table 7. Current Threshold Summary (continued)

Overdischarge Current (fast)	DIS off	Charging or load removal detection	5-Bit, 2.5mV steps to 77.5mV. Delay programmable 4-bit, 1ms to 15ms in 0.9ms steps.
Overdischarge Current (slow)	DIS off		Programmable 0.4mV steps to 51.2mV. Delay programmable 351ms to 45s.
Short-Circuit Current	DIS off		5-Bit, 5mV steps to 155mV. Delay programmable 4-bit, 70µs steps to 985µs.
Charging Detected	Normal	—	Current > CurrDet or AvgCurrent > AvgCurrDet or PCKP > BATT + 0.15V to release overdischarge protection.
Discharging Detected	Normal	—	Current < -CurrDet or AvgCurrent < -AvgCurrDet or PCKP < BATT + 0.15V (falling-edge) indicates discharging. When discharging is detected, overcharge current faults release. Other charge faults such as OVP, OTP, and UTP remain set, however the CHG FET turns on to prevent the heat and voltage drop associated with the 0.6V CHG FET body diode. See the *Ideal Diode Behavior* section for more details. An OVP fault remains remembered (unreleased) until voltage falls and discharging is also detected.

Overcurrent Protection

The MAX17332 provides three levels of protection for overdischarge current events: fast, medium, and slow as shown in Figure 12. The MAX17332 also provides fast and slow levels of protection for overcharge current protection. The fast and medium levels of protection are provided by comparators and the slow levels are based on the ADC readings.

The MAX17332 maintains the protection until the source of the fault has been removed. Overcharge protection fault releases when pack voltage falls below BATT + 0.1V (edge, not level) while the IC tests charger removal by applying a 40kΩ pull down from PCKP to GND (during any charger fault). Overdischarge current (fast or slow) or short-circuit current protection faults release when PCKP rises above 1V, while the IC applies a 30µA source current test to PCKP.

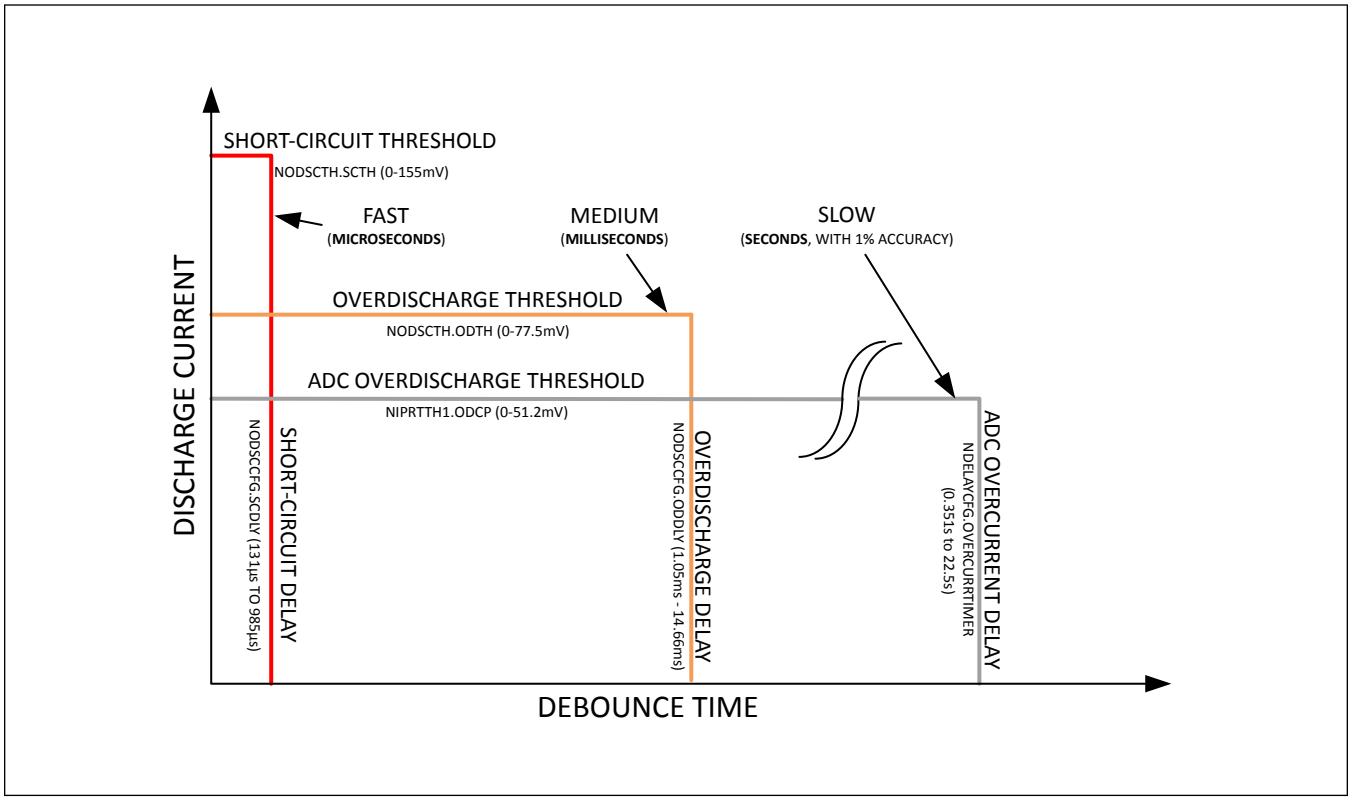


Figure 12. Fast, Medium, and Slow Overdischarge Protection

Fast Overcurrent Comparators

The MAX17332 contains three programmable fast overcurrent comparators called Overdischarge (OD), Short-Circuit (SC), and Overcharge (OC) that allow control protection for overdischarge current, short-circuit current, and overcharge current. These comparators have programmable threshold levels and programmable debounced delays. See Figure 13.

The OD comparator threshold can be programmed from 0mV to -77.5mV with 2.5mV resolution (0A to -7.75A with 0.25A resolution using 10mΩ sense resistor). The OC comparator threshold can be programmed from 0mV to 38.75mV with 1.25mV resolution (0A to 38.75A with 0.125A resolution using a 10mΩ sense resistor). The OD and OC comparators have a programmable delay from 1.05ms to 14.6ms with 0.97ms resolution. The SC comparator threshold can be programmed from 0mV to -155mV with 5mV resolution (0A to -15.5A with 0.5A resolution using a 10mΩ sense resistor) and has a programmable delay from 70µs to 985µs with a 61µs resolution.

The nODSCTh register sets the threshold levels where each comparator trips. The nODSCCfg register enables each comparator and sets their debounce delays. The nODSCCfg register also maintains indicator flags of which comparator has been tripped. These register settings are maintained in nonvolatile memory if the nNVCfg1.enODSC bit is set.

Slow Overcurrent Protection

The MAX17332 provides programmable thresholds for the slow overdischarge current protection (ODCP) and overcharge current protection (OCCP). ODCP and OCCP can be configured to provide different levels of protection across the nine temperature zones as shown in Figure 10.

Overcurrent Comparator Diagram

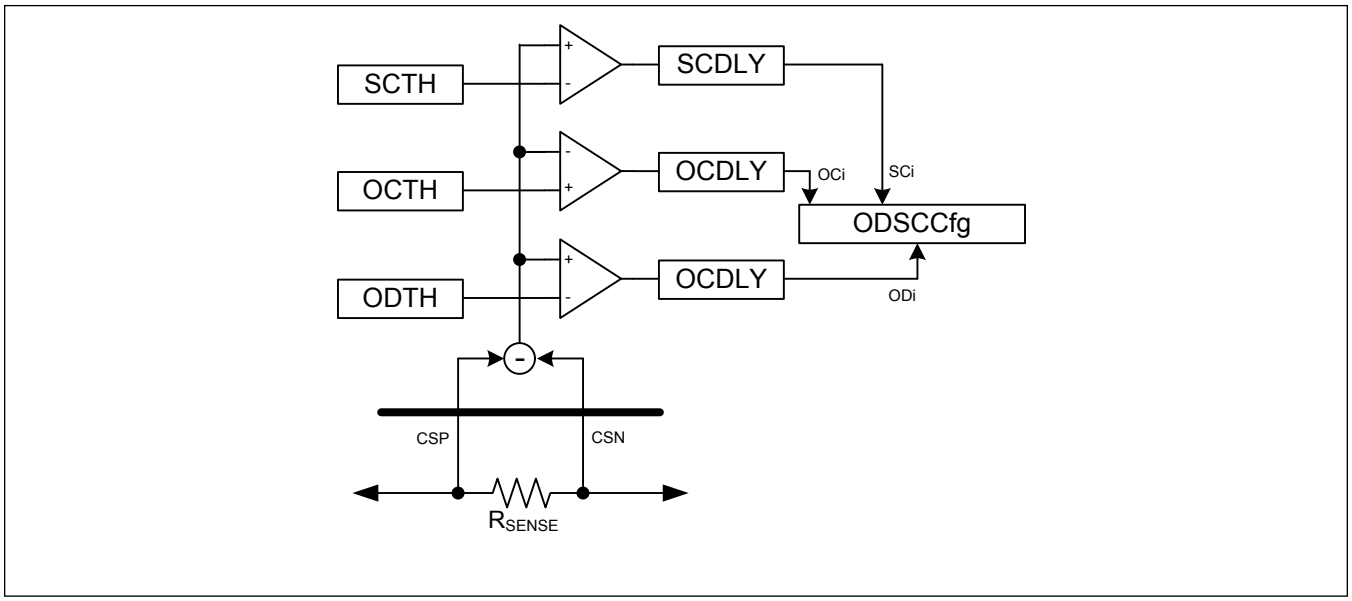


Figure 13. Overcurrent Comparator Diagram

Temperature Thresholds

The nine temperature zones shown in Figure 9 and Figure 10 can be configured in the nTPrtTh1 and nTPrtTh2 registers.

Other Thresholds

The MAX17332 also supports additional thresholds for suspending/releasing charge, detecting permanent failures of the charge and discharge FETs, and providing the recommended charging prescription as described in Table 8.

Table 8. Other Thresholds

THRESHOLD	ACTION	CONDITIONS
Charge Suspend	CHG off	FullDet Fault—if enabled (nProtCfg.FullEn) and charge termination criteria (see *ICHGTerm* and charge termination). ChgWDT Fault—if enabled (nProtCfg.ChgWDTEn) and communications timeout.
Charge-Suspend Release	Normal	FullDet Release—Discharge or charger removal detected. ChgWDT Release—Communications or discharge or charger removal detected.
Charge FET Failure	Blow fuse	CHG off yet charge-current persists (programmable).
Discharge FET Failure	Blow fuse	DIS off yet discharge-current persists (programmable).
Charge Voltage/Current "Prescription"	N/A	Nine-zone JEITA (four charge currents and voltages).

Permanent Failure

The IC supports several types of faults that result in a permanent failure. When any enabled permanent failure is detected, both FETs turn off and remain off regardless of power cycling. Upon permanent failure detection, the IC records the permanent failure status into nonvolatile nBattStatus. Furthermore, the PFAIL output drives high to either drive an external fuse or latch a secondary protector. This action is useful when FET failure is detected since charge and discharge can not be blocked in any other way.

The following permanent failure faults are supported whenever permanent failures are enabled (nProtCfg.PFEn = 1) and the condition persists longer than the Permanent Fail debounce timer (nDelayCfg.permFailTimer). When any permanent failure fault is detected, the nBattStatus.PermFail bit is set in addition to the specific fault bit (also in nBattStatus), and both FET drivers are put in the off state.

- **CHG/DIS FET open/short Failures:** Enable/disable this feature by configuring nProtCfg.FetPFEn.
  - **DIS FET Shorted:** If DIS = off and discharging is detected, nBattStatus.DFETFs is set and written to NVM.
  - **CHG FET Shorted:** If CHG = off and charging is detected, nBattStatus.CFETFs is set and written to NVM.
  - **FET Open Failure:** For either detection method below, the cause of an open can not be distinctly blamed on specifically either the CHG or DIS FET.
    - Detected By Discharge Fail: If DIS = On and PCKP = low and discharge current isn't detected, nBattStatus.FETFo is set and written to NVM.
    - Detected By Charge Fail**:** If CHG = On and DIS = On and PCKP > BATT + nOVPrtTh.ChgDetTh and charge current isn't detected, nBattStatus.FETFo is set and written to NVM.
- **Severe Over-Voltage Failure:** If VCell exceeds nOVPrtTh.OVPPermFail, nBattStatus.OVPF is set and written to NVM. Disable by configuring OVPPermFail to the maximum value of 5.12V (0xF8__).
- **Severe Over-Temperature Failure:** If Temp exceeds nTPrtTh3.TpermFailHot, nBattStatus.OTPF is set and written to NVM. Disable by configuring TpermFailHot to the maximum value of 125degC (0xF___).
- **Nonvolatile Protector Checksum Failure:** If enabled (nNVCfg1.enProtChkSum), during startup a checksum of the protector configuration is calculated and compared against the nChkSum register. If the value mismatches, nBattStatus.ChkSumF is set.

Disabling FETs by Pin-Control or I²C Command

The IC provides FET override control by either I²C command or pin command to the ALRT pin. This functionality can be useful for various types of applications:

- **Factory Testing:** Disconnecting the battery is useful for testing with a controlled external power supply.
- **Battery Selection:** In a multiple-battery system, one battery can be disconnected and another connected by

operating the FETs.

When allowed by nonvolatile configuration, both FETs can be turned off by pin control or either FET can be individually turned off by I²C command. The control operates as follows:

- **ALRT Pin Override:** Set nProtCfg.OvrdEn = 1 and drive ALRT low to force both FETs into the off state. Releasing the ALRT line recovers the FETs according to the protector's fault state machine.
- **I²C Command Override:** Set nProtCfg.CmOvrdEn = 1 and write CommStat.CHGOff or CommStat.DISOff to independently disable either the charge or discharge FET. Clearing CHGOff and DISOff recovers the FETs according to the protector's fault state machine.

These features can be disabled and locked by nonvolatile memory to prevent malicious code from blocking the FETs. Although disabling FETs does not produce any safety issues, it can be a nuisance if malicious system-side software denies power to the system.

Fuel Gauge

ModelGauge m5 EZ Algorithm

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated, causes the reported capacity error to increase over time, and requires periodic corrections. Corrections are usually performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true state-of-charge (SOC) based on the battery voltage after a long time of no current flow. Both have the same limitation; if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Voltage measurement-based SOC estimation has accuracy limitations due to imperfect cell modeling but does not accumulate offset error over time.

The IC includes an advanced voltage fuel gauge (VFG) which estimates OCV even during current flow and simulates the nonlinear internal dynamics of a Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC. This SOC estimation does not accumulate offset error over time. The IC performs a smart empty compensation algorithm that automatically compensates for the effect of temperature condition and load conditions to provide accurate state-of-charge information. The converge-to-empty function eliminates error toward an empty state. The IC learns battery capacity over time automatically to improve long-term performance. The age information of the battery is available in the output registers.

The ModelGauge m5 EZ algorithm combines a high-accuracy coulomb counter with a VFG. See Figure 14. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm weighs and combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, canceling the coulomb-counter drift.

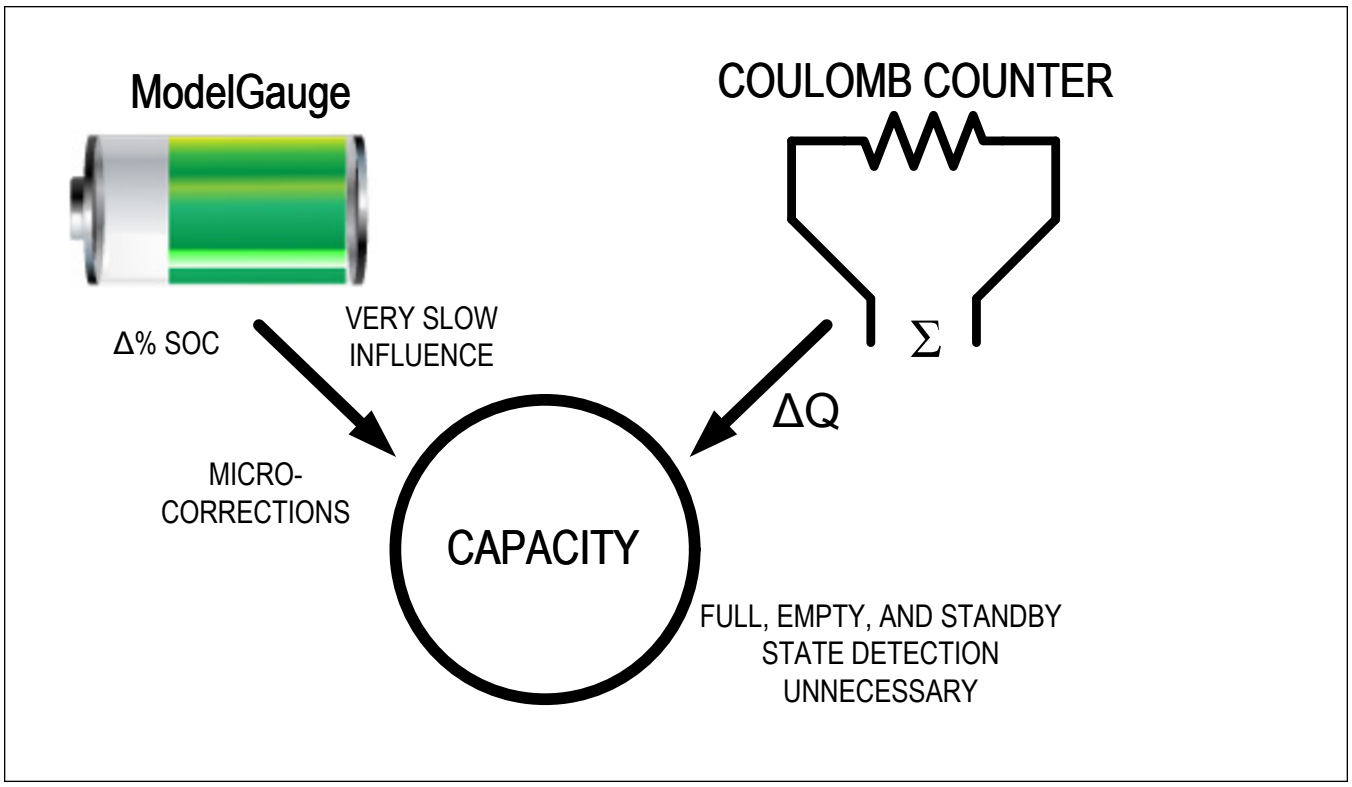


Figure 14. Merger of Coulomb Counter and Voltage Based Fuel Gauge

The ModelGauge m5 EZ algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. As the battery approaches the critical region near empty, the ModelGauge m5 EZ algorithm invokes a special error correction mechanism that eliminates any error.

The ModelGauge m5 EZ algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

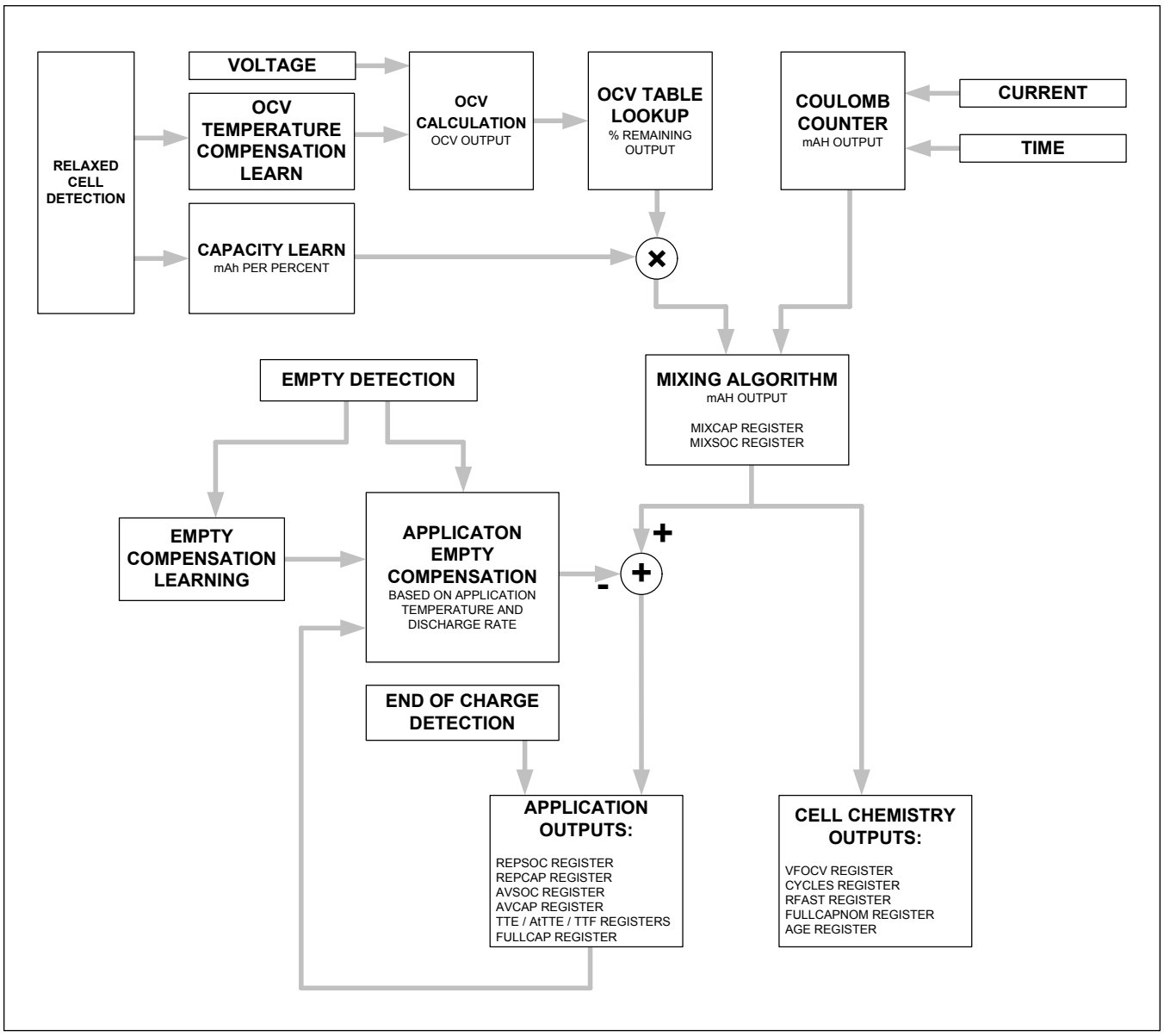


Figure 15. ModelGauge m5 EZ Block Diagram

Wakeup/Shutdown

Modes Of Operation

The MAX17332 supports six power modes (three active modes and three shutdown modes) as shown in Table 9 with descriptions of the features available in each mode, the typical current consumption of each mode, and the method to enter and exit each mode.

Table 9. Modes of Operation

MODE	SYMBOL	CONSUMPTION (TYPICAL) (µA)	DESCRIPTION
Active	IQ_A	35	Full Functionality. The Protection FETs, charge pump, and ADC are on. Tasks execute every 351ms.
Hibernate (optional)	IQ_H	21	FETs, charge pump, and ADC is on. Tasks execute every 1.4s. If enabled, the the device automatically enters and exits this mode depending on current measurements. Entering hibernate mode requires a low enough current for a long enough duration. Exiting requires just one high enough current event. For specific details regarding the thresholds, see the *nHibCfg* register definition.
Protected and Awake	IQ_P	11	ADC is on. The FETs and charge pump are disabled due to a protection fault, disconnecting the battery from the system. RAM is preserved and the gauge continues to monitor the battery. Firmware remains awake and ready to communicate or enable the battery. Firmware executes every 1.4s.
Ship*	IQ_S	11	Similar state as "Protected and Awake" except the firmware is responsive to wakeup events such as: charger connection, communications wakeup, or pushbutton wakeup (depending on which wakeups are enabled by configuration). Firmware executes every 1.4s.
		8	Similar state as "Protected and Awake" except the firmware is responsive to wakeup events such as: charger connection, communications wakeup, or pushbutton wakeup (depending on which wakeups are enabled by configuration). Firmware executes every 5.625s.
DeepShip1*	IQ_{DS}	0.5	FETs, charge pumps, ADC, and firmware are all placed into a shutdown state. The only activity alive relates to analog circuits that monitor for wakeup conditions (charger detection, communications, or pushbutton, depending on which are enabled).
DeepShip2*/ Undervoltage Shutdown	IQ_{UV}	0.5	FETs, charge pumps, ADC, firmware, and most wakeup circuits are powered down. Only the charger detection wakeup circuit remains powered in this mode to best conserve the small remaining battery capacity and prevent deep discharge.

**When an I²C SHIP command (setting Config.SHIP = 1) or I²C SCL/SDA lines collapse (and depending on whether COMMSH is enabled), the MAX17332 either enters Ship (if nProtCfg.DeepShpEn = 0) or DeepShip (if nProtCfg.DeepShpEn = 1) or DeepShip2 (if nProtCfg.DeepShp2En = 1) according to the configuration.*

Table 10. MAX17332 Ship Modes

	ENTER	WAKEUP	FUNCTIONALITY	nProtCfg. DeepShipEn	nProtCfg. DeepShip2En
8µA Ship	Config.SHIP or SDA-collapse	I²C, Pushbutton, or Charge Source	5.6s Measurements/ Updates	0	0
0.5µA DeepShip			No updates	1	0
0.5µA DeepShip2		Charge Source		1	1
0.5µA UVShdn	VCell < UVShdn			X	X

The MAX17332 can be awoken with a variety of methods depending on the configuration. If pushbutton wake-up

is enabled (nConfig.PBen = 1), then consistently pulling the ALRT/PIO pin low, either by pushbutton or system configuration, wakes up the device. A high-to-low transition on any of the communication lines wakes up the device. A consistent connection to a charge source wakes up the device.

The MAX17332 prevents accidental wakeup when the system is boxed and shipped. When awoken by any source, it debounces all wakeup sources (button, communications, and charger-detection) to ensure that the wakeup is valid. If no valid wakeup is discovered, the device returns to Ship or DeepShip.

The I_Q in the active, hibernate, and ship modes are impacted by the configuration of the IC. [[Recommended nHibCfg Settings and the Impact on I_Q]] shows the recommended configuration settings for the nConfig register and the impact those settings have on the I_Q of each mode. Note that when in hibernate mode, the protection for overtemperature and overvoltage is delayed by the nHibCfg.HibScalar value. It is not recommended to have hibernation enabled with the nHibCfg.HibScalar set to more than 1.4 seconds.

Table 11. Recommended nHibCfg Settings and the Impact on I_Q

AVAILABLE LOW POWER CONFIGURATION	nHibCfg	FETS-OFF	FETS-ON MODES	UPDATE RATE		NOTES
		SHIP I_Q (µA)	ACTIVE/ HIBERNATE I_Q (µA)	ACTIVE (s)	SHIP (s)	
1.4s Ship	0x0909	10	24/NA	0.351	1.4	—
1.4s Ship + Hibernate	0x8909	10	24/18	0.351	1.4	Overtemperature and overvoltage detection is delayed by 1.4s when in hibernate mode.
5.625s Ship	0x090B	7	24/NA	0.351	5.625	—

Power Mode Transition State Diagram

Figure 16 illustrates how the device transitions in and out of all of the possible power modes of operation of the device.

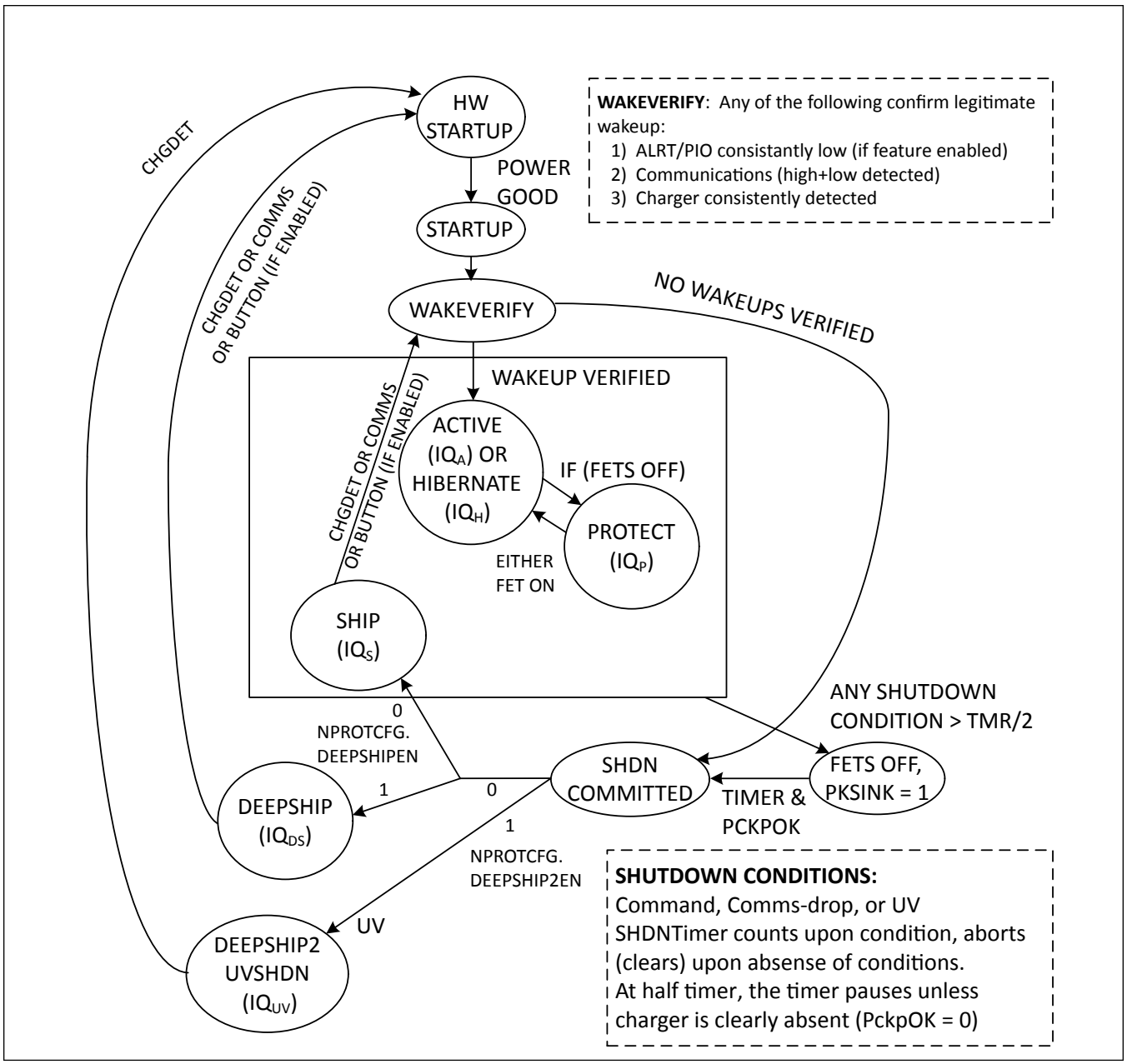


Figure 16. Power Mode Transition State Diagram

Pushbutton Wakeup

The ALRT/PIO pin can be used to wake up the device by enabling the pushbutton wakeup function by setting the nConfig.PBen. The pushbutton can be implemented in the system to wakeup the device and the system as shown in the *Pushbutton Schematic*.

Applications Information

Component Selection

MAX17332 has the following fixed components. These must remain the same in all designs. Voltage ratings listed are minimums. Higher ratings can be used, but should minimize derating on capacitors. The subscript denotes the pin name to which the component is connected. See the *Typical Application Schematic* for reference.

Table 12. MAX17332 Standard Components

COMPONENT	VALUE	MINIMUM RATING	NOTES
R_{BATT}	10Ω	—	Must match RC time with R_{PCKP}. Power rating should be sized with R_{ZVC}. If Zero-Volt charging is not used, use 1mA rating.
C_{BATT}	0.1µF	5V	Must match RC time with C_{PCKP}.
R_{PCKP}	1kΩ	—	Low Current. RC time matching is helpful for supplement mode detection.
C_{PCKP}	1nF	10V	This node can be exposed to higher voltage. A higher voltage capacitor can be used.
C_{CP}	0.1µF	10V	—
C_{REG2}	0.47µF	5V	—
R_{CHG}	5kΩ	—	—
C_{CHG}	22nF	—	—
R_{DIS}	1kΩ	—	Lower resistance can be used for faster DIS response. 0Ω is acceptable. Higher resistance increases FET Turn Off switching time.

Sense Resistor

Sense resistor selection is critical to MAX17332 operation. The charging and protection current range and resolution are defined by the sense resistor, as are the capacity range and resolution. Table 13 provides guidance for regulation current ranges based on the sense resistor. A current range should be selected for the Constant Current regulation. Termination Current being below the charge current range is allowed. For managed DC-DC applications, the heat generated in the CHG/DIS FETs is significantly less, and smaller sense resistors and larger currents are allowed. For applications with fixed DC voltage input, and larger thermal budget, larger currents than the listed range are allowed, see *nIChgCfg1/2 Registers* for the maximum current range. For fixed DC applications, at low cell voltage, the MAX17332 can regulate in Constant Power mode until the cell voltage is high enough to enter CC mode. See Table 19 for heat limits.

Table 13. Sense Resistor Selection

CHARGE SOURCE	R_{SENSE} (mΩ)	CHARGE CURRENT RANGE (mA)
Managed DC-DC or Switching Charger	2	1850—17500
Managed DC-DC or Switching Charger	5	740—7000
Managed DC-DC or Switching Charger	10	185—3500
5V or USB	10	185—2331
5V or USB	20	92.5—1166
5V or USB	50	37—466
5V or USB	100	18.5—233
5V or USB	200	9.25—117
5V or USB	500	3.7—47

Charging and Protection FETs

After sense resistor selection, FET selection is the the next critical component choice for system design. The MAX17332 uses a voltage doubler charge pump as the input to the FET drivers. With this design, V_{GS} for the CHG FET is always equal to V_{Cell}. The FET V_{TH} must be low to allow it to turn on and regulate the FET from a low battery. V_{TH} < 2V is

recommended.

V_{DS} for the CHG FET (or V_{SS} for dual FETs) must be set based on the application requirements. For pack side applicaiton with removable batteries, 12V is recommended and 20V is optional. For implementations where the battery is captive, or MAX17332 is installed on the system board, lower V_{DS} (or V_{SS}) is allowed but must meet the maximum charge source voltage.

Power Dissipation is a critical function since the MAX17332 operates the FET in the Ohmic/Linear region. For FETs with lower power dissipation, the HeatLim of MAX17332 reduces charging current to keep the FET in the safe operating range. Good thermal rated FETs and PCB design is needed for maximum charging current.

R_{DSON} and package size can be other considerations for application purposes. They are not critical for MAX17332 operation.

ESD and Optional Components

Thermistors are optional, but recommended components on the MAX17332. See the *nPackCFG.THCfg* register subfield for details on how thermistors are used by the MAX17332. Table 104 lists common NTC thermistors with their associated Beta value and the nThermCfg value. Other thermistors can be used with the formula listed in Table 104, or by contacting Maxim Integrated.

The Typical Application Schematic shows series resistors and Zener diodes on the ALRT, SDA, and SCL pins. For applications where these pins are exposed, adding some ESD protection is necessary. TVS diodes can be used instead of Zener diodes for stronger protection. 150Ω resistors have been tested with 4.7V Zener diodes to withstand ±8kV contact and ±16kV air discharge without damage to the IC. These components can be omitted for applications where the MAX17332 is installed on the system board.

In application using multiple protection ICs where the secondary protector is connected between MAX17332 and the cell, R_{ZVC} must be populated. If the secondary protector blocks Zero-Volt charging, R_{ZVC} doesn't need an exact calculation and only provides current to wake the secondary protector if it is in a protected or shutdown state (use 100Ω for this application). For Zero-Volt charging, R_{ZVC} is calculated with the formula in the Zero-Volt Charging section. For applications with only the MAX17332 as the protector and no Zero-Volt charging, do not connect R_{ZVC}.

Register Description Conventions

The following sections define standard conventions used throughout the data sheet to describe register functions and device behavior. Any register that does not match one of the following data formats is described as a special register.

Standard Register Formats

Unless otherwise stated during a given register's description, all IC registers follow the same format depending on the type of register. See Table 14 for the resolution and range of any register described hereafter. Note that current and capacity values are displayed as a voltage and must be divided by the sense resistor to determine amps or amp-hours. It is strongly recommended to use the lower byte of nRSense (19Ch) register to store the sense resistor value for use by the host software.

Table 14. ModelGauge Register Standard Resolutions

REGISTER TYPE	LSB SIZE	MINIMUM VALUE	MAXIMUM VALUE	NOTES
Capacity	5.0µVh/ R_{SENSE}	0µVh	327.675mVh/ R_{SENSE}	Equivalent to 0.5mAh with a 10mΩ sense resistor.
Percentage	1/256%	0%	255.9961%	1% LSb when reading only the upper byte.
Voltage	78.125µV	0V	5.11992V	—
Current	1.5625µV/ R_{SENSE}	-51.2mV/ R_{SENSE}	51.1984mV/ R_{SENSE}	Signed 2's complement format. Equivalent to 156.25µA with a 10mΩ sense resistor.
Temperature	1/256°C	-128°C	127.996°C	Signed 2's complement format. 1°C LSb when reading only the upper byte.
Resistance	1/4096Ω	0Ω	15.99976Ω	—
Time	5.625s	0s	102.3984hr	—

Table 14. ModelGauge Register Standard Resolutions (continued)

REGISTER TYPE	LSB SIZE	MINIMUM VALUE	MAXIMUM VALUE	NOTES
Power	$8mW/R_{SENSE}$	$-262W/R_{SENSE}$	$262W/R_{SENSE}$	Signed 2's complement format. Equivalent to 0.8mW with a 10mΩ sense resistor.
Special	—	—	—	Format details are included with the register description.

Device Reset

Device reset refers to any condition that would cause the IC to recall nonvolatile memory into RAM locations and restart operation of the fuel gauge. Device reset refers to initial power up of the IC, temporary power loss, or reset through the software power-on-reset command.

Nonvolatile Backup and Initial Value

All configuration register locations have nonvolatile memory backup that can be enabled with control bits in the nNVCfg0, nNVCfg1, and nNVCfg2 registers. If enabled, these registers are initialized to their corresponding nonvolatile register value after device reset. If nonvolatile backup is disabled, the register restores to an alternate initial value instead. See each register description for details.

Register Naming Conventions

Register addresses are described throughout the document as 9-bit internal values from 000h to 1FFh. These addresses must be translated to 8-bit external slave address and 8-bit register address. A leading '0' indicates the primary slave address (0x6C by default) should be used to read this register and a leading '1' indicates the secondary slave address (default 0x16) should be used to read this register. See the *Memory* section for details.

Register names that start with a lowercase 'n', such as nPackCfg for example, indicate that the register is a nonvolatile memory location. Register names that start with a lower case 's' indicate the register is part of the SBS compliant register block.

Charging Registers

Charging Status and Configuration Registers

ChgStat Register (0A3h)

Register Type: Special

The ChgStat register shown in Table 15 indicates the charger control mode.

Table 15. ChgStat (0A3h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Dropout	x	x	x	x	x	x	x	x		x	x	CP	CT	CC	CV

CC: Constant Current mode. Charging is controlled by ChargingCurrent register.

CV: Constant Voltage mode. Charging is controlled by ChargingVoltage register.

CP: Heat Limit. If the Pack+ voltage is adjustable, decrease the voltage to exit CP mode to increase charging speed.

CT: FET Temperature limit. If the Pack+ voltage is adjustable, decrease the voltage to decrease FET temperature and increase charging speed.

Dropout: Dropout Saturation Prevention. An alert is also generated on Status.CA whenever dropout is detected. If PACK+ voltage is adjustable, the application processor should increase the voltage to increase charging speed.

When charging directly from USB, the MAX17332 attempts to charge at the current indicated in ChargingCurrent. If this exceeds the current limit of the USB charger, the USB output voltage drops and the MAX17332 enters Dropout mode. The USB output voltage increases as a function of the cell voltage and the dropout voltage until the battery reaches CV mode. The USB output voltage returns back to regulation as the battery current tapers closer to the termination current.

nChgCfg0 Register (1C2h)

Type: Special

The nChgCfg0 register is shown in Table 16 and sets the Prequal voltage and current, and Minimum System voltage.

Table 16. nChgCfg0 Register (1C2h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CVStepDis	BackupEn	0	PreQualVolt				VSysMin			PrechgCurr					

CVStepDis: Disable Constant Voltage Step. The Charging Current steps from one constant current step to the next constant current step as defined in *nStepCurr*. When CVStepDis = 0 enabled, there is a constant voltage step between each constant current step as described in the *Step-Charging* section. Set CVStepDis = 1 to disable the constant voltage step between each charging step.

BackupEn: Backup-Battery Applicaton Mode. Set BackupEn = 1 to enabled Backup-Battery application mode. In Backup-Battery Application mode, the MAX17332 prevents discharging until the main battery voltage (measured at PCKP of the backup MAX17332) drops 0.6V below the backup-battery voltage (measured at BATT of the backup MAX17332).

PreQualVolt: Sets the prequal voltage. Prequal Voltage = UVP + PreQualVolt x 20mV, PreQualVolt has a range of UVP to UVP + 300mV.

PreChgCurr: Sets the precharging current for the ChargingCurrent register. Precharge current is calculated as:

PreChargeCurrent = nIChgCfg1.RoomChargingCurrent x ((1 + PreChgCurr)/256) rounded to the nearest QScale with a range from RoomChargingCurrent/256 to RoomChargingCurrent/4.

VSysMin: If the charge source is overloaded and is not able to hold the output voltage, Minimum System Voltage increases PACK+ voltage by keeping the DIS FET Off until cell voltage reaches VSysMin. The system minimum voltage is relative to Vempty and can be configured from Vempty + 0.2V to Vempty - 0.4V in 100mV steps. The recommended setting for VSysMin is 3.4V or lower, as this generates extra heat during charging. Set to 0 to disable this feature.

Table 17. VSysMin Settings

SETTING	VSysMin VALUE
0	Disabled
1	VEmpty + 0.2V
2	VEmpty + 0.1V
3	VEmpty
4	VEmpty - 0.1V
5	VEmpty - 0.2V
6	VEmpty - 0.3V
7	VEmpty - 0.4V

nChgCfg1 Register (1CBh)

Type: Special

The nChgCfg1 register is shown in Table 18 and sets the heat and temperature parameters for the charger.

Table 18. nChgCfg1 (1CBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HeatLim							FetLim				FetTheta				

HeatLim: Set HeatLim to limit the thermal dissipation in the protection FETs during prequal regulation. Set HeatLim from 25.5mW to 3264mW in 25.5mW steps according to 10mΩ R_{SENSE} (Heat = I x V). The effective power-dissipation limit is (HeatLim) x 25.5mW. See Table 19 for other sense resistors.

Table 19. HeatLim Range and Resolution for Different Sense Resistors

SENSE RESISTOR (mΩ)	MIN (mW)	MAX (mW)	STEP (mW)

Table 19. HeatLim Range and Resolution for Different Sense Resistors (continued)

5	51	6528	51
10	25.5	3264	25.5
20	12.75	1632	12.75
50	5.1	652.8	5.1
100	2.55	326.4	2.55
200	1.275	163.2	1.275

FetTheta: FetTheta is used to calculate actual Junction temp with only observing DieTemp and Thermistor 2 during charging. FET Junction temperature is calculated with the following equation:

FETTemp = TH2_Temp+ (TH2_Temp - DieTemp) x FetTheta.

The FetTheta configuration range is 0 to 3.875 with 0.125 steps. FetTheta is a scalar and does not have units. If PFail pin is used, or Thermistor 2 is not used, DieTemp is used as FET temperature.

FETLim: Set FET Lim to limit FET temperature during charging. The range is 75°C to 135°C with a 4°C lsb.

nChgCfg2 Register (1E4h)

Register Type: Special

The nChgCfg2 register configures the noiseless filter, relax enable and charge restart threshold. The default factory setting for nChgCfg2 is 0x1800. Table 20 shows the register format.

Table 20. nChgCfg2 Register (0x1E4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RechgThr		0	1	1	0	0	0	0	0	0	0	0	0	0	0

RechgThr: Charge Restart Threshold. Full is released when VFOCV is less than (VFOCVFull - (RechgThr+1) x 0.010V) providing charger restart thresholds of 10mV, 20mV, 30mV, and 40mV. VFOCVFull is the VFOCV value recorded at the end-of-charge.

Charging Configuration Registers

The ChargingVoltage and ChargingCurrent display the calculated target charge voltage and current. This includes the programmed charging voltage and current, charging modifications according to battery temperature, and step-charging.

ChargingVoltage Register (02Ah)

Register Type: Voltage

Nonvolatile Backup: None

The ChargingVoltage register reports the target charging voltage. This register is automatically updated by the IC based on temperature region and charging step. However, manual control of the charging voltage can be enabled by setting Config.ManChg = 1 where the host can directly write the desired charging voltage to the ChargingVoltage Register.

ChargingCurrent Register (028h)

Register Type: Current

Nonvolatile Backup: None

The ChargingCurrent register reports the target charging current. This register is automatically updated by the IC based on temperature region and charging step. However, manual control of the charging current can be enabled by setting Config.ManChg = 1 where the host can directly write the desired charging current to the ChargingCurrent Register.

nIChgTerm Register (1C1h)

Register Type: Current

Nonvolatile Restore: IChgTerm (0E1h) if nNVCfg0.enICT is set

Alternate Initial Value: 1/3rd the value of the nFullCapNom register (corresponds to C/9.6)

The nIChgTerm register allows the device to detect when a charge cycle of the cell has completed. nIChgTerm should be programmed to the exact charge termination current used in the application. The device detects end-of-charge if all the following conditions are met:

• VFOCV > FullOCVThr

• Current < IChgTerm

• AvgCurrent < IChgTerm

• FullTimer Expired

See the *End-of-Charge* section for more details.

nVChgCfg1 Register (1CCh) and nVChgCfg2 Register (1CDh)

The nVChgCfg1 and nVChgCfg2 registers shown in Table 21 and Table 22, sets the JEITA charge voltage configuration for the MAX17332. The JEITA charge voltage is used to calculate the Charging Voltage register and is used to determine the overvoltage-protection threshold.

nDesignCap.VScale determines the center voltage for RoomChargeVoltage (4.2V or 3.7V) and the step size (5mV or 10mV). The additional charge voltages are set relative to the RoomChargeVoltage based on the temperature.

To disable the temperature dependence and create a flat charging voltage across the temperature range, set RoomChargeVoltage as desired and configure the other settings with a value of 0x0.

Table 21. nVChgCfg1 Register (1CCh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WarmChargeVolt				RoomChargeVolt								CoolChargeVolt			

Table 22. nVChgCfg2 Register (1CDh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Hot2ChargeVolt				Hot1ChargeVolt				Cold1ChargeVolt				Cold2ChargeVolt			

RoomChargeVolt: Sets the nominal room-temperature charging voltage in the room temperature region and step 4 (Highest charging voltage) as shown in Figure 9. RoomChargeVoltage is a signed value. nDesignCap.VScale determines the Center Voltage (CV) and the step size.

nDesignCap.VScale = 0 --> CenterVoltage = 4.2V, StepSize = 5mV

nDesignCap.VScale = 1 --> CenterVoltage = 3.7V, StepSize = 10mV

The charging voltage for each temperature region is calculated as:

RoomChgVolt = CV + (RoomChargeVolt x StepSize)

WarmChgVolt = CV + ((RoomChargeVolt - WarmChargeVolt) x StepSize)

Hot1ChgVolt = CV + ((RoomChargeVolt - WarmChargeVolt - Hot1ChargeVolt) x StepSize)

Hot2ChgVolt = CV + ((RoomChargeVolt- WarmChargeVolt - Hot1ChargeVolt - Hot2ChargeVolt) x StepSize)

CoolChgVolt = CV + ((RoomChargeVolt - CoolChargeVolt) x StepSize)

Cold1ChgVolt = CV + ((RoomChargeVolt - CoolChargeVolt - Cold1ChargeVolt) x StepSize)

Cold2ChgVolt = CV + ((RoomChargeVolt - CoolChargeVolt - Cold1ChargeVolt - Cold2ChargeVolt) x StepSize)

nIChgCfg1 Register (1CEh) and nIChgCfg2 Register (1CFh)

The nIChgCfg1 and nIChgCfg2 registers shown in Table 23 and Table 24 sets the highest charging current across the temperature zones shown in Figure 10. Each charging current is scaled by the nDesignCap.QScale value.

To disable the temperature dependence and create a flat charging current across the temperature range, set RoomChargeCurr as desired and set the other thresholds with a value of 0.

Table 23. nIChgCfg1 Register (1CEh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WarmChargeCurr					RoomChargeCurr						CoolChargeCurr				

Table 24. nIChgCfg2 Register (1CFh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Hot2ChargeCurr				Hot1ChargeCurr				Cold1ChargeCurr				Cold2ChargeCurr			

nDesignCap.QScale determines the step size as shown in *nDesignCap* section.

The charging current at each temperature region and StepCurr0 (highest charging current) is calculated as follows:

RoomChgCurr = (RoomChargeCurr +1) x StepSize

WarmChgCurr = (RoomChargeCurr + 1 - WarmChargeCurr) x StepSize

Hot1ChgCurr = (RoomChargeCurr + 1 - WarmChargeCurr - Hot1ChargeCurr) x StepSize

Hot2ChgCurr = (RoomChargeCurr + 1 - WarmChargeCurr - Hot1ChargeCurr - Hot2ChargeCurr) x StepSize

CoolChgCurr = (RoomChargeCurr + 1 - CoolChargeCurr) x StepSize

Cold1ChgCurr = (RoomChargeCurr + 1 - CoolChargeCurr - Cold1ChargeCurr) x StepSize

Cold2ChgCurr = (RoomChargeCurr + 1 - CoolChargeCurr - Cold1ChargeCurr - Cold2ChargeCurr) x StepSize

nStepCurr Register (1C4h) and nStepVolt Register (1C5h)

The nStepCurr and nStepVolt registers shown in Table 25 and Table 26 define the step-charging prescription as shown in Figure 2.

To disable step-charging completely, set nStepCurr = 0000h and nStepVolt = 0000h. Additionally, any step can be disabled by setting the associated nibbles to 0.

Charging begins with Step 0 (StepCurr0 is the highest charging current, and StepVolt0 is the lowest charging voltage). As the cell voltage progresses towards the full voltage, the stages advance to Step 4 (Step 0->1->2->3->4). The current at each step moves from highest current to lowest current and the charge voltage increases to the highest charging voltage.

Table 25. nStepCurr Register (1C4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
StepCurr4				StepCurr3				StepCurr2				StepCurr1			

The step size of StepCurr1 is double the nDesignCap.QScale value. The step size of StepCurr2/3/4 is the nDesignCap.QScale value.

The charginge current at each step is calculated as follows:

ChargingCurrent[Step0][Room] = (RoomChargeCurr + 1) x Qscale //(Highest Current)

ChargingCurrent[Step1][Room] = (RoomChargeCurr + 1 - StepCurr1 x 2) x Qscale

ChargingCurrent[Step2][Room] = (RoomChargeCurr + 1 - StepCurr1 x 2 - StepCurr2) x Qscale

ChargingCurrent[Step3][Room] = (RoomChargeCurr + 1 - StepCurr1 x 2 - StepCurr2 - StepCurr3) x Qscale

ChargingCurrent[Step4][Room] = (RoomChargeCurr + 1 - StepCurr1 x 2 - StepCurr2 - StepCurr3 - StepCurr4) x Qscale

Table 26. nStepVolt Register (1C5h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
StepVolt0				StepVolt1				StepVolt2				StepVolt3			

The step size of each voltage step and the CenterVoltage (CV) is defined by the nDesignCap.VScale value.

The charging voltage at each step is calculated as follows:

ChargingVoltage[Step0][Room] = CV + ((RoomChargeVolt - StepVolt3 -StepVolt2 - StepVolt1 - StepVolt0) x Vscale)

ChargingVoltage[Step1][Room] = CV + ((RoomChargeVolt - StepVolt3 -StepVolt2 - StepVolt1) x Vscale)

ChargingVoltage[Step2][Room] = CV + ((RoomChargeVolt - StepVolt3 -StepVolt2) x Vscale)

ChargingVoltage[Step3][Room] = CV + ((RoomChargeVolt - StepVolt3) x Vscale)

ChargingVoltage[Step4][Room] = CV + (RoomChargeVolt x Vscale) //(Highest Voltage)

nFullCfg Register (0x1B5h)

Factory Default Value: 0785h

The nFullCfg register shown in Table 27 sets full OCV threshold which gates detection of end-of-charge (charge termination and RepSOC = 100%) and charger restart.

Charge termination and full detection occur when all of the following conditions are met:

• VFOCV > FullOCVThr

• Current < IChgTerm

• AvgCurrent < IChgTerm

• FullTimer Expired

See the *nIChgTerm* register description and the *End-Of-Charge Detection* section for details. Additionally, the charger restarts if the open circuit voltage falls nChgCfg2.RechgTh below the VFOCV at end-of-charge.

The recommended nFullCfg.FullOCV register setting for most custom characterized applications is 50mV below the charge voltage (nFullCfg = 0x0275). For EZ Performance without characterization, the recommendation is to essentially disable the feature by setting to 150mV below ChargingVoltage (nFullCfg = 0x0785).

Table 27. nFullCfg Register (0x1B5h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				FullOCV									1	0	1

FullOCV: FullOCV Threshold is relative to Step 4 ChargingVoltage at the present temperature range. FullOCV is a positive number with 0.625mV resolution and 320mV range. It is translated to a negative offset relative to ChargeVoltage. FullOCV Threshold is calculated as follows:

FullOCVThreshold = nVChgCfg1/2.ChargingVoltage[Temperature] - ((FullOCV + 1) x 0.625mV)

nAgeChgCfg Register (0x1B9h)

Factory Default Value: 0000h

The nAgeChgCfg register shown in Table 28 configures the Age-based derating of the charging voltage and charging current.

Table 28. nAgeChgCfg Register (0x1B9h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
End		ndCurrAge				ndVAge				ndCycles				Begin	

Begin: Delay to Begin Age Derating. Begin defines how many ndCycles count to delay before ChargingVoltage and ChargingCurrent derating begins.

Example: Begin = 2, ndCycles = 50, ChargingVoltage and ChargingCurrent start to derate after 2x50 = 100 Cycles. Then ChargingVoltage and ChargingCurrent follows:

ChargingVoltage = ChargingVoltage - ndVAge x int[max((Cycles/ndCycles)- Begin, 0)]

ChargingCurrent = ChargingCurrent - (ndCurrAge x QScale)/2 x int[max((Cycles/ndCycles)- Begin, 0)]

End: End defines the derating steps before reaching the final ChargingVoltage ad ChargingCurrent.

FinalStage = int((End + 4) x 4) >> int(log_2 (ndVAge/5))

Cycles FinalStage = FinalStage x ndCycles

ChargingVoltage FinalStage = FinalStage x ndVAge

ChargingCurrent FinalStage = FinalStage x ndCurrAge x QScale/2

Final ChargingV = ChargingV(Temp, Step) - FinalStage x ndVAge Final ChargingC = ChargingC(Temp, Step) - FinalStage x ndCurrAge x QScale/2

ndVAge: Defines the voltage derating rate. Range 5mV to 75m, step is 5mV. 0 disables Age Derating feature (even though ndCurrAge is not zero.).

ndCurrAge: Defines the current derating rate. (0 - 15 x Qscale) step is 1 x Qscale (Qscale is set to be 3 by default which means the current step size is 20x(10/RSense) (See the Table 70). This can also be read in the nDesignCap regiser, D3: VScale, D2-D0: QScale)

ndCycles: Derating cycle steps of the voltage and current. Based on nNVCfg2.FibScl setting there are different options for ndCycles:

nNVCfg2.FibScl	ndCycles SETTING
0	[12.5,25,37.5,…200]
1	[25,50,…400]
2	[50,100..800]
3	[100,200…1600]

Final Equation:

Finally, the voltage and current derate are based on the following two equations:

ChargingCurrent = ChargingCurrent - (ndCurrAge x QScale)/2 x int[max((Cycles/ndCycles)- Begin, 0)]

ChargingVoltage = ChargingVoltage - ndVAge x int[max((Cycles/ndCycles)- Begin, 0)]

Therefore the final Voltage and Current derating curve is a step function.

An Example of Calculating End:

ndCycles = 50, ndVAge = 35mV, End = 2, dnCurrAge = 1 QScale.

int(log_2 (ndVAge/5)) = int(log_2 (35/5)) = 2

FinalStage = int((End + 4) \times 4) >> 2 = 6

ChargingVoltage and ChargingCurrent derate every ndCycles by the value of ndVage and ndCurrAge respectively. In total FinalStage (6 in this example) steps.

So after 6x5 = 300 cycles, ChargingVoltage and ChargingCurrent stop derating and

Final ChargingV = ChargingV(Temp, Step) - FinalStage x ndVAge Final ChargingC = ChargingC(Temp, Step) - FinalStage x ndCurrAge x QScale/2

Protection Registers

Voltage Protection Registers

nUVPrtTh Register (1D0h)

Register Type: Special

The nUVPrtTh register shown in Table 29 sets undervoltage protection, deep-discharge-state protection, and undervoltage-shutdown thresholds.

Table 29. nUVPrtTh Register (1D0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
UVP						DisUVP	UOCVP					UVShdn			

UVP: UnderVoltage Protection Threshold. The MAX17332 opens the discharge FET when VCell < UVP. UVP can be configured from 2.2V to 3.46V in 20mV steps. UVP is unsigned.

DisUVP: Disable UVP. Set DisUVP = 1 to disable undervoltage protection threshold only. UOCVP and UVShdn still function normally. The DisUVP feature allows the application to continue to run down to the 2.16V minimum voltage of the IC.

UOCVP: Under Open Circuit Voltage Protection Threshold (also referred to as SmartEmpty). The MAX17332 opens the discharge FET when VFOCV < UOCVP. UOCVP is relative to UVP and can be configured from UVP to UVP + 1.28V in 40mV steps. Set UOCVP=0 to disable.

UVShdn: UnderVoltage Shutdown Threshold. The MAX17332 shutdowns when VCell < UVShdn. UVShdn is relative to UVP and can be configured from UVP - 0.32V to UVP + 0.28V in 40mV steps. Note that this is a signed value and UVShdn should be configured as a 2's compliment negative value so that UVShdn < UVP.

nOVPrtTh Register (1DAh)

Factory Default Value: B354h

The nOVPrtTh register shown in Table 30 sets the permanent overvoltage protection threshold, the charge-detection threshold, the overvoltage-protection threshold, and the overvoltage-protection-release threshold. dOVP and dOVPR are relative to the Charge Voltage that is set in the nVChgCfg register and has a 10mV resolution.

Table 30. nOVPrtTh Register (1DAh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OVPPermFail					dOVP					dOVPR					

dOVP: Delta from ChargeVoltage to Overvoltage Protection. dOVP sets JEITA overvoltage protection relative to ChargeVoltage (see *nVChgCfg1/2*). If nNVCfg1.enJP is disabled, then OVP voltage is calculated from RoomChargeV across all temperature zones. This is a positive number with 5mV resolution and 155mV range. Overvoltage protection is calculated as:

OVP = ChargeVoltage + dOVP x 5mV

dOVPR: Delta from Overvoltage Protection to the Overvoltage-Release Threshold. dOVPR sets overvoltage-protection release relative to the overvoltage-protection setting. This is a positive number with 5mV resolution and is translated to a negative offset relative to OVP. Overvoltage-protection release is calculated as:

OVPR = OVP - dOVPR x 5mV

OVPPermFail: Permanent Failure OVP (permanent overvoltage protection) Threshold. Permanent failure overvoltage protection occurs when any cell voltage register reading exceeds this value. The OVPPermFail range is $OVP\_threshold_{Room}$ + 40mV to $OVP\_threshold_{Room}$ + 195mV with a 5 mV lsb.

If nOVPrtTh.D15 = 1: $OVP\_PermFail\_Threshold = OVP_{Room}$ + 40mV + (OVPPermFail(Bits D15-D11) x 5mV) If nOVPrtTh.D15 = 0: $OVP\_PermFail\_Threshold = OVP_{Room}$ + 40mV + (OVPPermFail(Bits D15-D12 Only) x 10mV)

Current Protection Registers

nODSCTh Register (1DDh)

Factory Default Value: 0EAFh

The nODSCTh register sets the current thresholds for each overcurrent alert. The format of the registers is shown in Table 31.

Table 31. nODSCTh Register (1DDh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OCTH						SCTH					ODTH				

SCTH: Short-Circuit Threshold Setting. Sets the short-circuit threshold to a value between 0mV and -158.72mV with a step size of -5.12mV. The SCTH bits are stored such that 0x1F = 0mV and 0x00 = -158.72mV. The short-circuit threshold is calculated as -158.72mV + (SCTH x 5.12mV).

ODTH: Overdischarge Threshold Setting. Sets the overdischarge threshold to a value between 0mV and -38.75mV with a step size of -1.25mV. The ODTH bits are stored such that 0x1F = 0mV and 0x00 = -38.75mV. The overdischarge threshold is calculated as -38.75mV + (ODTH x 1.25mV).

OCTH: Overcharge Threshold Setting. Sets the overcharge threshold to a value between 0mV and 39.375mV with a step size of 0.625mV. The OCTH bits are stored such that 0x3F = 0mV and 0x00 = 39.375mV. The overcharge threshold

is calculated as 39.375mV - (OCTH x 0.625mV). The MAX17332 internally overwrites this OCTH setting to a level slightly above the Charging Current in order to quickly react to transient loads while charging.

Table 32 shows sample values of calculated thresholds in millivolts for OCTH, SCTh, and ODTH. Equivalent current thresholds are shown assuming a 10mΩ sense resistor.

Table 32. OCTH, SCTh, and ODTH Sample Values

	OCTH		SCTH		ODTH	
0x00	39.375mV	3.9375A	-158.72mV	-15.872A	-38.75mV	-3.875A
0x01	38.75mV	3.875A	-153.6mV	-15.36A	-37.5mV	-3.75A
0x02	38.125mV	3.8125A	-148.8mV	-14.848A	-36.25mV	-3.625A
0x04	36.875mV	3.6875A	-138.24mV	-13.824A	-33.75mV	-3.375A
0x08	34.735mV	3.4735A	-117.76mV	-11.776A	-28.75mV	-2.875A
0x10	29.375mV	2.9375A	-76.8mV	-7.68A	-18.75mV	-1.875A
0x14	26.875mV	2.6875A	-56.32mV	-5.632A	-13.75mV	-1.375A
0x18	24.375mV	2.4375A	-35.84mV	-3.584A	-8.75mV	-0.875A
0x1E	20.625mV	2.0625A	-5.12mV	-0.512A	-1.25mV	0.125A
0x1F	20mV	2A	0mV	0.00A	0.0mV	0.00A
0x2F	10mV	1A	—	—	—	—
0x3F	0mV	0A	—	—	—	—

nODSCCfg Register (1DEh)

Factory Default Value: 0x4355

The nODSCCfg register configures the delay behavior for the short-circuit, over-discharge-current, and over-charge-current comparators. The format of the register is shown in Table 33.

Table 33. nODSCCfg Register (1DEh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	1	X	X	SCDLY				X	1	X	1	OCDLY			

X: Don't Care.

SCDLY: Short-Circuit Delay. Configure from 0x0 to 0xF to set short-circuit detection debouncing delay between 70µs and 985µs (70µs + 61µs x SCDLY). There can be up to 31µs of additional delay before the short-circuit's alert affects the discharge FET.

OCDLY: Overdischarge and Overcharge Current Delay. Configure from 0x1 to 0xF to set overdischarge/overcharge detection debouncing delay between 70µs and 14.66ms (70µs + 977µs x OCDLY).

nIPrtTh1 Register (1D3h)—Overcurrent-Protection Threshold

Register Type: Special

The nIPrtTh1 register shown in Table 34 sets the overcharge current-protection threshold and the virtual resistance setting. The upper 10-bits set the overcharge current-protection threshold and the lower 5-bits sets the virtual resistance. The protection threshold limit is configurable in 50µV resolution over the full operating range of the current register.

Table 34. nIPrtTh1 Register (1D3h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OverChargeCurrent Threshold											00000				

OverChargeCurrent: Overcharge current-protection threshold in room temperature. Overcharge current-protection occurs when the current register reading exceeds this value. This field is unsigned 50µV resolution (5mA resolution with a 10mΩ sense resistor). If nNVCfg1.enJP = 0, the OverChargeCurrent is flat across all of the temperature regions. If nNVCfg1.enJP = 1, then the OverChargeCurrent is updated for each temperature region base on the charging current

settings in *nIChgCfg1 and nIChgCfg2* as shown below:

Cold2OverChargeCurrent = OverChargeCurrent x (Cold2ChgCurr/RoomChargeCurr)

Cold1OverChargeCurrent = OverChargeCurrent x (Cold1ChgCurr/RoomChargeCurr)

CoolOverChargeCurrent = OverChargeCurrent x (CoolChgCurr/RoomChargeCurr)

RoomOverChargeCurrent = OverChargeCurrent

WarmOverChargeCurrent = OverChargeCurrent x (WarmChgCurr/RoomChargeCurr)

Hot1OverChargeCurrent = OverChargeCurrent x (Hot1ChgCurr/RoomChargeCurr)

Hot2OverChargeCurrent = OverChargeCurrent x (Hot2ChgCurr/RoomChargeCurr)

Cold2OverChargeCurrent = OverChargeCurrent x (Cold2ChgCurr/RoomChargeCurr)

The fault delay for overcharge current is configured in *nDelayCfg*.OverCurrTimer.

nIPrtTh2 Register (1D4h)

Register Type: Special

The nIPrtTh2 register shown in Table 35 sets the overdischarge current-protection threshold, charge-detection threshold, and low voltage charge blocking threshold. The upper 10-bits set the overdischarge current protection threshold. Charge detection threshold and undervoltage charge blocking are set in the lower bits. The protection threshold limit is configurable in 50µV resolution over the full operating range of the current register.

Table 35. nIPrtTh2 Register (1D4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OverDischargeCurrent Threshold										ChgDetTh			UVChg		

OverDischargeCurrent: Overdischarge current-protection threshold across all temperature regions. Overdischarge current-protection occurs when the current register reading exceeds this value. This field is an unsigned positive value with a 50µV resolution (5mA resolution with a 10mΩ sense resistor). To set an overdischarge threshold of -3000mA, set OverDischargeCurrent Threshold to 3000mA.

UVChg: Low Voltage Charge Blocking Feature. Enable this feature to prevent charging of the battery if the battery voltage drops below the UVChg threshold. The UVChg threshold can be set from 2.2V to 2.8V in 100mV steps. If VCell < UVChg, ProtStatus.UVChg (D5) is set to 1 without delay. If VCell > UVChg, ProtStatus.UVChg (D5) is cleared.

Set UVChg = 000b to disable the feature.

ChgDetTh: Charger Detection Threshold. The IC determines that a charger is connected when PCKP > (BATT + ChgDetTh). ChgDetTh has a range of 10mV to 80mV with a 10mV lsb.

Temperature Protection Registers

The IC has seven thresholds for charging protection as well as overdischarge temperature protection and overtemperature permanent failure protection. The standard register format for each of these thresholds is a unsigned number with 2.5°C resolution. The IC has 2.5°C of hysteresis for releasing temperature faults.

nTPrtTh1 Register (1D1h) and nTPrtTh2 Register (1D5h)

Register Type: Special

The nTPrtTh1 register shown in Table 36 and nTPrtTh2 register shown in Table 37 set the thresholds for the nine temperature regions (Tcold2, Tcold1, Tcool, Troom, Twarm, Thot1, Thot2, and Ttoohot) which control JEITA and provide charging (Too-Hot or Too-Cold) protection as shown in Figure 17. nProtMiscTh.TooHotDischarge provides discharging (Too-Hot only) protection. Threshold limits are configurable with 2.5°C resolution, have a 2.5°C hysterisis, and are all relative to Troom and adjacent temperature regions as shown below.

Note: Tcold2 should be set with a value between 1 and 15. TtooHot should be set with a value between 1 and 7.

Note: As temperature moves away from room temperature region, the IC transitions to the next temperature region at the threshold limit. As the temperature moves from hotter regions towards the room temperature region, the IC transitions to the next temperature region at the threshold limit - 2.5°C hysteresis. As the temperature moves from colder regions

towards the room temperature region, the IC transitions to the next temperature region at the threshold limit + 2.5°C hysteresis.

Table 36. nTPrtTh1 Register (1D1h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Tcold2				Tcold1				Tcool				Troom			

Table 37. nTPrtTh2 Register (1D5h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Ttoohot			Thot2				Thot1				Twarm			

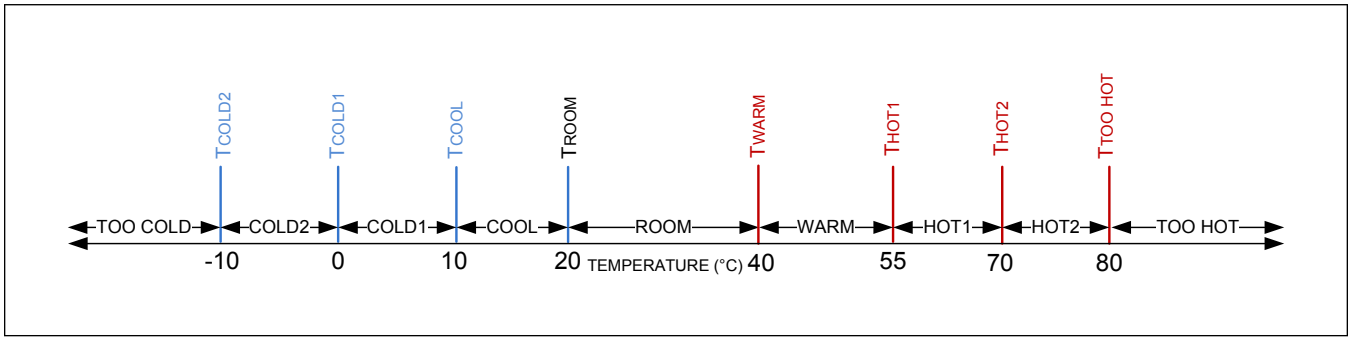


Figure 17. Nine Temperature Regions

Each threshold is calculated as follows:

TroomThr : Room temperature threshold is calculated as: TroomThr = Troom x 2.5°C

TcoolThr: Cool temperature threshold is calculated as: TcoolThr = TroomThr - (Tcool + 1) x 2.5°C

Tcold1Thr: Cold1 temperature threshold is calculated as: Tcold1Thr = TcoolThr - (Tcold1 + 1) x 2.5°C

Tcold2Thr: Cold2 temperature threshold is calculated as: Tcold2Thr = Tcold1Thr - (Tcold2 + 1) x 2.5°C

TwarmThr: Warm temperature threshold is calculated as: TwarmThr = TroomThr + (Twarm + 1) x 2.5°C

Thot1Thr: Hot1 temperature threshold is calculated as: Thot1Thr = TwarmThr + (Thot1 + 1) x 2.5°C

Thot2Thr: Hot2 temperature threshold is calculated as: Thot2Thr = Thot1Thr + (Thot2 + 1) x 2.5°C

TtoohotThr: TooHot temperature threshold is calculated as: TtoohotThr = Thot2Thr + (Ttoohot + 1) x 2.5°C

nTPrtTh3 Register (1D2h)

Register Type: Special

The nTPrtTh3 register shown in Table 38 sets the temperature permanent failure threshold. TpermFailHot is configurable with 5°C resolution from 50°C to 125°C.

Table 38. nTPrtTh3 Register (1D2h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TpermFailHot				UserMemory											

TpermFailHot: If enabled, the MAX17332 goes into permanent failure mode, and permanently disables the charge FET as well as trips the secondary protector (if installed) or blows the fuse (if installed) when the temperature exceeds the TpermFailHot threshold.

TpermFailHot threshold = 50°C + TpermFaiHot x 5°C

Fault Timer Registers

nDelayCfg Register (1DCh)

Factory Default Value: 0x9B3D

Set nDelayCfg to configure debounce timers for various protection faults. A fault state is concluded only if the condition persists throughout the duration of the timer. All delay times start when the ADC first measures the value to exceed the protection threshold which could be up to an additional 351ms of delay between the time the fault is observed externally and the time the ADC first measures the fault.

Charging faults can have an additional delay at the conclusion of the timer before the current completely drops 0mA.There is a capacitor from the gate to source of the CHG FET that is needed for charge regulation, which also slows down the ability to completely stop charge current for any charging faults. The current is immediately reduced at the end of the protection timer setting and is completely reduced to 0mA when the capacitor voltage decays to 0V.

Table 39. nDelayCfg (1DCh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHGWDT		FullTimer			OVPTimer		OverCurrTimer			PermFailTimer		TempTimer		UVPTimer	

UVPTimer: Set UVPTimer to configure the Undervoltage-Protection timer.

Shutdown Timer: Set UVPTimer to configure the Shutdown timer which controls the timing for entering Ship, DeepShip, and DeepShip2/UVShutdown. When the IC begins to enter a low-power mode, it is important to let the Shutdown Timer expire for the IC to fully enter the low-power mode before returning to active mode.

Table 40. UVPTimer Settings

UVPTimer SETTING	0	1	2	3
UVPTimer Configuration	0ms to 351ms	351ms to 0.7s	0.7s to 1.4s	1.4s to 2.8s
Shutdown Timer Configuration	22.5s to 45s	45s to 90s	90s to 180s	3min to 6min

TempTimer: Set TempTimer to configure the fault-timing for the following faults: Too-Cold-Charging (TooColdC), Too-Hot-Charging (TooHotC), Die-Hot (DieHot), and Too-Hot-Discharging (TooHotD).

Table 41. TempTimer Setting

TempTimer SETTING	0	1	2	3
Configuration	0ms to 351ms	351ms to 0.7s	0.7s to 1.4s	1.4s to 2.8s

The TempTimer setting also controls the temperature transition delay. If the MAX17332 detects a change in temperature that results in a lower OVP threshold, the MAX17332 applies a delay equal to the TempTrans configuration before the new lower OVP threshold goes into effect. There is a delay equal to the TempTrans configuration before the new lower OVP threshold goes into effect.

Table 42. TempTrans Configuration Settings

TempTimer SETTING	0	1	2	3
TempTrans Configuration	3.151s to 4.55s	5.951s to 8.75s	11.55s to 17.15s	23.351s to 34.851s

PermFailTimer: Set PermFailTimer to configure the fault timing for permanent failure detection. Generally, larger configurations are preferred to prevent permanent failure unless some severe condition persists.

Table 43. PermFailTimer Settings

PermFailTimer SETTING	0 (NOT RECOMMENDED)	1	2	3
Configuration	0ms to 351ms	351ms to 0.7s	0.7s to 1.4s	1.4s to 2.8s

OverCurrTimer: Set OverCurrTimer to configure the slower overcurrent protection (the additional fast hardware protection thresholds are described in nODSCCfg and nODSCTh). OverCurrTimer configures the fault timing for the slow overcharge-current detection (OCCP) as well as overdischarge-current detection (ODCP).

Table 44. OverCurrTimer Settings

OverCurrTimer SETTING	0	1	2	3	4	5	6	7
Configuration	0ms to 351ms	0.351s to 0.7s	0.7s to 1.4s	1.4s to 2.8s	2.8s to 5.6s	5.6s to 11.25s	11.25s to 22.5s	22.5s to 45s

OVPTimer: Set OVPTimer to configure the fault timing for overvoltage protection.

Table 45. OVPTimer Settings

OVPTimer SETTING	0	1	2	3
Configuration	0ms to 351ms	351ms to 0.7s	0.7s to 1.4s	1.4s to 2.8s

FullTimer: Set FullTimer to configure the timing for full detection. When charge-termination conditions are detected after the timeout, the CHG FET turns off (if feature is enabled).

Prequal Timer: Set FullTimer to configure the timing for prequal charging. Prequal Timer and FullTimer share the same bits in the nDelayCfg register.

Table 46. FullTimer Settings

FullTimer SETTING	0	1	2	3	4	5	6	7
FullTimer Configuration	33s to 44s	67s to 90s	2.25min to 3min	4.5min to 6min	9min to 12min	18min to 24min	36min to 48min	72min to 96min
Prequal Timer Configuration	16.875s to 22.5s	33s to 44s	67s to 90s	2.25min to 3min	4.5min to 6min	9min to 12min	18min to 24min	36min to 48min

CHGWDT: Set CHGWDT to configure the charger communication watchdog timer. If enabled, the MAX17332 charge-protects whenever the host has stopped communicating and the SDA/SCL lines idle high for longer than this timeout.

ChgRm: Charger removal debounce (1/4 ChgWDT debounce setting)

Table 47. ChgWDT/ChgRm Settings

ChgWDT/ChgRm SETTINGS	0	1	2	3
CHGWDT Timer	11.2s to 22.5s	22.5s to 45s	45s to 90s	90s to 3min
ChgRm Timer	2.8s to 5.6s	5.6s to 11.2s	11.2s to 22.4s	22.4s to 44.8s

Battery Internal Self-Discharge Detection Registers

Factory Default nProtCfg2 Value: 1006h

To enable the ISD feature using the coulombic-efficiency (CE) method, configure LeakFaultCfg, LeakCurrTh, and CEEn as shown in Table 48. Choose the alert and fault mode with LeakFaultCfg and configure the thresholds with LeakCurrTh, as shown in Table 49. When the ISD alerts are enabled, any leakage current detected beyond the threshold is indicated by the ProtAlrt.LDET bit and *Status*.PA bit (if nConfig.ProtAlrtEn = 1). If the ALRT pin is enabled for alerts (nConfig.Aen = 1 and nConfig.ProtAlrtEn = 1), then the pin indicates the ISD alert. To service the alert, first clear the *ProtAlrt* register and then clear *Status*.PA. The event is also indicated in *nBattStatus*.LDET, which is recorded in the permanent lifelog.

The reported leakage-current measurement can be read from two different registers:

- LeakCurrRep = 15-bit unsigned left-justified value with an LSB of 1.5625µV/16 (or 0.15625mA/16 with 10mΩ sense resistor).
- *nBattStatus*.LeakCurr = 8-bit unsigned value with an LSB of 3.125µV (or 0.3125mA with 10mΩ sense resistor).

Contact Analog Devices for configuring the ISD feature.

Table 48. nProtCfg2 Register (1DFh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LeakFaultCfg			CEEn	LeakCurrTh				CheckSum							

Table 49. Alert and Fault Mode Settings

LeakFaultCfg SETTING	DESCRIPTION	LeakCurrTh RESOLUTION	ALERT RANGE	FAULT RANGE
		Note: Leakage current above LeakCurrTh triggers an alert/fault. Currents refer to the 10mΩ R_{SENSE}.		
000	Disabled			
001	Alert Only	0.3125mA	0.3125mA to 5mA	
010	Fault = Alert + 2.5mA			2.8125mA to 7.5mA
011	Fault = Alert + 5mA			5.3125mA to 10mA
100	Fault Only (+2.5mA offset)	0.625mA		3.125mA to 12.5mA
101	Alert Only		0.625mA to 10mA	
110	Fault = Alert + 2.5mA			3.125mA to 12.5mA
111	Fault = Alert + 10mA			10.625mA to 20mA

X: Don't Care

CEEn: Coulombic-efficiency (CE) method enable. Set to 1 to enable self-discharge detection.

LeakFaultCfg: Leakage Fault Configuration. Set LeakFaultCfg to configure the alert and fault behavior as shown in Table 49.

LeakCurrTh: Leakage Current Threshold is an unsigned 4-bit threshold for leakage current alert and fault generation. The LSB resolution is either 0.625mA or 1.25mA based on the LeakCurrCfg setting as shown in Table 49. When alerts and faults are both enabled, the fault threshold is either 5mA, 10mA, or 20mA above the alert threshold as shown in the Description column of Table 49.

CheckSum: Protector NVM CheckSum. CheckSum is the checksum value of the protection registers for validating NVM at startup when nNVCfg1.enProtChksm = 1.

LeakCurrRep Register (0x16F)

The LeakCurrRep register contains the reported leak current when it is enabled with nCheckSum.CEEn as shown in Table 50.

Table 50. LeakCurrRep Register (0x16F) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Reported LeakCurrent														

Reported LeakCurrent: Reported Leak Current is an unsigned 15-bit leakage current. This register stores the reported leakage current with an LSB of 1.5625µV/16 (or 0.15625mA/16 with a 10mΩ sense resistor). The range is 0mA to 319.99mA.

Status/Configuration Protection Registers

nProtCfg Register (1D7h)

The Protection Configuration register contains enable bits for various protection functions.

Table 51. nProtCfg Register (1D7h) Format

D15	D14	D13	D12	D11	D10	D9	D8
ChgWDTEn	0	FullEn	SCTest		CmOvrdEn	ChgTestEn	PrequalEn
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved	PFEn	DeepShpEn	OvrdEn	0	FetPFEn	BlockDisCEn	DeepShp2En

BlockDisCEn: Block Discharge FET at too Cold (nTPrtTh1).

PFEn: PermFail Enable. Set PFEn = 1 to enable the detection of a permanent failure to permanently turn the FETs off.

All types of permanent failures operate only if PFEn = 1 and are all disabled if PFEn = 0. PFEn must be enabled for the PFAIL pin to be operational. See the *Permanent Failure* section for more details. PermFail can not be enabled if Thermistor 2 is enabled. See *nPackCfg* for details.

FetPFEn: FET PermFail Enable. Set to 1 to enable Charge FET and Discharge FET open or short detection, which registers a permanent failure, permanently turns the FETs off, and drives the PFAIL pin high. PFEn must also be set for the FET PermFail Enable to operate.

OvrdEn: Override Enable. Set OvrdEn = 1 to enable the Alert pin to be an input to disable the protection FETs.

CmOvrdEn: Comm Override Enable. This bit when set to 1 allows the ChgOff and DisOff bits in CommStat to be set by I^2C communication to turn off the protection FETs.

See the *Disabling FETs by Pin-Control or I^2C Command* section for more details about OvrdEn and CmOvrdEn.

DeepShpEn: Set DeepShpEn = 1 to associate shutdown actions (I^2C shutdown command or communication removal) with shutdown. All registers power down in this mode. Set DeepShpEn = 0 to continue full calculations but with protector disabled (CHGEn = 0, DISEn = 0, pump off), operating at the consumption rate.

DeepShp2En: Set DeepShp2En = 1 to associate shutdown actions (I^2C shutdown command or communication removal) with shutdown. All registers power down in this mode. Set DeepShp2En = 0 to use DeepShip 1 (or modes. Wake up DeepShip2 by connecting a charge source.

SCTest: Set SCTest = 10 to source 30µA from BATT to PCKP for testing the presence/removal of any overload/short-circuit at PCKP. SCTest is only used during special circumstances when DIS = off. Particularly if an overdischarge current fault has been tripped. Because of this, the PCKP resistor must be 10kΩ or less for proper short-circuit removal detection. Set SCTest = 00b to disable.

BlockChgEn: Enable block Chg FET from I^2C for parallel charging application. Protstatus.D7 is set to 1 or 0 according to Config.D0.

PrequalEn: Prequal Fault Enable. Charge the battery at prequal current until cell voltage is greater than Prequal Voltage setting. If PrequalEn = 1, VCell must increase beyond the Prequal Voltage level before the nDelayCfg.PrequalTimer expires or a charge fault is triggered. If PrequalEn = 0, the prequal charging current continues until VCell increases beyond the Prequal Voltage level. Prequal current and voltage are set in *nChgCfg0*.

FullEn: Full Charge Protection Enable. If the full charge protection feature is enabled, the charge FET opens when the battery is fully charged (RepSOC reaches 100%).

ChgWDTEn: Charger WatchDog Enable. If the charger watchdog feature is enabled, the protector disallows charging unless communication has not been detected for more than the Charger WatchDog delay that is configured in nDelayCfg.ChgWdg.

nBattStatus Register (1A8h)

Battery Status Nonvolatile Register

The Battery Status register contains the permanent battery status information. If nProtCfg.PFen = 1, then a permanent fail results in permanently turning the FETs off to ensure the safety of the battery.

Table 52. nBattStatus Register (1A8h) Format

D15	D14	D13	D12	D11	D10	D9	D8
PermFail	OVPF	OTPF	CFETFs	DFETFs	FETFo	BattHlth	ChksumF
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved							

PermFail: Permanent Failure. This bit is set if any permanent failure is detected.

CFETFs: ChargeFET Failure-Short Detected. If the MAX17332 detects that the charge FET is shorted and cannot be opened, it sets the CFETFs bit and the PermFail bit. This function is enabled with nProtCfg.FetPFEn.

DFETFs: DischargeFET Failure-Short Detected. If the MAX17332 detects that the discharge FET is shorted and cannot be opened, it sets the DFETFs and the PermFail bit. This function is enabled with nProtCfg.FetPFEn.

FETFo: FET Failure Open. If the MAX17332 detects an open FET failure on either FET, it sets FETFo. This function is

enabled with nProtCfg.FetPFEn.

ChksumF: Checksum Failure. ChksumF protection related NVM configuration registers checksum failure. In the case of a checksum failure, the device sets the PermFail bit but does not write it to NVM to prevent using an additional NVM write. This allows the PermFail bit to be cleared by the host so that the INI file can be reloaded.

ProtAlrt Register (0AFh)

The Protection Alerts register contains a history of any protection events that have been logged by the device and is formatted as shown in Table 53. If any bit of ProtAlrt is 1, then the Status.PA bit is also 1 if Config.PAEn = 1. Once a bit is set, it remains set until cleared by the host. The Alert pin is driven low if Config.ProtAlrtEn = 1.

Table 53. ProtAlrt Register (0AFh) Format

D15	D14	D13	D12	D11	D10	D9	D8
ChgWDT/LDet	TooHotC	Full	TooColdC	OVP	OCCP	Qovflw	Reserved
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved	TempRegionChange	DieHot	TooHotD	UVP	ODCP	Reserved	Reserved

TempRegionChange: Temperature Region Change. A change in the JEITA temperature region creates this alert so that the host is alerted to a reduction in JEITA charging voltage that can impact the charging or protection parameters.

HProtCfg2 Register (0F1h)

Register Type: Special

Nonvolatile Backup: None

The status of the discharge FET and charge FET can be monitored in the HProtCfg2 register as shown in Table 54.

Table 54. HProtCfg2 (0F1h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	DISs	CHGs

DISs: Discharge FET Status. DISs = 1 indicates the discharge FET is on and allows discharge current. DISs = 0 indicates the discharge FET is off and blocks discharge current.

CHGs: Charge FET Status. CHGs = 1 indicates the charge FET is on and allows charge current. CHGs = 0 indicates the charge FET is off and blocks charge current.

X: Reserved.

FProtStat Register (0DAh)

Table 55. FProtStat Register (0DAh) format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X										IsDis	X		Hot	Cold	Warm

X: Don't Care

IsDis: Battery is in Discharging state. Cleared when charging signal is detected.

Hot: Operating in Hot JEITA region.

Cold: Operating in Cold JEITA region.

Warm: Operating in Warm JEITA region.

ProtStatus Register (0D9h)

The Protection Status register contains the Fault States of the Protection State Machine.

Table 56. ProtStatus Register (0D9h) Format

D15	D14	D13	D12	D11	D10	D9	D8

Table 56. ProtStatus Register (0D9h) Format (continued)

ChgWDT	TooHotC	Full	TooColdC	OVP	OCCP	Qovflw	PreqF/LDet
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BlockChg	PermFail	DieHot/UVChg	TooHotD	UVP	ODCP	BlockDis/TooColdD	Shdn

BlockChg: Blocks charging from either communication timeout or absence of recurring Status.BlockChg = 0 command.

BlockDis: Blocks discharging by direct I^2C command (Config2.BlockDis) BlockDis auto-releases when BlockChg begins.

TooColdD: Same threshold with TooColdC. Enable this function by setting BlockDisCEn in nProtCfg register.

Shdn: A flag to indicate the Shutdown Event status to Protector module for further action on Charging/Discharging FETs, Charge Pump, and PkSink.

PermFail: Permanent Failure Detected. See nBatteryStatus for details of the Permanent Failure.

Discharging Faults:

ODCP—Overdischarge current protection

UVP—Undervoltage Protection

TooHotD—Overtemperature for Discharging

DieHot—Overtemperature for die temperature

Charging Faults:

TooHotC—Overtemperature for Charging

OVP—Overvoltage

OCCP—Overcharge Current Protection

Qovrflw—Q Overflow

TooColdC—Undertemperature

Full—Full Detection (Not a fault, but CHG FET is opened when Full is detected)

ChgWDT—Charge Watchdog Timer

DieHot—Overtemperature for Die Temperature

PreqF—Prequal timeout was detected

LDet—Leakage fault was detected

UVChg—Undervoltage Charge Blocking

Other Protection Registers

nProtMiscTh Register (1D6h)

Register Type: Special

The nProtMiscTh register is shown in Table 57 and sets a few miscellaneous protection and alert thresholds.

Table 57. nProtMiscTh Register (1D6h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
QovflwTh				TooHotDischarge				CurrDet				DieTempTh			

DieTempTh: Sets the dietemp overtemperature protection threshold relative to 50°C and has an LSB of 2.5°C. DieTempTh defines the delta between 50°C and the dietemp protection threshold. The range is 50°C and 87.5°C.

CurrDet: CurrDet is configurable from 25µV/R_{SENSE} to 400µV/R_{SENSE} in 25µV/R_{SENSE} steps (equivalent to 2.5mA to 40mA in 2.5mA steps with a 10mΩ sense resistor). It is a threshold to detect discharging and charging event from the device perspective. If (current > CurrDet) charging; if (current < -CurrDet) discharging. By default, the CurrDet setting of 2, corresponding with ±7.5mA (on 10mΩ sense resistor). Analog Devices recommends this setting which is optimized

according to the ADC noise.

TooHotDischarge: Sets the over-temperature protection threshold associated with discharge. TooHotDischarge has 2°C LSB's and defines the delta between Over-Temp-Charge (nTPrtTh1.T4) and Over-Temp-Discharge. The range is nTPrtTh1.T4(TooHot) to nTPrtTh1.T4(TooHot) + 30°C.

QovflwTh: QovflwTh sets the coefficient for the Qoverflow alert threshold. Qoverflow alert threshold = designCap x coefficient. The MAX17332 monitors the delta Q between the Q at the start of charge and the current Q. If the delta Q exceeds the Qoverflow alert threshold, indicating that the charger has charged more than the expected capacity of the battery, then a ProtStatus.Qovrflw fault is generated and the charge is briefly interrupted. The ProtAlrt.QOverflow bit remains set until the host clears the bit. The coefficient is calculated as: coefficient = 1.0625 + (QovflwTh x 0.0625).

ModelGauge m5 Algorithm

ModelGauge m5 EZ Registers

For accurate results, the ModelGauge m5 EZ uses information about the cell and the application as well as the real-time information measured by the IC. Figure 18 shows inputs and outputs to the algorithm grouped by category. Analog input registers are the real-time measurements of voltage, temperature, and current performed by the IC. Application-specific registers are programmed by the customer to reflect the operation of the application. The Cell Characterization Information registers hold characterization data that models the behavior of the cell over the operating range of the application. The Algorithm Configuration registers allow the host to adjust the performance of the IC for its application. The Learned Information registers allow an application to maintain the accuracy of the fuel gauge as the cell ages. The register description sections describe each register function in detail.

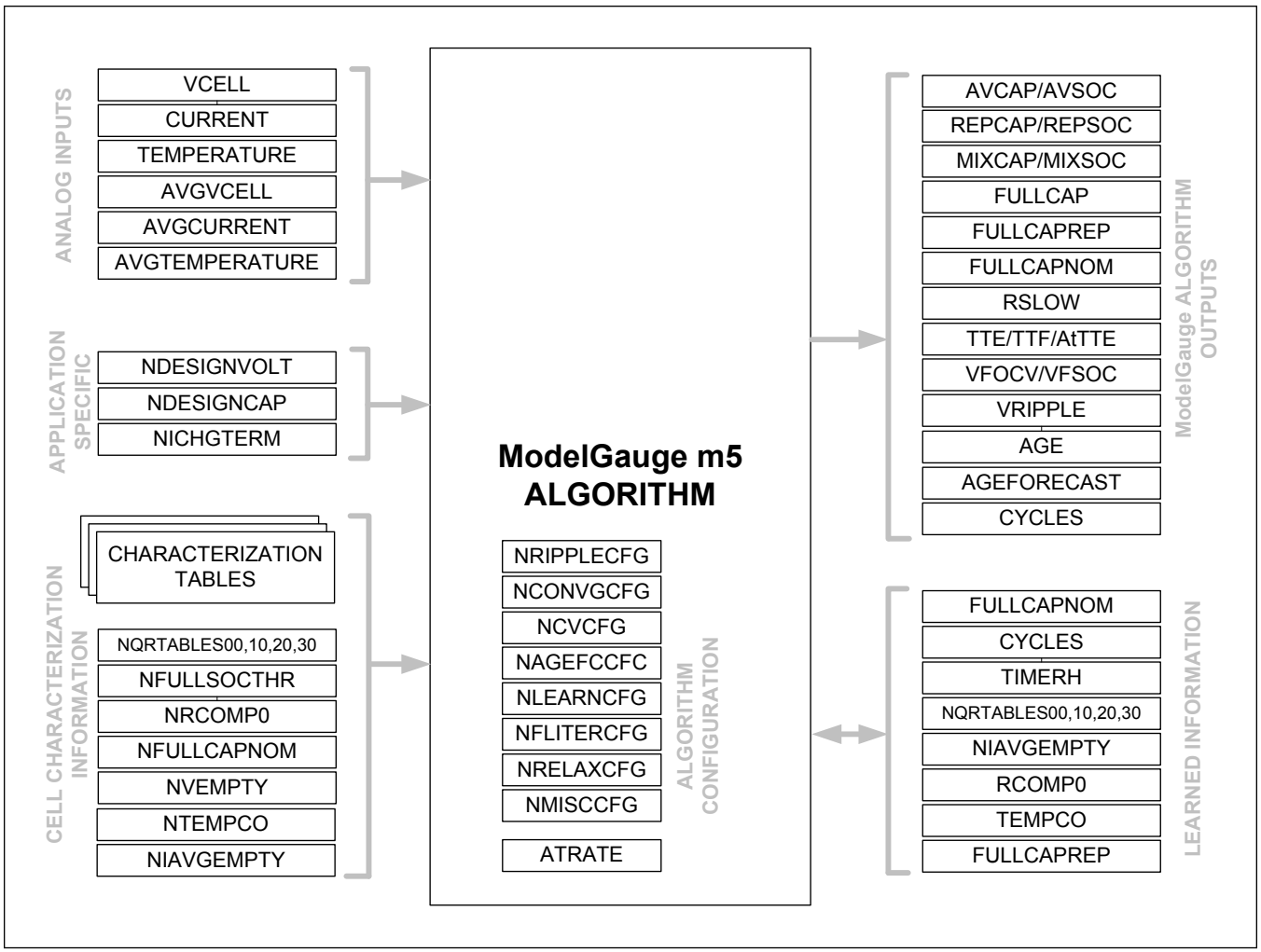


Figure 18. ModelGauge m5 EZ Registers

ModelGauge m5 EZ Algorithm Output Registers

The following registers are outputs from the ModelGauge m5 EZ algorithm. The values in these registers become valid 480ms after the IC is reset.

RepCap Register (005h)

Register Type: Capacity

Nonvolatile Backup: None

RepCap or Reported Capacity is a filtered version of the AvCap register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in temperature or load current. See the *Fuel-Gauge Empty Compensation* section for details.

RepSOC Register (006h)

Register Type: Percentage

Nonvolatile Backup: None

RepSOC is a filtered version of the AvSOC register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in load current. RepSOC corresponds to RepCap and *FullCapRep*. RepSOC

is intended to be the final state of charge percentage output for use by the application. See the *Fuel-Gauge Empty Compensation* section for details.

FullCapRep Register (010h)

Register Type: Capacity

Nonvolatile Backup and Restore: nFullCapRep (1A9h) or *nFullCapNom* (1A5h)

This register reports the full capacity that goes with *RepCap*, generally used for reporting to the user. A new full-capacity value is calculated at the end of every charge cycle in the application.

TTE Register (011h)

Register Type: Time

Nonvolatile Backup: None

The TTE register holds the estimated time-to-empty for the application under present temperature and load conditions. The TTE value is determined by dividing the AvCap register by the AvgCurrent register. The corresponding AvgCurrent filtering gives a delay in TTE empty, but provides more stable results.

TTF Register (020h)

Register Type: Time

Nonvolatile Backup: None

The TTF register holds the estimated time-to-full for the application under present conditions. The TTF value is determined by learning the constant current and constant voltage portions of the charge cycle based on experience of prior charge cycles. Time-to-full is then estimated by comparing the present charge current to the charge termination current. Operation of the TTF register assumes all charge profiles are consistent in the application. See the *Typical Operating Characteristics* for sample performance.

Age Register (007h)

Register Type: Percentage

Nonvolatile Backup: None

The Age register contains a calculated percentage value of the application's present cell capacity compared to its expected capacity. The result can be used by the host to gauge the battery pack health as compared to a new pack of the same type. The equation for the register output is:

Age Register = 100% x (*FullCapNom* register/DesignCap register)

Cycles Register (017h) and nCycles (1A4h)

Register Type: Special

Nonvolatile Backup and Restore: nCycles (1A4h)

The Cycles register maintains a total count of the number of charge/discharge cycles of the cell that have occurred. The result is stored as a percentage of a full cycle. For example, a full charge/discharge cycle results in the Cycles register incrementing by 100%. The Cycles register has a full range of 0 to 16383 cycles with a 25% LSb. Cycles is periodically saved to nCycles to provide a long-term nonvolatile cycle count.

Table 58. nCycles Register (1A4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CycleCount (Cycles register << (3-nNVCfg2.FibScl))													nFib		

The LSB of nCycles.CycleCount depends nNVCfg2.fibScl as shown in Table 59. The LSB of the Cycles register is 25%.

Table 59. nNVCfg2.FibScl Setting Determines LSb of nNVCfg2.CyclesCount

NNVCFG2.FIBSCL	NCYCLES.CYCLECOUNT LSB
00b	25%

Table 59. nNVCfg2.FibScl Setting Determines LSb of nNVCfg2.CyclesCount (continued)

01b	50%
10b	100%
11b	200%

Configure nFib = 0 for any new pack. nFib is a reset counter which controls Fibonacci-saving reset accelleration (see the *100 Record Life Logging* section). Each reset followed by any nonvolatile save increases by 1. Maximum value is 7 without overflow.

TimerH Register (0BEh)

Register Type: Special

Nonvolatile Backup and Restore: nTimerH (1AFh) if nNVCfg2.enT is set

Alternate Initial Value: 0x0000

This register allows the IC to track the age of the cell. An LSb of 3.2 hours gives a full-scale range for the register of up to 23.94 years. If enabled, this register is periodically backed up to nonvolatile memory as part of the learning function.

FullCap Register (035h)

Register Type: Capacity

Nonvolatile Restore: Derived from nFullCapNom (1A5h)

This register holds the calculated full capacity of the cell based on all inputs from the ModelGauge m5 EZ algorithm including empty compensation. A new full-capacity value is calculated continuously as application conditions change.

nFullCapNom Register (1A5h)

Register Type: Capacity

Nonvolatile Backup and Restore: FullCapNom (023h)

This register holds the calculated full capacity of the cell, not including temperature and empty compensation. A new full-capacity nominal value is calculated each time a cell relaxation event is detected. This register is used to calculate other outputs of the ModelGauge m5 EZ algorithm.

RCell Register (014h)

Register Type: Resistance

Nonvolatile Backup: None

Initial Value: 0x0290

The RCell register displays the calculated internal resistance of the cell. RCell is determined by comparing open-circuit voltage (VFOCV) against measured voltage (VCell) over a long time period while under load current.

VRipple Register (0B2h)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0000

The VRipple register holds the slow average RMS value of VCell register reading variation compared to the AvgVCell register. The default filter time is 22.5 seconds. See *nRippleCfg* register description. VRipple has an LSb weight of (1.25/128)mV.

nVoltTemp Register (1AAh)

Register Type: Special

Nonvolatile Backup: AvgVCell and AvgTA registers if nNVCfg2.enVT = 1

This register has dual functionality depending on configuration settings. If nNVCfg2.enVT = 1, this register provides nonvolatile back up of the AvgVCell and AvgTA registers as shown in Table 60.

Table 60. nVoltTemp Register (1AAh) Format when nNVCfg2.enVT = 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AvgVCell Upper 9 Bits									AvgTA Upper 7 Bits						

Alternatively, if nNVCfg0.enAF = 1, this register stores an accumulated age slope value to be used with the Age Forecasting algorithm. Regardless of which option is enabled, this register is periodically saved to nonvolatile memory as part of the learning function. If neither option is enabled, this register can be used as general purpose user memory.

ModelGauge m5 EZ Performance

ModelGauge m5 EZ performance provides plug-and-play operation of the IC. While the IC can be custom tuned to the applications battery through a characterization process for ideal performance, the IC has the ability to provide reasonable performance for most applications with no custom characterization required.

While EZ performance provides reasonable performance for most cell types, some chemistries such as lithium-iron-phosphate (LiFePO4) and Panasonic NCR/NCA series cells require custom characterization for best performance. EZ performance provides models for applications with empty voltages ranging from 3V to 3.4V through the EV kit GUI Configuration Wizard. Contact Analog Devices for details of the custom characterization procedure.

OCV Estimation and Coulomb Count Mixing

The core of the ModelGauge m5 EZ algorithm is a mixing algorithm that combines the OCV state estimation with the coulomb counter. After power-on reset of the IC, coulomb-count accuracy is unknown. The OCV state estimation is weighted heavily compared to the coulomb count output. As the cell progresses through cycles in the application, the coulomb-counter accuracy improves and the mixing algorithm alters the weighting so that the coulomb-counter result is dominant. From this point forward, the IC switches to servo mixing, which provides a fixed magnitude continuous error correction to the coulomb count (up or down) based on the direction of the error from the OCV estimation. This allows differences between the coulomb count and OCV estimation to be corrected quickly (see Figure 19).

The resulting output from the mixing algorithm does not suffer accumulation drift from current measurement offset error and is more stable than a stand-alone OCV estimation algorithm. See Figure 20. Initial accuracy depends on the relaxation state of the cell. The highest initial accuracy is achieved with a fully relaxed cell.

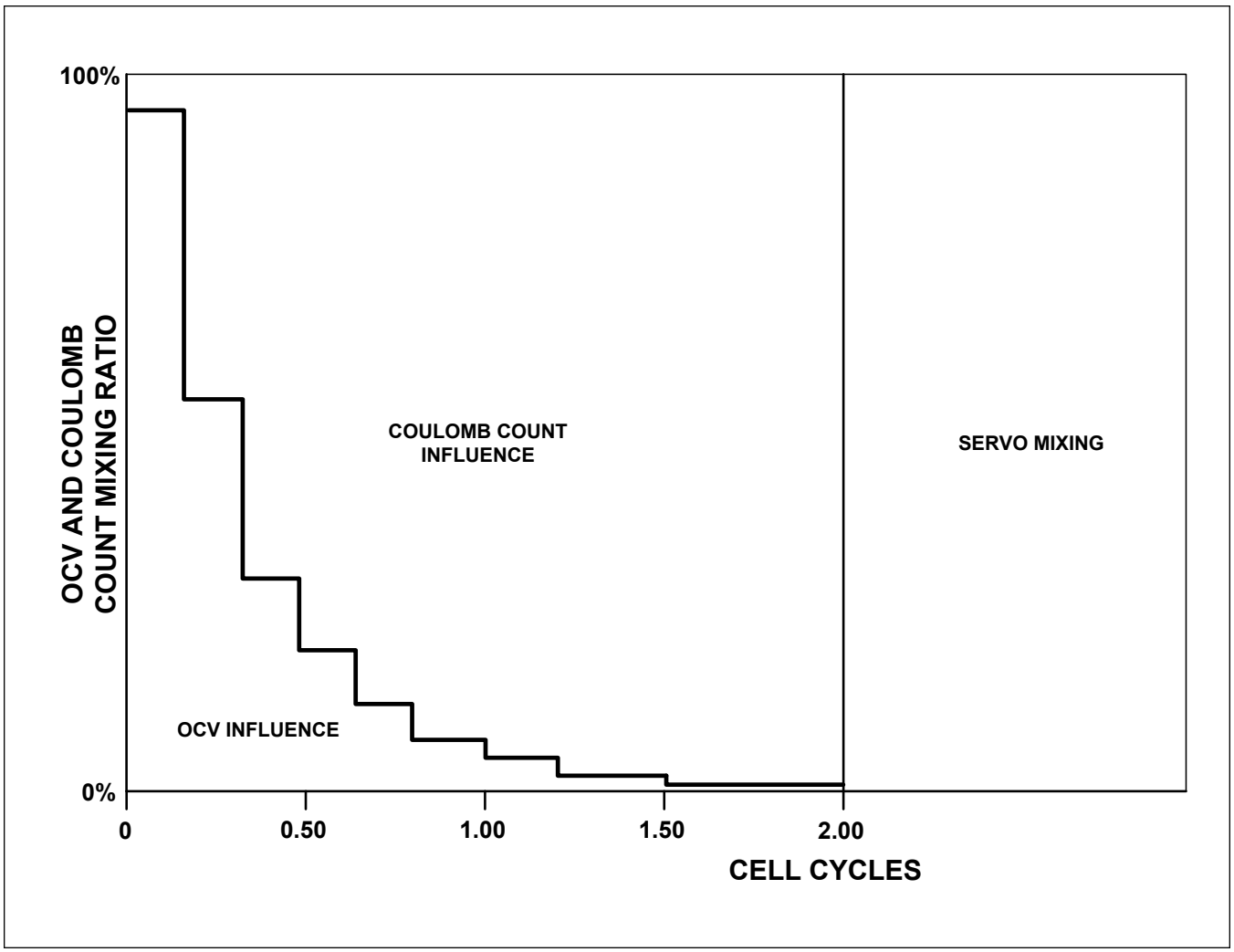


Figure 19. Voltage and Coulomb Count Mixing

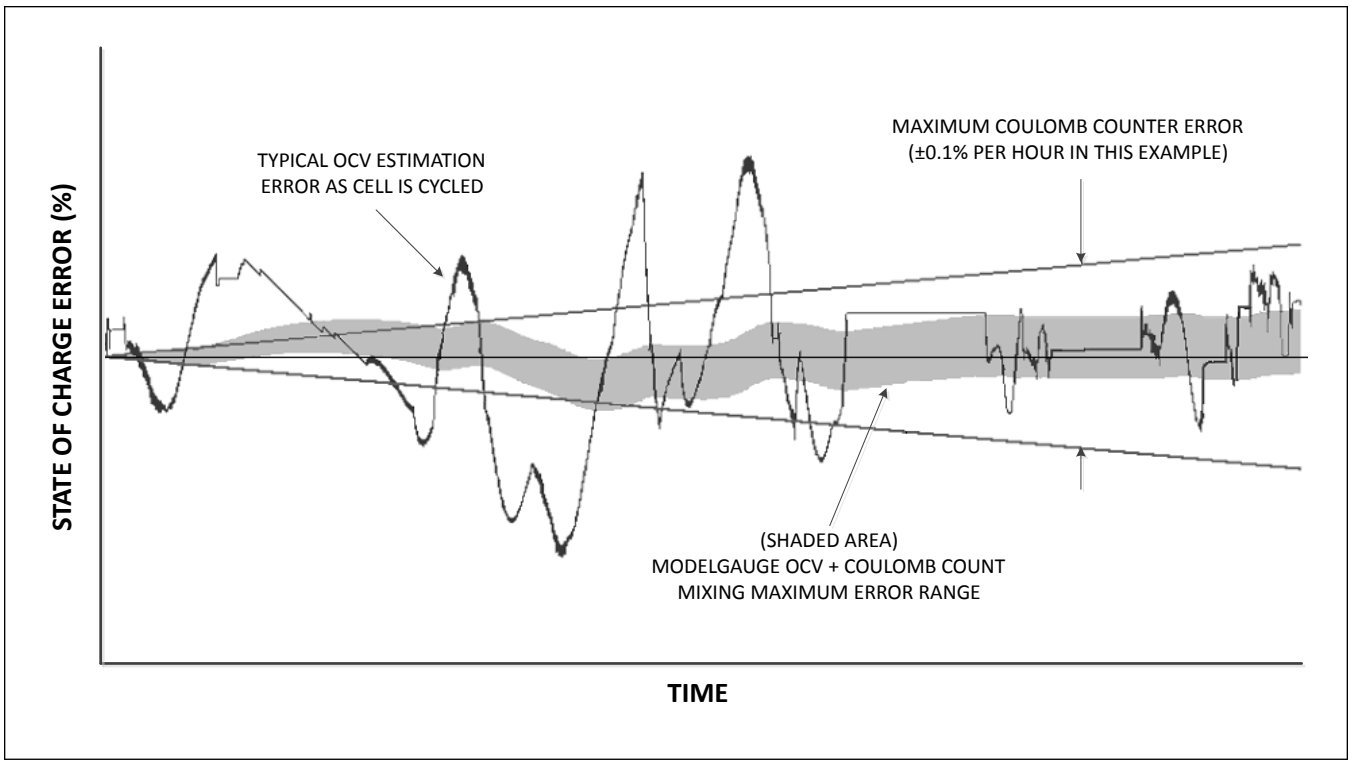


Figure 20. ModelGauge m5 EZ Typical Accuracy Example

Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m5 EZ algorithm distinguishes between the remaining capacity of the cell and the remaining capacity of the application, and reports both results to the user.

The *MixCap* output register tracks the charge state of the cell. This is the theoretical miliamp-hours of charge that can be removed from the cell under ideal conditions—extremely low discharge current and independent of cell voltage. This result is not affected by application conditions such as cell impedance or minimum operating voltage of the application. ModelGauge m5 EZ continually tracks the expected empty point of the application in milliamp-hours. This is the amount of charge that cannot be removed from the cell by the application because of minimum voltage requirements and internal losses of the cell. The IC subtracts the amount of charge not available to the application from the *MixCap* register and reports the result in the *AvCap* register.

Since the available remaining capacity is highly dependent on discharge rate, the *AvCap* register can be subject to large instantaneous changes as the application load current changes. The result can increase if the load current suddenly drops, even while discharging. This result, although correct, can be very counterintuitive to the host software or end user. The *RepCap* output register contains a filtered version of *AvCap* that removes any abrupt changes in remaining capacity. *RepCap* converges with *AvCap* over time to correctly predict the application empty point while discharging or the application full point while charging. Figure 21 shows the relationship of these registers.

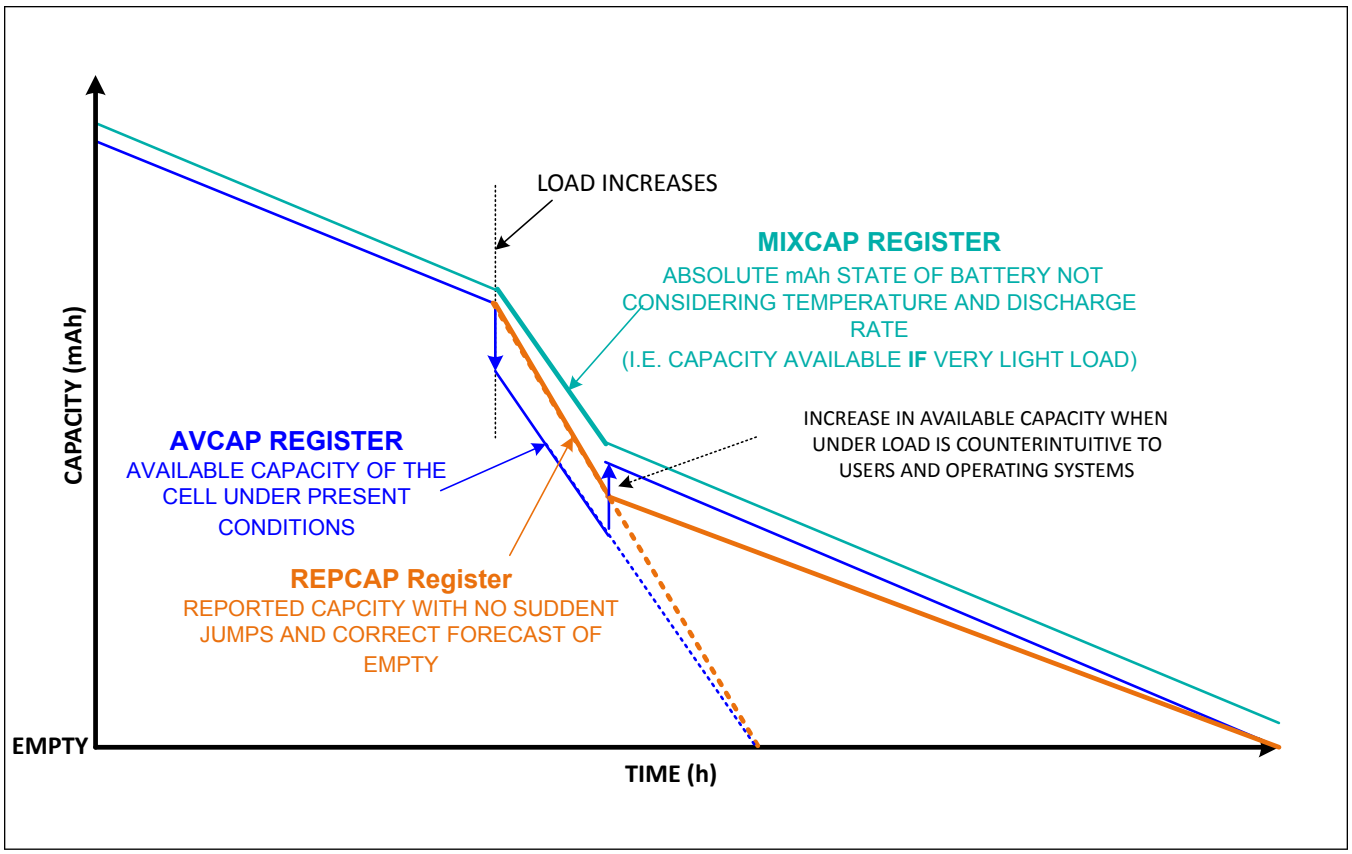


Figure 21. Handling Changes in Empty Calculation

Fuel Gauge Learning

The IC periodically makes internal adjustments to cell characterization and application information to remove initial error and maintain accuracy as the cell ages. These adjustments always occur as small under-corrections to prevent instability of the system and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. In addition to estimating the battery's state-of-charge, the IC observes the battery's relaxation response and adjusts the dynamics of the voltage fuel gauge. Registers used by the algorithm include:

• **Application Capacity (*FullCapRep* Register):** This is the total capacity available to the application at full, as described in the End-of-Charge section. See the *FullCapRep* register description.

• **Cell Capacity (*FullCapNom* Register):** This is the total cell capacity at full, according to the voltage fuel gauge. This includes some capacity that is not available to the application at high loads and/or low temperature. The IC periodically compares percent change based on an open circuit voltage measurement verses coulomb-count change as the cell charges and discharges, maintaining an accurate estimation of the pack capacity in milliamp-hours as the pack ages. See Figure 22.

• **Voltage Fuel-Gauge Adaptation:** The IC observes the battery's relaxation response and adjusts the dynamics of the voltage fuel gauge. This adaptation adjusts the RComp0 register during qualified cell relaxation events.

• **Empty Compensation:** The IC updates internal data whenever cell empty is detected (*VCell* < *VEmpty*) to account for cell age or other cell deviations from the characterization information.

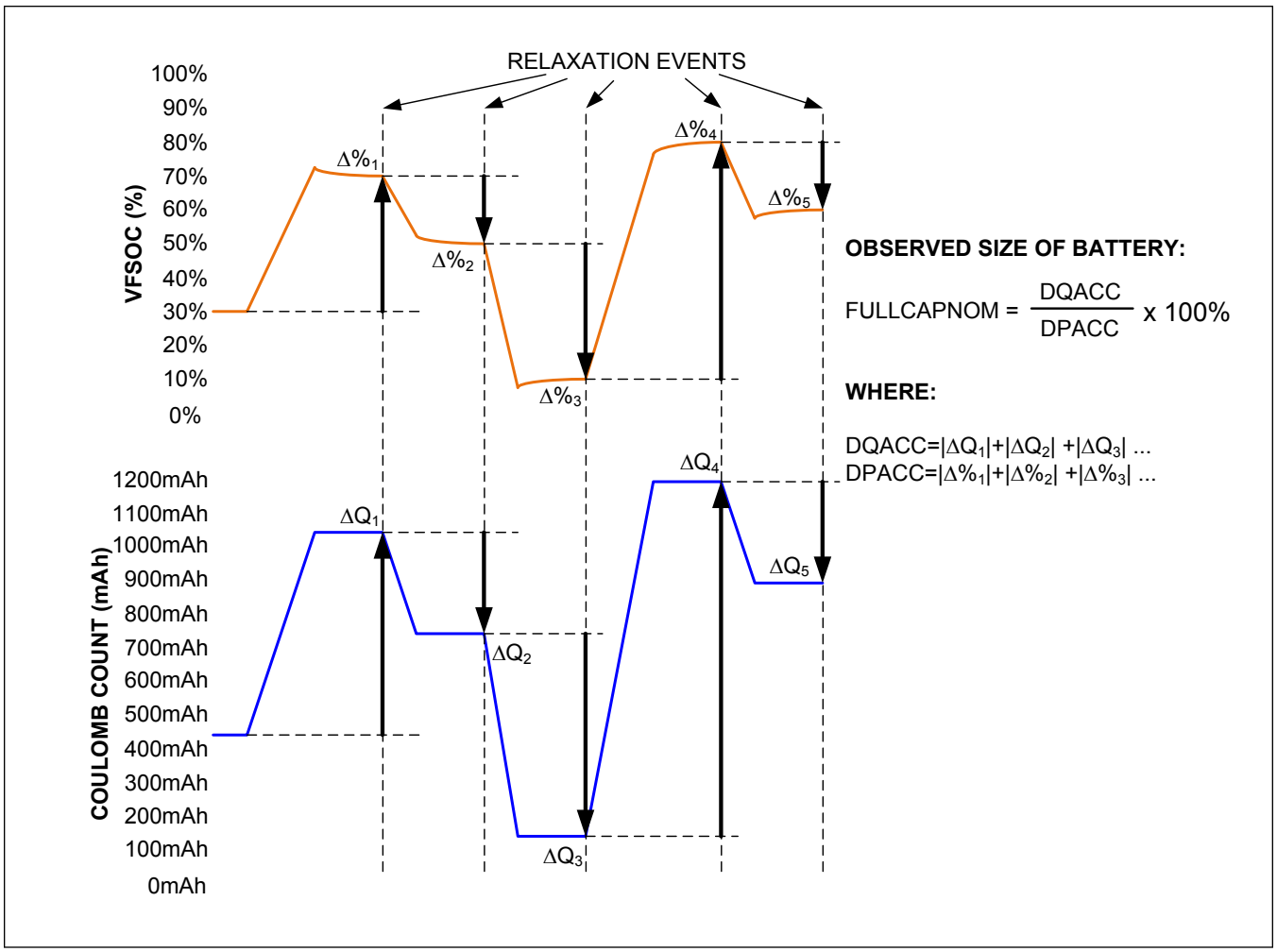


Figure 22. FullCapNom Learning

Converge-To-Empty

The MAX17332 includes a feature that guarantees the fuel gauge output converges to 0% as the cell voltage approaches the empty voltage. As the cell's voltage approaches the expected empty voltage (*AvgVCell* approaches *VEmpty*) the IC smoothly adjusts the rate of change of *RepSOC* so that the fuel gauge reports 0% at the exact time the cell's voltage reaches empty. This prevents minor over or undershoots in the fuel gauge output. See Figure 23.

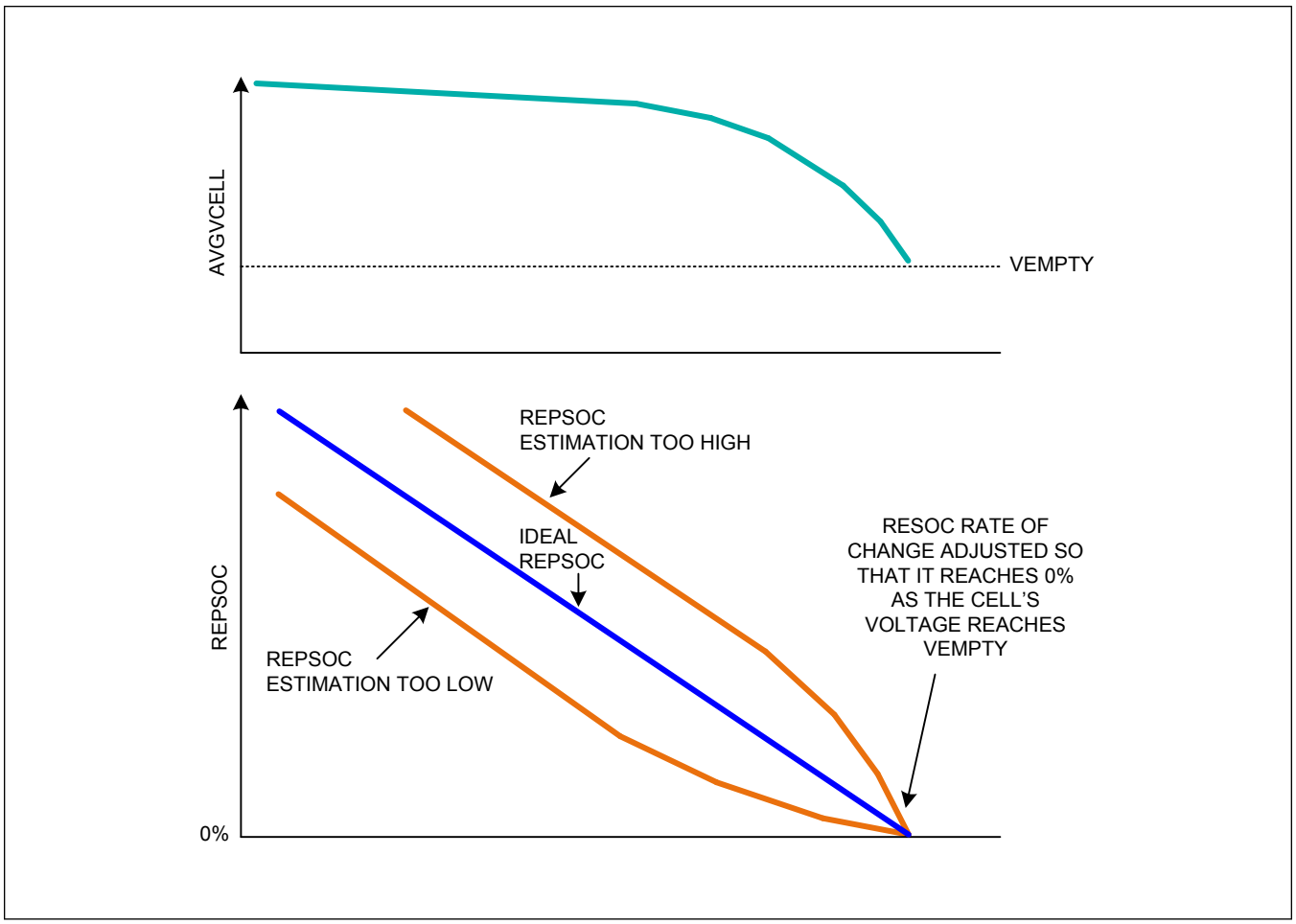


Figure 23. Converge-To-Empty

Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge as experienced by end users, the battery should be exercised in a dynamic manner. The end-user accuracy cannot be understood with only simple cycles. To challenge a correction-based fuel gauge such as a coulomb counter, test the battery with partial loading sessions. For example, a typical user can operate the device for ten minutes and then stop use for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and duration. Refer to the *Application Note 4799: Cell Characterization Procedure for a ModelGauge m3/ModelGauge m5 Fuel Gauge.*

Initial Accuracy

The IC uses the first voltage reading after power-up or after the cell is connected to the IC to determine the starting output of the fuel gauge. It is assumed that the cell is fully relaxed prior to this reading, however this is not always the case. If there is a load or charge current present, the initial reading is compensated using the characterized internal impedance of the cell (RFast register) to estimate the cell's relaxed voltage. If the cell was recently charged or discharged, the voltage measured by the IC might not represent the true state-of-charge of the cell resulting in initial error in the fuel gauge outputs. In most cases, this error is minor and is quickly removed by the fuel gauge algorithm during the first hour of normal operation.

Cycle+ Age Forecasting

A special feature of the ModelGauge m5 EZ algorithm is the ability to forecast the number of cycles the cell lasts before its end-of-life. This allows an application to adjust a cell's charge profile over time to meet the cycle life requirements of the cell (see Figure 24). The algorithm monitors the change in cell capacity over time and calculates the number of cycles it takes for the cell's capacity to drop to a predefined threshold of 85% of the original. Remaining cycles below 85% of the original capacity are unpredictable and not managed by age forecasting.

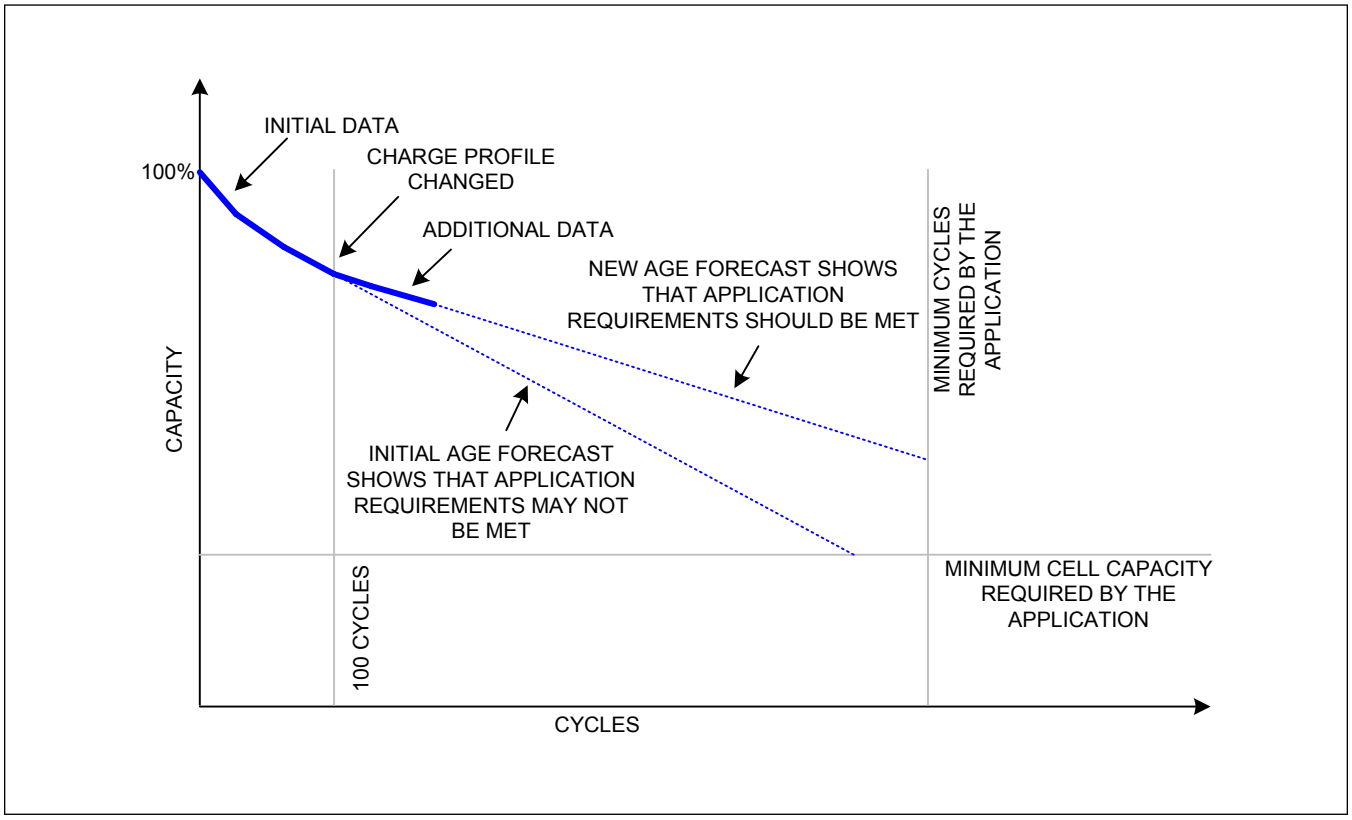


Figure 24. Benefits of Age Forecasting

nAgeFcCfg Register (1E2h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nAgeFcCfg register is used to configure age forecasting functionality. Register data is nonvolatile and is typically configured only once during pack assembly. Table 61 shows the register format.

Table 61. nAgeFcCfg Register (1E2h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DeadTargetRatio				CycleStart							0	0	0	1	1

DeadTargetRatio: Sets the remaining percentage of initial cell capacity where the cell is considered fully aged. DeadTargetRatio can be adjusted between 75% and 86.72% with an LSb of 0.7813%. For example, if age forecasting was configured to estimate the number of cycles until the cell's capacity dropped to 85.1574% of when it was new, DeadTargetRatio should be programmed to 1101b.

CycleStart: Sets the number of cell cycles before age forecasting calculations begin. CycleStart has a range of 0.00

to 81.92 cycles with an LSb of 0.64 cycles. Since age forecasting estimation becomes more accurate over time, most applications use a default value of 30 cycles.

0: Always write this location 0.

1: Always write this location 1.

AgeForecast Register (0B9h)

Register Type: Special

Nonvolatile Backup: None

The AgeForecast register displays the estimated cycle life of the application cell. The AgeForecast value should be compared against the Cycles (017h) register to determine the estimated number of remaining cell cycles. This is accomplished by accumulating the capacity loss per cycle as the cell ages. The result becomes more accurate with each cycle measured. The AgeForecast register has a full range of 0 cycles to 10485 cycles with a 0.16 cycle LSb. This register is recalculated from learned information at power-up.

Age Forecasting Requirements

There are several requirements for proper operation of the age forecasting feature as follows:

1. There is a minimum and maximum cell size that the age forecasting algorithm can handle. Table 62 shows the allowable range of cell sizes that can be accurately age forecasted depending on the size of the sense resistor used in the application. Note this range is different from the current and capacity measurement range for a given sense resistor. See the *Current Measurement* section for details.

Table 62. Minimum and Maximum Cell Sizes for Age Forecasting

SENSE RESISTOR (Ω)	MINIMUM CELL SIZE FOR FORECASTING (mAh)	MAXIMUM CELL SIZE FOR FORECASTING (mAh)
0.005	1600	5000
0.010	800	2500
0.020	400	1250

2. Age forecasting requires a minimum of 100 cycles before achieving reasonable predictions. Ignore the age forecasting output until then.

3. Age forecasting requires a custom characterized battery model to be used by the IC. Age forecasting is not valid when using the default model.

Enabling Age Forecasting

The following steps are required to enable the Age Forecasting feature:

1. Set nNVCfg2.enVT = 0. This function conflicts with age forecasting and must be disabled.
2. Set nFullCapFltr (Register 1AEh) to the value of nFullCapNom.
3. Set nVoltTemp (Register 1AAh) to 0x0001.
4. Set nNVCfg0.enAF = 1 to begin operation.

Battery Life Logging

The MAX17332 can log learned battery information, providing the host with a history of conditions experienced by the cell pack over its lifetime. The IC can store up to 100 snapshots of page 1Ah in nonvolatile memory. Individual registers from page 1Ah are summarized in Table 63. Their nonvolatile backup must be enabled and LOCK1 unlocked in order for logging to occur. See each register's detailed description in other sections of this data sheet. The logging rate follows the "Fibonacci Saving" interval to provide recurring log-saving according to the expected battery lifespan and is configured by nNVCFG2.FibMax and nNVCFG2.FibScl. See the *100 Record Life Logging* section for more details.

Table 63. Life Logging Register Summary

REGISTER ADDRESS	REGISTER NAME	FUNCTION
1A0h	nQRTable00	Learned characterization information used to determine when the cell pack is empty under application conditions.
1A1h	nQRTable10	
1A2h	nQRTable20	
1A3h	nQRTable30	
1A4h	nCycles	Total number of equivalent full cycles seen by the cell since assembly.
1A5h	nFullCapNom	Calculated capacity of the cell independent of application conditions.
1A6h	nRComp0	Learned characterization information related to the voltage fuel gauge.
1A7h	nTempCo	
1A8h	nBattStatus	Contains the permanent battery status information.
1A9h	nFullCapRep	Calculated capacity of the cell under present application conditions.
1AAh	nVoltTemp	The average voltage and temperature seen by the IC at the instance of learned data backup. If Age Forecasting is enabled, this register contains different information.
1ABh	nMaxMinCurr	Maximum and minimum current, voltage, and temperature seen by the IC during this logging window.
1ACh	nMaxMinVolt	
1ADh	nMaxMinTemp	
1AEh	nFaultLog/ nFullCapFltr	If Fault Logging is enabled, this register contains a history of any faults that have occurred during this life segment. If Age Forecasting is enabled, this register contains a highly filtered nFullCapNom.
1AFh	nTimerH	Total elapsed time since cell pack assembly, not including time spent in shutdown mode.

Life Logging Data Example

Figure 25 shows a graphical representation of sample history data read from an IC. Analysis of this data can provide information of cell performance over its lifetime as well as detect any application anomalies that may have affected performance.

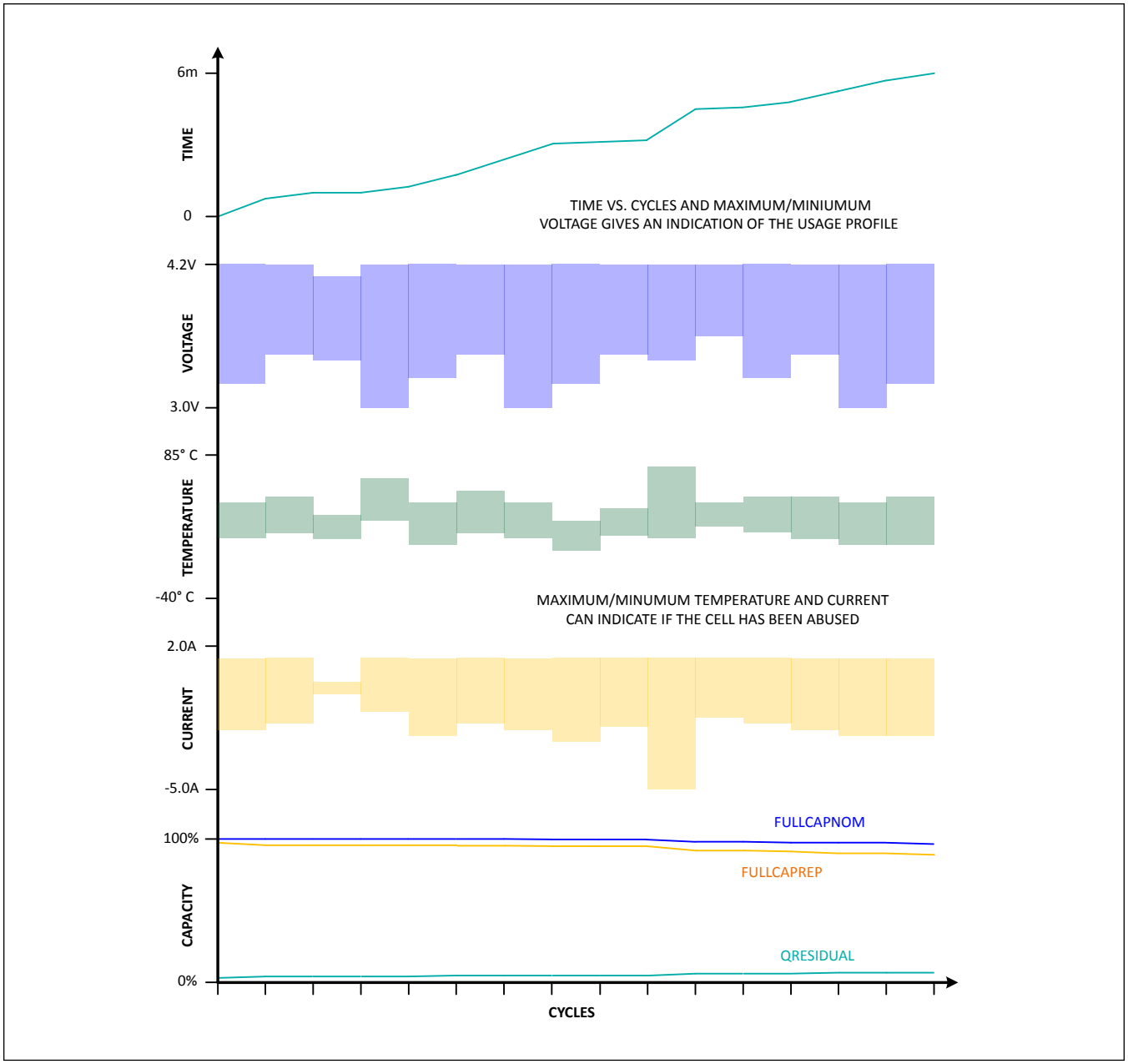


Figure 25. Sample Life Logging Data

Determining Number of Valid Logging Entries

While logging data, the IC begins on history page 1 and continues until all history memory has been used at page 100. Prior to reading history information out of the IC, the host must determine which history pages have been written and which, if any, have write errors and should be ignored. Each page of history information has two associated write flags that indicate if the page has been written and two associated valid flags which indicate if the write was successful. The HISTORY RECALL command [0xE2XX] is used to load the history flags into page 1Fh of IC memory where the host can then read their state. Table 64 shows which command and which page 1Fh address has the flag information for a given history page. For example, to see the write flag information of history pages 1-8, send the 0xE29C command then read address 1F2h. To see the **valid flag** information of pages 1-8, send the 0xE29C command and then read address 1FFh.

Table 64. Reading History Page Flags

ASSOCIATED HISTORY PAGES	COMMAND TO RECALL WRITE FLAGS	WRITE FLAG ADDRESS	COMMAND TO RECALL VALID FLAGS	VALID FLAG ADDRESS
1-8	0xE29C	1F2h	0xE29C	1FFh
9-16		1F3h	0xE29D	1F0h
17-24		1F4h		1F1h
25-32		1F5h		1F2h
33-40		1F6h		1F3h
41-48		1F7h		1F4h
49-56		1F8h		1F5h
57-64		1F9h		1F6h
65-72		1FAh		1F7h
73-80		1FBh		1F8h
81-88		1FCh		1F9h
89-96		1FDh		1FAh
97-100		1FEh		1FBh

Once the write flag and valid flag information is read from the IC, it must be decoded. Each register holds two flags for a given history page. Figure 26 shows the register format. The flags for a given history page are always spaced 8-bits apart from one another. For example, history page 1 flags are always located at bit positions D0 and D8, history page 84 flags are at locations D3 and D11, etc. Note that the last flag register contains information for only three pages, in this case the upper 5-bits of each byte should be ignored.

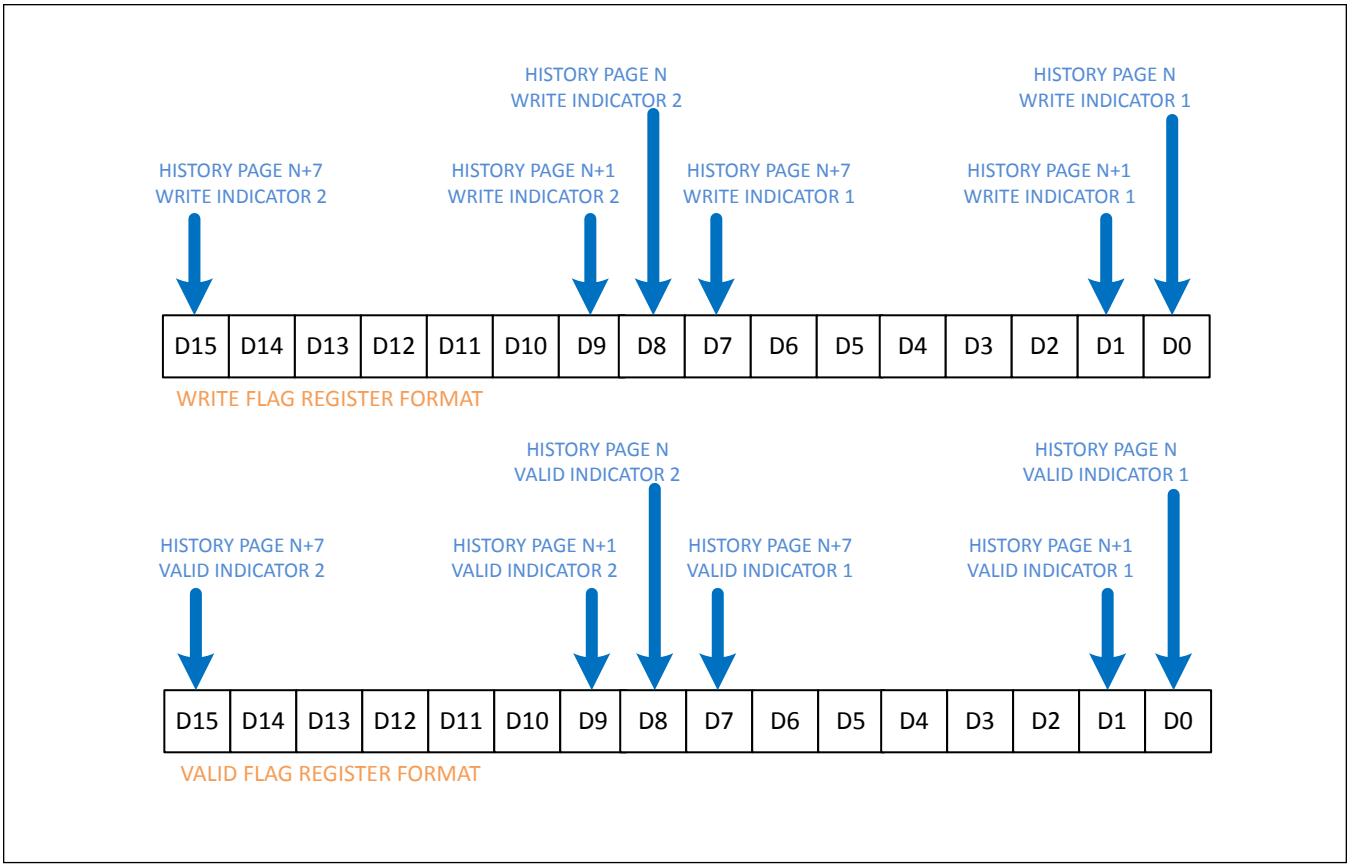


Figure 26. Write Flag Register and Valid Flag Register Formats

Once all four flags for a given history page are known, the host can determine if the history page contains valid data. If either write flag is set, then data has been written to that page by the IC. If both write flags are clear, the page has not yet been written. Due to application conditions, the write might not have been successful. Next, check the valid flags; if either valid flag is set, the data should be considered good. If both valid flags are clear, then the data should be considered bad and the host should ignore it. Table 65 shows how to decode the flags.

Table 65. Decoding History Page Flags

WRITE INDICATOR 1	WRITE INDICATOR 2	VALID INDICATOR 1	VALID INDICATOR 2	PAGE STATUS
0	0	X	X	Page empty.
1	X	0	0	Write failure. Page has invalid data.
		1	X	Write success. Page has valid data.
		X	1	
X	1	0	0	Write failure. Page has invalid data.
		1	X	Write success. Page has valid data.
		X	1	

Reading History Data

Once all pages of valid history data have been identified, they can be read from the IC using the HISTORY RECALL command. Table 66 shows the command and history page relationship. After sending the command, wait t_{RECALL} then read the history data from IC page 1Fh. Each page of history data has the same format as page 1Ah. For example, nCycles is found at address 1A4h and nCycles history are at 1F4h, nTimerH is located at address 1AFh, and nTimerH history is located at address 1FFh, etc.

Table 66. Reading History Data

COMMAND	HISTORY PAGE RECALLED TO PAGE 1EH
0xE22E	Page 1
0xE22F	Page 2
...	...
0xE291	Page 100

History Data Reading Example

The host would like to read the life logging data from a given IC. The host must first determine how many history pages have been written and if there are any errors. To start checking history page 1, the host sends 0xE29C to the command register, wait t_{RECALL}, then read location 1F2h. If either the D0 or the D8 bit in the read data word is a logic 1, the host knows that history page 1 contains history data. The host can then check page 2 (bits D1 and D9) up to page 7 (bits D7 and D15). The host continues to pages 8 to 16 by reading location 1F3h and then repeating individual bit testing. This process is repeated for each command and address listed in Table 64 until the host finds a history page where both write flags read logic 0. This is the first unwritten page. All previous pages contain data, all following pages are empty.

The host must now determine which, if any, of the history pages have bad data and must be ignored. The above process is repeated for every location looking at the valid flags instead of the write flags. Any history page where both valid flags read logic 0 is considered bad due to a write failure and that page should be ignored. Once the host has a complete list of valid written history pages, commands 0xE22E to 0xE291 can be used to read the history information from page 1Fh for processing.

Note that this example was simplified to describe the procedure. A more efficient method would be for the host to send a history command once and then read all associated registers. For example, the host could send the 0xE29C command once and then read the entire memory space of 1F0h to 1FFh which would contain all write flags for pages 1 to 100 (1F2h to 1FEh) and all valid flags for pages 1 to 8 (1FFh). This applies to all 0xE2XX history commands.

See the *Appendix A: Reading History Data Pseudo-Code Example* section for a pseudo-code example of reading history data.

ModelGauge m5 EZ Algorithm Input Registers

The following registers are inputs to the ModelGauge algorithm and store characterization information for the application cells as well as important application specific specifications. They are described only briefly here. Contact Analog Devices for information regarding cell characterization.

nXTable0 (180h) to nXTable11 (18Bh) Registers

Register Type: Special

Nonvolatile Restore: There are no associated restore locations for these registers.

Cell characterization information is used by the ModelGauge algorithm to determine capacity versus operating conditions. This table comes from battery characterization data. These are nonvolatile memory locations.

nOCVTable0 (190h) to nOCVTable11 (19Bh) Registers

Register Type: Special

Nonvolatile Restore: There are no associated restore locations for these registers.

Cell characterization information is used by the ModelGauge algorithm to determine capacity versus operating conditions.

This table comes from battery characterization data. These are nonvolatile memory locations.

nQRTable00 (1A0h) to nQRTable30 (1A3h) Registers

Register Type: Special

Nonvolatile Backup and Restore: QRTable20 and QRTable30 (032h, 042h)

The nQRTable00 to nQRTable30 register locations contain characterization information regarding cell capacity that is not available under certain application conditions.

nVEmpty Register (19Eh)

Register Type: Special

Nonvolatile Restore: None

The nVempty register sets thresholds related to empty detection during operation. Table 67 shows the register format.

Table 67. nVEmpty (19Eh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VE									VR						

VE: Empty Voltage. Sets the voltage level for detecting empty. A 10mV resolution gives a 0V to 5.11V range. This value is written to 3.3V after reset if nonvolatile backup is disabled.

VR: Recovery Voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is reenabled. A 40mV resolution gives a 0V to 5.08V range. This value is written to 3.88V after reset if nonvolatile backup is disabled.

nDesignCap Register(1B3h)

Register Type: Capacity

Factory Default Value: 2A83h

Nonvolatile Restore: DesignCap (018h)

The nDesignCap register holds the expected capacity of the cell, VScale, and QScale values. The DesignCap value is used to determine age and health of the cell by comparing against the measured present cell capacity. The VScale value determines the center voltage and stepsize for calculating the charging voltage. The QScale value determines the Center Voltage (4.2V or 3.7V) and the step size (5mV or 10mV).

Table 68. nDesignCap Register (1B3h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DesignCap										Reserved		Vscale	Qscale		

Vscale: VScale sets the CenterVoltage and StepSize used for calculating the ChargingVoltage as shown in Table 69. The VScale StepSize applies to only to the charging voltage and not to other voltage thersholds. See the *nVChgCfg1 and nVChgcfg2 Registers* for more details on calculating the charging voltage at the various temperature regions.

Table 69. VScale Center Voltage and StepSize Options

VScale SETTING	CenterVoltage (V)	StepSize (mV)
0	4.2	5
1	3.7	10

Qscale: QScale sets the StepSize for calculating the ChargingCurrent and DesignCap and is scaled by the sense resistor as shown in Table 70. The QScale StepSize applies to only to the ChargingCurrent and the DesignCap and does not apply to other current thresholds or capacities. See the *nIChgCfg1 and nIChgCfg2* registers for more details on calculating the charging current at the various temperature regions.

Table 70. QScale StepSize Options

QScale SETTING	CURRENT StepSize (mA)	CAPACITY StepSize (mAH)

Table 70. QScale StepSize Options (continued)

0	2.5 x (10/R_{SENSE})	1.25 x (10/R_{SENSE})
1	5 x (10/R_{SENSE})	2.5 x (10/R_{SENSE})
2	10 x (10/R_{SENSE})	5.0 x (10/R_{SENSE})
3	20 x (10/R_{SENSE})	10.0 x (10/R_{SENSE})
4	25 x (10/R_{SENSE})	12.5 x (10/R_{SENSE})
5	40 x (10/R_{SENSE})	20.0 x (10/R_{SENSE})
6	50 x (10/R_{SENSE})	25.0 x (10/R_{SENSE})
7	100 x (10/R_{SENSE})	50.0 x (10/R_{SENSE})

DesignCap: DesignCap is calculated based on the QScale setting to determing the StepSize.

DesignCapacity = DesignCap x QScale.CapacityStepSize.

For example, the factory default setting of 2A83h provides:

VScale = 0 --> CenterVoltage = 4.2V, StepSize = 5mV

QScale = 3 --> CurrentStepSize = 20mA, CapacityStepSize = 10mAH

DesignCap = 170

DesignCapacity = 170 x 10mAH = 1700mAH

nRComp0 Register (1A6h)

Register Type: Special

Nonvolatile Restore: RComp0 (038h)

The nRComp0 register holds characterization information critical to computing the open circuit voltage of a cell under loaded conditions.

nTempCo Register (1A7h)

Register Type: Special

Nonvolatile Restore: TempCo (039h)

The nTempCo register holds temperature compensation information for the nRComp0 register value.

ModelGauge m5 EZ Algorithm Configuration Registers

The following registers allow operation of the ModelGauge m5 EZ algorithm to be adjusted for the application. It is recommended that the default values for these registers be used.

nFilterCfg Register (19Dh)

Register Type: Special

Nonvolatile Restore: FilterCfg (029h) if nNVCfg0.enFCfg is set.

Alternate Initial Value: 0x0EA4

The nFilterCfg register sets the averaging time period for all A/D readings, for mixing OCV results, and coulomb count results. It is recommended that these values are not changed unless required by the application. Table 71 shows the nFilterCfg register format.

Table 71. FilterCfg (029h)/nFilterCfg (19Dh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	TEMP			MIX				VOLT			CURR			

CURR: Sets the time constant for the AvgCurrent register. The default POR value of 0100b gives a time constant of 5.625s. The equation setting the period is:

AvgCurrent time constant = 45s x $2^{(CURR-7)}$

VOLT: Sets the time constant for the AvgVCell register. The default POR value of 010b gives a time constant of 45s. The equation setting the period is:

AvgVCell time constant = 45s x $2^{(VOLT-2)}$

MIX: Sets the time constant for the mixing algorithm. The default POR value of 1101b gives a time constant of 12.8 hours. The equation setting the period is:

Mixing Period = 45s x $2^{(MIX-3)}$

TEMP: Sets the time constant for the AvgTA register. The default POR value of 0001b gives a time constant of 1.5 minutes. The equation setting the period is:

AvgTA time constant = 45s x 2^{TEMP}

0: Write these bits to 0.

nRelaxCfg Register (1B6h)

Register Type: Special

Nonvolatile Restore: RelaxCfg (0A0h) if nNVCfg0.enRCfg is set.

Alternate Initial Value: 0x2039

The nRelaxCfg register defines how the IC detects if the cell is in a relaxed state. See Figure 27. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time (dV/dt) shows little or no change. If AvgCurrent remains below the LOAD threshold while VCell changes less than the dV threshold over two consecutive periods of dt, the cell is considered relaxed. Table 72 shows the nRelaxCfg register format.

Table 72. RelaxCfg (0A0h)/nRelaxCfg (1B6h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LOAD							dV					dt			

LOAD: Sets the threshold, which the AvgCurrent register is compared against. The AvgCurrent register must remain below this threshold value for the cell to be considered unloaded. Load is an unsigned 7-bit value where 1 LSb = 50µV. The default value is 800µV.

dV: Sets the threshold, which VCell is compared against. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed; dV has a range of 0mV to 40mV where 1 LSb = 1.25mV. The default value is 3.75mV.

dt: Sets the time period over which change in VCell is compared against dV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed. The default value is 1.5 minutes. The comparison period is calculated as:

Relaxation period = $2^{(dt-8)}$ x 45s

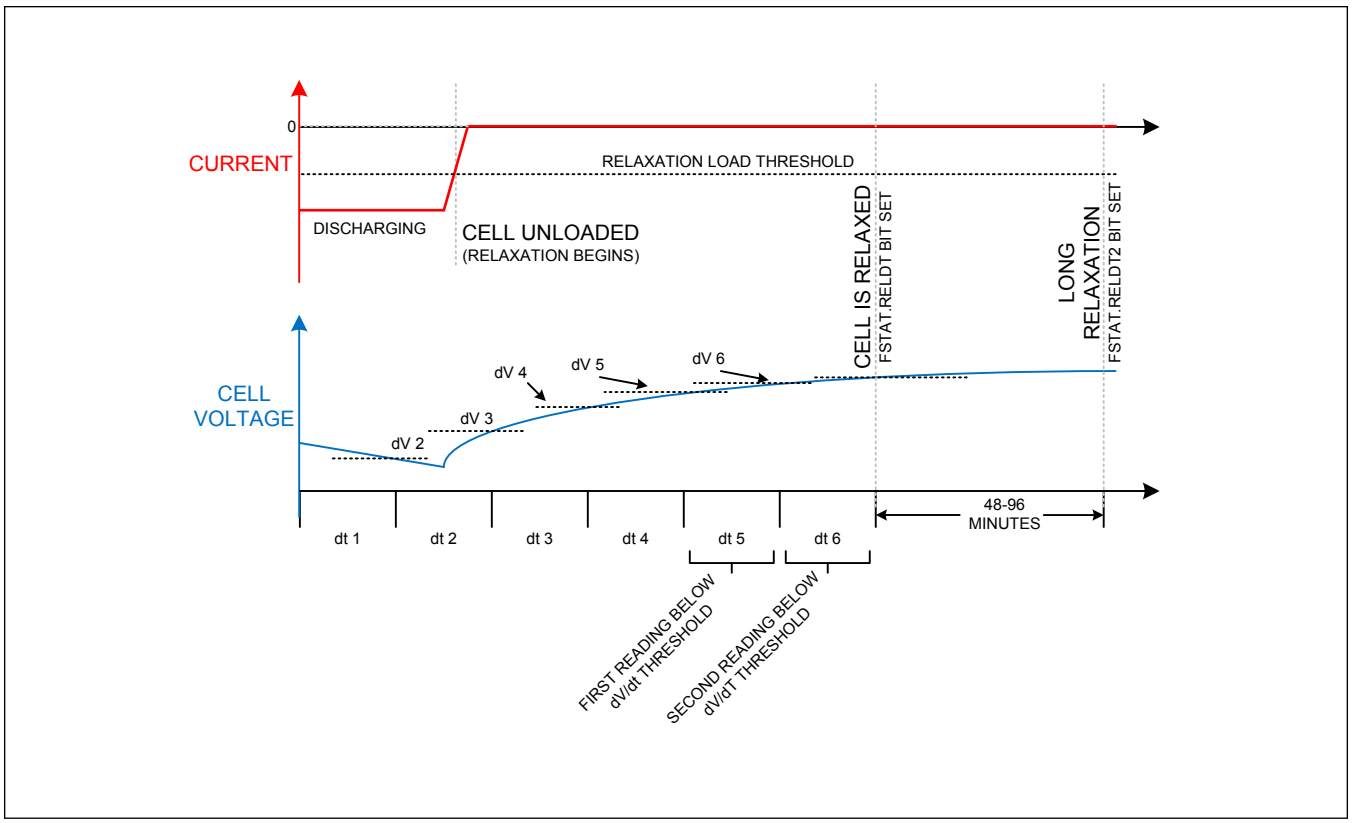


Figure 27. Cell Relaxation Detection

nConvgCfg Register (1B7h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nConvgCfg register configures operation of the converge-to-empty feature. The recommended value for nConvgCfg is 0x2241. Table 73 shows the nConvgCfg register format. Set nConvgCfg = 0x0000 to disable the converge-to-empty functionality.

Table 73. nConvgCfg Register (1B7h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RepLow				VoltLowOff					MinSlopeX				RepL_per_stage		

RepL_per_stage: Adjusts the RepLow threshold setting depending on the present learn stage using the following equation. This allows the RepLow threshold to be at higher levels for earlier learn states. RepL_per_stage has an LSb of 1% which gives a range of 0% to 7%.

RepLow Threshold = RepLow Field Setting + RemainingStages x RepL_per_stage

MinSlopeX: Sets the amount of slope-shallowing which occurs when *RepSOC* falls below RepLow. MinSlopeX LSb corresponds to a ratio of 1/16 which gives a full range of 0 to 15/16.

VoltLowOff: When the *AvgVCell* register value drops below the VoltLow threshold, *RepCap* begins to bend downwards by a ratio defined by the following equation. VoltLowOff has an LSb of 20mV which gives a range of 0mV to 620mV.

RepCap = (*AvgVCell* - *nVEmpty*)/VoltLowOff

RepLow: Sets the threshold below which *RepCap* begins to bend upwards. The RepLow field LSb is 2% giving a full-scale range from 0% to 30%.

nRippleCfg Register (1B1h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nRippleCfg register configures ripple measurement and ripple compensation. The recommended value for this register is 0x0204. Table 74 shows the register format.

Table 74. nRippleCfg Register (1B1h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
kDV													NR		

NR: Sets the filter magnitude for ripple observation as defined by the following equation giving a range of 1.4 seconds to 180 seconds.

Ripple Time Range = 1.4 seconds x 2^{NR}

kDV: Sets the corresponding amount of capacity to compensate proportional to the ripple.

nMiscCfg Register (1B2h)

Register Type: Special

Nonvolatile Restore: MiscCfg (00Fh) if nNVCfg0.enMC is set.

Alternate Initial Value: 0x3070

The nMiscCfg control register enables various other functions of the device. The nMiscCfg register default values should not be changed unless specifically required by the application. Table 75 shows the register format.

Table 75. MiscCfg (00Fh)/nMiscCfg (1B2h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FUS				0	0	MR					1	0	0	SACFG	

0: Bit must be written 0. Do not write 1.

1: Bit must be written 1. Do not write 0.

SACFG: SOC Alert Config. SOC Alerts can be generated by monitoring any of the SOC registers as follows. SACFG defaults to 00 at power-up:

0 0 SOC Alerts are generated based on the RepSOC register.

0 1 SOC Alerts are generated based on the AvSOC register.

1 0 SOC Alerts are generated based on the MixSOC register.

1 1 SOC Alerts are generated based on the VFSOC register.

MR: Mixing Rate. This value sets the strength of the servo mixing rate after the final mixing state has been reached (greater than 2.08 complete cycles). The units are MR0 = 6.25µV, giving a range up to 19.375mA with a standard 10mΩ sense resistor. Setting this value to 00000b disables servo mixing and the IC continues with time-constant mixing indefinitely. The default setting is 18.75µV or 1.875mA with a standard sense resistor.

FUS: Full Update Slope. This field prevents jumps in the RepSOC and FullCapRep registers by setting the rate of adjustment of FullCapRep near the end of a charge cycle. The update slope adjustment range is from 2% per 15 minutes (0000b) to a maximum of 32% per 15 minutes (1111b).

ModelGauge m5 EZ Algorithm Additional Registers

The following registers contain intermediate ModelGauge m5 data which can be useful for debugging or performance analysis. The values in these registers are initialized to 480ms after the IC is reset.

Timer Register (03Eh)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0000

This register holds timing information for the fuel gauge. It is available to the user for debugging purposes. The Timer register LSb is equal to 175.8ms which gives a full-scale range of 0 hours to 3.2 hours.

dQAcc Register (045h)

Register Type: Capacity (2mAh/LSB)

Nonvolatile Backup: Translated from nFullCapNom

Alternate Initial Value: 0x0017 (368mAh)

This register tracks change in battery charge between relaxation points. It is available to the user for debugging purposes.

dPAcc Register (046h)

Register Type: Percentage (1/16% per LSB)

Nonvolatile Backup: None

Initial Value: 0x0190 (25%)

This register tracks change in battery state-of-charge between relaxation points. It is available to the user for debugging purposes.

QResidual Register (00Ch)

Register Type: Capacity

Nonvolatile Backup: None

The QResidual register displays the calculated amount of charge in milliamp-hours that is presently inside of (but cannot be removed from) the cell under present application conditions. This value is subtracted from the MixCap value to determine the capacity available to the user under present conditions (AvCap).

VFSOC Register (0FFh)

Register Type: Percentage

Nonvolatile Backup: None

The VFSOC register holds the calculated present state-of-charge of the battery according to the voltage fuel gauge.

VFOCV Register (0FBh)

Register Type: Voltage

Nonvolatile Backup: None

The VFOCV register contains the calculated open-circuit voltage of the cell as determined by the voltage fuel gauge. This value is used in other internal calculations.

QH Register (4Dh)

Register Type: Capacity

Nonvolatile Backup: None

Alternate Initial Value: 0x0000

The QH register displays the raw coulomb count generated by the device. This register is used internally as an input to the mixing algorithm. Monitoring changes in QH over time can be useful for debugging device operation.

AvCap Register (01Fh)

Register Type: Capacity

Nonvolatile Backup: None

The AvCap register holds the calculated available capacity of the cell pack based on all inputs from the ModelGauge m5 EZ algorithm including empty compensation. The register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application such as abrupt changes in load current or temperature. See the *Fuel-Gauge*

Empty Compensation section for details.

AvSOC Register (00Eh)

Register Type: Percentage

Nonvolatile Backup: None

The AvSOC register holds the calculated available state-of-charge of the cell based on all inputs from the ModelGauge m5 EZ algorithm including empty compensation. The AvSOC percentage corresponds with *AvCap* and *FullCapNom*. The AvSOC register value is an unfiltered calculation. Jumps in the reported value can be caused by changes in the application such as abrupt changes in load current or temperature. See the *Fuel-Gauge Empty Compensation* section for details.

MixSOC Register (00Dh)

Register Type: Percentage

Nonvolatile Backup: None

The MixSOC register holds the calculated present state-of-charge of the cell before any empty compensation adjustments are performed. MixSOC corresponds with *MixCap* and *FullCapNom*. See the *Fuel-Gauge Empty Compensation* section for details.

MixCap Register (02Bh)

Register Type: Capacity

Nonvolatile Backup: None

The MixCap register holds the calculated remaining capacity of the cell before any empty compensation adjustments are performed. See the *Fuel-Gauge Empty Compensation* section for details.

VFRemCap Register (04Ah)

Register Type: Capacity

Nonvolatile Backup: None

The VFRemCap register holds the remaining capacity of the cell as determined by the voltage fuel gauge before any empty compensation adjustments are performed. See the *Fuel-Gauge Empty Compensation* section for details.

SOCHold Register (0D0h)

Register Type: Special

The SOCHold register configures operation of the hold-before-empty feature and also the enable bit for 99% hold during charge. The default value for SOCHold is 0x1002. Table 76 shows the SOCHold register format.

Table 76. SOCHold (0D0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	99%HoldEn	EmptyVoltHold							EmptySocHold				

EmptyVoltHold: The positive voltage offset that is added to VEmpty. Empty detection/learning occurs at the point that VCell = VEmpty + EmptyVoltHold. EmptyVoltHold has an LSb of 10mV which gives a range of 0mV to 1270mV.

EmptySocHold: It is the threshold at which RepSOC is held constant. After empty detection/learning occurs, the RepSOC update continues as expected. EmptySocHold has an LSb of 0.5% which gives it a full range of 0% to 15.5%.

99%HoldEn: Enable bit for 99% hold feature during charging. When enabled, RepSOC holds a maximum value of 99% until Full Qualified is reached.

FStat Register (03Dh)

Register Type: Special

Nonvolatile Backup: None

The FStat register is a read-only register that monitors the status of the ModelGauge algorithm. Do not write to this

register location. Table 77 is the FStat register format.

Table 77. FStat Register (03Dh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	RelDt	EDet	FQ	RelDt2	X	X	X	X	X	DNR

DNR: Data Not Ready. This bit is set to 1 at cell insertion and remains set until the output registers have been updated. Afterwards, the IC clears this bit indicating the fuel gauge calculations are now up to date. This takes between 445ms and 1.845s depending on whether the IC was in a powered state prior to the cell-insertion event.

RelDt2: Long Relaxation. This bit is set to 1 whenever the ModelGauge m5 EZ algorithm detects that the cell has been relaxed for a period of 48 to 96 minutes or longer. This bit is cleared to 0 whenever the cell is no longer in a relaxed state. See Figure 31.

FQ: Full Qualified. This bit is set when all charge termination conditions have been met. See the *End-of-Charge* section for details.

EDet: Empty Detection. This bit is set to 1 when the IC detects that the cell empty point has been reached. This bit is reset to 0 when the cell voltage rises above the recovery threshold. See the *nVEmpty* register for details.

RelDt: Relaxed Cell Detection. This bit is set to a 1 whenever the ModelGauge m5 EZ algorithm detects that the cell is in a fully relaxed state. This bit is cleared to 0 whenever a current greater than the load threshold is detected. See Figure 31.

X: Don't Care. This bit is undefined and can be logic 0 or 1.

nLearnCfg (19Fh) Register

Register Type: Special

Nonvolatile Restore: LearnCfg (0A1h) if nNVCfg0.enLCfg is set.

Alternate Initial Value: 0x4686

The nLearnCfg register controls all functions relating to adaptation during operation. Table 78 shows the register format.

Table 78. LearnCfg (0A1h)/nLearnCfg (19Fh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	1	LS			0	1	1	0

0: Bit must be written 0. Do not write 1 unless guided by Maxim.

1: Bit must be written 1. Do not write 0 unless guided by Maxim.

LS: Learn Stage. The Learn Stage value controls the influence of the voltage fuel gauge on the mixing algorithm. The Learn Stage defaults to 0h, making the voltage fuel gauge dominate. The Learn Stage then advances to 7h over the course of two full cell cycles to make the coulomb counter dominate. The host software can write the Learn Stage value to 7h to advance to the final stage at any time. Writing any value between 1h and 6h is ignored.

Memory

The memory space of the MAX17332 is divided into 32 pages, each containing 16 registers where each register is 16-bits wide. Registers are addressed using an internal 9-bit range of 000h to 1FFh. Externally, registers are accessed with an 8-bit address for 2-wire communication. Registers are grouped by functional block. See the functional descriptions for details of each register's functionality. Certain memory blocks can be permanently locked to prevent accidental overwrite, see the *Locking Memory Blocks* section for details. Table 79 shows the full memory map of the IC. Note that some individual user registers are located on RESERVED memory pages. These locations can be accessed normally while the remainder of the page is considered RESERVED. Memory locations listed as RESERVED should never be written to. Data read from RESERVED locations are not defined.

Table 79. Top Level Memory Map

REGISTER PAGE	LOCK	DESCRIPTION	2-WIRE SLAVE ADDRESS (8-BIT)	2-WIRE PROTOCOL	2-WIRE EXTERNAL ADDRESS RANGE

Table 79. Top Level Memory Map (continued)

00h	—	MODELGAUGE m5 EZ DATA BLOCK	6Ch	I²C	00h-4Fh
01h-04h	LOCK2				
05h-0Ah		RESERVED			
0Bh	LOCK2	MODELGAUGE m5 EZ DATA BLOCK (continued)	6Ch	I²C	B0h-BFh
0Ch	SHA	SHA MEMORY	6Ch	I²C	C0h-CFh
0Dh	LOCK2	MODELGAUGE m5 EZ DATA BLOCK (continued)	6Ch	I²C	D0h-DFh
0Eh-0Fh	—	RESERVED	—	—	—
10h-17h	—	SBS DATA BLOCK	16h	SBS	00h-7Fh
18h-19h	LOCK3	MODELGAUGE m5 EZ NONVOLATILE MEMORY BLOCK	16h	I²C	80h-EFh
1Ah-1Bh	LOCK1	LIFE LOGGING and CONFIGURATION NONVOLATILE MEMORY BLOCK			
1Ch	LOCK4	CONFIGURATION NONVOLATILE MEMORY BLOCK			
1Dh	LOCK5	CHARGING AND PROTECTION NONVOLATILE MEMORY BLOCK			
1Eh	LOCK1	USER and SBS NONVOLATILE MEMORY BLOCK			
1Fh	—	NONVOLATILE HISTORY	16h	I²C	F0h-FFh

Table 80. Individual Registers

REGISTER ADDRESS	LOCK	DESCRIPTION	2-WIRE SLAVE ADDRESS	2-WIRE PROTOCOL	2-WIRE EXTERNAL ADDRESS RANGE
060h	—	Command REGISTER	6Ch	I²C	60h
061h	—	CommStat REGISTER	6Ch	I²C	61h
07Fh	—	Lock REGISTER	6Ch	I²C	7Fh

ModelGauge m5 EZ Memory Space

Registers that relate to the functionality of the ModelGauge m5 EZ fuel gauge are located on pages 00h-04h and are continued on pages 0Bh and 0Dh. See the *ModelGauge m5 EZ Algorithm* section for details of specific register operation. These locations (other than page 00h) can be permanently locked by setting LOCK2. Register locations shown in gray are reserved locations and should not be written to. See Table 81.

Table 81. ModelGauge m5 EZ Register Memory Map

PAGE/ WORD	00XH	01XH	02XH	03XH	04XH	0AXH	0BXH	0DXH
0h	Status	FullCapRep	TTF	Reserved	AvgDieTemp	RelaxCfg	Status2	SOCHold
1h	VAlrtTh	TTE	DevName	Reserved	Reserved	LearnCfg	Power	Reserved
2h	TAlrtTh	VCellRep	CurrRep	QRTable20	QRTable30	Reserved	VRipple	Reserved
3h	SAlrtTh	FullSocThr	FullCapNom	Reserved	Reserved	ChgStat	AvgPower	Reserved
4h	AtRate	RCell	Reserved	DieTemp	Reserved	MaxPeakPower	Reserved	AvgCell1
5h	RepCap	FETTemp	Reserved	FullCap	dQAcc	SusPeakPower	TTFCfg	Reserved
6h	RepSOC	AvgTA	Reserved	IAvgEmpty	dPAcc	PackResistance	CVMixCap	Reserved

Table 81. ModelGauge m5 EZ Register Memory Map (continued)

PAGE/ WORD	00XH	01XH	02XH	03XH	04XH	0AXH	0BXH	0DXH
7h	Age	Cycles	Reserved	Reserved	Reserved	SysResistance	CVHalfTime	Batt
8h	MaxMinVolt	DesignCap	Charging Current	Reserved	Reserved	MinSysVoltage	CGTempCo	Cell1
9h	MaxMinTemp	AvgVCell	FilterCfg	FStat2	ProtTmrStat	MPPCurrent	AgeForecast	ProtStatus
Ah	MaxMinCurr	VCell	Charging Voltage	Reserved	VFRemCap	SPPCurrent	Reserved	FProtStat
Bh	Config	Temp	MixCap	Reserved	Reserved	Config2	FOTPSTAT	PCKP
Ch	QResidual	Current	Reserved	Reserved	Reserved	IAlrtTh	Reserved	AtQResidual
Dh	MixSOC	AvgCurrent	Reserved	FStat	QH	MinVolt	Reserved	AtTTE
Eh	AvSOC	IChgTerm	Reserved	Timer	QL	MinCurr	TimerH	AtAvSOC
Fh	MiscCfg	AvCap	Reserved	Reserved	Reserved	ProtAlrt	Reserved	AtAvCap

Nonvolatile Memory

Nonvolatile Memory Map

Certain ModelGauge m5 and device configuration values are stored in nonvolatile memory to prevent data loss if the IC loses power. The MAX17332 internally updates page 1Ah values over time based on actual performance of the ModelGauge m5 algorithm. The host system does not need to access this memory space during operation. Nonvolatile data from other accessible register locations is internally mirrored into the nonvolatile memory block automatically. Note that non-volatile memory has a limited number of writes. User accessible configuration memory is limited to seven writes. Internal and external updates to page 1Ah as the fuel gauge algorithm learns are limited to 100 writes. Do not exceed these write limits. Table 82 shows the nonvolatile memory register map.

Table 82. Nonvolatile Register Memory Map (Slave Address 0x16)

PAGE/ WORD	18XH	19XH	1AXH[1]	1BXH	1CXH	1DXH	1EXH
0h	nXTable0	nOCVTable0	nQRTable00	nConfig	nChgCtrl1	nUVPrtTh	UserMemory_1E0
1h	nXTable1	nOCVTable1	nQRTable10	nRippleCfg	nIChgTerm	nTPrtTh1	nScOcvLim
2h	nXTable2	nOCVTable2	nQRTable20	nMiscCfg	nChgCfg0	nTPrtTh3	nAgeFcCfg
3h	nXTable3	nOCVTable3	nQRTable30	nDesignCap	nChgCtrl0	nIPrtTh1	nDesignVoltage
4h	nXTable4	nOCVTable4	nCycles	nI2CCfg	nStepCurr	nIPrtTh2	nChgCfg2
5h	nXTable5	nOCVTable5	nFullCapNom	nFullCfg	nStepVolt	nTPrtTh2	nPackResistance
6h	nXTable6	nOCVTable6	nRComp0	nRelaxCfg	UserMemory_1C6	nProtMiscTh	nManfctrDate
7h	nXTable7	nOCVTable7	nTempCo	nConvgCfg	nPackCfg	nProtCfg	nFirstUsed
8h	nXTable8	nOCVTable8	nBattStatus	nRGain	nCGain	nNVCfg0	nSerialNumber0
9h	nXTable9	nOCVTable9	nFullCapRep	nAgeChgCfg	nADCCfg	nNVCfg1	nSerialNumber1
Ah	nXTable10	nOCVTable10	nVoltTemp	nTTFCfg	nThermCfg	nOVPrtTh	nSerialNumber2
Bh	nXTable11	nOCVTable11	nMaxMinCurr	nHibCfg	nChgCfg1	nNVCfg2	nDeviceName0
Ch	nVAlrtTh	nRsense	nMaxMinVolt	nROMID0[2]	nVChgCfg1	nDelayCfg	nDeviceName1
Dh	nTAlrtTh	nFilterCfg	nMaxMinTemp	nROMID1[2]	nVChgCfg2	nODSCTh	nManfctrName0
Eh	nIAlrtTh	nVEmpty	nFaultLog/ nFullCapFltr	nROMID2[2]	nIChgCfg1	nODSCCfg	nManfctrName1
Fh	nSAlrtTh	nLearnCfg	nTimerH	nROMID3[2]	nIChgCfg2	nProtCfg2	nManfctrName2

1. Locations 1A0h to 1AFh are updated automatically by the IC each time it learns.
2. The ROM ID is unique to each IC and cannot be changed by the user.

100 Record Life Logging

Addresses 0x1A0 to 0x1AF support 100 OTP entries of learned battery characteristics and other life logging if LOCK1 is unlocked. The save interval is managed automatically using a Fibonacci algorithm which provides the following benefits:

1. **Lifespan autopsy/debug data** to support analysis of any aged or returned battery.
   a. **Battery Characteristic Learning/Adaptation.** FullCap (nFullCapRep, nFullCapNom), empty-compensation (nQRTable00-30), resistance (nRComp0 and nTempCo)
   b. **Permanent Failure Information** (nBattStatus)
   c. **Battery Charge/Discharge Fractional Cycle Counter** (nCycles)
   d. **23 Year Timer** (nTimerH)
   e. **Log-Interval Max/Min Voltage/Current/Temperature** (nMaxMinCurr, nMaxMinVolt, nMaxMinTemp)
   f. **Voltage/Temperature** at logging moment (nVoltTemp)
2. **Intelligently managed save-intervals**:

a. **Frequent when New**. When the battery is new, updates occur more frequently since early information learned about the battery (such as full-capacity) is more critical for overall performance.
b. **Slower with Age.** As the battery matures, the update interval slows down since changes in learned information also progress slower.
c. **Faster Updates Following Power Loss**. This limits the loss of information associated with power loss. Each time the power is lost and this learned information is restored, the rate of the next save is accelerated as shown in Table 85. This is limited to seven reset accelerations. The reset counter is also recorded (see also *nCycles* register). Most battery applications can proceed for longer than one year without interruption in power.
d. **Limitation on Slowest Interval.** Beyond a certain cycle life, the update interval remains constant.

Configure this behavior according to the expected battery lifespan using the FibMax and FibScl parameters in nNVCfg2 as follows:

Table 83. Fibonacci Configuration Settings

		FIBONACCI SCALAR—FIBSCL			
Setting		**00**	**01**	**10**	**11**
1st and 2nd Interval		0.25	0.5	1	2
Battery Cycles Record Limit	FibMax = 0	193	386	**772**	1544
	FibMax = 1	**310.5**	**621**	**1242**	2484
	FibMax = 2	**496.5**	**993**	**1986**	3972
	FibMax = 3	**795.5**	**1591**	3182	6364
	FibMax = 4	**1273.25**	2546.5	5093	10186
	FibMax = 5	2038.75	4077.5	8155	16310
	FibMax = 6	3262	6524	13048	26096
	FibMax = 7	5220	10440	20880	41760

The **bold** settings in Table 83 are the generally recommended choices, depending on preference for update interval, slowest update rates, and lifespan.

Table 84 shows the slowest update intervals associated with each configuration.

Table 84. Eventual Matured Update Interval (in battery cycles)

		FIBONACCI SCALAR—NNVCFG2.FIBSCL			
Setting		00	01	10	11
1st and 2nd Interval		0.25	0.5	1	2
Slowest Update Interval	FibMax = 0	2	4	**8**	16
	FibMax = 1	**3.25**	**6.5**	**13**	26
	FibMax = 2	**5.25**	**10.5**	**21**	42
	FibMax = 3	**8.5**	**17**	34	68
	FibMax = 4	**13.75**	27.5	55	110
	FibMax = 5	22.25	44.5	89	178
	FibMax = 6	36	72	144	288
	FibMax = 7	58.25	116.5	233	466

Table 85 illustrates the saving schedule with the most preferred configurations.

Table 85. Saving Schedule Example with the Most Preferred Configurations

EXAMPLE	CYCLE LIFE	FIB MAX	FIB SCL	SLOWEST UPDATE	1ST	2ND	3RD	4TH	5TH	6TH	7TH	8TH	9TH	10TH	11TH
1	**310.5**	1	0	3.25	0.25	0.25	0.5	0.75	1.25	2	3.25	3.25	3.25	—	—
2	**386**	0	1	4	0.5	0.5	1	1.5	2.5	4	4	4	—	—	—

Table 85. Saving Schedule Example with the Most Preferred Configurations (continued)

3	**496.5**	2	0	5.25	0.25	0.25	0.5	0.75	1.25	2	3.25	5.25	5.25	5.25	—
4	**621**	1	1	6.5	0.5	0.5	1	1.5	2.5	4	6.5	6.5	6.5	—	—
5	**772**	0	2	8	1	1	2	3	5	8	8	8	—	—	—
6	**795.5**	3	0	8.5	0.25	0.25	0.5	0.75	1.25	2	3.25	5.25	8.5	8.5	—
7	**993**	2	1	10.5	0.5	0.5	1	1.5	2.5	4	6.5	10.5	10.5	10.5	—
8	**1242**	1	2	13	1	1	2	3	5	8	13	13	13	—	—
9	**1273.25**	4	0	13.75	0.25	0.25	0.5	0.75	1.25	2	3.25	5.25	8.5	13.75	13.75

As an example for all subsequent startups, for the configuration of example 9 from Table 85:

1st startup [0.25, 0.25, 0.5, 0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

2nd startup [0.25, 0.5, 0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

3rd startup [0.5, 0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

4th startup [0.75, 1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

5th startup [1.25, 2, 3.25, 5.25, 8.5, 13.75, ...]

6th startup [2, 3.25, 5.25, 8.5, 13.75, ...]

7th startup [3.25, 5.25, 8.5, 13.75, ...]

8th startup [5.25, 8.5, 13.75, ...]

nNVCfg0 Register (1D8h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nNVCfg0 register manages nonvolatile memory backup of device and fuel gauge register RAM locations. Each bit of the nNVCfg0 register, when set, enables a given register location to be restored from a corresponding nonvolatile memory location after reset of the IC. If nonvolatile restore of a given register is not enabled, that location initializes to a default value after reset instead. See the individual register descriptions for details. The factory default value for nNVCfg0 register is 0x0702. Table 86 shows the nNVCfg0 register format.

Table 86. nNVCfg0 Register (1D8h) Format

D15	D14	D13	D12	D11	D10	D9	D8
enOCV	enX	enSHA	0	enCfg	enFCfg	enRCfg	enLCfg
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
enICT	enDP	enVE	0	enMC	enAF	0	0

enAF: Enable Age Forecasting. Set this bit to enable the Age Forecasting functionality. When this bit is clear, nAgeFcCfg can be used for general-purpose data storage. When set, nVoltTemp becomes repurposed for Age Forecasting data. When enAF is set to 1, nNVCfg2.enVT must be 0 for proper operation.

enMC: Enable MiscCfg Restore. Set this bit to enable the MiscCfg register to be restored after reset by the nMiscCfg register. When this bit is clear, MiscCfg restores with its alternate initialization value and nMiscCfg can be used for general-purpose data storage.

enVE: Enable VEmpty Restore. Set this bit to enable the VEmpty register to be restored after reset by the nVEmpty register. When this bit is clear, VEmpty restores with its alternate initialization value and nVEmpty can be used for general-purpose data storage.

enDP: Enable Dynamic Power. Set this bit to enable the Dynamic Power calculations. When this bit is set to 0, Dynamic Power calculations are disabled, and registers MaxPeakPower/SusPeakPower/MPPCurrent/SPPCurrent can be used as general-purpose memory. If enDP is set, enVE also needs to be set, and nVEmpty value needs to be valid.

enICT: Enable IChgTerm restore. Set this bit to enable the IChgTerm register to be restored after reset by the nIChgTerm register. When this bit is clear, IChgTerm restores to a value of 1/3rd of the nFullCapNom register and nIChgTerm can be used for general-purpose data storage.

enFCfg: Enable FilterCfg restore. Set this bit to enable the FilterCfg register to be restored after reset by the nFilterCfg register. When this bit is clear, FilterCfg restores with its alternate initialization value and nFilterCfg can be used for general-purpose data storage

enCfg: Enable Config and Config2 restore. Set this bit to enable the Config and Config2 registers to be restored after reset by the nConfig register. When this bit is clear, Config and Config2 restores with their alternate initialization values and nConfig can be used for general-purpose data storage.

enX: Enable XTable restore. Set this bit to enable the nXTable register locations to be used for cell characterization data. When this bit is clear, the IC uses the default cell model and all nXTable register locations can be used as general-purpose user memory.

enOCV: Enable OCVTable restore. Set this bit to enable the nOCVTable register locations to be used for cell characterization data. When this bit is clear, the IC uses the default cell model and all nOCVTable register locations can be used as general-purpose user memory.

enLCfg: Enable LearnCfg restore. Set this bit to enable the LearnCfg register to be restored after reset by the nLearnCfg register. When this bit is clear, LearnCfg restores with its alternate initialization value and nLearnCfg can be used for general-purpose data storage.

enRCfg: Enable RelaxCfg restore. Set this bit to enable the RelaxCfg register to be restored after reset by the nRelaxCfg register. When this bit is clear, RelaxCfg restores with its alternate initialization value and nRelaxCfg can be used for general-purpose data storage.

enSHA: Set to 1 to configure the MTP at address 0x1DC to 0x1DF as SHA space. Set to 0 to configure address 0x1DC to 0x1DF as user MTP.

nNVCfg1 Register (1D9h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nNVCfg1 register manages nonvolatile memory restore of device and fuel gauge register RAM locations. Each bit of the nNVCfg1 register, when set, enables a given register location to be restored from a corresponding nonvolatile memory location after reset of the IC. If nonvolatile backup of a given register is not enabled, that location initializes to a default value after reset instead. See the individual register descriptions for details. Table 87 shows the nNVCfg1 register format.

Table 87. nNVCfg1 Register (1D9h) Format

D15	D14	D13	D12	D11	D10	D9	D8
0	enMtl	0	0	enODSC	enJP	enSC	enProt
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
x	enProtChksm	enTP	enTTF	enAT	0	1	0

enProt: Enable Protector. Set this bit to enable the FET drivers for protector and charging functionality. When this bit is clear, FET drivers for protector and charging functions do not execute and protector and charging functions are disabled.

enJP: Enable Protection with JIETA (temperature region dependent). Set this bit to 1 to enable JEITA Protection. Clear this bit to disable JEITA protection and make OVP and OCCP thresholds for room temperature apply across the whole temperature range.

enSC: Enable Special Chemistry Model. Set this bit to 1 if a special chemistry model is used. This bit enables the use of nScOcvLim.

enAT: Enable Alert Thresholds. Set this bit to enable the IAlrtTh, VAlrtTh, TAlrtTh, and SAlrtTh registers to be restored after reset by the nIAlrtTh, nVAlrtTh, nTAlrtTh, and nSAlrtTh registers respectively. When this bit is clear, these registers restore with their alternate initialization values and the nonvolatile locations can be used for general-purpose data storage.

enTTF: Enable Time-to-Full Configuration. Set to 1 to enable the nTTFCfg (configures CVMixCap and CVHalftime) for tuning of Time-to-Full performance. Otherwise, CVMixCap and CVHalftime restore to their alternate initialization values and nTTFCfg can be used for general-purpose data storage.

enODSC: Enable OD and SC Over-Current Comparators. Set this bit to enable the ODSCTh and ODSCCfg registers to be restored after reset by the nODSCTh and nODSCCfg registers. When this bit is clear, ODSCTh and ODSCCfg restore with their alternate initialization values (comparators disabled) and nODSCTh and nODSCCfg can be used for general-purpose data storage.

enMtl: Enable CGTempCo Restore. Set this bit to enable the CGTempCo register to be restored after reset by the nADCCfg/nCGTempCo register. When this bit is clear, CGTempCo restores with its alternate initialization value. nADCCfg can be used for general-purpose data storage if both Config.FastADCen and enMtl are clear. Do not set both Config.FastADCen and enMtl at the same time.

enTP: Set to 1 to Associate the TaskPeriod Register with nTaskPeriod MTP. Otherwise, TaskPeriod restores with the POR value and the register's address configures **nRippleCfg** instead of nTaskPeriod.

enProtChksm: Enable Protector Checksum Function. Set this bit to enable the protector checksum function. When this bit is clear, the checksum protection is disabled.

0: This location must remain 0. Do not write this location to 1.

nNVCfg2 Register (1DBh)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nNVCfg2 register manages nonvolatile memory backup and restore of device and fuel gauge register RAM locations. Each bit of the nNVCfg2 register, when set, enables a given register location to be restored from or backed up to a corresponding nonvolatile memory location after reset of the IC. If nonvolatile backup of a given register is not enabled, that location initializes to a default value after reset instead. See the individual register descriptions for details. Table 88 shows the nNVCfg2 register format.

Table 88. nNVCfg2 Register (1DBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
enT	0	enMMT	enMMV	enMMC	enVT	enFC	0	enMet	0	enFL	FibMax			FibScl	

FibMax/FibScl: Set the FibMax and FibScl "Fibonacci Saving" intervals to provide recurring log-saving according to the expected battery lifespan. See the 100 Record Life Logging section for more details.

enMet: Enable Metal Current Sensing. Setting this bit to 1 enables temperature compensation of current readings for allowing copper trace current sensing. This also forces the PackCfg.TdEn bit to 1 after reset of the IC to guarantee internal temperature measurements occurs. See *nNVCfg1*.enMtl, which enables the nCGTempCo/nADCCfg register operation for adjustment of the current sensing temperature coefficient.

enFL: Enable Fault Logging. At each Life Logging event, any protection faults that have occurred during that life segment are recorded into the nFaultLog Register (0x1AE).

enFC: Enable FullCap and FullCapRep Backup and Restore. Set this bit to enable FullCap and FullCapRep registers to be restored after reset by the nFullCapRep register and FullCapRep to backup to nFullCapRep. When this bit is clear, FullCap and FullCapRep registers restore from the nFullCapNom register. nFullCapRep can then be used as general-purpose user memory.

enVT: Enable Voltage and Temperature Backup. Set this bit to enable storage of AvgVCell and AvgTA register information into the nVoltTemp register during save operations. There is no corresponding restore option. When this bit and nNVCfg0.enAF are clear, nVoltTemp can be used as general-purpose memory. Note that enVT should not be set simultaneously with nNVCfg0.enAF (AgeForecasting).

enMMC: Enable MinMaxCurr Backup. Set this bit to enable storage of the MinMaxCurr register information into the nMinMaxCurr register during save operations. There is no corresponding restore option. When this bit is clear, nMinMaxCurr can be used as general-purpose memory.

enMMV: Enable MinMaxVolt Backup. Set this bit to enable storage of the MinMaxVolt register information into the

nMinMaxVolt register during save operations. There is no corresponding restore option. When this bit is clear, nMinMaxVolt can be used as general-purpose memory.

enMMT: Enable MinMaxTemp Backup. Set this bit to enable storage of the MinMaxTemp register information into the nMinMaxTemp register during save operations. There is no corresponding restore option. When this bit is clear, nMinMaxTemp can be used as general-purpose memory.

enT: Enable TimerH Backup and Restore. Set this bit to enable the TimerH register to be backed up and restored by the nTimerH register. When this bit is clear, TimerH restores with its alternate initialization value and nTimerH can be used as general-purpose memory.

Enabling and Freeing Nonvolatile vs. Defaults

There are seven nonvolatile memory words labeled nUser that are dedicated to general-purpose user data storage. Most other nonvolatile memory locations can also be used as general-purpose storage if their normal function is disabled. The *nNVCfg0*, *nNVCfg1*, and *nNVCfg2* registers control which nonvolatile memory functions are enabled and disabled. Table 89 shows how to free up the specific registers for user data storage. Table 90 shows which nNVCfg bits control different IC functions and the effects when the bit is set or cleared. See the *nNVCfg* register descriptions for complete details. Do not convert a nonvolatile register to general-purpose memory space if that register's function is used by the application.

Below is a summary of how many bytes can be made available for user memory and the functional trade off to free up those bytes.

- 150 bytes maximum freeable: The cost is to sacrifice any optional features/configuration, including no custom OCV table and protector disabled.
- 68 bytes reasonably freeable: Made available without reverting halfway to EZ or disabling protector.
- 56 bytes freeable: Made available by using half of miscellaneous configurability.
- 30 bytes easily freeable
- 26.5 bytes always free: If SBS mode is not enabled.
- 6.5 bytes always free: Register 0x1C6 (2 bytes), Register 0x1E0 (2 bytes), lower 12 bit of Register 0x1D2, and upper byte of Register 0x19C (1 byte).

Table 89. Making Nonvolatile Memory Available for User Data

	RELATED FEATURE	FREE BY:	BYTES	REGISTERS	ADDRESS	COMMENTS
MAJOR FEATURE CHOICES	SBS NVM	Disable SBS features nNVCfg0.enSBS = 0	11 words 22 bytes	nDesignVoltage* nManfctrDate nFirstUsed nSerialNumber[0:2] nDeviceName[0:1] nManfctrName[0:2]	0x1E3*, 0x1E6-0x1EF	Generally freeable *nDesignVoltage is freeable if enSBS = 0 AND enDP = 0
	Time-to-Full Configurability	nNVCfg1.enTTF = 0	1 word 2 bytes	nTTFCfg	0x1BA	Free if default nTTFCfg is acceptable.
	Dynamic Power	nNVCfg0.enDP = 0	2 word 4 bytes	nDesignVoltage*, nRGain	0x1E3*, 0x1B8	Free if feature is not used. *nDesignVoltage is freeable if enSBS = 0 AND enDP = 0

Table 89. Making Nonvolatile Memory Available for User Data (continued)

	Age Forecasting	nNVCfg0.enAF = 0	1 word 2 bytes	nAgeFcCfg nVoltTemp* nFaultLog/ nFullCapFltr	0x1E2, 0x1AA, 0x1AE	Free if feature is not used. *nVoltTemp is freeable if enAF = 0 AND enVT = 0 *nFaultLog/ nFullCapFltr is freeable if enAF = 0 AND enFL = 0
	$LiFePO_4$	nNVCfg1.enSC	1 word 2 bytes	nScOcvLim	0x1E1	Free if feature is not used.
MODELLING/ CHARACTER-IZATION CONFIGURATION OPTIONS	Relaxation Configuration	nNVCfg0.enRCfg = 0	3 words 6 bytes	nRelaxCfg	0x1B6	Normally freeable. Defaults work for most applications.
	Misc Configuration	nNVCfg0.enMC = 0		nMiscCfg	0x1B2	
	Filter Configuration	nNVCfg0.enFCfg = 0		nFilterCfg	0x19D	
	nLearnCfg	nNVCfg0.enLCfg = 0	1 word 2 bytes	nLearnCfg	0x19F	Freeable depending on modelling/ characterization.
	Misc Configuration (Pushbutton, Comm-Shutdown, AtRate-enable	nNVCfg0.enCfg = 0	1 word 2 bytes	nConfig	0x1B0	Needed only for: Pushbutton feature, temp-alerts, 1% alerts, AtRate, comm-shutdown.
	Charge Termination	nNVCfg0.enICT = 0	1 word 2 bytes	nIChgTerm	0x1C1	Free if feature is not used and IChgTerm restores to the default value.
	FullCapRep Restore	nNVCfg0.enFC = 0	1 word 2 bytes	nFullCapRep	0x1A9	Free if feature is not used. FullCapRep is restored from nFullCapNom
	SOC Table	Use m5 EZ model by setting nNVCfg.enOCV = 0 nNVCfg.enX = 0	12 words 24 bytes	nXTable[0:11]	0x180-0x18B	With custom models/ characterization, this is not freeable.
	OCV Table		12 words 24 bytes	nOCVTable[0:11]	0x190-0x19B	
OTHER	Alert Startup Configuration	nNVCfg1.enAT = 0	4 words 8 bytes	nVAlrtTh nTAlrtTh nIAlrtTh nSAlrtTh	0x18C-0x18F	Free if feature is not used.
	Voltage Temperature Logging	nNVCfg2.enVT = 0	1 word 2 bytes	nVoltTemp*	0x1AA	*nVoltTemp is freeable if enAF = 0 AND enVT = 0

Table 89. Making Nonvolatile Memory Available for User Data (continued)

	Fault Logging	nNVCfg2.enFL = 0	1 word 2 bytes	nFaultLog/ nFullCapFltr*	0x1AE	*nFaultLog/ nFullCapFltr is freeable if enAF = 0 AND enFL = 0
	TimerH Logging	nNVCfg2.enT= 0	1 word 2 bytes	nTimerH	0x1AF	Free if feature is not used.
	Save MaxMinCurr	nNVCfg2.eMMC = 0	1 word 2 bytes	nMaxMinCurr	0x1AB	Free if feature is not used.
	Save MaxMinVolt	nNVCfg2.eMMV = 0	1 word 2 bytes	nMaxMinVolt	0x1AC	Free if feature is not used.
	Save MaxMinTemp	nNVCfg2.eMMT = 0	1 word 2 bytes	nMaxMinTemp	0x1AD	Free if feature is not used.
	Protector NVM Checksum	nNVCfg1 .enProtChkSm = 0	1 bytes	nProtCfg2	0x1DF	The lower byte is freeable.
	Protector and Charger	nNVCfg1.enProt = 0 nNVCfg1.enJP = 0	18 words 36 bytes	nStepCurr, nStepVolt, nVChgCfg1, nVChgCfg2, nIChgCfg1,nIChgCfg2, nUVPrtTh, nTPrtTh1 nTPrtTh3, nIPrtTh1 nIPrtTh2, nTPrtTh2 nProtMisTh nProtCfg, nOVPrtTh, nDelayCfg nODSCTh, nODSCCfg	0x1C4-0x1C5, 0x1CC-0x1CF, 0x1D0-0x1D7, 0x1DA, 0x1DC-0x1DE	Most applications of MAX17332 use the protector and charger. However, if the protector and charger are entirely disabled, these 32 bytes become free NVM. FET drivers for charging and protection do not execute in this configuration.

Table 90. Nonvolatile Memory Configuration Options

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT(S) IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
180h - 18Bh	nXTable0 through nXTable12	All 0x0000	nNVCfg0.enX	180h-18Bh Hold Custom Cell Model Information	Becomes Free[1], IC Uses Default EZ Cell Model
18Ch	nVAlrtTh	0x0000	nNVCfg1.enAT	VAlrtTh, TAlrtTh, IAlrtTh, SAlrtTh initialize from nVAlrtTh, nTAlrtTh, nIAlrtTh, nSAlrtTh	Becomes Free[1], VAlrtTh, TAlrtTh, IAlrtTh, SAlrtTh → Disabled Threshold Values
18Dh	nTAlrtTh	0x0000			
18Eh	nIAlrtTh	0x0000			
18Fh	nSAlrtTh	0x0000			
190h - 19Bh	nOCVTable0 through nOCVTable12	All 0x0000	nNVCfg0.enOCV	190h-19Bh Hold Custom Cell Model Information	Becomes Free[1], IC Uses Default EZ Cell Model
19Ch	nRsense	0x000A	N/A	Upper Byte is Always Free. Lower Byte is the Sense Resistor Value—Helps Host Translate Currents and Capacities	
19Dh	nFilterCfg	0x0000	nNVCfg0.enFCfg	nFilterCfg→ FilterCfg	Becomes Free[1], FilterCfg = 0x0EA4
19Eh	nVEmpty	0xA561	N/A	nVEmpty must be set to the empty voltage and recovery voltage of the battery.	

Table 90. Nonvolatile Memory Configuration Options (continued)

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT(S) IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
19Fh	nLearnCfg	0x0000	nNVCfg0.enLCfg	nLearnCfg → LearnCfg	Becomes Free[1], LearnCfg = 0x4696
1A0h	nQRTable00	0x1080	N/A	Always QRTable Information nQRTable20→ QRTable20 nQRTable30→ QRTable30	
1A1h	nQRTable10	0x2043			
1A2h	nQRTable20	0x078C			
1A3h	nQRTable30	0x0880			
1A4h	nCycles	0x0000		Always nCycles→ Cycles	
1A5h	nFullCapNom	0x0D48		Always nFullCapNom→ FullCapNom	
1A6h	nRComp0	0x08CC		Always nRComp0→ RComp0	
1A7h	nTempCo	0x223E		Always nTempCo→ TempCo	
1A8h	nBattStatus	0x0000	N/A	Logs/Saves Permanent Failure Status	
1A9h	nFullCapRep	0x0D48	nNVCfg2.enFC	nFullCapRep→ FullCapRep	Becomes Free[1] nFullCapNom→ FullCapRep
1AAh	nVoltTemp	0x0000	nNVCfg2.enVT (nNVCfg0.enAF = 0)	AvgVCell→ nVoltTemp and AvgTA→ nVoltTemp at each backup event	Becomes Free[1], Voltage, Temperature Logging Disabled
			nNVCfg0.enAF (nNVCfg2.enVT = 0)	nVoltTemp stores Age Forecasting Information	Becomes Free[1], Age Forecasting Disabled
1ABh	nMaxMinCurr	0x0000	nNVCfg2.enMMC	MaxMinCurr→ nMaxMinCurr at each backup event	Becomes Free[1]
1ACh	nMaxMinVolt	0x0000	nNVCfg2.enMMV	MaxMinVolt→ nMaxMinVolt at each backup event	Becomes Free[1],
1ADh	nMaxMinTemp	0x0000	nNVCfg2.enMMT	MaxMinTemp→ nMaxMinTemp at each backup event	Becomes Free[1],
1AEh	nFaultLog/ nFullCapFltr	0x0000	nNVCfg2.enFL	nFaultLog stores the history of all protection events tha happened in this save segment	Becomes Free[1], Fault logging and Age Forecasting are Disabled
			nNVCfg2.enAF	nFullCapFltr contains a highly filtered nFullCapNom.	
1AFh	nTimerH	0x0000	nNVCfg2.enT	TimerH→ nTimerH at each backup event	Becomes Free[1],
1B0h	nConfig	0x0000	nNVCfg0.enCfg	nConfig→ Config nConfig→ Config2	Becomes Free[1], Config = 0x2214, Config2 = 0x2058
1B1h	nRippleCfg	0x0204	N/A	Always nRippleCfg→ RippleCfg	
1B2h	nMiscCfg	0x0000	nNVCfg0.enMC	nMiscCfg→ MiscCfg	Becomes Free[1], MiscCfg = 0x3070
1B3h	nDesignCap	0x2A83	N/A	Always nDesignCap→ DesignCap, VScale, QScale	
1B4h	nI2CCfg	0x0010	N/A	Always nI2CCfg	
1B5h	nFullCfg	0x0785	N/A	Always nFullCfg	
1B6h	nRelaxCfg	0x0000	nNVCfg0.enRCfg	nRelaxCfg→ RelaxCfg	Becomes Free[1], RelaxCfg = 0x2039,

Table 90. Nonvolatile Memory Configuration Options (continued)

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT(S) IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
1B7h	nConvgCfg	0x2241	N/A	Always Converge-to-Empty	
1B8h	nRGain	0x0000	nNVCfg0.enDP	Used for Dynamic Power	Becomes Free[1], Dynamic Power Disabled
1B9h	nAgeChgCfg	0x0000	N/A	Always nAgeChgCfg	
1BAh	nTTFCfg	0x0000	nNVCfg1.enTTF	nTTFCfg Configures Time-to-Full Calculation	Becomes Free[1], Time-to-Full Default Configuration
1BBh	nHibCfg	0x0909	N/A	Always nHibCfg	
1BCh	nROMID0	Varies	N/A	Always the Unique 64-bit ID	
1BDh	nROMID1	Varies			
1BEh	nROMID2	Varies			
1BFh	nROMID3	Varies			
1C0h	nChgCtrl1	0x4209	N/A	Do Not Modify without Special Guidance from Analog Devices	
1C1h	nIChgTerm	0x0280	nNVCfg0.enICT	nIChgTerm→ IChgTerm	Becomes Free[1], IChgTerm = FullCapRep/3
1C2h	nChgCfg0	0x141F	N/A	Always nChgCfg0	
1C3h	nChgCtrl0	0xE272	N/A	Do Not Modify without Special Guidance from Maxim	
1C4h	nStepCurr	0x00A7	nNVCfg1.enProt	Always nStepCurr/nStepVolt. Set to 0x0000 to disable Step Charging	Becomes Free[1]
1C5h	nStepVolt	0xAA00			
1C6h	UserMemory_1C6	0x0000	N/A	Always Free	
1C7h	nPackCfg	0x2000	N/A	Always nPackCfg	
1C8h	nCGain	0x4000	N/A	Trim for Calibrating Current-Sense Gain	
1C9h	nCGTempCo/ nADCCfg	0x5188	nNVCfg1.enMtl (nNVCfg2.enMet = 1) (nNVCfg1.enADCcfg = 0)	Metal Current Sense TempCo Configurable Custom ADCCfg doesn't apply	Becomes Free[1], Metal Current Sense TempCo Enabled, CGTempCo = 0x20C8
			nNVCfg1.enCrv (nNVCfg2.enMet = 0)(nNVCfg1.enADCcfg = 1)	Custom ADCCfg	Becomes Free[1], ADC configuration defaulted
1CAh	nThermCfg	0x71BE	N/A	Configuration for Translating Thermistor to ºC	
1CBh	nChgCfg1	0x3E3F	N/A	Always nChgCfg1	
1CCh	nVChgCfg1	0x5005	nNVCfg1.enProt	Configuration for Charging Voltage	
1CDh	nVChgCfg2	0x6666			
1CEh	nICChgCfg1	0x2FE8	nNVCfg1.enProt	Configuration for Charging Current	
1CFh	nICChgCfg2	0x5555			

Table 90. Nonvolatile Memory Configuration Options (continued)

ADDRESS	REGISTER NAME	FACTORY DEFAULT	CONTROL BIT(S)	FUNCTION WHEN CONTROL BIT(S) IS SET	FUNCTION WHEN CONTROL BIT(S) CLEARED
1D0h	nUVPrtTh	0x3D4C	nNVCfg1.enProt	Configures Protection Thresholds	Becomes Free[1] Protector Disabled (Lower 12 bits of nTPrtTh3 are always free)
1D1h	nTPrtTh1	0x2038			
1D2h	nTPrtTh3	0x7000			
1D3h	nIPrtTh1	0x5107			
1D4h	nIPrtTh2	0xA028			
1D5h	nTPrtTh2	0x3005			
1D6h	nProtMiscTh	0x7A28			
1D7h	nProtCfg	0x3000			
1D8h	nNVCfg0	0x0000	N/A	Always Required Nonvolatile Memory Control Registers	
1D9h	nNVCfg1	0x0182			
1DAh	nOVPrtTh	0xFA81	nNVCfg1.enProt	Configures Protection Thresholds	Becomes Free[1] Protector Disabled
1DBh	nNVCfg2	0xFE0A	N/A	Always Required Nonvolatile Memory Control Registers	
1DCh	nDelayCfg	0x9B3D	nNVCfg1.enProt	Configures Protection Thresholds	Becomes Free[1] Protector Disabled
1DDh	nODSCTh	0x0EAF			
1DEh	nODSCCfg	0x4355			
1DFh	nProtCfg2	0x0048	nNVCfg1. {enProtChkSm and enProt}	Holds CheckSum Value of 1B0h-1BBh, 1C0h-1CFh 1D0h-1DEh for Validating NVM at Startup	Upper Byte is always for ISD Settings, Lower Byte Becomes Free[1]
1E0h	UserMemory_1E0	0x0000	N/A	Always Free	
1E1h	nScOcvLim	0x0000	nNVCfg1.enSC	Used for $LiFePO_4$ Gauging	Becomes Free[1] $LiFePO_4$ Disabled
1E2h	nAgeFcCfg	0x0000	nNVCfg0.enAF	Configures Age Forecast	Becomes Free[1]
1E3h	nDesignVoltage	0x0000	nNVCfg0.enSBS or nNVCfg0.enDP	nDesignVoltage→ sDesignVolt/ MinSysVoltage	Becomes Free[1]
1E4h	nChgCfg2	0x1800	N/A	Always nChgCfg2	
1E5h	nPackResistance/ Reserved	0x0000	nNVCfg0.enDP	Configures nPackResistance→ sPackResistance	Reserved
1E6h	nManfctrDate	0x0000	nNVCfg0.enSBS	nManfctrDate→ sManfctrDate	Becomes Free[1]
1E7h	nFirstUsed	0x0000		nFirstUsed→ sFirstUsed	Becomes Free[1]
1E8h	nSerialNumber0	0x0000		nSerialNumber[2:0]→ sSerialNumber	Becomes Free[1]
1E9h	nSerialNumber1	0x0000			
1EAh	nSerialNumber2	0x0000			
1EBh	nDeviceName0	0x0000		nDeviceName[1:0]→ sDeviceName	Becomes Free[1]
1ECh	nDeviceName1	0x0000			
1EDh	nManfctrName0	0x0000		nManfctrName[2:0]→ sManfctrName	
1EEh	nManfctrName1	0x0000			
1EFh	nManfctrName2	0x0000			

Note 1: "Free" Indicates the address is unused and available as general user nonvolatile.

Shadow RAM

Nonvolatile memory is never written to or read from directly by the communication interface. Instead, data is written to or read from shadow RAM located at the same address. Copy and recall commands are used to transfer data between the nonvolatile memory and the shadow RAM. Figure 28 describes this relationship. Nonvolatile memory recall occurs automatically at IC power-up and software POR.

Shadow RAM and Nonvolatile Memory Relationship

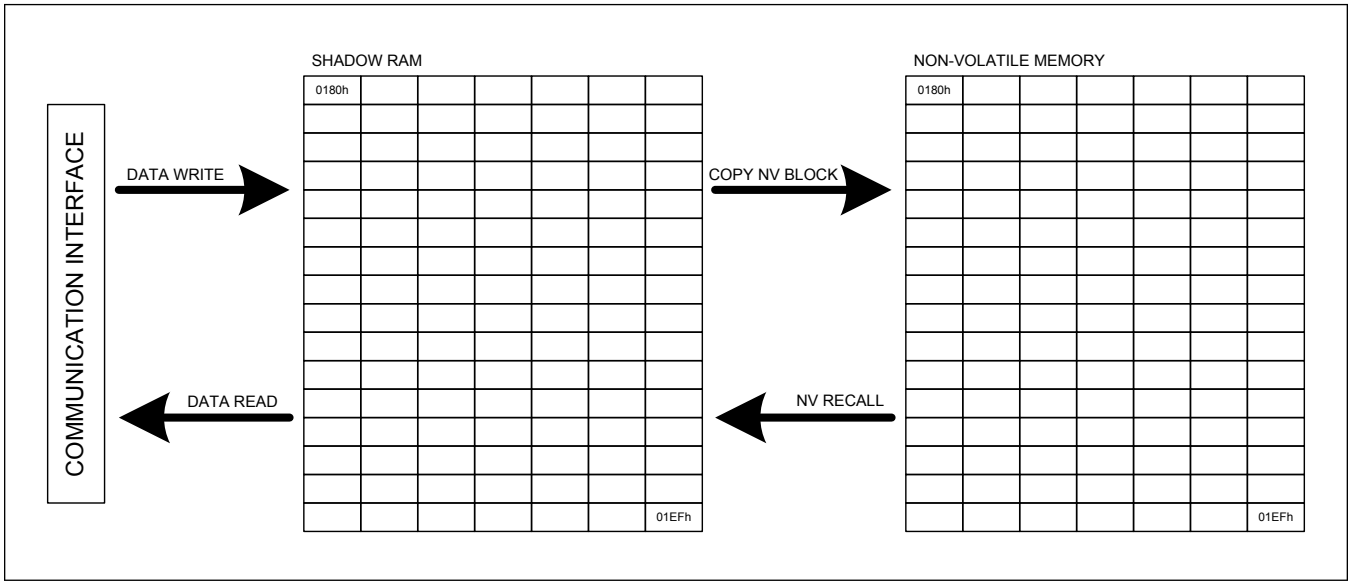


Figure 28. Shadow RAM and Nonvolatile Memory Relationship

Nonvolatile Memory Commands

The following commands are used to copy or recall data from the nonvolatile memory. All commands are written to the Command register at memory address 060h to perform the desired operation. The CommStat register can be used to track the status of the request.

COPY NV BLOCK [E904h]

This command copies the entire block from shadow RAM to nonvolatile memory addresses 180h to 1EFh excluding the unique ID locations of 1BCh to 1BFh. After issuing this command, the host must wait t_{BLOCK} for the operation to complete. The configuration memory can be copied a maximum of seven times. Note that the supply voltage must be above V_{NVM} for the operation to complete successfully.

NV RECALL [E001h]

This command recalls the entire block from nonvolatile memory to Shadow RAM addresses 180h to 1EFh. This is a low-power operation that takes up to t_{RECALL} to complete. Note that the supply voltage must be above VNVM for the operation to complete successfully.

HISTORY RECALL [E2XXh]

This command copies history data into page 1Fh of memory. After issuing this command, the host must wait t_{RECALL} for the operation to complete before reading page 1Fh. Table 91 shows what history information can be recalled. See the *SHA-256*, *Battery Life Logging*, and *Determining Number of Remaining Updates* sections for details on how to decode this information.

Table 91. History Recall Command Functions

COMMAND	FUNCTION
0xE29D	Recall indicator flags to determine remaining SHA-256 secret updates or clears
0xE29B	Recall indicator flags to determine remaining configuration memory writes
0xE29C	Recall indicator flags to determine remaining Battery Life Logging updates
0xE29C, 0xE29D	Recall indicator flags to determine Battery Life Logging update errors
0xE22E to 0xE291	Recall Battery Life Logging information

Nonvolatile Block Programming

The host must program all nonvolatile memory locations at the same time by using the Copy NV Block command. The host first writes all desired nonvolatile memory shadow RAM locations to their desired values, sends the Copy NV Block command, and then waits tBLOCK for the copy to complete. Afterwards, the host sends the power-on-reset sequence to reset the IC and the new nonvolatile settings take effect. The CommStat.NVError bit should be read to determine if the copy command executed successfully. Note that configuration memory is limited to nBLOCK total write attempts. The recommended full sequence is:

1. Write 0x0000 to the CommStat register (0x061) 2 times in a row to unlock Write Protection.
2. Write and Verify the desired memory locations to new values.
3. Write 0x0000 to the CommStat register (0x061) to clear CommStat.NVError bit.
4. Write 0xE904 to the Command register 0x060 to initiate a block copy.
5. Wait tBLOCK for the copy to complete.
6. Check the CommStat.NVBusy bit. Continue to wait while CommStat.NVBusy = 1.
7. Check the CommStat.NVError bit. If set, return to Step 2 to repeat the process. If clear, continue.
8. Write 0x000F to the Command register 0x060 to POR the IC.
9. Wait 10ms.
10. Verify all of the nonvolatile memory locations are recalled correctly.
11. Write 0x0000 to the CommStat register (0x061) 3 times in a row to unlock Write Protection and clear NVError bit.
12. Write 0x8000 to Config2 register 0x0AB to reset firmware.
13. Wait for POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate POR sequence is complete.
14. Write 0x00F9 to the CommStat register (0x061) 2 times in a row to lock Write Protection.

To only update the Shadow RAM without copying the values to NVM, the recommended sequence is:

1. Write 0x0000 to the CommStat register (0x061) 2 times in a row to unlock Write Protection.
2. Write and Verify the desired memory locations to new values.
3. Write 0x8000 to Config2 register 0x0AB to reset firmware.
4. Wait for POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate POR sequence is complete.
5. Write 0x00F9 to the CommStat register (0x061) 2 times in a row to lock Write Protection.

Determining Number of Remaining Updates

The configuration memory can only be updated seven times by the user (first update occurs during manufacturing test). The number of remaining updates can be calculated using the following procedure:

1. Write 0xE29B to the Command register (060h).
2. Wait t_{RECALL}.
3. Read memory address 1FDh.
4. Decode address 1FDh data as shown in Table 92. Each block write has redundant indicator flags for reliability. Logically OR the upper and lower bytes together, then count the number of 1s determine how many updates have already

been used. The first update occurs in manufacturing test prior to shipping to the user.

Table 92. Number of Remaining Config Memory Updates

ADDRESS 1FDH DATA	LOGICAL OR OF UPPER AND LOWER BYTES	NUMBER OF UPDATES USED	NUMBER OF UPDATES REMAINING
0000000x00000001b or 000000010000000xb	00000001b	1	7
000000xx0000001xb or 0000001x000000xxb	00000011b	2	6
00000xxx000001xxb or 000001xx00000xxxb	00000111b	3	5
0000xxxx00001xxxb or 00001xxx0000xxxxb	00001111b	4	4
000xxxxx0001xxxxb or 0001xxxx000xxxxxb	00011111b	5	3
00xxxxxx001xxxxxb or 001xxxxx00xxxxxxb	00111111b	6	2
0xxxxxxx01xxxxxxb or 01xxxxxx0xxxxxxxb	01111111b	7	1
xxxxxxxx1xxxxxxxb or 1xxxxxxxxxxxxxxxb	11111111b	8	0

Memory Locks and Write Protection

ModelGauge m5 EZ RAM Registers and all nonvolatile memory locations can be write protected or permanently locked to prevent accidental overwriting or data loss in the application. Write protecting or locking a memory block only prevents future writes to the locations. Reading locked locations is still allowed. The IC has write protection enabled by default and must be disabled (as described in *CommStat Register*) before any registers can be written. **Note that locking a memory location is permanent so carefully choose all desired locks before sending the NV LOCK command.**

The SHA secret is stored in a separate secure non-readable memory. There is a different command for locking the SHA secret and its state is not displayed in the Lock register. See the *SHA-256 Authentication* section for details. Once a lock bit is set, it can never be cleared. Table 79 shows which lock bits correspond to which memory blocks of the IC.

CommStat Register (061h)

Register Type: Special

Nonvolatile Backup: None

The CommStat register tracks the progress and error state of any command sent to the Command register. It also provides the write protection control and status of each page of registers. Table 93 shows the register format.

Table 93. CommStat Register (061h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	DISOff	CHGOff	WP5	WP4	WP3	WP2	WP1	NVError	NVBusy	WPGlobal

X: Don't Care. This bit is undefined and can be logic 0 or 1.

Write Protection: To prevent the host from accidentally writing any registers of the IC, write protection is enabled by default. Any time the host wants to write a register, the global write protection must be disabled as well as the write protection for the specific register page. To prevent accidental unlocking of the write protection, the CommStat register must be written with the desired value two times in a row (without accessing any other registers) to set or clear any of the write protection bits. All bits can be set or cleared in the same write sequence. For example, writing 0x0000 to CommStat twice in a row clears the WPGlobal and all WP1-WP5 at the same time.

WPGlobal: Write Protection Global Enable. Set to 1 to write protect all register pages. Clear to 0 to allow individual write protect bits (WP1–WP5) to be disabled.

WP1–WP5: Write Protection Enable Bits. Set any bit to 1 to write protect the following specified pages. Clear any bit to 0 to allow pages to be writable. To update any of these bits, the WPGlobal bit must be 0.

WP1: Write protects register pages 1Ah, 1Bh, 1Eh

WP2: Write protects register pages 01h, 02h, 03h, 04h, 0Bh, 0Dh

WP3: Write protects register pages 18h, 19h

WP4: Write protects register pages 1Ch

WP5: Write protects register pages 1Dh

DISOff: Set this bit to 1 to forcefully turn off DIS FET (ignoring all other conditions) if nProtCfg.CmOvrdEn is enabled. DIS FET remains off as long as this bit stays to 1. Clear to 0 for normal operation. Write Protection must be disabled before writing to the DISOff bit.

CHGOff: Set this bit to 1 to forcefully turn off CHG FET (ignoring all other conditions) if nProtCfg.CmOvrdEn is enabled. CHG FET remains off as long as this bit stays set to 1. Clear to 0 for normal operation. Write Protection must be disabled before writing to the CHGOff bit.

NVBusy: This read only bit tracks if nonvolatile memory is busy or idle. NVBusy defaults to 0 after reset indicating nonvolatile memory is idle. This bit sets after a nonvolatile related command is sent to the command register and clears automatically after the operation completes.

NVError: This bit indicates the results of the previous SHA-256 or nonvolatile memory related command sent to the command register. This bit sets if there was an error executing the command or if the Full Reset command is executed. Once set, the bit must be cleared by system software in order to detect the next error. Write Protection must be disabled before the NVError bit can be cleared by the host.

NV LOCK [6AXXh]

This command permanently locks a block or blocks of memory. To set a lock, send 6AXXh to the Command register where the lower 5 bits of the command determine which locks are set. Table 94 shows a detailed format of the NV LOCK command. Set each individual LOCK bit to 1 to lock the corresponding register block. Set the LOCK bit to 0 to do nothing at this time. For example, writing 6A02h to the Command register sets LOCK2. Writing 6A1Fh sets all five locks. Writing 6A00h does not set any locks.

Table 94. Format of LOCK Command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	1	0	0	0	0	LOCK 5	LOCK 4	LOCK 3	LOCK 2	LOCK 1

LOCK1: Locks register pages 1Ah, 1Bh, 1Eh (Locking disables History Life Logging)

LOCK2: Locks register pages 01h, 02h, 03h, 04h, 0Bh, 0Dh

LOCK3: Locks register pages 18h, 19h

LOCK4: Locks register pages 1Ch

LOCK5: Locks register pages 1Dh

Locking Memory Blocks

Prior to sending the lock command, the CommStat.NVError bit should be cleared; after the command is sent, the

CommStat.NVError bit should be read to determine if the lock command executed successfully. Note that locking memory blocks is a permanent operation. The recommended full sequence is:

1. Write 0x0000 to the CommStat register (0x61) two times in a row to unlock write protection.
2. Write 0x0000 to the CommStat register (0x61) one more time to clear CommStat.NVError bit.
3. Write 0x6AXX to the Command register 0x060 to lock desired blocks.
4. Wait t_{UPDATE} for the copy to complete.
5. Check the CommStat.NVError bit. If set, repeat the process.
6. Write 0x00F9 to the CommStat register (0x61) two times in a row to lock write protection.

Reading Lock State

The Lock register at address 07Fh reports the state of each lock. See Table 95 for the format of the Lock register. If a LOCK bit is set, the corresponding memory block is locked. If the LOCK bit is cleared, the corresponding memory block is unlocked. Note that the SHA-256 secret lock state cannot be read through this register.

Table 95. Format of Lock Register (07Fh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	LOCK 5	LOCK 4	LOCK 3	LOCK 2	LOCK 1

X: Don't Care

1: LOCK is set

0: LOCK is clear

Analog Measurements

The MAX17332 monitors cell pack voltage, cell pack current, cell pack temperature, and the voltage of the cell. This information is provided to the fuel-gauge algorithm to predict cell capacity and trigger protection FETs in case of fault conditions and is also made available to the user. Note that ADC-related register information is not maintained while the IC is in shutdown mode. The following register information is invalid until the first measurement cycle after the IC returns to active mode of operation.

Voltage Measurement

The MAX17332 monitors the voltage at the BATT pin.

VCell Register (01Ah)

Register Type: Voltage

Nonvolatile Backup: None

Each update cycle, the reading of the cell voltage measurement is placed in the VCell register. VCell is used as the voltage input to the fuel-gauge algorithm and triggers protection FETs in case of fault conditions.

VCellRep Register (012h)

Register Type: Voltage

Nonvolatile Backup: None

VCellRep reports a low-noise measurement of battery voltage as shown in Figure 29.

AvgVCell Register (019h)

Register Type: Voltage

Nonvolatile Backup: None

The AvgVCell register reports an average of the VCell register readings. The time period for averaging is configurable from a 12 second to 24 minute time period. See the *FilterCfg* register description for details on setting the time filter.

The first VCell register reading after power-up or exiting shutdown mode sets the starting point of the AvgVCell register. Note that when a cell relaxation event is detected, the averaging period changes to the period defined by the RelaxCfg.dt setting. The register reverts to its normal averaging period when a charge or discharge current is detected.

MaxMinVolt Register (0008h)

Register Type: Special

Nonvolatile Backup: Saves to nMaxMinVolt (1ACh) if nNVCfg2.enMMV is set (does not restore from nonvolatile).

Initial Value: 0x00FF

The MaxMinVolt register maintains the maximum and minimum of VCell register values since device reset. They are compared against these values each time the voltage registers update. If the new reading is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power-up, the maximum voltage value is set to 00h (the minimum) and the minimum voltage value is set to FFh (the maximum). Therefore, both values are changed to the voltage register reading after the first update. The host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution. Table 96 shows the register format.

Table 96. MaxMinVolt (008h)/nMaxMinVolt (1ACh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxVCELL								MinVCELL							

MaxVCELL: Maximum VCell register reading (20mV resolution).

MinVCELL: Minimum VCell register reading (20mV resolution).

MaxMinVolt is not cumulative across the entire battery lifetime. After each periodic nonvolatile-memory save, MaxMinVolt resets to 0x00FF to find the next max/min volt across the next segment of battery life. This behavior helps provide a useful log across the battery lifetime where each log segment shows the maximum and minimum voltage experienced across only that segment.

Cell1 Register (0D8h)

Register Type: Voltage

Nonvolatile Backup: None

In the MAX17332, the Cell1 register duplicates the voltage from the VCell register (measured at the BATT pin). This register is only provided for cross-compatibility with multicell chips where a set of cell voltages is provided.

AvgCell1 Register (0D4h)

Register Type: Voltage

Nonvolatile Backup: None

The AvgCell1 register reports an 8-sample filtered average of the corresponding Cell1 register readings.

Batt Register (0D7h)

Register Type: Special

Nonvolatile Backup: None

The Batt registers contains the VCell voltage measured inside the protector on a 20.48V scale with an LSB of 0.3125mV for cross-compatibility with other Maxim Integrated gauges that provide multicell functionality. This allows a generalized driver to interact both with single-cell and multicell chips.

PCKP Register (0DBh)

Register Type: Special

Nonvolatile Backup: None

The PCKP register contains the voltage between PACK+ and GND on a 20.48V scale with an LSB of 0.3125mV.

MinVolt Register (0ADh)

Register Type: Voltage

Nonvolatile Backup: None

The MinVolt register maintains the minimum BATT register value within a 45 second period or until cleared by host software. Each time the BATT register updates, it is compared against its value. If the reading is less than the minimum, the corresponding value is replaced with the new reading. At power-up, MinVolt value is set to 0xFFFF. Therefore, the value is changed to the BATT register reading after the first update. The host software can reset this register by writing it to its power-up value of 0xFFFF. LSB is 1.25mV.

Current Measurement

The MAX17332 can monitor the current flow through the cell pack by measuring the voltage between the CSN and CSP pins over a ±51.2mV range. While in active mode, updates occur in intervals of 351.5ms. In hibernate mode, the update interval is set by the nHibCfg register. All ICs are calibrated for current-measurement accuracy at the factory. However, Current register readings can be adjusted by changing the nCGain register setting if the application requires it.

If the application uses a sense resistor with a large temperature coefficient such as a copper metal board trace, current readings can be adjusted based on the temperature measured by the IC. The CGTempCo register stores a percentage per ºC value that is applied to current readings if the nNVCfg2.enMet bit is set. If nNVCfg1.enMtl = 0, the default temperature coefficient of copper is used for temperature adjustments. If enMt = 1, the CGTempCo register value is used for temperature adjustments.

Additionally, the IC maintains a record of the minimum and maximum current measured by the IC and an average current over a time period defined by the host. Contents of the Current and AvgCurrent registers are indeterminate for the first conversion cycle time period after IC power-up.

Current Measurement Timing

Current measurements are always enabled regardless of nPackCfg settings. Table 97 shows the timing for current measurements made by the IC. All times in this table are considered typical.

Table 97. Current Measurement Timing

APPLICATION	NPACKCFG SETTING	REGISTER	FIRST UPDATE AFTER RESET[1] (ms)	UPDATE RATE IN ACTIVE MODE (ms)	UPDATE RATE IN HIBERNATE MODE[2] (s)
Any	Any	Current	150	351	1.4
		AvgCurrent	150	351	1.4

1. AvgCurrent register is initialized using a single reading instead of an average.

2. Hibernate mode update times assume the recommended nHibCfg.HibScalar setting of 4 task periods.

Current Register (01Ch)

Register Type: Current

Nonvolatile Backup: None

The IC measures the voltage between the CSP and CSN pins, and the result is stored as a two's complement value in the Current register. Voltages outside the minimum and maximum register values are reported as the minimum or maximum value. The register value should be divided by the sense resistance to convert to amps. The value of the sense resistor determines the resolution and the full-scale range of the current readings. Table 98 shows range and resolution values for typical sense resistances.

Table 98. Current Measurement Range and Resolution vs. Sense Resistor Value

BATTERY FULL CAPACITY (mAh)	SENSE RESISTOR (mΩ)	nRSENSE	CURRENT REGISTER RESOLUTION (µA)	CURRENT REGISTER RANGE (A)	CAPACITY RESOLUTION (mAh)	MAXIMUM CAPACITY (mAh)
> 4000	1	0064h	1562.5	±51.2	5	144360
> 2000	2	00C8h	781.25	±25.6	2.5	71680

Table 98. Current Measurement Range and Resolution vs. Sense Resistor Value (continued)

BATTERY FULL CAPACITY (mAh)	SENSE RESISTOR (mΩ)	nRSENSE	CURRENT REGISTER RESOLUTION (µA)	CURRENT REGISTER RANGE (A)	CAPACITY RESOLUTION (mAh)	MAXIMUM CAPACITY (mAh)
> 800	5	01F4h	312.5	±10.24	1	28672
> 400	10	03E8h	156.25	±5.12	0.5	14336
> 200	20	07D0h	78.125	±2.56	0.25	7168
> 80	50	1388h	31.25	±1.02	0.1	2867
> 40	100	2710h	15.625	±0.51	0.05	1433

CurrRep Register (022h)

Register Type: Current

Nonvolatile Backup: None

CurrRep reports a low-noise measurement of current as shown in Figure 29.

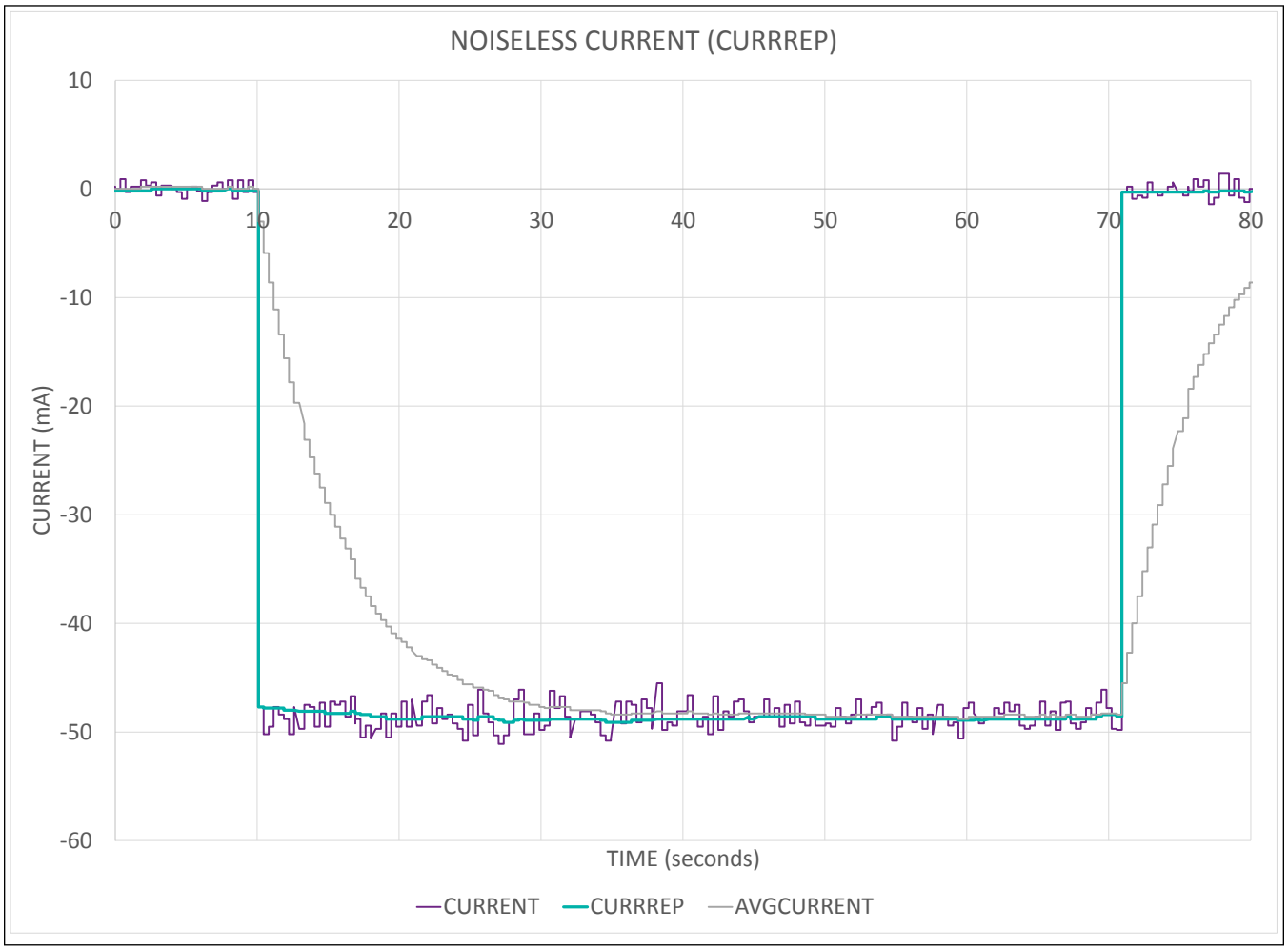


Figure 29. Noiseless Current

AvgCurrent Register (01Dh)

Register Type: Current

Nonvolatile Backup: None

The AvgCurrent register reports an average of Current register readings over a configurable 0.7 second to 6.4 hour time period. See the *FilterCfg* register description for details on setting the time filter. The first Current register reading after returning to active mode sets the starting point of the AvgCurrent filter.

MaxMinCurr Register (00Ah)

Register Type: Special

Nonvolatile Backup: Periodically saves to nMaxMinCurr (1ABh) if nNVCfg2.enMMC is set, but does not restore from nonvolatile memory.

Alternate Initial Value: 0x807F

The MaxMinCurr register maintains the maximum and minimum Current register values since the last IC reset or until cleared by host software. Each time the Current register updates, it is compared against these values. If the reading is larger than the maximum or less than the minimum, the corresponding value is replaced with the new reading. At power-up, the maximum current value is set to 80h (the minimum) and the minimum current value is set to 7Fh (the maximum). Therefore, both values are changed to the Current register reading after the first update. The host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum voltages are each stored as two's complement 8-bit values with 0.4mV/R_{SENSE} resolution. Table 99 shows the register format.

Table 99. MaxMinCurr (00Ah)/nMaxMinCurr (1ABh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MaxCurrent								MinCurrent							

MaxCurrent: Maximum Current register reading (0.40mV/R_{SENSE} resolution)

MinCurrent: Minimum Current register reading (0.40mV/R_{SENSE} resolution)

MaxMinCurr is not cumulative across the entire battery lifetime. After each periodic nonvolatile-memory save, MaxMinCurr resets to 0x807F to find the next maximum and minimum current across the next segment of battery life. This behavior helps provide a useful log across the battery lifetime where each log segment shows the maximum and minimum current experienced across only that segment.

nCGain Register (1C8h)

Register Type: Special

The nCGain register adjusts the gain and offset of the current measurement result. The current measurement A/D is factory trimmed to data sheet accuracy without the need for the user to make further adjustments. The recommended default for the nCGain register is 0x4000 which applies no adjustments to the Current register reading.

For specific application requirements, the CGain and COff values can be used to adjust readings as follows:

Current register = (current A/D reading × (CGain / 256)) + COff

CGain and COff are combined into a single register formatted as shown in Table 100.

Table 100. nCGain Register (1C8h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CGain										COff					

COff: COff has a range of -32 to +31 LSbs. However, it is normally not recommended to calibrate COff. **COff = 0** is recommended for most applications.

CGain: The recommended default value of CGain = 0x100 corresponds to a gain of 1. CGain can be calculated as follows: CGain = ((MeasuredCurrent/ReportedCurrent) x 0x0100). CGain is a signed value and can be negative.

CGTempCo (0B8h)/nCGTempCo (0x1C9) Register

Register Type: Special

Alternate Initial Value: 0x20C8

If Config.FastADCen= 0 and nNVCfg1.enMet = 1, then CGTempCo is used to adjust current measurements for temperature. CGTempCo has a range of 0% to 3.1224% per °C with a step size of 3.1224/0x10000 percent per °C. If the nNVCfg1.enMtl bit is clear, CGTempCo defaults to a value of 0x20C8 or 0.4% per °C which is the approximate temperature coefficient of a copper trace. If the nNVCfg1.enMtl bit is set, CGTempCo restores from nCGTempCo (1C9h) after IC reset allowing a custom sense resistor temperature coefficient to be used. Note that Config.FastADCen and nNVCfg1.enMet cannot be enabled simultaneously.

Copper Trace Current Sensing

The MAX17332 can measure current using a copper board trace instead of a traditional sense resistor, the main difference being the ability to adjust to the change in sense resistance over temperature. To enable copper trace current sensing, set the following configuration bits nNVCfg1.enADCCfg = 0 and nNVCfg2.enMet = 1. The IC's default temperature adjustment is 0.4% per °C but can be adjusted using the nCGTempCo/nADCCfg register if nNVCfg1.enMtl = 1. Note that copper trace current sensing cannot be enabled at the same time as custom ADC Configuration. For 1-ounce copper, a length-to-width ratio of 6:1 creates a 0.0035Ω sense resistor which is suitable for most applications. Table 101 summarizes the IC setting for copper trace sensing.

Table 101. Copper Trace Sensing

PARAMETER	SETTING	RESULT
nNVCfg1.enADCCfg	0	ADC Configuration defaulted.
nNVCfg1.enMet	1	Sense resistor temperature compensation enabled.
nNVCfg2.enMlt	0	Sense resistor temperature compensation set to default of 0.4% per °C (typical copper).
nRense	0x012C	Sense resistor indicator to host software set to 3.5mΩ.
R_{SENSE} Size	6:1	A 6:1 length-to-width ratio of 1oz copper gives a resistance of 3.5mΩ.

MinCurr Register (0AEh)

Register Type: Current

Nonvolatile Backup: None

The MinCurr register maintains the minimum discharge Current register value within a 45-second period or until cleared by the host software. Each time the Current register updates, it is compared against its value. If the reading is less than the minimum, the corresponding value is replaced with the new reading. At power-up, MinCurr value is set to 0 (maximum discharge current). Therefore, the value is changed to the Current register reading after the first update during discharge. The host software can reset this register by writing it to its power-up value of 0. LSB is 1.5625µV/R_{SENSE}.

Temperature Measurement

The IC can be configured to measure its own internal die temperature and an external NTC thermistor. See the *nPackCfg* register for details.

Every 1.4s the IC biases the external thermistor with an internal trimmed pullup. After the pullup is enabled, the IC waits for a settling period of tPRE before making measurements on the TH pin. Measurement results are converted to a ratiometric value from 0% to 100%. The active pullup is disabled when temperature measurements are complete. This feature limits the time the external resistor-divider network is active and lowers the total amount of energy used by the system.

The ratiometric results are converted to temperature using logarithmic thermistor resistance translation each time the TH pin is measured. Internal die temperature measurements are factory calibrated and are not affected by *nThermCfg* register settings. Proper *nThermCfg* configuration is needed to achieve thermistor accuracy from -40ºC to +85ºC.

Additionally, the IC maintains a record of the minimum and maximum temperature measured and an average temperature over a time period defined by the host.

Temperature Measurement Timing

Temperature measurement channels are individually enabled using the nPackCfg register. A/D measurement order and firmware post-processing determine when a valid reading becomes available to the user. In addition, not all channels are measured each time through the firmware task loop. Selection options for enabled channels create a large number of possible timing options. Table 102 shows the timing for all temperature measurements made by the IC for some typical pack configurations. All times in this table are considered typical.

Table 102. Temperature Measurement Timing

APPLICATION	nPackCfg SETTING	REGISTER	FIRST UPDATE AFTER RESET	UPDATE RATE IN ACTIVE MODE[1]	UPDATE RATE IN HIBERNATE MODE[2]
Die Temperature Only	nPackCfg.A1En = 0	Temp, IntTemp, AvgIntTemp	550ms	351ms	1.4s
		AvgTA		351ms	
Die Temperature and Thermistor	nPackCfg.A1En = 1	IntTemp, Temp1, Temp, AvgIntTemp, AvgTemp1	550ms	1406ms	5.625s
		AvgTA		351ms	1.4s

1. Not all registers update at the same time. Updates are staggered to one channel per task period. Update order is IntTemp and Temp.

2. Hibernate mode update times assume the recommended nHibCfg.HibScalar setting of four task periods.

Temp Register (01Bh)

Register Type: Temperature

Nonvolatile Backup: None

The Temp register is the input to the fuel gauge algorithm. The Temp register reflects the thermistor or die temperature as configured in nPackCfg.

AvgTA Register (016h)

Register Type: Temperature

Nonvolatile Backup: None

The AvgTA register reports an average of the readings from the Temp register. Averaging period is configurable from 6 minutes up to 12 hours as set by the FilterCfg register. The first Temp register reading after returning to active mode sets the starting point of the averaging filters.

MaxMinTemp Register (009h)

Register Type: Special

Nonvolatile Backup: Periodically saves to nMaxMinTemp (1ADh) if nNVCfg2.enMMT is set, but does not restore from nonvolatile memory.

Alternate Initial Value: 0x807F

The MaxMinTemp register maintains the maximum and minimum Temp register (008h) values since the last fuel-gauge reset or until cleared by host software. It is compared against these values each time the Temp register updates. If the reading is larger than the maximum or less than the minimum, the corresponding values are replaced with the new reading. At power-up, the maximum value is set to 80h (minimum) and the minimum value is set to 7Fh (maximum). Therefore, both values are changed to the Temp register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum temperatures are each stored as two's complement 8-bit values with 1°C resolution. Table 103 shows the format of the register.

Table 103. MaxMinTemp (009h)/nMaxMinTemp (1ADh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 103. MaxMinTemp (009h)/nMaxMinTemp (1ADh) Register Format (continued)

MaxTemperature	MinTemperature

MaxTemperature: Maximum Temp register reading (1ºC resolution)

MinTemperature: Minimum Temp register reading (1ºC resolution)

MaxMinTemp is not cumulative across the entire battery lifetime. After each periodic nonvolatile memory save, MaxMinTemp resets to 0x807F to find the next maximum and minimum temperatures across the next segment of battery life. This behavior helps provide a useful log across the battery lifetime where each log segment shows the maximum and minimum temperature experienced across only that segment.

nThermCfg Register (1CAh)

Factory Default Value: 71BEh

External NTC thermistors generate a temperature-related voltage measured at the TH/TH2 pins. Set nThermCfg register to compensate the thermistor for accurate translation of temperature.

Table 104 lists common NTC thermistors with their associated Beta value and the nThermCfg value. The thermistors in the table translate within ±1°C from -40°C to +85°C. For other thermistors, use the equation in Table 104 to translate within ±2.5°C.

Table 104. Register Settings for Common Thermistor Types

THERMISTOR	R_{25C}(kΩ)	BETA at 25°C to 85°C	nThermCfg
Murata NCP15XH103F03RC	10	3435	71E8h
Semitec 103AT-2	10	3435	91C3h
TDK B57560G1103 7003	10	3610	5183h
Murata NCU15WF104F6SRC	100	4250	48EBh
NTC TH11-4H104F	100	4510	08D9h
TDK NTCG064EF104FTBX	100	4225	58EFh
Other 10K	10	nThermCfg = 7000h + (3245919/Beta[1] - 512)	
Other 100K	100	nThermCfg = 3000h + (3245919/Beta[1] - 512)	

1. Use Beta 25°C to 85°C.

DieTemp (034h) Register

Register Type: Temperature

Nonvolatile Backup: None

This register displays temperature in degrees Celsius, ±128ºC, or 1ºC in the high-byte, or 1/256ºC LSB.

AvgDieTemp (040h) Register

Register Type: Temperature

Nonvolatile Backup: None

The AvgDieTemp register reports a 4-sample filtered average of the DieTemp register.

FETTemp (015h) Register

Register Type: Temperature

Nonvolatile Backup: None

This register displays FET temperature in degrees Celsius, ±128ºC, or 1ºC in the high-byte, or 1/256ºC LSB.

FETTemp is used during charge regulation to regulate/limit the FET temperature during charging.

When a second thermistor is not installed and enabled, FETTemp simply equals DieTemp, and DieTemp is used as an

approximation for FET temperature.

When a second thermistor is installed, FETTemp is calculated by the temperature measured at TH2 and exaggerated according to the thermal gradient observed between TH2 and DieTemp. The gradient helps estimate the "unseen temperature" inside the FET (which is always hotter than any directly measurable temperature) according to the following equation:

FETTemp = TH2_Temp + (TH2_Temp - DieTemp) x FetTheta

The FetTheta range is 0 to 4.0 with 0.125 steps.

See also the *nChgCfg1* and *nPackCfg* for more details to enable and configure the FET thermistor.

Power

Power Register (0B1h)

Instant power calculation from immediate current and voltage. LSB is 0.8mW with a 10mΩ sense resistor.

AvgPower Register (0B3h)

Filtered Average Power from the power register. LSB is 0.8mW with a 10mΩ sense resistor. Filter bits located in Config2.POWR.

nADCCfg Register (1C9h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

Set Config.FastADCen = 1 and nNVCfg2.enMet = 0, to use nADCCfg to set the the ADC for longer samples which reduce sample noise at the expense of quiescent current.

Table 105. nADCCfg (0x1C9) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TermEn	ChgTermEn	0	1	0	0	nTerm			0	0	0	0	0	0	0

Default value: 0x5188

Standard configuration for ADC averaging count select is fixed 4ms. With nADCCfg settings, longer than 4ms ADC conversions are possible and result in less noisy ADC readings.

Default value for nADCCfg reduces VCell noise by 4x (64ms), PCKP/Temp noise by 3x (32ms)

ChgTermEn: ADC Changes are only enabled during charging. Current consumption is not sensitive while the charge source is present. ADC behavior is returned back to 4ms sampling when the charge source is removed.

TermEn: ADC Changes are always on. This has significant current consumption impact and is not recommended.

nTerm: ADC averaging count select.

(0, 1, 2, 3, 4, 5, 6, or 7) setting of nMaxTerm/nTerm corresponds to (4, 8, 16, 32, 64, 128, 256, or 512)ms per ADC channel conversion, respectively.

256ms, 512ms choices are not recommended to avoid timekeeping issues.

Status and Configuration Registers

The following registers control IC operation not related to the fuel gauge such as power-saving modes, nonvolatile backup, and ALRT pin functionality.

DevName Register (021h)

Register Type: Special

Nonvolatile Backup: None

The DevName register holds firmware revision information. This allows the host software to easily identify the type of IC being communicated with. Table 106 shows the DevName register format.

Table 106. DevName Register (021h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Revision															

The DevName for the IC is 0x4130.

nROMID0 (1BCh)/nROMID1 (1BDh)/nROMID2 (1BEh)/nROMID3 (1BFh) Registers

Register Type: Special

Nonvolatile Restore: There are no associated restore locations for these registers.

Each MAX17332 IC contains a unique 64-bit identification value that is contained in the nROMID registers. The unique ID can be reconstructed from the nROMID registers as shown in Table 107.

Table 107. nROMID Registers (1BCh to 1BFh) Format

NROMID3[15:0]	NROMID2[15:0]	NROMID1[15:0]	NROMID0[15:0]
ROM ID [63:48]	ROM ID [47:32]	ROM ID [31:16]	ROM ID [15:0]

Status Register (000h)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0002

The Status register maintains all flags related to alert thresholds. Table 108 shows the Status register format.

Table 108. Status Register (000h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PA	Smx	Tmx	Vmx	CA	Smn	Tmn	Vmn	dSOCi	Imx	AllowChgB	X	Bst	Imn	POR	X

POR: Power-On Reset. This bit is set to 1 when the device detects that a software or hardware POR event has occurred. This bit must be cleared by the system software to detect the next POR event. POR is set to 1 at power-up.

Imn: Minimum Current Alert Threshold Exceeded. This bit is set to 1 whenever a Current register reading is below the minimum IAlrtTh value. This bit is cleared automatically when Current rises above minimum IAlrtTh value. Imn is set to 0 at power-up.

Bst: Battery Status. Useful when the IC is used in a host-side application. This bit is set to 0 when a battery is present in the system and set to 1 when the battery is absent. Bst is set to 0 at power-up.

Imx: Maximum Current Alert Threshold Exceeded. This bit is set to 1 whenever a Current register reading is above the maximum IAlrtTh value. This bit is cleared automatically when Current falls below the maximum IAlrtTh value. Imx is set to 0 at power-up.

dSOCi: State of Charge 1% Change Alert. This is set to 1 whenever the RepSOC register crosses an integer percentage boundary such as 50%, 51%, etc. Must be cleared by the host software. dSOCi is set to 0 at power-up.

Vmn: Minimum Voltage Alert Threshold Exceeded. This bit is set to 1 whenever a VCell register reading is below the minimum VAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.VS bit description. Vmn is set to 0 at power-up.

Tmn: Minimum Temperature Alert Threshold Exceeded. This bit is set to 1 whenever a Temperature register reading is below the minimum TAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.TS bit description. Tmn is set to 0 at power-up.

Smn: Minimum SOC Alert Threshold Exceeded. This bit is set to 1 whenever SOC falls below the minimum SAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.SS and MiscCFG.SACFG bit descriptions. Smn is set to 0 at power-up.

Vmx: Maximum Voltage Alert Threshold Exceeded. This bit is set to 1 whenever a VCell register reading is above the maximum VAlrtTh value. This bit may or may not need to be cleared by the system software to detect the next event.

See the Config.VS bit description. Vmx is set to 0 at power-up.

Tmx: Maximum Temperature Alert Threshold Exceeded. This bit is set to 1 whenever a Temperature register reading is above the maximum TAlrtTh value. This bit may or may not need to be cleared by the system software to detect the next event. See the Config.TS bit description. Tmx is set to 0 at power-up.

Smx: Maximum SOC Alert Threshold Exceeded. This bit is set to 1 whenever SOC rises above the maximum SAlrtTh value. This bit may or may not need to be cleared by the system software to detect the next event. See the Config.SS and MiscCFG.SACFG bit descriptions. Smx is set to 0 at power-up.

PA: Protection Alert. This bit is set to a 1 when there is a protection event. The details of each protection event can be found in the ProtAlrt register. This bit must be cleared by the system software to detect the next protection event. However, before clearing this bit, the ProtAlrt register must first be written to 0x0000. ProtAlrt is set to 0 at power-up.

CA: Charging Alert. This bit is set to a 1 when there is a CP or CT or Dropout event. The details of each charging event can be found in the Chgstat register. This bit must be cleared by the system software to detect the next event. Chgstat updates every 351ms and does not require interaction from the system software to clear it.

AllowChgB: Allow Charge Bar. The AllowChgB bit is used for managing the charging or discharging of multiple batteries in parallel and is enabled by setting *nPackCfg*.ParEn = 1. Clear this bit to 0 to allow charging as well as block discharging when Config2.BlockDis = 1. This bit must be cleared every 1.4 seconds for continuous charging or continuous discharge blocking.

X: Don't Care. This bit is undefined and can be logic 0 or 1.

Status2 Register (0B0h)

Register Type: Special

Nonvolatile Backup: None

Initial Value: 0x0000

The Status2 register maintains status of hibernate mode. Table 109 shows the Status register format.

Table 109. Status2 Register (0B0h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hib	x

Hib: Hibernate Status. This bit is set to 1 when the device is in hibernate mode or 0 when the device is in active mode. Hib is set to 0 at power-up.

X: Don't Care. This bit is undefined and can be logic 0 or 1.

nI2CCfg Register (1B4h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nI2CCfg register manages settings for I^2C and SBS mode operation of the IC. Table 110 shows the register format.

Table 110. nI2CCfg Register (1B4h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CapMd	X	X	X	X	X	X	X	X	X	SDA_OUT	DIS_SLT	WPen	MECfg		X

X: Don't Care. This bit is undefined and can be logic 0 or 1.

WPen: Write Protection Enable. WPen = 0 (Default) to enable write protection.

DIS_SLT: Disable Slave Timeout. DIS_SLT = 0 to enable slave timeout where slave stops communicating and drops off the bus after 30mS of SCL low duration. DIS_SLT = 1 (Default) to disable the slave timeout.

SDA_OUT: Enable SDA output to PFail pin. Set SDA_OUT = 1 to enable PFAIL pin to become open-drain for SDA and SDA pin is input only. SDA pin is bi-drectional when SDA_OUT is 0 (Default).

MECfg: Configures sMaxError register output when operating in SBS mode.

00: Always report 0% error

01: Always report 1% error

10: Report actual experienced error

11: Always report 3% error

CapMd: Selects sBatteryMode.CapMd bit default setting when operating in SBS mode. CapMd resets to 0 every time a pack removal occurs as detected by floating communication lines.

nPackCfg Register(1C7h)

Register Type: Special

The nPackCfg register configures the voltage and temperature inputs to the A/D and also to the fuel gauge. nPackCfg configuration must match the pack hardware for proper operation of the IC. Table 111 shows the register format. The factory default for nPackCfg is 0x2000.

Table 111. nPackCfg (1C7h) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	S_Hib	THCfg		THType	000			En1w	ParEn	I2CSid		0000			

I2CSid: Configure the primary I²C slave address and secondary slave address with this bit field. The primary slave address applies to all registers with a leading "0" in the register address, for example, **0**22h. The secondary slave address applies to all registers with a leading "1" in the register address, for example, **1**AAh.

Note: When entering Ship, DeepShip, and DeepShip2/UVShutdown, it is important for the IC to fully enter the low-power mode before returning to active mode (based on nDelayCfg.ShutdownTimer setting), otherwise the slave address may return to the 6Ch/16h slave addresses. If this occurs, sending a Fuel Gauge Reset command to the 6Ch slave address returns the IC to the nPackCfg.I2CSid setting.

Note: The addresses shown in Table 112 are 8-bit slave addresses.

En1w: Enable 1-Wire interface.

Table 112. I²C Address Configuration

I2CSID	PRIMARY ADDRESS (REGISTERS 0__h)	SECONDARY ADDRESS (REGISTERS 1__h)
0b00	6Ch	16h
0b01	ECh	96h
0b10	64h	1Eh
0b11	E4h	9Eh

ParEn: Enable parallel charging feature. See the *Parallel Management* section for details.

THType: If using 10kΩ NTC thermistor, set THType = 0. If using 100kΩ NTC thermistor, set THType = 1. See *nThermCfg* for additional details.

THCfg: THCfg sets the Thermistor behavior.

Table 113. Thermistor Configuration

THCFG	BEHAVIOR
0b00	Both thermistor channels disabled. Temp and FETTemp are measured from DieTemp.
0b01	Thermistor 1 is used as battery temperature, Thermistor 2 is used with DieTemp for calculating FETTemp.
0b10	Thermistor 1 is enabled. FETTemp is copied from DieTemp.
0b11	Invalid. Do not set.

S_Hib: Ship-Mode Hibernate. Set S_Hib = 1 to use hibernate operation during ship-mode. Set S_Hib = 0 for full-shutdown during ship-mode (DeepShip or DeepShip2, see nProtCfg). In Hibernate mode, the fuel gauge functionality is active, and the battery state is continually updated.

I2CCmd Register(12Bh)

Register Type: Special

The I2CCmd register changes the primary and secondary slave addresses of MAX17332. To change the slave ID, configure the Alert pin to a logic HIGH or LOW, write the target GoToSID and IncSID bits, and wait 1.4s. Table 114 shows the register format. If the Alert pin is logic HIGH, the I^2C addresses of the device change to the addresses listed in the ALERT HIGH column of Table 115. If the Alert pin is logic LOW, the I^2C addresses of the device change to the addresses listed in the ALERT LOW column of Table 115. If multiple MAX17332 devices are sharing the same I^2C bus, the Alert pin on one device should be set to logic LOW and the others set to logic HIGH, allowing the devices to move to different I^2C slave addresses.

Table 114. I2CCmd (12Bh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0										GoToSID		0			IncSID

GoToSID: Configure the primary I^2C slave address and secondary slave address with this bit field. The primary slave address applies to all registers with a leading "0" in the register address, for example, 022h. The secondary slave address applies to all registers with a leading "1" in the register address, for example, 1AAh. **Note:** The addresses shown in Table 115 are 8-bit slave addresses.

Table 115. GoToSID Address Configuration

GoToSID	ALERT HIGH	ALERT LOW
—	Primary/Secondary Address	Primary/Secondary Address
0b00	ECh/96h	6Ch/16h
0b01	64h/1Eh	ECh/96h
0b10	E4h/9Eh	64h/1Eh
0b11	6Ch/16h	E4h/9Eh

IncSID: Set to 1 to incremement the Slave ID as defined in the GoTOSID bitfield.

nConfig Register (1B0h)

Register Type: Special

Nonvolatile Restore: Config (00Bh) and Config2 (0ABh) if nNVCfg0.enCfg is set.

Alternate Initial Value: 0x2204 for Config, 0x2058 for Config2

The nConfig register holds all shutdown enable, alert enable, and temperature enable control bits. Writing a bit location enables the corresponding function within one task period. Table 116, Table 117, and Table 118 show the register formats.

Table 116. nConfig Register (1B0h) Format

D15	D14	D13	D12	D11	D10	D9	D8
PAen	SS	TS	VS	0	PBen	DisBlockRead	ParChgBBM
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AtRateEn	COMMSH	FastADCen	OCVQEn	FTHRM	Aen	dSOCen	TAlrtEn

Table 117. Config Register (00Bh) Format

D15	D14	D13	D12	D11	D10	D9	D8
ManChg	SS	TS	VS	0	PBen_status	DisBlockRead	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SHIP	COMMSH	FastADCen	OCVQEn	FTHRM	Aen	CAen	PAen

Table 118. Config2 Register (0ABh) Format

D15	D14	D13	D12	D11	D10	D9	D8
POR_CMD	0	AtRtEn	0	POWR			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
dSOCen	TAlrtEn	0	1	DRCfg		CPMode	BlockDis

0: Bit must be written 0. Do not write 1.

1: Bit must be written 1. Do not write 0.

BlockDis: Block Discharge. The BlockDis bit is used for managing the discharging of multiple batteries in parallel and is enabled by setting nPackCfg.ParEn = 1. Set to 1 and clear Status.BlockChg to enable blocking of discharge current. See the *Parallel Battery Management* for more detail.

PAen: Protection Alert Enable. Set PAen = 1 to drive the ALRT pin low on protection fault events. Additionally, enable this feature that saves the protector faults (TooHotC, TooColdC, OVP, OCCP, DieHot, TooHotD, UVP, ODCP, LDet) into the low byte of the nBattStatus register. After each life logging write to NVM, the low byte of nBattStatus is cleared

CAen: Charge Alerts Enable. Set CAen = 1 to drive the ALRT pin low on droput or heat limit alerts. Config.Aen must be set 1 to allow this function.

PBEn: PushButton Enable. Set PBEn = 1 to enable wakeup by pushbutton. This application allows a gadget to be completely sealed with the battery disconnected until a shared system button is pressed.

PBEn_status: PushButton Enable Status. PBen_status = 1 when nConfig.PBEn = 1. nConfig.PBen must be 1 to enable the pushbutton wakeup function.

DisBlockRead: Disable SBS Block Read. Set DisBlockRead to 1 for normal read access in the 16h memory space. Clear DisBlockRead to 0 to enable SBS block reads when SBS Mode is enabled with nNVCfg0.SBSen. The default setting for DisBlockRead is 1.

ParChgBBM: Parallel Charging Break-Before-Make ending option.

When the host stops allowing charging and block discharging cmd remains 1,

0, block charging and allow discharging change at the same time.

1, block charging comes first and then 0.351ms delay release discharging. Support break-before-make, avoid cross-charging, and system may crash if an emptier battery cannot support system load.

Aen: Enable alert on fuel-gauge outputs. When Aen = 1, a violation of any of the alert threshold register values by temperature, voltage, or SOC triggers an alert. This bit affects the ALRT pin operation only. The Smx, Smn, Tmx, Tmn, Vmx, Vmn, Imx, and Imn bits of the Status register (000h) are not disabled.

FTHRM: Force Thermistor Bias Switch. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal. Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional ~200µA to the current drain of the circuit.

FastADCen: Enable FastADC. Set to logic 1 to enable the FastADC feature.

COMMSH: Communication Shutdown. Set to logic 1 to force the device to enter shutdown mode if both SDA and SCL are held low. This also configures the device to wake up on the rising edge of any communication. See Table 9.

SHIP: Ship or Deepship Command. Write this bit to logic 1 to force into ship or deepship mode based on nProtCfg.DeepShpEn after timeout of the Shutdown Timer register which is configured in nDelayCfg.UVPTimer. SHIP is reset to 0 at power-up and upon exiting ship or deepship mode.

VS: Voltage ALRT Sticky. When VS = 1, voltage alerts can only be cleared through software. When VS = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded.

TS: Temperature ALRT Sticky. When TS = 1, temperature alerts can only be cleared through software. When TS = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded.

SS: SOC ALRT Sticky. When SS = 1, SOC alerts can only be cleared through software. When SS = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded.

ManChg: Manual Charge Control. When ManChg = 1, host controls the charging voltage/charging current by directly writing the ChargingVoltage/ChargingCurrent registers and the IC does not automatically update the ChargingVoltage/ ChargingCurrent registers.

POR_CMD: Firmware Restart. Set this bit to 1 to restart IC firmware operation without performing a recall of nonvolatile memory into RAM. This allows different IC configurations to be tested without changing nonvolatile memory settings. This bit is set to 0 at power-up and automatically clears itself after firmware restart.

TAlrten: Temperature Alert Enable. Set this bit to 1 to enable temperature-based alerts. Write this bit to 0 to disable temperature alerts. This bit is set to 1 at power-up.

dSOCen: SOC Change Alert Enable. Set this bit to 1 to enable the Status.dSOCi bit function. Write this bit to 0 to disable the Status.dSOCi bit. This bit is set to 0 at power-up.

CPMode: Constant-power mode. Set to 1 to enable constant-power mode.

DRCfg: Deep Relax Time Configuration. 00 for 0.8 to 1.6 hours, 01 for 1.6 to 3.2 hours, 10 for 3.2 to 6.4 hours, and 11 for 6.4 to 12.8 hours.

OCVQEn: OCV Empty Compensation Enable. Set OCVQEn=1 to enable automatic empty compensation based on VFOCV information. Enable this feature for EZConfig. For custom model, follow characterization guidance.

AtRateEn: AtRate Enable. Set this bit to 1 to enable the AtRate functionality.

POWR: Sets the time constant for the AvgPower register. The default POR value of 0000b gives a time constant of 0.7s. The equation setting the period is:

AvgPower time constant = $45s \times 2^{(POWR-6)}$

nHibCfg Register (1BBh)

Register Type: Special

Nonvolatile Restore: None

The nHibCfg register controls hibernate mode functionality. The IC enters hibernate mode if the measured system current falls below the HibThreshold setting for longer than the HibEnterTime delay. While in hibernate mode, the IC reduces its operating current by slowing down its task period as defined by the HibScalar setting. The IC automatically returns to active mode of operation if current readings go above the HibThreshold setting for longer than the HibExitTime delay. Table 119 shows the register format.

Table 119. nHibCfg Register (1BBh) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EnHib	HibEnterTime			HibThreshold				0	0	0	HibExitTime		HibScalar		

0: Bit must be written 0. Do not write 1.

HibScalar: Sets the task period while in hibernate mode based on the following equation:

Hibernate Mode Task Period(s) = $702ms \times 2^{(HibScalar)}$

HibExitTime: Sets the required time period of consecutive current readings above the HibThreshold value before the IC exits hibernate mode and returns to active mode of operation.

Hibernate Mode Exit Time(s) = $(HibExitTime + 1) \times 702ms \times 2^{(HibScalar)}$

HibThreshold: Sets the threshold level for entering or exiting hibernate mode. The threshold is calculated as a fraction of the full capacity of the cell using the following equation:

Hibernate Mode Threshold(mA) = $(FullCap(mAh)/0.8 \text{ hours})/2^{(HibThreshold)}$

HibEnterTime: Sets the time period that consecutive current readings must remain below the HibThreshold value before the IC enters hibernate mode as defined by the following equation. The default HibEnterTime value of 000b causes the IC to enter hibernate mode if all current readings are below the HibThreshold for a period of 5.625 seconds, but the IC could enter hibernate mode as quickly as 2.812 seconds.

$2.812s \times 2^{(HibEnterTime)} <$ Hibernate Mode Entry Time $< 2.812s \times 2^{(HibEnterTime + 1)}$

EnHib: Enable Hibernate Mode. When set to 1, the IC enters hibernate mode if conditions are met. When set to 0, the

IC always remains in active mode of operation.

nRSense Register (19Ch)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

The nRSense register is the designated location to store the sense resistor value used by the application. This value is not used by the IC as all current and capacity information is reported in terms of µV and µVh. Host software can use the lower byte of the nRSense register value as shown in Table 120 to convert current and capacity information into mA and mAh. It is recommended that the sense resistor value be stored with an LSb weight of 1mΩ giving a range of 1mΩ to 255mΩ. The upper byte is User Memory. Table 121 shows recommended register settings based on common sense resistor values.

Table 120. nRsense Register (19Ch) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
UserMemory								RSense							

Table 121. Recommended nRSense Register Values for Common Sense Resistors

SENSE RESISTOR (Ω)	nRSense REGISTER
0.005	0x0005
0.010	0x000A
0.020	0x0014

nDesignVoltage Register (1E3h)

Register Type: Special

Nonvolatile Restore: There is no associated restore location for this register.

Table 122. nDesignVoltage Register (1E3h) Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Vminsys								Vdesign							

Vminsys: (unsigned byte) = Minimum system voltage specification for the design. Generates MinSysVoltage value.

Vdesign: (unsigned byte) = Design voltage specification for the design.

Each byte has a LSB = 20mV (resolution) giving a full-scale range between 0V and 5.12V.

These values are used in Dynamic Power Calculations when enDP = 1.

AtRate Functionality

The AtRate function allows the host software to see theoretical remaining time or capacity for any given load current. AtRate can be used for power management by limiting system loads depending on the present conditions of the cell pack. Whenever the AtRate register is programmed to a negative value indicating a hypothetical discharge current, the AtQResidual, AtTTE, AtAvSOC, and AtAvCap registers display theoretical residual capacity, time-to-empty, state-of-charge, and available capacity respectively. The host software should wait two full task periods (703ms minimum in active mode) after writing the AtRate register before reading any of the result registers.

AtRate Register (004h)

Register Type: Current

Nonvolatile Backup: None

The host software should write the AtRate register with a negative two's-complement 16-bit value of a theoretical load current prior to reading any of the AtRate output registers.

AtQResidual Register (0DCh)

Register Type: Capacity

Nonvolatile Backup: None

The AtQResidual register displays the residual charge held by the cell at the theoretical load current level entered into the AtRate register.

AtTTE Register (0DDh)

Register Type: Time

Nonvolatile Backup: None

The AtTTE register can be used to estimate time-to-empty for any theoretical current load entered into the AtRate register. The AtTTE register displays the estimated time-to-empty for the application by dividing AtAvCap by the AtRate register value.

AtAvSOC Register (0CEh)

Register Type: Percentage

Nonvolatile Backup: None

The AtAvSOC register holds the theoretical state-of-charge of the cell based on the theoretical current load of the AtRate register. The register value is stored as a percentage with a resolution of 0.0039% per LSB. If a 1% resolution state-of-charge value is desired, the host can read only the upper byte of the register instead.

AtAvCap Register (0DFh)

Register Type: Capacity

Nonvolatile Backup: None

The AtAvCap register holds the estimated remaining capacity of the cell based on the theoretical load current value of the AtRate register. The value is stored in terms of µVh and must be divided by the application sense-resistor value in terms of mΩ to determine the remaining capacity in mAh.

Alert Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, current, temperature, or state-of-charge. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup resistor is required to generate a logic-high signal. Alerts can be triggered by any of the following conditions:

• Over/undervoltage—VAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).

• Over/undertemperature—TAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).

• Over/under current—IAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).

• Over/under SOC—SAlrtTr register threshold violation (upper or lower) and alerts enabled (Aen = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the Status (000h) register. Alerts generated by a threshold-level violation can be configured to be cleared only by the host software or cleared automatically when the threshold level is no longer violated. See the Config register description for details of the alert function configuration.

nVAlrtTh Register (18Ch)

Register Type: Special

Nonvolatile Restore: VAlrtTh (001h) if nNVCfg1.enAT is set.

Alternate Initial Value: 0xFF00 (Disabled)

The nVAlrtTh register shown in Table 123 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the VCell register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 20mV resolution over the full operating range of the VCell register. At power-up, the

thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 123. VAlrtTh (001h)/nVAlrtTh (18Ch) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VMAX								VMIN							

VMAX: Maximum voltage reading. An alert is generated if the VCell register reading exceeds this value. This field has 20mV LSb resolution.

VMIN: Minimum voltage reading. An alert is generated if the VCell register reading falls below this value. This field has 20mV LSb resolution.

nTAlrtTh Register (18Dh)

Register Type: Special

Nonvolatile Restore: TAlrtTh (002h) if nNVCfg1.enAT is set.

Alternate Initial Value: 0x7F80 (Disabled)

The nTAlrtTh register shown in Table 124 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the Temp register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are stored in 2's-complement format with 1ºC resolution over the full operating range of the Temp register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 124. TAlrtTh (002h)/nTAlrtTh (18Dh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TMAX								TMIN							

TMAX: Maximum temperature reading. An alert is generated if the Temp register reading exceeds this value. This field is signed 2's-complement format with 1ºC LSb resolution.

TMIN: Minimum temperature reading. An alert is generated if the Temp register reading falls below this value. This field is signed 2's-complement format with 1ºC LSb resolution.

nSAlrtTh Register (18Fh)

Register Type: Special

Nonvolatile Restore: SAlrtTh (003h) if nNVCfg1.enAT is set.

Alternate Initial Value: 0xFF00 (Disabled)

The nSAlrtTh register shown in Table 125 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the selected RepSOC, AvSOC, MixSOC, or VFSOC register values. See the MiscCFG.SACFG setting for details. The upper 8 bits set the maximum value and the lower 8 bits set the minimum value. Interrupt threshold limits are selectable with 1% resolution over the full operating range of the selected SOC register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 125. SAlrtTh (003h)/nSAlrtTh (18Fh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SMAX								SMIN							

SMAX: Maximum state-of-charge reading. An alert is generated if the selected SOC register reading exceeds this value. This field has 1% LSb resolution.

SMIN: Minimum state-of-charge reading. An alert is generated if the selected SOC register reading falls below this value. This field has 1% LSb resolution.

nIAlrtTh Register (0ACh)

Register Type: Special

Nonvolatile Restore: IAlrtTh (1ACh) if nNVCfg1.enAT is set.

Alternate Initial Value: 0x7F80 (Disabled)

The nIAlrtTh register shown in Table 126 sets upper and lower limits that generate an ALRT pin interrupt if exceeded by the Current register value. The upper 8 bits set the maximum value and the lower 8 bits set the minimum vaue. Interrupt threshold limits are selectable with 400µV resolution over the full operating range of the Current register. At power-up, the thresholds default to their maximum settings unless they are configured to be restored from nonvolatile memory instead by setting the nNVCfg1.enAT bit.

Table 126. IAlrtTh (0ACh)/nIAlrtTh (18Eh) Register Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CURRMAX								CURRMIN							

CURRMAX: Maximum Current Threshold. An alert is generated if the current register reading exceeds this value. This field is signed 2's-complement with 400µV LSb resolution to match the upper byte of the Current register.

CURRMIN: Minimum Current Threshold. An alert is generated if the current register reading falls below this value. This field is signed 2's-complement with 400µV LSb resolution to match the upper byte of the Current register.

Dynamic Battery Power Technology (DBPT) Registers

Many mobile systems with high-performance CPUs, GPUs, motors, radios, etc., require the battery to deliver short pulses of high power without the battery voltage falling below critical system undervoltage levels. Managing these pulse loads optimally without sacrificing performance is quite challenging without appropriate battery capability information being available to the system.

To achieve better run-time and to help the system run at optimal performance, Analog Devices has developed Dynamic Battery Power Technology (DBPT). The MAX17332 supports this DBPT feature, which provides the on-demand battery capability to be used for managing pulse loads. To support these high pulses without the battery voltage falling below critical system undervoltage levels, the MAX17332 indicates the instantaneous peak and sustained power levels that can be extracted safely from the battery. The system can use this information to set its maximum current in accordance with battery power capability. For example, in many applications, the system requires at least 3.3V to operate correctly. By configuring the MAX17332 for DBPT, the system's loads can be controlled or limited to stay within the battery's capability and ensure that a minimum system voltage (MinSysVolt) is not crossed until the battery is in a very low state.

The implementation of DBPT in the MAX17332 hews closely to Intel's Dynamic Battery Power Technology v2.0 standard and relies on specific functions and corresponding registers. This section defines those functions. The implementation in the MAX17332 includes all the same registers as the Intel spec. However, the MAX17332 register set uses different LSBs and addresses from the Intel standard.

The following registers are used for DBPT. The MAX17332 uses the standard current register format (0.15625µV/Sense Resistor) for current, 0.8mW for power, and 0.2441mΩ (precisely 1/4.096) for resistance.

MaxPeakPower Register (0A4h)

Specification Description:

The fuel gauge computes and returns the maximum instantaneous peak output power of the battery pack in cW, which is available for up to 10ms, given the external resistance and required minimum system voltage. The MaxPeakPower value is expected to be negative and is updated every 351mS. MaxPeakPower is initialized to the present value of MaxPeakPower on reset or power-up.

The system designer should limit the actual maximum peak power to account for various system limitations, such as limiting the cell discharge current to the 2C rate and allowing for the safe operating area specifications for devices in the power path, such as MOSFETs.

LSB is 0.8mW.

Actual Calculation:

MaxPeakPower = MPPCurrent x AvgVCell

SusPeakPower Register (0A5h)

Specification Description:

The fuel gauge computes and returns the sustained peak output power of the battery pack in cW, which is available for up to 10s, given the external resistance and required minimum voltage of the voltage regulator. The SusPeakPower value is expected to be negative and is updated every 351mS. SusPeakPower is initialized to the present value of SusPeakPower on reset or power-up.

The system designer should limit the actual sustained peak power to account for various system limitations, such as limiting the cell discharge current to the 2C rate and allowing for the safe operating area specifications for devices in the power path, such as MOSFETs.

LSB is 0.8mW.

Actual Calculation:

SusPeakPower = SPPCurrent x AvgVCell

nPackResistance (1E5h) and PackResistance (0A6h)

Specification Description:

The PackResistance register configures the total noncell pack resistance value to account for the resistances due to cell interconnect, sense resistor, FET, fuse, connector, and other impedances between the cells and output of the battery pack. The cell internal resistance should NOT be included. PackResistance is initialized to a default value from the nPackResistance at power up. nPackResistance is set in non-volatile memory at time of pack manufacture. Writes to nPackResistance register has no change to the value during normal operation. The system designer can write the PackResistance register during normal operation to change from the default setting. This value is usually determined by the battery pack manufacturer and set at time of pack manufacture.

The pack-maker can configure PackResistance by programming the nonvolatile nPackResistance during production.

LSB of 0.2441mΩ per LSB.

SysResistance (0A7h)

Specification Description:

The SysResitance register configures the total resistance value into fuel gauge to account for the resistances due to the resistance of power/ground metal, sense resistor, FET, and other parasitic resistance on the system main board. SysResistance is initialized to a default value of 0mΩ. The system designer is expected to overwrite the default value with the value from the system in question. This allows a single pack to be used in multiple systems which can have various values for SysResistance.

LSB of 0.2441mΩ per LSB

MinSysVoltage() (0A8h)

Specification Description:

The MinSysVoltage register configures the required minimum system input voltage in mV into the fuel gauge. The system regulator still operates normally if its input voltage is at this level. MinSysVoltage is initialized to a default value from the upper byte of the nDesignVoltage register at power up. Table 122 shows the register format for nDesignVoltage.

The system designer can write the MinSysVoltage register directly during normal operation to change from the default setting. This allows a single pack to be used in multiple systems, which may have various values for MinSysVoltage.

Writing MinSysVoltage above or below the empty point should not change the empty point. However, calculations for MPPCurrent, SPPCurrent, MaxPeakPower, and SusPeakPower reports 0x0000 when VCell is less than the MinSysVoltage.

For accurate performance, the system should normally update MinSysVoltage according to its requirements.

MPPCurrent (0A9h)

Register Type: Current

Specification Description:

The fuel gauge computes and returns the maximum instantaneous peak current of the battery pack in the standard current register format, which is available for up to 10ms, given the external resistance and required minimum voltage of the voltage regulator. The MPPCurrent value is expected to be negative and has to be updated at least once every second. MPPCurrent is initialized to the present value of MPPCurrent on reset or power-up.

Actual Calculation:

MPPCurrent = (AvgVCell - MinSySVoltage) / [(PackResistance + SysResistance) x Rgain1]

SPPCurrent (0AAh)

Register Type: Current

Specification Description:

The fuel gauge computes and returns the sustained peak current of the battery pack in the standard current register format, which is available for up to 10s, given the external resistance and required minimum system voltage. The SPPCurrent value is expected to be negative and has to be updated at least once every second. SPPCurrent is initialized to the present value of SPPCurrent on reset or power-up.

Actual Calculation:

SPPCurrent = (AvgVCell - MinSySVoltage) / (RCell x Rgain2)

nRGain Register (1B8h)

Register Type: Special

Recommended Initial Value: 0x8080

The nRGain register sets the value of RGain1, RGain2, and SusToPeakRatio during DBPT register calculation. Table 127 shows the register format.

Table 127. nRGain (1B8h) Format

D15	D14		D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Rg1									Rg2				SusToPeakRatio			

RGain1: Gain resistance used for maximum peak current and power calculation. RGain1 = 80% + (0.15625% x Rg1). The range of Rgain1 is between 80~120%.

RGain2: Gain resistance used for sustained peak current and power calculation. RGain2 = 60% + (5% x Rg2). The range of Rgain2 is between 60~140%.

SusToPeakRatio: Used to calculate the maximum ratio between SPPCurrent to MPPCurrent. The maximum value of SPPCurrent = MPPCurrent x (0.75-SusToPeakRatio x 0.04).

SHA-256 Authentication

The MAX17332 supports authentication which is performed using a FIPS 180-4 compliant SHA-256 one-way hash algorithm on a 512-bit message block. The message block consists of a 160-bit secret, a 160-bit challenge, and 192 bits of constant data. Optionally, the 64-bit ROM ID replaces 64 of the 192 bits of constant data used in the hash operation. Contact Analog Devices for details of the message block organization.

The host and the IC both calculate the result based on the mutually known secret. The result of the hash operation is known as the message authentication code (MAC) or message digest. The MAC is returned by the IC for comparison to the host's MAC. Note that the secret is never transmitted on the bus and thus cannot be captured by observing bus traffic. Each authentication attempt is initiated by the host system by writing a 160-bit random challenge into the SHA memory address space 0C0h to 0C9h. The host then issues the compute MAC or compute MAC with ROM ID command. The MAC is computed per FIPS 180-4 and stored in address space 0C0h to 0CFh, overwriting the challenge value.

The MAX17332 also provides a 2-stage authentication scheme that utilizes a temporary secret.

Note that the results of the authentication attempt are determined by host verification. Operation of the IC is not affected by authentication success or failure.

Authentication Procedure

Figure 30 shows how a host system verifies the authenticity of a connected battery. The host first generates a random 160-bit challenge value and writes the challenge to IC memory space 0C0h to 0C9h. The host then sends the Compute MAC with ROM ID (3500h) or Compute MAC without ROM ID (3600h) to the Command register 060h and waits t_{SHA} for computation to complete. Finally, the host reads the MAC from memory space 0C0h to 0CFh to verify the result. This procedure requires the secret to be maintained on the host side as well as in the battery. The host must perform the same calculations in parallel to verify that the battery is authentic.

Procedure to Verify a Battery

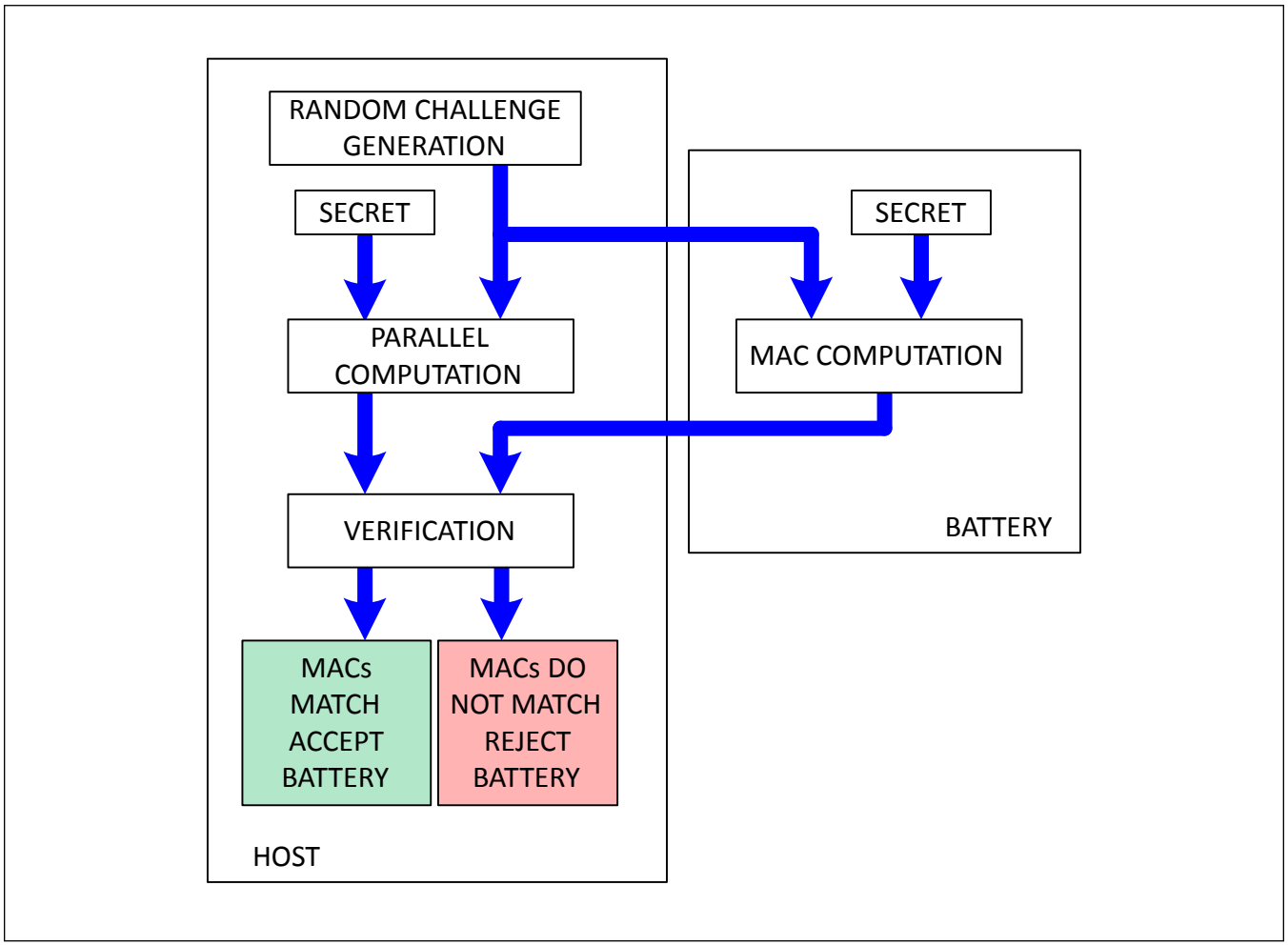


Figure 30. Procedure to Verify a Battery

Alternate Authentication Procedure

Figure 31 shows an alternative method of battery authentication that does not require the host to know the secret. In this method, each host device knows a challenge and MAC pair that matches the secret stored in an authentic battery, but each host device uses a different pair. This eliminates the need for special hardware on the host side to protect the secret from hardware intrusion. A battery could be cloned for a single host device, but creating a clone battery that works with any host would not be possible without knowing the secret.

The authentication process for this method is less complex. The host simply writes the challenge to IC memory space 0C0h to 0C9h. The host then sends the Compute MAC without ROM ID (3600h) command to the Command register 060h. Note that the Compute MAC with ROM ID command is not valid for this authentication method. The host then waits t_{SHA} for the computation to complete and reads the MAC from memory space 0C0h to 0CFh to verify the result.

Battery Authentication without a Host Side Secret

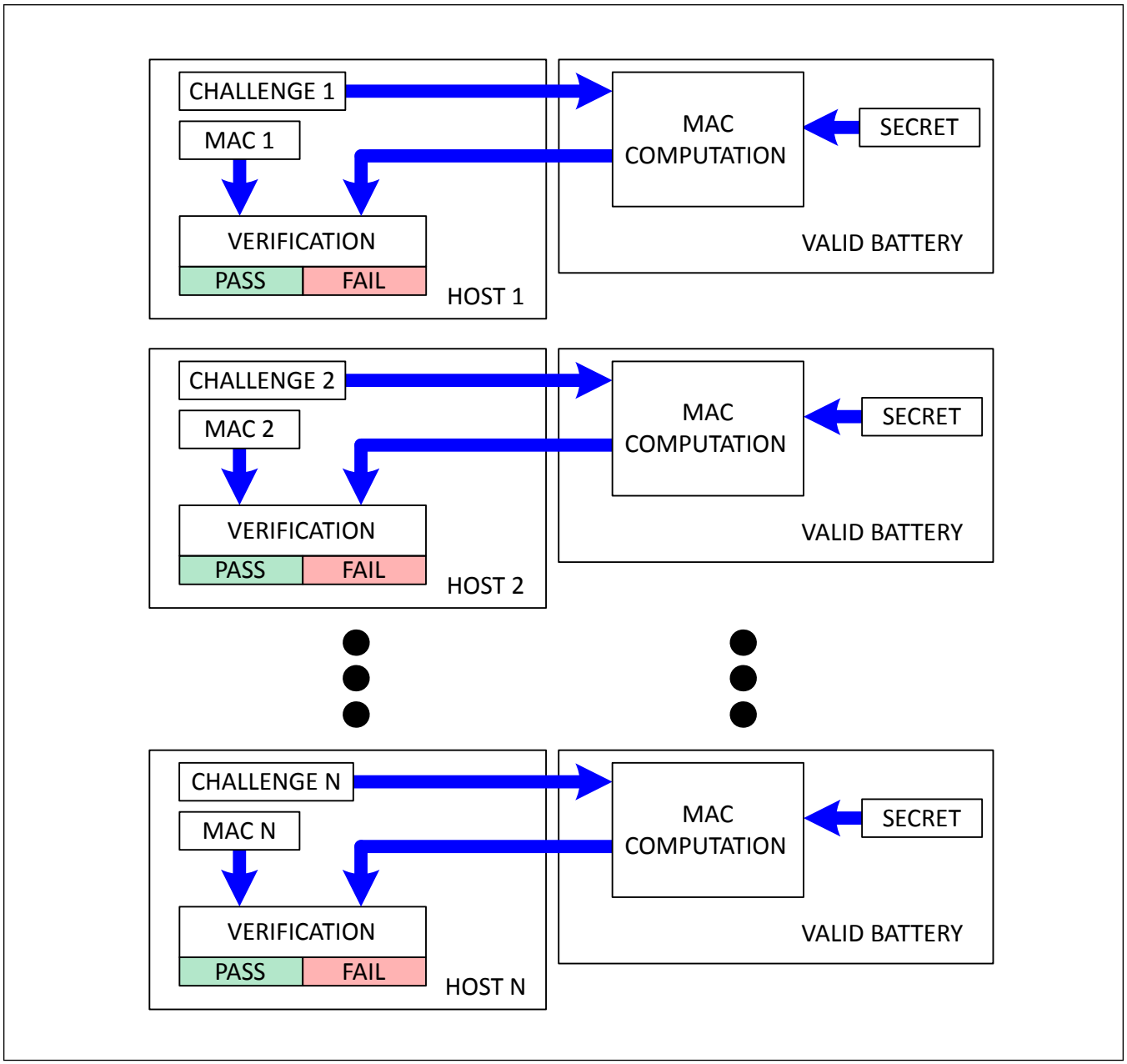


Figure 31. Battery Authentication without a Host Side Secret

Secret Management

The secret value must be programmed to a known value before performing authentication in the application. The secret cannot be written directly. Instead, the user must generate a new internal secret by performing a SHA computation with the old internal secret and a seed value sent as a challenge. To prevent any one entity from knowing the complete secret value, the process can be repeated multiple times by sending additional challenge seeds and performing additional computations.

Note that programming the Secret should be done at the factory before connecting the battery as 5.5V is required at the BATT pin of the IC to update the Secret in NVM.

Note that secret memory can only be changed a maximum of n_{SECRET} times including erase operations, and nonvolatile memory updates are not guaranteed. See the n_{SECRET} write limit in the *Electrical Characteristics* table. Any secret update operation that fails does not change the secret value stored in the IC but consumes one of the available limited updates. Be careful not to use up all secret memory during the generation process. Maxim Integrated strongly recommends permanently locking the secret after it has been generated.

Single-Step Secret Generation

The single-step secret generation procedure should be used in production environments where the challenge seed value can be kept confidential, for example when there are no OEM manufacturing steps or situations where an outside individual or organization would need to know the challenge seed. Use the following sequence to program the IC. Since the secret cannot be read from the IC, a parallel computation must be performed externally to calculate the stored secret. Figure 32 shows an example of a single-step secret generation operation. Note that new units have their secret value already cleared to all 0s. Also note that programming the Secret should be done at the factory before connecting the battery as 5.5V is required at the BATT pin of the IC to update the Secret in NVM.

1. Clear the CommStat.NVError bit.
2. Write a challenge seed value to the SHA memory space 0C0h to 0C9h.
3. Write Compute Next Secret with ROM ID 3300h or Compute Next Secret without ROM ID 3000h to the Command register 060h.
4. Wait t_{SHA} + t_{UPDATE} for the computation to complete and the new secret to be stored.
5. If CommStat.NVError is set, return to step 1; otherwise, continue.
6. Verify that the secret has been generated correctly with a test challenge at this time. If verification fails, return to step 1. See the *Determining Number of Remaining Updates* section to verify that enough nonvolatile memory writes remain to repeat the process.
7. Write Lock Secret 6000h to the Command register 060h. **Note that this operation cannot be reversed.**
8. Wait t_{UPDATE} for the secret to lock permanently.

Single-Step Secret Generation Example

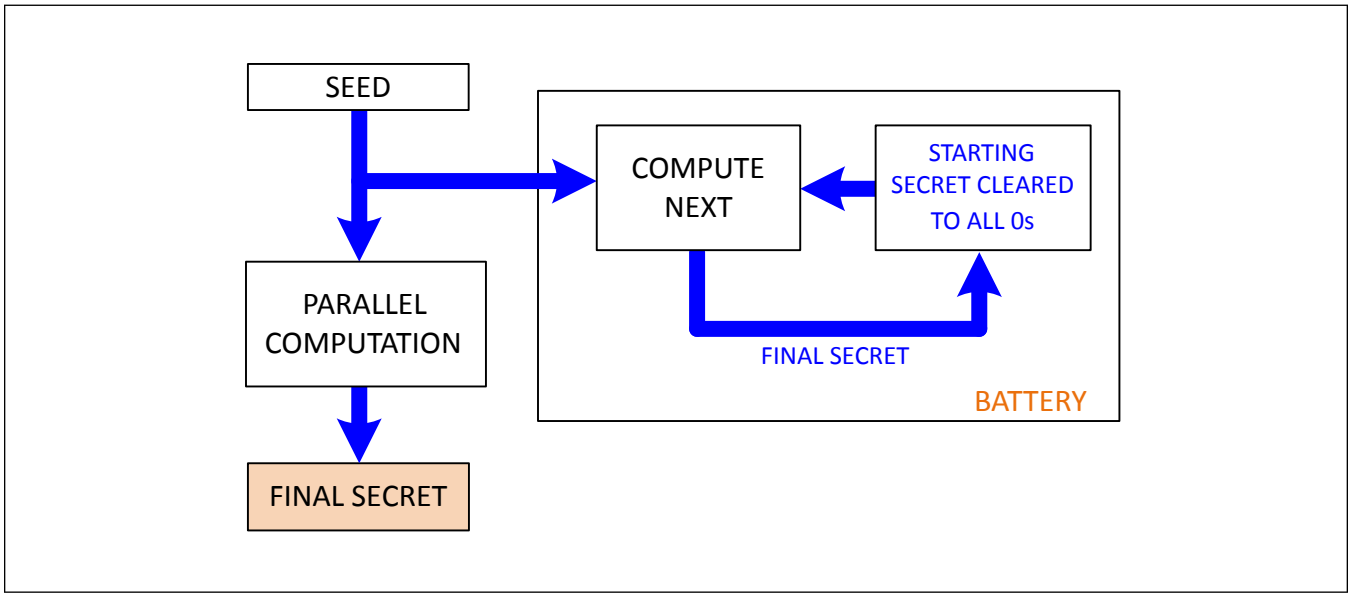


Figure 32. Single-Step Secret Generation Example

Multi-Step Secret Generation Procedure

The multi-step secret generation procedure should be used in environments where an outside individual or organization would need to know the challenge seed such as OEM manufacturing. The multi-step procedure is more complicated but allows a secret to be stored inside the IC without providing any information to an OEM that could jeopardize secret integrity. Figure 33 shows an example where three OEMs are each provided with a seed value for a Compute Next operation. The final secret value stored inside the IC is known only to the top-level manager who knows all seed values and has performed the computation separately. Use the following procedures when generating a multi-step secret. Note that the secret can only be updated or cleared n_{SECRET} times total. New units have their secret value already cleared to all 0s. Also, note that programming the Secret should be done at the factory before connecting the battery as 5.5V is required at the BATT pin of the IC to update the Secret in NVM.

All OEMs:

1. Clear the CommStat.NVError bit.
2. Write challenge seed value to the SHA memory space 0C0h to 0C9h.
3. Write Compute Next Secret with ROM ID 3300h or Compute Next Secret without ROM ID 3000h to the Command register 060h.
4. Wait t_{SHA} + t_{UPDATE} for the computation to complete and the new secret to be stored.
5. If CommStat.NVError is set, return to step 1; otherwise, continue.
6. Verify that the secret has been generated correctly with a test challenge at this time. If verification fails, return to step 1. See the *Determining Number of Remaining Updates* section to verify that enough nonvolatile memory writes remain to repeat the process.

Last OEM:

1. Follow the previous procedure for the final secret update.
2. Write Lock Secret 6000h to the Command register 060h. **Note that this operation cannot be reversed.**
3. Wait t_{UPDATE} for the secret to lock permanently.

Top Level:

1. Generate all seed values to provide to OEMs.
2. Perform SHA calculations separately to determine what the final secret is after all manufacturing steps.
3. Keep the final secret value secure.

Multi-Step Secret Generation Example

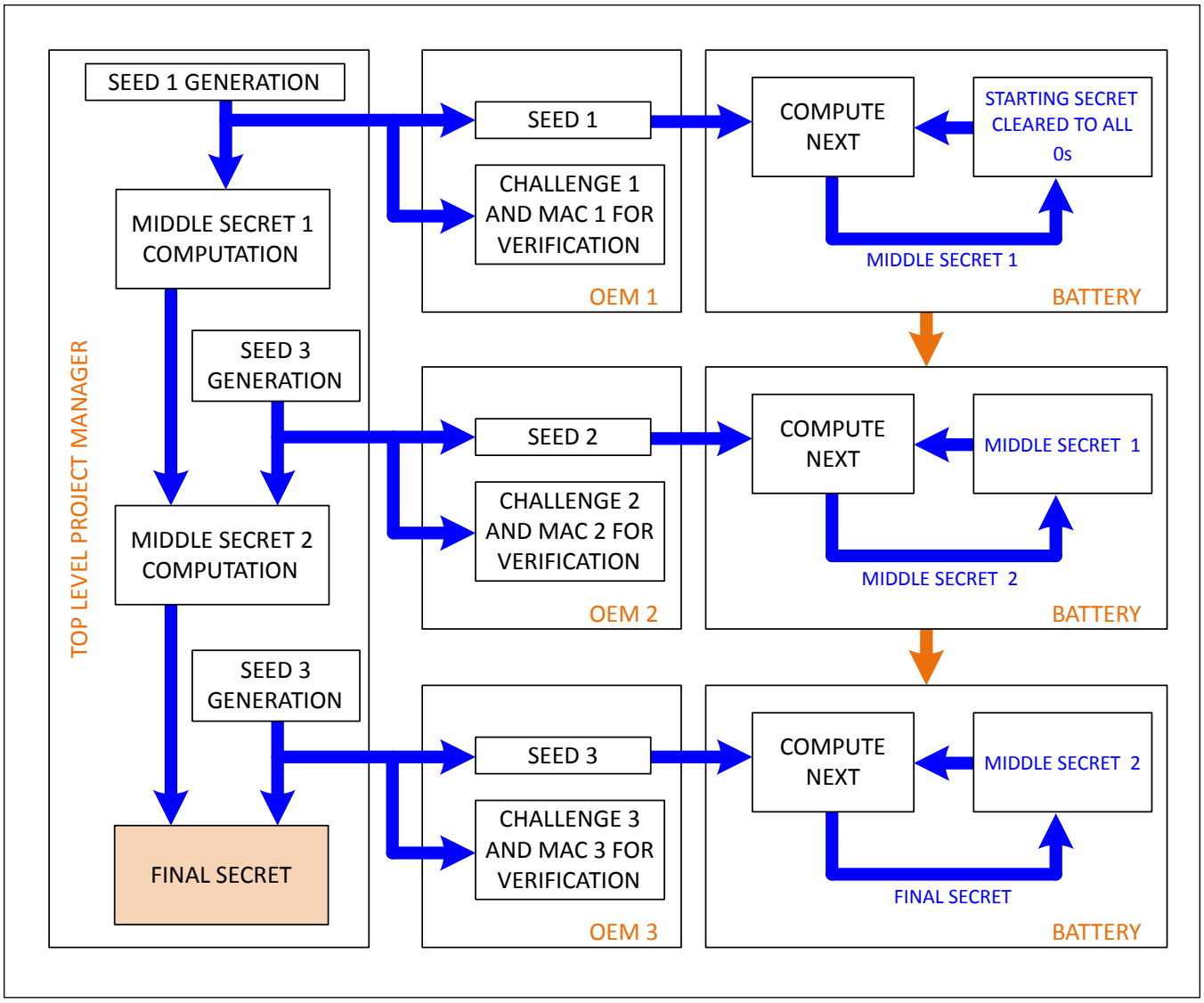


Figure 33. Multi-Step Secret Generation Example

2-Stage Authentication Scheme

The MAX17332 provides a 2-stage authentication scheme that utilizes a temporary secret for an added layer of security. Figure 34 illustrates how to create a unique intermediate secret that can be stored in the host at the factory. Figure 35 outlines the procedure to complete the 2-stage authentication.

The following procedure implements the 2-stage authentication scheme:

1. Write Copy Temporary Secret from NVM command 3800h to the Command register 060h.
2. Write unique challenge seed value to the SHA memory space 0C0h to 0C9h to be used to compute the next temporary secret.
3. Write Compute Next Temporary Secret with ROM ID 3900h or Compute Next Temporary Secret without ROM ID 3A00h to the Command register 060h.
4. Wait t_{SHA} for the computation to complete.

5. Write challenge seed value to the SHA memory space 0C0h to 0C9h to be used to compute the MAC using the temporary secret.
6. Write Compute MAC From Temporary Secret with ROM ID 3D00h or Compute MAC From Temporary Secret without ROM ID 3C00h to the Command register 060h.
7. Wait t_{SHA} for the computation to complete.
8. Read the MAC from SHA memory space 0C0h to 0CFh to verify the result.

Because the temporary secret is stored in the same RAM location used for SHA calculation, executing some commands overwrites the temporary secret. The functional impact is summarized as follows.

- Compute MAC and Compute Next Secret commands overwrite the temporary secret.
- Copy temporary secret from NVM overwrites the temporary secret (as expected).
- Compute MAC from temporary secret also overwrites the temporary secret. If a temporary secret is used for multiple MAC calculations, the temporary secret needs to be reconstructed after each MAC computation.

Create a Unique Intermediate Secret

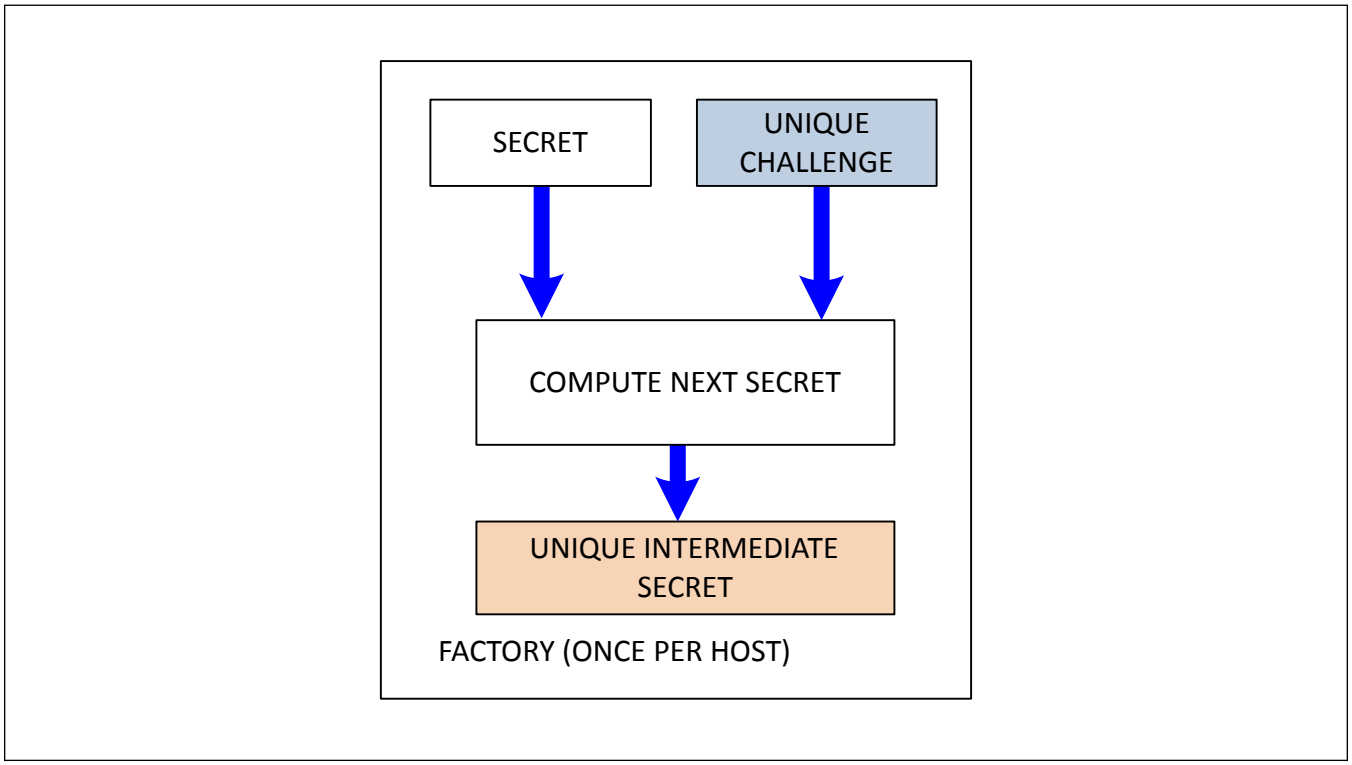


Figure 34. Create a Unique Intermediate Secret

Procedure for 2-Stage Authentication

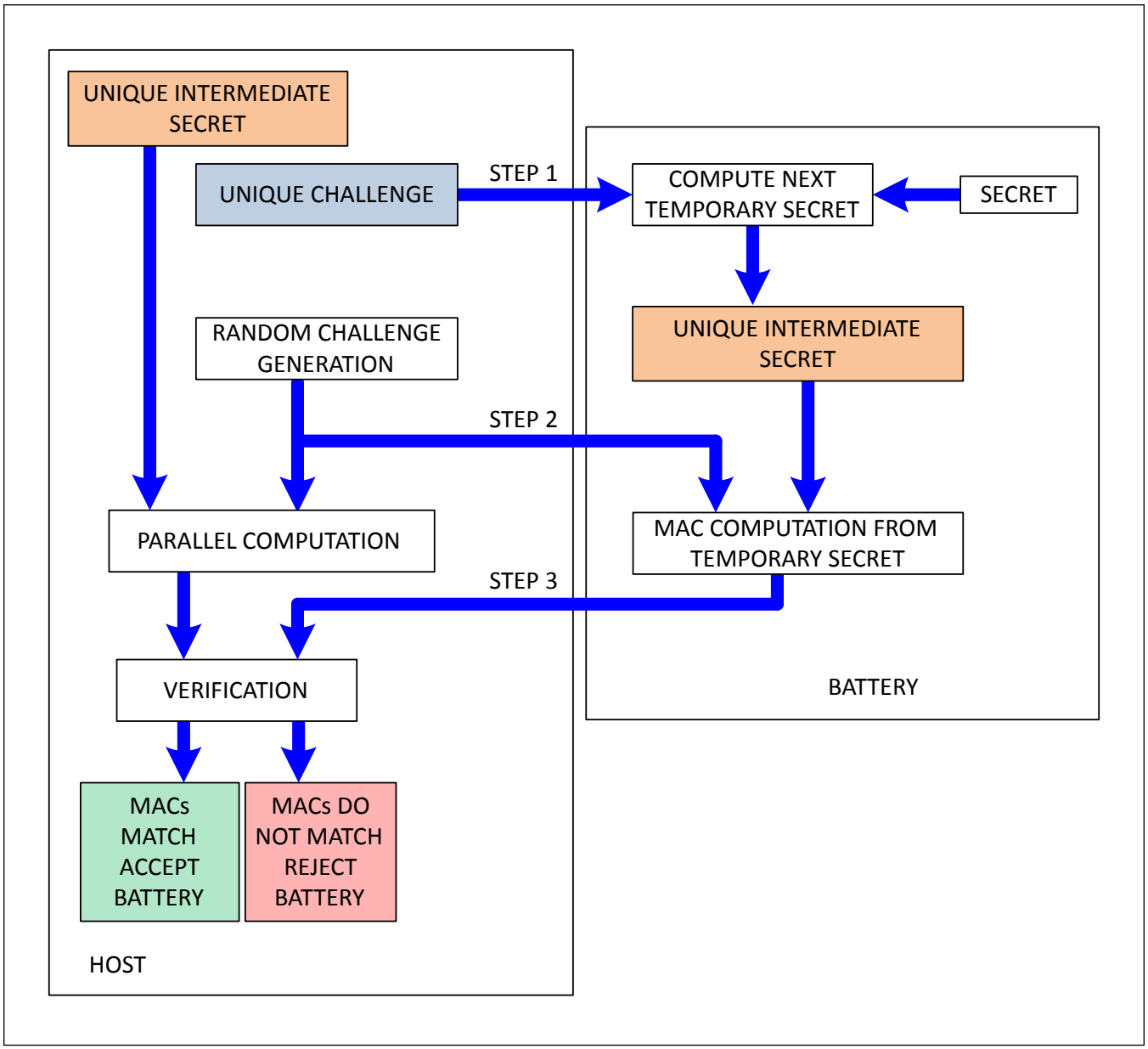


Figure 35. Procedure for 2-Stage Authentication

Determining Number of Remaining Updates

The internal secret can only be updated or cleared n_{SECRET} times total. The number of remaining updates can be calculated using the following procedure:

1. Write 0xE29D to the Command register (060h).
2. Wait t_{RECALL}.
3. Read memory address 1FDh.
4. Decode address 1FDh data as shown in Table 128. Each secret update has redundant indicator flags for reliability.

Logically OR the upper and lower bytes together, then count the number of 1s to determine how many updates have already been used. The first update occurs in a manufacturing test to clear the secret memory before shipping to the user.

Table 128. Number of Remaining Secret Updates

ADDRESS 0E6H DATA	LOGICAL OR OF UPPER AND LOWER BYTES	NUMBER OF UPDATES USED	NUMBER OF UPDATES REMAINING
0000000x00000001b or 000000010000000xb	00000001b	1	5
000000xx0000001xb or 0000001x000000xxb	00000011b	2	4
00000xxx000001xxb or 000001xx00000xxxb	00000111b	3	3
0000xxxx00001xxxb or 00001xxx0000xxxxb	00001111b	4	2
000xxxxx0001xxxxb or 0001xxxx000xxxxxb	00011111b	5	1
00xxxxxx001xxxxxb or 001xxxxx00xxxxxxb	00111111b	6	0

Authentication Commands

All SHA authentication commands are written to memory address 060h to perform the desired operation. Writing the challenge or reading the MAC is handled by accessing the SHA memory space on page 0Ch through direct read and write operations.

COMPUTE MAC WITHOUT ROM ID [3600h]

The challenge value must be written to the SHA memory space before performing a Compute MAC command. This command initiates a SHA-256 computation without including the ROM ID in the message block. Instead, the ROM ID portion of the message block is replaced with a value of all 1s. Since the ROM ID is not used, this command allows the use of a master secret and MAC response independent of the ROM ID. The IC computes the MAC in t_{SHA} after receiving the last bit of this command. After the MAC computation is complete, the host can read the MAC from the SHA memory space.

COMPUTE MAC WITH ROM ID [3500h]

The challenge value must be written to the SHA memory space before performing a Compute MAC command. This command is structured the same as the compute MAC without ROM ID, except that the ROM ID is included in the message block. With the unique ROM ID included in the MAC computation, the MAC is unique to each unit. After the MAC computation is complete, the host can read the MAC from the SHA memory space.

COMPUTE NEXT SECRET WITHOUT ROM ID [3000h]

This command initiates a SHA-256 computation and uses the resulting MAC as the next or new secret. The hash operation is performed with the current 160-bit secret and the new 160-bit challenge. Logical 1s are loaded in place of the ROM ID. The last 160 bits of the MAC are used as the new secret value. The host must allow t_{SHA} after issuing this command for the SHA calculation to complete, then wait t_{UPDATE} for the new secret value to be stored in nonvolatile memory. During this operation, the SHA memory space is not updated. Note that the old secret value must be known before executing this command to calculate what the new secret value is. Also, note that programming the Secret should

be done at the factory before connecting the battery as 5.5V is required at the BATT pin of the IC to update the Secret in NVM.

COMPUTE NEXT SECRET WITH ROM ID [3300h]

This command initiates a SHA-256 computation and uses the resulting MAC as the next or new secret. The hash operation is performed with the current 160-bit secret, the 64-bit ROM ID, and the new 160-bit challenge. The last 160 bits of the output MAC are used as the new secret value. The host must allow t_{SHA} after issuing this command for the SHA calculation to complete, then wait t_{UPDATE} for the new secret value to be stored in nonvolatile memory. During this operation, the SHA memory space is not updated. Note that the old secret value must be known before executing this command to calculate what the new secret value is. Also, note that programming the Secret should be done at the factory before connecting the battery as 5.5V is required at the BATT pin of the IC to update the Secret in NVM.

CLEAR SECRET [5A00h]

This command sets the 160-bit secret to all 0s. The host must wait t_{UPDATE} for the IC to write the new secret value to nonvolatile memory. This command uses up one of the secret write cycles.

LOCK SECRET [6000h]

This command write protects the secret preventing accidental or malicious overwrite of the secret value. The secret value stored in nonvolatile memory becomes permanent. The host must wait t_{UPDATE} for the lock operation to complete.

SHA-256 Lock state is not shown in the Lock register. The lock state can be verified by reading nonvolatile memory history using the following sequence:

1. Send 0xE29B to the Command register (060h).
2. Wait for t_{RECALL}.
3. Read memory address 1FCh.

If address 1FCh is 0x0000, then the secret is not locked. If address 1FCh is anything other than 0x0000, then the secret is permanently locked.

COPY TEMPORARY SECRET FROM NVM [3800]

This command copies the secret from NVM and places it in RAM to allow the secret to be used by the other commands.

COMPUTE NEXT TEMPORARY SECRET WITH ROMID [3900]

This command is similar to COMPUTE NEXT SECRET WITH ROMID except the secret used in the computation comes from the previously executed COPY TEMPORARY SECRET FROM NVM or COMPUTE NEXT TEMPORARY SECRET WITH/WITHOUT ROMID and the next secret is placed in RAM so it can be used in subsequent commands.

COMPUTE NEXT TEMPORARY SECRET WITHOUT ROMID [3A00]

This command is similar to COMPUTE NEXT SECRET WITHOUT ROMID except the secret used in the computation comes from the previously executed COPY TEMPORARY SECRET FROM NVM or COMPUTE NEXT TEMPORARY SECRET WITH/WITHOUT ROMID and the next secret is placed in RAM so it can be used in subsequent commands.

COMPUTE MAC FROM TEMPORARY SECRET WITHOUT ROMID [3C00]

This command is the same as COMPUTE MAC WITHOUT ROMID except the secret used in the computation comes from the previously executed COPY TEMPORARY SECRET FROM NVM or COMPUTE NEXT TEMPORARY SECRET WITH/WITHOUT ROMID.

COMPUTE MAC FROM TEMPORARY SECRET WITH ROMID [3D00]

This command is the same as COMPUTE MAC WITH ROMID except the secret used in the computation comes from the previously executed COPY TEMPORARY SECRET FROM NVM or COMPUTE NEXT TEMPORARY SECRET WITH/WITHOUT ROMID.

Device Reset

There are two different levels of reset for the IC; a full reset restores the IC to its power-up state (the same as if power had

been cycled) and a fuel-gauge reset resets only the fuel gauge operation without resetting IC hardware. This is useful for testing different configurations without writing to nonvolatile memory. Use the following sequences to reset the IC.

FULL RESET

1. Reset IC hardware by writing 000Fh to the Command register at 060h.
2. Wait 10ms.
3. Reset IC fuel gauge operation by writing 8000h to the Config2 register at 0ABh. This command does not disturb the state of the protection FETs.
4. Wait for the POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate that the POR sequence is complete.

FUEL-GAUGE RESET

1. Reset IC fuel gauge operation by writing 8000h to the Config2 register at 0ABh. This command does not disturb the state of the protection FETs.
2. Wait for the POR_CMD bit (bit 15) of the Config2 register to be cleared to indicate that the POR sequence is complete.

Reset Commands

There are two commands that can be used to reset either the entire IC or just the operation of the fuel gauge, protection, and charging configuration without interrupting the hardware (CHG, DIS FETs, or Non-Volatile Shadow Memory). Note that the configuration reset command is written to Config2 instead of the Command register.

HARDWARE RESET [000Fh to address 060h]

Send the hardware reset command to the Command register to recall all nonvolatile memory into shadow RAM and reset all hardware-based operations of the IC. This command should always be followed by the reset fuel gauge command to fully reset operation of the IC.

CONFIGURATION RESET [8000h to address 0ABh]

The Configuration Reset command resets operation of the IC without restoring nonvolatile memory values into shadow RAM or resetting the FET Control. This command allows different configurations to be tested without using one of the limited numbers of nonvolatile memory writes. This command does not disturb the state of the protection FETs.

Summary of Commands

Any operation other than reading or writing a memory location is executed by writing the appropriate command to the Command or Config2 registers. Table 129 lists all function commands understood by the MAX17332. The function command must be written to the Command (060h) or Config2 (0ABh) registers. Device commands are described in detail in the *Authentication*, *Nonvolatile Memory*, *Reset*, and *Power Up* sections of the data sheet.

Table 129. All Function Commands

COMMAND	TYPE	REGISTER	HEX	DESCRIPTION
Compute MAC *Without* ROM ID	SHA	060h	3600h	Computes hash operation of the message block with logical 1s in place of the ROM ID.
Compute MAC *With* ROM ID	SHA	060h	3500h	Computes hash operation of the message block including the ROM ID.
Compute Next Secret *Without* ROM ID	SHA	060h	3000h	Computes hash operation of the message block with logical 1s in place of the ROM ID. The result is then stored as the new secret.
Compute Next Secret *With* ROM ID	SHA	060h	3300h	Computes hash operation of the message block including the ROM ID. The result is then stored as the new secret.
Clear Secret	SHA	060h	5A00h	Resets the SHA-256 secret to a value of all 0s.
Lock Secret	SHA	060h	6000h	Permanently locks the SHA-256 secret.
Copy NV Block	Memory	060h	E904h	Copies all shadow RAM locations to nonvolatile memory at the same time.
NV Recall	Memory	060h	E001h	Recalls all nonvolatile memory to RAM.

Table 129. All Function Commands (continued)

COMMAND	TYPE	REGISTER	HEX	DESCRIPTION
History Recall	Memory	060h	E2XXh	Recalls a page of nonvolatile memory history into RAM page 1Eh.
NV Lock	Memory	060h	6AXXh	Permanently locks an area of memory. See the *Memory Locks* section for details.
Hardware Reset	Reset	060h	000Fh	Recalls nonvolatile memory into RAM and resets the IC hardware. Fuel gauge operation is not reset.
Fuel Gauge Reset	Reset	0ABh	8000h	Restarts the fuel gauge operation without affecting nonvolatile shadow RAM settings.

Communication

2-Wire Bus System

The uses a 2-Wire bus system to communicate by both standard I²C protocol or by SBS smart battery protocol. The slave address used by the host to access the IC determines which protocol is used and what memory locations are available to read or write. The following description applies to both protocols. See the *I²C* and SBS Bus System descriptions for specific protocol details.

Hardware Configuration

The 2-Wire bus system supports operation as a slave-only device in a single or multi-slave, and single or multi-master system. Up to 128 slave devices can share the bus using 7-bit slave addresses. The 2-Wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the IC and a master device at speeds up to 400kHz. The IC's SDA pin operates bidirectionally. When the IC receives data, the SDA operates as an input. When the IC returns data, the SDA operates as an open-drain output with the host system providing a resistive pullup. See Figure 36. The IC always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits which begin and end each transaction.

2-Wire Bus Interface Circuitry

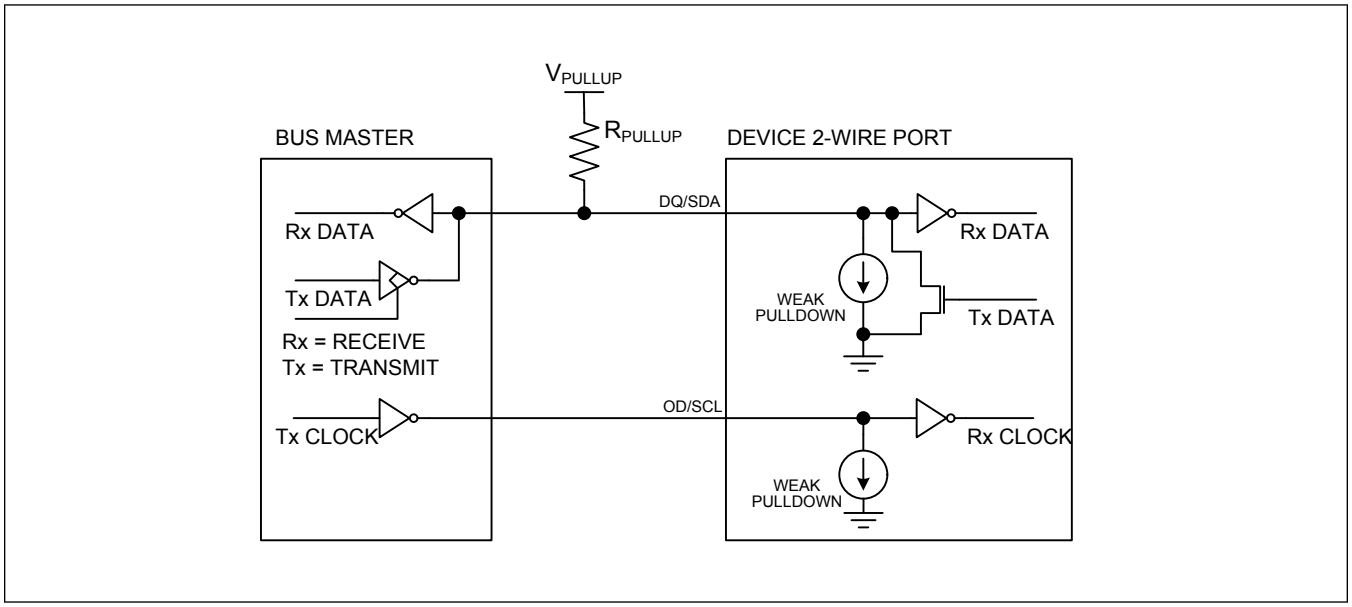


Figure 36. 2-Wire Bus Interface Circuitry

I/O Signaling

The following individual signals are used to build byte level 2-Wire communication sequences.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low to high and then high to low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle (i.e., not busy) when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition by a low-to-high transition on SDA while SCL is high. A Repeated START condition can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multi-master systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an Acknowledge bit (ACK) or a No Acknowledge bit (NACK). Both the master and the IC slave generate acknowledge bits. To generate an Acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a No Acknowledge, the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication. If a transaction is aborted mid-byte, the master should send additional clock pulses to force the slave IC to free the bus before restarting communication.

Data Order

With 2-Wire communication, a byte of data consists of 8 bits ordered most significant bit (MSb) first. The least significant bit (LSb) of each byte is followed by the Acknowledge bit. IC registers composed of multibyte values are ordered least significant byte (LSB) first.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address and the read/write (R/W) bit. When the bus is idle, the IC continuously monitors for a START condition followed by its slave address. When the IC receives a slave address that matches its Slave Address, it responds with an Acknowledge bit during the clock period following the R/W bit. The supports the slave addresses shown in Table 130. **Note:** The addresses shown in Table 130 are 8-bit slave addresses.

Table 130. 2-Wire Slave Addresses

SLAVE ADDRESS	PROTOCOL	ADDRESS BYTE RANGE	INTERNAL MEMORY RANGE ACCESSED
6Ch	I^2C	00h to FFh	000h to 0FFh
16h	SMBUS™	00h to 7Fh	100h to 17Fh
	I^2C	80h to FFh	180h to 1FFh

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the slave by the master.

Bus Timing

The IC is compatible with any bus timing up to 400kHz. See the *Electrical Characteristics* table for timing details. No special configuration is required to operate at any speed. Figure 37 shows an example of standard 2-Wire bus timing.

2-Wire Bus Timing Diagram

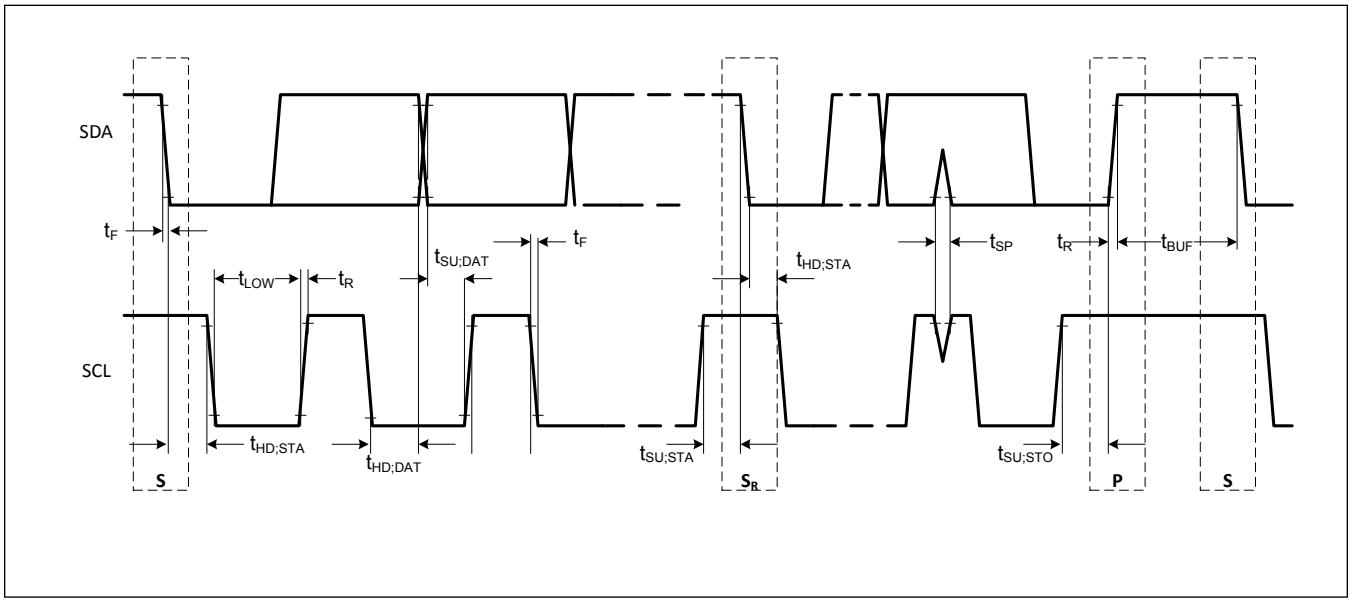


Figure 37. 2-Wire Bus Timing Diagram

I²C Protocols

The following 2-Wire communication protocols must be used by the bus master to access memory locations 000h to 1FFh. Addresses 000h to 0FFh and from 180h to 1FFh can be read continuously. Addresses 100h to 17Fh must be read one word at a time. These protocols follow the standard I²C specification for communication.

I²C Write Data Protocol

The Write Data protocol is used to transmit data to the IC at memory addresses from 000h to 1FFh. Addresses 000h to 0FFh and 180h to 1FFh can be written as a block. Addesses 100h to 17Fh must be written one word at a time. The memory address is sent by the bus master as a single byte value immediately after the slave address, followed by an ACK from the IC. The LSB of the data to be stored is written immediately after the memory address byte, followed by an ACK from the IC. The MSB of the data to be stored is written next, followed by an ACK from the IC. Because the address is automatically incremented after the least significant bit (LSb) of the MSB of each word received by the IC, the LSB of the data at the next memory address can be written immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. If the bus master continues an auto-incremented write transaction beyond address 0FFh or 1FFh, the IC ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. See Figure 38 for an example Write Data communication sequence.

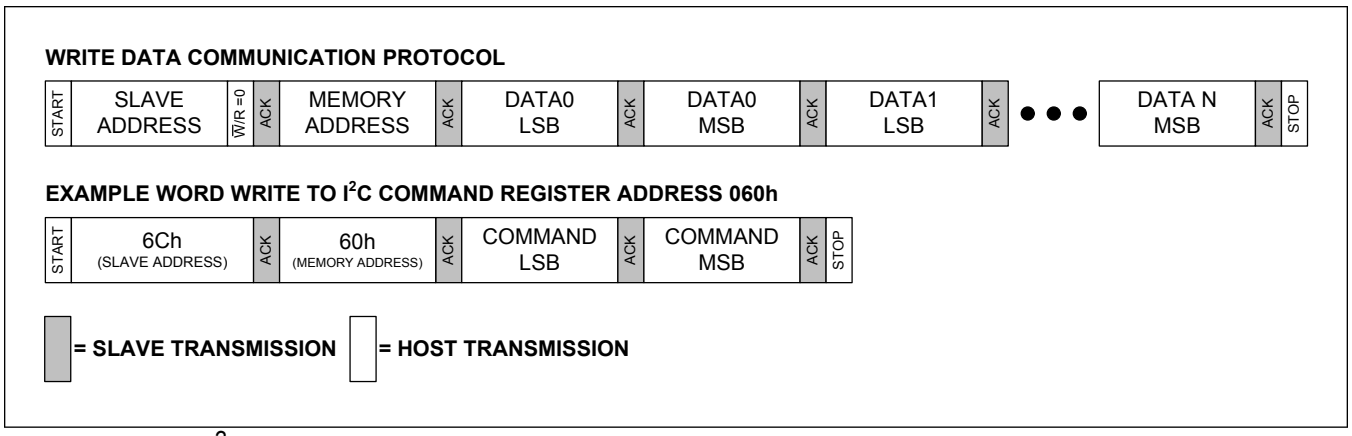


Figure 38. Example I²C Write Data Communication Sequence

I²C Read Data Protocol

The Read Data protocol is used to transmit data from IC memory locations 000h to 1FFh. Addresses 000h to 0FFh and 180h to 1FFh can be read as a block. Addresses 100h to 17Fh must be read as individual words. The memory address is sent by the bus master as a single-byte value immediately after the slave address. Immediately following the memory address, the bus master issues a REPEATED START followed by the slave address. The MAX17332 ACKs the address and begins transmitting data. A word of data is read as two separate bytes that the master must ACK. The LSB is read first, followed by an ACK from the master. The MSB is read next, followed by an ACK from the master. Because the address is automatically incremented after the least significant bit (LSb) of the MSB of each word transmitted by the IC, the LSB of the data at the next memory address can be read immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a read transaction by sending a NACK followed by a STOP. If the bus master continues an auto-incremented read transaction beyond memory address 0FFh or 1FFh, the IC transmits all 1s until a NACK or STOP is received. Data from reserved address locations is undefined. See Figure 39 for an example Read Data communication sequence.

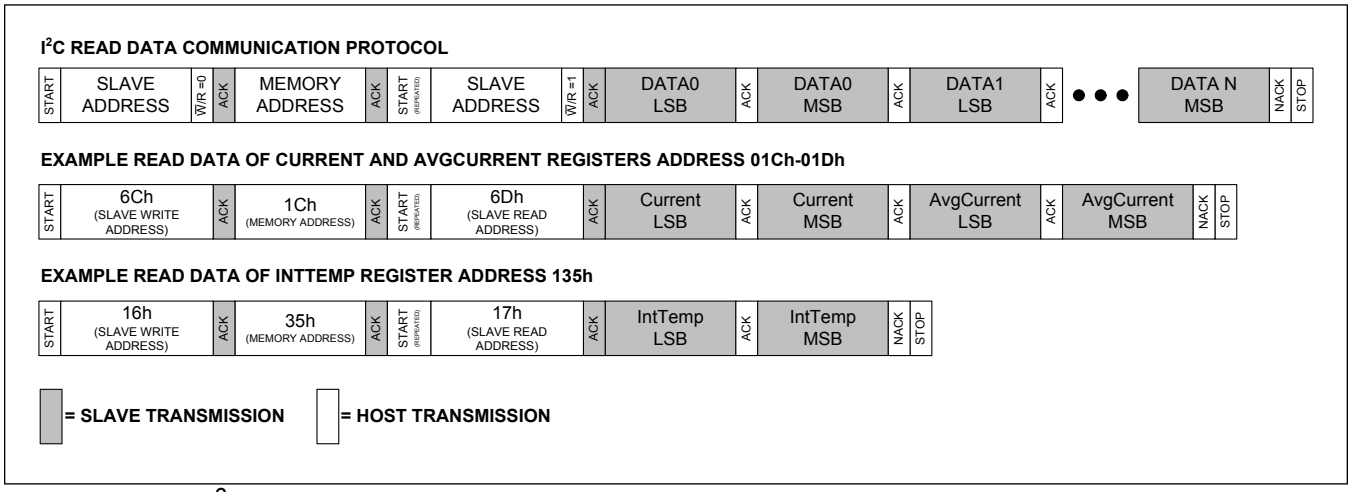


Figure 39. Example I²C Read Data Communication Sequence

1-Wire Bus System

The 1-Wire version of the MAX17332 communicates to a host through a Maxim 1-Wire interface. The 1-Wire bus is a system that has a single bus master and one or more slaves. A multi-drop bus is a 1-Wire bus with multiple slaves, while a single-drop bus has only one slave device. In all instances, this IC is a slave device. The bus master is typically a microprocessor in the host system. The discussion of this bus system consists of five topics: 64-bit net address, CRC

generation, hardware configuration, transaction sequence, and 1-Wire signaling.

Hardware Configuration

Because the 1-Wire bus has only a single line, each device on the bus must be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus with open-drain or tri-state output drivers. The MAX17332 uses an open-drain output driver as part of the bidirectional interface circuitry shown in Figure 40. If a bidirectional pin is not available on the bus master, separate output and input pins can be connected together. Communication speed is controlled by the OD/SCL pin. Connect OD/SCL to PACK- to enable communication at standard speed. Connect OD/SCL to the REG3 pin to enable communication at overdrive speed.

The 1-Wire bus must have a pullup resistor on the host side of the bus. A value between 2kΩ and 5kΩ is recommended for most applications. The idle state for the 1-Wire bus is logic high. If, for any reason, a bus transaction must be suspended, the bus must be left in the idle state to properly resume the transaction later. Note that if the bus is left low for more than t_{LOW0}, slave devices on the bus begin to interpret the low period as a reset pulse, effectively terminating the transaction.

1-Wire Bus Interface Circuitry

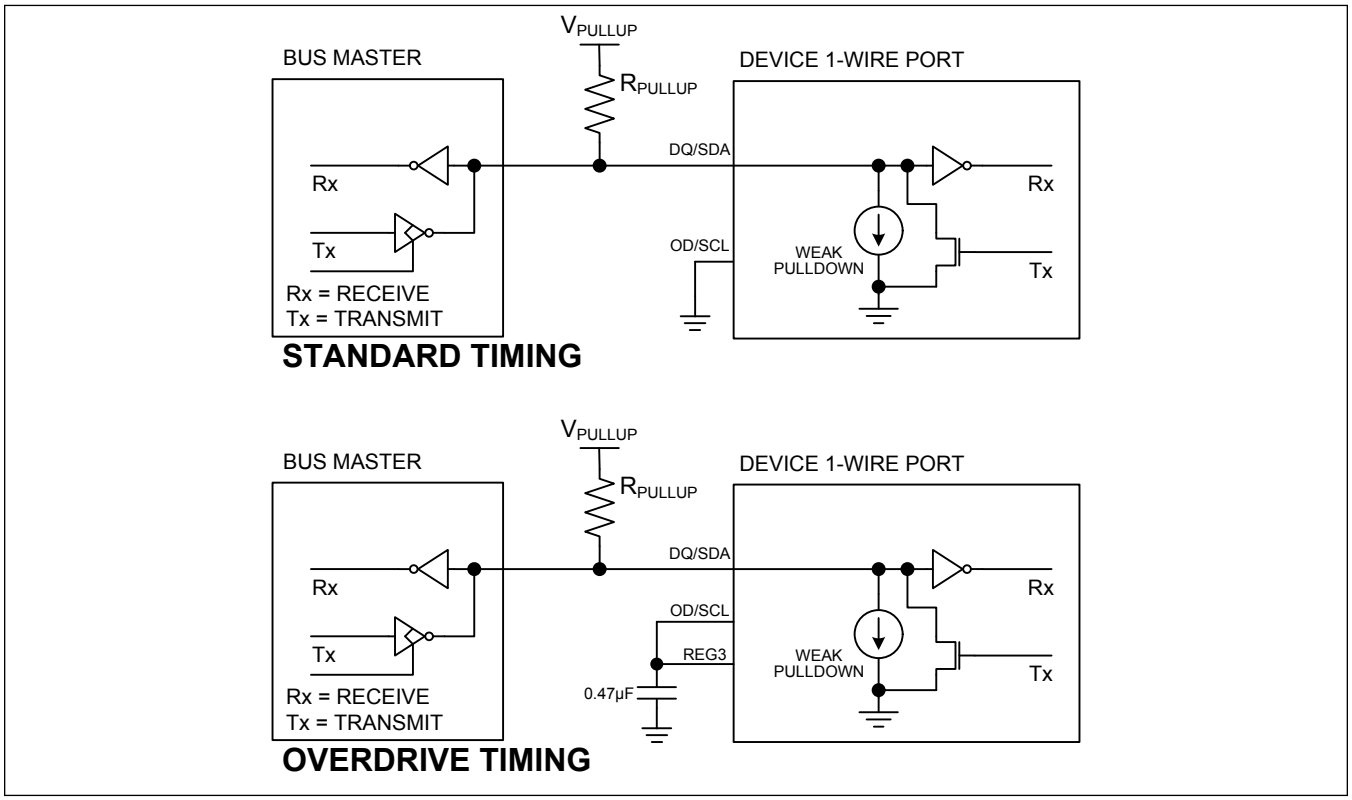


Figure 40. 1-Wire Bus Interface Circuitry

64-Bit Net Address (ROM ID)

The 1-Wire net address is 64 bits in length. The term net address is synonymous with the ROM ID or ROM code terms used in other 1-Wire documentation. The value of the net address is stored in nonvolatile memory and cannot be changed. In a 1-Wire standard net address, the first eight bits of the net address are the 1-Wire family code. This value is the same for all ICs of the same type. The next 48 bits are a unique serial number. The last eight bits are a cyclic redundancy check (CRC) of the first 56 bits. Table 131 details the Net Address data format. The 64-bit net address and the 1-Wire I/O circuitry built into the device enable the IC to communicate through the 1-Wire protocol detailed in this data sheet if enabled.

Table 131. 1-Wire Net Address Format

MSb: 8-Bit CRC	48-Bit Serial Number	LSb: 8-Bit Family Code (26h)

I/O Signaling

The 1-Wire bus requires strict signaling protocols to ensure data integrity. The four protocols used by the MAX17332 are as follows: the initialization sequence (reset pulse followed by presence pulse), write 0, write 1, and read data. The bus master initiates all signaling except for the presence pulse.

Reset Time Slot

The initialization sequence required to begin any communication with the MAX17332 is shown in Figure 41. The bus master transmits (Tx) a reset pulse for t_{RSTL}. The bus master then releases the line and goes into Receive mode (Rx). The 1-Wire bus line is then pulled high by the pullup resistor. After detecting the rising edge on the DQ pin, the MAX17332 waits for t_{PDH} and then transmits the presence pulse for t_{PDL}. A presence pulse following a reset pulse indicates that the MAX17332 is ready to accept a net address command.

1-Wire Initialization Sequence

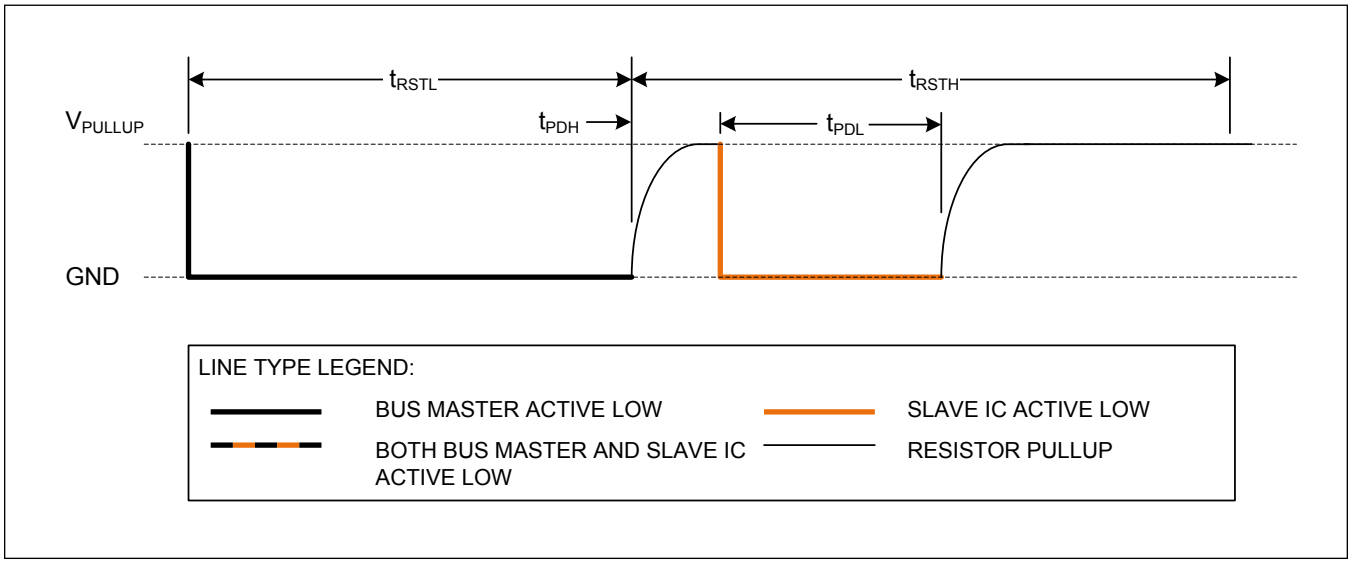


Figure 41. 1-Wire Initialization Sequence

Write Time Slots

A write-time slot is initiated when the bus master pulls the 1-Wire bus from a logic-high (inactive) level to a logic-low level. There are two types of write-time slots: write 1 and write 0. All write-time slots must be t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. The MAX17332 samples the 1-Wire bus line between t_{LOW1_MAX} and t_{LOW0_MIN} after the line falls. If the line is high when sampled, a write 1 occurs. If the line is low when sampled, a write 0 occurs. The sample window is illustrated in Figure 42. For the bus master to generate a write-1 time slot, the bus line must be pulled low and then released, allowing the line to be pulled high less than t_{RDV} after the start of the write time slot. For the host to generate a write 0 time slot, the bus line must be pulled low and held low for the duration of the write-time slot.

Read Time Slots

A read-time slot is initiated when the bus master pulls the 1-Wire bus line from a logic-high level to a logic-low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the MAX17332 to present valid data. The bus master can then sample the data t_{RDV} from the start of the read-time slot. By the end of the read-time slot, the MAX17332 releases the bus line and allows it to be pulled high by the external pullup resistor. All read-time slots must be

t_{SLOT} in duration with a 1µs minimum recovery time, t_{REC}, between cycles. See Figure 42 and the timing specifications in the *Electrical Characteristics* table for more information.

1-Wire Write and Read Time Slots

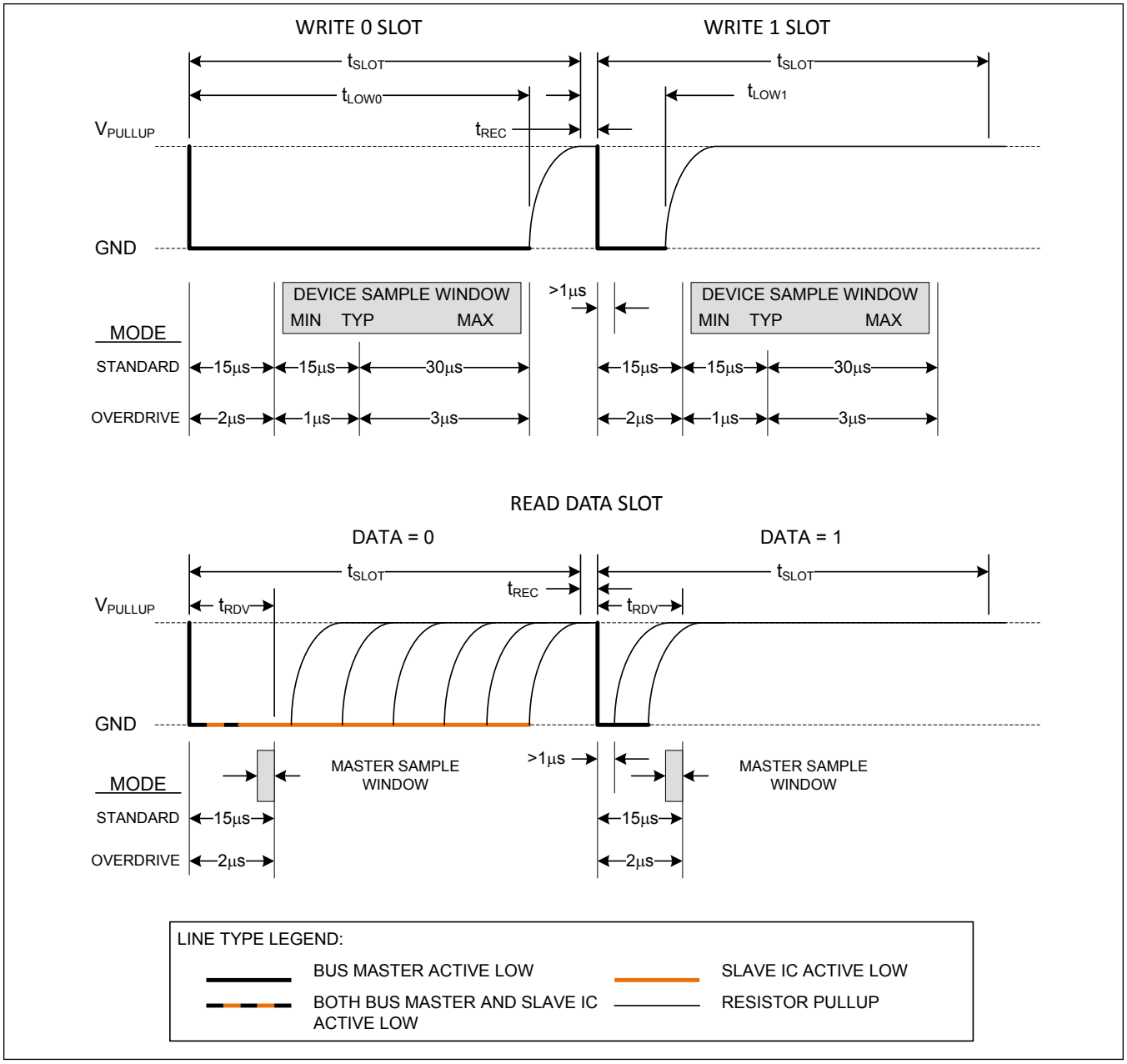


Figure 42. 1-Wire Write and Read Time Slots

Transaction Sequence

The protocol for accessing the MAX17332 through the 1-Wire port is as follows:

- Initialization

- Net Address Command
- Function Command(s)
- Data Transfer (not all commands have data transfer)

Net Address Commands

Once the bus master has detected the presence of one or more slaves, it can issue one of the net address commands described in the following paragraphs. The name of each net address command (ROM command) is followed by the 8-bit op code for that command in square brackets.

Read Net Address [33h]

This command allows the bus master to read the MAX17332's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open-drain produces a wired-AND result).

Match Net Address [55h]

This command allows the bus master to specifically address one MAX17332 on the 1-Wire bus. Only the addressed MAX17332 responds to any subsequent function command. All other slave devices ignore the function command and wait for a reset pulse. This command can be used with one or more slave devices on the bus.

Skip Net Address [CCh]

This command saves time when there is only one MAX17332 on the bus by allowing the bus master to issue a function command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent function command can cause a data collision when all slaves transmit data at the same time.

Search Net Address [F0h]

This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. The remaining devices can then be identified on additional iterations of the process. Refer to Chapter 5 of the *Book of iButton® Standards* for a comprehensive discussion of a net address search, including an actual example (www.maximintegrated.com/iButtonBook).

iButton is a registered trademark of Maxim Integrated Products, Inc.

1-Wire Functions

After successfully completing one of the net address commands, the bus master can access the features of the MAX17332 with either a Read Data or Write Data function command described in the following paragraphs. Any other IC operation such as a Compute MAC operation is accomplished by writing to the COMMAND register. See the Nonvolatile Memory Commands section for details.

Read Data [69h, LL, HH]

This command reads data from the MAX17332 starting at memory address HHLL. Any memory address from 0000h to 01FFh is a valid starting address. The LSb of the data in address HHLL is available to be read immediately after the MSb of the address has been entered. Because the address is automatically incremented after the MSb of each byte is received, the LSb of the data at address HHLL+ 1 is available to be read immediately after the MSb of the data at address HHLL. If the bus master continues to read beyond address 01FFh, data is undefined. Addresses labeled "Reserved" in the memory map contain undefined data values. The Read Data command can be terminated by the bus master with a reset pulse at any bit boundary. Reads from nonvolatile memory addresses return the data in the shadow RAM. A Recall Data command is required to transfer data from nonvolatile memory to the shadow RAM. See the Nonvolatile Memory Commands section for more details. See Figure 43 for an example Read Data communication sequence.

Write Data [6Ch, LL, HH]

This command writes data to the MAX17332 starting at memory address HHLL. Any memory address from 0000h to

01FFh is a valid starting address. The LSb of the data to be stored at address HHLL can be written immediately after the MSb of address has been entered. Because the address is automatically incremented after the MSb of each byte is written, the LSb to be stored at address HHLL + 1 can be written immediately after the MSb to be stored at address HHLL. If the bus master continues to write beyond address 01FFh, the data is ignored by the IC. Writes to read-only addresses and locked memory blocks are ignored. Do not write to RESERVED address locations. Incomplete bytes are not written. Writes to unlocked nonvolatile memory addresses modify the shadow RAM. A Copy NV Block command is required to transfer data from the shadow RAM to nonvolatile memory. See the Nonvolatile Memory Commands section for more details. See Figure 43 for an example Write Data communication sequence.

Example 1-Wire Communication Sequences

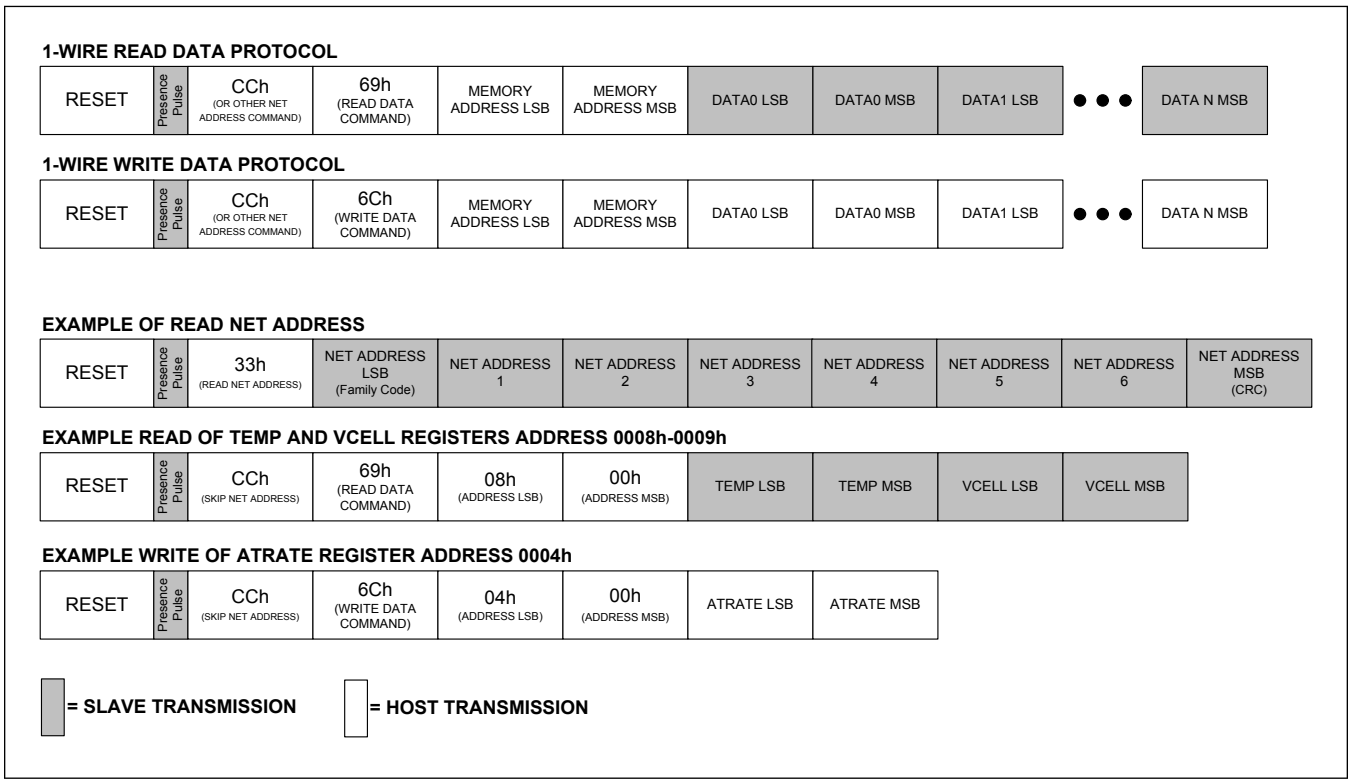


Figure 43. Example 1-Wire Communication Sequences

Appendix A: Reading History Data Pseudo-Code Example

The following pseudo-code can be used as a reference for reading history data from the IC. The code first reads and tests all flag information, then reads all valid history data into a two-dimensional array. Afterwards, the HistoryLength variable indicates the depth of the history array data.

```
Int WriteFlags[26];
Int ValidFlags[26];
Boolean PageGood[100];
Int HistoryData[100][16];
Int HistoryLength;
Int word, position, flag1, flag2, flag3, flag4;
//Read all flag information from the IC
WriteCommand(0xE29C);
Wait(tRECALL);
WriteFlags[0] = ReadData(0x1F2);
WriteFlags[1] = ReadData(0x1F3);
WriteFlags[2] = ReadData(0x1F4);
WriteFlags[3] = ReadData(0x1F5);
WriteFlags[4] = ReadData(0x1F6);
WriteFlags[5] = ReadData(0x1F7);
WriteFlags[6] = ReadData(0x1F8);
WriteFlags[7] = ReadData(0x1F9);
WriteFlags[8] = ReadData(0x1FA);
WriteFlags[9] = ReadData(0x1FB);
WriteFlags[10] = ReadData(0x1FC);
WriteFlags[11] = ReadData(0x1FD);
WriteFlags[12] = ReadData(0x1FE);
ValidFlags[0] = ReadData(0x1FF);
WriteCommand(0xE29D);
Wait(tRECALL);
ValidFlags[1] = ReadData(0x1F0);
ValidFlags[2] = ReadData(0x1F1);
ValidFlags[3] = ReadData(0x1F2);
ValidFlags[4] = ReadData(0x1F3);
ValidFlags[5] = ReadData(0x1F4);
ValidFlags[6] = ReadData(0x1F5);
ValidFlags[7] = ReadData(0x1F6);
ValidFlags[8] = ReadData(0x1F7);
ValidFlags[9] = ReadData(0x1F8);
ValidFlags[10] = ReadData(0x1F9);
ValidFlags[11] = ReadData(0x1FA);
```

```
ValidFlags[12] = ReadData(0x1FB);
//Determine which history pages contain valid data
For loop = 0 to 99
{
    word = (int)( loop / 8 );
    position = loop % 8 ;  //remainder
    flag1 = (WriteFlags[word] >> position) & 0x0001;
    flag2 = (WriteFlags[word] >> (position+8)) & 0x0001;
    flag3 = (ValidFlags[word] >> position) & 0x0001;
    flag4 = (ValidFlags[word] >> (position+8)) & 0x0001;
    if (flag1 || flag2) && (flag3 || flag4)
        PageGood[loop] = True;
    else
        PageGood[loop] = False;
}
//Read all the history data from the IC
HistoryLength = 0;
For loop = 0 to 99
{
    if(PageGood[loop]) == TRUE
    {
        SendCommand(0xE22E + loop);
        Wait(tRECALL);
        HistoryData[HistoryLength][0] = ReadData(0x1F0);
        ...
        HistoryData[HistoryLength][15] = ReadData(0x1FF);
        HistoryLength++;
    }
}
```

Appendix B: Parallel Cell Management Example

The following pseudo-code can be used as a reference for managing parallel batteries.

```
HOST PSEUDOCODE (on 500ms timer):
def on_500ms_timer():
   if(all(AllBatts.FProtStat.IsDis==0)):
      VMax = max(AllBatts.VCell)
      VMin = min(AllBatts.VCell)
      stepDown=stepUp=CrossCharge=False
      if(VMin<VSys_Min):  CrossCharge=True                    #1
      for Batt in AllBatts:
         Batt.Status=0xFFDF (AllowChgB=0)                    #2
         if(Batt.VCell>VMin+400mV and !CrossCharge):          #3
            Batt.Config2.BlockDis=1
```

```
    else:
       Batt.Config2.BlockDis=0                    #4

    if (Status.CA):
          if  (Batt.ChgStat.[CP,CT]): stepDown=True      #5
          elif(Batt.ChgStat.Dropout): stepUp  =True      #6
       Status=0xF7FF                              #7

 if(stepDown):   step DC-DC down                  #8
 elif(stepUp):   step DC-DC up
```

Notes:

1) Evaluate the minimum voltage battery for the ability to support system discharge. When the cell is too low, unplugging the charge source would result in a crash except if cross-charging is allowed
2) Indicate charger presense to all batteries (even blocked batteries)
3) Determine which batteries to block-discharge, to avoid cross-charging
4) Allow discharging if the low battery is much lower than the full battery or the low battery is below VSys_Min
5) Consider FET heat: (DC-DC voltage down)
6) Consider dropout: (DC-DC voltage up)
7) Clear Charge Alert bit
8) Optional: apply DC-DC update

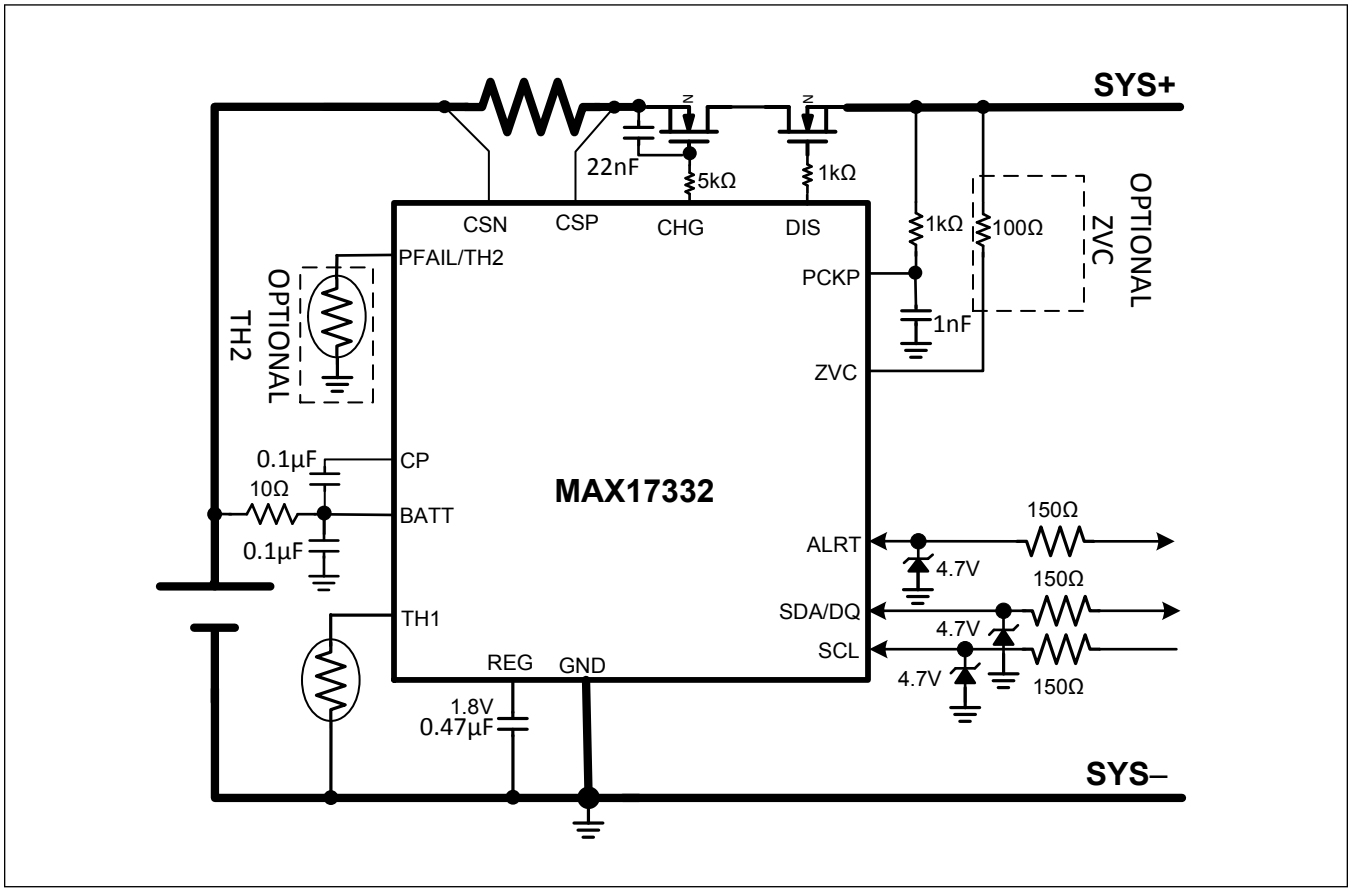
Applications:

1) Low-Power Parallel Charging (<500mA total). A 5V source such as USB connects directly to the system and both MAX17332 ICs. USB detection (such as BC1.2) is not needed since all USB adaptors provide 500mA. With each battery charge current set below 250mA, the CHG FET heat is lower than 350mW for 99% of the charge curve since the majority of the charge curve VBATT exceeds 3.6V. The heat in the CHG FET is calculated by the following equation: 250mA x (5.0V - 3.6V) = 350mW.

2) High-Power Parallel Charging (>500mA total). The application must have a programmable DC-DC converter supplying power to the MAX17332 ICs.

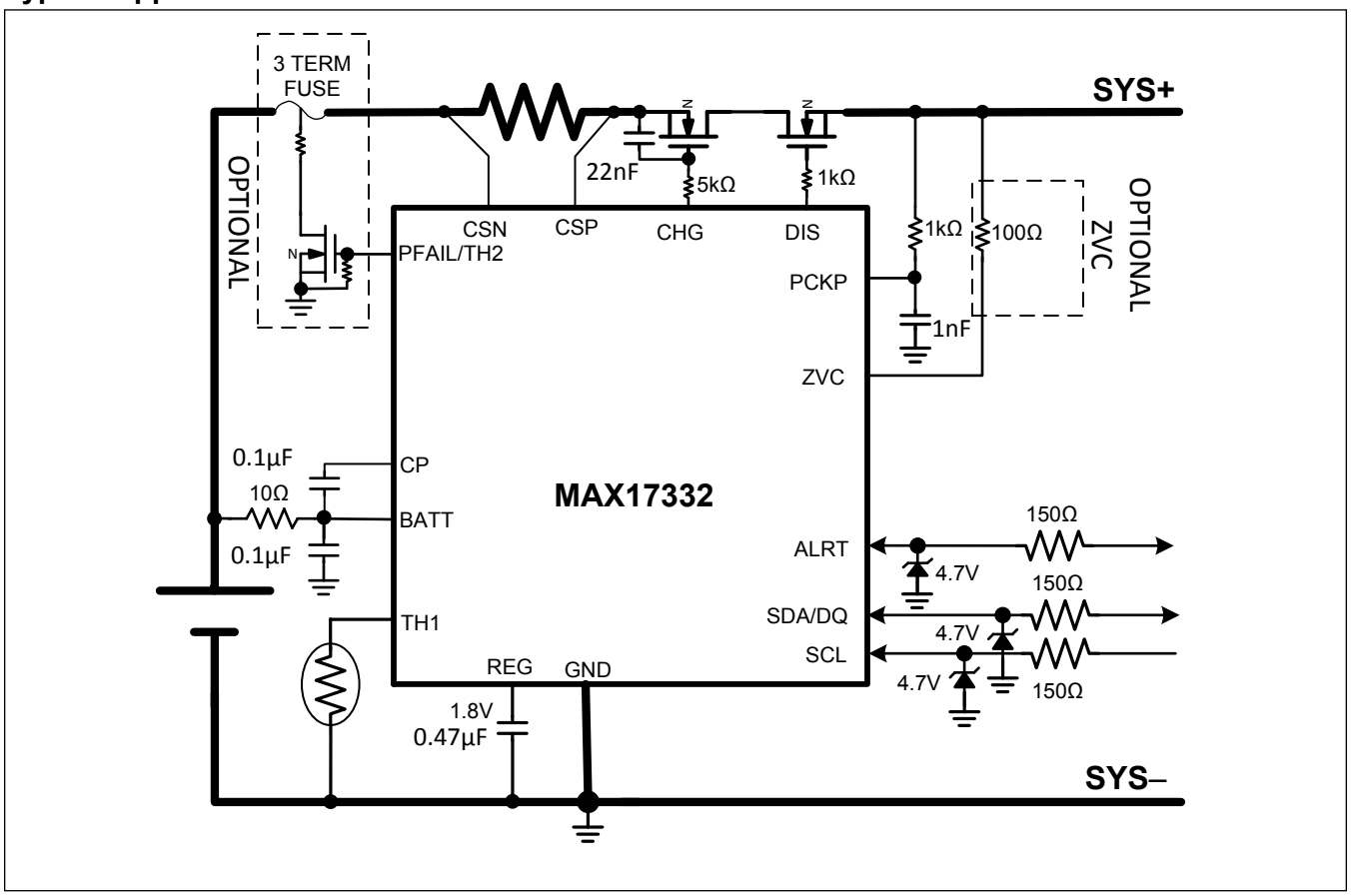
Typical Application Circuits

Typical Application Schematic



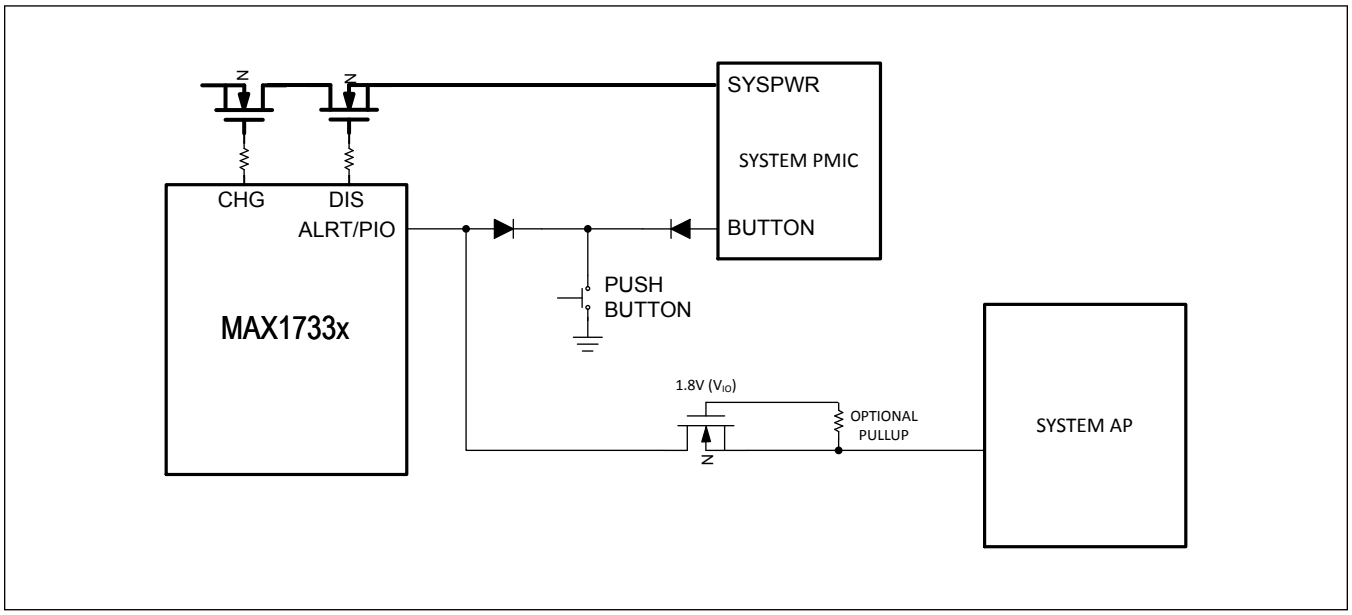
Typical Application Circuits (continued)

Typical Application Schematic with Fuse



Typical Application Circuits (continued)

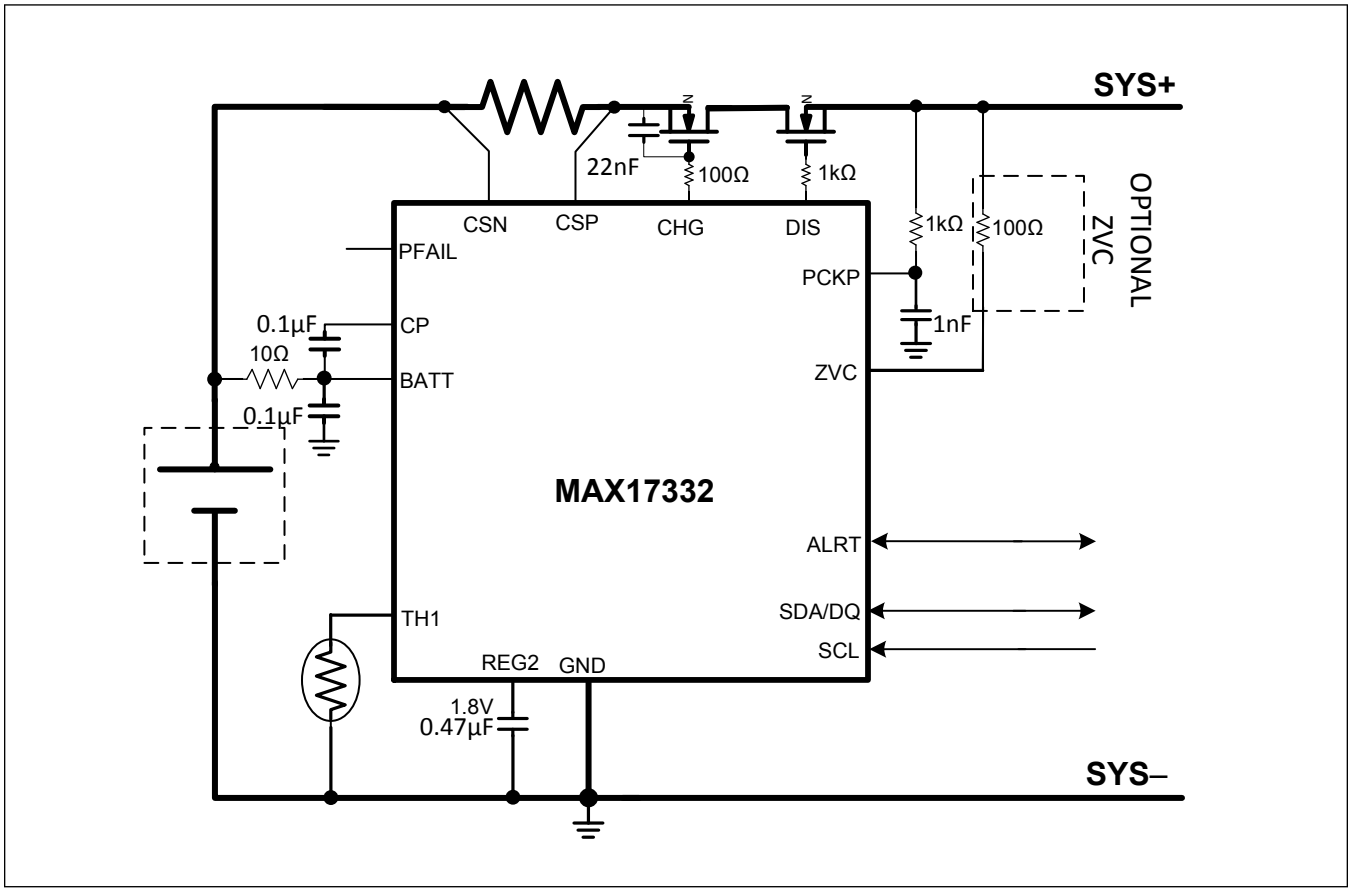
Pushbutton Schematic



A pushbutton can be shared by the MAX17332 and the system to wake up both the system and the MAX17332. The diode on the system interface PMIC blocks the pulldown when there is no supply, which prevents the wakeup for the MAX17332 when the system interface PMIC loses power in ship mode. The diode on the ALRT/PIO pin prevents the alert pulldown from triggering a button action on the PMIC, which prevents accidental shutdown in the event of an alert being uncleared for greater than ten seconds. The FET between MAX17332 and System AP blocks the System AP pulldown from triggering the wakeup when the AP doesn't have power. The FET acts as a level shifter and passes the pulldown alert signal in both directions when 1.8V of voltage is present.

Typical Application Circuits (continued)

Typical Application Schematic for System Side Implementation



Ordering Information

PART	INTERFACE	PIN-PACKAGE
MAX17332X22+	I²C	15 WLP
MAX17332X22+T	I²C	15 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Initial release	—
1	1/23	Release for Market Intro	—

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