Click here to ask an associate for production status of specific part numbers.

10A, 1.5MHz, 2.7V to 16V Integrated Step-Down Switching Regulator

MAX16710

General Description

The MAX16710 is a fully integrated, highly efficient, step-down DC-DC switching regulator. The regulator is able to operate from 2.7V to 16V input supplies, and the output can be adjusted from 0.5V to 5.8V, delivering up to 10A of load current.

The switching frequency of the device can be configured from 500kHz to 1.5MHz and can optimize the design in terms of size and performance.

The MAX16710 utilizes fixed-frequency, current-mode control with internal compensation. The IC features an advanced modulation scheme (AMS) and selectable discontinuous current mode (DCM) operation to provide improved performance. Operation settings and configurable features can be selected by three programming pins PGM0, PGM1, and PGM2.

The IC has an internal 1.8V linear regulator (LDO) output to power the gate drives (V_{CC}) and internal circuitry (AVDD).

The IC has multiple protections including positive and negative overcurrent protection, output overvoltage protection, and overtemperature protection to ensure a robust design.

The device is available in a compact 2.52mm x 2.93mm wafer-level package (WLP). It supports -40°C to +125°C junction temperature operation.

Applications

- Data Center Power
- Communications Equipment
- Networking Equipment
- Servers and Storage
- Point-of-Load Voltage Regulators

***Ordering Information* appears at end of data sheet.**

Benefits and Features

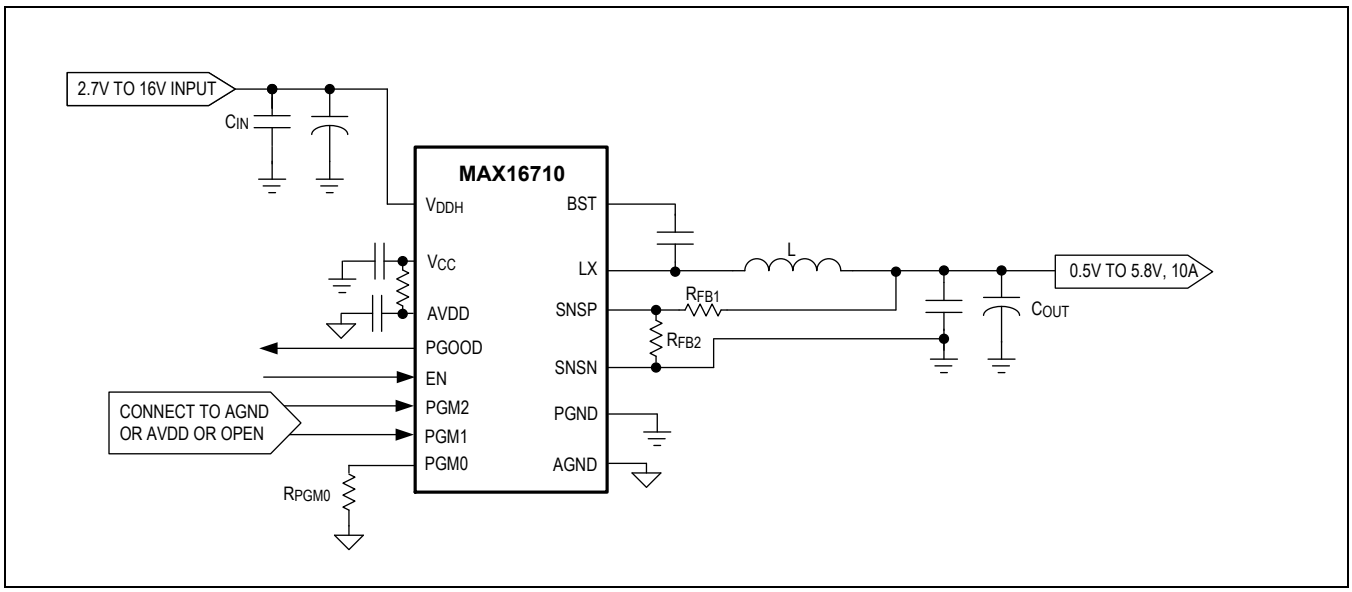
- High Power Density with Low Component Count
  - Compact 2.52mm x 2.93mm, 25-Bump WLP
  - Internal Compensation
  - Single-Supply Operation with Integrated LDO for Bias Generation
- Wide Operating Range
  - 2.7V to 16V Input Voltage Range
  - 0.5V to 5.8V Output Voltage Range
  - 500kHz to 1.5MHz Configurable Switching Frequency
  - -40°C to +125°C Junction Temperature Range
  - Three Programming Pins to Select Different Configurations
- Optimized Performance and Efficiency
  - 93.1% Peak Efficiency with V_{DDH} = 12V, V_{OUT} = 1.8V, and f_{SW} = 500kHz
  - AMS to Improve Load Transient
  - Selectable DCM to Improve Light Load Efficiency
  - Differential Remote Sense

DESCRIPTION	CURRENT RATING* (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating	10	2.7 to 16	0.5 to 5.8
Thermal Rating T_A = 55°C, 200LFM air flow	10	12	3.3
Thermal Rating T_A = 85°C, no air flow	10	12	1.8

**Maximum T_J = 125°C. For specific operating conditions, see the Safe Operating Area (SOA) curves in the Typical Operating Characteristics section.*

19-101592; Rev 0; 11/22

Simplified Application Circuit



Absolute Maximum Ratings

V_{DDH} to PGND (Note 1) ..... -0.3V to +19V

LX to PGND (DC) ..... -0.3V to +19V

LX to PGND (AC) (Note 2) ..... -10V to +23V

V_{DDH} to LX (DC) (Note 1) ..... -0.3V to +19V

V_{DDH} to LX (AC) (Note 2) ..... -10V to +23V

BST to PGND (DC) ..... -0.3V to +21.5V

BST to PGND (AC) (Note 2) ..... -7V to +25.5V

BST to LX ..... -0.3V to +2.5V

PGND to AGND ..... -0.3V to +0.3V

V_{CC} to PGND ..... -0.3V to +2.5V

AVDD to AGND ..... -0.3V to +2.5V

EN, PGOOD to AGND ..... -0.3V to +4V

SNSP to AGND ..... -0.3V to AVDD+0.3V

SNSN to AGND ..... -0.3V to +0.3V

PGM0, PGM1, PGM2 to AGND ..... -0.3V to AVDD+0.3V

Peak LX Current ..... -21A to +27A

Junction Temperature (T_J) (Note 3) ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Peak Reflow Temperature Lead-Free ..... +260°C

Note 1: Input HF capacitors placed not more than 40 mils away from the V_{DDH} pin required to keep inductive voltage spikes within Absolute Maximum limits.

Note 2: AC is limited to 25ns.

Note 3: Recommended operating junction temperature from -40°C to +125°C. The device guarantees 100k hours of continuous operation with 10A output current at +85°C junction temperature, or 50k hours of continuous operation with 8A output current at +105°C junction temperature, for a typical application with 12V input, 1.2V output.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

25 WLP

Package Code	W252W2Z+1
Outline Number	21-100614
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance	
Junction-to-Ambient Thermal Resistance (θ_{JA}) JEDEC	43.98°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) on MAX16710EVKIT# (no heat sink, no airflow)	24.3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, Refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(See *Typical Application Circuit*. V_{DDH} = 12V, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A =+32°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
Input Voltage Range	V_{DDH}		2.7		16	V
Input Supply Current	I_{VDDH}	EN = AGND		6.5		mA
Internal LDO Regulated Output	V_{CC}		1.71	1.80	1.95	V
Linear Regulator Current Limit			85	170		mA
		V_{CC} < 1.6V		25		
AVDD Undervoltage Lockout	AVDD	Rising	1.65	1.67	1.70	V
AVDD Undervoltage Lockout Hysteresis				55		mV
V_{DDH} Undervoltage Lockout		Rising	2.4	2.5	2.6	V
V_{DDH} Undervoltage Lockout Hysteresis				100		mV
V_{DDH} Overvoltage Lockout		Rising	17.3	17.8	18.3	V
V_{DDH} Overvoltage Lockout Hysteresis				500		mV
Output Voltage Range and Accuracy						
Feedback Voltage	$V_{SNSP} - V_{SNSN}$		0.495	0.500	0.505	V
		$T_A = T_J$ = 0°C to +85°C	0.497	0.500	0.503	
Positive Voltage Sense Leakage Current	I_{SNSP}		-1		1	µA
Negative Voltage Sense Input Range	V_{SNSN}		-100		+100	mV
Negative Voltage Sense Bias Current	I_{SNSN}			300	550	µA
Switching Frequency						
Switching Frequency	F_{SW}			500		kHz
				600		
				750		
				1000		
				1200		
				1500		
Switching Frequency Accuracy			-10		+10	%
Minimum Controllable On-Time		Inductor Valley Current ≤ 0A (Note 4)		36	50	ns
		Inductor Valley Current > 0A (Note 4)		30	45	
Minimum Controllable Off-Time		(Note 4)		100	140	ns
Enable and Startup						
Initialization Time	t_{INIT}			800		µs
EN Threshold		Rising	0.9			V

(See *Typical Application Circuit*. V_{DDH} = 12V, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A =+32°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Falling			0.6	
EN Filtering Delay	$t_{EN\_RISING\_DELAY}$	Rising		250		µs
	$t_{EN\_FALLING\_DELAY}$	Falling		2		
Soft-Start Time	t_{SS}			1		ms
Power Good and Fault Protections						
PGOOD Output Low		I_{PGOOD} = 4mA			0.4	V
Output Undervoltage (UV) Threshold		Falling	-16	-13	-10	%
		Rising		-10		
Output UV Deglitch Delay				4		µs
Output Overvoltage Protection (OVP) Threshold			10	13	16	%
Output OVP Deglitch Delay				2		µs
Positive Overcurrent Protection (POCP) Threshold		Inductor Peak Current, POCP = 15A	13.5	15	16.5	A
		Inductor Peak Current, POCP = 13A	11.7	13	14.3	
		Inductor Peak Current, POCP = 11A	9.8	11	12.1	
POCP Deglitch Delay	t_{POCP}			40		ns
Fast Positive Overcurrent Protection (FPOCP) Threshold			17.1	19	21.4	A
Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio				-86		%
NOCP Accuracy			-20		+20	%
BST UVLO Threshold	V_{BST}	Rising	1.48	1.56	1.64	V
BST UVLO Threshold Hysteresis				52		mV
Overtemperature Protection (OTP) Rising Threshold				155		°C
OTP Accuracy				6		%
OTP Hysteresis				20		°C
Hiccup Protection Time				20		ms
DCM Operation Mode						
DCM Comparator Threshold to Enter DCM		POCP = 15A, Inductor Valley Current		-0.75		A
		POCP = 13A, Inductor Valley Current		-0.67		
		POCP = 11A, Inductor Valley Current		-0.6		
DCM Comparator Threshold to Exit DCM		Inductor Valley Current		0.15		A
Programming Pins						

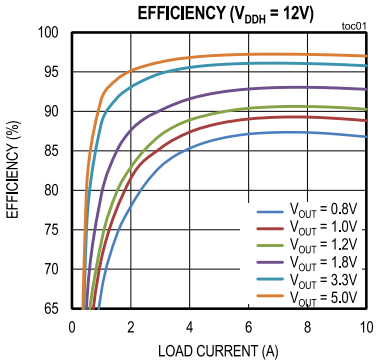
(See *Typical Application Circuit*. V_{DDH} = 12V, $T_A = T_J$ = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A =+32°C; limits within the operating temperature range are guaranteed by design and characterization.)

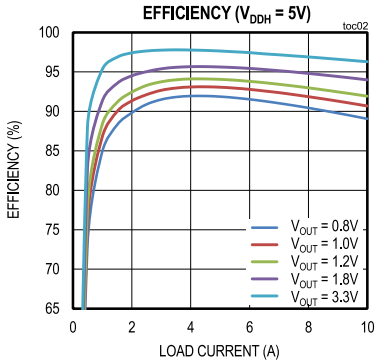
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGM0 Pin Resistor Range			0.095		115	kΩ
PGM0 Resistor Accuracy			-1		+1	%
PGM1 / PGM2 3-Level Detection Thresholds		PGM_ Pin Connected to AVDD	AVDD – 0.2			V
		PGM_ Pin OPEN		0.68		
		PGM_ Pin Connected to AGND or PGM0			0.24 × AVDD	
PGM1 / PGM2 Input Current		PGM_ Pin Connected to AVDD		125		µA
		PGM_ Pin Connected to AGND or PGM0		-125		

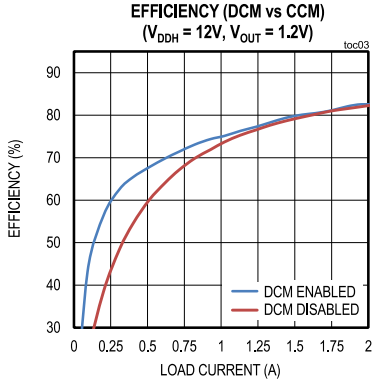
Note 4: Guaranteed by design.

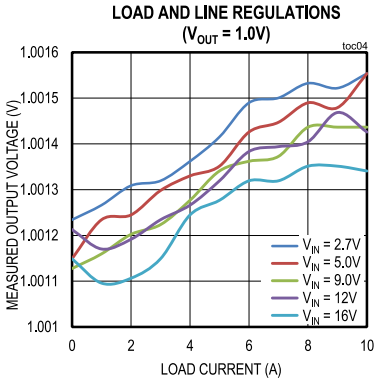
Typical Operating Characteristics

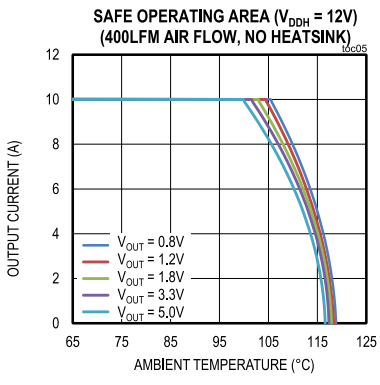
(*Typical Application Circuit*, tested on MAX20815EVKIT#, V_{DDH} = 12V, F_{SW} = 500kHz, T_A = +25°C, Inductor = PA5034.XXXHLT or PA4987.102HL for V_{OUT} > 2.5V, unless otherwise noted.)

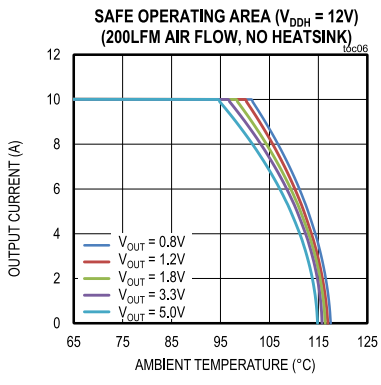




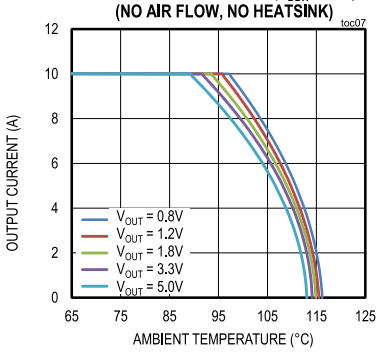




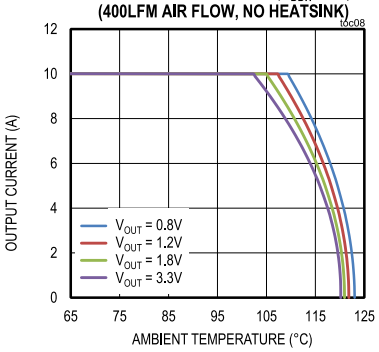




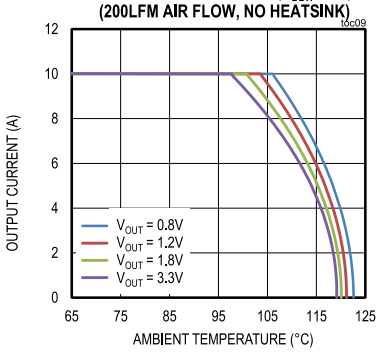
SAFE OPERATING AREA (V_{DDH} = 12V)
(NO AIR FLOW, NO HEATSINK)



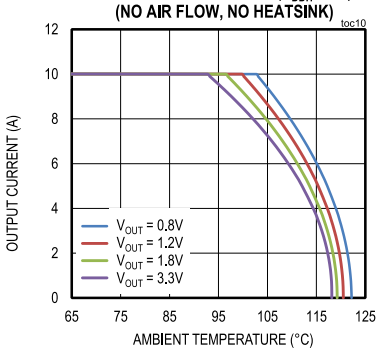
SAFE OPERATING AREA (V_{DDH} = 5V)
(400LFM AIR FLOW, NO HEATSINK)



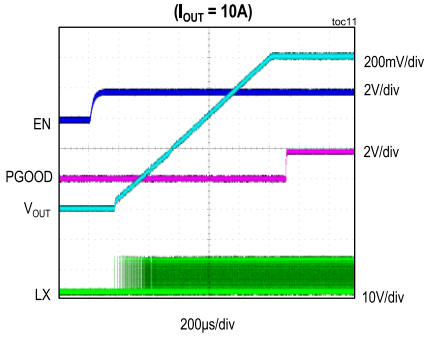
SAFE OPERATING AREA (V_{DDH} = 5V)
(200LFM AIR FLOW, NO HEATSINK)



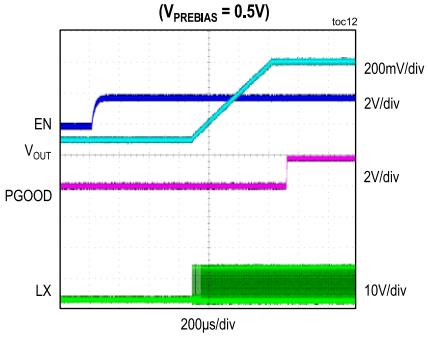
SAFE OPERATING AREA (V_{DDH} = 5V)
(NO AIR FLOW, NO HEATSINK)



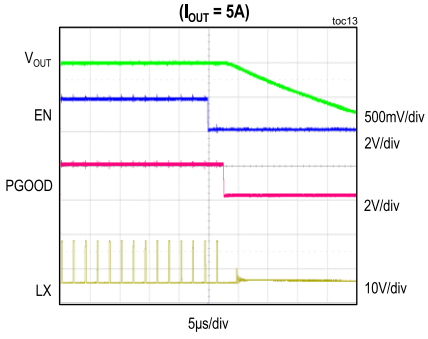
STARTUP
(I_{OUT} = 10A)



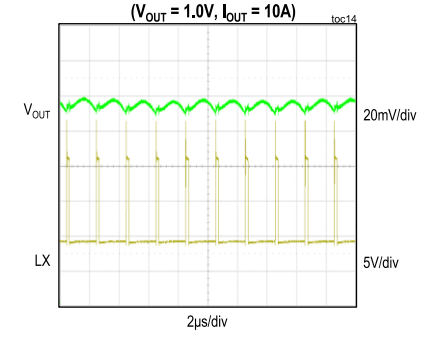
PRE-BIASED STARTUP
($V_{PREBIAS}$ = 0.5V)



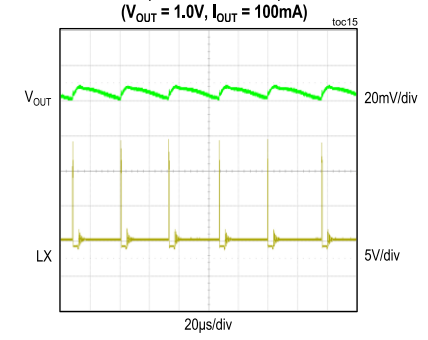
SHUTDOWN
(I_{OUT} = 5A)



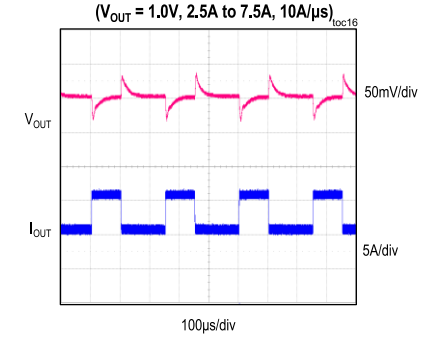
OUTPUT VOLTGE RIPPLE
(V_{OUT} = 1.0V, I_{OUT} = 10A)



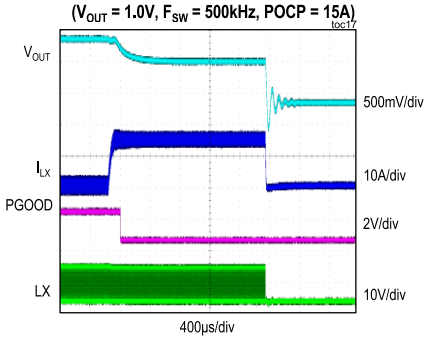
OUTPUT VOLTGE RIPPLE
(DCM OPERATION)
(V_{OUT} = 1.0V, I_{OUT} = 100mA)



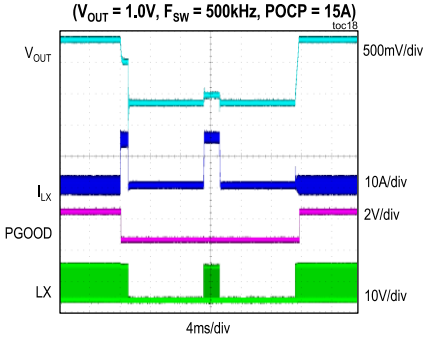
LOAD TRANSIENT RESPONSE
(V_{OUT} = 1.0V, 2.5A to 7.5A, 10A/µs)

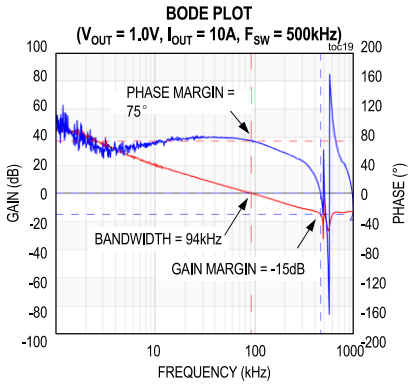


POSITIVE OVERCURRENT PROTECTION
(V_{OUT} = 1.0V, F_{SW} = 500kHz, POCP = 15A)



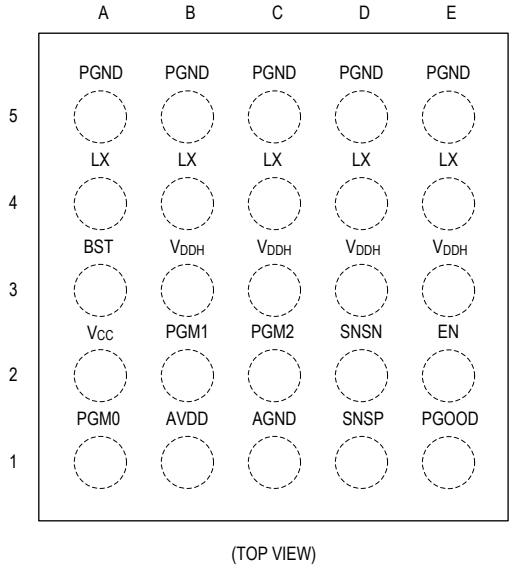
POCP HICCUP AND AUTO-RETRY
(V_{OUT} = 1.0V, F_{SW} = 500kHz, POCP = 15A)





Pin Configuration

25-Bump WLP



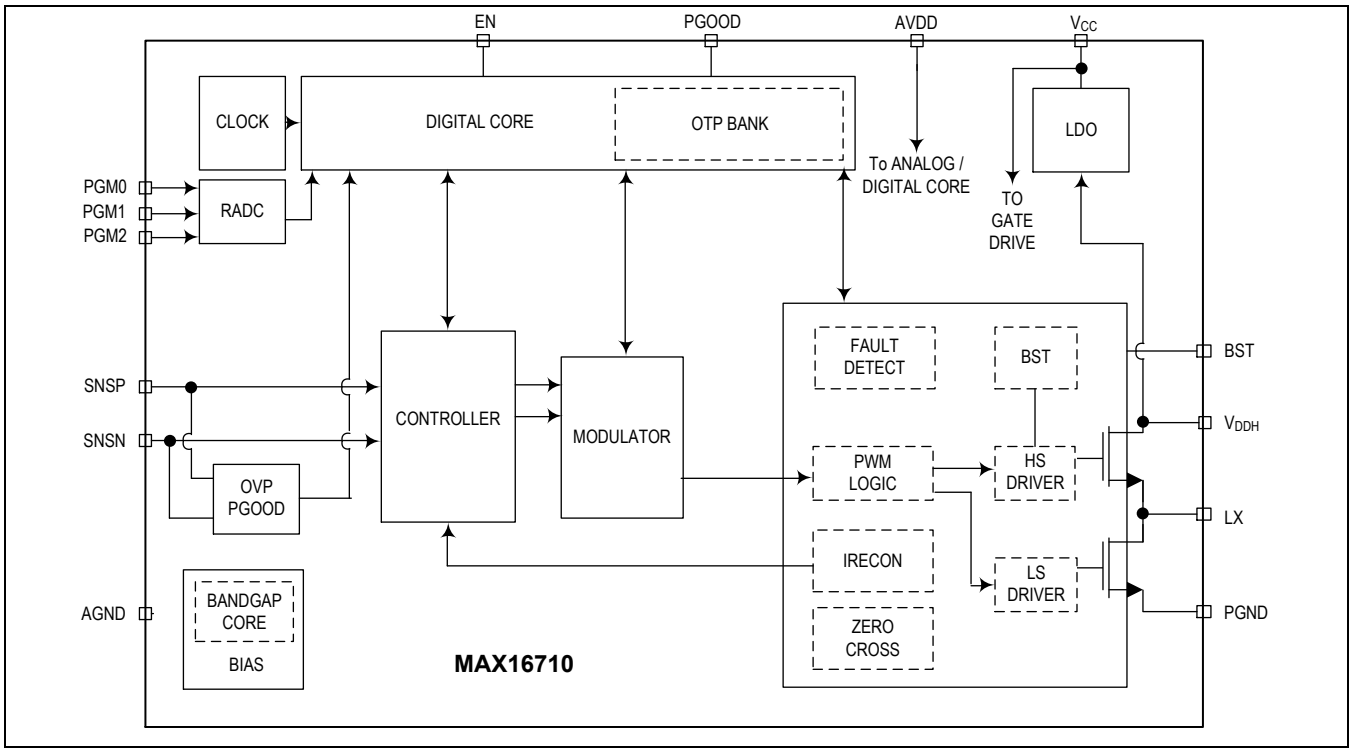
(TOP VIEW)

Pin Descriptions

PIN	NAME	FUNCTION
A1	PGM0	Program Input. Connect this pin to ground though a programming resistor.
B1	AVDD	1.8V Supply for Analog Circuitry. Connect a 2.2Ω to 4.7Ω resistor from AVDD to V_{CC}. Connect a 1µF or greater ceramic capacitor from AVDD to AGND.
C1	AGND	Analog Ground.
D1	SNSP	Output Voltage Remote Sense Positive Input Pin. Connect SNSP to output voltage at the load. A resistive voltage divider can be inserted between the output and SNSP to regulate the output above the reference voltage.
E1	PGOOD	Open-Drain Power-Good Output.
A2	V_{CC}	Internal 1.8V LDO Output. Connect a 4.7µF or greater ceramic capacitor from V_{CC} to PGND.

B2	PGM1	Program Input. Connect this pin to AGND or AVDD or leave it unconnected.
C2	PGM2	Program Input. Connect this pin to AGND or AVDD or leave it unconnected.
D2	SNSN	Output Voltage Remote Sense Negative Input.
E2	EN	Output Enable.
A3	BST	Bootstrap Pin. Connect a 0.47µF ceramic capacitor from BST to LX.
B3, C3, D3, E3	V_{DDH}	Regulator Input Supply.
A4, B4, C4, D4, E4	LX	Switching Node. Connect LX directly to the output inductor.
A4, B4, C4, D4, E4	PGND	Power Ground.

Block Diagram



Detailed Description

Control Architecture

Fixed-Frequency, Peak Current-Mode Control Loop

The MAX16710 control loop is based on the fixed-frequency, peak current-mode control architecture. A simplified control architecture is shown in *Figure 1*. The loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation, and a PWM modulator that generates the PWM signals to drive high-side and low-side MOSFETs. The device has a fixed 0.5V reference voltage (V_{REF}). The difference of V_{REF} and the sensed output voltage is amplified by the first error amplifier. Its output voltage (V_{ERR}) is used as the input of the voltage loop compensation network. The output of the compensation network (V_{COMP}) is fed to a PWM comparator with the current-sense signal (V_{ISENSE}) and the slope compensation (V_{RAMP}). The output of the PWM comparator is the input of the

PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It is a fixed-frequency phase-shifted clock generated by the AMS block (see the *Advanced Modulation Scheme (AMS)* section).

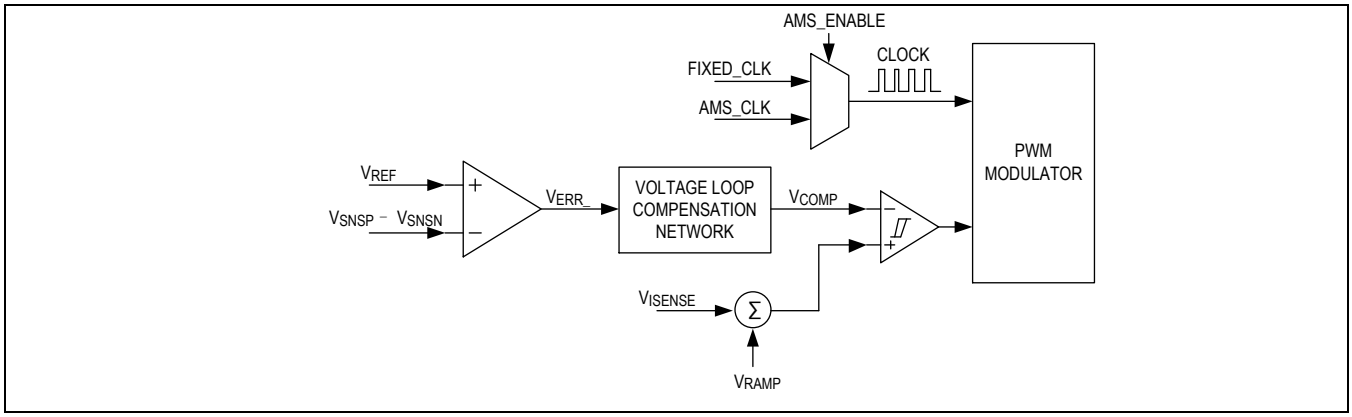


Figure 1. Simplified Control Architecture

Advanced Modulation Scheme (AMS)

The device offers the AMS to provide improved transient response. The AMS provides a significant advantage over conventional fixed-frequency PWM schemes. The AMS feature allows for modulation at both the leading and trailing edges, which result in a temporary increase or decrease of the switching frequency during large load transients. *Figure 2* shows the scheme to include the leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off with minimal delay. Since the total inductor current increases very quickly, thus satisfying the load demand, the current drawn from the output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty. As a result, the output capacitance can be minimized.

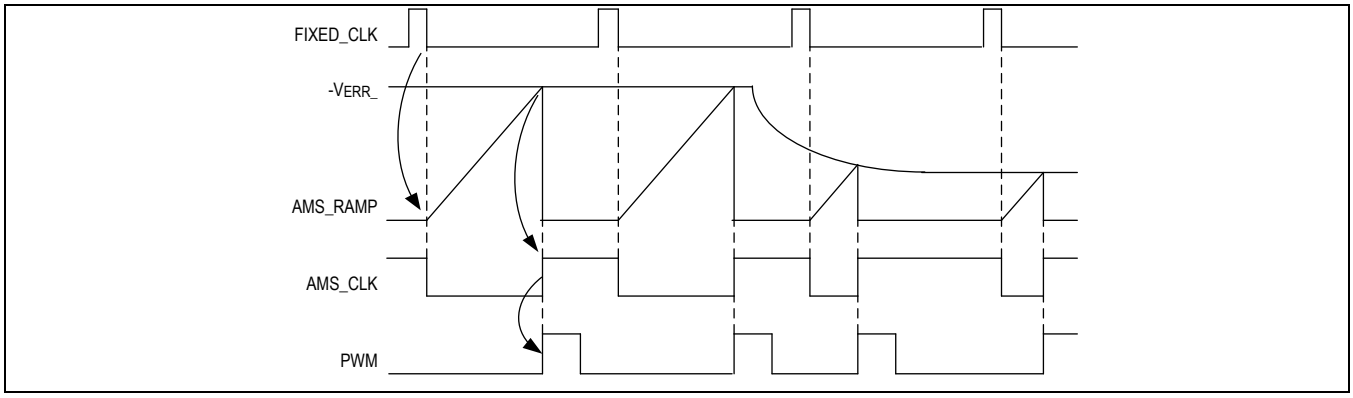


Figure 2. AMS Operation

Discontinuous Current Mode (DCM) Operation

The discontinuous current mode (DCM) operation can be enabled to improve the light-load efficiency. The device has a DCM current-detection comparator to monitor the inductor valley current while operating in the continuous current mode (CCM). At light load, if the inductor valley current is below the DCM comparator threshold for 48 consecutive cycles, the device transitions seamlessly to the DCM. Once in DCM, the switching frequency decreases as load decreases. The MAX16710 transitions back to CCM operation as soon as the inductor valley current is higher than 0.15A.

Internal Linear Regulator

The MAX16710 contains an internal 1.8V linear regulator (LDO). The 1.8V LDO output voltage on V_{CC} is derived from the V_{DDH} pin. It provides the supply voltage for the MOSFET gate drives. A decoupling capacitor of at least 4.7µF must

be connected between the V_{CC} and PGND. The AVDD pin of the MAX16710 also requires a 1.8V supply to power the device's internal analog circuitry. A 2.2Ω to 4.7Ω resistor must be connected between the AVDD and V_{CC}. A 1µF or greater decoupling capacitor must be used between the AVDD and AGND.

Startup and Shutdown

The startup and shutdown timing is shown in *Figure 3*. When the AVDD pin voltage is above its rising UVLO threshold, the device goes through an initialization procedure. Configuration settings on the PGM_ pins are read. Once initialization is complete, the device detects V_{DDH} UVLO and EN status. When both are above their rising thresholds, the soft-start begins and switching is enabled. The output voltage of the enabled output starts to ramp up. The soft-start ramp time is 1ms. If there are no faults, the open-drain PGOOD pin is released from being held low after the soft-start ramp is complete. The device supports smooth startup with the output prebiased.

During operation, if either the V_{DDH} UVLO or EN falls below their thresholds, switching is stopped immediately. The output voltage is discharged by the load current.

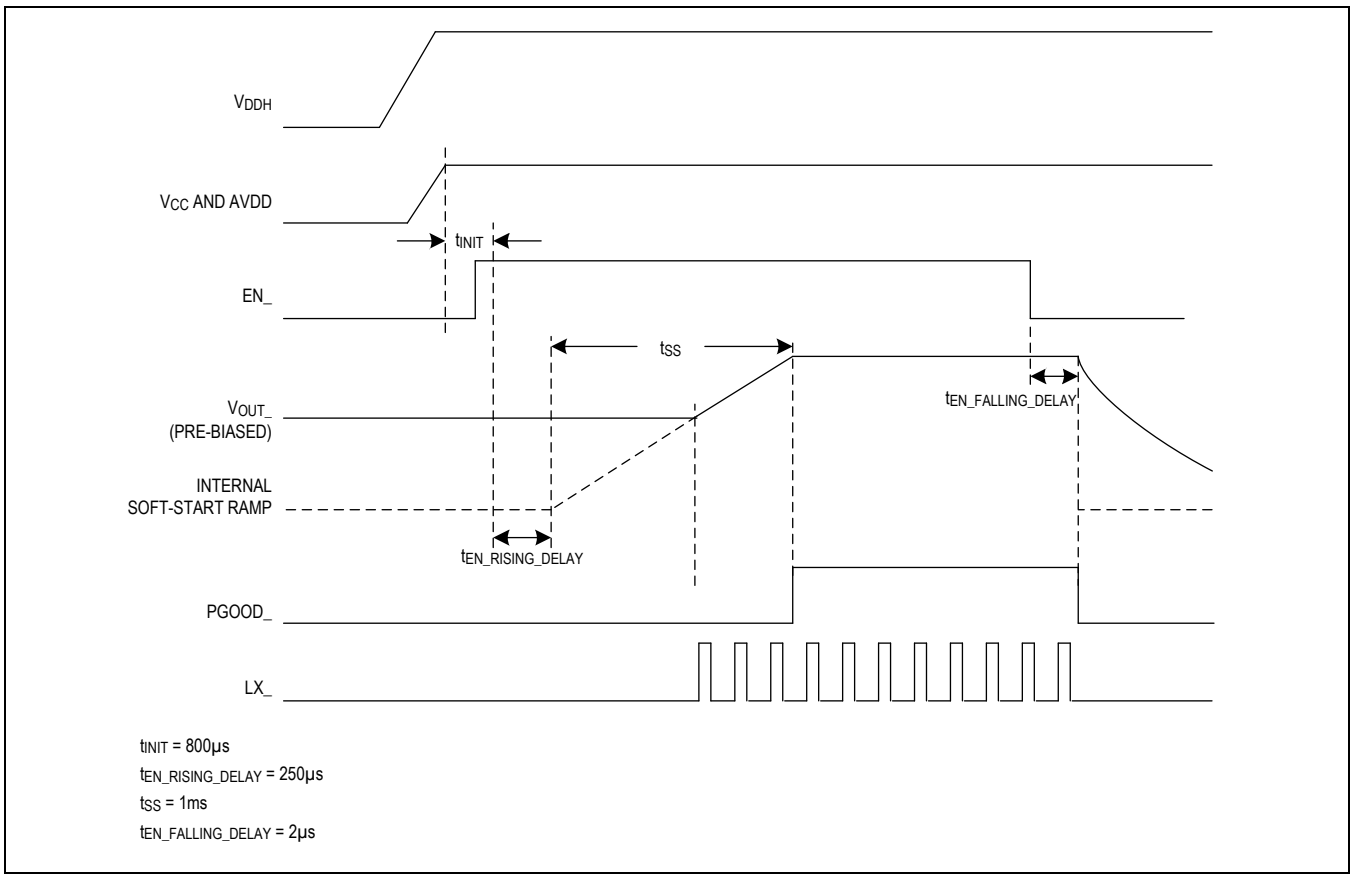


Figure 3. Startup and Shutdown Timing

Fault Handling

Input Undervoltage and Overvoltage Lockout (V_{DDH} UVLO, V_{DDH} OVLO)

The MAX16710 internally monitors the V_{DDH} voltage level. When the input supply voltage is below the UVLO threshold or above the OVLO threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the UVLO or OVLO status is cleared. See the *Startup and Shutdown* section for startup sequence.

Output Overvoltage Protection (OVP)

The feedback voltage on $V_{SNSP} – V_{SNSN}$ is monitored for output overvoltage once the soft-start ramp is complete. If the feedback voltage is above the OVP threshold beyond the deglitch filtering delay, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the OVP status is cleared.

Positive Overcurrent Protection (POCP)

The device's peak current mode control architecture provides inherent current limiting and short-circuit protection. The inductor current is continuously monitored while switching. The inductor peak current limits on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events each switching cycle. If the counter exceeds 1024, the device stops switching and drives the PGOOD pin low. The POCP is a hiccup protection, and the device restarts after 20ms.

The MAX16710 offers three POCP thresholds (15A, 13A, and 11A), which can be selected by the PGM1 and PGM2 pins (see the *Pin-Strap Programmability* section). Due to the POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher (see the *Output Inductor Selection* section).

Negative Overcurrent Protection (NOCP)

The device also has negative overcurrent protection against inductor valley current. The NOCP threshold is -86% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by input voltage. Same as POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives the PGOOD pin low. The NOCP is a hiccup protection, and the device restarts after 20ms.

Overtemperature Protection (OTP)

The overtemperature protection threshold is 155°C with 20°C hysteresis. If the junction temperature reaches OTP threshold during operation, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the OTP status is cleared.

Pin-Strap Programmability

The MAX16710 has three program pins (PGM0, PGM1, and PGM2) to set some of the key configurations of the device. The PGM_ values are read during startup initialization. The PGM0 has 32 detection levels. A pin-strap resistor is connected from PGM0 pin to AGND to select one of the 32 PGM0 codes. See *Table 1* for the PGM0 switching frequencies and scenario selections. PGM0 is used to select the switching frequency and a predefined scenario, which is defined in *Table 3*. The PGM1 and PGM2 each has three levels. The PGM1 or PGM2 can be connected to AVDD or AGND (PGM0) or left OPEN to select the POCP level and DCM operation mode of the device as shown in *Table 2*.

Table 1. PGM0 Switching Frequency and Scenario Selections

PGM0 CODES	R_{PGM0} (Ω)	SWITCHING FREQUENCY (kHz)	SCENARIO #
0	95.3	500	A
1	200		B
2	309		C
3	422		D
4	536		E
5	649		F
6	768	600	A
7	909		B
8	1050		C
9	1210		D
10	1400		E
11	1620		F
12	1870	750	A
13	2150		B
14	2490		C
15	2870		D
16	3740		E
17	8060		F
18	12400	1000	A
19	16900		B
20	21500		C

21	26100		D
22	30900		E
23	36500		F
24	42200	1200	A
25	48700		B
26	56200		C
27	64900		D
28	75000		E
29	86600		F
30	100000	1500	A
31	115000		B

Table 2. PGM1 and PGM2 Settings

PGM1 and 2 CODES	PGM1 CONNECTION	PGM2 CONNECTION	DCM	POCP (A)
0	OPEN	OPEN	Disable	15
1		AGND	Enable	
2		AVDD	Disable	11
3	AGND or PGM0	OPEN	Enable	15
4		AGND	Disable	
5		AVDD	Enable	
6	AVDD	OPEN	Disable	11
7		AGND	Enable	
8		AVDD	Disable	13

The MAX16710 has six predefined scenarios as summarized in *Table 3*, which can be selected by a pin-strap resistor connected from PGM1 pin to AGND. See the *Voltage Loop Gain* section for information to select the voltage loop gain resistance (R_{VGA}) for optimized control loop performance.

Table 3. Predefined Scenarios

SCENARIO #	R_{VGA} (kΩ)
A	15.7
B	22.7
C	26.8
D	31.3
E	37.3
F	44.8

Reference Design Procedure

Output Voltage Sensing

The MAX16710 has an internal 0.5V reference voltage. When the desired output voltage is higher than 0.5V, it is required to use a resistor-dividers R_{FB1} and R_{FB2} to sense the output voltage (see the *Typical Application Circuit*). It is recommended that the value of R_{FB2} does not exceed 5kΩ. The resistor-divider ratio is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:

V_{OUT} = Output voltage

V_{REF} = 0.5V fixed reference voltage

R_{FB1} = Top divider resistor

R_{FB2} = Bottom divider resistor

Selecting the Switching Frequency

The MAX16710 offers a wide range of selectable switching frequencies from 500kHz to 1.5MHz. Switching frequency selection can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation due to reduced switching losses. It is required that the frequency be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SWMAX} = MIN\left\{\frac{V_{OUT}}{t_{ONMIN} \times V_{DDHMAX}}, \frac{V_{DDHMIN} - V_{OUT}}{t_{OFFMIN} \times V_{DDHMIN}}\right\}$$

where:

f_{SWMAX} = Maximum selectable switching frequency

V_{DDHMAX} = Maximum input voltage

V_{DDHMIN} = Minimum input voltage

T_{ONMIN} = Minimum controllable on-time

T_{OFFMIN} = Minimum controllable off-time

The MAX16710 internally has a slope compensation applied to the current loop during on-time to guarantee stability and improve noise immunity. To avoid the slope compensation saturating the current loop, it is required that the maximum on-time be limited by:

$$T_{ONMAX} = \frac{5pF\left[800mV \times \left(I_{OUTMAX} + \frac{I_{RIPPLE}}{2}\right) \times \frac{1.6\Omega}{62.5}\right]}{1.89\mu A}$$

where:

T_{ONMAX} = Maximum on-time of the high-side MOSFET

I_{OUTMAX} = Maximum load current

I_{RIPPLE} = Inductor current ripple peak-to-peak value

The minimum recommended switching frequency is calculated by the following equation:

$$f_{SWMIN} = \frac{V_{OUT}}{T_{ONMAX} \times V_{DDHMIN}}$$

where:

f_{SWMIN} = Minimum selectable switching frequency

Due to system noise injection, even at steady-state operation, typically the LX rising and falling edges would have some random jittering noise. The selection of the switching frequency f_{SW} should take into consideration the jittering and be higher than f_{SWMIN} and lower than f_{SWMAX}. To improve the LX jittering, it is recommended to use smaller inductor values and lower voltage loop gain to minimize the noise sensitivity.

Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance. Typically, the output inductor is selected so that the inductor current ripple is 20% to 40% of the maximum load current for optimized performance. To improve current loop noise immunity, it is recommended that the inductor current ripple is at least 2A. The inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{RIPPLE} \times f_{SW}}$$

where:

V_{DDH} = Input voltage

I_{RIPPLE} = Inductor current ripple peak-to-peak value

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX16710 offers three POCP thresholds (15A, 13A, and 11A), which can be selected by the PGM1 and PGM2 pins (see the *Pin-Strap Programmability* section) . Due to deglitch delay from the POCP comparator tripping to the high-side MOSFET turning off for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where:

$POCP_{ADJUST}$ = Adjusted POCP threshold

POCP = POCP level specified in the *Electrical Characteristics* table

t_{POCP} = POCP deglitch delay (40ns typical)

It needs to be verified that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$I_{OUTMAX} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where:

I_{OUTMAX} = Maximum load current

$POCP_{ADJUST(MIN)}$ = Minimum adjusted POCP threshold, calculated with the minimum value of the POCP threshold

Table 4 shows some suitable inductor part numbers which are verified on the MAX16710 evaluation kit to offer optimal performance.

Table 4. Recommended Inductors

COMPANY	VALUE (nH)	I_{SAT} (A)	R_{DC} (mΩ)	FOOTPRINT (mm)	HEIGHT (mm)	PART NUMBER
Eaton	220	58	0.17	10.8 × 8.0	8.0	FP1008R5-R220-R
Eaton	270	44	0.17	10.8 × 8.0	8.0	FP1008R5-R270-R
Pulse	330	40	0.4	10.0 × 7.0	10.0	PA5034.331HLT
Pulse	470	30	0.4	10.0 × 7.0	10.0	PA5034.471HLT
Pulse	1000	20.5	0.81	10.0 × 7.0	10.0	PA4987.102HLT

Output Capacitor Selection

One major factor in determining the total required output capacitance is the output-voltage ripple. To meet the output-voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where:

$V_{OUTRIPPLE}$ = Maximum allowed output-voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output-voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance should also satisfy the following equation:

$$C_{OUT} \geq MAX \left\{ \frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times (V_{DDH} - V_{OUT})}, \frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times V_{OUT}} \right\}$$

where:

C_{OUT} = Output capacitance

$\triangle I$ = Loading or unloading current step

$\triangle V_{OUT}$ = Maximum allowed output voltage undershoot or overshoot

Input Capacitor Selection

The selection of input capacitance is determined by the requirement of input-voltage ripple. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{f_{SW} \times V_{DDH} \times V_{INPP}}$$

where:

$I_{OUT(MAX)}$ = Maximum output current

V_{OUT} = Output voltage

f_{SW} = Switching frequency

V_{INPP} = Peak-to-peak input voltage ripple

Besides the minimum required input capacitance, it is required to also place 0.1µF and 1µF high-frequency decoupling capacitors next to the V_{DDH} pin to suppress the high-frequency switching noises.

Voltage Loop Gain

For stability purpose, it is recommended that the voltage loop bandwidth (BW) must be lower than 1/5 of the switching frequency. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The voltage loop BW can be estimated with the following equation:

$$BW = \frac{\frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 8m\Omega \times C_{OUT}}$$

where:

R_{VGA} = The voltage loop gain resistance, which is set by the scenario selected (*Table 3*).

Typical Reference Designs

See the *Typical Application Circuit* or examples of reference schematics. Reference design examples for some common output voltages are shown in *Table 5*.

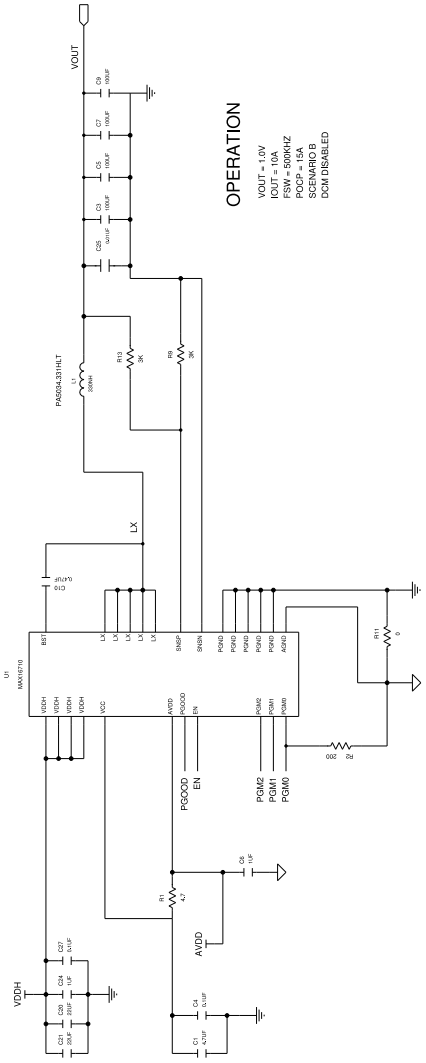
Table 5. Reference Design Examples

V_{OUT} (V)	I_{OUT} (A)	f_{SW} (kHz)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	PGM0 (Ω)	PGM1	PGM2	L (nH)	C_{IN}	C_{OUT}
0.8	10	750	1.82	3.01	1870	OPEN	OPEN	330	2 × 10µF +1µF +0.1µF	4 × 100µF
0.9	10	750	2.40	3.01	1870	OPEN	OPEN	330	2 × 10µF +1µF +0.1µF	4 × 100µF
1.0	10	750	3.01	3.01	1870	OPEN	OPEN	330	2 × 10µF +1µF +0.1µF	4 × 100µF
1.2	10	750	4.22	3.01	1870	OPEN	OPEN	470	2 × 10µF +1µF +0.1µF	4 × 100µF
1.8	8	1000	7.87	3.01	12400	OPEN	OPEN	470	2 × 10µF +1µF +0.1µF	3 × 100µF
3.3	7	1200	16.9	3.01	42200	AVDD	AVDD	1000	2 × 10µF +1µF +0.1µF	3 × 100µF
5.0	6	1500	22.6	2.49	100000	OPEN	AVDD	1000	2 × 10µF +1µF +0.1µF	3 × 47µF

PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.
- The input decoupling capacitor should be located closest to the IC and no more than 40mils from the V_{DDH} pin.
- The V_{CC} decoupling capacitors should be connected to PGND and placed as close as possible to the V_{CC} pin.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This “quiet” analog ground copper polygon or island should be connected to the PGND through a single connection close to the AGND pin. The analog ground can be used as a shield and ground reference for the control signals.
- The AVDD decoupling capacitors should be connected to AGND and placed as close as possible to the AVDD pin.
- The boost capacitors should be placed as close as possible to the LX and BST pins on the same side of the PCB with the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize the noise injection.
- Output voltage should be sensed with the differential remote sense lines routed directly from an output capacitor from the load point, shielded by the ground plane, and be kept away from the switching node and the inductor.
- Multiple vias are recommended for all paths that carry high currents and for heat dissipation.
  - The input capacitors and output inductors should be placed near the IC and the traces to the components should be kept as short and wide as possible to minimize the parasitic inductance and resistance.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16710AWA+	-40°C to +125°C	25-Bump WLP
MAX16710AWA+T	-40°C to +125°C	25-Bump WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/22	Release for Market Intro	—

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