High-Voltage Ideal Diode Controller with Integrated CSA

MAX16170

General Description

The MAX16170, a high-voltage ideal diode controller, offers full system-level protections for automotive applications. The MAX16170 is designed to enhance system safety, reliability, and performance with added diagnostics, robust fault-recovery mode, and a high-side, integrated current-sense amplifier (CSA). The MAX16170 features dual-gate-driver topology that supports common-drain configuration and protects systems against reverse voltage, input overvoltage (OV), undervoltage (UV), overcurrent, and thermal fault conditions. During power-up, the device monitors the health of the external power metal-oxide semiconductor field effect transistors (MOSFETs) for open or short-circuit conditions and asserts an open-drain output (FETOK) when one or both power MOSFETs are damaged. Additionally, the device offers an open-drain fault output ($\overline{FLT}$) that asserts low when there is a fault condition.

During normal operation, the MAX16170 regulates the voltage drop across the drain-to-source of MOSFET (Q1) to 10mV to block DC flow to the battery in reverse voltage fault condition. A resistor from a low-voltage input (ILIM) to ground sets the overcurrent threshold.

During sleep mode of operation, the device consumes only 5uA (typ) while delivering 1mA (min) of current to the load to support stand-by system operation. In shutdown mode, the charge pump is disabled, and the OV and UV resistive dividers are disconnected from the battery through the TERM switch to lower the shutdown supply current to 3µA (typ).

The MAX16170 is available in a 4mm x 4mm x 0.75mm, 20-pin, side-wettable, TQFN package with an exposed pad and operates over the automotive temperature range of −40°C to +125°C.

Applications

- Automotive Power Systems
- Network/Telecom Power Systems
- RAID Systems
- Servers
- PoE Systems

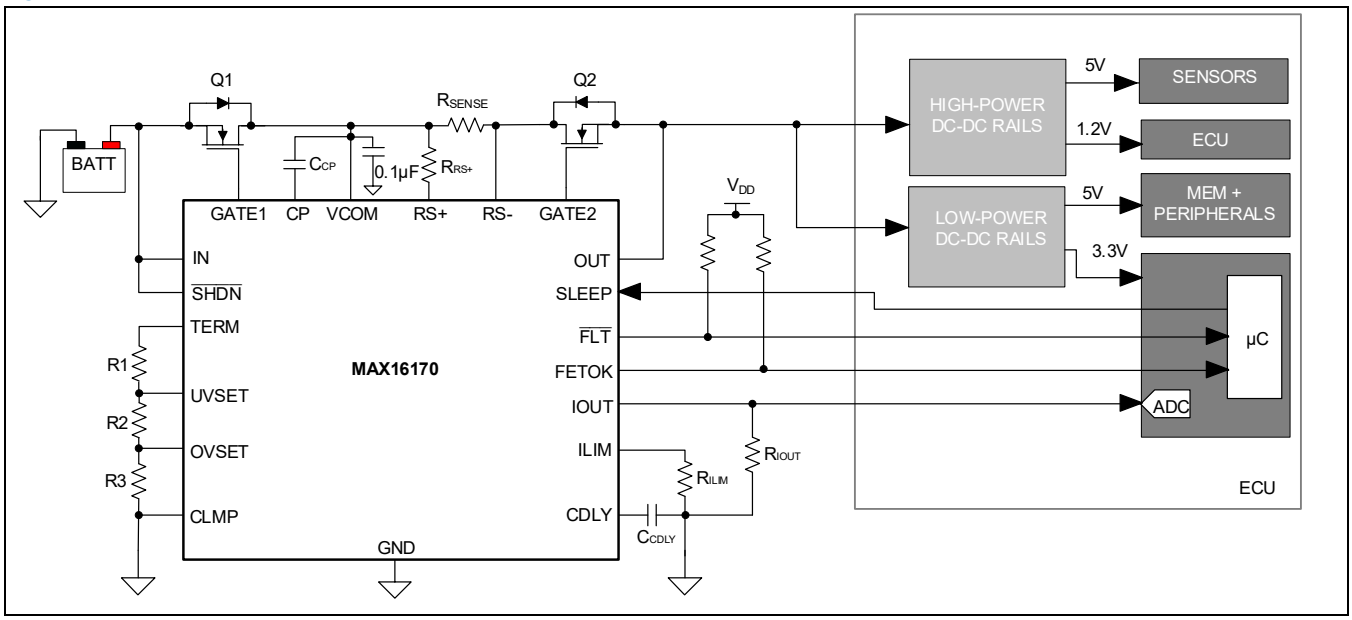
Features and Benefits

- AEC-Q100 Qualified for Automotive Applications
- 3V to 65V Operating Voltage Range
  - Supports 12V/24V Battery Systems
- −42V to +76V Input Protection Range
  - Wider Transients Immunity
- High-Side CSA
  - Enables System Power-Level Measurement
- Output Sensing
  - Enables Fast Fault Recovery
- 30kHz Active Rectification
  - Facilitates System Level Testing Per Automotive Standard
- Support ORing Application
- Robust Fault-Recovery Mode
- 5µA Shutdown Mode Current
  - Extends Battery Life
- Resistor-Adjustable OCP Threshold
  - Adds Design Flexibility
- 1mA (min) Sleep Mode Current Output
  - Supports Standby Mode of Operation
- FETOK/$\overline{FLT}$ Outputs
  - Enhance System Diagnostics

Ordering Information appears at end of data sheet.

19-101635; Rev 0; 1/24

Typical Application Circuit



Absolute Maximum Ratings

IN, GATE1, $\overline{SHDN}$ to GND ..... −42V to +76V

VCOM, GATE2, RS+, RS−, OUT, TERM to GND ..... −0.3V to +76V

UVSET to GND ..... −0.3V to +15V

GATE1 to IN, GATE2 to OUT ..... −0.3V to +15V

IN to $\overline{SHDN}$, TERM ..... −42V to +76V

CP to VCOM ..... −0.3V to +18V

CP to IN, GATE1 ..... −0.3V to +76V

VCOM to IN ..... −18V to +65V

IN to OUT ..... −65V to +76V

SLEEP, $\overline{FLT}$, FETOK, OVSET, IOUT, CDLY, CLMP, ILIM to GND ..... −0.3V to +6V

Continuous Sink/Source Current (all pins except $\overline{FLT}$) .. ±20mA

$\overline{FLT}$ Continuous Sink/Source Current ..... ±5mA

Continuous Power Dissipation (TQFN 20-Pin (T2044Y+4C) derate 30.3mW/°C above +70°C) 2424mW

Operating Temperature Range ..... −40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... −60°C to +150°C

Lead Temperature (soldering 10s) ..... +300°C

Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20-TQFN

Package Code	T2044Y+3C
Outline Number	*21-100068*
Land Pattern Number	*90-0409*
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W
THERMAL RESISTANCE, MULTI-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	33°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html* . Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html* .

Electrical Characteristics

(V_{IN} = 12V, R_{IOUT} = 330kΩ, R_{RS+} = 1kΩ, V_{SENSE} = 10mV, C_{CP} = 0.1µF, T_A = −40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25°C. *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Operating range	3		65	V
V_{IN} Start-Up Voltage	V_{SU_IN}	V_{IN} Rising	4			V
VCOM Undervoltage Lockout	V_{VCOM_UVLO}	V_{VCOM} Rising		2.6	2.8	V
Maximum Input Voltage to Disable GATE1 and GATE2				67		V
Input Voltage Protection Range	V_{IN_PROT}		−42		76	V
Output Voltage Range	V_{OUT}	After Start-Up	3		65	V
V_{OUT} Undervoltage Lockout Voltage	V_{OUT_UVLO}			2.6		V
Input Supply Current	I_{VCOM}	$V_{\overline{SHDN}}$ = V_{IN} = V_{OUT} = 12V, RS+ shorted to RS−		370	690	µA
		$V_{\overline{SHDN}}$ = V_{IN} = V_{OUT} = 24V, RS+ shorted to RS−		380	700	
Shutdown Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, V_{IN} = V_{OUT} = 12V		3	10	µA
		$V_{\overline{SHDN}}$ = 0V, V_{IN} = V_{OUT} = 24V		6	15	
Sleep Mode Current	I_{SLEEP}	V_{SLEEP} = High, V_{IN} = V_{OUT} = 12V		5	15	µA
		V_{SLEEP} = High, V_{IN} = V_{OUT} = 24V		9	20	
CLMP Internal Pull-Up Resistor	R_{CLMP}			10		MΩ
IN Leakage Current	I_{IN_LK}	V_{IN} = 0V to −42V		4	10	µA
UVSET/OVSET Input Current				3	100	nA
UVSET/OVSET Threshold Voltage	V_{TH}			0.5		V
UVSET/OVSET Threshold Voltage Accuracy	V_{TH_AC}		−1.8		+1.8	%
UVSET Threshold Voltage Hysteresis	V_{TH_HYS}	For UV V_{IN} rising		20		% of V_{INTH}
OVSET Threshold Voltage Hysteresis	V_{TH_HYS}	For OV V_{IN} falling		5		% of V_{INTH}
TERM Resistance	R_{TERM}			0.15	0.4	kΩ
Start-Up Time	t_{SU}	From the time V_{VCOM} cross POR to the GATE1 enabled; C_{CP} = 0.1µF		800		µs

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OV to GATE2 Prop Delay		V_{IN} rising from (V_{TH_OV}−100mV) to (V_{TH_OV}+100mV)	GATE2 starts falling		0.4		µs
UV to GATE1 Prop Delay		V_{IN} falling to (V_{TH_UV} +100mV) to (V_{TH_UV}−100mV)	GATE1 starts falling		0.4		µs
OV or UV to $\overline{FLT}$ Prop Delay		V_{IN} rising from (V_{TH_OV} −100mV) to (V_{TH_OV}+100mV)	$\overline{FLT}$ starts falling		0.3		µs
SLEEP Mode Output Current		V_{SLEEP} = High, V_{IN} = 12V, V_{OUT} = 10V		1	2.5		mA
SLEEP Mode Clamp		V_{CLMP} = High		18	26	36	V
		V_{CLMP} = Low		36	52	72	
$\overline{SHDN}$, SLEEP, CLMP Input Voltage High	V_{IH}			1.4			V
$\overline{SHDN}$, SLEEP, CLMP Input Voltage Low	V_{IL}					0.4	V
$\overline{FLT}$, FETOK Output Voltage Low	V_{OL}					0.4	V
$\overline{FLT}$, FETOK Leakage Current					4	100	nA
OCP Threshold		R_{ILIM} = 10kΩ		17.2	20	22.8	mV
		R_{ILIM} = 20kΩ		27	30	33	
		R_{ILIM} = 30kΩ		36	40	44	
		R_{ILIM} = 40kΩ		45	50	55	
OCP Response Time		20mV overdrive C_{GS2} = 10nF, C_{CDLY} = floating	GATE2 discharge to 1V+V_{OUT}		5		µs
OUT Short-Circuit Response Time		20mV overdrive, C_{GS2} = 10nF,	V_{OUT} shorted to GND after OC and before CDLY grounded, GATE2 discharge to 2V		3	10	µs
OCP Blanking Time		OV fault removed, V_{OUT} > V_{VOUT_UVLO}			400		µs
		Note 2			400		
CDLY Ramp Threshold Voltage	V_{CDLY}			0.95	1	1.05	V
CDLY Ramp Current	I_{CDLY}			8	10	12	µA
Auto-Retry Timing		Response to OC and UV			300		ms
Thermal Shutdown					145		˚C
Thermal Shutdown Hysteresis					10		˚C

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RS+ Leakage Current		Shutdown mode, $V_{\overline{SHDN}}$ = 0V		0.01	0.1	µA
RS− Leakage Current		Shutdown mode, $V_{\overline{SHDN}}$ = 0V		0.4	1	µA
CHARGE PUMP						
Charge Pump Current	I_{CP}	(V_{CP}−V_{IN}) = 7V, V_{VCOM} = 6V	0.5	1.0		mA
		(V_{CP}−V_{IN}) = 7V, 12V ≤V_{VCOM} ≤ 65V	0.7	1.5		
Charge Pump Turn-On Voltage		V_{CP}-V_{VCOM}	8	9	10.2	V
Charge Pump Turn-Off Voltage			8.8	10	11.2	V
Charge Pump Rising UVLO Threshold	V_{CP_UVLO+}		4.5	5.5	6.5	V
Charge Pump Falling UVLO Threshold	$V_{CP\_UVLO−}$		4	5	6	V
GATE2 DRIVER						
V_{GATE2}-V_{OUT}	V_{GS2}	3V ≤ V_{VCOM} < 5V	6.8	7.6		V
	V_{GS2}	5V < V_{VCOM} ≤ 65V	8	9.6	11.2	
GATE2 Soft-Start Pull-Up Current	I_{GS2_SS}	V_{OUT} < V_{OUT_UVLO}	10	25	40	µA
GATE2 Pull-Down Current	I_{GS2_PD}	V_{OV} > V_{OVSET_TH}		300		mA
GATE2 Fast Pull-Up Current	I_{GS2_PUF}	V_{OUT} > V_{OUT_UVLO}		7		mA
GATE1 DRIVER						
Maximum GATE1 Voltage	V_{GS1}	V_{GS1} = V_{GATE}−V_{IN} 3V ≤ V_{VCOM} < 5V	6.8	7.6		V
		V_{GS1} = V_{GATE1}−V_{IN} 5V < V_{VCOM} ≤ 65V	8	9.6	11.2	
GATE1 Peak Pull-Up Current	I_{GATE1_PU}	V_{IN}−V_{COM} = 100mV, V_{GATE1} −V_{IN} = 1V		55		mA
GATE1 Peak Pull-Down Current	I_{GATE1_PDPK}	V_{IN}−V_{COM} = −20mV, V_{GATE1} -V_{IN} = 11V		1200		mA
GATE1 Regulation Current		V_{IN}−V_{COM} = 0V, V_{GATE1} -V_{IN} = 11V		22		µA
Regulation Voltage	V_{IN}−V_{COM}		6	10	15	mV
Forward Voltage Threshold	V_{IN}−$V_{COM,\ FW}$		50	70	100	mV
GATE1 to IN Resistance				2.0		MΩ
Reverse Current Threshold Voltage	V_{REV_TH}	V_{IN}−V_{COM}	−17	-10	−4	mV
GATE1 Reverse Voltage Turn-Off Time	t_{REV_OFF}	V_{VCOM}−V_{IN} =V_{REV_TH} + 40mV		0.3	1	µs

(V_{IN} = 12V, R_{IOUT} = 330kΩ, R_{RS+} = 1kΩ, V_{SENSE} = 10mV, C_{CP} = 0.1µF, T_A = −40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25°C. *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE1 Reverse Voltage Turn-On Time	t_{REV_RECOV}	V_{IN}−V_{VCOM} = −20mV to 130mV to V_{GATE1}-V_{IN} > 5V, C_{GS1} = 10nF		5	8	µs
AC Input Rectification Frequency		V_{GS1} > 5V C_{GS1} = 10nF		30		kHz
CURRENT-SENSE AMPLIFIER						
Input Offset Voltage		T_A = 25˚C, V_{RS+} = 4.5V to 65V	−100	30	100	µV
		T_A = −40°C to 125°C, V_{RS+} = 4.5V to 65V	−160		160	
Gain Error		V_{SENSE} =10mV, V_{RS+} = 4.5V to 65V	−1	0.1	1	%
Signal Bandwidth	f_{BW}	V_{SENSE} =5mVpp		35		kHz
IOUT Voltage	V_{IOUT}	V_{SENSE} =−10mV		5		µV
IOUT Maximum Voltage	V_{IOUT_MAX}	V_{RS+} = 4.5V to 65V, 1% Gain Error	3.3			V

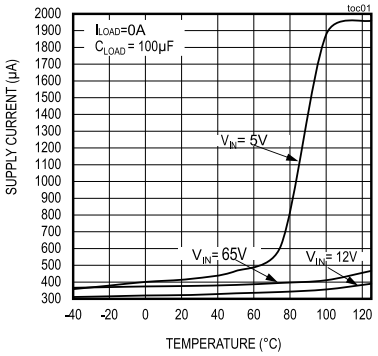
Note 1: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

Note 2: Once reverse voltage event is triggered (V_{IN} < V_{VCOM} + V_{REV_TH}), GATE1 pulls low and overcurrent protection (OCP) is disabled. When reverse voltage event recovers and GATE1 pulls high, OCP and 400µs (Typ) blanking time is active.

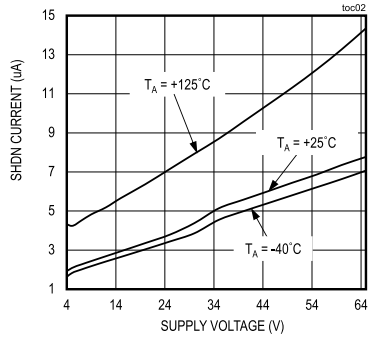
Typical Operating Characteristics

(V_{IN} = 12V, R_{IOUT} = 330kΩ, R_{RS+} = 1kΩ, V_{SENSE} = 10mV, C_{CP} = 0.1µF, T_A = −40°C to +125°C, unless otherwise noted.)

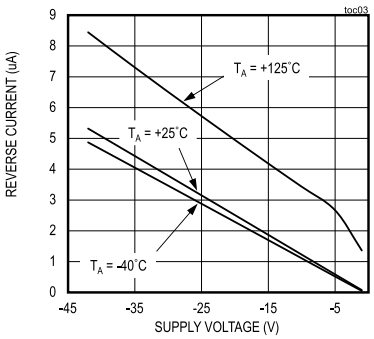
SUPPLY CURRENT vs. TEMPERATURE



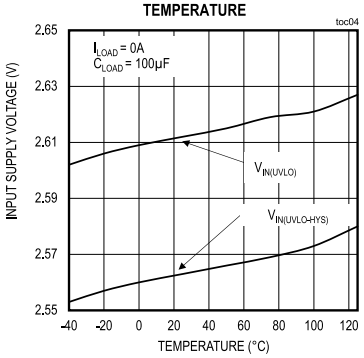
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



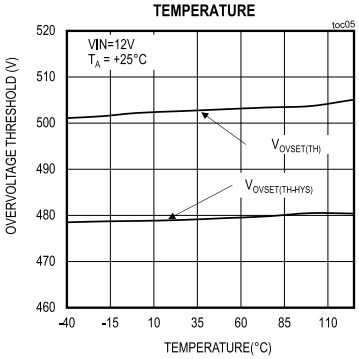
REVERSE CURRENT vs. NEGATIVE SUPPLY VOLTAGE



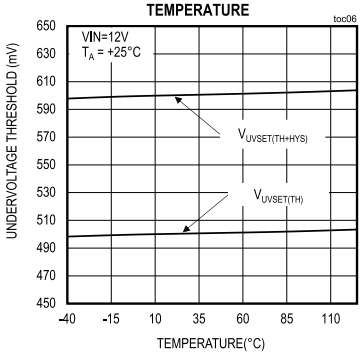
UVLO VOLTAGE vs. TEMPERATURE



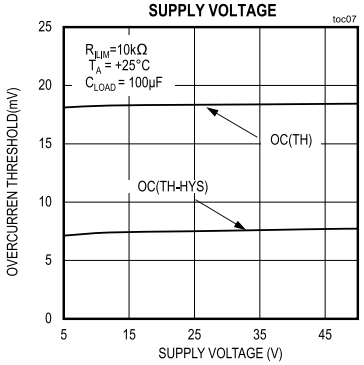
OVERVOLTAGE THRESHOLD vs. TEMPERATURE



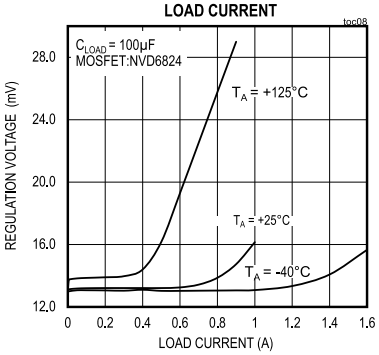
UNDERVOLTAGE THRESHOLD vs. TEMPERATURE



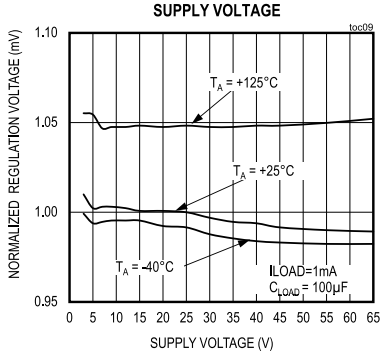
OVERCURRENT THRESHOLD vs. SUPPLY VOLTAGE



REGULATION VOLTAGE vs. LOAD CURRENT



REGULATION VOLTAGE vs. SUPPLY VOLTAGE



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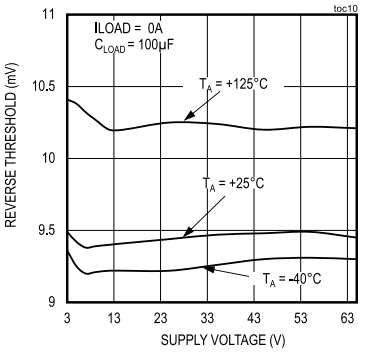
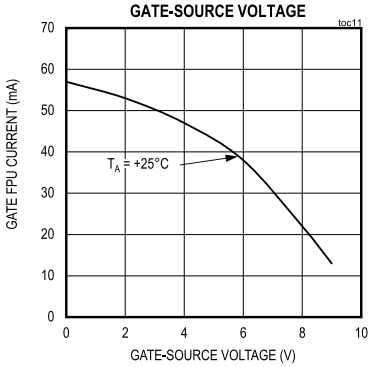
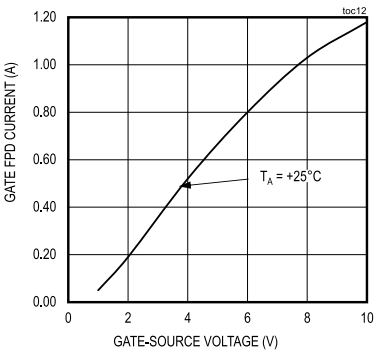
REVERSE THRESHOLD vs. SUPPLY VOLTAGE



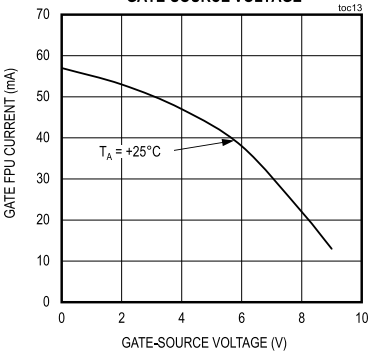
GATE1 FAST PULL-UP CURRENT vs. GATE-SOURCE VOLTAGE



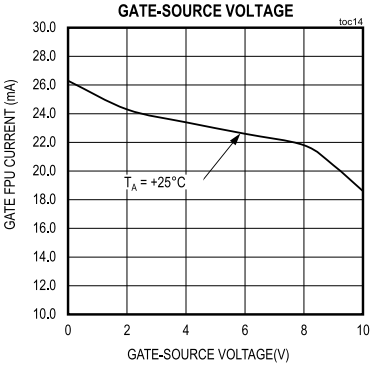
GATE1 FAST PULL-DOWN CURRENT vs. GATE-SOURCE VOLTAGE



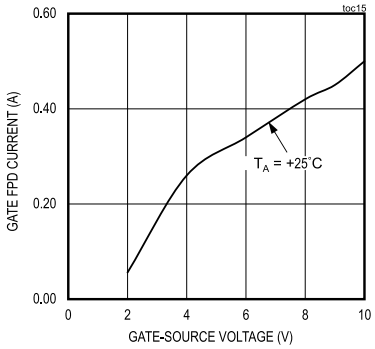
GATE2 FAST PULL-UP CURRENT vs. GATE-SOURCE VOLTAGE



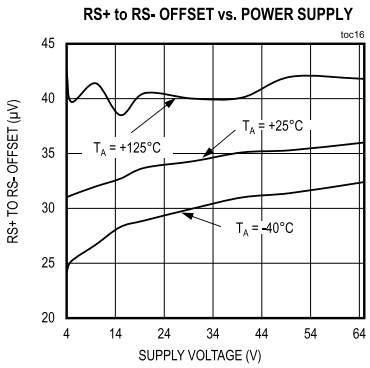
GATE2 SLOW PULL-UP CURRENT vs. GATE-SOURCE VOLTAGE



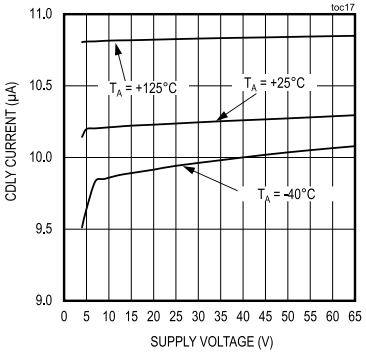
GATE2 FAST PULL-DOWN CURRENT vs. GATE-SOURCE VOLTAGE



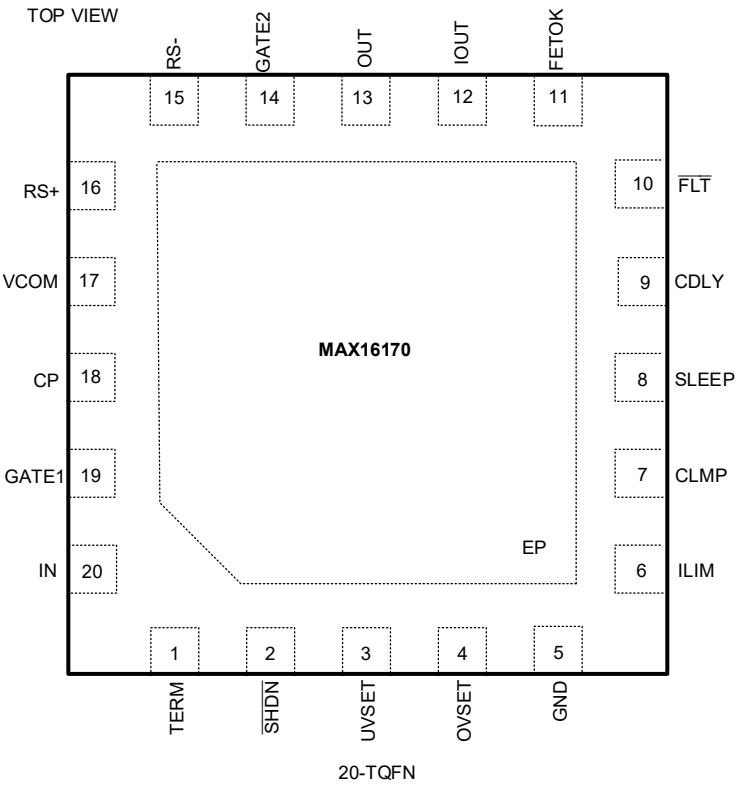
RS+ to RS- OFFSET vs. POWER SUPPLY



CDLY CURRENT vs. POWER SUPPLY



Pin Configurations

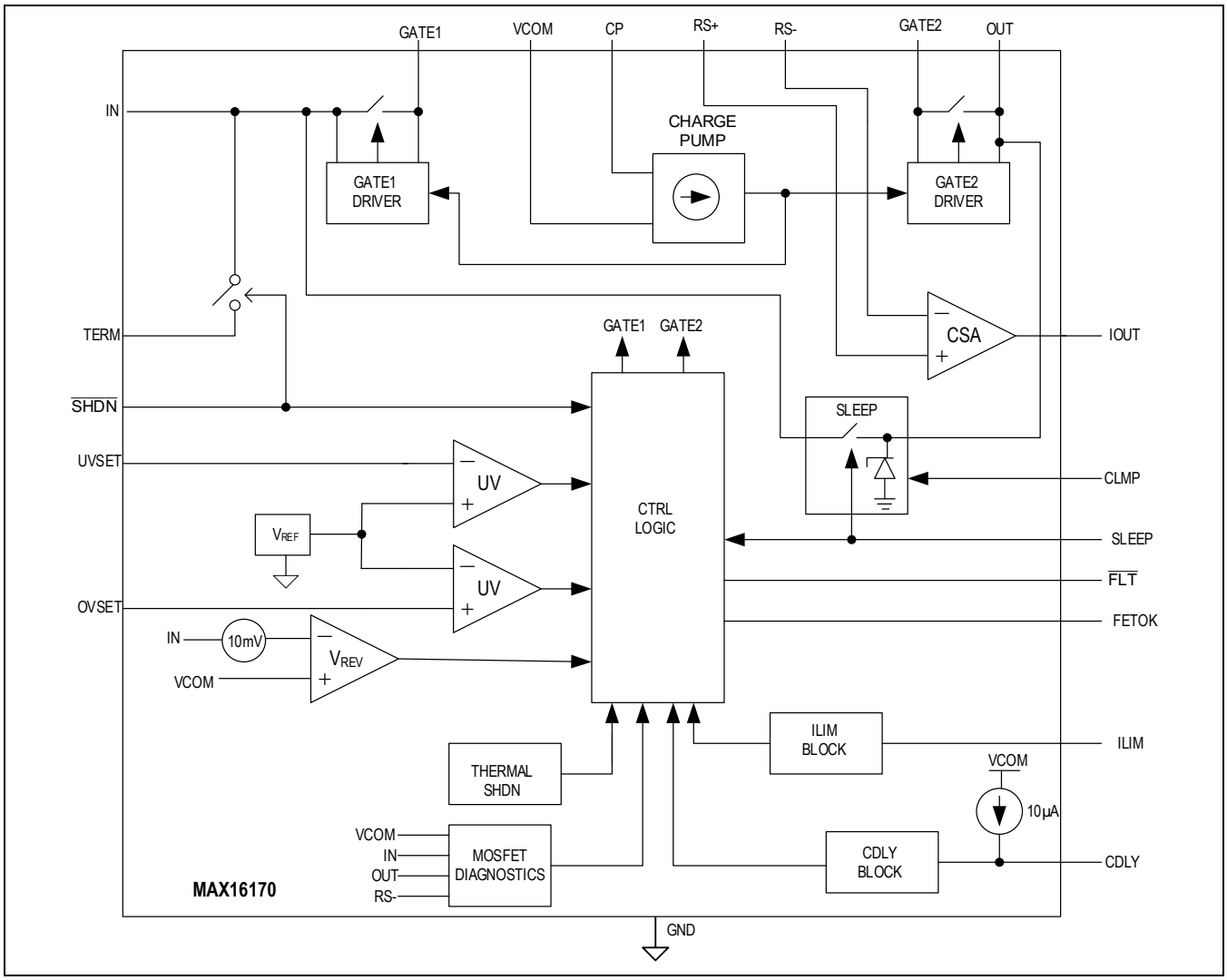


Pin Descriptions

PIN	NAME	FUNCTION
1	TERM	UVSET/OVSET Voltage-Divider Termination Output. TERM is internally connected to IN through a switch. Connect TERM to the UVSET/OVSET resistive-divider network for undervoltage and overvoltage threshold settings. TERM disconnects from IN when $\overline{SHDN}$ is forced low.
2	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ low to disable GATE1 and GATE2 and drive $\overline{FLT}$ low. Connect to IN for normal operation.
3	UVSET	Undervoltage Threshold Set Input. Connect a resistive divider from TERM to UVSET and GND to set the undervoltage threshold.
4	OVSET	Overvoltage Threshold Set Input. Connect a resistive divider from TERM to OVSET and GND to set the overvoltage threshold.
5	GND	Ground.
6	ILIM	Overcurrent Protection Threshold Setting Input. Connect a resistor from ILIM to ground to set the overcurrent threshold voltage. See *Table 1* for threshold options.
7	CLMP	Sleep Mode Clamp Voltage Set Input. Drive CLMP high to enable the internal clamp for 12V systems. Drive CLMP low to enable the internal clamp for 24V systems. See *Electrical Characteristics* table for clamp voltage range.
8	SLEEP	Active-High Sleep Mode Input. Drive Sleep high to place the MAX16170 in sleep mode. Drive SLEEP low to disable sleep mode. See *Sleep Mode* section for more details.
9	CDLY	OCP Comparator Delay Set Input. Connect a ceramic capacitor from CDLY to ground to adjust timing filter of the overcurrent fault condition caused by the superimposed AC signal on V_{IN}.

10	$\overline{FLT}$	Active-Low, Open-Drain Fault Output. $\overline{FLT}$ requires a pull-up resistor.
11	FETOK	Active-High, Open-Drain Output. FETOK pulls low when power MOSFETs are damaged. See *MOSFET Diagnostics* section for more details.
12	IOUT	Current-Sense Amplifier Output. Connect a resistor to set the output voltage. See *Electrical Characteristics* table for more details.
13	OUT	Output. Connect to the source of the second MOSFET, Q2.
14	GATE2	Load Disconnect Gate Driver. GATE2 is charged with respect to OUT by the internal charge pump. GATE2 shorts to OUT during overvoltage, overcurrent, thermal shutdown and when $\overline{SHDN}$ is pulled low.
15	RS−	Sense Resistor Low-Side Connection. RS− internally connects to the negative input of OCP comparator and negative input of the CSA.
16	RS+	Sense Resistor High-Side Connection. RS+ connects to the positive input of the internal CSA through an external resistor.
17	VCOM	Supply Voltage Input. Bypass VCOM to ground with 0.1µF ceramic capacitor. VCOM is also positive input of the OCP comparator.
18	CP	Charge Pump Output. Connect a 0.1µF to 1.0µF capacitor from CP to VCOM to proper operation.
19	GATE1	Ideal Diode Gate Voltage. GATE1 is shorted to IN when IN falls below the OUT by 10mV or $\overline{SHDN}$ is pulled low.
20	IN	TERM Switch Supply Input. IN is connected to the drain of the internal TERM switch.
-	EP	Exposed Pad. Connect EP to a contiguous ground plane for improved power dissipation.

Functional Diagrams



Detailed Description

The MAX16170 is an ideal diode controller that drives two back-to-back MOSFETs in common-drain configuration. The MAX16170's minimum start-up supply voltage is 4V. During normal operation, the device operates over the 3V to 65V supply voltage range. The wide operating voltage supports electronic control units (ECUs) designed for 12V and 24V car batteries. The input tolerates voltage transients in the range of −42V to 76V. The MAX16170 protects automotive and industrial systems against multiple fault conditions such as input overvoltage/undervoltage, reverse-current, overcurrent, and thermal fault conditions. Upon the detection of a fault condition, the open-drain, active low fault output ($\overline{FLT}$) pulls low to alert the system.

A user-adjustable window-voltage detector provides the flexibility to program the undervoltage and overvoltage thresholds at the input based on the system's requirement. A low-voltage input or ILIM offers the flexibility to change the sense voltage across the sense resistor (R_{SENSE}) through the low-cost, 5% tolerance resistors (R_{ILIM}). A CDLY-based timing offers the flexibility to program the delay time of overcurrent response. The MAX16170 offers 30kHz active rectification at the input to minimize power loss in the external power MOSFET and ensures that automotive systems achieve compliance during battery compliance tests. In the event of short input interruption (microcut) or overvoltage fault condition, the MAX16170 monitors the output voltage. Depending on the output voltage droop, this technique allows the device to enable GATE2 either in fast mode or slow mode. See the *Output Sensing* section for more detail.

Supply Voltage

VCOM is the supply input that powers the internal circuitry of the MAX16170. Bypass VCOM to ground with at least 0.1µF ceramic capacitor for proper operation. For normal operation, connect VCOM to the node where drains of the external MOSFETs are connected. When VCOM is provided and exceeds the maximum operation range 67V (typ), the chip enters shutdown.

Shutdown Input ($\overline{SHDN}$)

In shutdown mode, the supply current of the MAX16170 reduces to 5µA (max). During shutdown mode, the charge pump is disabled, and the TERM switch is turned off to eliminate the leakage current in the external OVSET/UVSET resistive divider. Drive $\overline{SHDN}$ low to place the MAX16170 into shutdown mode. Connect $\overline{SHDN}$ to IN or pull $\overline{SHDN}$ high for normal operation. Pulling $\overline{SHDN}$ high reduces the input voltage range that is still limited by the "IN to $\overline{SHDN}$" absolute maximum rating.

Undervoltage and Overvoltage Protection

The MAX16170 monitors the input voltage for undervoltage and overvoltage faults. An external resistive divider connected between TERM, OVSET, UVSET, and GND sets the UV and OV thresholds. (TERM is connected to IN through a switch when $\overline{SHDN}$ is high.)

When the input voltage falls below the undervoltage threshold V_{UVTH}, the MAX16170 pulls GATE1 and GATE2 low, turning off the external MOSFETs and $\overline{FLT}$ asserts, and sometime the retry mode is activated. After a retry delay, the input voltage rises above the undervoltage threshold $V_{UVTH+HYS}$, and GATE1 and GATE2 go high to turn on the MOSFETs.

When the input voltage rises above the overvoltage threshold V_{OVTH}, the MAX16170 pulls GATE2 low, turning off the external MOSFET, and $\overline{FLT}$ asserts. When the input voltage falls below the overvoltage threshold $V_{UVTH-HYS}$, GATE2 goes high to turn on the MOSFET.

The input's UV and OV setting values (V_{UVTH} and V_{OVTH}) should be in the input normal operation range.

MOSFET Diagnostics

The MAX16170 offers MOSFET diagnostic feature that only detects the heath of the power MOSFET (Q1 and Q2) once during power-up and normal activation operation without any fault events. When both or any one of MOSFETs are in short-circuit fault, the device detects it and asserts FETOK low. FETOK also pulls low when the MOSFET (Q2) remains in open-circuit condition. The detection for open-circuit condition for the MOSFET(Q1) is different. *Figure 1* shows the FETOK behavior in absence of Q1.

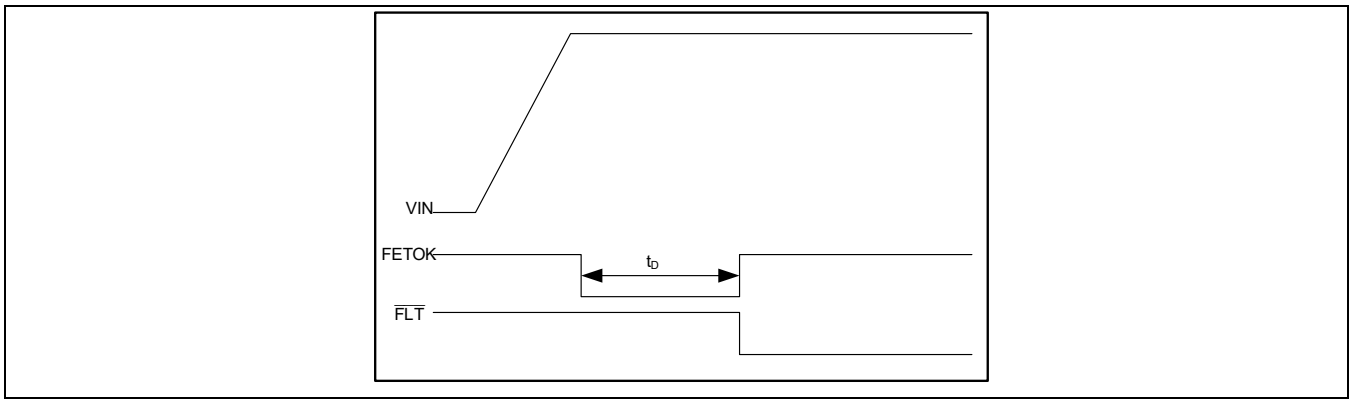


Figure 1. FETOK Operation with Q1

In the figure, FETOK pulls low after power-up event. FETOK remains low for t_D time period and then pulls high. The reason for FETOK pulling high is that initially an internal linear regulator powers up the FETOK and other circuitry. In the absence of Q1 and the presence of output load, linear regulator droops below its UVLO and causes $\overline{FLT}$ to pull low. The lighter the output load, the longer the duration of t_D.

Fault Output ($\overline{FLT}$)

The $\overline{FLT}$ asserts low in the events of overvoltage, undervoltage, overcurrent, short-circuit, thermal shutdown fault conditions, VCOM UVLO, shutdown mode, and sleep mode. $\overline{FLT}$ also pulls low when the Q1 remains in open-circuit condition that causes undervoltage lockout. $\overline{FLT}$ is an active-low open-drain output and requires a pull-up resistor. See *Absolute Maximum Ratings* section for proper pull-up voltage.

Sleep Mode

In sleep mode, the MAX16170 sources 1mA (min) of current to the load while consuming only 15uA. In sleep mode, the load is expected to be in standby mode of operation, not requiring a lot of power. To support standby operation, the MAX16170 disables the charge pump and uses a current mirror to deliver the required load current.The sleep mode circuit features integrated clamps. Pull SLEEP high to put the MAX16170 in sleep mode. In this mode, the charge pump remains disabled, and the quiescent current reduces to about 15µA. In addition, the MAX16170 features internal clamps that are enabled in sleep mode. The device offers two clamp voltage options that are set through CLMP. Pulling CLMP high enables the 24V (max) clamp voltage suitable for 12V systems. Pulling CLMP low enables the 48V (max) clamp voltage suitable for 24V systems. See *Figure 2* for details.

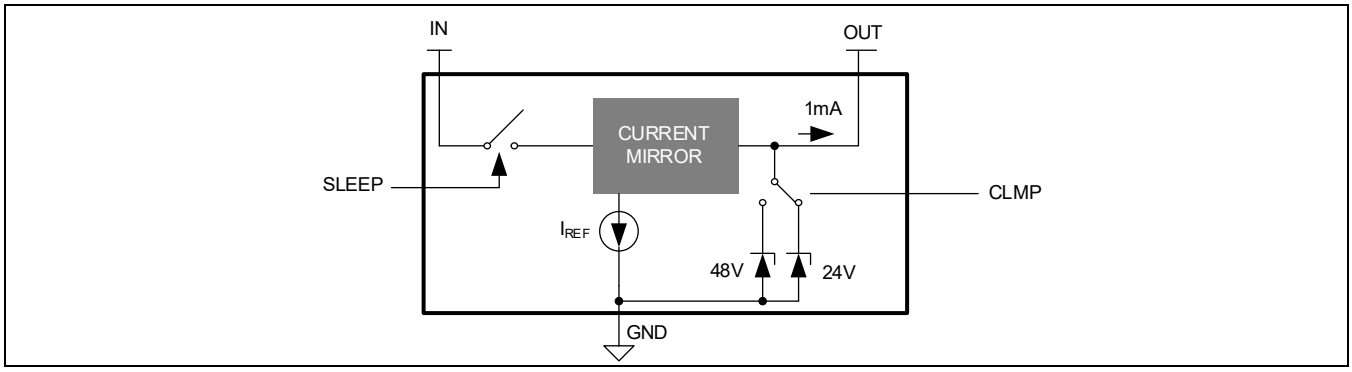


Figure 2. Sleep Mode Current Sourcing Topology

TERM Switch

The TERM switch helps eliminate leakage current in UVSET and OVSET resistive-divider network during shutdown mode. TERM switch is internally connected to IN and has a 400Ω (max) $R_{DS(ON)}$. Lower switch resistance improves UV and OV thresholds' accuracy. See *Figure 3*.

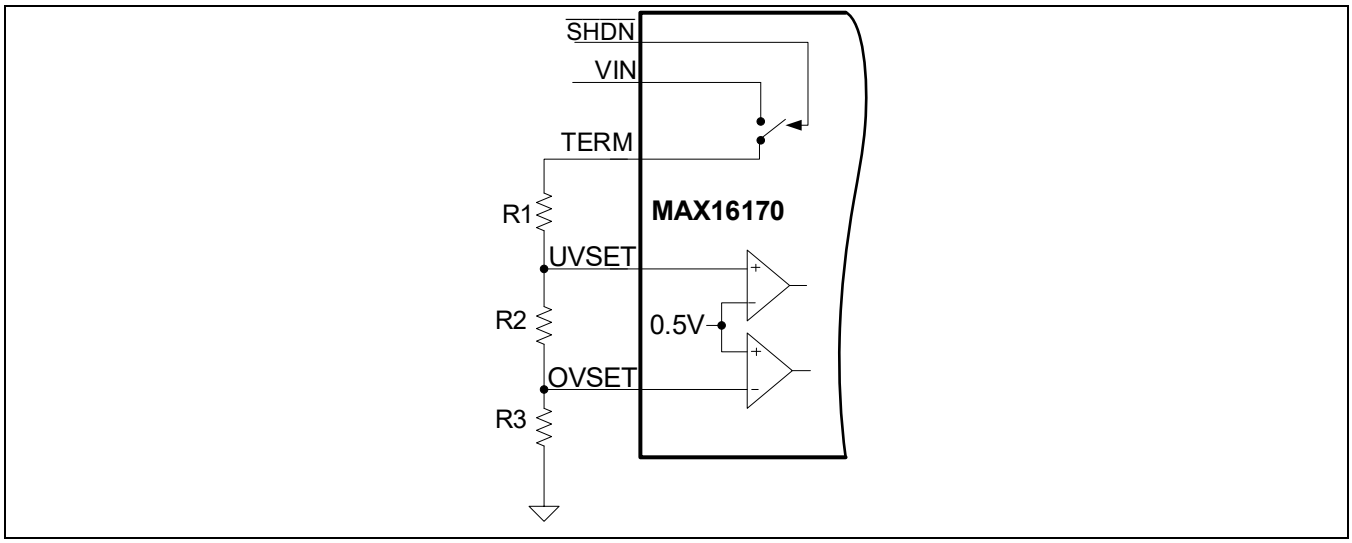


Figure 3. Term Switch

Charge Pump

The MAX16170 features an internal charge pump (CP) to drive the external N-channel MOSFETs. A minimum of 0.1µF reservoir between CP and VCOM is required to store the gate drive. Its charge current is 1.8mA (typ). After V_{VCOM} rises to its UVLO, the charge pump starts and charges C_{CP} capacitor to 10V in startup time. Once the C_{CP} voltage falls to 9V, the charge pump recharges C_{CP} recurrently. The charge pump is disabled in shutdown mode, sleep mode, and when V_{VCOM} exceeds the maximum operation range.

GATE1 Driver

In light load application, the MAX16170 controls the GATE1's voltage with respect to IN (V_{GS1}) to regulate the voltage drop across MOSFET, Q1 to 10mV (typ). In reverse current condition, the regulation scheme helps control the downward transition of GATE1 to prevent DC flow from load back into the battery. In addition, a fast-acting comparator shorts GATE1 to IN within 1µs (max) in the event of a reverse voltage fault condition, (V_{IN}−V_{OUT}) = −10mV. See the *Electrical Characteristics* table for more detail. For slow falling VIN, GATE1 remains on unless VIN falls below the undervoltage fault threshold set by the resistive divider network connected between TERM, OVSET, UVSET, and GND.

The MAX16170 features an internal resistor (2MΩ) between GATE1 and IN. This resistor ensures GATE1 is pulled to the input voltage when the battery voltage swings below ground and keeps the reverse protection MOSFET (Q1) in off state. See *Application Information* section for more detail.

GATE2 Driver

GATE2 controls the N-channel MOSFET, Q2. GATE2 disables to isolate the load when an overcurrent, undervoltage, overvoltage fault occurs. GATE2 remains on during reverse voltage/microcut fault conditions when $V_{OUT} > V_{OUT\_UVLO}$. See *Output Sensing* section for more detail on slow and fast rise times behavior of GATE2.

When the input voltage falls slowly and cannot cause reverse current, GATE2 remains on until the input voltage crosses the undervoltage fault threshold set by the resistive-divider network connected between TERM, OVSET, UVSET, and GND.

Current-Sense Amplifier

The MAX16170 current-sense amplifier operation is best understood as a specialized operational amplifier (op-amp) circuit with a p-channel MOSFET in the feedback path. The op amp forces a current through an external gain resistor at R_{RS+} (*Figure 4*), so that its voltage drop equals the voltage drop across the external sense resistor, R_{SENSE}, making the voltage at RS+ same as RS−.

The current through the R_{RS+} is sourced by the high-voltage p-channel FET into an external resistor (R_{IOUT}) at IOUT. This produces an output voltage whose magnitude is given by the following equations:

$$V_{SENSE} = I_{LOAD} \times R_{SENSE}$$
$$V_{IOUT} = \frac{V_{SENSE}}{R_{RS+}} \times R_{IOUT}$$

Here, the $\frac{V_{SENSE}}{R_{RS+}}$ is equal to the input current of CSA into R_{RS+}.

The gain accuracy is primarily determined by internal current-sense amplifier and the matching of the two gain resistors, R_{RS+} and R_{IOUT}.

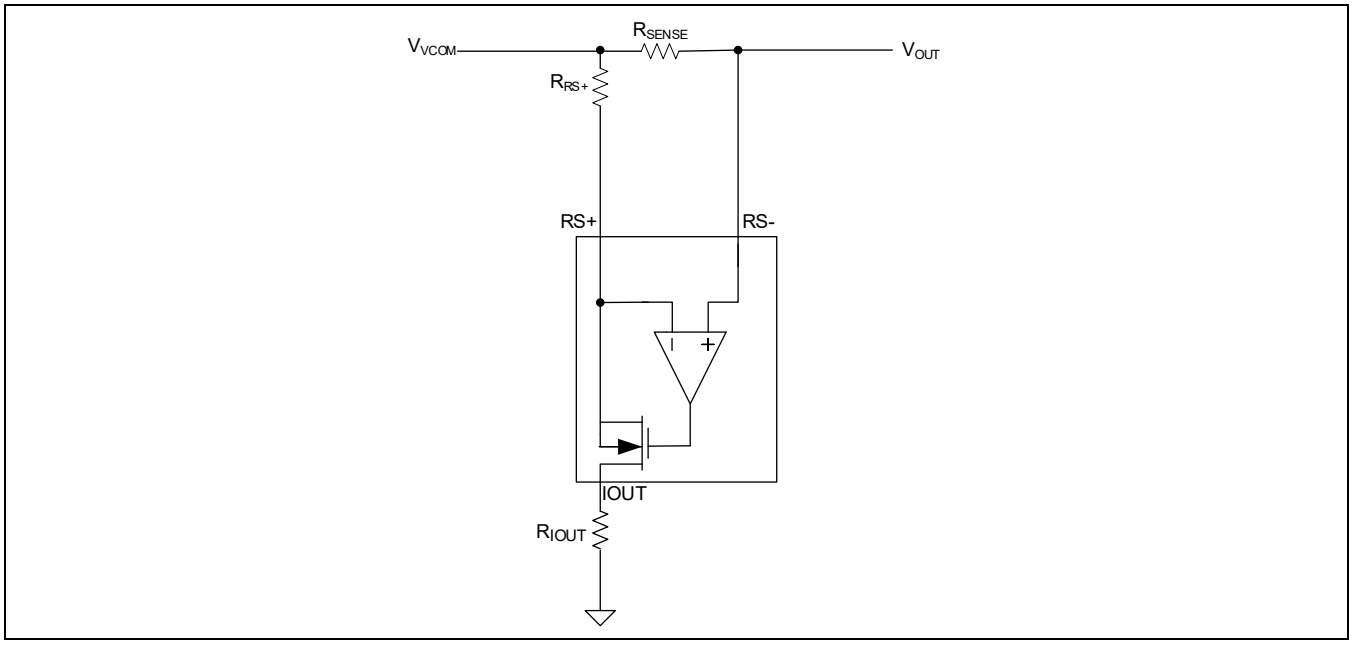


Figure 4. CSA Simplified Block Diagram

Programmable Overcurrent Protection

The MAX16170 detects an overcurrent fault condition by using the sense resistor between VCOM and RS−. Connect a resistor R_{ILIM} to set the overcurrent thresholds in *Table 1*. See *Figure 5* for the simplified internal diagram. Shorting ILIM to ground disables the overcurrent protection function.

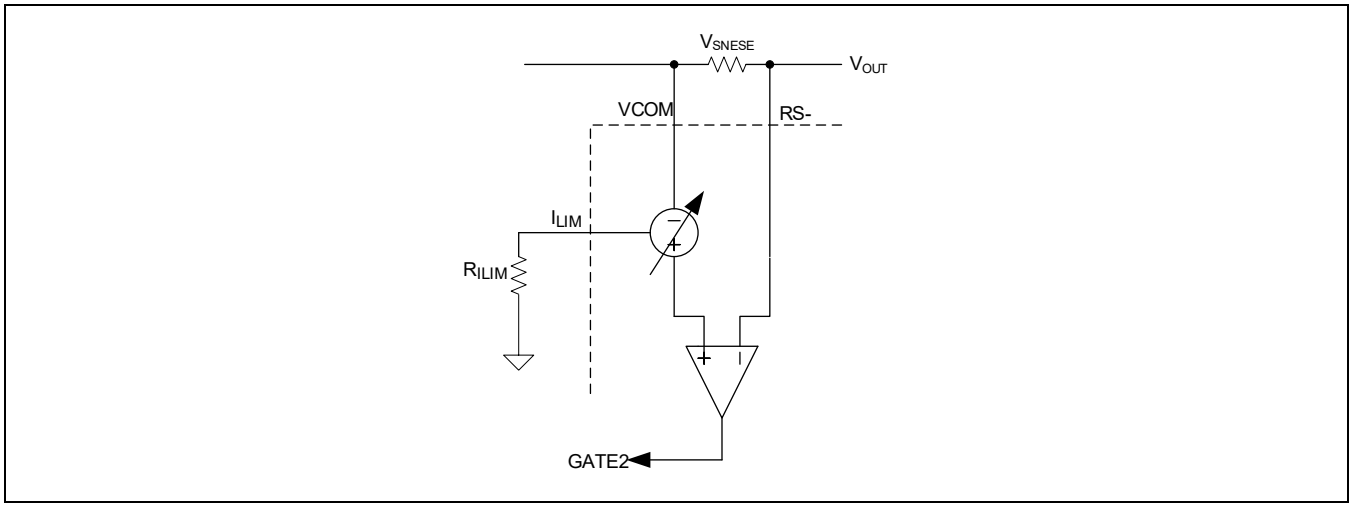
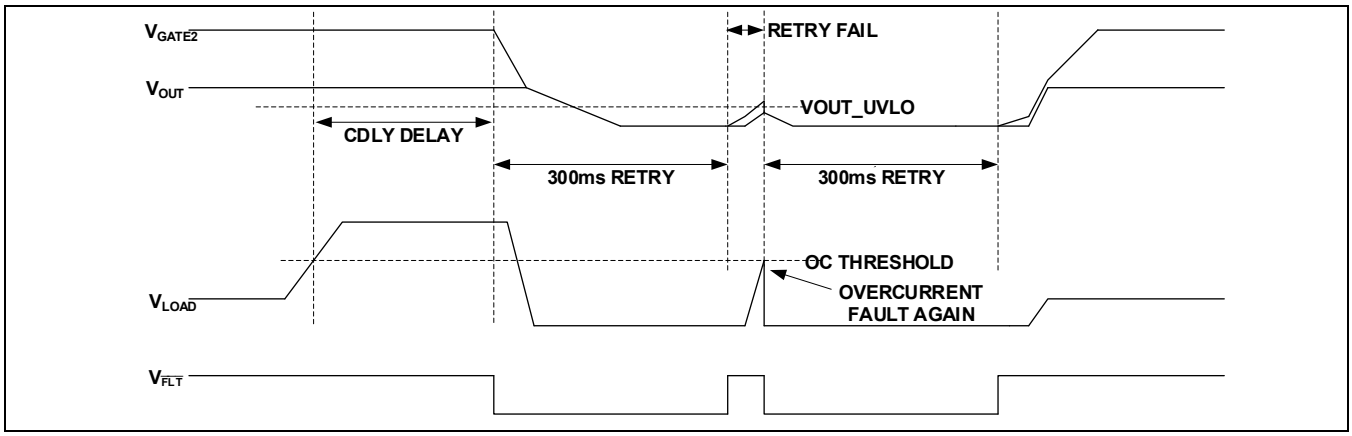


Figure 5. Simplified OCP Internal Block Diagram

Table 1. Sense Voltage Options

RILIM (kΩ)	V_{SENSE} (mV)
10	20
20	30
30	40
40	50
Short	Disabled

When the load current makes the voltage on sensor resistor to exceed the threshold, the MAX16170 drives GATE2 low and isolates the output load. During the overcurrent fault condition, the MAX16170 enters 300ms (typ) auto-retry mode and $\overline{FLT}$ stays asserted. Upon the termination of an overcurrent fault condition, the MAX16170 pulls GATE2 high and allows $\overline{FLT}$ to de-assert.



When the overcurrent fault is removed, GATE2 is enabled with a slew rate determined by the RC network connected from GATE2 to ground. See *In-Rush Current Control* section for more details.

Overcurrent Protection Delay

The overcurrent protection responds immediately or with a programmable delay after the overcurrent protection is triggered, which depends on the C_{CDLY} capacitor and V_{OUT} voltage. When the V_{OUT} is maintained higher than VOUT_UVLO level, the CDLY-based timing is activated and decides the delay time. Using the following equation, the delay time could be calculated:

$$t_{DELAY\_RESPONSE} = C_{CDLY} \times \frac{1V}{10\mu A}$$

Where the C_{CDLY} is the capacitor connected from CDLY to ground, 1V is the charging threshold of the capacitor CDLY and 10uA is the charge current. Once the VOUT droops to the VOUT_UVLO level, the CDLY-based timing breaks off and the MAX16170 disables GATE2 to isolate the load immediately. As long as VOUT remains below the VOUT_UVLO voltage, the part remains in auto-retry mode.

When there is a superimposed AC voltage at the input, the overcurrent fault could trigger depending on the AC frequency, overcurrent threshold setting, and the output capacitor. To avoid interruption during normal operation with superimposed AC at the input, the CDLY-based timing is in use to bypass the overcurrent fault.

AC Rectification

The MAX16170 offers AC input rectification of up to 30kHz TYP. The AC rectification capability reduces power dissipation into the external MOSFETs and helps facilitate system-level testing. See *Figure 6*.

When V_{IN} < V_{COM} + 10mV, the GATE1 pin is driven low and reduces external MOS's conduction until the V_{IN} is 10mV higher than the V_{COM}, this is the regulation operation. When V_{IN} < V_{COM} −10mV, the GATE1 pin is shorted to SRC fast through a small resistance to turn MOS off, this is the reverse protection, and when VIN > VDRN + 30mV, the GATE2 pin

is driven to highest as CP voltage to turn MOS on fully until VIN is not 30mV higher than VCOM, and then the MAX16170 is back to regulation operation. When the VIN is an AC wave input, the MAX16170 works alternately between these three modes and achieve the active rectifier function. During AC rectification, the GATE2 pin remains high as long as no other faults are triggered, and $\overline{SHDN}$ is always high.

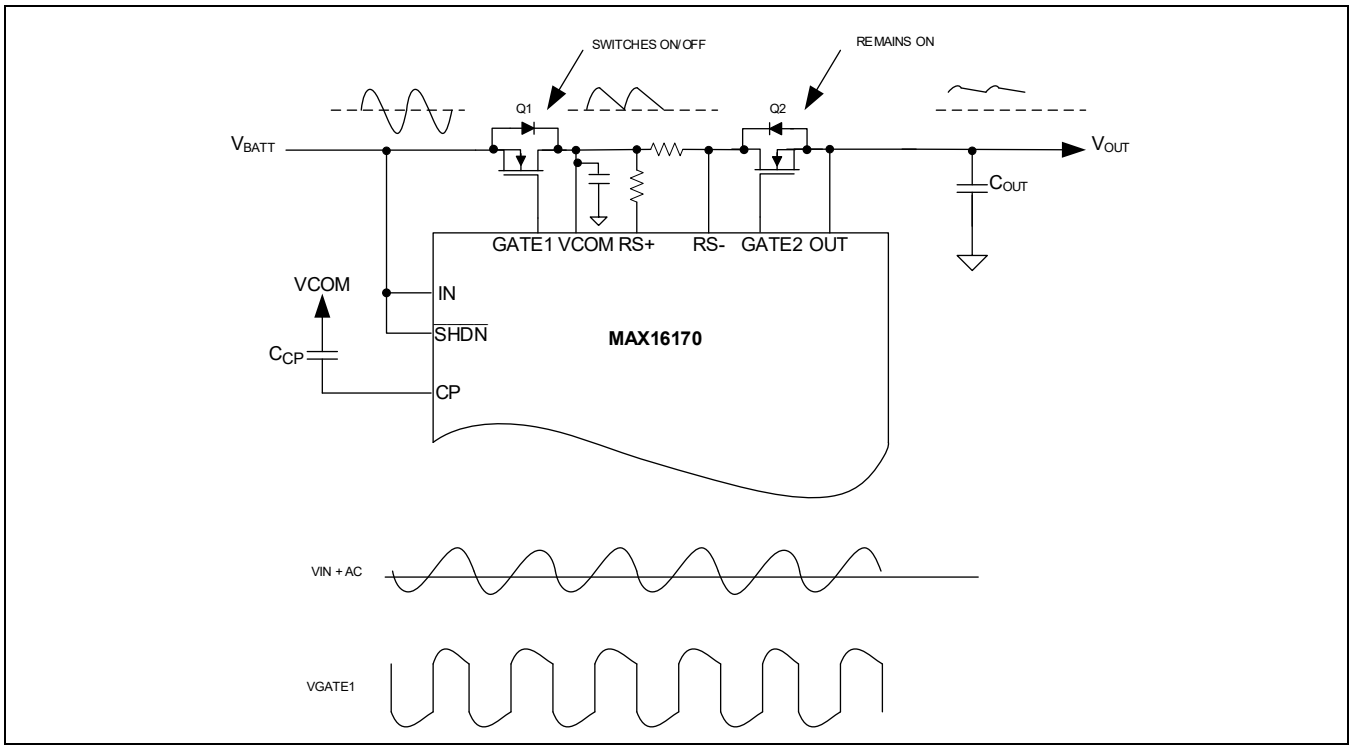
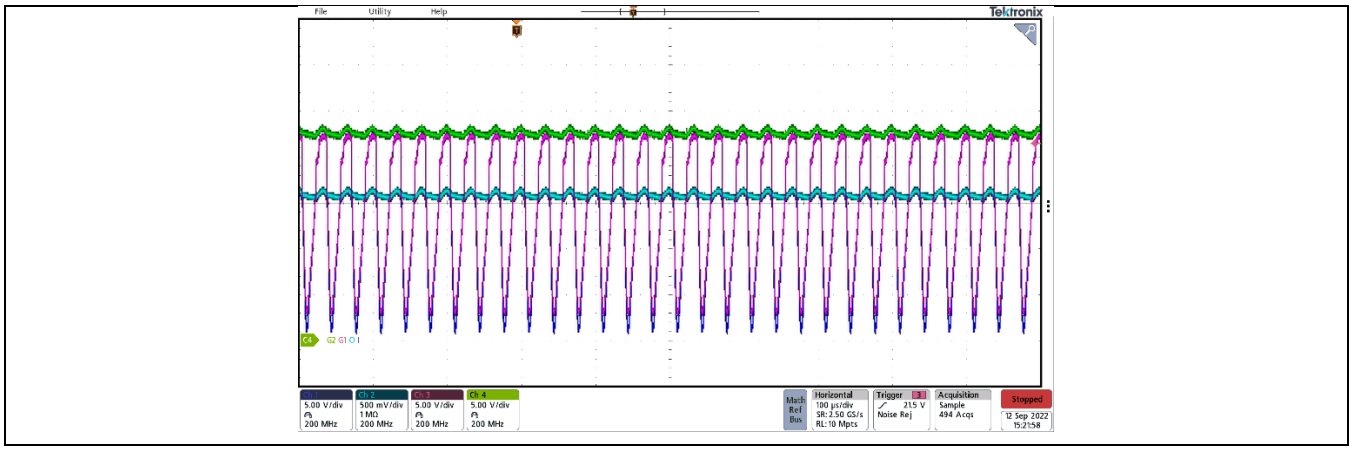


Figure 6. Input AC Rectification Behavior



MOS Type: ON semi NVD6824, load current: 2A, Output capacitor: 100µF

In-Rush Current Control

To help control the in-rush current during power-up, an RC network can be connected from GATE2 to ground. Use the following equation to calculate the desired in-rush current.

$$I_{IN\_RUSH} = \frac{C_{OUT}}{C_{GATE2}} X\ (I_{GATE2})$$

Where C_{OUT} is the output capacitor connected to output of the MAX16170, C_{GATE2} is the capacitor in the RC network connected from GATE2 and GND, and I_{GATE2} is GATE2's source current (TYP 25µA). The R_{GATE2} helps minimize turn-off delay during fault conditions. See *Figure 7* for more details.

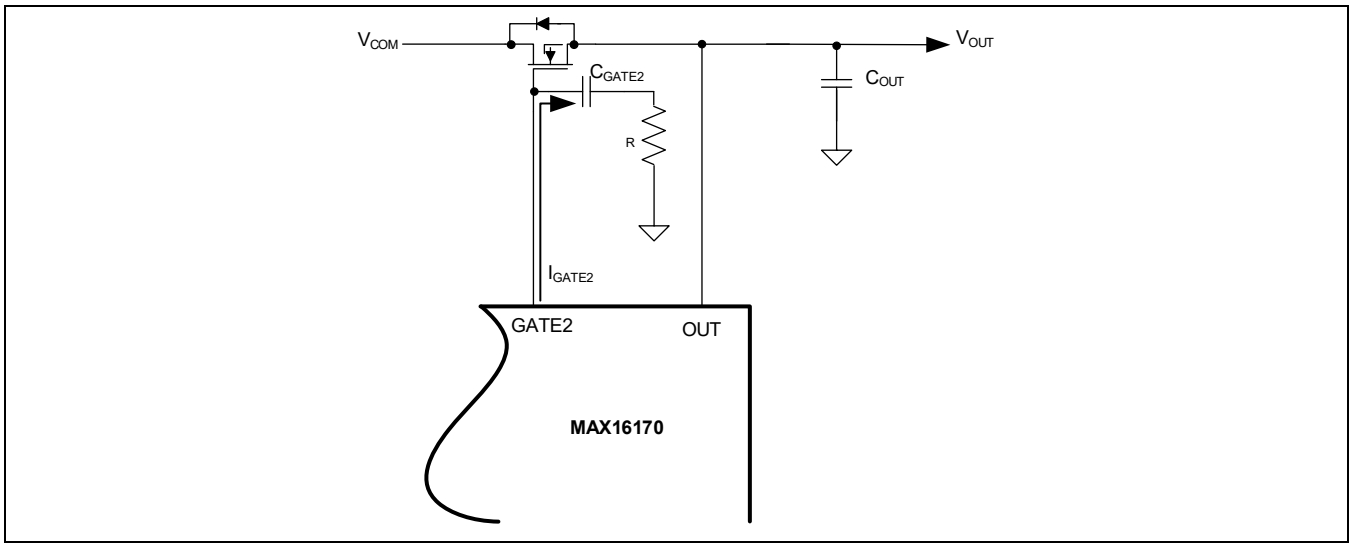


Figure 7. In-Rush Current Control

Output Sensing

In reverse voltage conditions, GATE1 disables with 1µs while GATE2 remains enabled (see *Figure 8*). Upon input voltage recovery from reverse voltage condition, if $V_{OUT} > V_{OUT\_UVLO}$, GATE1 ramps up quickly and the MAX16170 activates a ~400µs blanking time to quickly charge the output capacitor without triggering the OCP. If $V_{OUT} < V_{OUT\_UVLO}$, GATE2 rises in soft-start mode. See *Figure 9*. GATE2's soft-start ramp-up rate is set by the value of the in-rush current control capacitor connected between GATE2 and GND. See *In-Rush Current Control* section for more details.

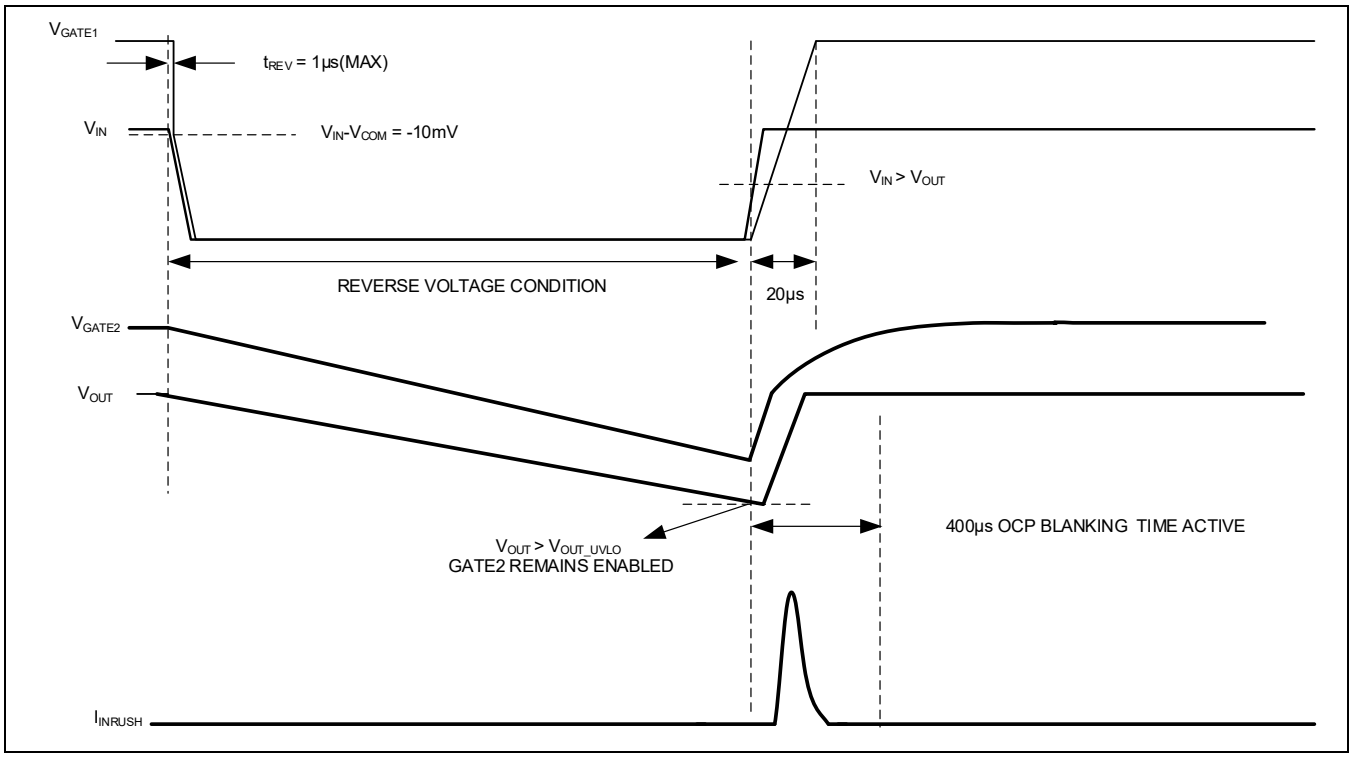


Figure 8. GATE Fast-Mode Recovery

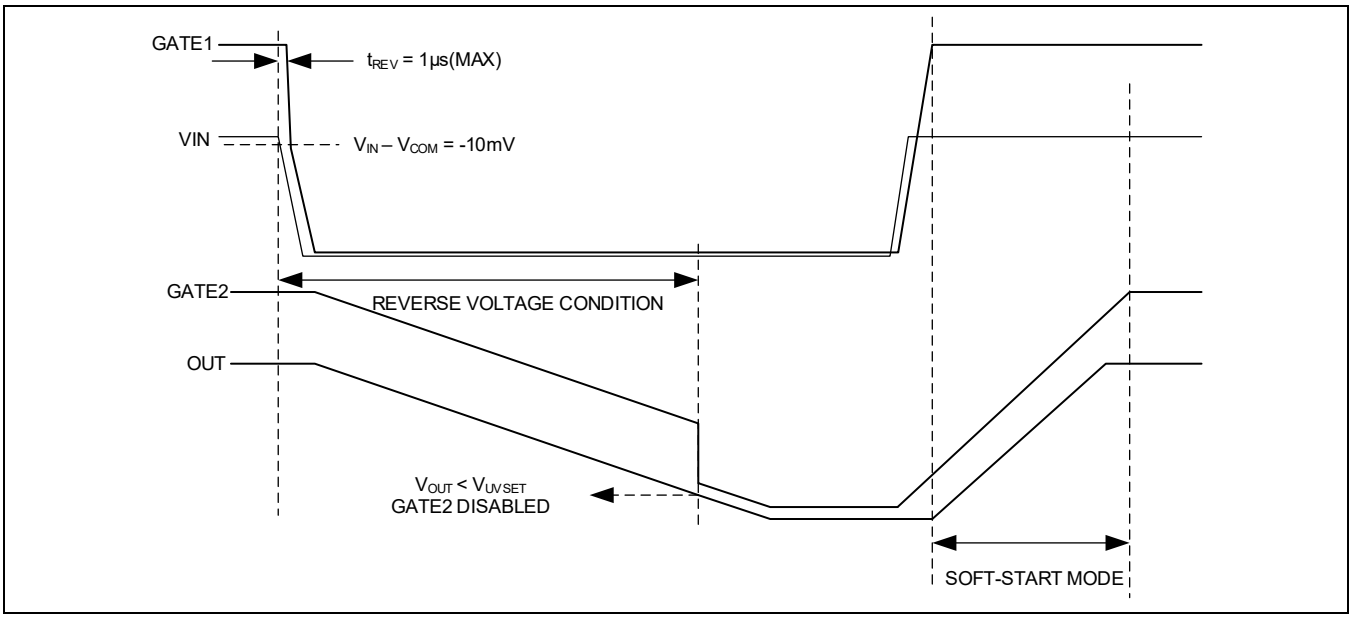


Figure 9. GATE2 Soft-Start Mode

Note: During GATE2 soft-start mode, the OC is active.

Overvoltage Fault

When the input voltage exceeds the input overvoltage fault threshold, GATE2 disables while GATE1 remains enabled. See *Figure 10*. During overvoltage fault condition, the output provides energy to the system. Upon recovery from overvoltage fault condition, if $V_{OUT} > V_{OUT\_UVLO}$, GATE2 ramps up in fast mode (20µs typ) to charge the output capacitor and the MAX16170 activates a 400µs blanking time to not trigger the OCP. If $V_{OUT} < V_{OUT\_UVLO}$, GATE2 rises in soft-start mode. See *Figure 11*. GATE2's soft-start ramp-up rate is set by the value of the in-rush current control capacitor connected between GATE2 and GND. See *In-Rush Current Control* section for more details.

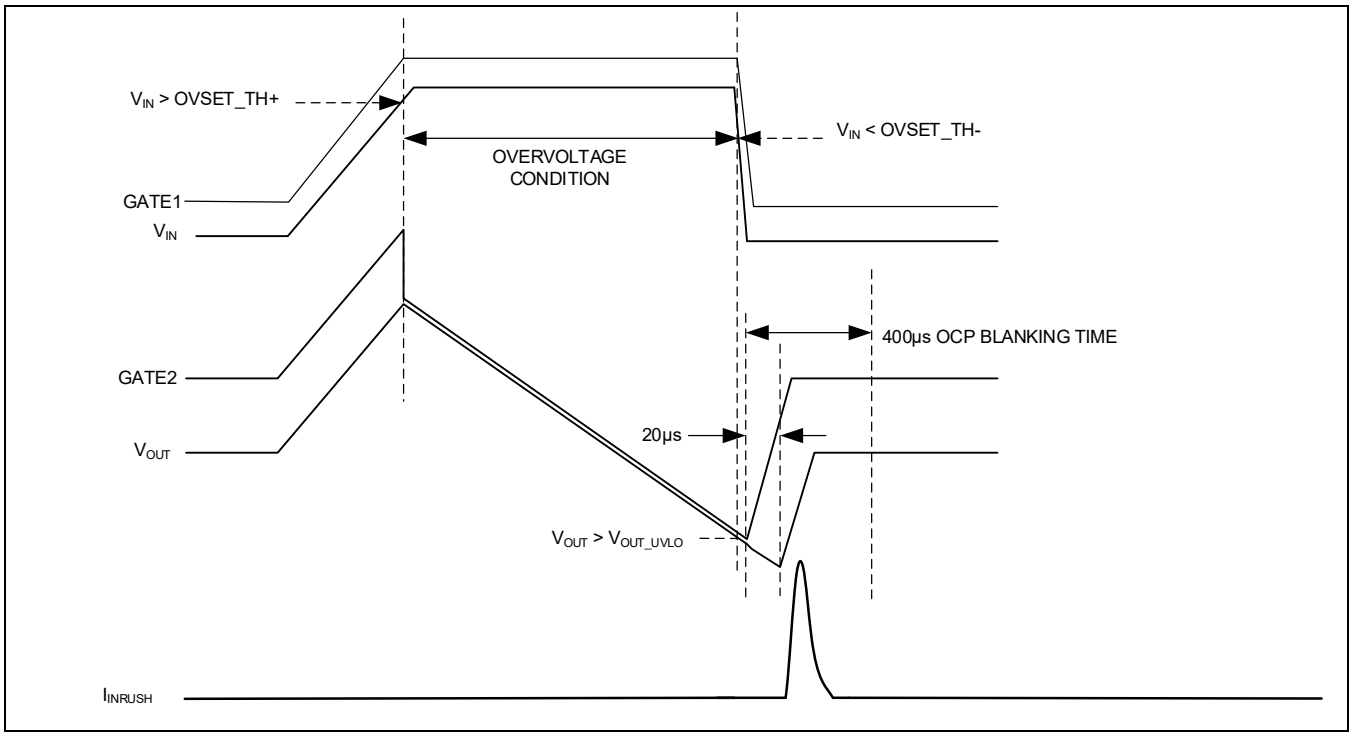


Figure 10. GATE2 Fast-Mode Recovery

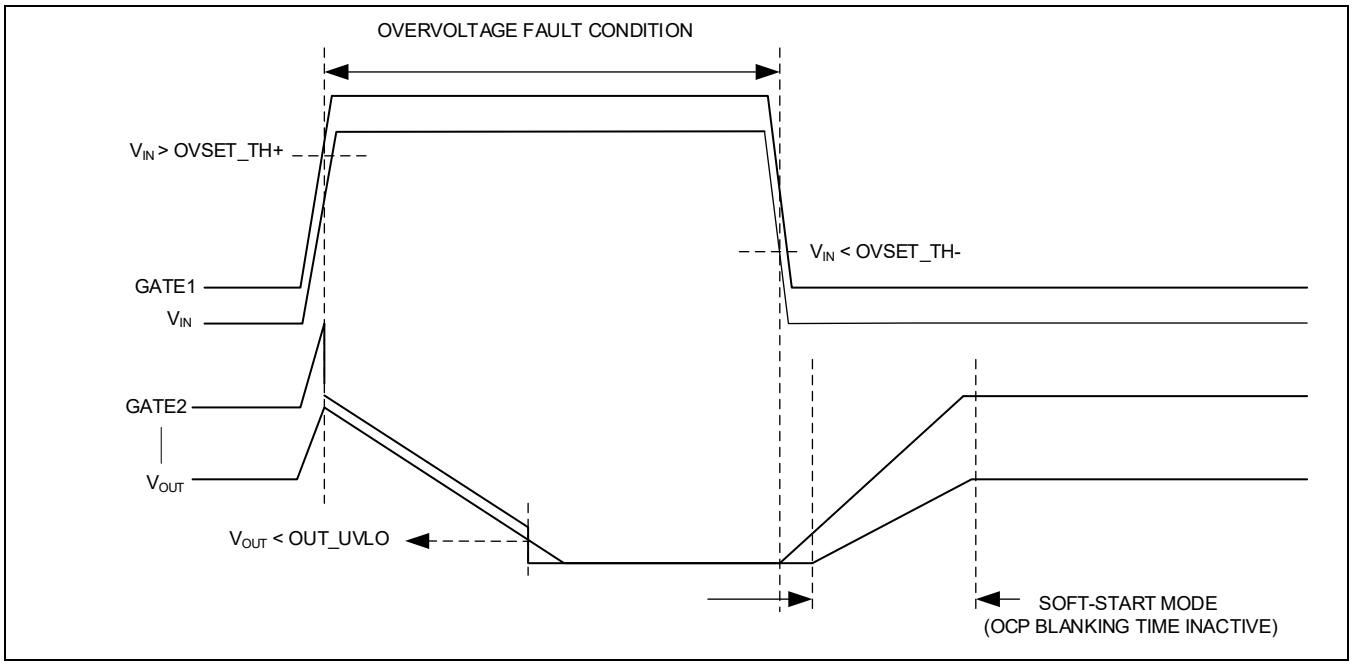


Figure 11. GATE2 Soft-Start Ramp-Up Mode

Note: During GATE2 soft-start mode, the OC is active.

Auto-Retry

The MAX16170 features a 300ms auto-retry timeout during OCP, UV, and thermal fault. *Figure 12* shows the input voltage very close to UV threshold, droops below UV threshold due to IR losses in the long cable routing and load current and disables both gate drivers. The sudden and complete isolation of the load from the source allows the input voltage rise-up but the gate drives are enabled 300ms later, otherwise UV protection is triggered frequently and MOSFETs may get heat. This 300ms auto-retry timeout helps operate the MOSFETs much cooler which would otherwise cause thermal and system reliability issues.

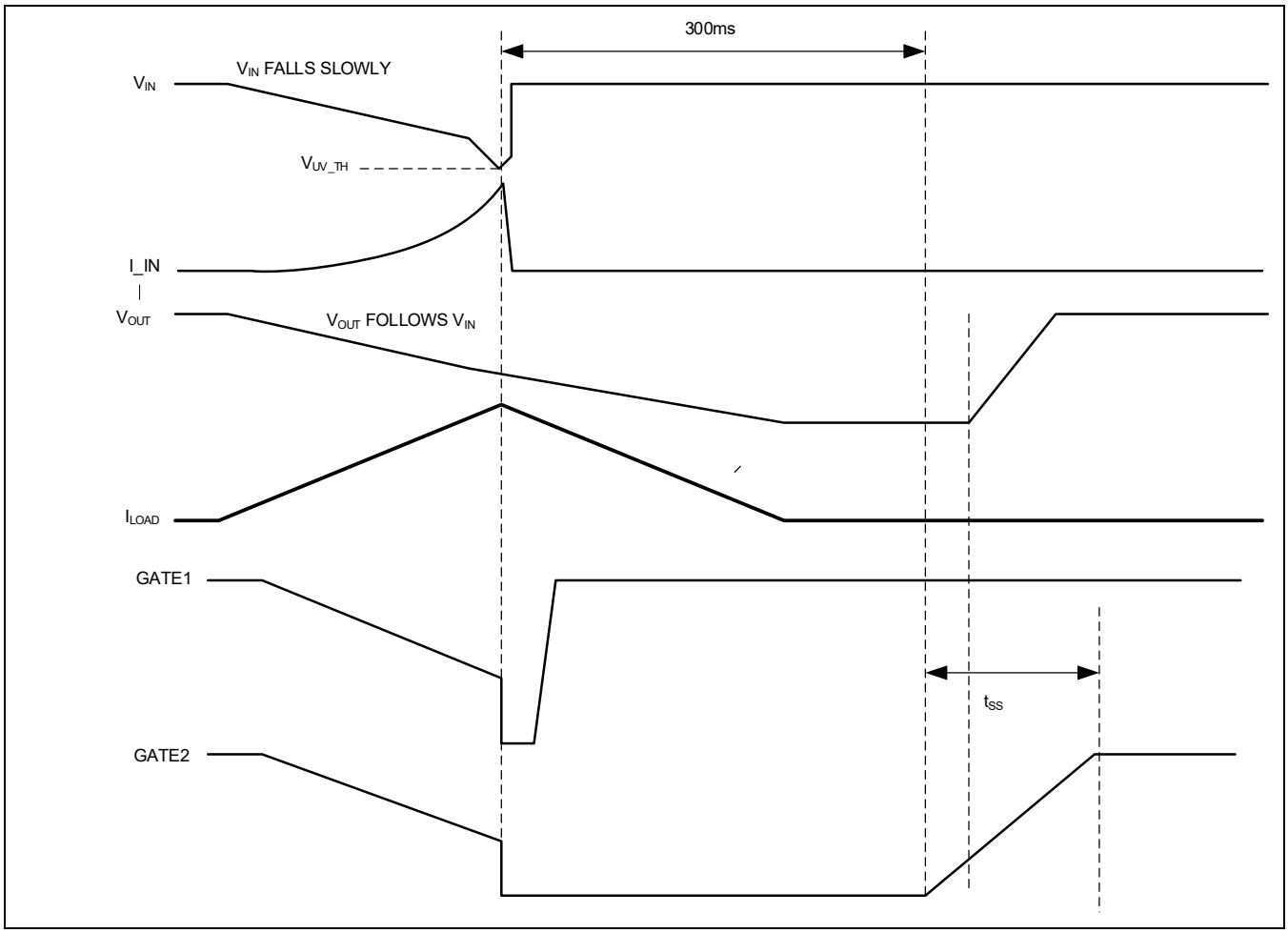


Figure 12. Undervoltage Fault Auto-Retry Timeout

Applications Information

Input Transient Protection

The MAX16170 can withstand voltage transients. The protection range extends from −42V to +76V. The wide range relaxes TVS requirement that might be needed for systems designed to comply with ISO 7637 and ISO 16750 requirements.

Protection Against Negative Input Transients

During negative input transients or reverse battery terminal connection, it is important to keep the reverse voltage MOSFET (Q1) in off state to keep the load circuit isolated from damaging negative input transients. To achieve that, the MAX16170 features an internal 2MΩ between GATE1 and IN. This 2MΩ resistor ensures Q1 remains off by pulling the GATE1 to the input voltage. To verify proper functionality of GATE1 when the input voltage transitions below ground, it is recommended to use an FET probe as it offers higher input impedance than passive probes. Using passive probes create a voltage divider between GND, GATE1, and IN which depending on the negative input excursion, could exceed the threshold of Q1 and keep it in the on state. See *Figure 13* for circuit details.

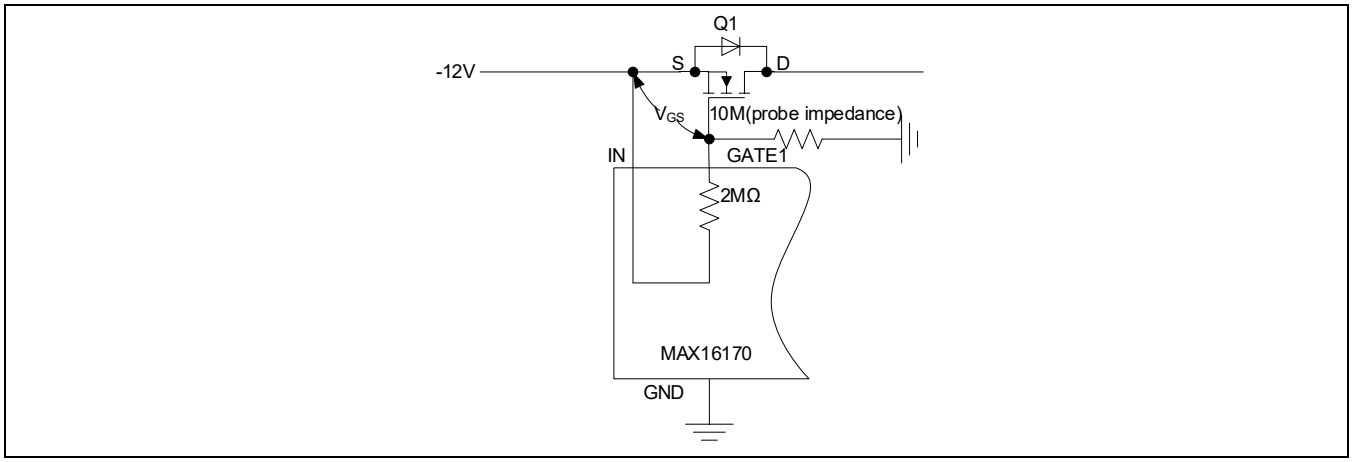


Figure 13. Passive Probe Resistive-Divider Network

Setting Overvoltage/Undervoltage Threshold

The MAX16170 features window-detection threshold comparators. The noninverting input of the undervoltage comparator shares the same reference voltage connected to the inverting input of the overvoltage comparator. This configuration allows using a three-resistor divider to set both undervoltage and overvoltage thresholds. The top of the resistive-divider network connects to TERM. See *Figure 3*. When the input voltage falls outside the set window threshold, the gate voltage is disabled and the N-channel MOSFETs are turned off. Use the following equations to set the thresholds:

$$V_{UVTH} = V_{TH}\left[\frac{R_{TOTAL}}{R2+R3}\right] \text{ and } V_{OVTH} = V_{TH}\left[\frac{R_{TOTAL}}{R3}\right]$$

where V_{UVTH} and V_{OVTH} are the undervoltage and overvoltage thresholds, respectively, R_{TOTAL} = R1 + R2 + R3 + R_{TERM}, V_{TH} is the 0.5V OVSET and UVSET threshold, and the V_{TH_HYS} is the hysteresis, R_{TERM} is the TERM on-resistance between IN and TERM pins whose typical value is 0.15kΩ.

The overvoltage and undervoltage threshold hysteresis is calculated as follows:

$$V_{UVTH} = V_{TH}(1 + V_{TH\_HYS})\ X\ \left[\frac{R_{TOTAL}}{R2+R3}\right] \text{ and } V_{OVTH} = V_{TH}(1 - V_{TH\_HYS})\ X\ \left[\frac{R_{TOTAL}}{R3}\right]$$

Where the V_{TH_HYS} is the hysteresis percentage.

ORing

Some applications require oring/redundant power supplies to support uninterrupted system operations. *Figure 14* below shows an ORing application with two MAX16170s operating in parallel.

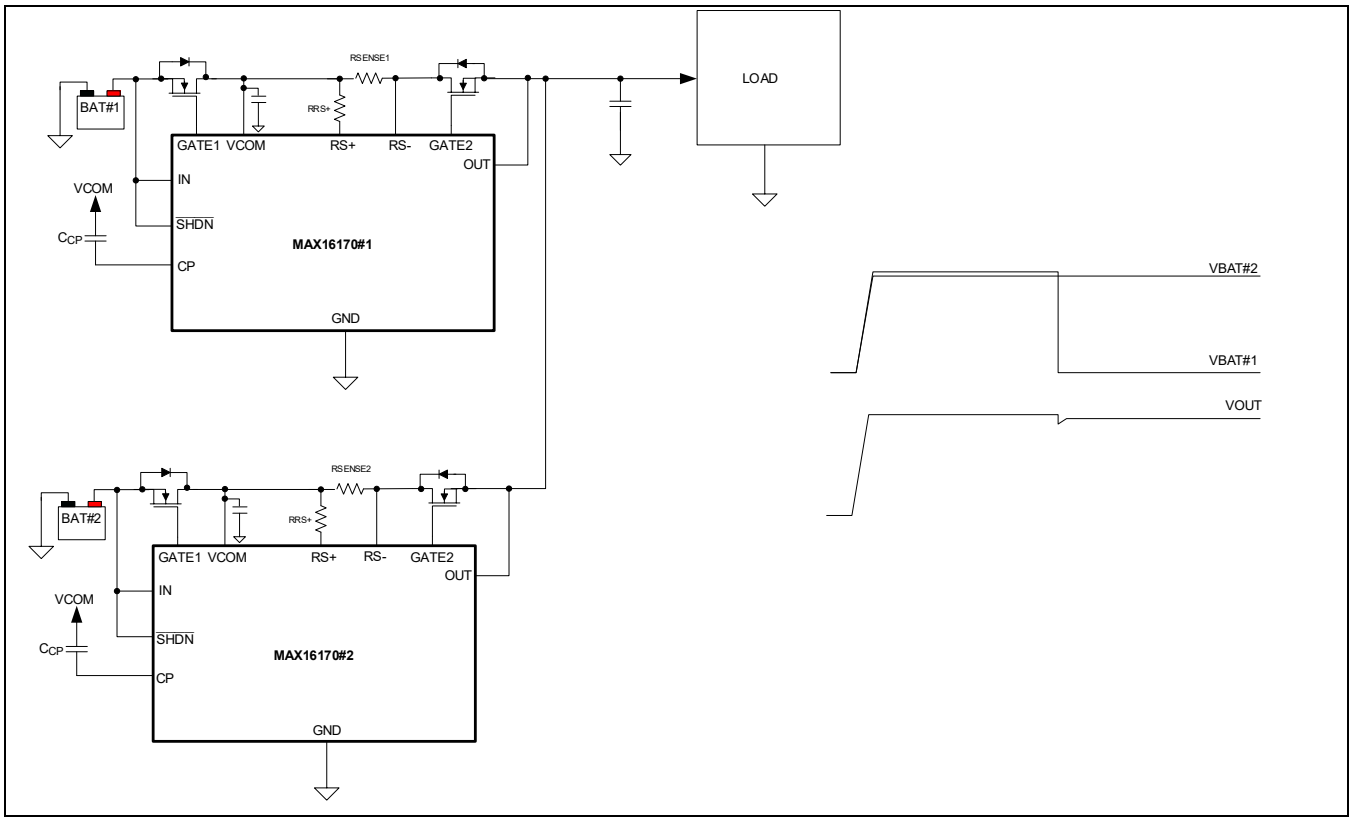


Figure 14. ORing Application

In *Figure 14*, the power supply with the higher output delivers all or most of the load current. If the power source, BAT#1, shorts to ground, the MAX16170#1 senses the reverse current flow from system output and blocks the reverse current flow within 300ns (typ) while the other power source, BAT#2, immediately takes over and delivers the required load current.

Layout Recommendations

To optimize device operation, use the following recommendations:

1. Bypass the VCOM to ground with a capacitor connected as close as possible between the VCOM pin and ground.
2. Connect GATE1/GATE2 to the gates of the external MOSFET directly with as few traces and vias as possible.
3. Connect the exposed pad to the ground pin of the IC and do not use the exposed pad as the only ground connection.
4. For high-current applications, minimize IR losses and heat dissipation by mounting the appropriate heat sink, air flow, and low-resistance traces.
5. Due to the high currents that may flow through R_{SENSE}, take care to eliminate solder and parasitic trace resistance from causing errors in the sense voltage. Either use a four-terminal current-sense resistor or use Kelvin (force and sense) PCB layout techniques. *Figure 15* shows a typical routing of Kelvin-sensed traces to RS+ and RS− pins. The Kelvin sense traces should be as close as possible to the current-sense resistor's solder contact pads.

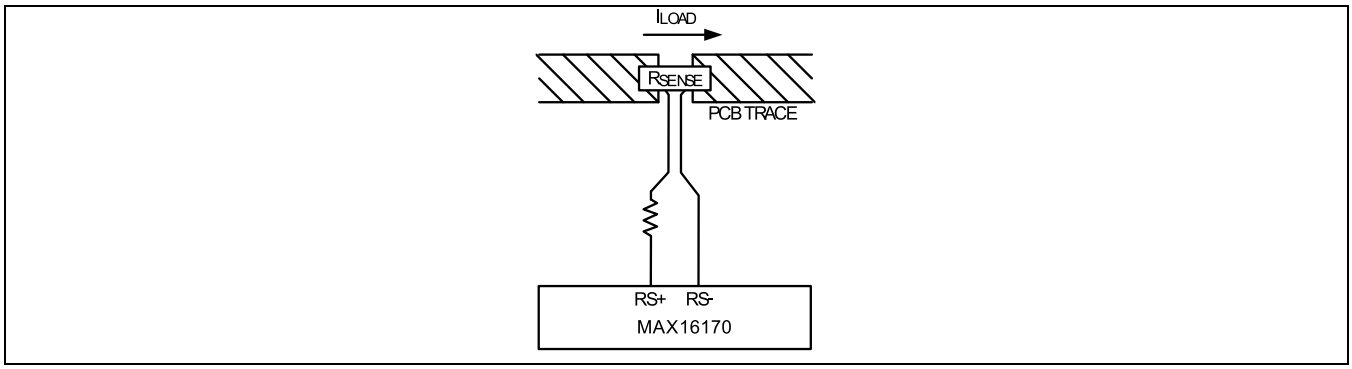


Figure 15. Kelvin Sensor Connection

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16170ATP/VY+T	−40°C to +125°C	20 TQFN

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/24	Initial release	—

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