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Portable Medical Power Management Solution with Cable Detection

MAX14663

General Description

The MAX14663 is a complete power solution for portable medical devices, including blood glucose meters.

The device integrates a high-efficiency single-cell Li-ion switching charger targeted at space-limited portable applications with small batteries.

An ultra low-power seal mode which significantly reduces standby current and preserves battery charge during prolonged periods of storage is also included. This mode extends battery shelf life, and enables improved customer experience with immediate out-of-box use.

Additionally, the MAX14663 embeds a Maxim proprietary ModelGauge™ (fuel gauge), which provides an accurate estimate of the available capacity for rechargeable Li-ion batteries.

A boost converter and LED current sinks are also integrated for powering OLED displays or LED backlights.

Internal cable-detection circuitry enables the MAX14663 to identify the presence of an unpowered/unconnected USB cable. This information can be used by the portable system to intelligently select its operating mode, maximizing accuracy and minimizing measurement errors.

The MAX14663 operates over the -20°C to +70°C temperature range and is available in a (5mm x 5mm), 40-pin, TQFN-EP package.

Applications

- Portable Blood Glucose Meters
- Portable Medical Devices
- USB Connected Devices

Benefits and Features

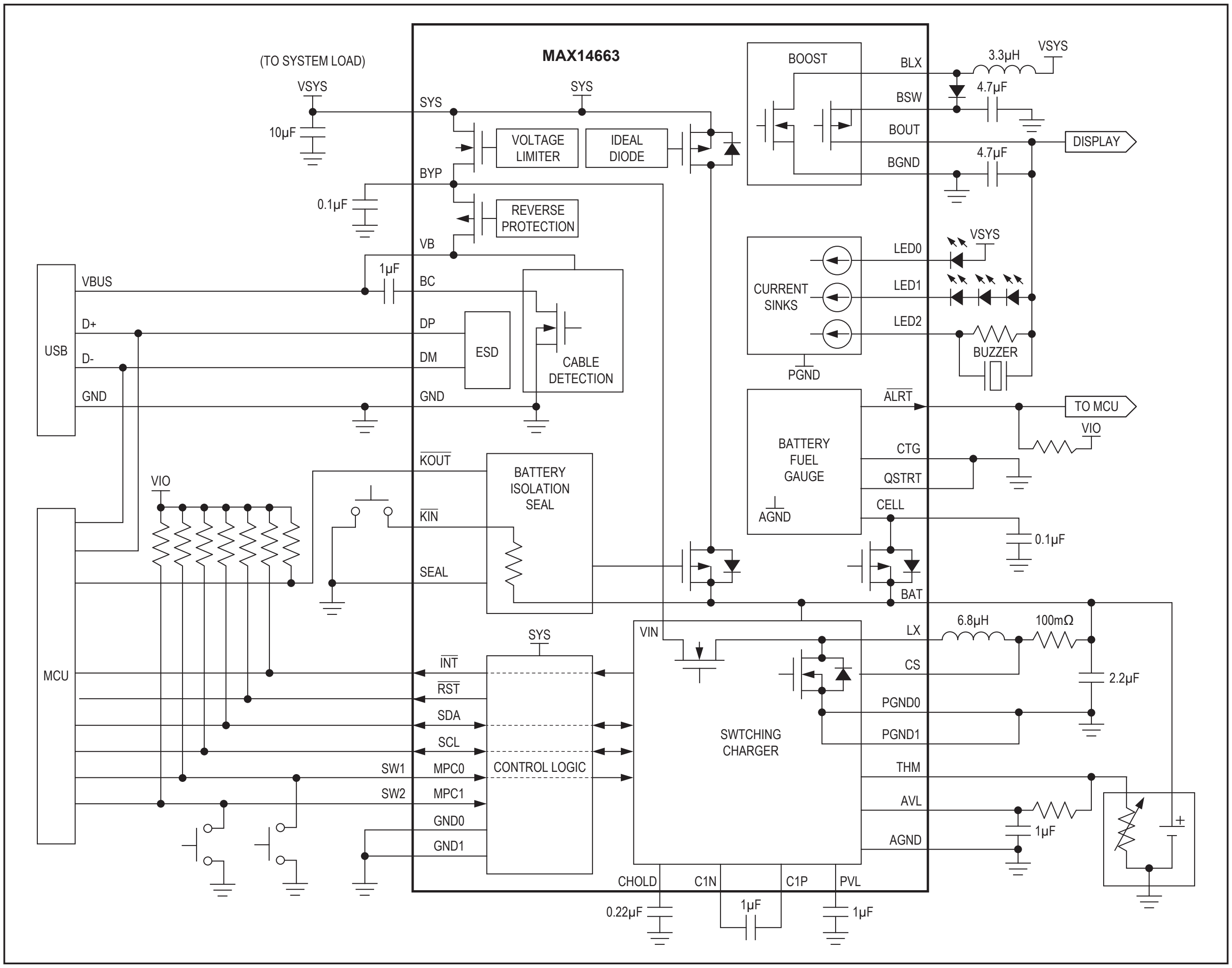
- High-Efficiency Switching Charger Tailored for Small Capacity Batteries Saves Space, Extends Battery Life
- Battery Isolation Switch Extends Battery Shelf Life
  - Hardware/Software Configurable
  - Integrated Power-Key Monitor
- Integration Simplifies and Shrinks Display Driving Circuitry
  - 3-Channel Programmable-LED Current Sinks
  - Integrated Step-Up Converter
- Integrated Protection and Control for Reliable Performance
  - Fully Integrated Cable Detection Controller to Ensure Measurement Accuracy
  - Overvoltage and Thermal Protection
    - 28V Tolerant VB Input Connection
  - High ESD Protection (VB, DP, DM, $\overline{\text{KIN}}$)
    - ±15kV HBM ESD Protection
    - ±10kV Air-Gap Protection
    - ±8kV Contact Discharge Protection
  - Manual Reset Controller
  - Programmable Interrupt Generation (I^2C)
- Integrated ModelGauge Host-Side Fuel Gauge Saves Space and Accurately Estimates State of Charge
  - ModelGauge Algorithm
  - Tolerates Temperature & Load Variation
  - No Error Accumulation
  - Learning Not Necessary
  - Current-Sense Resistor Not Required

***Ordering Information** appears at end of data sheet.*

ModelGauge™ is a registered trademark of Maxim Integrated Products, Inc.

19-6817; Rev 6; 8/20

Typical Application Circuit/Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND.)
BAT, $\overline{KIN}$, $\overline{KOUT}$, CS, THM, AVL, PVL, SYS, SEAL, MPC0, MPC1, $\overline{INT}$, $\overline{RST}$, SDA, SCL, $\overline{ALRT}$, CTG, QSTRT, DP, DM ....-0.3V to +6V
CELL....-0.3V to BAT+0.3V
LX ....-0.3V to PVL+0.3V
BBSW, BLX, LED0, LED1, LED2 .... -0.3V to +20V
BOUT....-0.3V to BSW+0.3V
BYP ....-0.3V to +30V
VB....-0.3V to BYP+0.3V
C1N ....-0.3V to PVL+0.3V
C1P.... PVL-0.3V to CHOLD+0.3V
C1P to C1N ....-0.3V to +6V
CHOLD .... PVL-0.3V to PVL+6V
VBC ....-0.3V to +0.6V
PGND0 to GSUB0, PGND1 to GSUB1....-0.3V to +0.3V
BGND to GSUB0, GSUB1 (GSUB0 and GSUB1 internally shorted).... -0.3V to +0.3V
AGND to GSUB0, GSUB1 (GSUB0 and GSUB1 internally shorted)....-0.3V to +0.3V
Continuous Current into VB, BAT.... ±800mA
Continuous Power Dissipation (multilayer board at T_A = +70°C):
40-pin, 5mm x 5mm TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature....-40° to +150°C
Storage Temperature Range ....-65ºC to +150ºC
Lead Temperature (soldering, 10s)....+300°C
Soldering Temperature (reflow)....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

40 TQFN-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).... 2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL SUPPLY CURRENT (V_{VB} = +5V, V_{BAT} = 3.6V, CD_EN = 00, CHG_EN = 00, BST_EN = 00, LDO_EN = 00, I_{BYP} = 0mA, I_{SYS} = 0mA.) (Fuel gauge disabled (FG_DIS = 1), LED disabled (LED0_CFG[2:0] = LED1_CFG[2:0] = LED2_CFG[2:0] = 000.))						
VB Input Supply Current	I_{VB}	All functions disabled		0.9	1.3	mA
		Cable detection enabled CD_EN = 11		1.5	2.5	
		Charger enabled, I_{CHG} = 0mA CEN_O = 11		5	10	
		Boost enabled, I_{BOUT} = 0mA BST_EN = 01		2.7	5	

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT Input Supply Current	I_{BAT}	Battery-isolation switch open, (SEAL condition active), V_{VB} = 0V		0.01	1	µA
		Battery-isolation switch closed, (SEAL condition off), V_{VB} = 0V, all functions disabled		2.7	4.5	µA
		Battery-isolation switch closed, (SEAL condition off), V_{VB} = 0V, fuel gauge active		23	45	µA
		Battery-isolation switch closed, V_{VB} = 0V, boost enabled (BST_V[3:0] = 0000), I_{BOUT} = 0mA, BST_EN = 1		1.3	2.3	mA
		Battery-isolation switch closed, V_{VB} = 0V, cable detect active, CD_EN = 11		300		µA
		Battery-isolation switch closed, V_{VB} = 0V, LED enabled		600		µA
POWER SWITCHES (V_{VB} = 4.4V to 28V, unless otherwise noted. Typical values are at V_{VB} = 5.0V, V_{BAT} = 3.6V.)						
VB Input Supply Voltage	V_{VB}		0		28	V
Q_{RPP} REVERSE POLARITY PROTECTION SWITCH (VB to BYP)						
RPP Switch On-Resistance	R_{ON_RPP}	V_{VB} = 4.4V		150	260	mΩ
Q_{OVP} OVERVOLTAGE PROTECTION SWITCH (BYP to SYS)						
Overvoltage Lockout Threshold	V_{OVLO}	BYP rising	6.15	6.7	7.2	V
Overvoltage Lockout Hysteresis	V_{OVLOH}	BYP falling		300		mV
Undervoltage Lockout Threshold	V_{UVLO}	BYP rising	3.3	3.8	4.2	V
Undervoltage Lockout Hysteresis	V_{UVLOH}	BYP falling		200		mV
V_{BYP} OVP Pulldown Current	I_{BYP_OVP}	V_{BYP} > V_{OVLO}		300		µA
V_{BYP} to BAT Shutdown UVLO Threshold		V_{VB} rising, V_{BYP} -V_{BAT} threshold	40	111	200	mV
		V_{VB} falling, V_{BYP} -V_{BAT} threshold	0.8	58	120	
SYS Voltage Regulation Voltage	V_{SYS}	I_{SYS} = 250mA	4.44	5	5.5	V
SYS UVLO	V_{SYS_UVLO}	SYS rising	2.0	2.4	2.8	V
SYS UVLO Hysteresis	V_{SYS_UVLOH}	SYS falling		130		mV
BAT UVLO	V_{BAT_UVLO}	BAT rising	1.95	2.2	2.5	V
BAT UVLO Hysteresis	V_{BAT_OVLOH}	BAT falling		110		mV
OVP Switch On-Resistance	R_{ON_OVP}	V_{VB} = 4.4V		220	500	mΩ
BAT OVLO	V_{BAT_OVLO}	BAT rising	4.3	4.38	4.55	V

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT OVLO Hysteresis	V_{BAT_OVLOH}	BAT falling		60		mV
SYS Turn-On Time	t_{ON}	V_{OVLO} > V_{VB} > V_{UVLO} (Note 3)		16		ms
SYS Voltage Rise Time		V_{SYS} from 20% to 80% of V_{VB} = 5V (Note 3)		1.1		ms
SYS Turn-Off time	t_{OFF}	R_{LOAD} = 20Ω, C_{SYS} = 10µF, V_{VB} > V_{OVLO} to V_{SYS} = 80% of V_{VB} (Note 3)		200		µs
Q_{DIO} IDEAL DIODE SWITCH (SYS to BAT)						
Ideal Diode Switch On-Resistance	R_{ON_DIO}	V_{BAT} = 3.6V		150	250	mΩ
BAT-SYS Ideal Switch Turn-On Threshold	$V_{(BATSYS)\_PPON}$			20.6		mV
BAT-SYS Ideal Switch Turn-Off Threshold	$V_{(BATSYS)\_PPOFF}$			2		mV
IBAT-to-SYS Current Limit	I_{BS_LIMIT}			1.3		A
Q_{ISO} BATTERY ISOLATION SWITCH (CELL to BAT)						
FG Seal Switch On-Resistance	R_{ON_ISO}	V_{BAT} = 3.6V		15	25	Ω
CABLE DETECTOR AND ESD PROTECTION DIODES (V_{VB} = 4.4V to 28V, unless otherwise noted. Typical values are at V_{VB} = 5.0V.)						
DP, DM Capacitance				15		pF
CABLE DETECTOR						
Capacitance Threshold 1	C_{TH1}	Room temperature only (Note 4)		20		pF
Capacitance Threshold 2	C_{TH2}	Room temperature only (Note 4)		40		pF
Capacitance Threshold 3	C_{TH3}	Room temperature only (Note 4)		60		pF
Capacitance Threshold 4	C_{TH4}	Room temperature only (Note 4)		80		pF
Maximum Injected Current During Cable Detection		CTH_SEL[1:0] = 00		1		µA
Maximum VB Voltage During Cable Detection				1		V
VBC On-Resistance		V_{VB} = 0V		0.24	1	Ω
TIMING CHARACTERISTICS						
Cable Detection Time	t_{DET}			470		ms
VB-Off Debounce Time	t_{DEB_FALL}	Cable detection active (VB falling edge)		64		ms
VB-On Debounce Time	t_{DEB_RIS}	Cable detection NOT active (VN rising edge)		36		ms
THERMAL PROTECTION (VB Supplied)						
Thermal Shutdown				150		°C

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Hysteresis					20		°C
THERMAL PROTECTION (VBAT Supplied)							
Thermal Shutdown					150		°C
Thermal Hysteresis					20		°C
BATTERY CHARGER (V_{VB} = 5V, 1µF capacitor from VB to PGND, 100nF from BYP to GND, 1µF capacitor from AVL, PVL to GND, (JEITA disabled, JEN = 0), V_{THM} = 2.5V, 1µF from C1P to C1N, L = 6.8µH, R_S = 100mΩ, CON_FR1 = 0, CON_FR2 = 0, unless otherwise noted.)							
BYP INPUT							
BYP to BAT Charger Shutdown Threshold	$V_{BYPvsBAT}$	VB rising: V_{BYP} - V_{BAT} threshold		200	360	550	mV
		VB falling: V_{BYP} - V_{BAT} threshold		40	100	200	
BATTERY CHARGER							
Battery Regulation Voltage	V_{CHG}	6-bit programmable from 3.5V to 4.4V in 20mV steps		3.5		4.4	V
		VCHG reduction for JEITA enabled and active			120		mV
Battery Regulation Voltage Accuracy		Linear charger mode	T_A = +25°C	-0.5		0.5	%
			T_A = -20°C to +70°C	-1		1	
Battery Refresh Threshold	BATRFH	Below regulation point	VRSTRT = 0	90	135	180	mV
			VRSTRT = 1	170	214	270	
Battery Overvoltage Protection	BATOV	BAT threshold over regulation voltage to turn off charger during charge (% of regulation voltage)		101	102.5	104	%
		Hysteresis (V_{BAT} Falling)			65		mV
Battery Removal Threshold		Battery voltage rising			5		
Battery Prequalification Threshold	V_{PQ}	3-bit programmable, BAT rising		2.4		3.1	V
		Hysteresis BAT falling			100		mV
Battery Prequalification Threshold Accuracy		T_A = +25°C		-1		1	%
Battery Prequalification Current	I_{PQ}	2.1V < V_{BAT} < V_{PQ}; T_A = +25°C		20	25	30	mA
		V_{BAT} < 2.1V			13		
Battery Fast-Charge Current	I_{CHG}	4-bit programmable (Note 5), R_S = 50mΩ		50		750	mA
		I_{CHG} percentage for JEITA enabled and active I_{CHG} ≥ 100mA			50		%

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery-Fast-Charge Current Accuracy		50mA < I_{CHG} < 500mA; T_A = +25°C	-10		10	%
		100mA < I_{CHG} < 500mA; T_A = -20°C to +70°C				
Charge-Current Termination Threshold	I_{DONE}	3-bit programmable, independent from JEITA	12.5		150	mA
		Hysteresis ICHARGE rising, I_{DONE} = 50mA		25		
Charge-Current Termination Accuracy		I_{DONE} > 25mA	-25		+25	%
		I_{DONE} ≤ 25mA	-60		+60	
Charge-Current Termination Deglitch	I_{DONE_DGL}	Deglitch time with 2mV overdrive, 100ns rise/fall time		4		ms
Battery Leakage Current	I_{BATLKG}	CHG_EN low, SEAL MODE		0.01	1	μA
Thermal Regulation Temperature	TH_{REG}	ICHG reduces thermal regulation temperature when die temp rises above		120		°C
Thermal Regulation Gain	TH_{GN}	Charge current drops to 0 at +120°C		5		%/°C
Charger Soft-Start Time	t_{SF}			160		ms
BATTERY CHARGER TIMER						
Prequalification Time	t_{PQ}	V_{BAT} < V_{PQ}		60		min
Fast-Charge Time	t_{FCH}	CHGTM[1:0] = 11		10		hrs
Charger-DONE Delay Time	$I_{DONEDLY}$	From I_{DONE} threshold detection until charger turns off and CHG goes high		15		s
Timer Accuracy				20		%
BUCK REGULATOR						
Switching Frequency	f_{SW}	CON_FR1 = I, CON_FR2 = 0, T_A = +25°C	0.95	1.1	1.25	MHz
		CON_FR1 = I, CON_FR2 = 0, T_A = +25°C	0.6	0.7	0.8	
Max Duty Cycle	D_{T_MAX}			99.7		%
Maximum On-Time	t_{ON_MAX}			8		μs
Minimum Off-Time	t_{ON_MIN}			40		ns
High-Side Resistance	R_{ONH}			90	210	mΩ
Low-Side Resistance	R_{ONL}			120	240	mΩ
JEITA THERMISTOR MONITOR SPECIFICATIONS						
Open Threshold	V_{THOP}	Battery missing	92	94	96	% of AVL

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THM Threshold T1	V_{THT1}	1.2% hysteresis		70.5	74	77.6	% of AVL
		Thermistor temperature falling			0		°C
THM Threshold T2	V_{THT2}	1.2% hysteresis		61.6	65	67.8	% of AVL
		Thermistor temperature falling			10		°C
THM Threshold T3	V_{THT3}	1.2% hysteresis		48	50	52	% of AVL
		Thermistor temperature falling			25		°C
THM Threshold T4	V_{THT4}	1.2% hysteresis		31.2	33	34.3	% of AVL
		Thermistor temperature rising			45		°C
THM Threshold T5	V_{THT5}	1.2% hysteresis		22.1	23	24.1	% of AVL
		Thermistor temperature rising			60		°C
SHORT Threshold	V_{THSH}	Thermistor fault		3	5	7	% of AVL
THM Pulldown Impedance, Shutdown	R_{THM_SD}	JEN = 0			12		kΩ
THM Input Bias Current	I_{THM}	VTHM = AVL and 0V, JEN = High	T_A = +25°C	-0.1		+0.1	µA
			T_A = +70°C		0.1		
AVL/PVL OUTPUT VOLTAGE							
AVL Regulated Output Voltage	V_{AVL}	5.5V < V_{VB}, I_{AVLOUT} < 1mA		4.3	4.5	4.7	V
PVL Regulated Output Voltage	V_{PVL}	5.5V < V_{VB}, I_{PVLOUT} < 1mA		4.8	5.1	5.25	V
FUEL GAUGE (V_{IN} = 2.5V to 4.5V, T_A = -20°C to +70°C, unless otherwise noted.)							
Supply Voltage	V_{CELL}	(Note 6)		2.5		4.5	
Fuel-Gauge SOC Reset (VRESET Register)	V_{RST}	Configuration range, in 40mV steps		2.28		3.48	V
		Trimmed at 3V		2.85	3	3.15	

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD0}	Sleep mode, T_A < +50°C		0.5	2	µA
		Hibernate mode, reset comparator enabled (VRESET.Dis = 1)		3	5	
		Hibernate mode, reset comparator disabled (VRESET.Dis = 0)		4		
	I_{DD1}	Active mode		23	40	
Time Base Accuracy	t_{ERR}	Active, hibernate modes (Note 7)	-3.5		3.5	%
ADC Sample Period		Active mode		250		ms
		Hibernate mode		45		S
Voltage Error	V_{ERR}	V_{CELL} = 3.6V, T_A = +25°C (Note 8)	-7.5		7.5	mV
		T_A = -20°C to 70°C	-20		20	
Voltage Measurement Resolution				1.25		mV
Voltage Measurement Range		V_{CELL} pin	2.5		4.5	V
BOOST CONVERTER (V_{SYS} = 3.6V.)						
Input Operating Range		Input voltage = V_{SYS}	2.7		5.5	V
Output Voltage Range			6		17	V
Output-Voltage Resolution		4 bits		1000		mV
Operating Frequency			1400	1500	1700	kHz
Oscillator Maximum Duty Cycle				96		%
Output Regulation Error			-2.5		2	%
BLX On-Resistance		I_{BLX} = 50mA		200	600	mΩ
True-Shutdown Switch [BSW to BOUT] On-Resistance		V_{BSW} = 5.8V		1	2	Ω
BLX Leakage Current		T_A = +25°C			26	µA
BLX Current Limit		Duty cycle = 80%	1.5	1.8	2.1	A
Soft-Start Period				50		ms

Electrical Characteristics (continued)

(T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Max Operative Boost Current				50		mA
CURRENT SINKS (V_{SYS} = 3.6V, V_{GND} = V_{PGND} = 0V.)						
Allowed V_{LED} Voltage Range	V_{INLED}				17	V
I_{LED} Input-Current Range		0.6mA steps, (register 0A) LEDIS-TEP[1:0] = 00	0.6		15	mA
		1mA steps, (register 0A) register LEDISTEP[1:0] = 01	1		25	
		1.2mA steps, (register 0A) LEDISTEP[1:0] = 11	1.2		30	
I_{LED} Current Accuracy		I_{LED} = 25mA, T_A = +25°C			2.6	%
		I_{LED} = 25mA, T_A = -20°C to +70°C			5	
I_{LED} Dropout Voltage	V_{LED_DROP}	V_{LED} AT I_{LED} = 0.9 x 25mA, T_A = +25°C		200	400	mV
		V_{LED} AT I_{LED} = 0.9 x 25mA, T_A = -20°C to +70°C			620	
Leakage in Shutdown		V_{LED} = 17V		0.1	5	µA
Open LED Detection Thresh-old		LED_ enabled, LED_ISTEP[1:0] = 00		87	150	mV
DIGITAL SIGNALS (V_{SYS} = 2.5V to 5.5V.)						
CTG, SDA, SCL, QSTRT, SEAL, MPC0, MPC1, $\overline{KIN}$, Input Logic-High	V_{IH}		1.4			V
CTG, SDA, SCL, QSTRT, SEAL, MPC0, MPC1, $\overline{KIN}$, Input Logic-Low	V_{IL}				0.5	V
SDA, ALRT, RST, INT, $\overline{KOUT}$ Output Logic-Low	V_{OL}	I_{OL} = 4mA			0.4	V
ALRT, RST, INT, $\overline{KOUT}$ High-Level Leakage Current	I_{LK}				1	µA
$\overline{KIN}$ Pullup Resistance to BAT	R_{PULL}		10	20	35	kΩ
SDA, SCL Bus Low-Detection Current	I_{PD}	V_{SDA} = V_{SCL} = 0.4V (Note 9)		0.2	0.4	µA
Bus Low Detection Timeout	t_{SLEEP}	(Note 10)		2.25		s
SCL Clock Frequency	f_{SCL}	(Note 11)			400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs

Electrical Characteristics (continued)

(T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C) (Note 2)

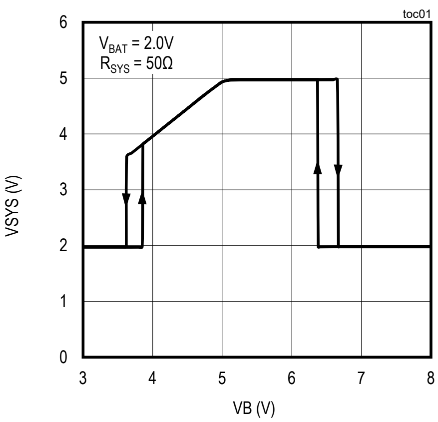
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition (Repeated) Hold Time	$t_{HD:STA}$	(Note 12)	0.6			µs
Low Period for SCL Clock	t_{LOW}		1.3			µs
High Period for SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Write hold time) (Notes 13, 14)			0	µs
Data Setup Time	$t_{SU:DAT}$	(Note 13)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 15)		100		ns
SCL, SDA Input Capacitance	$C_{B,IN}$	(Note 16)		11		pF
ESD PROTECTION						
DP, DM, VB, $\overline{\text{KIN}}$, VBC		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap		±10		kV
		IEC61000-4-2 Contact		±8		kV
All Other Pins		Human Body Model		±2		kV

Note 2: Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
Note 3: SYS capacitance range, C_{SYS} = 10µF to 50µF
Note 4: See *Cable Detection Section* for more information.
Note 5: Maximum charging and SYS current are limited by the total current into VB. Current into VB must not exceed 800mA up to 50% duty cycle or 640mA above 50% duty cycle.
Note 6: All voltages are referenced to VSS.
Note 7: Test is performed on unmounted/unsoldered parts.
Note 8: The voltage is trimmed and verified with 16X averaging.
Note 9: This current is always present.
Note 10: The device enters shutdown mode after SCL < V_{IL} and SDA < V_{IL} for longer than t_{SLEEP}.
Note 11: Timing must be fast enough to prevent the device from entering sleep mode due to bus low for period > t_{SLEEP}.
Note 12: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 13: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 14: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the V_{IH} (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 15: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
Note 16: CB is total capacitance of one bus line in pF.

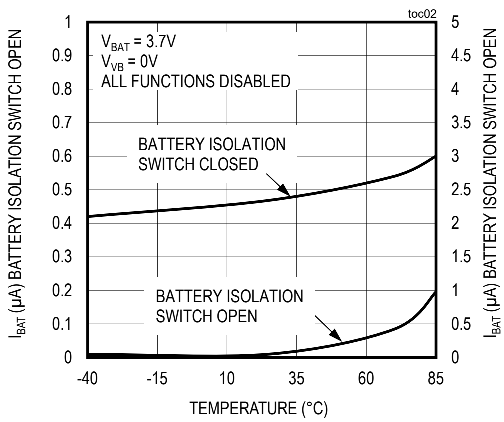
Typical Operating Characteristics

(R_S= 100mΩ, T_A = +25°C, unless otherwise noted.)

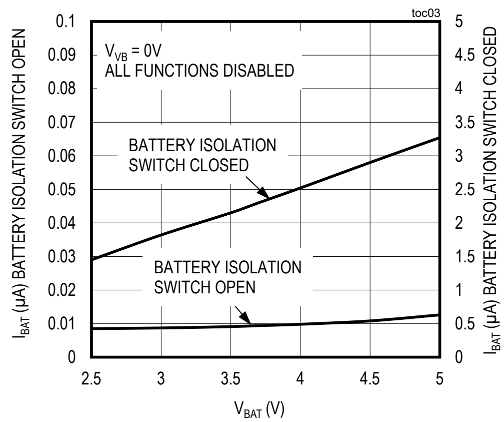
VSYS vs. VB



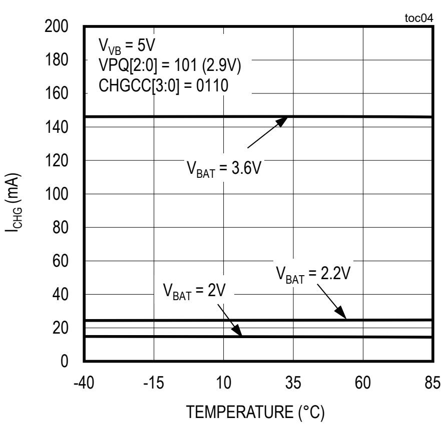
I_{BAT} vs. TEMPERATURE



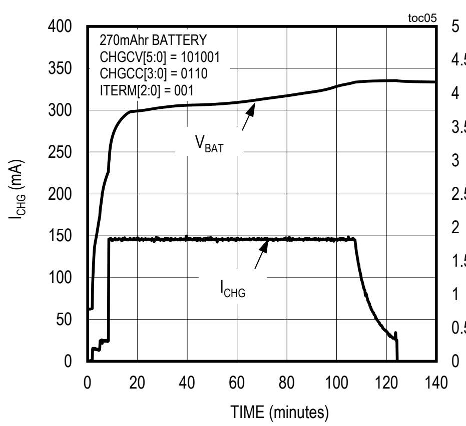
I_{BAT} vs. V_{BAT}



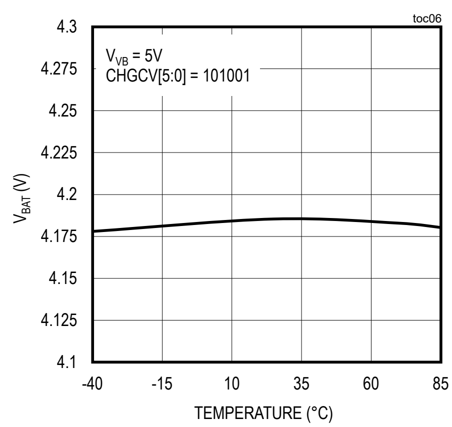
I_{CHG} vs. TEMPERATURE



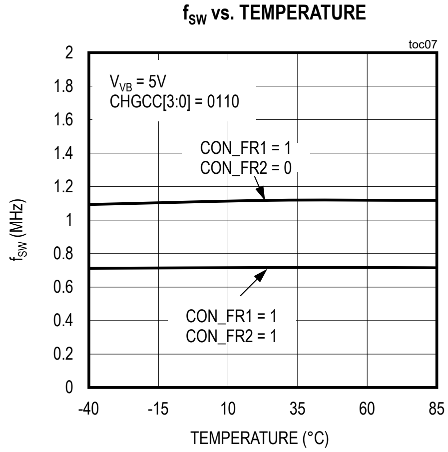
I_{CHG} / V_{BAT} vs. TIME



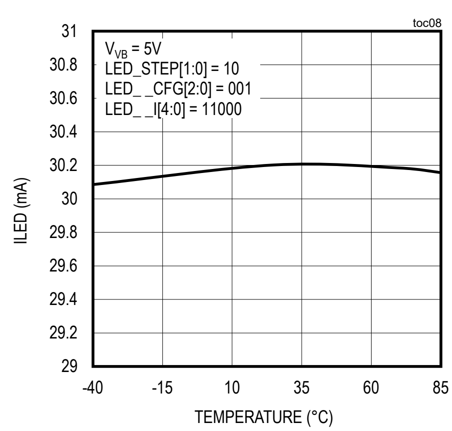
V_{BAT} REGULATION vs. TEMPERATURE



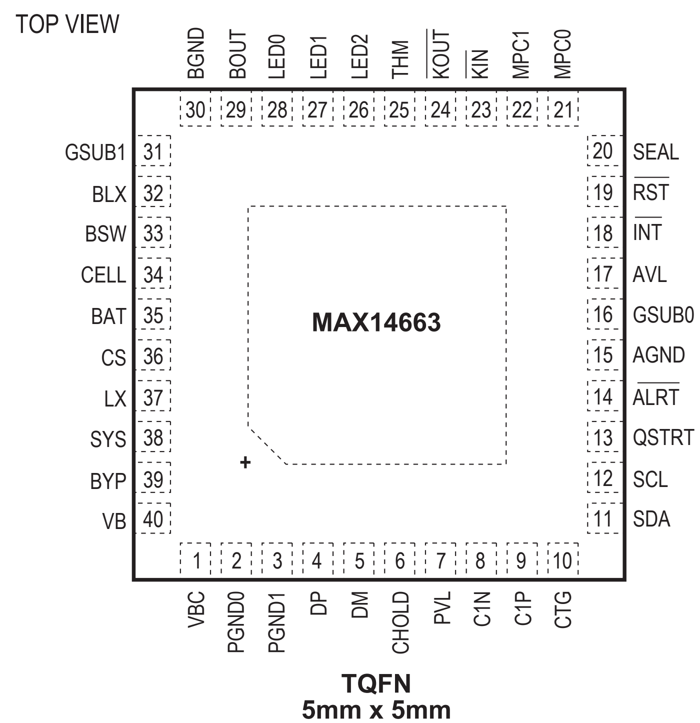
f_{SW} vs. TEMPERATURE



ILED vs. TEMPERATURE



Pin Configuration



Pin Description

PIN	NAME	I/O	FUNCTION
1	VBC	I/O	VB Bypass Cap Connection. Use as current injection/measuring point in cable detection algorithm.
2	PGND0	GND	Charger Power Ground
3	PGND1	GND	Charger Power Ground
4	DP	I	ESD Protection for D+
5	DM	I	ESD Protection for D-
6	CHOLD	O	Charge Pump Output
7	PVL	O	Charger Power Regulated Voltage 5.25V
8	C1N	O	Charge-Pump Capacitor Negative
9	C1P	O	Charge-Pump Capacitor Positive
10	CTG	I	Connect to Ground

Pin Description (continued)

PIN	NAME	I/O	FUNCTION
11	SDA	I/O	I²C Data
12	SCL	I/O	I²C Clock
13	QSTRT	I	Quick-Start Input. Allows reset of the fuel gauge through hardware. Connect to GND if not used.
14	$\overline{\text{ALRT}}$	O	Fuel Gauge Interrupt
15	AGND	GND	Analog Ground
16	GSUB0	GND	Substrate. Connect to ground.
17	AVL	O	Charger Analog 4.5V Regulated supply
18	$\overline{\text{INT}}$	O	Interrupt Output, Active-Low, Open-Drain
19	$\overline{\text{RST}}$	O	Reset Output, Active-Low, Open-Drain
20	SEAL	I	Battery-Storage Seal Input
21	MPC0	I	Multi-Purpose Control Input 0 (Charger/Cable Detect/LED)
22	MPC1	I	Multi-Purpose Control Input 1 (Charger/Cable Detect/LED)
23	$\overline{\text{KIN}}$	I	Key Input, Power Button Monitored. Active-low, internal pullup to BAT. Connect $\overline{\text{KIN}}$ to a momentary pushbutton to GND.
24	$\overline{\text{KOUT}}$	O	Key Output, Active-Low, Open-Drain, Buffered Copy of $\overline{\text{KIN}}$
25	THM	I	Thermistor Temperature Sensing pin
26	LED2	O	Programmable Current Sink
27	LED1	O	Programmable Current Sink
28	LED0	O	Programmable Current Sink
29	BOUT	I	Boost-Converter Output
30	BGND	GND	Boost Power Ground
31	GSUB1	O	Substrate. Connect to ground.
32	BLX	O	Boost-Converter Switching-Node Pin
33	BSW	O	Boost-Converter Output Power Switch Input
34	CELL	I	Fuel Gauge Voltage Input
35	BAT	I/O	Li-ION Battery Connection
36	CS	I	Charger Current Sense
37	LX	O	Switching Charger Switch Node
38	SYS	I/O	System Power Connection
39	BYP	O	Reverse-Protected Bypass Pin
40	VB	I	USB VBUS Supply

Detailed Description

The MAX14663 is a collection of power circuits commonly found in portable medical equipment such as high-end blood glucose meters. It is targeted at current high-end devices with more advanced displays that consume more power and require rechargeable batteries. It combines a battery charger and fuel gauge, voltage protection and conversion, and cable detection and protection.

Cable Detector and ESD Protection

The MAX14663 includes a cable detector for blood glucose meters (BGM), and the device detects the presence of a cable by measuring the capacitance on VB through the injection of probing currents into the VB node.

Cable Detection

The MAX14663 detects a valid VB voltage (VB) or a cable present. When a valid VB voltage is present, the DET status bit is asserted and an interrupt is signaled. When there is no valid VB voltage, the cable detection is enabled. VB detection is normally disabled during the cable detection loop to minimize the capacitance measurement but is periodically turned on to check whether VB has been reapplied. When ENB = 0, DET is updated at the end of each 200μs long cable detection cycle when BSY goes high. The MAX14663 automatically adjusts the internal current to the programmed threshold. When the detected capacitance is greater than the selected threshold, a cable is considered plugged. When the detected capacitance is smaller than the selected threshold, it is considered no cable present. See the CD-CFG register for capacitance threshold values.

Battery Charger

This charger is intended for portable medical applications. It is designed to charge a battery with minimal power dissipation. The charger regulates the current based on the charge profile, Figure 1. The currents shown in the diagram assume that the current is not being limited by the input or thermal considerations.

Prequalification Mode

This mode is utilized during battery prequalification (VBAT < VPQ). The current limit in this mode is specified to be less than 0.1C precharge for batteries with 280mAhr capacity, and low enough power so as not to be hazardous when applied to a shorted or damaged battery.

Fast-Charge Mode

This is the standard CC/CV charging mode. In this mode, the charger will attempt to charge the battery at the current specified in the fast-charge current register. The fast-charge current can be programmed from 50mA to 750mA in 25mA steps. This will be set in a 4-bit value indexed from 0mA.

Charge Termination

There are several conditions that cause the charger to stop charging. The charger can be manually stopped by an I^2C command. The charger can also stop itself if the AUTOSTP bit is set. When AUTOSTP is enabled, the charge current has dropped to the value set by ITERM, and the TopOffTime timer has expired the charger will transition to end-of-charge and the charger will be automatically disabled. In this condition, there is a 1.8mA (typ) discharging draw on the battery which supplies some of the internal control blocks of the charger. With AUTOSTP enabled, the charger will also restart when the voltage drops BATRFH threshold below the current charge voltage setting, VCHG (battery regulation voltage).

JEITA Control

The charger has a thermistor interface that allows it to adjust the charge settings based on the battery temperature. The temperatures are separated into five ranges based on the boundary temperatures of T1 (0°C), T2 (10°C), T3 (25°C), and T4 (45°C). Below T1 or above T4, the charger is disabled, and between T2 and T3, the charger functions normally. The behavior in the regions between T1-T2 and T3-T4 are specified in the JEITA control register. In each region the user can independently specify whether or not to reduce the charge voltage or current as illustrated in Figure 2. The voltage can be reduced by 120mV and the fast-charge current can be reduced by half in these regions. The thermistor monitor also has a fifth threshold (T5) of 60°C. This can be used by the system by making the interrupt.

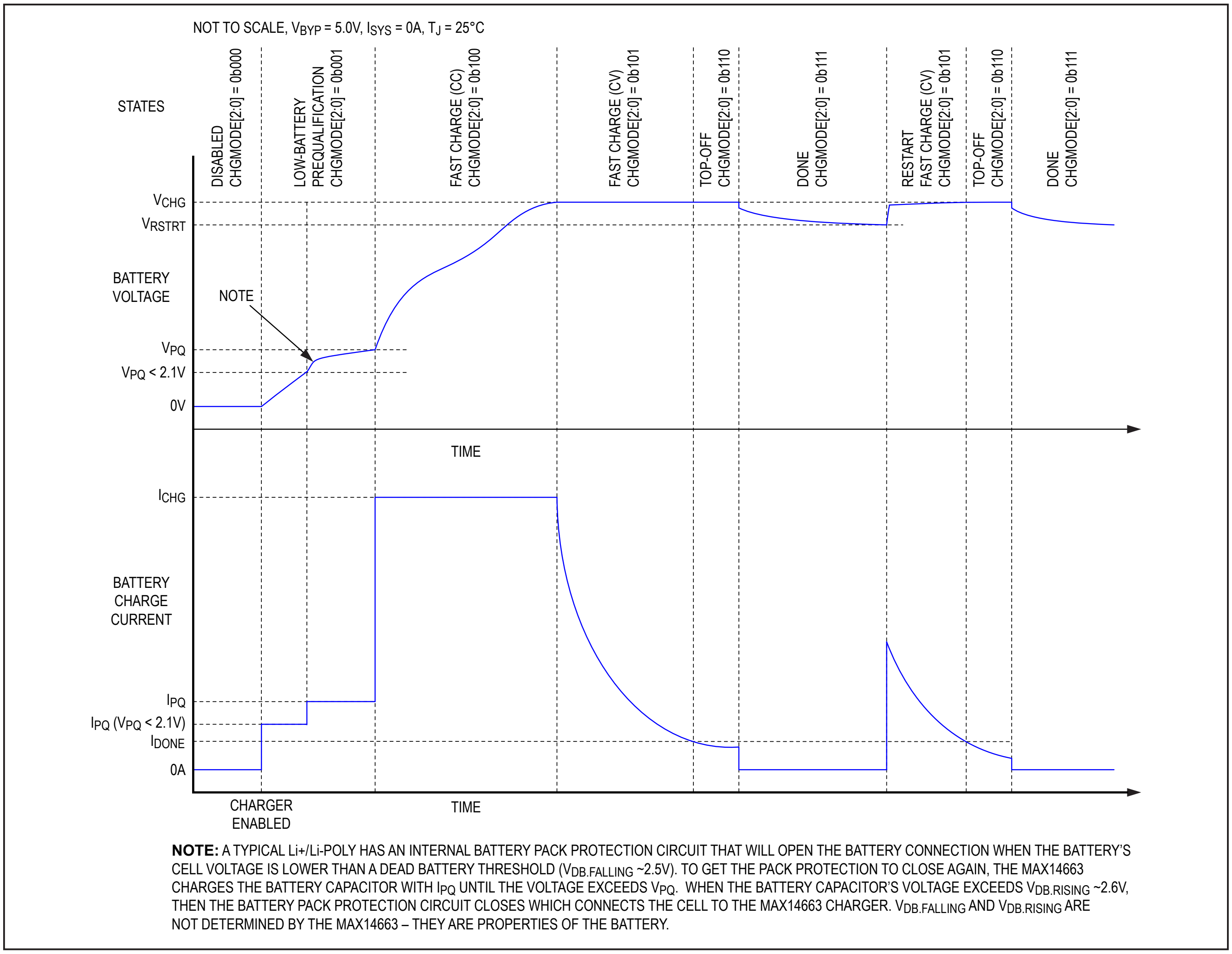


Figure 1. Charging Profile

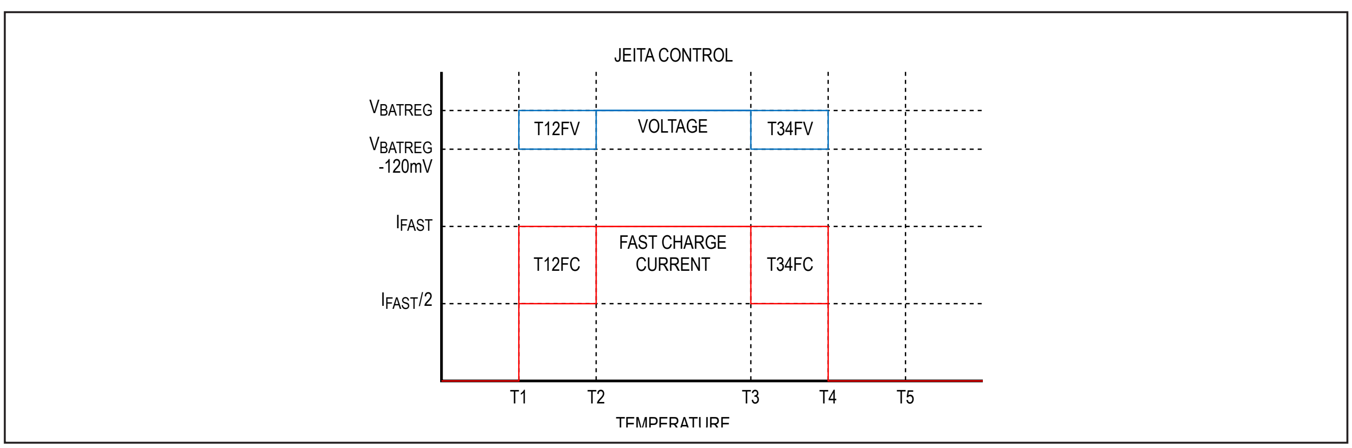


Figure 2. JEITA Control

Safety Timers

The charger includes safety timers to limit the amount of time that can be spent in the different charging modes.

Fuel Gauge

ModelGauge Theory of Operation

The MAX14663 fuel gauge is based on the MAX17048 stand-alone fuel gauge and simulates the internal, nonlinear dynamics of a Li+ battery to determine the state of charge (SOC). The sophisticated battery model considers impedance and the slow rate of chemical reactions in the battery. ModelGauge performs best with a custom model, obtained by characterizing the battery at multiple discharge currents and temperatures to precisely model it. At power-on reset (POR), the ICs have a preloaded ROM model that performs well for some batteries.

Fuel-Gauge Performance

In coulomb counter-based fuel gauges, SOC drifts because offset error in the current-sense ADC measurement accumulates over time. Instantaneous error can be very small, but never precisely zero. Error accumulates over time in such systems (typically 0.5%–2% per day) and requires periodic corrections. Some algorithms correct drift using occasional events, and until such an event occurs, the algorithm's error is boundless:

- Reaching predefined SOC levels near full or empty
- Measuring the relaxed battery voltage after a long period of inactivity
- Completing a full charge/discharge cycle

ModelGauge requires no correction events because it uses only voltage, which is stable over time. The ModelGauge remains accurate despite the absence of any of the above events; it neither drifts nor accumulates error over time.

To correctly measure performance of a fuel gauge as experienced by end-users, exercise the battery dynamically. Accuracy cannot be fully determined from only simple cycles.

Battery Voltage and State of Charge

Open-circuit voltage (OCV) of a Li+ battery uniquely determines its SOC; one SOC can have only one value of OCV. In contrast, a given VCELL can occur at many different values of OCV because VCELL is a function of time, OCV, load, temperature, age, and impedance, etc. One value of OCV can have many values of VCELL. Therefore, one SOC can have many values of VCELL, so VCELL cannot uniquely determine SOC.

Even the use of sophisticated tables to consider both voltage and load results in significant error due to the load transients typically experienced in a system. During charging or discharging, and for approximately 30min after, VCELL and OCV differ substantially, and VCELL has been affected by the preceding hours of battery activity. ModelGauge uses voltage comprehensively.

Temperature Compensation

For best performance, the host microcontroller must measure battery temperature periodically, and compensate the RCOMP ModelGauge parameter accordingly, at least once per minute. Each custom model defines constants RCOMP0 (default, 0x97), TempCoUp (default, -0.5), and TempCoDown (default, -5.0). To calculate the new value of CONFIG.RCOMP:

```
    T is battery temperature (°C)
if (T > 20) {
        RCOMP = RCOMP0 + (T - 20) x TempCoUp;
}
else {
        RCOMP = RCOMP0 + (T - 20) x TempCoDown;
}
```

Impact of Empty-Voltage Selection

Most applications have a minimum operating voltage below which the system immediately powers off (empty voltage). When characterizing the battery to create a custom model, choose empty voltage carefully. Capacity unavailable to the system increases at an accelerating rate as empty voltage increases.

To ensure a controlled shutdown, consider including operating margin into the fuel gauge based on some low threshold of SOC, for example shutting down at 3% or 5%. This utilizes the battery more effectively than adding error margin to empty voltage.

Battery Insertion

When the battery is first inserted into the system, the fuel gauge IC has no previous knowledge about the battery's SOC. Assuming that the battery is relaxed, the IC translates its first VCELL measurement into the best initial estimate of SOC. Initial error caused by the battery not being in a relaxed state diminishes over time, regardless of loading following this initial conversion. While SOC estimated by a coulomb counter diverges, ModelGauge SOC converges, correcting error automatically. Initial error has no long-lasting impact.

Battery Insertion Debounce

Any time the IC powers on or resets (see the VRESET/ ID Register (0x18) section), it estimates that OCV is the maximum of 16 VCELL samples (1ms each, full 12-bit resolution). OCV is ready 17ms after battery insertion, and SOC is ready after 175ms.

Battery Swap Detection

If VCELL falls below VRST, the IC quick starts when VCELL returns above VRST. This handles battery swap; the SOC of the previous battery does not affect that of the new one. See the *Quick Start and VRESET/ID Register* (0x18) sections.

Quick Start

If the IC generates an erroneous initial SOC, the battery insertion and system power-up voltage waveforms must be examined to determine if a quick start is necessary, as well as the best time to execute the command. The IC samples the maximum VCELL during the first 17ms. See the *Battery Insertion Debounce* section. Unless VCELL is fully relaxed, even the best sampled voltage can appear greater or less than OCV. Therefore, quick start must be used cautiously.

Most systems should not use quick start because the ICs handle most startup problems transparently, such as intermittent battery-terminal connection during insertion. If battery voltage stabilizes faster than 17ms, as illustrated in Figure 6, then do not use quick start.

The quick-start command restarts fuel-gauge calculations in the same manner as initial power-up of the IC. If the system power-up sequence is so noisy that the initial estimate of SOC has unacceptable error, the system microcontroller may be able to reduce the error by using quick-start. A quick-start is initiated by a rising edge on the QSTRT pin, or by writing 1 to the quick-start bit in the MODE register.

Power-On Reset (POR)

POR includes a quick start, so only use it when the battery is fully relaxed. See the *Quick Start* section. This command restores all registers to their default values. After this command, reload the custom model. See the *CMD Register* (0xFE) section.

Hibernate Mode

The ICs have a low-power hibernate mode that can accurately fuel gauge the battery when the charge/ discharge rate is low. By default, the device automatically enters and exits the hibernate mode according to the charge/discharge rate, which minimizes quiescent current (below 5FA) without compromising fuel-gauge accuracy. The ICs can be forced into hibernate or active modes. Force the IC into hibernate mode to reduce power consumption in applications with less than C/4-rate maximum loading. For applications with higher loading, Maxim recommends the default configuration of automatic control of hibernate mode.

In hibernate mode, the device reduces its ADC conversion period and SOC update to once per 45s. See the HIBRT Register (0x0A) section for details on how the IC automatically enters and exits hibernate mode.

Alert Interrupt

The ICs can interrupt a system microcontroller with five configurable alerts. All alerts can be disabled or enabled with software. When the interrupt occurs, the system microcontroller can determine the cause from the STATUS register.

When an alert is triggered, the IC drives the ALRT pin logic-low and sets CONFIG.ALRT = 1. The ALRT pin remains logic-low until the system software writes CONFIG.ALRT = 0 to clear the alert. The alert function is enabled by default, so any alert can occur immediately upon power-up. Entering sleep mode clears no alerts.

Sleep Mode

In sleep mode, the IC halts all operations, reducing current consumption to below 1µA. After exiting sleep mode, the IC continues normal operation. In sleep mode, the IC does not detect self-discharge. If the battery changes state while the IC sleeps, the IC cannot detect it, causing SOC error. Wake up the IC before charging or discharging. To enter sleep mode, write MODE.EnSleep = 1 and either:

- Hold SDA and SCL logic-low for a period for t_{SLEEP}. A rising edge on SDA or SCL wakes up the IC.
- Write CONFIG.SLEEP = 1. To wake up the IC, write CONFIG.SLEEP = 0. Other communication does not wake up the IC. POR does wake up the IC.

Applications which can tolerate 4µA should use hibernate rather than sleep mode.

Power Protection and Delivery

The MAX14663 is designed to deliver reliable power to the system from either a USB connector or battery, and to transition between these sources without disrupting the system. In addition to routing power to the system, the MAX14663 also provides protection for some common anomalies on the USB VB input such over voltage. This is accomplished through four power switches between five power connections.

RPP Switch

Q_{RPP} is the switch connecting VB to BYP. This switch is also utilized to isolate the bypass capacitance from the VB pin during cable detection.

Overvoltage Protection Switch

Q_{OVP} is the switch between BYP and SYS. This switch protects the system power output from overvoltage conditions up to +28V applied to the VB input. This overvoltage protection includes a voltage limiting mode so that for voltages greater than the V_{LIM} (plus minimum dropout at the given load current), but less than V_{OVLO}, the OVP switch will act as a linear regulator. Above V_{OVLO} the switch is opened and power is disconnected from the part, and below V_{LIM} the switch is closed and the voltage applied to VB is passed directly to the part. This OVP circuitry also blocks reverse current to prevent the battery from back feeding the charger cable detection circuits. The status of the OVP is accessible through the I^2C interface and can be programmed to generate an interrupt. To minimize inrush current, the MAX14663 features a soft-start capability to slowly turn on the internal MOSFET. The soft-start is initiated when VB is valid for longer than the debounce time, t_{DEB}.

Ideal Diode Switch

Q_{DIO} is the switch connecting SYS to BAT. This switch behaves as an ideal diode switch between the battery and the system power output (SYS). The purpose of this switch is to provide power to the system output from the battery when VB is outside the acceptable range. This switch is also used to isolate the system load from the battery in sealed battery isolation mode.

Battery Isolation Switch

Q_{ISO} is the switch between CELL and BAT. This battery isolation switch preserves battery life when the product is sitting on a shelf waiting to be purchased. The switch is opened in the factory just before packaging by actively driving the SEAL pin high, or through an I^2C command. The switch is closed by the included power-button monitoring circuitry when the end customer presses the power button ($\overline{KIN}$),or when a voltage larger than V_{UVLO} is present at VB. The battery seal circuitry includes a pull-up to monitor the $\overline{KIN}$ press and provides a buffered output ($\overline{KOUT}$) to the system.

Interrupts

The MAX14663 includes an interrupt output which can be configured to indicate status changes for a variety of different signals and events. The interrupt behavior and status is configured and read through the I^2C interface. The specific interrupt sources are detailed in the register descriptions.

Reset

The MAX14663 includes the ability to monitor key presses and other system status signals to force the processor into reset. The following criteria will cause manual reset to go active:

- VB > VB_UVLO
- MPC1, MPC0 and $\overline{KIN}$ are all held low

Reset will go active when these conditions have been met for two seconds and remain active until one of the conditions is no longer satisfied. Reset will also be driven active when the part is in its internal power-on reset state immediately after VSYS becomes valid.

Boost Converter

The MAX14663 includes a boost converter suitable for providing power to an OLED display or white LED backlights. This step-up DC-DC converter operates from a 2.7V to 5.5V supply. It includes an internal high-voltage nMOSFET switch with low on-resistance. A true-shutdown feature disconnects the battery from the load and minimizes the supply current consumption. This DC-DC converter provides adjustable output voltage from 6V to 17V with 1V steps.

Programmable Current-Sinks

The MAX14663 includes three low-dropout linear current regulators from LED_ to PGND. These current-sink regulators are suitable for sinking current from external LED cathode terminals. The LED_ currents are individually regulated to an I2C programmable level from OFF to 30mA in 25 steps, independently set for each LED_. There is a single register that allows the selection of one of three step sizes which applies to all three current sinks. The behavior of the current-sinks is programmable. They can be configured to be gated by a PWM signal for finer dimming control or to provide status information such as the state of the battery charger. The LED PWM input frequency range is 5MHz to 50MHz. The LED PWM input duty cycle range is 10% to 100%.

I²C Interface

The MAX14663 uses the two-wire I²C interface to communicate with the host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions.

I²C Addresses

The MAX14663 appears as three separate I²C devices on the bus to simplify code reuse of drivers designed for existing ModelGauge™ based fuel gauges, the switching charger, and the cable detector. The registers for the fuel gauge are accessed through the slave address of 0110110 (0x6C for writes/0x6D for reads). The registers for the switching charger are accessed through the slave address of 0100101 (0x4A for writes and 0x4B for reads). The rest of the configuration registers are accessed through the slave address of 0101000 (0x50 for writes/0x51 for reads). Both of these address spaces are described in more detail below.

I²C Address 0101000 Register Map (Cable Detector and LED Driver)

Table 1. TOP Grid Register Map (Slave Address 0101000)

REGISTER ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0	POR	R/W
GLOBAL											
0x00	DEVICE_ID	CHIP_ID[7:0]								0x18	R
0x01	RSVD	-	-	-	-	-	-	-	-	0x00	R/W
0x02	INT	-	-	-	-	CD_DETI	CD_BSYI	CD_VBOVPI	CD_VBDETI	0x00	COR
0x03	STATUS	-	-	-	-	CD_DET	CD_BSY	CD_VBOVP	CD_VBDET	0x00	R
0x04	INTMASK	-	-	-	-	CD_DETM	CD_BSYM	CD_VBOVPM	CD_VBDETM	0x00	R/W
0x05	CD_CFG	CD_EN[1:0]		-	-	-	VB_DSC	CTH_SEL[1:0]		0x00	R/W
0x06	R_CNT1	-	-	-	-	-	R_CNT[10:8]			0x00	R
0x07	R_CNT0	R_CNT[7:0]								0x00	R

Table 1. TOP Grid Register Map (Slave Address 0101000) (continued)

REGISTER ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0	POR	R/W
CONFIGURATION											
0x08	DEBOUNCE	D_CNT[7:0]								0x80	R/W
0x09	BST_CFG	BST_EN[1:0]		-	-	BST_V[3:0]				0x00	R/W
0x0A	LED_ISTEP	-	-	-	-	-	-	LED_ISTEP[1:0]		0x01	R/W
0x0B	LED0	LED0_CFG[2:0]			LED0_I[4:0]					0x00	R/W
0x0C	LED1	LED1_CFG[2:0]			LED1_I[4:0]					0x00	R/W
0x0D	LED2	LED2_CFG[2:0]			LED2_I[4:0]					0x00	R/W
0x0E	SEAL	SEAL_CMD[7:0]								0x00	R/W
0x0F	PINS	-	-	-	KOUT	SEAL	-	MPC1_IN	MPC0_IN	0x00	R
0x10	DIAG	-	-	-	-	-	LEDLO[2:0]			0x00	R
0x11	EXTRA_CFG	BST_TMR	-	-	-	-	-	-	FG_DIS	0x00	R/W

I²C Address 0101000 Register Descriptions

Table 2. DEVICE_ID Register (0x00)

REGISTER	BIT	NAME	DESCRIPTION
0x00		**DEVICE_ID**	**Device Identification Register**
	7	CHIP_ID[7:0]	Device ID
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Table 3. INT Register (0x02)

REGISTER	BIT	NAME	DESCRIPTION
0x02		INT	**Interrupt Register** **CLEAR ON READ REGISTER, all bits are cleared after a read**
	7	-	
	6	-	
	5	-	
	4	-	
	3	CD_DETI	Cable Detection Interrupt 0 = no change 1 = CD_DET state has changed
	2	CD_BSYI	Cable Detection Busy Interrupt 0 = no change 1 = CD_BSY state has changed
	1	CD_VBOVPI	VB OVP Interrupt 0 = no change 1 = CD_VBOVP state has changed
	0	CD_VBDETI	VB Detect Interrupt 0 = no change 1 = CD_VBDET state has changed

Table 4. STATUS Register (0x03)

REGISTER	BIT	NAME	DESCRIPTION
0x03		**STATUS**	**Status Register**
	7	-	
	6	-	
	5	-	
	4	-	
	3	CD_DET	Cable Detection Status 0 = no cable detected 1 = cable present OR VB present: VB>VBuvlo AND VB<VBovlo AND VB>VBAT with long deglitch
	2	CD_BSY	Cable Detection Busy 0 = cable detection running 1 = cable detection not running
	1	CD_VBOVP	VB OVP Status 0 = VB < VBOVP 1 = VBOVP < VB
	0	CD_VBDET	VB Detect Status 0 = VB< V_{UVLO} 1 = VB> V_{UVLO}

Table 5. INTMASK Register (0x04)

REGISTER	BIT	NAME	DESCRIPTION
0x04		**INTMASK**	**Interrupt Mask Register**
	7	-	
	6	-	
	5	-	
	4	-	
	3	CD_DETM	Cable Detection Interrupt Mask 0 = mask 1 = not masked
	2	CD_BSYM	Cable Detection Busy Interrupt Mask 0 = mask 1 = not masked
	1	CD_VBOVPM	VB OVP Interrupt Mask 0 = mask 1 = not masked
	0	CD_VBDETM	VB Detect Interrupt Mask 0 = mask 1 = not masked

Table 6. CD_CFG Register (0x05)

REGISTER	BIT	NAME	DESCRIPTION
0x05		**CD_CFG**	**Cable Detection Configuration**
	7	CD_EN[1:0]	Cable Detection Enable 00 = disabled (regardless of MPC0/1) 01 = enabled (regardless of MPC0/1) 10 = enabled when MPC0 is high (regardless of MPC1) 11 = enabled when MPC1 is high (regardless of MPC0)
	6		
	5	-	
	4	-	
	3	-	
	2	VB_DSC	VB Discharge Disable. VB is discharged as at the first startup for every 250ms (only if VB is present for all of the previous 250ms). 0 = enabled 1 = disabled
	1	CTH_SEL[1:0]	Capacitance Threshold Select. CTH_SEL sets the desired capacitance thresh-old. 00 = 1st threshold (Capacitance threshold) = 20pF 01 = 2nd threshold (Capacitance threshold) = 40pF 10 = 3rd threshold (Capacitance threshold) = 60pF 11 = 4th threshold (Capacitance threshold) = 80pF
	0		

Table 7. R_CNT1 Register (0x06)

REGISTER	BIT	NAME	DESCRIPTION
0x06		**R_CNT1**	**Ramp Counter MSBs**
	7	-	
	6	-	
	5	-	
	4	-	
	3	-	
	2	R_CNT[10:8]	High Bits of Ramp Counter. R_CNT reads the number of the external clock oscillator shots in the detection time.
	1		
	0		

Table 8. R_CNT0 Register (0x07)

REGISTER	BIT	NAME	DESCRIPTION
0x07		**R_CNT0**	**Ramp Counter LSBs**
	7	R_CNT[7:0]	Low Bits of Ramp Counter. R_CNT reads the number of the external clock oscillator shots in the detection time.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Table 9. DEBOUNCE Register (0x08)

REGISTER	BIT	NAME	DESCRIPTION
0x08		**DEBOUNCE**	**VB Invalid Debounce Time**
	7	D_CNT[7:0]	Debounce Counter. D_CNT sets the number of time needed to debounce VB in the negative slope. The minimum debounce step (LSB) is 0.5ms. The default debounce time is 65ms (typ).
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Table 10. BST_CFG Register (0x09)

REGISTER	BIT	NAME	DESCRIPTION							
0x09		**BST_CFG**	**Boost Configuration Register**							
	7, 6	BST_EN[1:0]	Boost Enable							
			00	Disabled	10	Enabled when MPC0 is high				
			01	Enabled	11	Enabled when MPC1 is high				
	5	-								
	4	-								
	3, 2, 1, 0	BST_V[3:0]	Boost Output Voltage. (The boost regulator should be disabled when changing the voltage setting.)							
			0000	6V	0100	10V	1000	14V	1100	8V
			0001	7V	0101	11V	1001	15V	1101	8V
			0010	8V	0110	12V	1010	16V	1110	8V
			0011	9V	0111	13V	1011	17V	1111	8V

Table 11. LED_ISTEP Register (0x0A)

REGISTER	BIT	NAME	DESCRIPTION			
0x0A		**LED_ISTEP**	**LED Current Step Configuration**			
	7	-				
	6	-				
	5	-				
	4	-				
	3	-				
	2	-				
	1, 0	LED_ISTEP[1:0]	LED Step Current			
			00	0.6mA	10	1.2mA
			01	1.0mA	11	1.2mA

Table 12. LED0 Register (0x0B)

REGISTER	BIT	NAME	DESCRIPTION					
		LED0	**LED0 Configuration**					
0x0B		LED0_CFG[2:0]	Current Sink Configuration					
	7		000	Off	011	Controlled by internal charger status signal	110	Controlled by external MPC1 pin no filter
	6		001	On	100	Controlled by external MPC0 pin, no filter	111	Controlled by external MPC1 pin with PWM filter
	5		010	Controlled by internal cable detection signal	101	Controlled by external MPC0 pin, with PWM filter		
		LED0_I[4:0]	LED Sink Current Setting					
	4		LED_ISTEP[1:0]	00	01	10/11		
			00000	0.6mA	1.0mA	1.2mA		
	3		00001	1.2mA	2.0mA	2.4mA		
	2		00010	1.8mA	3.0mA	3.6mA		
			....					
	1		11000	15mA	25mA	30mA		
			11001	15mA	25mA	30mA		
	0		....					
			11111	15mA	25mA	30mA		

Table 13. LED1 Register (0x0C)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td></td><td></td><td>LED1</td><td colspan="6">LED1 Configuration</td></tr>
<tr><td rowspan="14">0x0C</td><td rowspan="2">7</td><td rowspan="4">LED1_CFG[2:0]</td><td colspan="6">Current Sink Configuration</td></tr>
<tr><td>000</td><td>Off</td><td>011</td><td>Controlled by internal charger status signal</td><td>110</td><td>Controlled by external MPC1 pin no filter</td></tr>
<tr><td>6</td><td>001</td><td>On</td><td>100</td><td>Controlled by external MPC0 pin, no filter</td><td>111</td><td>Controlled by external MPC1 pin with PWM filter</td></tr>
<tr><td>5</td><td>010</td><td>Controlled by internal cable detection signal</td><td>101</td><td>Controlled by external MPC0 pin, with PWM filter</td><td></td><td></td></tr>
<tr><td rowspan="3">4</td><td rowspan="10">LED1_I[4:0]</td><td colspan="6">LED Sink Current Setting</td></tr>
<tr><td>LED_ ISTEP[1:0]</td><td>00</td><td>01</td><td>10/11</td><td rowspan="9" colspan="2"></td></tr>
<tr><td>00000</td><td>0.6mA</td><td>1.0mA</td><td>1.2mA</td></tr>
<tr><td>3</td><td>00001</td><td>1.2mA</td><td>2.0mA</td><td>2.4mA</td></tr>
<tr><td rowspan="2">2</td><td>00010</td><td>1.8mA</td><td>3.0mA</td><td>3.6mA</td></tr>
<tr><td>........</td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">1</td><td>11000</td><td>15mA</td><td>25mA</td><td>30mA</td></tr>
<tr><td>11001</td><td>15mA</td><td>25mA</td><td>30mA</td></tr>
<tr><td rowspan="2">0</td><td>........</td><td></td><td></td><td></td></tr>
<tr><td>11111</td><td>15mA</td><td>25mA</td><td>30mA</td></tr>
</table>

Table 14. LED2 Register (0x0D)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td></td><td></td><td>LED2</td><td colspan="6">LED2 Configuration</td></tr>
<tr><td rowspan="14">0x0D</td><td rowspan="2">7</td><td rowspan="4">LED2_CFG[2:0]</td><td colspan="6">Current Sink Configuration</td></tr>
<tr><td>000</td><td>Off</td><td>011</td><td>Controlled by internal charger status signal</td><td>110</td><td>Controlled by external MPC1 pin no filter</td></tr>
<tr><td>6</td><td>001</td><td>On</td><td>100</td><td>Controlled by external MPC0 pin, no filter</td><td>111</td><td>Controlled by external MPC1 pin with PWM filter</td></tr>
<tr><td>5</td><td>010</td><td>Controlled by internal cable detection signal</td><td>101</td><td>Controlled by external MPC0 pin, with PWM filter</td><td></td><td></td></tr>
<tr><td rowspan="3">4</td><td rowspan="10">LED2_I[4:0]</td><td colspan="6">LED Sink Current Setting</td></tr>
<tr><td>LED_ ISTEP[1:0]</td><td>00</td><td>01</td><td>10/11</td><td colspan="2"></td></tr>
<tr><td>00000</td><td>0.6mA</td><td>1.0mA</td><td>1.2mA</td><td colspan="2" rowspan="8"></td></tr>
<tr><td>3</td><td>00001</td><td>1.2mA</td><td>2.0mA</td><td>2.4mA</td></tr>
<tr><td rowspan="2">2</td><td>00010</td><td>1.8mA</td><td>3.0mA</td><td>3.6mA</td></tr>
<tr><td>........</td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">1</td><td>11000</td><td>15mA</td><td>25mA</td><td>30mA</td></tr>
<tr><td>11001</td><td>15mA</td><td>25mA</td><td>30mA</td></tr>
<tr><td rowspan="2">0</td><td>........</td><td></td><td></td><td></td></tr>
<tr><td>11111</td><td>15mA</td><td>25mA</td><td>30mA</td></tr>
</table>

Table 15. SEAL Register (0x0E)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="9">0x0E</td><td></td><td>SEAL</td><td>SEAL Command</td></tr>
<tr><td>7</td><td rowspan="8">SEAL_CMD[7:0]</td><td rowspan="8">SEAL Command
0xA5 = Enter battery seal mode when written.
All others = Do nothing
Always reads 0x00</td></tr>
<tr><td>6</td></tr>
<tr><td>5</td></tr>
<tr><td>4</td></tr>
<tr><td>3</td></tr>
<tr><td>2</td></tr>
<tr><td>1</td></tr>
<tr><td>0</td></tr>
</table>

Table 16. PINS Register (0x0F)

REGISTER	BIT	NAME	DESCRIPTION
		PINS	
0x0F	7	-	
	6	-	
	5	-	
	4	KOUT	KOUT Output State 0 = $\overline{\text{KIN}}$ low and debounced 1 = $\overline{\text{KIN}}$ open
	3	SEAL	SEAL Input State 0 = pin low 1 = pin high
	2	-	
	1	MPC1_IN	MPC1 Input State 0 = pin low 1 = pin high
	0	MPC0_IN	MPC0 Input State 0 = pin low 1 = pin high

Table 17. DIAG Register (0x10)

REGISTER	BIT	NAME	DESCRIPTION
0x10		**PINS2**	**Current sink diagnostic**
	7	-	
	6	-	
	5	-	H: LED2 short high
	4	-	H: LED1 short high
	3	-	H: LED0 short high
	2	LEDLO[2:0]	H: LED2 open
	1		H: LED1 open
	0		H: LED0 open

Table 18. EXTRA_CFG Register (0x11)

REGISTER	BIT	NAME	DESCRIPTION
0x11		**EXTRA_CFG**	**Fuel Gauge Configuration**
	7	BST_TMR	Boost Startup Timer 0 = standard boost start-up time 1 = extended (double) boost start-up time
	6	-	
	5	-	
	4	-	
	3	-	
	2	-	
	1	-	
	0	FG_DIS	Fuel Gauge Disable 0 = fuel gauge enabled 1 = fuel gauge disabled (disconnected from BAT)

I^2C Address 0100101 Register Map (Battery Charger)

Table 19. CHG Register Map

REGISTER ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0	POR	R/W
STATUS											
0x00	CHG_ID	CHG_ID[7:0]								0x18	R
0x01	INT	-	-	THMI	ChgEn bldI	CHGE RRI	OVPI	POKI	EOCI	0x00	COR
0x02	STATUS1	-	-	THME	ChgEn bld	CHGE RR	OVP	POK	EOC	0x00	R
0x03	STATUS2	-		CHGMODE[2:0]		-		TMP[2:0]		0x00	R
CONTROL											
0x04	INTMASK	-	-	THMM	ChgEn bldM	CHGE RRM	OVPM	POKM	EOCM	0x00	R/W
0x05	CHGTMR	-	-	SCTDS	PQTDS	TopOffTime [1:0]		CHGTM [1:0]		0x07	R/W
0x06	CHGCTL	-	-	CEN_O[1:0]		-	VPQ[2:0]			0x05	R/W
0x07	CHGCV	-	-	CHGCV[5:0]						0x29	R/W
0x08	CHGCC	-	-	-	CHGCC[3:0]					0x04	R/W
0x09	CHGTRM	AUTOSTP	-	-	VRSTRT	-	ITERM[2:0]			0x81	R/W
0x0A	JEITA	JEN	-	-	-	T34FV	T12FV	T34FC	T12FC	0x8F	R/W
0x0B	FUNC	THsoft OFF	EIC_ LIM	EN_ SKIP	-	CON_ FR1	CON_ FR2	ABS_ OFF	EIN_ LIM	0x68	R/W

Note: R: read only
COR: clear on read
R/W: readable and writeable

I2C Address 0100101 Register Descriptions

Table 20. CHG_ID Register (0x00)

REGISTER	BIT	NAME	DESCRIPTION
0x00		**CHG_ID**	**Charger Identification Register**
	7	CHG_ID[7:0]	Charger ID
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Table 21. INT Register (0x01)

REGISTER	BIT	NAME	DESCRIPTION
0x01		**INT**	**Interrupt Register. CLEAR ON READ REGISTER, all bits are cleared after a read**
	7	-	
	6	-	
	5	THMI	Thermistor Temperature Zone Changed Interrupt 0 = no change 1 = interrupt (TMP[2:0] bits have changed)
	4	ChgEnbldI	Battery Charger Enabled Interrupt 0 = no change 1 = interrupt (ChgEnbld bit has changed)
	3	CHGERRI	Battery Fast-Charge Timer Expire Interrupt 0 = no change 1 = interrupt (CHGERR bit has changed)
	2	OVPI	VB Overvoltage Protection Interrupt 0 = no change 1 = interrupt (OVP bit has changed)
	1	POKI	Charger Power-OK Interrupt (occurs when VB rises above V_{UYLO}) 0 = no change 1 = interrupt (POK bit has changed)
	0	EOCI	End-of-Charge Interrupt 0 = no change 1 = interrupt (EOC bit has changed)

Table 22. status1 Register (0x02)

REGISTER	BIT	NAME	DESCRIPTION
0x02		**STATUS1**	**Status Register 1**
	7	-	
	6	-	
	5	THME	Thermistor Error 0 = no thermistor error 1 = thermistor open or shorted
	4	ChgEnbld	Indicates if battery charger is enabled. This bit does not indicate if the charger is passing current, it only indicates that the charger logic is enabled. EOC determines if charging is active. 0 = charger is not enabled 1 = charger is enabled
	3	CHGERR	Battery Fast Charging Timer Expired 0 = timer not expired 1 = timer expired
	2	OVP	VB Overvoltage Protection Trip Level Indication – Interrupt Generated for OVP Rising and Falling 0 = $V_{VB} \leq V_{OVLO}$) 1 = $V_{VB} > V_{OVLO}$) Please note that this bit is only valid when the charger is enabled. The same information is also available in the CD_VBOVP bit which is always valid.
	1	POK	Charger Power-OK Monitor 0= V_{VB} < (VB undervoltage lockout) 1 = $V_{VB} \geq$ (VB undervoltage lockout) Please note that this bit is only valid when the charger is enabled. The same information is also available in the CD_VBDET bit which is always valid.
	0	EOC	End-of-Charge Status 0 = charger is in top-off or disabled 1 = charger in prequal or fast-charge mode

Table 23. STATUS2 Register (0x03)

REGISTER	BIT	NAME	DESCRIPTION
0x03		STATUS2	**Status Register 2**
	7	-	
	6	CHGMODE[2:0]	Present Charger Mode of Operation 000 = charging disabled 001 = prequalification 010 = slow-charge constant current 011 = slow-charge constant voltage 100 = fast-charge constant current 101 = fast-charge constant voltage 110 = top off 111 = done (battery charged)
	5		
	4		
	3	-	
	2	TMP[2:0]	Battery Thermistor Temperature 000 = thermistor open 001 = TMP < 0C (T1) 010 = 0C (T1) < TMP < 10C (T2) 011 = 10C (T2) < TMP < 25C (T3) 100 = 25C (T3) < TMP < 45C (T4) 101 = 45C (T4) < TMP < 60C (T5) 110 = 60C (T5) < TMP 111 = thermistor shorted
	1		
	0		

Table 24. INTMASK Register (0x04)

REGISTER	BIT	NAME	DESCRIPTION
0x04		**INTMASK**	**Interrupt Mask Register**
	7	-	
	6	-	
	5	THMM	Thermistor Temperature Zone Change Interrupt Mask 0 = mask 1 = not masked
	4	ChgEnbldM	Battery Charger Enabled Interrupt Mask 0 = mask 1 = not masked
	3	CHGERRM	Battery Fast Charge Timer Interrupt Mask 0 = mask 1 = not masked
	2	OVPM	VB Overvoltage Protection Interrupt Mask 0 = mask 1 = not masked
	1	POKM	Charger Power-OK Interrupt Mask 0 = mask 1 = not masked
	0	EOCM	End-of-Charge Interrupt Mask 0 = mask 1 = not masked

Table 25. CHGTMR Register (0x05)

REGISTER	BIT	NAME	DESCRIPTION
0x05		**CHGTMR**	**Charger Timimg Set Register**
	7	-	
	6	-	
	5	SCTDS	Slow-Charge Timer Disable (The timer for slow charge is the same as fast charge.) 0 = timer active during slow charge 1 = timer disabled during slow charge
	4	PQTDS	Pre-Qualification Timer Disable (FIXED TIME = 60 minutes) 0 = prequalification timer enabled 1 = prequalification timer disabled
	3	TopOffTime[1:0]	Top Off Timer Setting 00 = timer disabled 01 = 1 minute 10 = 10 minutes 11 = 30 minutes
	2		
	1	CHGTM[1:0]	Charger Elapsed Timer Setting 00 = timer disabled 01 = 2.5hrs 10 = 5hrs 11 = 10hrs
	0		

Table 26. CHGCTL Register (0x06)

REGISTER	BIT	NAME	DESCRIPTION
0x06		**CHGCTL**	**Charger Control Register**
	7	-	
	6	-	
	5	CEN_O[1:0]	Charger Enable 00 = disabled 01 = enabled 10 = enabled when MPC0 pin is high 11 = enabled
	4		
	3	-	
	2	VPQ[2:0]	Prequalification Voltage Threshold 000 = 2.4V 001 = 2.5V 010 = 2.6V 011 = 2.7V 100 = 2.8V 101 = 2.9V 110 = 3.0V 111 = 3.1V
	1		
	0		

Table 27. CHGCV Register (0x07)

REGISTER	BIT	NAME	DESCRIPTION					
		CHGCV	**Charger Constant Voltage Setting**					
0x07			**CHGV[1:0]**					
					11	**10**	**01**	**00**
	7	-	CHGCV[5:2]	**0000**	3.5V	3.5V	3.5V	3.5V
				0001	3.52V	3.5V	3.5V	3.5V
	6	-		**0010**	3.60V	3.58V	3.56V	3.54V
				0011	3.68V	3.66V	3.64V	3.62V
	5	CHGCV[5:0]		**0100**	3.76V	3.74V	3.72V	3.70V
				0101	3.84V	3.82V	3.80V	3.78V
	4			**0110**	3.92V	3.90V	3.88V	3.86V
				0111	4.00V	3.98V	3.96V	3.94V
	3			**1000**	4.08V	4.06V	4.04V	4.02V
				1001	4.16V	4.14V	4.12V	4.10V
	2			**1010**	4.24V	4.22V	4.20V	4.18V
				1011	4.32V	4.30V	4.28V	4.26V
	1			**1100**	4.40V	4.38V	4.36V	4.34V
				1101	4.40V	4.40V	4.40V	4.40V
	0			**1110**	4.40V	4.40V	4.40V	4.40V
				1111	4.40V	4.40V	4.40V	4.40V

Table 28. CHGCC Register (0x08)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="10">DESCRIPTION</th></tr>
<tr><td></td><td></td><td>CHGCC</td><td colspan="10">Fast-Charge Constant Current Limit. Set to maximum allowable battery charge current.</td></tr>
<tr><td rowspan="11"></td><td>7</td><td>-</td><td colspan="10"></td></tr>
<tr><td>6</td><td>-</td><td colspan="10"></td></tr>
<tr><td>5</td><td>-</td><td colspan="10"></td></tr>
<tr><td>4</td><td>-</td><td colspan="10"></td></tr>
<tr><td rowspan="3">3</td><td rowspan="7">CHGCC[3:0]</td><td colspan="2" rowspan="3"></td><td colspan="8">CHGCC[1:0]</td></tr>
<tr><td colspan="2">11</td><td colspan="2">10</td><td colspan="2">01</td><td colspan="2">00</td></tr>
<tr><td>Rs = 50 mΩ</td><td>Rs = 100 mΩ</td><td>Rs = 50 mΩ</td><td>Rs = 100 mΩ</td><td>Rs = 50 mΩ</td><td>Rs = 100 mΩ</td><td>Rs = 50 mΩ</td><td>Rs = 100 mΩ</td></tr>
<tr><td rowspan="2">2</td><td rowspan="4">CHGCC [3:2]</td><td>00</td><td>150mA</td><td>75mA</td><td>100mA</td><td>50mA</td><td>100mA</td><td>50mA</td><td>100mA</td><td>50mA</td></tr>
<tr><td>01</td><td>350mA</td><td>175mA</td><td>300mA</td><td>150mA</td><td>250mA</td><td>125mA</td><td>200mA</td><td>100mA</td></tr>
<tr><td>1</td><td>10</td><td>550mA</td><td>275mA</td><td>500mA</td><td>250mA</td><td>450mA</td><td>225mA</td><td>400mA</td><td>200mA</td></tr>
<tr><td>0</td><td>11</td><td>750mA</td><td>375mA</td><td>700mA</td><td>350mA</td><td>650mA</td><td>325mA</td><td>600mA</td><td>300mA</td></tr>
</table>

Table 29. CHGTRM Register (0x09)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td rowspan="10">0x09</td><td></td><td>CHGTRM</td><td colspan="8">Charger Termination Control Register</td></tr>
<tr><td>7</td><td>AUTOSTP</td><td colspan="8">Enable battery charge automatically stops and restarts after EOC.
0 = always charge when enabled (the state machine remains in the “TOP OFF” box after fast charge)
1 = stop and start based on register settings
(Note: When charger reaches end-of-charge with AUTOSTP enabled, there is a 1.8mA (typ) load on the battery, which powers some of the internal battery charger control circuits.)</td></tr>
<tr><td>6</td><td>-</td><td colspan="8"></td></tr>
<tr><td>5</td><td>-</td><td colspan="8"></td></tr>
<tr><td>4</td><td>VRSTRT</td><td colspan="8">Restart Voltage Threshold
0 = 135mV below CHGCV setting
1 = 214mV below CHGCV setting</td></tr>
<tr><td>3</td><td>-</td><td colspan="8"></td></tr>
<tr><td rowspan="2">2</td><td rowspan="4">ITERM[2:0]</td><td colspan="8">Termination current setting in mA (Rs=50mΩ/Rs=100mΩ)</td></tr>
<tr><td>000</td><td>25 / 12.5</td><td>011</td><td>100 / 50</td><td>110</td><td>250 / 125</td><td></td><td></td></tr>
<tr><td>1</td><td>001</td><td>50 / 25</td><td>100</td><td>150 / 75</td><td>111</td><td>300 /150</td><td></td><td></td></tr>
<tr><td>0</td><td>010</td><td>75 / 37.5</td><td>101</td><td>200 / 100</td><td></td><td></td><td></td><td></td></tr>
</table>

Table 30. JEITA Register (0x0A)

REGISTER	BIT	NAME	DESCRIPTION
		JEITA	**JEITA Control Register**
0x0A	7	JEN	JEITA Enable. The default value can be set by OTP 0 = no thermistor based control 1 = charger disabled below T1 and above T4 and behaves as specified below
	6	-	
	5	-	
	4	-	
	3	T34FV	T3-T4 Float Voltage when temperature between T3 and T4 0 = CHGCV – 120mV 1 = CHGCV
	2	T12FV	T1-T2 Float Voltage when temperature between T1 and T2 0 = CHGCV – 120mV 1 = CHGCV
	1	T34FC	T3-T4 Fast charge current limit when temperature between T3 and T4 0 = MAX(CHGCC/2,50mA); if CHGCC->100mA for JEITA the fast charge timeout is suspended. If CHGCC = 50mA, I_{FAST} charge goes to zero between T3 and T4. 1 = CHGCC
	0	T12FC	T1-T2 Fast charge current limit when temperature between T1 and T2 0 = MAX(CHGCC/2,50mA)); if CHGCC->100mA for JEITA the fast charge timeout is suspended. If CHGCC = 50mA, I_{FAST} charge goes to zero between T1 and T2. 1 = CHGCC

Table 31. FUNC Register (0x0B)

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="11">0x0B</td><td></td><td>FUNC</td><td colspan="4">Charger Function Control Register</td></tr>
<tr><td>7</td><td>THsoftOFF</td><td colspan="4">Soft Thermal Shutdown Disable
0 = soft thermal shutdown enabled
1 = disable soft thermal shutdown</td></tr>
<tr><td>6</td><td>EIC_LIM</td><td colspan="4">Charge-Current Control Limit Enable
0 = charge-current control limit disabled
1 = charge-current control limit enabled</td></tr>
<tr><td>5</td><td>EN_SKIP</td><td colspan="4">Skip Mode Enable
0 = charger skip mode disabled
1 = charger skip mode enabled</td></tr>
<tr><td>4</td><td>-</td><td colspan="4"></td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">CON_FR1</td><td rowspan="3">Duty-cycle frequency dependence disable</td><td>FR1</td><td>FR2</td><td></td></tr>
<tr><td>0</td><td>0</td><td>Fsw at 50% duty = 1.1MHz
Constant ripple mode</td></tr>
<tr><td>0</td><td>1</td><td>Fsw at 50% duty = 700kHz
Constant ripple mode</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">CON_FR2</td><td rowspan="2">Icharge frequency dependence disable</td><td>1</td><td>0</td><td>Fsw at =1.1MHz</td></tr>
<tr><td>1</td><td>1</td><td>Fsw =700kHz</td></tr>
<tr><td>1</td><td>ABS_OFF</td><td colspan="4">Safety charge-pump mode enable</td></tr>
<tr><td></td><td>0</td><td colspan="5">–</td></tr>
</table>

I2C Address 0110110 Register Map (Fuel Gauge)

Register Summary

All registers must be written and read as 16-bit words; 8-bit writes cause no effect. Any bits marked X (don't care) or read only must be written with the rest of the register, but the value written is ignored by the IC. The values read from don't care bits are undefined. Calculate the register's value by multiplying the 16-bit word by the register's LSb value, as shown in Table 33.

VCELL Register (0x02)

The MAX14663 measures VCELL between the VDD and GND pins. VCELL is the average of four ADC conversions. The value updates every 250ms in active mode and every 45s in hibernate mode.

SOC Register (0x04)

The ICs calculate SOC using the ModelGauge algorithm. This register automatically adapts to variation in battery size since ModelGauge naturally recognizes relative SOC.

The upper byte least-significant bit has units of 1%. The lower byte provides additional resolution.

The first update is available approximately 1s after POR of the IC. Subsequent updates occur at variable intervals depending on application conditions.

Table 32. MDGG Register Map

ADDRESS	REGISTER NAME	16-BIT LSb	DESCRIPTION	READ/WRITE	DEFAULT
0x02	VCELL	78.125µV/cell	ADC measurement of VCELL.	R	—
0x04	SOC	1%/256	Battery state of charge.	R	—
0x06	MODE	—	Initiates quick-start, reports hibernate mode, and enables sleep mode.	W	0x0000
0x08	VERSION	—	IC production version.	R	0x001_
0x0A	HIBRT	—	Controls thresholds for entering and exiting hibernate mode.	R/W	0x8030
0x0C	CONFIG	—	Compensation to optimize performance, sleep mode, alert indicators, and configuration.	R/W	0x971C
0x14	VALRT	—	Configures the VCELL range outside of which alerts are generated.	R/W	0x00FF
0x16	CRATE	0.208%/hr	Approximate charge or discharge rate of the battery.	R	—
0x18	VRESET/ID	—	Configures VCELL threshold below which the IC resets itself, ID is a one-time factory-programmable identifier.	R/W	0x96__
0x1A	STATUS	—	Indicates overvoltage, undervoltage, SOC change, SOC low, and reset alerts.	R/W	0x01__
0x40 to 0x7F	TABLE	—	Configures battery parameters.	W	—
0xFE	CMD	—	Sends POR command.	R/W	0xFFFF

MODE Register (0x06)

The MODE register allows the system processor to send special commands to the IC (see Figure 3).

- **Quick-Start** generates a first estimate of OCV and SOC based on the immediate cell voltage. Use with caution; see the Quick-Start section·
- **EnSleep** enables sleep mode. See the Sleep Mode section.
- **HibStat** indicates when the IC is in hibernate mode (read only).

VERSION Register (0x08)

The value of this read-only register indicates the production version of the IC.

HIBRT Register (0x0A)

To disable hibernate mode, set HIBRT = 0x0000. To always use hibernate mode, set HIBRT = 0xFFFF (see Figure 4).

- **ActThr** (active threshold): If at any ADC sample |OCV-CELL| is greater than ActThr, the IC exits hibernate mode. 1 LSb = 1.25mV.
- **HibThr** (hibernate threshold). If the absolute value of CRATE is less than HibThr for longer than 6min, the IC enters hibernate mode. 1 LSb = 0.208%/hr.

CONFIG Register (0x0C)

See Figure 5.

- **RCOMP** is an 8-bit value that can be adjusted to optimize IC performance for different lithium chemistries or different operating temperatures. Contact Maxim for instructions for optimization. The POR value of RCOMP is 0x97.
- **SLEEP** forces the IC in or out of sleep mode if Mode.EnSleep is set. Writing 1 forces the IC to enter sleep mode, and 0 forces the IC to exit. The POR value of SLEEP is 0.

MSB—ADDRESS 0x06

MSb							LSb
X	Quick-Start	EnSleep	HibStat	X	X	X	X

LSB—ADDRESS 0x07

MSb							LSb
X	X	X	X	X	X	X	X

Figure 3. Mode Register Format

MSB (HibThr)—ADDRESS 0x0A

MSb							LSb
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

LSB (ActThr)—ADDRESS 0x0B

MSb							LSb
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

HibThr 2^0 UNIT: 0.208%/hr
ActThr 2^0 UNIT: 1.25mV

Figure 4. HIBRT Register Format

- **ALSC** (SOC change alert) enables alerting when SOC changes by at least 1%. Each alert remains until STATUS.SC is cleared, after which the alert automatically clears until SOC again changes by 1%. Do not use this alert to accumulate changes in SOC.
- **ALRT** (alert status bit) is set by the IC when an alert occurs. When this bit is set, the ALRT pin asserts low. Clear this bit to service and deassert the ALRT pin. The power-up default value for ALRT is 0. The STATUS register specifies why the ALRT pin was asserted.
- **ATHD** (empty alert threshold) sets the SOC threshold, where an interrupt is generated on the ALRT pin and can be programmed from 1% up to 32%. The value is (32 - ATHD)% (e.g., 00000b à 32%, 00001b à 31%, 00010b à 30%, 11111b à 1%). The POR value of ATHD is 0x1C, or 4%. The alert only occurs on a falling edge past this threshold.

VALRT Register (0x14)

This register is divided into two thresholds: Voltage alert maximum (VALRT.MAX) and minimum (VALRT.MIN). Both registers have 1 LSb = 20mV. The IC alerts while VCELL > VALRT.MAX or VCELL < VALRT.MIN (see Figure 6).

CRATE Register (0x16)

The IC calculates an approximate value for the average SOC rate of change. 1 LSb = 0.208% per hour (not for conversion to ampere).

VRESET/ID Register (0x18)

See Figure 7.

- **ID** is an 8-bit read-only value that is one-time programmable at the factory, which can be used as an identifier to distinguish multiple cell types in production. Writes to these bits are ignored.

MSB (RCOMP)—ADDRESS 0x0C

RCOMP 7	RCOMP 6	RCOMP 5	RCOMP 4	RCOMP 3	RCOMP 2	RCOMP 1	RCOMP 0
MSb							LSb

LSB—ADDRESS 0x0D

SLEEP	ALSC	ALRT	ATHD 4	ATHD 3	ATHD 2	ATHD 1	ATHD 0
MSb							LSb

Figure 5. CONFIG Register Format

MSB (VALRT.MIN)—ADDRESS 0x14

MIN^7	MIN^6	MIN^5	MIN^4	MIN^3	MIN^2	MIN^1	MIN^0
MSb							LSb

LSB (VALRT.MAX)—ADDRESS 0x15

MAX^7	MAX^6	MAX^5	MAX^4	MAX^3	MAX^2	MAX^1	MAX^0
MSb							LSb

UNIT: 20mV

Figure 6. VALRT Register Format

MSB (VRESET)—ADDRESS 0x18

2^7	2^6	2^5	2^4	2^3	2^2	2^1	Dis
MSb							LSb

LSB (ID)—ADDRESS 0x19

ID^6	ID^5	ID^4	ID^3	ID^2	ID^1	ID^0	ID
MSb							LSb

VRESET 2^0 UNITS: 40mV

Figure 7. VRESET/ID Register Format

- **VRESET[7:1]** adjusts a fast analog comparator and a slower digital ADC threshold to detect battery removal and reinsertion. For captive batteries, set to 2.5V. For removable batteries, set to at least 300mV below the application's empty voltage, according to the desired reset threshold for your application. If the comparator is enabled, the IC resets 1ms after VCELL rises above the threshold. Otherwise, the IC resets 250ms after the VCELL register rises above the threshold.
- **Dis.** Set Dis = 1 to disable the analog comparator in hibernate mode to save approximately 0.5μA

STATUS Register (0x1A)

An alert can indicate many different conditions. The STATUS register identifies which alert condition was met. Clear the corresponding bit after servicing the alert (see Figure 8).

Reset Indicator:

- **RI** (reset indicator) is set when the device powers up. Any time this bit is set, the IC is not configured, so the model should be loaded and the bit should be cleared.

Alert Descriptors:

These bits are set only when they cause an alert (e.g., if CONFIG.ALSC = 0, then SC is never set).

- **VH** (voltage high) is set when VCELL has been above ALRT.VALRTMAX.
- **VL** (voltage low) is set when VCELL has been below ALRT.VALRTMIN.
- **VR** (voltage reset) is set after the device has been reset regardless of EnVr.
- **HD** (SOC low) is set when SOC crosses the value in CONFIG.ATHD.
- **SC** (1% SOC change) is set when SOC changes by at least 1% if CONFIG.ALSC is set.

Enable or Disable VRESET Alert:

- **EnVr** (enable voltage reset alert) when set to 1 asserts the ALRT pin when a voltage-reset event occurs under the conditions described by the VRESET/ID register.

TABLE Registers (0x40 to 0x7F)

Contact Maxim for details on how to configure these registers. The default value is appropriate for some Li+ batteries.

To unlock the TABLE registers, write 0x57 to address 0x3F, and 0x4A to address 0x3E. While TABLE is unlocked, no ModelGauge registers are updated, so relock as soon as possible by writing 0x00 to address 0x3F, and 0x00 to address 0x3E.

CMD Register (0xFE)

Writing a value of 0x5400 to this register causes the device to completely reset as if power had been removed (see the Power-On Reset (POR) section). The reset occurs when the last bit has been clocked in. The IC does not respond with an I2C ACK after this command sequence.

MSB—ADDRESS 0x1A

MSb							LSb
X	EnVR	SC	HD	VR	VL	VH	RI

LSB—ADDRESS 0x1B

MSb							LSb
X	X	X	X	X	X	X	X

Figure 8. STATUS Register Format

Table 33. CMD Register (0xFF)

REGISTER	BIT	NAME	DESCRIPTION
0xFF		**CMD**	**Command Register LSB**
	7	CMD[7:0]	
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14663ETL+	-40ºC to +85ºC	40 TQFN –EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN	T4055+1	21-0140	90-0016

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/13	Initial release	—
1	1/15	Updated page 1 content	1
2	7/16	Updated ambiguous charge current capability	1, 3, 6, 8–11, 15, 21, 27–29, 40
3	10/16	Corrected typo in T3 Jetta Thermistor Falling Temperature spec in *Electrical Characteristics* table	8
4	1/17	Corrected incorrect temperature compensation calculation and typo in *Model Gauge* section	17, 18, 44
5	3/17	Updated *Typical Operating Circuit/Functional Diagram*, *Electrical Characteristics* table, deleted Table 3, and made various text updates	2, 10, 15, 19, 20, 22, 38
6	8/20	Updated the *Benefits and Features, Electrical Characteristics, Pin Description,* and *Battery Isolation Switch* sections	1, 10–11, 14, 19