36V_{IN}, 12A Step-Up/Step-Down Buck-Boost µModule Regulator

FEATURES

- **Complete Buck-Boost Switch Mode Power Supply**
- **V_{OUT} Equal, Greater, Less Than V_{IN}**
- **Wide Input Voltage Range: 5V to 36V**
- **Wide Output Voltage Range: 1V to 36V**
- **12A in Buck and Buck-Boost Mode, 6A under 12V_{IN} and 24V_{OUT}**
- **Up to 98% Efficiency**
- **Peak Current Mode Control**
- **Adjustable Input or Output Average Current Limits**
- Input or Output Current Monitoring
- Power Good Output Signal
- Parallelable for Increased Output Current
- Phase-Lockable Fixed Frequency: 100kHz to 600kHz
- Selectable Forced Continuous/Pulse-Skipping Modes
- V_{OUT} is Disconnected from V_{IN} During Shutdown
- 16mm ×16mm × 8.34mm BGA Package

APPLICATIONS

- Telecom, Servers and Networking Equipment
- Industrial Control
- High Power Battery-Operated Devices

DESCRIPTION

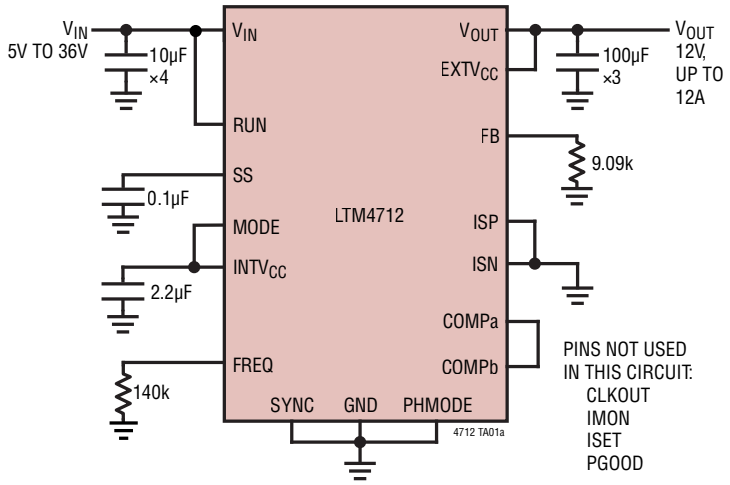
The LTM®4712 is a high efficiency buck-boost µModule® (micromodule) regulator. The switching controller, power switches, inductor and support components are included in the package. The complete design requires only a few external components, including a resistor to set frequency, a resistor to set output voltage, input, and output capacitors, a sensing resistor to achieve input or output average current regulation. The LTM4712 operates over a 5V to 36V input voltage range and can regulate output voltages between 1V and 36V.

The LTM4712 supports selectable forced continuous mode (FCM)/pulse-skipping mode (PSM) operation. The current mode control enables a fast transient response to line and load changes without sacrificing stability. The SYNC input and CLKOUT output allow easy synchronization. It supports multi-phase parallel operation for high power applications.

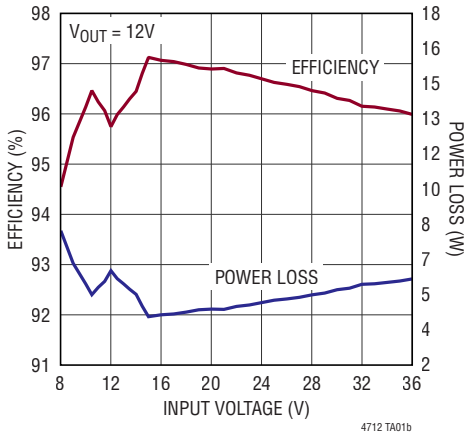
The LTM4712 is offered in a 16mm × 16mm × 8.34mm ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM4712 is RoHS-compliant.

TYPICAL APPLICATION

12V_{OUT} from 5V_{IN} to 36V_{IN} Buck-Boost Regulator



Efficiency and Power Loss vs V_{IN}



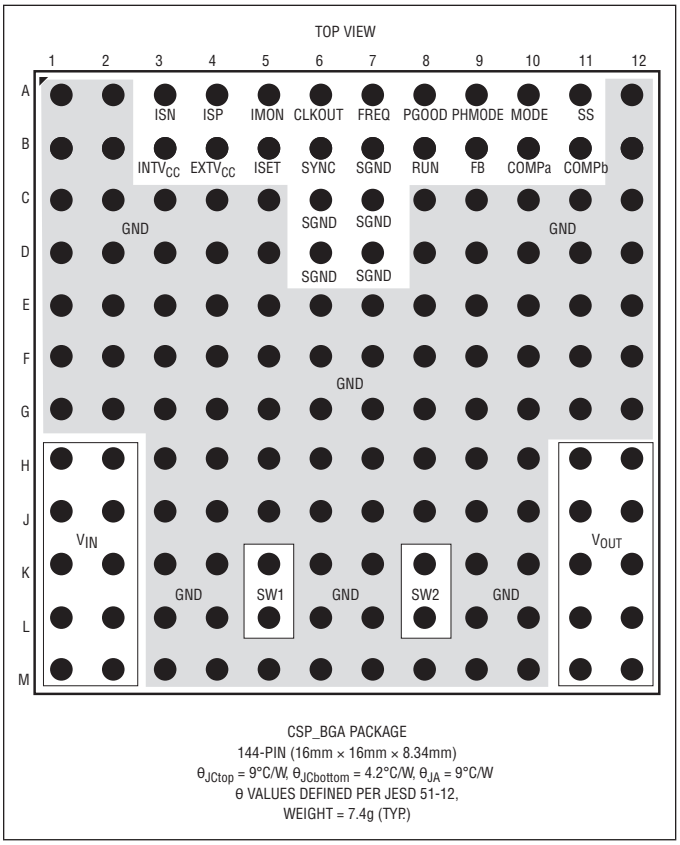
Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT}, ISP, ISN, $EXTV_{CC}$ ..... –0.3V to 38V
SW1, SW2 ..... –0.3V to 38V
RUN ..... –0.3V to 12V
$INTV_{CC}$, PGOOD ..... –0.3V to 6V
PHMODE, ISET, IMON, FB ..... –0.3V to $INTV_{CC}$
MODE, SS, COMPa, COMPb ..... –0.3V to $INTV_{CC}$
FREQ, SYNC, CLKOUT ..... –0.3V to $INTV_{CC}$
Maximum Junction Temperature
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

PIN CONFIGURATION



CSP_BGA PACKAGE
144-PIN (16mm × 16mm × 8.34mm)
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 4.2°C/W, θ_{JA} = 9°C/W
θ VALUES DEFINED PER JESD 51-12,
WEIGHT = 7.4g (TYP)

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH*	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4712EY#PBF	SAC305 (RoHS)	LTM4712Y	e1	BGA	4	–40°C to 125°C
LTM4712IY#PBF	SAC305 (RoHS)	LTM4712Y	e1	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- This product is not recommended for second side reflow.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 5V unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	5		36	V
Output Voltage Range	(Note 4)	●	1		36	V
Output DC Voltage	R_{FB} = Open R_{FB} = 9.09k			1 12		V V
Output DC Current Range (Note 5)	V_{IN} = 5V, V_{OUT} = 12V, 400kHz V_{IN} = 12V, V_{OUT} = 12V, 400kHz			6 12		A A
Quiescent Current Into V_{IN}, V_{IN} = 12V, V_{OUT} = 12V	RUN = 0V (Disabled) RUN = 0.9V (Standby) No load, MODE = OPEN (PSM) No load, MODE=0V Forced Continuous Mode (FCM)			80 2.5 40 55		µA mA mA mA
Voltage at FB Pin	Forced Continuous Mode (FCM)	 ●	0.99 0.98	1	1.01 1.02	V V
Resistor Between V_{OUT} and FB Pins				100		kΩ
Output Voltage Line Regulation	5V ≤ V_{IN} ≤ 36V, V_{OUT} = 12V, I_{OUT} = 10mA, FCM , 400kHz	●		0.02	0.1	%/V
Output Voltage Load Regulation	V_{IN} = 12V, V_{OUT} = 12V, 10mA < I_{OUT} < 12A, FCM , 400kHz	 ●			0.5 0.8	% %
Input Undervoltage Lockout	V_{IN} Rising V_{IN} Falling			4.6 4.4		V v
$INTV_{CC}$ Regulation Voltage	V_{IN} = 6V to 36V		4.8	5		V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 10mA, V_{IN} = 12V			0.3		%
Switching Frequency	R_T = 58k R_T = 140k (Recommended) R_T = 200k			100 400 600		kHz kHz kHz
FREQ Pin Output Current			9	10	11	µA
RUN Pin Falling Threshold	RUN Pin Threshold 1 (Shutdown to Standby) RUN Pin Threshold 2 (Standby to ON)	●	0.4 1.1	0.55 1.2	0.7 1.3	V V
RUN Pin Current	RUN = 1V RUN = 1.6V			2 6		µA µA
Soft-Start Charging Current				2.5		µA
ISP Pin Input Current	V_{ISP} = V_{ISN} = 12V, V_{ISP} – V_{ISN} = 50 mV			14		µA
ISN Pin Input Current	V_{ISP} = V_{ISN} = 12V, V_{ISP} – V_{ISN} = 50 mV			14		µA
Average Current Sense Amplifier Output	V_{ISP} –V_{ISN} = 0mV V_{ISP} –V_{ISN} = 50mV			200 1200		mV mV
ISET Pin Output Current			14	15	16	µA
PGOOD Leakage Current	V_{PGOOD} = 6.0V				±1	µA
PGOOD Trip Level, V_{FB} Respect to Set Regulated Voltage	V_{FB} Ramping Negative V_{FB} Ramping Positive			–10 10		% %
CLKOUT Output High			4.8	5		V
CLKOUT Output Low					0.2	V
$EXTV_{CC}$ Threshold	$EXTV_{CC}$ Threshold Rising $EXTV_{CC}$ Threshold Falling			7.7 7.2		V V
SYNC Input High Threshold	SYNC Pin Rising SYNC Pin Falling			1.35 1		V V
Synchronizable Frequency	SYNC = External Clock		100		600	kHz

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4712 is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTM4712E is guaranteed to meet performance specifications from 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4712I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance.

Note 3: The LTM4712 contains overtemperature protection that is intended to protect the device during momentary overload conditions. The internal temperature exceeds the maximum operating junction temperature when the overtemperature protection is active.

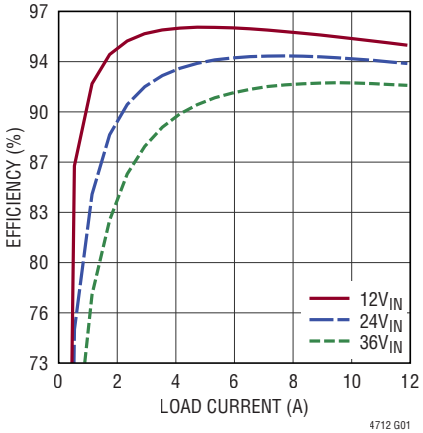
Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Output voltage lower than 7V requires minimum input voltage of 7V.

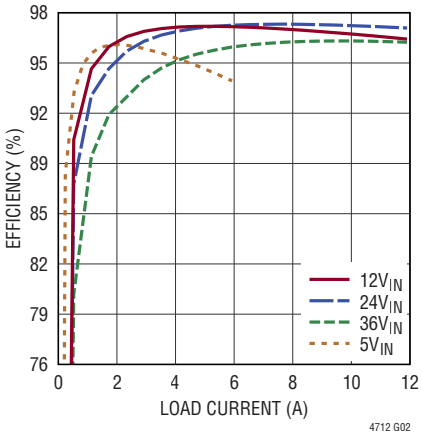
Note 5: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

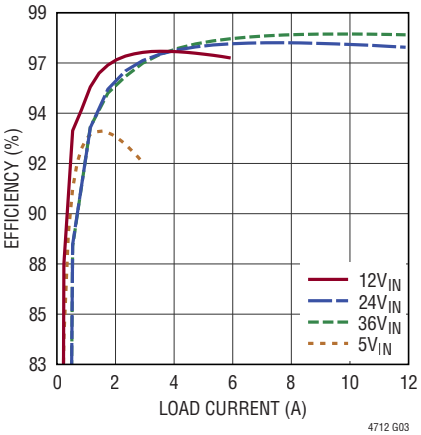
5V_{OUT} Efficiency, 400kHz, FCM



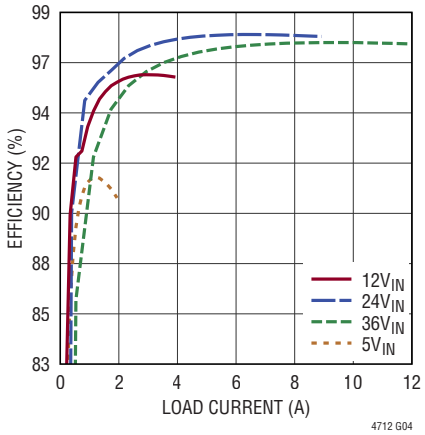
12V_{OUT} Efficiency, 400kHz, FCM



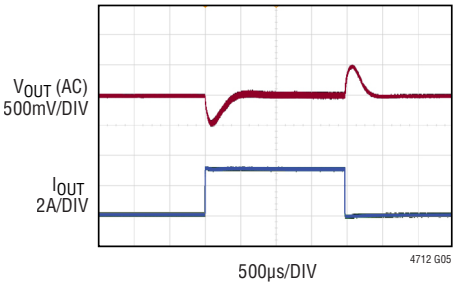
24V_{OUT} Efficiency, 400kHz, FCM



36V_{OUT} Efficiency, 400kHz, FCM

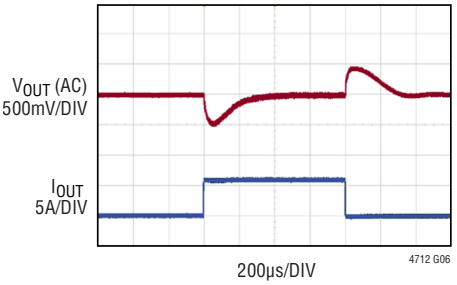


Transient Response, 5V_{IN} to 12V_{OUT}



f_{SW} = 400kHz

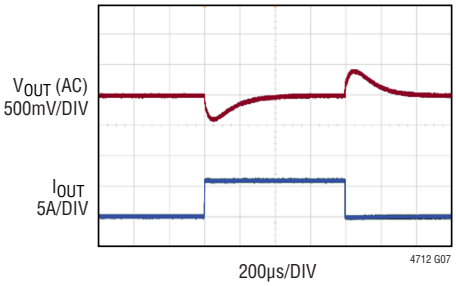
Transient Response, 12V_{IN} to 12V_{OUT}



f_{SW} = 400kHz

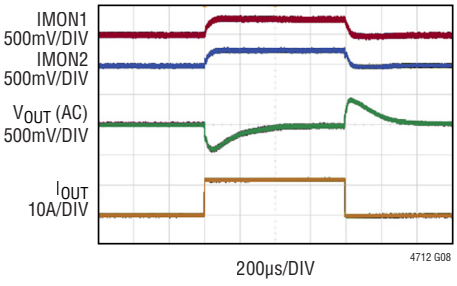
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response, 36V_{IN} to 12V_{OUT}



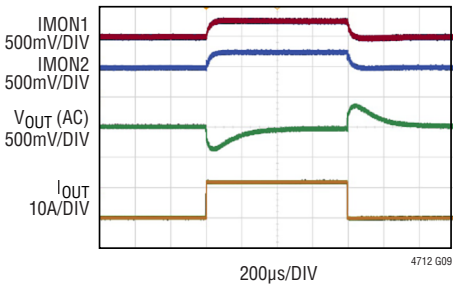
f_{SW} = 400kHz

Two-Phase Parallel Operation Load Step (12V_{IN}, 12V_{OUT})



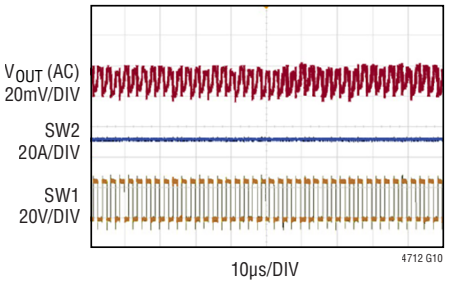
f_{SW} = 400kHz

Two-Phase Parallel Operation Load Step (12V_{IN}, 12V_{OUT})



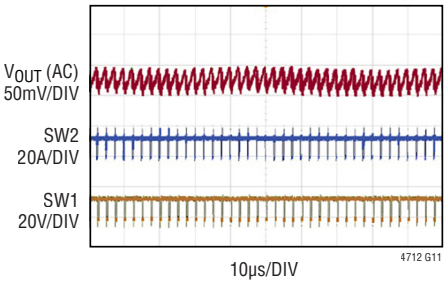
f_{SW} = 400kHz

Switching Waveforms (Buck Region)



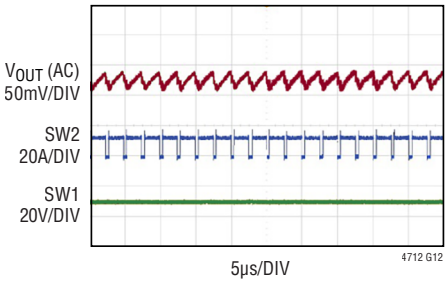
V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 12A,
f_{SW} = 400kHz

Switching Waveforms (Buck-Boost Region)



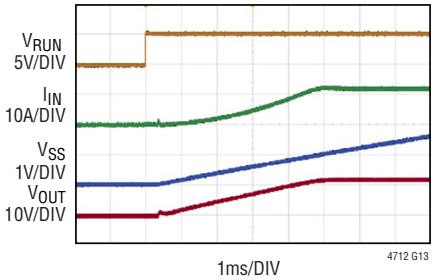
V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 12A,
f_{SW} = 400kHz

Switching Waveforms (Boost Region)



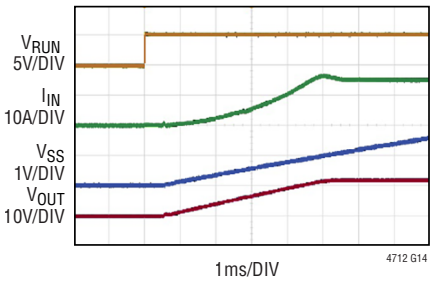
V_{IN} = 10V, V_{OUT} = 12V, I_{OUT} = 6A,
f_{SW} = 400kHz

Start-Up with 5V_{IN} to 12V_{OUT}, FCM



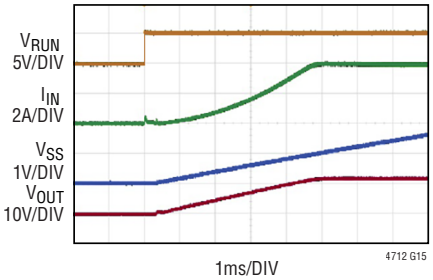
I_{OUT} = 6A
f_{SW} = 400kHz
C_{SS} = 10nF

Start-Up with 12V_{IN} to 12V_{OUT}, FCM



I_{OUT} = 12A
f_{SW} = 400kHz
C_{SS} = 10nF

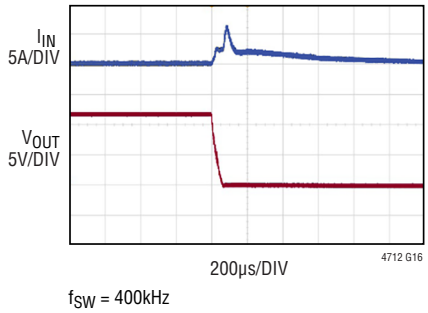
Start-Up with 36V_{IN} to 12V_{OUT}, FCM



I_{OUT} = 12A
f_{SW} = 400kHz
C_{SS} = 10nF

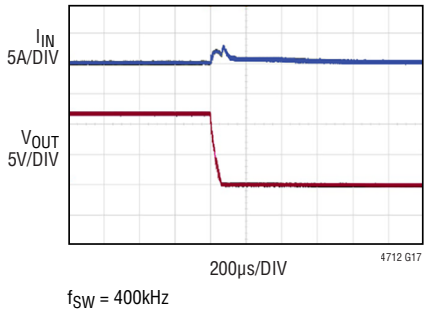
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit with $5V_{IN}$ to $12V_{OUT}$, No Load



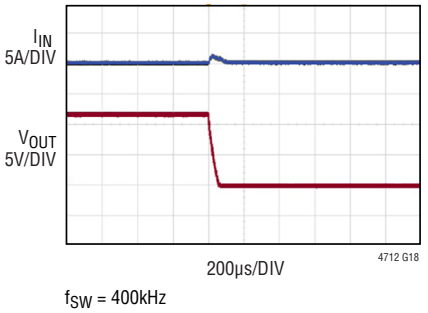
f_{SW} = 400kHz

Short-Circuit with $12V_{IN}$ to $12V_{OUT}$, No Load



f_{SW} = 400kHz

Short-Circuit with $36V_{IN}$ to $12V_{OUT}$, No Load



f_{SW} = 400kHz

PIN FUNCTIONS

GND (Pins A1-G1, A2-G2, C3-M3, C4-M4, C5-J5, M5, E6-M6, E7-M7, C8-J8, M8, C9-M9, C10-M10, C11-G11, A12-G12): Tie these GND pins to a local ground plane below the LTM4712 and the circuit components. In most applications, the bulk of the heat flow out of the LTM4712 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations and Output Current Derating sections for more details.

ISP, ISN (Pins A3, A4): Average Current Sensing Pins. The positive/negative inputs of the internal rail-to-rail average current sense amplifier.

IMON (Pin A5): Input or Output Current Monitor. This feature is generally useful only if a current sense resistor is placed on input or output. ISP needs to be connected to the positive side, while ISN on the negative side. This pin produces a voltage that is proportional to the voltage across the sense resistor. IMON will equal 1.2V when $V_{ISP} - V_{ISN}$ = 50mV.

CLKOUT (Pin A6): Clock Output. Use this pin as a clock source when synchronizing other devices to the switching frequency of the LTM4712. When this function is not used, leave this pin open. See the Applications Information section for detailed parallel configuration.

FREQ (Pin A7): Frequency Set Pin. A resistor between this pin and SGND sets the switching frequency. This pin sources 10µA current.

PGOOD (Pin A8): Power Good Indicator Output for the Regulated Output Voltage. Open-drain logic out is pulled down to ground when the regulated output voltage exceeds ±10% regulation window with the internal 30µs delay.

PHMODE (Pin A9): Phase Mode Program Pin. This pin sets the phase relationship between the internal oscillator clock and the output clock on the CLKOUT pin. Tying this pin to SGND sets 180° phase shift, floating this pin sets 120° phase shift and tying this pin to $INTV_{CC}$ sets 90°phase shift. See the Applications Information section for details.

MODE (Pin A10): Forced Continuous Mode (FCM) and Pulse-Skipping Mode. Tying this pin to GND enables FCM operation, otherwise the controller works in the pulse-skipping mode when MODE pin is floated. Do not tie to $INTV_{CC}$ or other voltage source. See the Applications Information section for details.

SS (Pin A11): Soft-Start. Connect a capacitor from this pin to GND to increase the soft-start time. Soft-start reduces the input power source's surge current by gradually increasing the controller's current limit. Larger values of the soft-start capacitor result in longer soft-start times. See the Applications Information section.

PIN FUNCTIONS

$INTV_{CC}$ (Pin B3): Internal 5V Regulator Output of the Switching Mode Regulator Channel. The internal control circuits are powered from this voltage. The LTM4712 has an internal 2.2µF decoupling capacitor connecting to SGND.

$EXTV_{CC}$ (Pin B4): External Power Input to an Internal LDO powering the gate driver. When the voltage on this pin is greater than 8V and lower than the V_{IN} pin voltage, this LDO bypasses the internal LDO powered from V_{IN}. The LTM4712 has an internal 0.1µF decoupling capacitor.

ISET (Pin B5): Average Current Regulation Pin. A resistor from this pin to SGND sets the maximum average input or output current sensed by the ISP and ISN pins. This pin sources 15µA current. See the Applications Information section.

SYNC (Pin B6): External Synchronization Input. The SYNC pin has an internal pull-down resistor. See the Operating Frequency Selection and Phase-Locked Loop (FREQ, SYNC, PHMODE and CLKOUT Pins) section in Applications Information for details. Tie this pin to GND when not used.

RUN (Pin B8): Enable Control Input. A voltage above 1.22V turns on the IC. There is a 2µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold, the pull-up increases to 6µA.

FB (Pin B9): The Negative Input of the Error Amplifier for the Switching Mode Regulator. This pin is internally connected to V_{OUT} with a 100k precision resistor. Output voltages can be programmed with an additional resistor between FB and SGND pins.

COMPa (Pin B10): Current control threshold and error amplifier compensation point of the switching mode regulator channel. The internal current comparator threshold is linearly proportional to this voltage. Tie the COMPa pins from different channels together for parallel operation. The device is internally compensated. Connect to COMPb to use the internal compensation. Or connect to a Type-II C-R-C network to use customized compensation.

COMPb (Pin B11): Internal Loop Compensation Network. Connect to COMPa to use the internal compensation in majority of applications.

SGND (Pins C6-D6, B7-D8): Signal Ground Pin. Tie to GND with minimum distance. Connect all small signal components e.g., $INTV_{CC}$, SS, FB, Comp, FREQ, etc. to SGND.

V_{IN} (Pins H1-M1, H2-M2): Power Input Pins. Apply input filter capacitors between these pins and GND pins. See the Applications Information section.

V_{OUT} (Pins H11-M11, H12-M12): Power Output Pins. Apply output filter capacitors between these pins and GND pins. See the Applications Information section.

SW1, SW2 (Pins K5-L5, K8-L8): Switching Nodes of Buck Side or Boost Side that is Used for Testing Purposes. An R-C snubber network can be applied to reduce switch node ringing, or otherwise leave floating.

BLOCK DIAGRAM

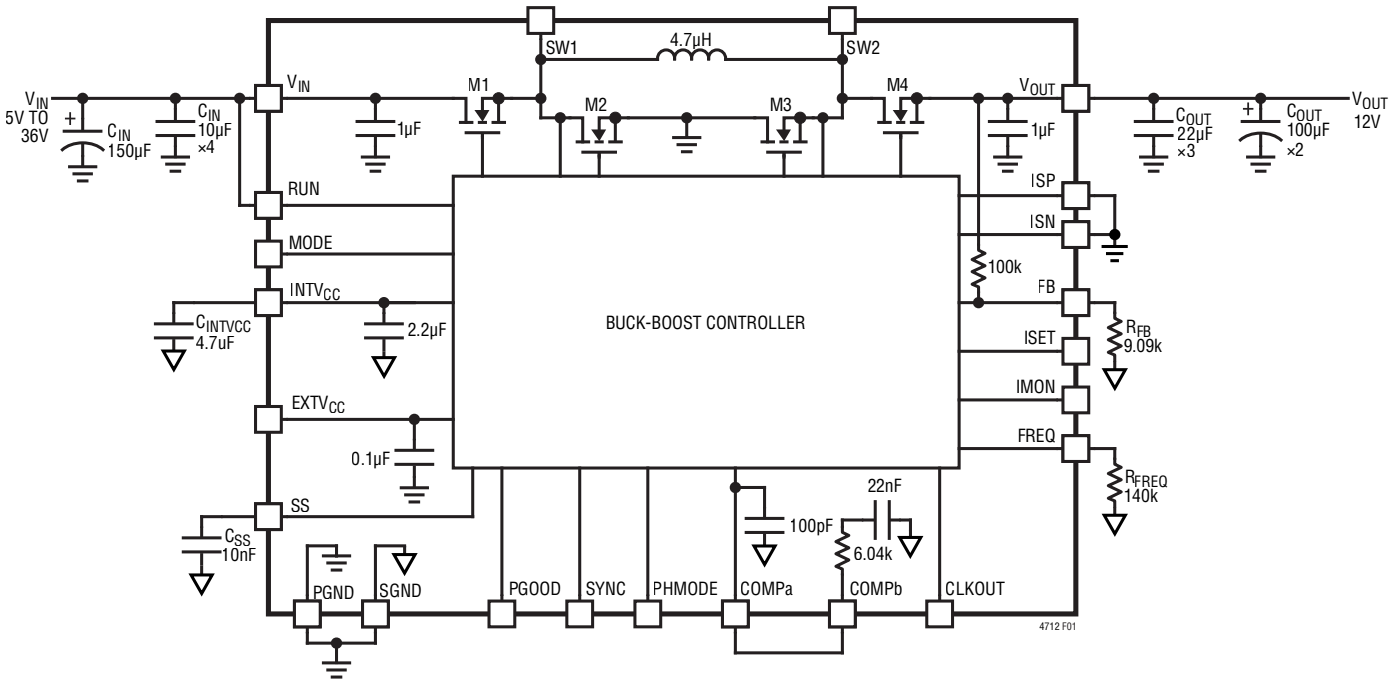


Figure 1. LTM4712 Block Diagram

OPERATION

The LTM4712 is a standalone nonisolated buck-boost switching DC/DC power supply. The buck-boost topology allows the LTM4712 to regulate its output voltage for input voltages both above and below the magnitude of the output. The maximum output current depends upon the input voltage. Higher input voltages yield higher maximum output current.

This converter provides a precisely regulated output voltage programmable via an external resistor divider from 1V to 36V. The input voltage range is 5V to 36V. See the Block Diagram (Figure 1).

The LTM4712 contains a constant frequency, peak current mode controller, power switching elements, power inductor and a modest amount of input and output capacitance. The LTM4712 is a constant frequency PWM regulator. The operating frequency can be adjusted from 100kHz to 600kHz by connecting the appropriate resistor value from the FREQ pin to SGND. Alternatively, its frequency can be synchronized by an input clock signal on the SYNC pin. The typical switching frequency is 400kHz.

The output voltage of the LTM4712 is set by connecting the FB pin to a resistor between FB pin and GND.

In addition to regulating output voltage, the LTM4712 is equipped with average current control loops for either the input or output. Add a current sense resistor to limit the input or output current below maximum value. When the resistor is present, the IMON pin reflects the current flowing though the sense resistor between input or output.

The LTM4712 features an integrated compensation network for most conditions. Some applications, however, benefit from a different compensation network. In such cases, apply an appropriate external compensation network for optimal and proper operation.

If an external bias supply is applied on the $EXTV_{CC}$ pin, then an efficiency improvement occurs due to the reduced power loss in the internal linear regulator. This is especially true at the higher end of the input voltage range.

APPLICATIONS INFORMATION

The typical LTM4712 application circuit is shown on the front page. External component selection is primarily determined by the input voltage, the output voltage, and the maximum load current.

Output Voltage Programming

The PWM controller has an internal 1V reference voltage. A 100k internal feedback resistor connects V_{OUT} and FB pins together. Adding a resistor R_{FB} from the FB pin to GND programs the output voltage (see Equation 1).

$$R_{FB}\ (k\Omega) = \frac{100}{V_{OUT} - 1} \quad (1)$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	3.3	5	8	12	16	20	24	28
R_{FB} (k)	43.5	25	14.3	9.09	6.67	5.23	4.35	3.74

For parallel operation of N-channels LTM4712, Equation 2 can be used to solve for R_{FB}.

$$R_{FB}\ (k\Omega) = \frac{100}{N \bullet V_{OUT} - 1} \quad (2)$$

Operating Frequency Selection and Phase-Locked Loop (FREQ, SYNC, PHMODE and CLKOUT Pins)

The switching frequency of the LTM4712 can be selected using the FREQ pin. If the SYNC pin is not being driven by an external clock source, the FREQ pin is used to program the controller's operating frequency from 100kHz to 600kHz. Switching frequency is determined by the voltage on the FREQ pin. Since there is a precision 10µA current flowing out of the FREQ pin, program the controller's switching frequency with a single resistor to SGND (e.g., the FREQ pin voltage is 1.58V with 158k resistor from the FREQ pin to SGND). Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. Switching Frequency vs R_T Value

FREQUENCY (kHz)	R_T VALUE (kΩ)
100	58
200	80
300	120
400	140
500	170
600	200

A phase-locked loop (PLL) is integrated to synchronize the internal oscillator to an external clock source driving the SYNC pin. The PLL is capable of locking to any frequency within the range of 100kHz to 600kHz. The frequency setting resistor at FREQ pin should always be present to set the controller's initial switching frequency before locking to the external clock or in any cases the external clock is missing during the operation. The CLKOUT pin is a clock signal output with the same frequency as the internal oscillator with phase shift programmed by the PHMODE pin. It can be used in multi-IC parallel applications by passing the clock signal of the first IC to the SYNC pin of the second IC for frequency synchronization. The phase shift can be programmed based on Table 3.

Table 3. PHMODE Setting vs CLKOUT Phase Shift

PHMODE PIN	CLKOUT PHASE SHIFT REFERS TO THE INTERNAL OSCILLATOR
SGND	180°
FLOAT	120°
$INTV_{CC}$	90°

Input Decoupling Capacitors

In boost mode, since the input current is continuous, only minimum input capacitors are required. However, the input current is discontinuous in buck mode. So the selection of input capacitor C_{IN} is driven by the need of filtering the input square wave current.

APPLICATIONS INFORMATION

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated with Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUTMAX}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (3)$$

where η is the estimated efficiency of the power module. The formula has a maximum at D = 0.5 or $V_{IN} = 2V_{OUT}$, where $I_{IN(RMS)} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design.

Output Decoupling Capacitors

Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by Equation 4.

$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f_{SW}}$$
$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{8 \bullet L \bullet C_{OUT} \bullet V_{IN(MAX)} \bullet f_{SW}^2} \quad (4)$$

The maximum steady ripple due to the voltage drop across the ESR is given by Equation 5.

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{OUT(MAX)}}{V_{IN(MAX)}} \bullet ESR$$
$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \bullet L \bullet f_{SW}} \bullet ESR \quad (5)$$

The bulk output capacitors defined as C_{OUT} are chosen with low enough ESR to meet the output voltage ripple and transient requirements. C_{OUT} can be the low ESR tantalum capacitor, the low ESR polymer capacitor, or the ceramic capacitor. Multiple capacitors can be placed in parallel to meet the ESR and RMS current handling requirements. The typical capacitance is 10µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required.

Power Good (PGOOD Pin)

The PGOOD pin is connected to the open-drain of an internal N-channel MOSFET. When V_{FB} is not within ±10% of the 1.0V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when RUN is below 1.22V or when the LTM4712 is in the soft-start phase. There is an internal 30µs delay when V_{FB} goes in or out of the ±10% window. The PGOOD pin can be pulled up by an external resistor to $INTV_{CC}$ or an external source of up to 6V.

Low Current Operation (MODE Pin)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation is enabled by tying the MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4712's output voltage is in regulation.

In applications where high efficiency at intermediate current are more important than output voltage ripple, pulse-skipping mode of operation can be selected by floating the MODE pin to improve light load efficiency.

Constant Current Regulation (ISP, ISN, and ISET Pins)

The LTM4712 provides a constant-current regulation loop for either input or output average current. A sensing resistor close to the input or output capacitor can be used to sense the input or output current. Because the input or output current may be a pulse current in the different operation regions, an RC filter has to be applied on ISP and ISN pins for average current sensing. When the voltage on the current sensing resistor exceeds the programmed current limit, the voltage on the COMP pin is pulled low to decrease the inductor current and maintain the desired maximum input or output current. The current limit may be set by the voltage on the ISET pin from 0.2V to 1.2V corresponding to the linearly 0mV to 50mV across the sensing resistor. There is a 15µA current out of the

APPLICATIONS INFORMATION

ISET pin if the ISET pin is float or ISET pin voltage higher than 1.2V, the current limit is clamped at 50mV internally. The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as an extra current limit protection for a constant-voltage regulation application. The input/output current limit function has an operating voltage range of GND to the absolute maximum V_{OUT}/V_{IN} (36V).

Output Current Monitor (IMON)

The IMON pin produces a voltage proportional to the voltage of ISP–ISN. When $V_{ISP} – V_{ISN}$ = 0mV, IMON is 0.2V. When $V_{ISP}–V_{ISN}$ = 50mV, IMON is 1.2V.

Soft-Start Function

When a capacitor is connected to the SS pin, a soft-start current of 2.5µA starts to charge the capacitor. A soft-start function is achieved by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled during this phase to ensure smooth soft-start. When the chip is in the shutdown state with its RUN pin voltage below 1.22V, the SS pin is actively pulled to ground. The soft-start range is defined to be the voltage range from 0V to 1.0V on the SS pin. The total soft-start time can be calculated with Equation 6.

$$t_{SOFTSTART} = 1.0 \bullet \frac{C_{SS}}{2.5\mu A} \quad (6)$$

Regardless of the mode selected by the MODE pin, the regulator always starts in pulse-skipping mode up to SS = 1.0V.

Run Enable

The RUN pin is used to enable the power module. The pin can be driven with a logic input, not to exceed 12V. The RUN pin can also be used as an undervoltage lockout (UVLO) function by connecting a resistor from the input supply to the RUN pin. Increasing the RUN pin voltage above 1.22V turns on the entire chip.

Stability Compensation

The LTM4712 has already been internally optimized and compensated for all output voltages and capacitor combinations including all ceramic capacitor applications when COMPb is tied to COMPa. For specific optimized requirement, disconnect COMPb from COMPa and apply a Type II C-R-C compensation network from COMPa to GND to achieve external compensation. The LTpowerCAD® design tool is available to download on-line to perform specific control loop optimization and analyze the control stability and load transient performance.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a peak current mode controller with a 20A maximum current limit.

To promote limit current in the event of a short-circuit to ground, the LTM4712 includes foldback current limiting. If the output falls by more than 40%, then the maximum current is progressively lowered to about 4A.

Parallel Operations

For output loads that demand high current, multiple LTM4712s can be paralleled with interleaving to provide more output current without increasing input and output voltage ripple. The SYNC pin allows the LTM4712 to synchronize to the CLKOUT signal of another LTM4712. The CLKOUT signal can be connected to the SYNC pin of the following LTM4712 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to GND, floating or $INTV_{CC}$ generates a phase difference (between SW1 and CLKOUT) of 180°, 120° or 90°, respectively for 2, 3, or 4 ICs parallel operations.

When designing multiple ICs parallel operations, always start from the single LTM4712 design and check the output current capability and load current transient stability. Then the LTM4712s can be paralleled by making the following connections:

- Tie all V_{FB} pins together
- Tie all COMP pins together (assuming COMPa short to COMPb for initial debug)

APPLICATIONS INFORMATION

- Tie all SS pins together
- Tie all RUN pins together
- Tie all converter inputs together
- Tie all converter outputs together
- Route one IC's CLKOUT to another IC's SYNC pin

Refer to the Figure 24 section for an example of a 2-phase parallel operation design.

The LTM4712 can also be paralleled from different input voltages for a redundancy design. Do not tie SS and RUN pins of the LTM4712s together so each LTM4712 can start up with different input voltages to supply current to a single output. Any one input voltage failure does not affect the output voltage regulation as long as the other input sources supply enough load current. The peak inductor currents are shared among all the buck-boost converters by tying all the COMP pins together. In the redundancy design, it is suggested that each LTM4712 has its own compensation network and feedback resistor locally closed to the pin and then short the FB pins and COMP pins all together with PCB traces.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section are consistent with those parameters defined by JESD 51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD 51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients is found in JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to application usage and can be adapted to correlate thermal performance to application itself.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions do not generally match the application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions do not generally match the application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board.

APPLICATIONS INFORMATION

A graphical representation of the aforementioned thermal resistances is given in Figure 2; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package. Granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED 51-9 to predict power loss heat flow.

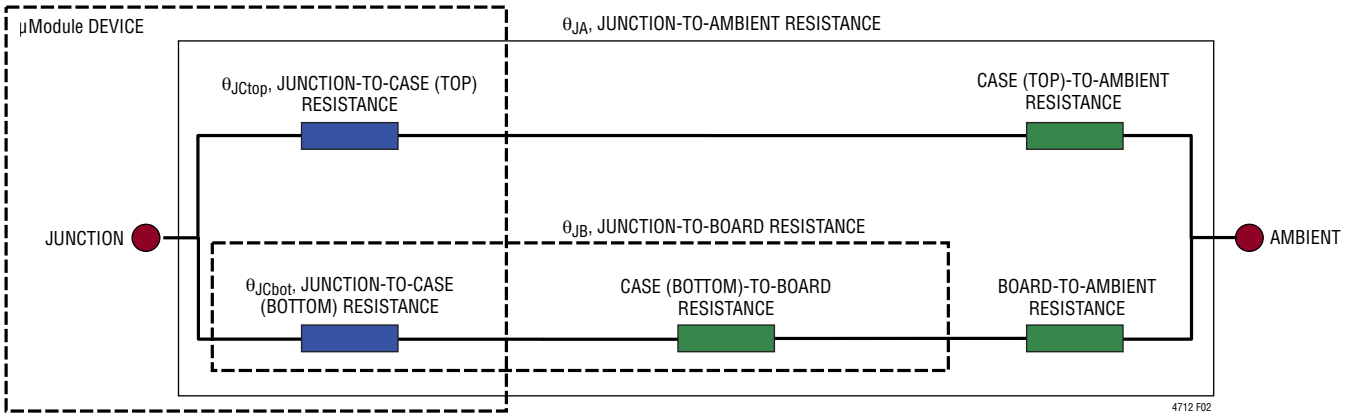


Figure 2. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

APPLICATIONS INFORMATION

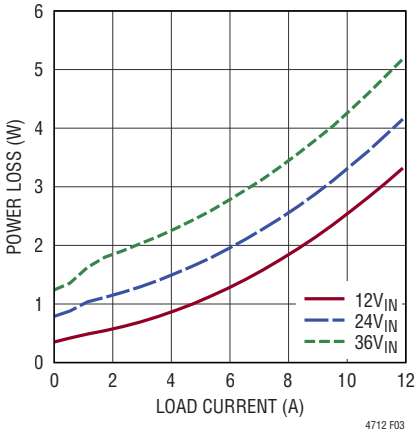


Figure 3. Power Loss $5V_{OUT}$, 400kHz, FCM

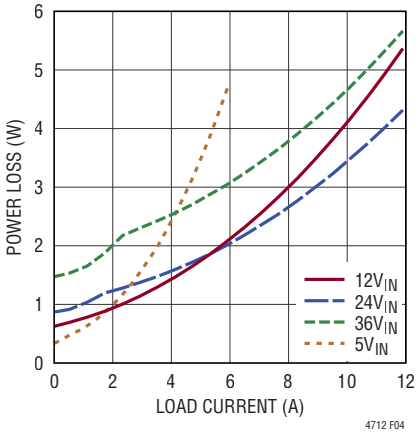


Figure 4. Power Loss $12V_{OUT}$, 400kHz, FCM

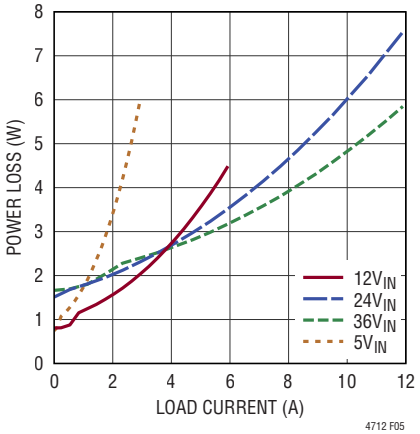


Figure 5. Power Loss $24V_{OUT}$, 400kHz, FCM

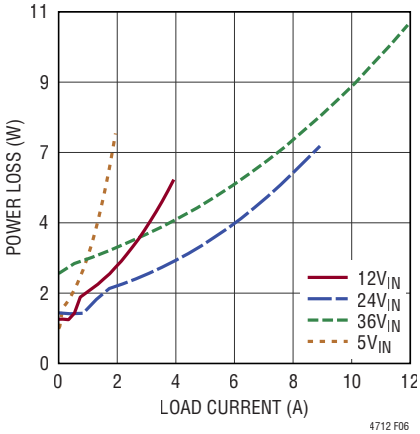


Figure 6. Power Loss $36V_{OUT}$, 400kHz, FCM

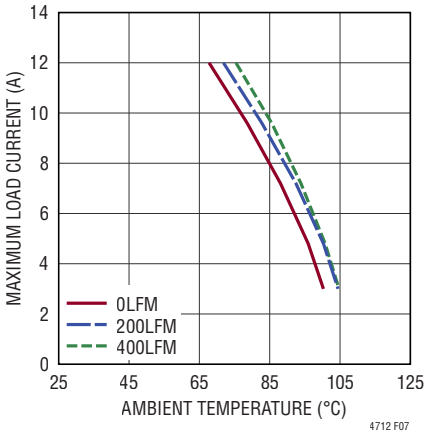


Figure 7. $36V_{IN}$ to $5V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

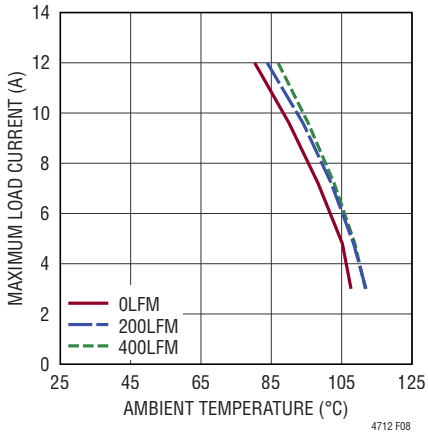


Figure 8. $24V_{IN}$ to $5V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

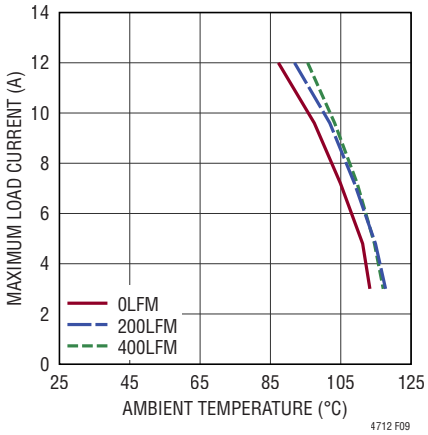


Figure 9. $12V_{IN}$ to $5V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

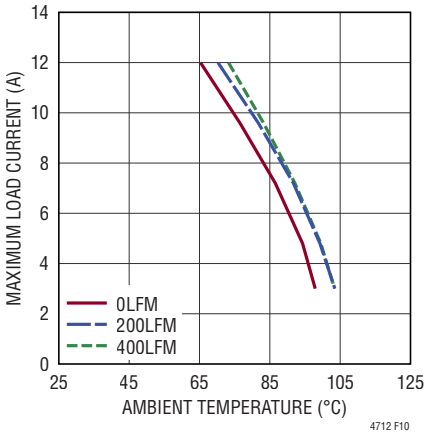


Figure 10. $36V_{IN}$ to $12V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

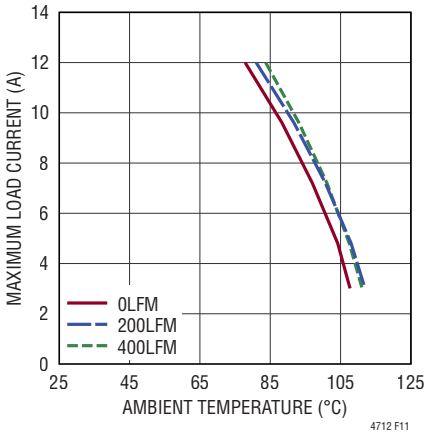


Figure 11. $24V_{IN}$ to $12V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

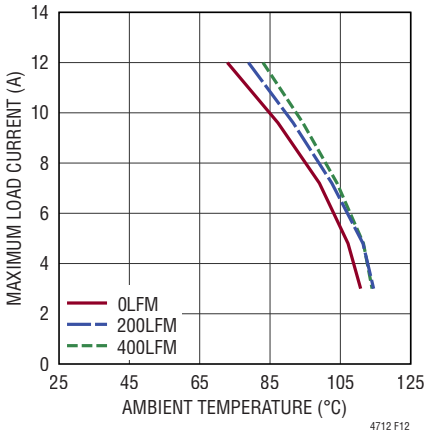


Figure 12. $12V_{IN}$ to $12V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

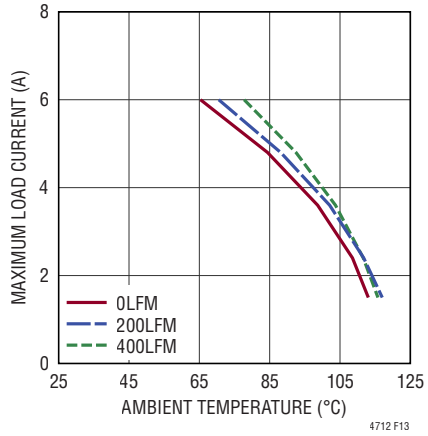


Figure 13. $5V_{IN}$ to $12V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

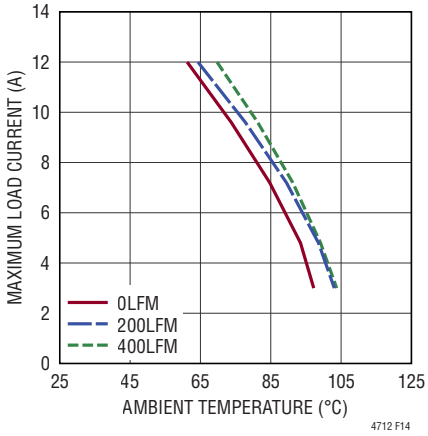


Figure 14. $36V_{IN}$ to $24V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

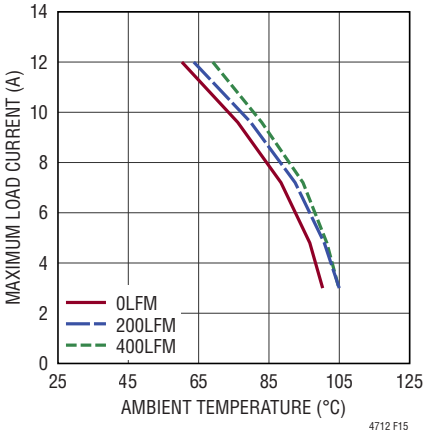


Figure 15. $24V_{IN}$ to $24V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

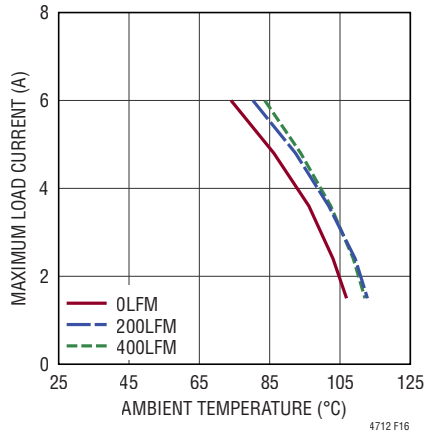


Figure 16. $12V_{IN}$ to $24V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

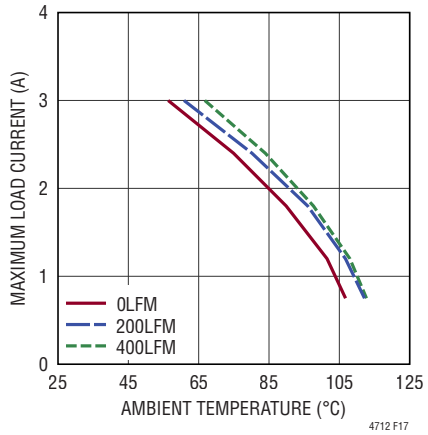


Figure 17. $5V_{IN}$ to $24V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

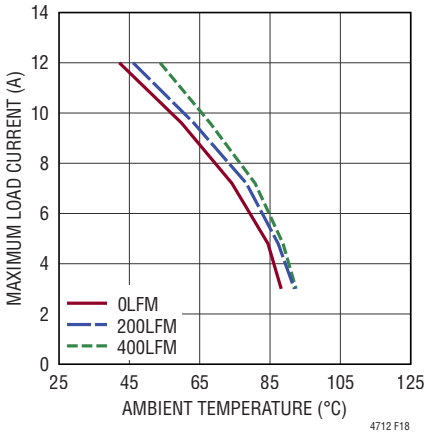


Figure 18. $36V_{IN}$ to $36V_{OUT}$, 400kHz, Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

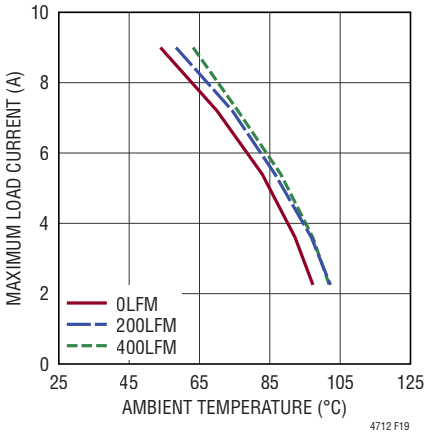


Figure 19. 24V_{IN} to 36V_{OUT}, 400kHz, Derating Curve, No Heat Sink

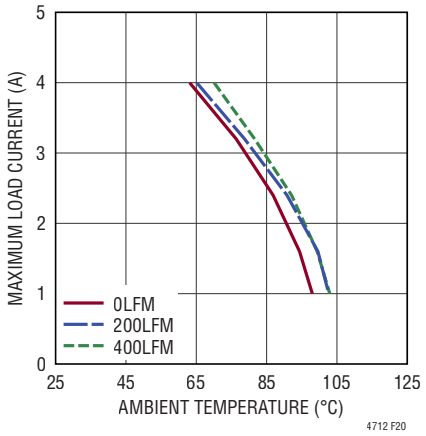


Figure 20. 12V_{IN} to 36V_{OUT}, 400kHz, Derating Curve, No Heat Sink

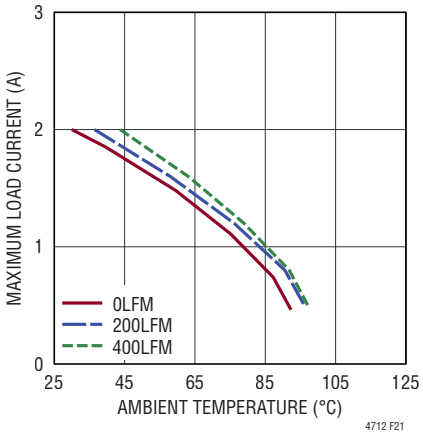


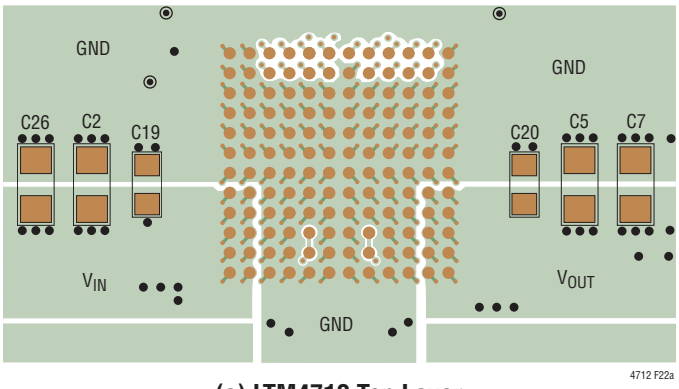
Figure 21. 5V_{IN} to 36V_{OUT}, 400kHz, Derating Curve, No Heat Sink

PCB Layout

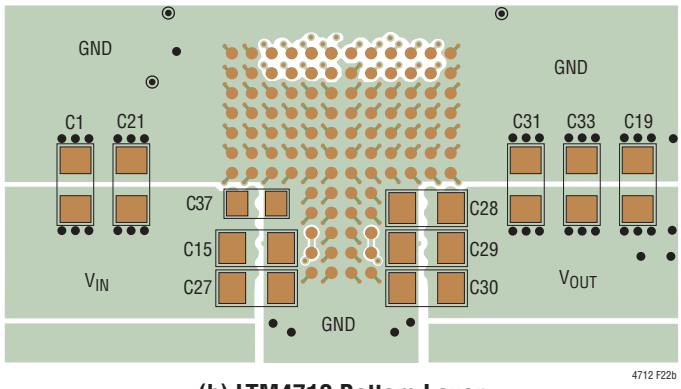
The high integration of LTM4712 makes the PCB layout very simple and easy. However, to optimize its electrical and thermal performance, the following layout considerations are still necessary:

- Use large PCB copper areas for high current path, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high-frequency input and output ceramic capacitors next to the V_{IN}, GND, and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
- Do not put vias directly on pads, unless the vias are capped.
- Use a separated SGND ground copper area for components connected to the signal pins. Connect the SGND to PGND underneath the unit.

Figure 22 gives a good example of the recommended PCB layout.



(a) LTM4712 Top Layer



(b) LTM4712 Bottom Layer

Figure 22. Recommended PCB Layout

APPLICATIONS INFORMATION

Table 4. Bulk and Ceramic Capacitor Manufacturers

C_{IN} (BULK)			C_{OUT} (BULK)		
VENDORS	**VALUE**	**PART NUMBER**	**VENDORS**	**VALUE**	**PART NUMBER**
Panasonic	150µF, 50V	EEEFK1H151P	Panasonic	100µF, 16V	16TQC100MYF
C_{IN} (CERAMIC)			**C_{OUT} (CERAMIC)**		
VENDORS	**VALUE**	**PART NUMBER**	**VENDORS**	**VALUE**	**PART NUMBER**
AVX	0.1µF, 50V, 0805, X7R	08055C104KAT2A	AVX	0.1µF, 50V, 0805, X7S	08055C104KAT2A
Murata	10µF, 50V, 1210, X7R	GRM32ER71H106KA12L	TDK	22µF, 100V, 1210, X7R	C3225X7R1C226K250AC

Table 5. Component Selection Table for Typical LTM4712 Applications

V_{IN} (V)	V_{OUT} (V)	C_{IN} (BULK) (µF)	C_{IN} (CERAMIC) (µF)	C_{OUT} (BULK) (µF)	C_{OUT} (CERAMIC) (µF)	R_{FB} (kΩ)	R_{FREQ} (kΩ)
12	12	150	10 ×4	100	22 ×4	9.09	140
24	12	150	10 ×4	100	22 ×4	9.09	140
36	12	150	10 ×4	100	22 ×4	9.09	140
24	24	150	10 ×4	82	10 ×8	4.32	140
12	36	150	10 ×4	330 ×2	10 ×8	2.87	140
12	5	150	10 ×4	100	22 ×4	25	140

TYPICAL APPLICATIONS

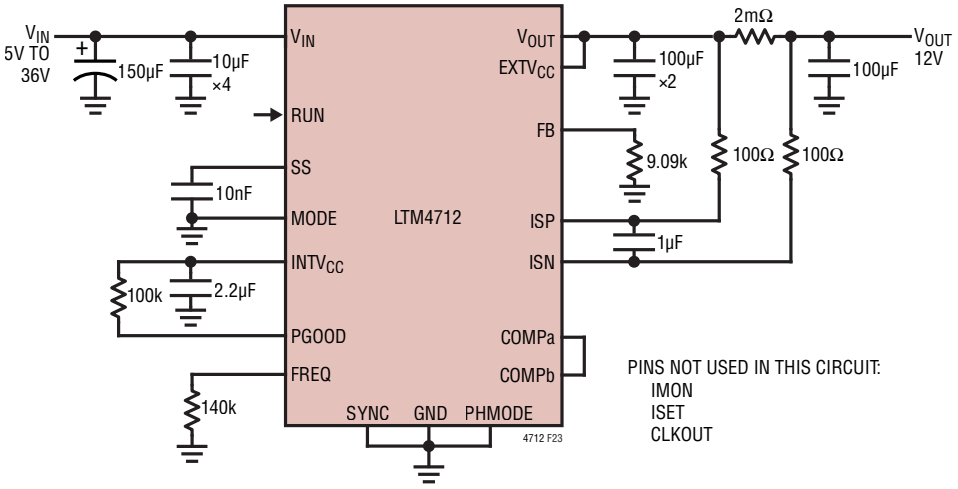


Figure 23. 12V_{OUT} with Wide Input Voltage Range, 12A I_{OUT} for Buck/Buck-Boost, 6A I_{OUT} for Boost

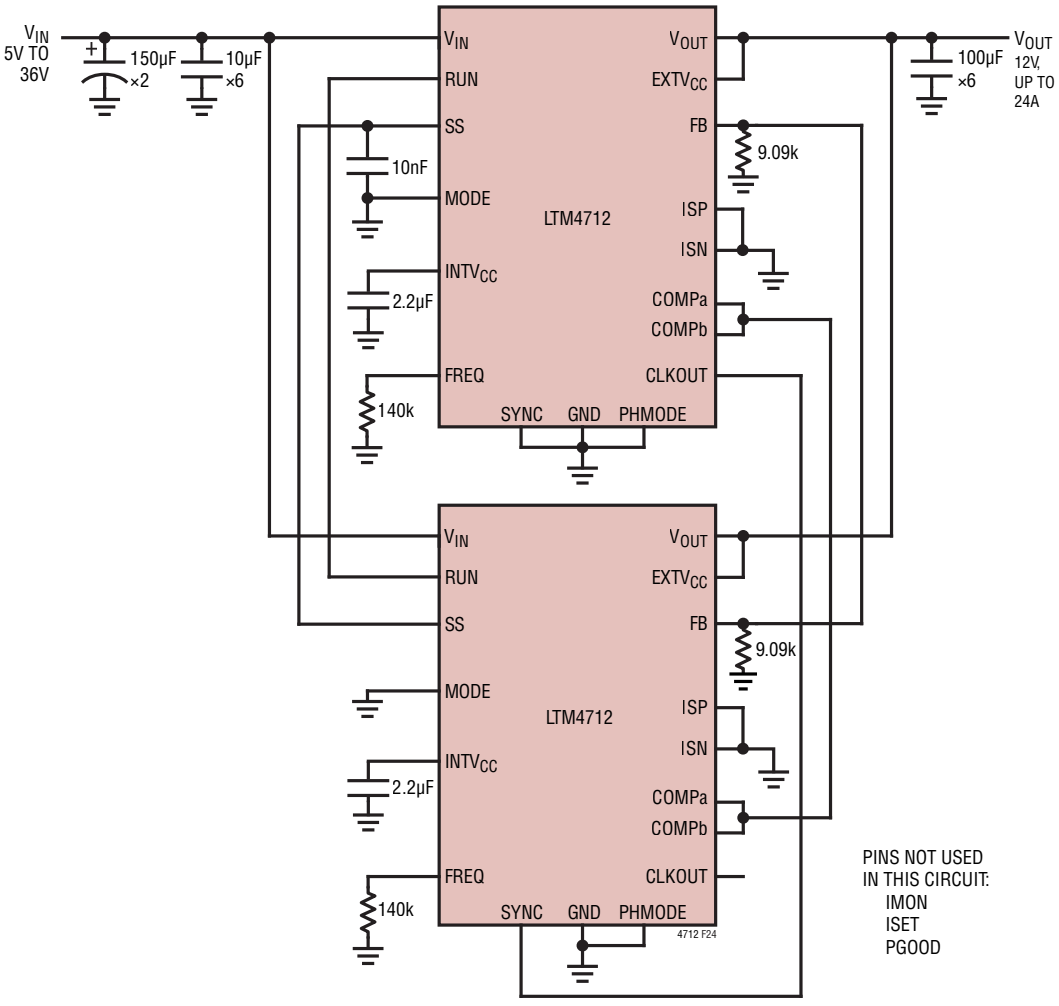


Figure 24. 2× LTM4712 Parallel to Provide Up to 24A Output Current

TYPICAL APPLICATIONS

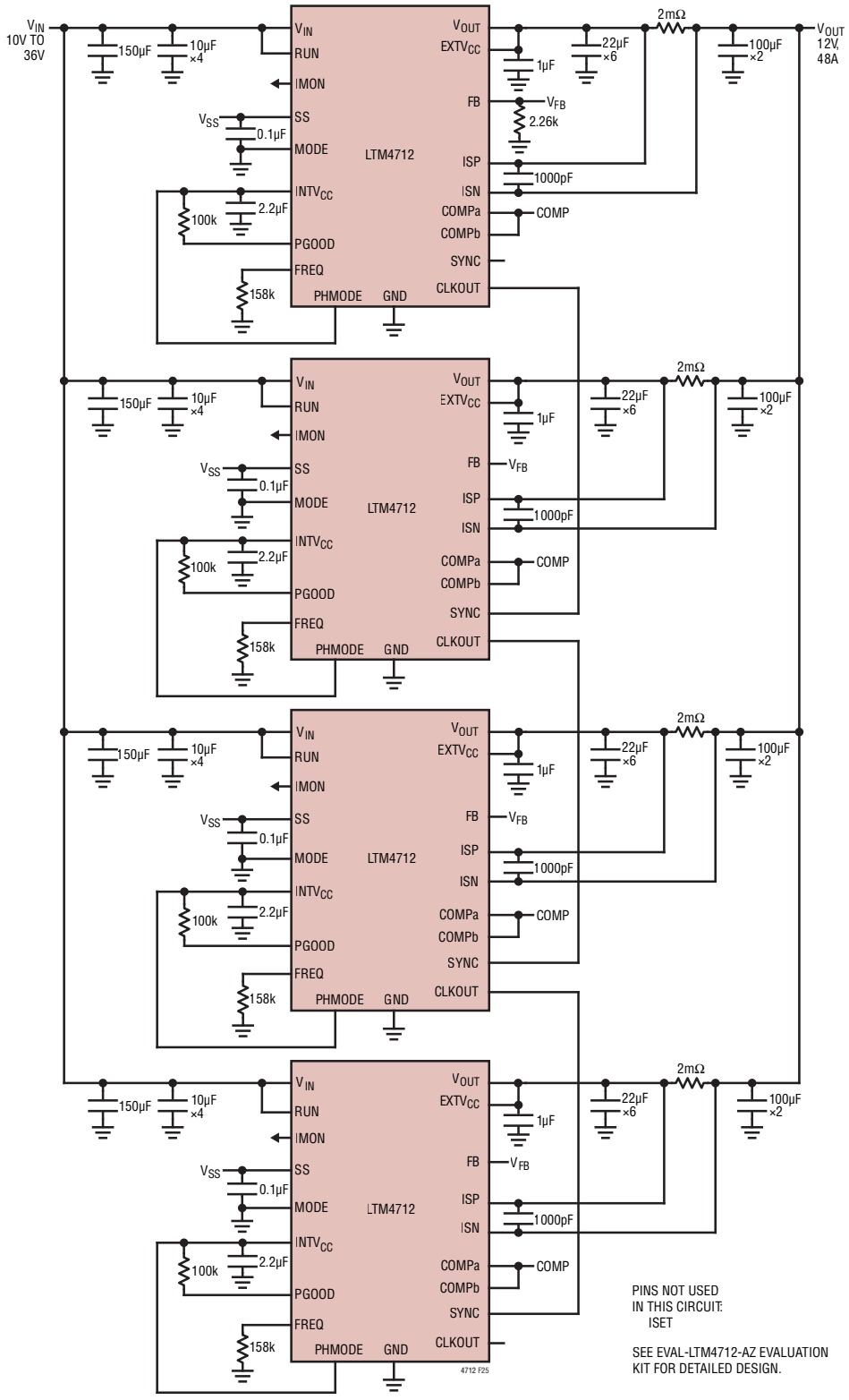


Figure 25. 4× LTM4712 in Parallel to Provide Up to 48A Output Current

TYPICAL APPLICATIONS

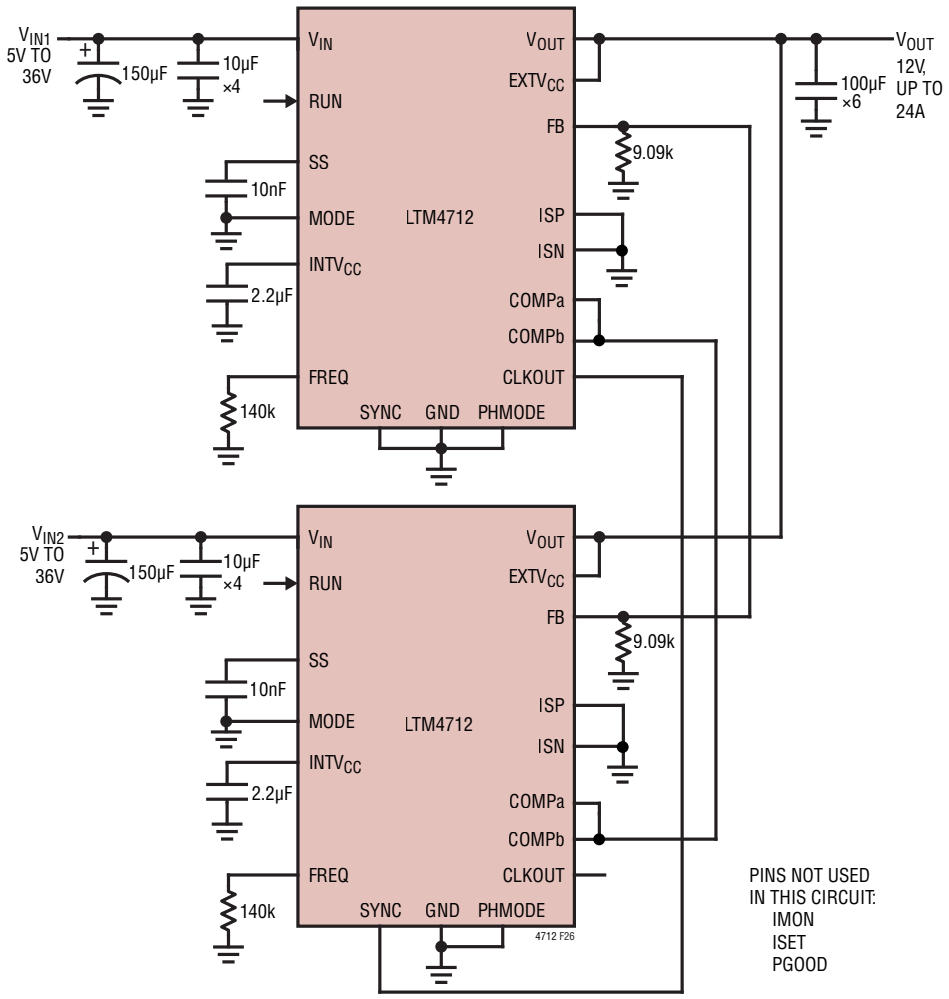


Figure 26. Input Redundancy Application Circuit

TYPICAL APPLICATIONS

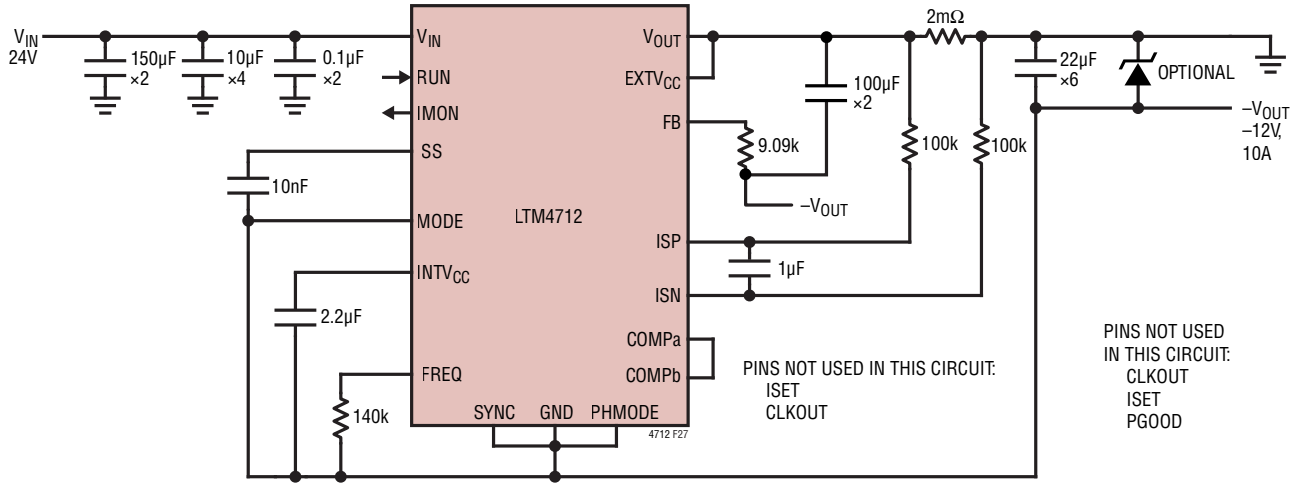


Figure 27. Inverting Configuration Example for 24V_{IN}, –12V_{OUT}

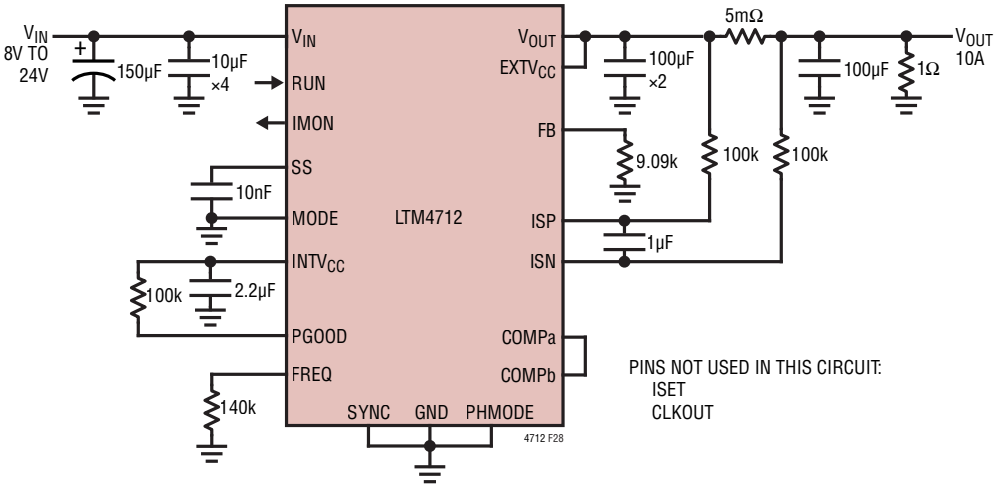


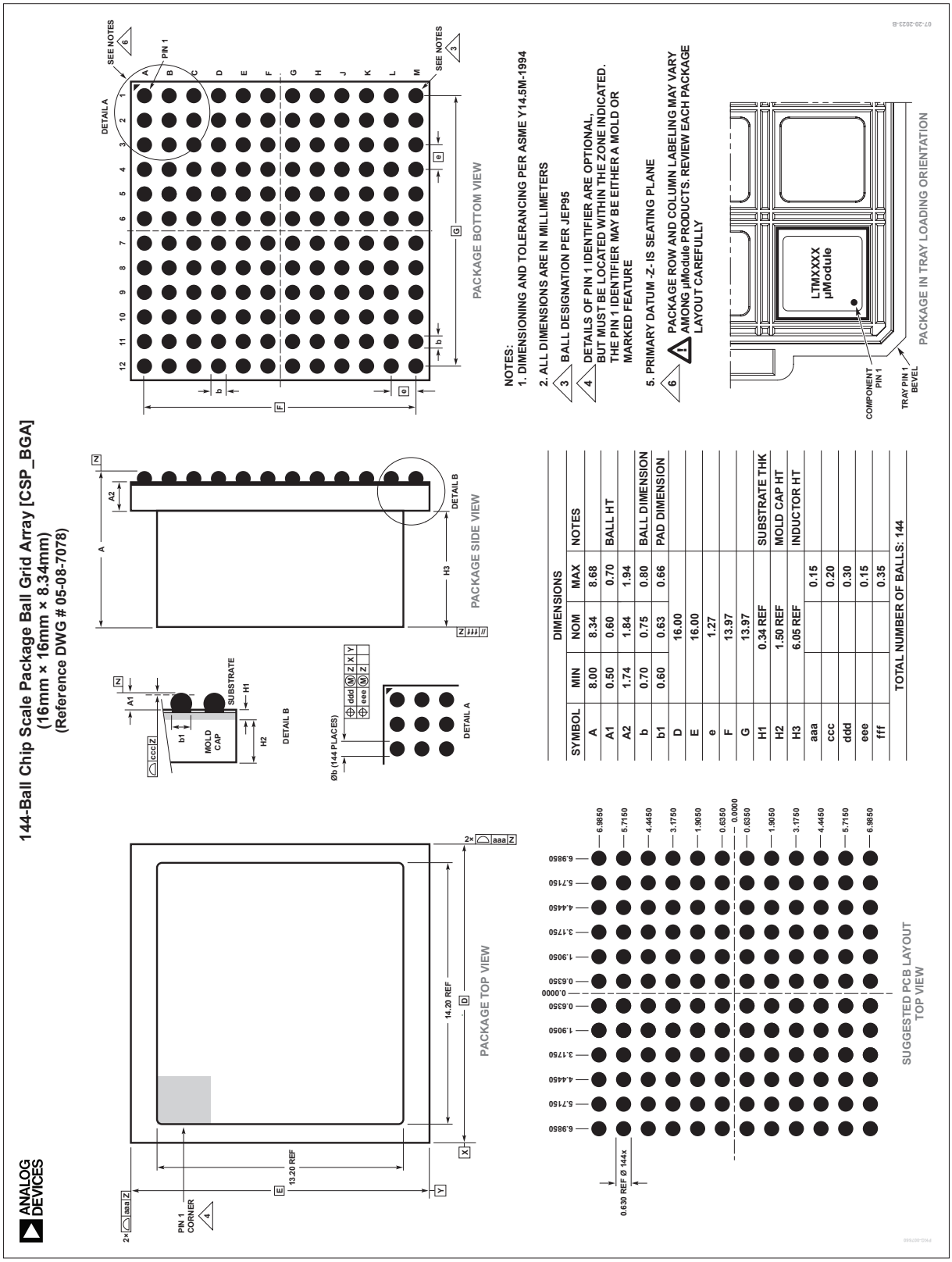
Figure 28. Application Circuit for 10A Constant Load Current

PACKAGE DESCRIPTION

Table 6. LTM4712 Pin Assignment (Arranged by Pin Number)

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	GND	C1	GND	D1	GND	E1	GND	F1	GND
A2	GND	B2	GND	C2	GND	D2	GND	E2	GND	F2	GND
A3	ISN	B3	$INTV_{CC}$	C3	GND	D3	GND	E3	GND	F3	GND
A4	ISP	B4	$EXTV_{CC}$	C4	GND	D4	GND	E4	GND	F4	GND
A5	IMON	B5	ISET	C5	GND	D5	GND	E5	GND	F5	GND
A6	CLKOUT	B6	SYNC	C6	SGND	D6	SGND	E6	GND	F6	GND
A7	FREQ	B7	SGND	C7	SGND	D7	SGND	E7	GND	F7	GND
A8	PGOOD	B8	RUN	C8	GND	D8	GND	E8	GND	F8	GND
A9	PHMODE	B9	FB	C9	GND	D9	GND	E9	GND	F9	GND
A10	MODE	B10	COMPa	C10	GND	D10	GND	E10	GND	F10	GND
A11	SS	B11	COMPb	C11	GND	D11	GND	E11	GND	F11	GND
A12	GND	B12	GND	C12	GND	D12	GND	E12	GND	F12	GND
G1	GND	H1	V_{IN}	J1	V_{IN}	K1	V_{IN}	L1	V_{IN}	M1	V_{IN}
G2	GND	H2	V_{IN}	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}	M2	V_{IN}
G3	GND	H3	GND	J3	GND	K3	GND	L3	GND	M3	GND
G4	GND	H4	GND	J4	GND	K4	GND	L4	GND	M4	GND
G5	GND	H5	GND	J5	GND	K5	SW1	L5	SW1	M5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND	M6	GND
G7	GND	H7	GND	J7	GND	K7	GND	L7	GND	M7	GND
G8	GND	H8	GND	J8	GND	K8	SW2	L8	SW2	M8	GND
G9	GND	H9	GND	J9	GND	K9	GND	L9	GND	M9	GND
G10	GND	H10	GND	J10	GND	K10	GND	L10	GND	M10	GND
G11	GND	H11	V_{OUT}	J11	V_{OUT}	K11	V_{OUT}	L11	V_{OUT}	M11	V_{OUT}
G12	GND	H12	V_{OUT}	J12	V_{OUT}	K12	V_{OUT}	L12	V_{OUT}	M12	V_{OUT}

PACKAGE DESCRIPTION



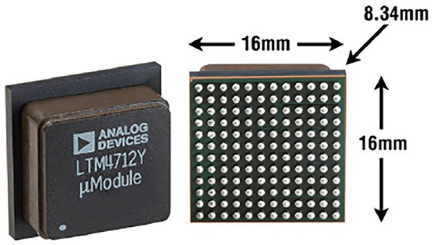
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	8.00	8.34	8.68	
A1	0.50	0.60	0.70	BALL HT
A2	1.74	1.84	1.94	
b	0.70	0.75	0.80	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1		0.34 REF		SUBSTRATE THK
H2		1.50 REF		MOLD CAP HT
H3		6.05 REF		INDUCTOR HT
aaa			0.15	
ccc			0.20	
ddd			0.30	
eee			0.15	
fff			0.35	
TOTAL NUMBER OF BALLS: 144				

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	10/23	Initial Release.	—

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4605	$20V_{IN}$, $20V_{OUT}$, 12A Buck-Boost µModule Regulator with External Inductor	$4.5V \le V_{IN} \le 20V$, $0.8V \le V_{OUT} \le 16V$, 15mm × 15mm × 2.82mm LGA
LTM4607	$36V_{IN}$, $24V_{OUT}$, 10A Buck-Boost µModule Regulator with External Inductor	$4.5V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 24V$, 15mm × 15mm × 2.82mm LGA
LTM4609	$36V_{IN}$, $34V_{OUT}$, 10A Buck-Boost µModule Regulator with External Inductor	$4.5V \le V_{IN} \le 36V$. $0.8V \le V_{OUT} \le 34V$, 15mm × 15mm × 2.82mm LGA, 15mm × 15mm × 3.42mm BGA
LTM8054	$36V_{IN}$, $36V_{OUT}$, 5.4A Buck-Boost µModule Regulator with Integrated Inductor	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$, 11.25mm × 15mm × 3.42mm BGA
LTM8055	$36V_{IN}$, $36V_{OUT}$, 8.5A Buck-Boost µModule Regulator with Integrated Inductor	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$, 15mm × 15mm × 4.92mm BGA
LTM8056	$58V_{IN}$, $48V_{OUT}$ Buck-Boost µModule Regulator with Integrated Inductor	$5V \le V_{IN} \le 58V$, $1.2V \le V_{OUT} \le 48V$, 15mm × 15mm × 4.92mm BGA
LTM4656	$36V_{OUT}$, 4A Boost µModule Regulator	$4.5V \le V_{IN} \le 28V$, $6V \le V_{OUT} \le 36V$, 16mm × 16mm × 7.07mm BGA

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