

## 150V Half Bridge Driver with Adaptive Shoot-Through Protection

### FEATURES

- ▶ **150V Maximum Input Voltage Independent of IC Supply Voltage  $V_{CC}$**
- ▶ **6V to 14V  $V_{CC}$  and Bottom Gate Driver Voltage**
- ▶ **4V to 14V Top Gate Driver Voltage**
- ▶ **1.3 $\Omega$  Pull-Down, 1.6 $\Omega$  Pull-Up**
- ▶ **Adaptive Shoot-Through Protection**
- ▶ **Three-State PWM Input with Enable Pin**
- ▶  **$V_{CC}$  UVLO and Floating Supply UVLO**
- ▶ Drives Dual N-Channel MOSFETs
- ▶ Available in Thermally Enhanced 10-LEAD Mini Small Outline Package (MSOP)

### APPLICATIONS

- ▶ Industrial Power Systems
- ▶ Half-bridge DC/DC Converters
- ▶ Telecommunication Power Systems

### GENERAL DESCRIPTION

The **LTC7068** is a half-bridge dual N-Channel MOSFET gate driver that operates at up to 150V input voltage and features a supply-independent three-state pulse width modulation (PWM) input logic.

The strong 1.3 $\Omega$  pull-down and 1.6 $\Omega$  pull-up drive capability can drive large gate capacitances of high voltage MOSFETs with short transition times in high switching frequency applications. The adaptive shoot-through protection is designed for optimized efficiency and MOSFET cross-conduction protection.

The LTC7068 contains undervoltage lockout (UVLO) circuits on both the  $V_{CC}$  supply and floating driver supply that turn off the external MOSFETs when activated. See the following table for a comparison of the parts in this family.

PARAMETER	LTC7060	LTC7063	LTC7065	LTC7068
Absolute Max Voltage	115V	155V	115V	155V
Floating Bot. Gate Driver	Yes	Yes	No	No
$V_{CC}$ OVLO	Yes	Yes	No	No
Package	MS12E	MS12E	MS10E	MS10E

### TYPICAL APPLICATION

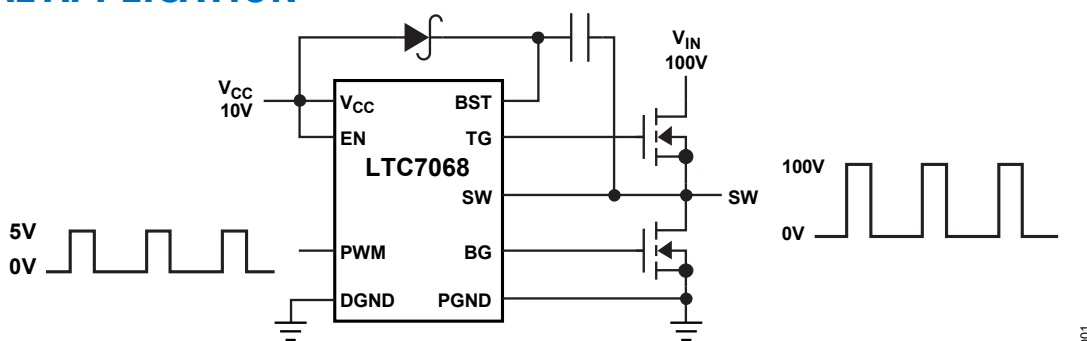


Figure 1. 100V Half-Bridge Driver

## TABLE OF CONTENTS

Features.....	1
Applications .....	1
General Description .....	1
Typical application.....	1
Revision History .....	2
Specifications.....	3
Timing Diagram.....	5
Absolute Maximum Ratings .....	6
Pin Configurations and Function Descriptions .....	7
Typical Performance Characteristics .....	8
Block Diagram.....	10
Theory of Operation.....	10
OVERVIEW .....	10
V <sub>CC</sub> SUPPLY .....	10
INPUT STAGE (PWM, EN).....	10
OUTPUT STAGE.....	11
PROTECTION CIRCUITRY .....	12
ADAPTIVE SHOOT-THROUGH PROTECTION .....	13
Applications Information.....	13
BOOTSTRAPPED SUPPLY (BST-SW) .....	13
POWER DISSIPATION .....	13
BYPASSING AND GROUNDING .....	14
Typical Application .....	15
Ordering Guide.....	16
Related Parts.....	17
Outline Dimensions.....	18

## REVISION HISTORY

**2/2024 - Rev. 0: Initial Release for Product Intro**

## SPECIFICATIONS

Table 1. Electrical Characteristics

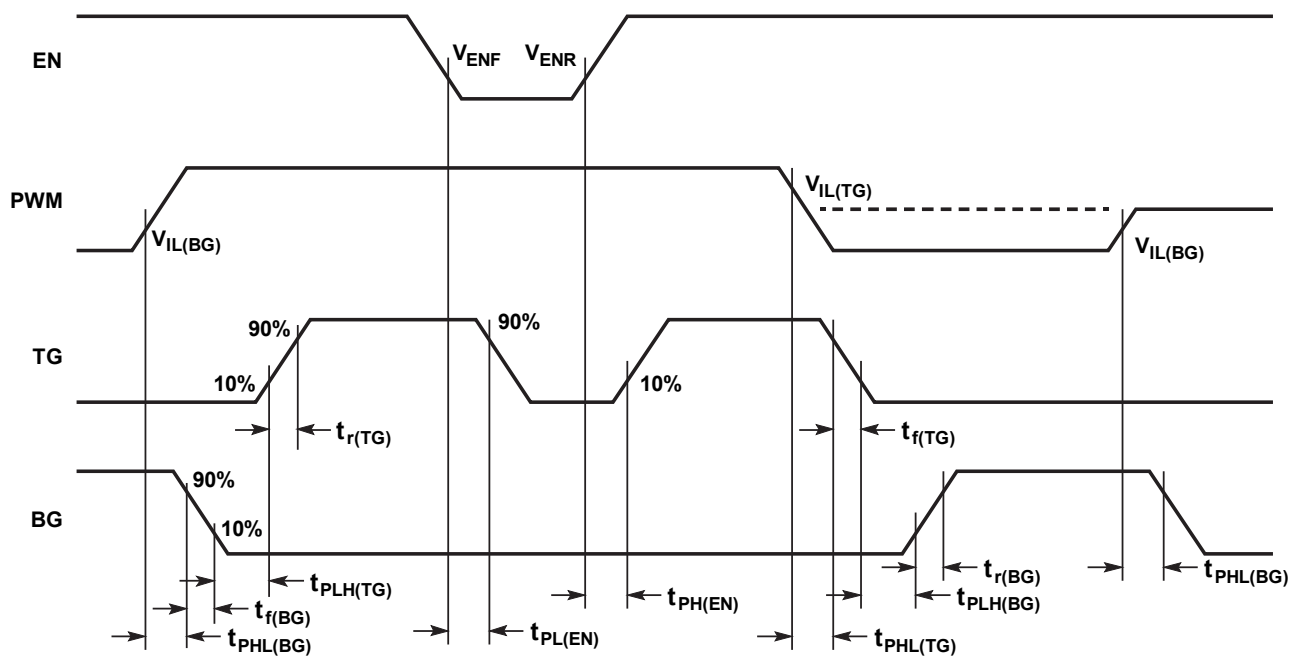
(T<sub>A</sub> = 25°C <sup>(1)</sup>, V<sub>CC</sub> = V<sub>BST</sub> = 10V, V<sub>SW</sub> = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Input Supply and V <sub>cc</sub> Supply							
Input Voltage	V <sub>IN</sub>			150			V
IC and BG Driver Supply Voltage Range	V <sub>CC</sub>			6	14		V
V <sub>CC</sub> Supply Current <sup>(3)</sup>	I <sub>VCC</sub>	No Switching, BG = Low		150			μA
		No Switching, BG = High		300			
V <sub>CC</sub> Undervoltage Lockout Threshold	V <sub>UVLO_VCC</sub>	V <sub>CC</sub> Falling		5.4			V
UVLO Hysteresis	V <sub>UVLO_VCC</sub>			0.3			V
TG Gate Driver Supply (BST)							
TG Driver Supply Voltage Range	V <sub>BST-SW</sub>	(With Respect to SW)		4	14		V
Total BST Current <sup>(3)</sup>	I <sub>BST</sub>	No Switching, TG = Low		9			μA
		No Switching, TG = High		105			
Undervoltage Lockout Threshold	V <sub>UVLO_BST</sub>	BST Falling, With Respect to SW		3.4			V
UVLO Hysteresis	V <sub>UVLO_BST</sub>			0.3			V
Input Signal (PWM, EN)							
TG Turn-On Input Threshold	V <sub>IH(TG)</sub>	PWM Rising	-40°C ≤ T <sub>J</sub> ≤ 150°C	2.7	3.2	3.7	V
TG Turn-Off Input Threshold	V <sub>IL(TG)</sub>	PWM Falling	-40°C ≤ T <sub>J</sub> ≤ 150°C	2.45	2.95	3.45	V
BG Turn-On Input Threshold	V <sub>IH(BG)</sub>	PWM Falling	-40°C ≤ T <sub>J</sub> ≤ 150°C	0.6	1	1.4	V
BG Turn-Off Input Threshold	V <sub>IL(BG)</sub>	PWM Rising	-40°C ≤ T <sub>J</sub> ≤ 150°C	0.85	1.25	1.65	V
PWM Input Three State Float Voltage	V <sub>PWM_TRI</sub>			1.9	2.1	2.3	V
PWM Internal Pull-Up resistor	R <sub>UP_PWM</sub>	To Internal 4.5V Supply		48			kΩ
PWM Internal Pull-Down resistor	R <sub>DOWN_PWM</sub>			42			kΩ
EN Pin Threshold	V <sub>EN</sub>	EN Rising	-40°C ≤ T <sub>J</sub> ≤ 150°C	1.15	1.25	1.35	V
EN Pin Threshold Hysteresis	V <sub>EN</sub>			165			mV

( $T_A = 25^\circ\text{C}$  <sup>(1)</sup>,  $V_{CC} = V_{BST} = 10\text{V}$ ,  $V_{SW} = 0\text{V}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
EN Internal Pull-Down resistor	$R_{\text{DOWN\_EN}}$			2		$\text{M}\Omega$
<b>Dead-Time</b>						
BG Low to TG High Propagation Delay	$t_{\text{PLH(TG)}}$			37		nsec
TG Low to BG High Propagation Delay	$t_{\text{PLH(BG)}}$			41		nsec
<b>Low Side Gate Driver Output (BG)</b>						
BG Pull-Up Resistance	$R_{\text{BG\_UP}}$	$V_{CC} = 10\text{V}$ , Source 100mA		1.6		$\Omega$
BG Pull-Down Resistance	$R_{\text{BG\_DOWN}}$	$V_{CC} = 10\text{V}$ , Sink 100mA		1.3		$\Omega$
<b>High Side Gate Driver Output (TG)</b>						
TG Pull-Up Resistance	$R_{\text{TG\_UP}}$	$BST = 10\text{V}$ , $SW = 0\text{V}$ , Source 100mA		1.6		$\Omega$
TG Pull-Down Resistance	$R_{\text{TG\_DOWN}}$	$BST = 10\text{V}$ , $SW = 0\text{V}$ , Sink 100mA		1.3		$\Omega$
<b>Switching Time</b>						
PWM High to BG Low Propagation Delay	$t_{\text{PHL(BG)}}$			17		ns
PWM Low to TG Low Propagation Delay	$t_{\text{PHL(TG)}}$			24		ns
BG Output Rising Time	$t_{\text{r(BG)}}$	10% – 90%, $C_{\text{LOAD}} = 3\text{nF}$		23		ns
BG Output Falling Time	$t_{\text{f(BG)}}$	10% – 90%, $C_{\text{LOAD}} = 3\text{nF}$		20		ns
TG Output Rising Time	$t_{\text{r(TG)}}$	10% – 90%, $C_{\text{LOAD}} = 3\text{nF}$		29		ns
TG Output Falling Time	$t_{\text{f(TG)}}$	10% – 90%, $C_{\text{LOAD}} = 3\text{nF}$		28		ns
EN High to TG/BG High Propagation Delay	$t_{\text{PH(EN)}}$			35		ns
EN Low to TG/BG Low Propagation Delay	$t_{\text{PL(EN)}}$			43		ns

## TIMING DIAGRAM



018

Figure 2. Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise specified.

**Table 2. Absolute Maximum Ratings**

PARAMETER	RATING
$V_{CC}$ Supply Voltage	-0.3V to 15V
Top Side Driver Voltage (BST)	-0.3V to 155V
SW	-10V to 150V
(BST-SW)	-0.3V to 15V
TG Voltage (Respect to SW)	-0.3V to 15V
BG Voltage (Respect to PGND)	-0.3V to 15V
EN	-0.3V to 15V
PWM	-0.3V to 6V
Operating Junction Temperature Range <sup>(1,2)</sup>	-40°C to 150°C
Storage Temperature Range	-65°C to 150°C

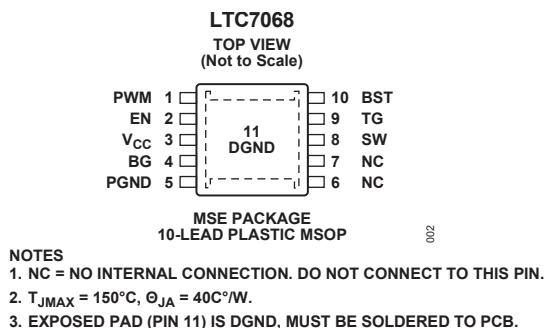
<sup>1</sup> The LTC7068 is guaranteed to meet performance specifications from -40°C to 150°C junction temperature. High junction temperature degrades operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

<sup>2</sup>  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation PD according to the following formula:  
 $T_J = T_A + (PD \cdot 40^\circ\text{C/W})$  for the MSOP package.

<sup>3</sup> The total current includes both the current from  $V_{CC}$ /BST to PGND/SW and the current to DGND. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

**Figure 3. Pin Configurations and Function Descriptions****Table 3. Pin Descriptions**

PIN	NAME	DESCRIPTION
1	PWM	The three-State Gate Driver Input Signal is referenced to the DGND Pin. The TG/BG state is determined by the voltage at this pin. If this pin is floating, an internal resistor divider triggers the High-Z mode in which both BG and TG are turned off. Trace capacitance on this pin should be minimized.
2	EN	Enable Control Input Pin. This pin is referred to DGND. A voltage on this pin above 1.25V enables the gate drivers. The TG and BG pins are both in the low state if this pin is logic low.
3	V <sub>CC</sub>	V <sub>CC</sub> Supply. The bottom gate driver is powered from the V <sub>CC</sub> supply. An internal 4.5V supply is generated from the V <sub>CC</sub> supply to power most of the internal circuitry. A bypass capacitor with a minimum value of 4.7μF low ESR tantalum or ceramic capacitor should be tied between this pin and PGND.
4	BG	Bottom MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between the V <sub>CC</sub> and PGND pins.
5	PGND	Power Ground Pin. Connect this pin closely to the source of the bottom N-channel MOSFETs.
6, 7	NC	No Internal Connection. Always keep this pin floating. It is intentionally skipped to isolate adjacent high-voltage pins.
8	SW	Top MOSFET Driver Return. The top gate driver is biased between BST and the SW pin. Kelvin connect the SW pin to the top MOSFET source pin for high noise immunity.
9	TG	Top MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between the BST and SW pins.
10	BST	Top MOSFET Driver Supply. The top MOSFET gate driver is biased between this pin and the SW pin. An external capacitor should be tied between this pin and the SW pin and placed close to the IC.
11	DGND	Signal Ground Pin. Connect this pin closely to the negative terminals of V <sub>CC</sub> bypassing capacitors. All small-signal components should also connect to this ground. This exposed pad is also connected to PGND and must be soldered to the PCB ground for electrical contact and rated thermal performance.

## TYPICAL PERFORMANCE CHARACTERISTICS

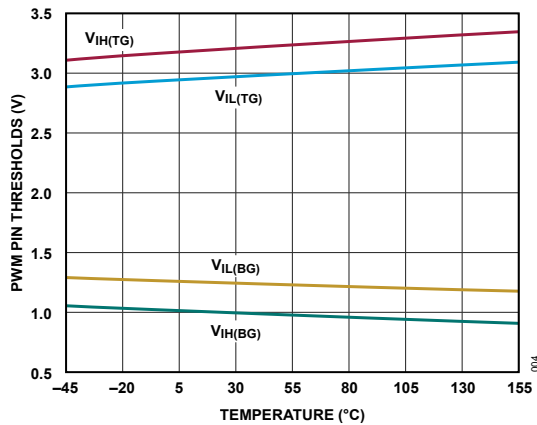


Figure 4. PWM Pin Thresholds vs Temperature

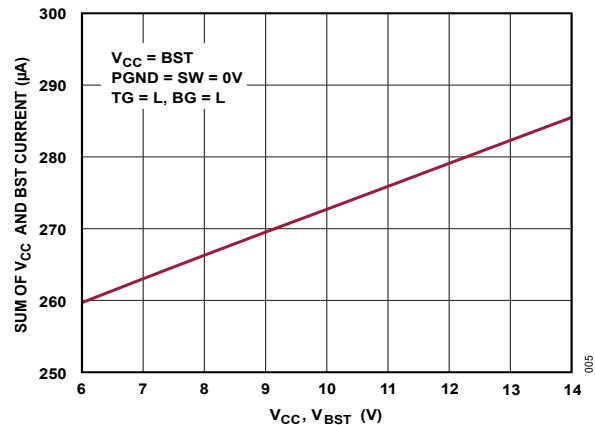


Figure 5. Total Supply Current vs Supply Voltage

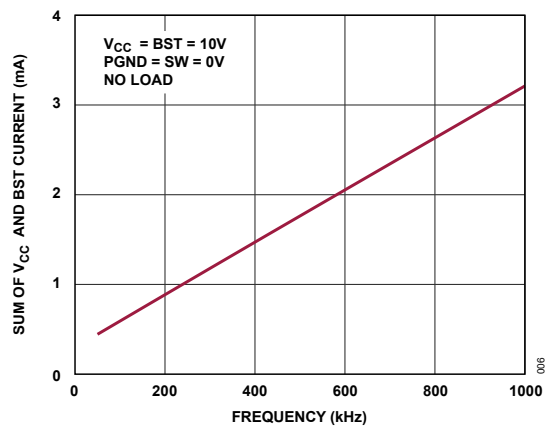


Figure 6. Total Supply Current vs Input Frequency

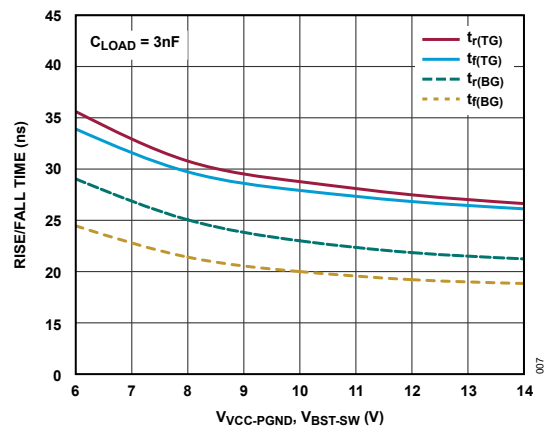


Figure 7. Rise and Fall Time vs Driver Supply Voltage

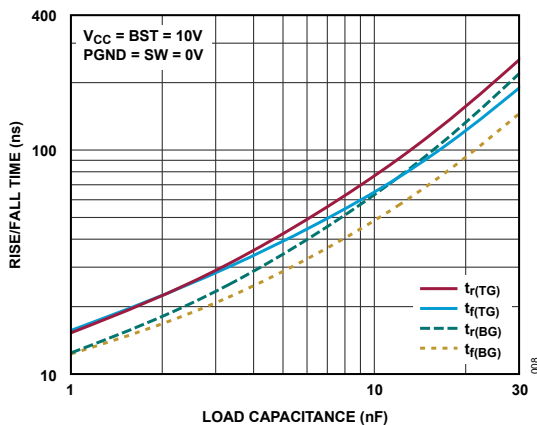


Figure 8. Rise and Fall Time vs Load Capacitance

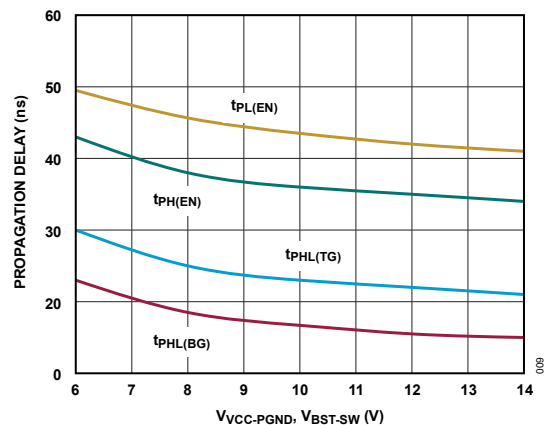


Figure 9. Propagation Delay vs Driver Supply Voltage



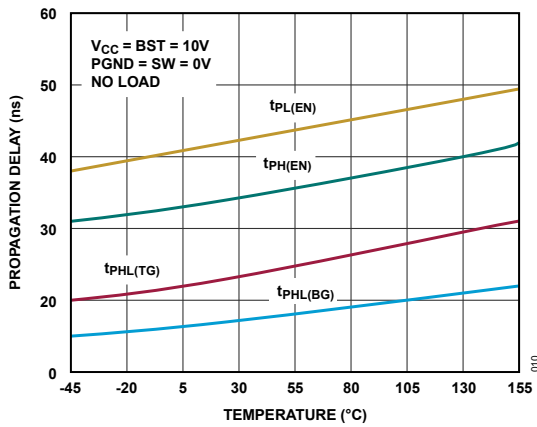


Figure 10. Propagation Delay vs Temperature

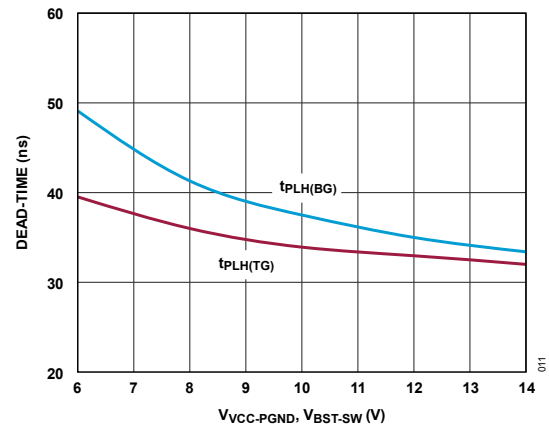


Figure 11. Dead-Time vs Driver Supply

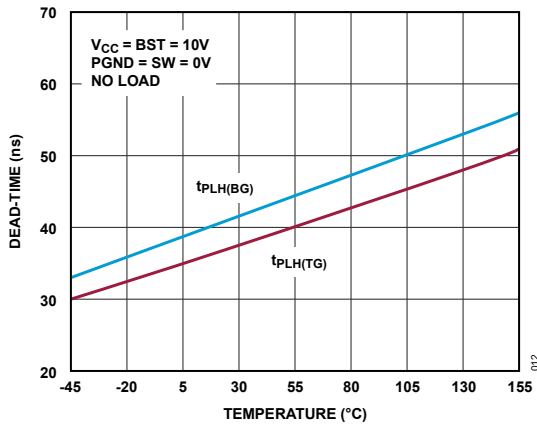


Figure 12. Dead-Time vs Temperature

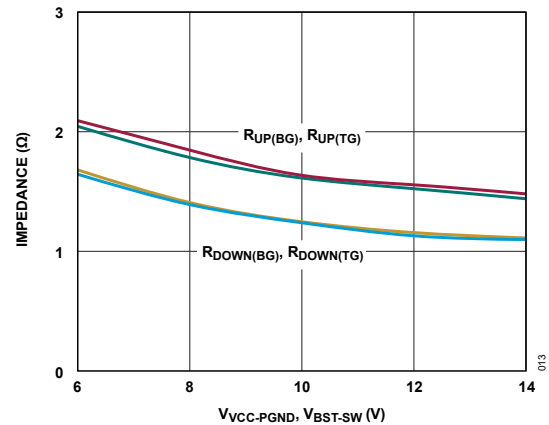


Figure 13. TG/BG Pull-Up and Pull-Down Resistance vs Driver Supply Voltage

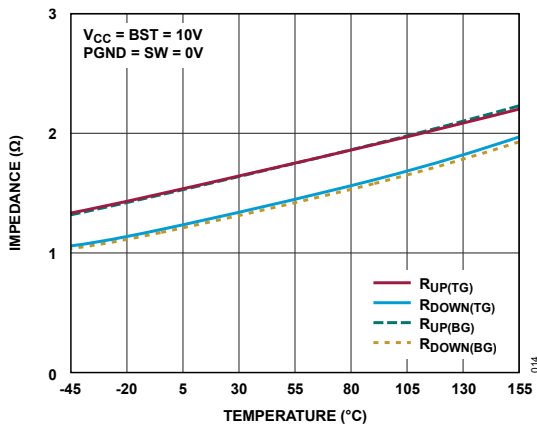


Figure 14. TG/BG Pull-Up and Pull-Down Resistance vs Temperature

## BLOCK DIAGRAM

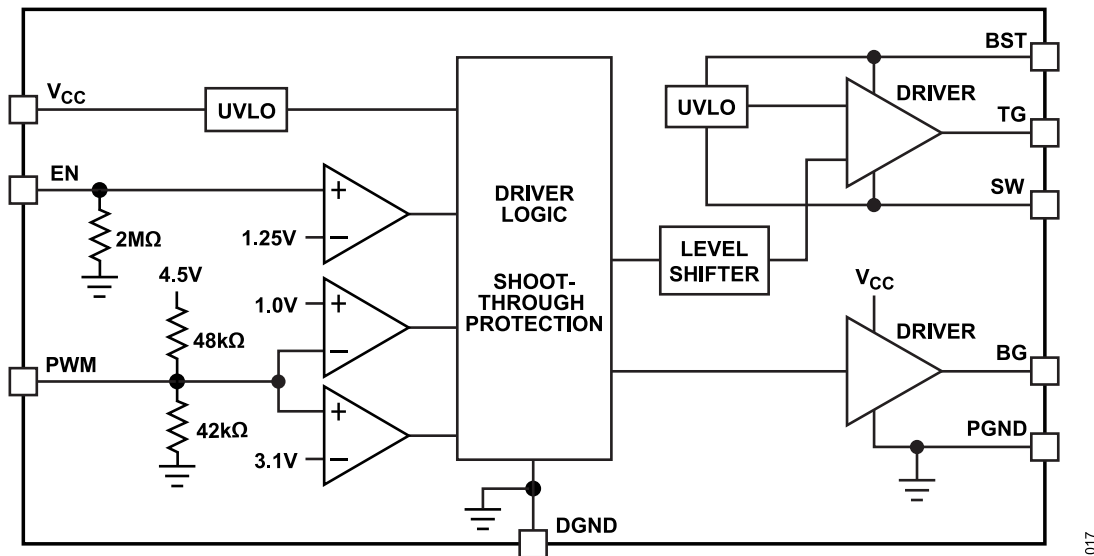


Figure 15. Block Diagram

## THEORY OF OPERATION

## OVERVIEW

The LTC7068 receives a ground-referenced, low-voltage digital PWM signal to drive two N-channel power MOSFETs in a half-bridge configuration. The gate of the low side MOSFET is driven high or low, swinging between  $V_{CC}$  and PGND, depending on the state of the PWM pin. Similarly, the gate of the high side MOSFET is driven complementary to the low side MOSFET, swinging between BST and SW.

 $V_{CC}$  SUPPLY

$V_{CC}$  is the power supply for LTC7068. The bottom gate driver is powered from the  $V_{CC}$  supply. An internal 4.5V supply is generated from the  $V_{CC}$  supply to power the internal circuits referred to DGND.  $V_{CC}$  is independent of  $V_{IN}$ .

## INPUT STAGE (PWM, EN)

The LTC7068 employs a three-state PWM input with fixed transition thresholds. The relationship between the transition thresholds and three input states of the LTC7068 is shown in [Figure 16](#). When the voltage on PWM is greater than the threshold  $V_{IH(TG)}$ , TG is pulled up to BST, turning the high side MOSFET on. This MOSFET will stay on until PWM falls below  $V_{IL(TG)}$ . Similarly, when PWM is less than  $V_{IH(BG)}$ , BG is pulled up to  $V_{CC}$ , turning the low side MOSFET on. BG will stay until PWM increases above the threshold  $V_{IL(BG)}$ .

The hysteresis between the corresponding  $V_{IH}$  and  $V_{IL}$  voltage levels eliminates false triggering due to the noise during switch transitions. However, care should be taken to keep noise from coupling into the PWM pin, particularly in high-frequency, high-voltage applications.

The thresholds are positioned to allow for a region in which BG and TG are low. An internal resistor divider sets the PWM pin voltage into this region if the signal driving the PWM pin goes into a high impedance state.

The EN pin can keep both BG and TG low if the high impedance state is unavailable from the PWM driving signal. Driving the EN pin low keeps both TG and BG off. Driving the EN pin high enables TG and BG switching based on the

PWM input. An internal 2M $\Omega$  pull-down resistor from the EN pin to DGND keeps the EN default state low if its input is not driven.

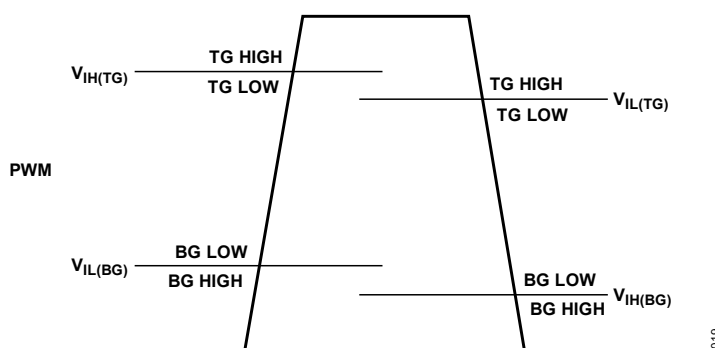


Figure 16. Three-State PWM Operation

## OUTPUT STAGE

A simplified version of the LTC7068's output stage is shown in [Figure 17](#). The pull-up device is a PMOS with a typical 1.6 $\Omega$   $R_{DS(ON)}$ , and the pull-down device is an NMOS with a typical 1.3 $\Omega$   $R_{DS(ON)}$ . The bottom driver supply voltage ranges from 6V to 14V. The wide top driver supply voltage ranges from 4V to 14V. The wide driver supply voltage enables the driving of different power MOSFETs, such as logic level or high threshold MOSFETs. However, the LTC7068 is optimized for higher threshold MOSFETs (for example, BST - SW = 10V and  $V_{CC} - PGND = 10V$ ). The driver output pull-up and pull-down resistance may increase with lower driver supply voltage.

Since the power MOSFETs generally account for the majority of the power loss in a converter, it is important to turn them on and off quickly, thereby minimizing the transition time and power loss. The LTC7068's typical 1.6 $\Omega$  pull-up resistance and 1.3 $\Omega$  pull-down resistance are equivalent to a 2.6A peak pull-up current and 3.6A peak pull-down current at a 10V driver supply. At this supply voltage, both BG and TG can produce a rapid turn-on transition for the MOSFETs with the capability of driving a 3nF load with a 23ns rise time for BG and 29ns rise time for TG.

Furthermore, a strong pull-down on the driver outputs prevents the cross-conduction current. For example, in the half-bridge configuration shown in [Figure 17](#), when BG turns the low side power MOSFET off, and TG turns the high side power MOSFET on, the voltage on the SW pin could rise to  $V_{IN}$  very rapidly. This high-frequency positive voltage transient will couple through the  $C_{GD}$  capacitance of the low-side power MOSFET to the BG pin. If the BG pin is not held down sufficiently, the voltage on the BG pin will rise above the threshold voltage of the low-side power MOSFET, momentarily turning it back on. As a result, both the high side and low side MOSFETs will be conducting, which will cause significant cross-conduction current to flow through the MOSFETs from  $V_{IN}$  to ground, thereby incurring substantial power loss and potentially damaging the MOSFETs. For this reason, short PCB traces for the BG and TG pins, which minimize the parasitic inductances, are recommended.

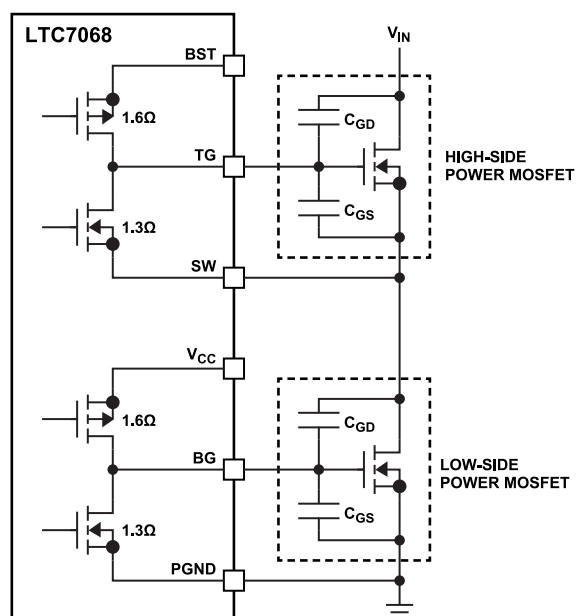


Figure 17. Simplified Output Stage in Half-Bridge Configuration

## PROTECTION CIRCUITRY

When using the LTC7068, care must be taken not to exceed any of the ratings specified in the [Absolute Maximum Ratings](#) section.

The LTC7068 contains an undervoltage lockout detector that monitors the  $V_{CC}$  supply. When  $V_{CC}$  falls below 5.4V, the output pins BG and TG are pulled to PGND and SW, respectively. This turns off both the external MOSFETs. When  $V_{CC}$  reaches adequate supply voltage, normal operation will resume.

Additional undervoltage lockout circuitry is included in the top gate driver supply. The TG will be pulled down to SW when the floating voltage from BST to SW is less than 3.4V. Both  $V_{CC}$  and BST-SW undervoltage lockout circuits have hysteresis.

The normal operation and undervoltage logic are shown in [Table 4](#).

**Table 4. Normal Operation and Undervoltage Logic**

PWM	EN	$V_{CC}$ UVLO	(BST-SW) UVLO	TG	BG
X	L	X	X	L	L
X	X	Y	X	L	L
L	H	N	X	L	H
H	H	N	N	H	L
H	H	N	Y	L	L
HIGH-Z	X	X	X	L	L

Note: X = Don't Care, H = High, L = Low, Y = Yes, and N = No.

## ADAPTIVE SHOOT-THROUGH PROTECTION

Internal adaptive shoot-through protection circuitry monitors the voltage on the external MOSFETs to ensure they do not conduct simultaneously. The LTC7068 does not allow the bottom MOSFET gate (BG) to turn on until the gate-source voltage on the top MOSFET (TG-SW) is sufficiently low, and vice-versa. This feature improves efficiency and reliability by eliminating the potential large shoot-through current through the MOSFETs during switching transitions.

## APPLICATIONS INFORMATION

### BOOTSTRAPPED SUPPLY (BST-SW)

The BST-SW supply of the LTC7068 is a bootstrapped supply. An external boost capacitor,  $C_B$ , connected between BST and SW, supplies the high-side MOSFET gate driver voltage. When the external high-side MOSFET is turned on, the driver places the  $C_B$  voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns it on.

The charge to turn on the external MOSFET is referred to as gate charge,  $Q_G$ , and is typically specified in the external MOSFET datasheet. The boost capacitor,  $C_B$ , must have at least ten times the gate charge to fully turn on the external high-side MOSFET. Gate charge can range from 5nC to hundreds of nC and is influenced by the gate drive level and type of external MOSFET used. For most applications, a capacitor value of 0.1μF for  $C_B$  will be sufficient. However, if multiple MOSFETs are paralleled and driven by the LTC7068,  $C_B$  needs to be increased correspondingly, and the following relationship for the  $C_B$  should be maintained:

$$C_B > \frac{10 \cdot \text{External MOSFET } Q_G}{1V} \quad (1)$$

An external supply, typically  $V_{CC}$  connected through a Schottky diode, is required to keep the  $C_B$  charged. The LTC7068 does not charge the  $C_B$  and always discharges the  $C_B$ . When the TG is high, the total current from BST to SW is typically 105μA; when the TG is low, the total current from BST is typically 9μA.

### POWER DISSIPATION

To ensure proper operation and long-term reliability, the LTC7068 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA}) \quad (2)$$

where:

$T_J$  = junction temperature

$T_A$  = ambient temperature

$P_D$  = power dissipation

$\theta_{JA}$  = junction-to-ambient thermal resistance

Power dissipation consists of standby, switching and capacitive load power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

$P_{DC}$  = quiescent power loss

$P_{AC}$  = internal switching loss at input frequency  $f_{IN}$

$P_{QG}$  = loss due to turning on and off external

MOSFET with gate charge  $Q_G$  at frequency  $f_{in}$

The LTC7068 consumes very little quiescent current. The DC power loss at  $V_{CC} = 10V$  is only  $(10V)(0.15mA) = 1.5mW$ .

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load is shown in the [Typical Performance Characteristics](#) plot of Total Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads  $C_{LOAD}$  on BG and TG at switching frequency  $f_{IN}$ , the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f_{IN})[(V_{BST-SW})^2 + (V_{VCC-PGND})^2] \quad (3)$$

In a typical synchronous buck configuration, the  $V_{CC}$  is connected to the power for the bottom MOSFET driver,  $BGV_{CC}$ .  $V_{BST-SW}$  is equal to  $V_{CC} - V_D$ , where  $V_D$  is the forward voltage drop of the external Schottky diode between  $V_{CC}$  and BST. If this drop is small relative  $V_{CC}$ , the load losses can be approximated as follows:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2 \quad (4)$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its  $V_{GS}$  voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge,  $Q_G$ . The  $Q_G$  value corresponding to the MOSFET's  $V_{GS}$  value ( $V_{CC}$  in this case) can be readily obtained from the manufacturer's  $Q_G$  vs  $V_{GS}$  curves. For identical MOSFETs on BG and TG:

$$P_{QG} \approx 2(Q_G)(f_{IN})(V_{CC}) \quad (5)$$

## BYPASSING AND GROUNDING

The LTC7068 requires proper bypassing on the  $V_{CC}$  and  $V_{BST-SW}$  supplies due to their high-speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimal performance for the LTC7068:

- ▶ Mount the bypass capacitors as close as possible between the  $V_{CC}$  and PGND pins and the BST and SW pins. The leads should be shortened as much as possible to reduce lead inductance.
- ▶ Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC7068 switches greater than 3A peak currents, and any significant ground drop will degrade signal integrity.
- ▶ Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- ▶ Kelvin connect the TG pin to the top MOSFET gate and the SW pin to the top MOSFET source. Kelvin connect the BG pin to the bottom MOSFET gate and PGND to the bottom MOSFET source. Keep the copper trace between the driver output pin and load short and wide.

- Be sure to solder the Exposed Pad on the back side of the LTC7068 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than specified for the packages.

## TYPICAL APPLICATION

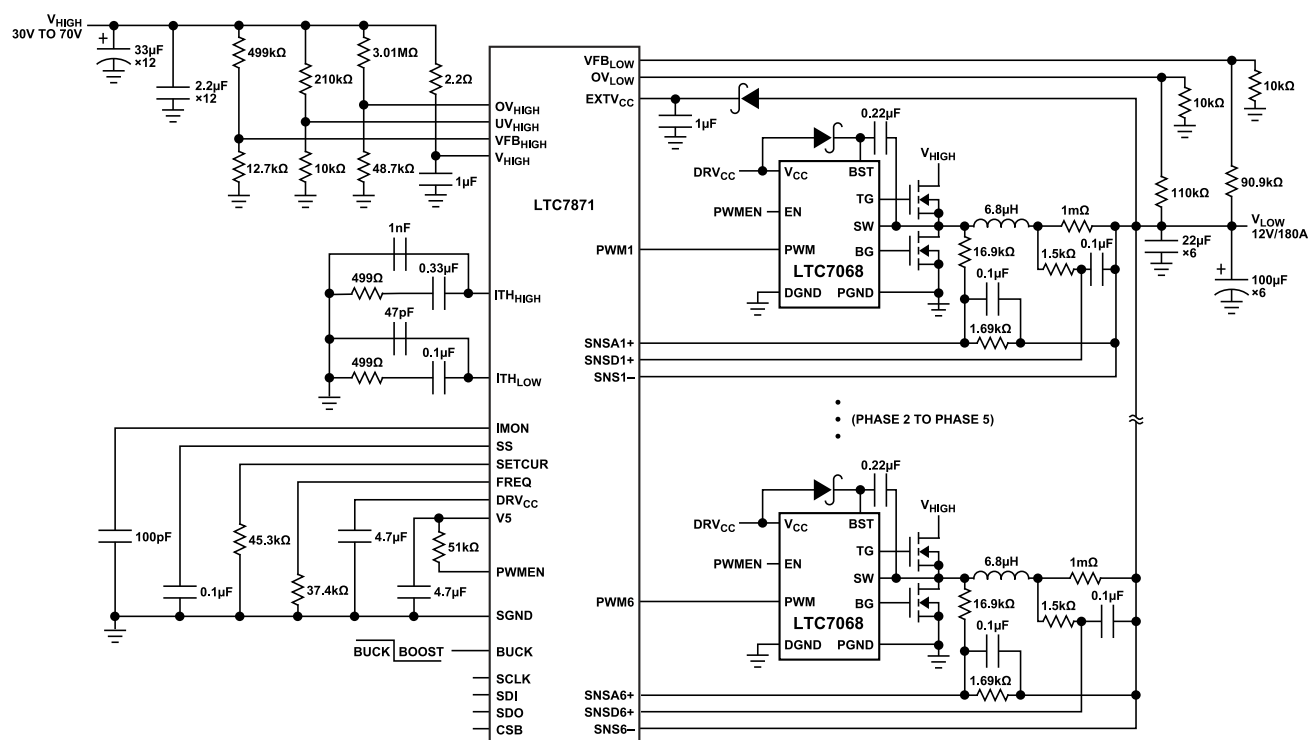


Figure 18. 6-Phase 12V/180A Converter with the LTC7068 and MOSFETs Using LTC7871

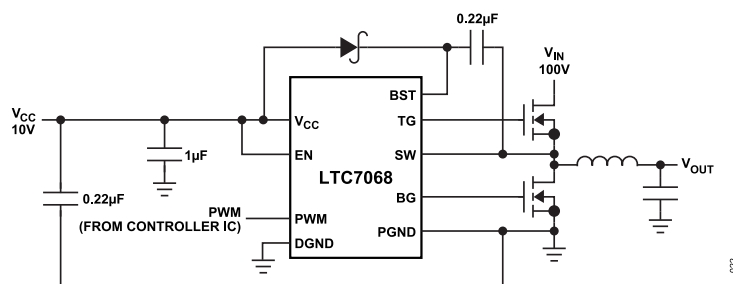


Figure 19. High Input Voltage Buck Converter

## ORDERING GUIDE

**Table 5. Ordering Guide**

LEAD-FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7068RMSE#PBF	LTC7068RMSE#TRPBF	LTHRH	10-LEAD Plastic MSOP	-40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

The LTC7068 is guaranteed to meet performance specifications over the full -40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with the #TRMPBF suffix.

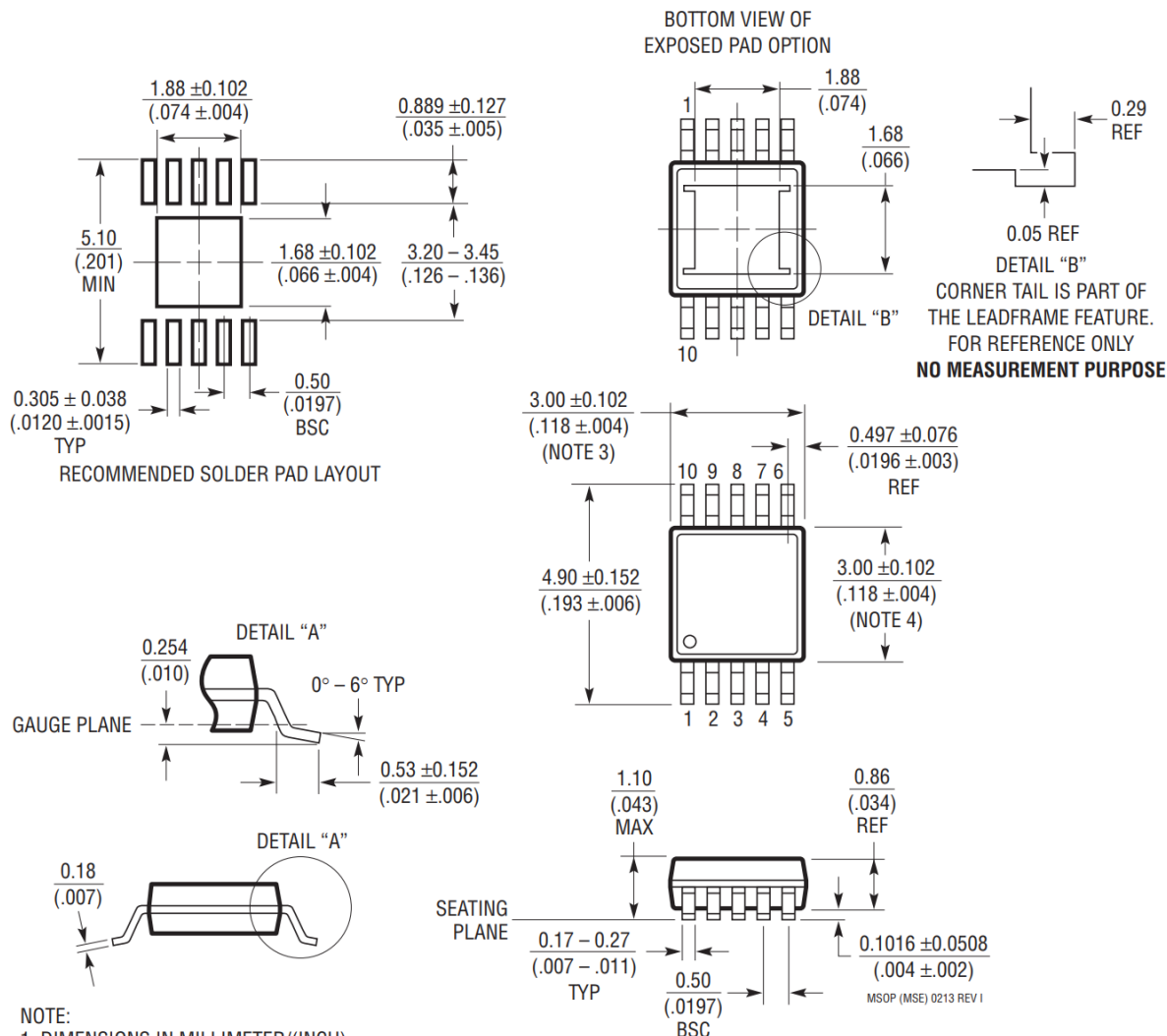


## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC7065</a>	100V Half Bridge Driver with Adaptive Shoot-Through Protection	Up to 100V Supply Voltage, $6V \leq V_{CC} \leq 14V$ , 1.3 $\Omega$ Pull-Down, 1.6 $\Omega$ Pull-Up, Three-State PWM Input with Enable Pin, Thermally Enhanced MSOP-10
<a href="#">LTC7060</a>	100V Half-Bridge MOSFET Driver with Floating Grounds and Programmable Dead-Time and shoot-through protection	Up to 100V Supply Voltage, $6V \leq V_{CC} \leq 14V$ , 0.8 $\Omega$ Pull-Down, 1.5 $\Omega$ Pull-Up, Three-State PWM Input with Enable Pin, Thermally Enhanced MSOP-12
<a href="#">LTC7061</a>	100V Half-Bridge MOSFET Driver with Floating Grounds and Programmable Dead-Time and shoot-through protection	Up to 100V Supply Voltage, $6V \leq V_{CC} \leq 14V$ , 0.8 $\Omega$ Pull-Down, 1.5 $\Omega$ Pull-Up, Dual PWM Inputs, Thermally Enhanced MSOP-12
<a href="#">LTC7062</a>	100V Dual High-Side MOSFET Gate Driver with Floating Ground Capability	Up to 100V Supply Voltage, Shoot-Through Protection is Disabled, which allows Both MOSFETs to Turn-on at the same time
<a href="#">LTC7063</a>	150V Half-Bridge Driver with Floating Grounds and Adjustable Dead-Time	Up to 150V Supply Voltage, $6V \leq V_{CC} \leq 14V$ , 0.8 $\Omega$ Pull-Down, 1.5 $\Omega$ Pull-Up, Three-State PWM Input with Enable Pin, Thermally Enhanced MSOP-12
<a href="#">LTC4449</a>	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, $4V \leq V_{CC} \leq 6.5V$ , 3.2A Peak Pull-Up/4.5A Peak Pull-Down
<a href="#">LTC4442/LTC4442-1</a>	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, $6V \leq V_{CC} \leq 9.5V$ , 2.4A Peak Pull-Up/5A Peak Pull-Down
<a href="#">LTC4446</a>	High Voltage Synchronous N-Channel MOSFET Driver without Shoot-Through Protection	Up to 100V Supply Voltage, $7.2V \leq V_{CC} \leq 13.5V$ , 2.5A Peak Pull-Up/3A Peak Pull-Down

## OUTLINE DIMENSIONS

**MSE Package**  
**10-Lead Plastic MSOP, Exposed Die Pad**  
 (Reference LTC DWG # 05-08-1664 Rev I)



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