Multiphase Current Mode Step-Up DC/DC Controller

FEATURES

- Wide Input Voltage Range: 3V to 40V
- 2-Phase Interleaved Operation Reduces Input and Output Capacitance Requirements
- SPI Interface for Output Voltage Adjustment
- Low Shutdown Current < 1µA
- Internal 5V Low Dropout Voltage Regulator Supplied from V_{IN} or V_{OUT}
- PGOOD Output Status Reporting Pin
- Programmable Internal Frequency: 100kHz to 2MHz
- Frequency Synchronization
- Clock Output for 4- or 8-Phase Operation
- Spread Spectrum Frequency Modulation (SSFM) for EMI Reduction
- Available in a 3mm × 4mm 20-Lead Side Solderable QFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive, Telecom, and Industrial Power Supplies

DESCRIPTION

The LT8277 is a 2-phase constant frequency, current mode boost and SEPIC controller that drives N-channel power MOSFETs. The 2-phase interleaved operation reduces system filtering capacitance requirements. An internal LDO regulator draws power from V_{IN} or V_{OUT} to provide a 5V supply for the gate drivers. The fixed frequency, current-mode architecture results in stable operation over a wide range of supply and output voltages. The operating frequency of the LT8277 can be set over a 100kHz to 2MHz range with an external resistor or can be synchronized to an external clock using the SYNC pin. The CLKOUT and SYNC pins allow multiple LT8277 devices to work together, enabling 4- or 8-phase operation.

The LT8277 output voltage ranges from 9V to 60V, which can be set through the SPI interface. A window comparator on the V_{OUT} pin reports via the PGOOD pin, providing an output voltage status indication. The device is available in a 20-Lead 3mm x 4mm side-solderable QFN package.

TYPICAL APPLICATION

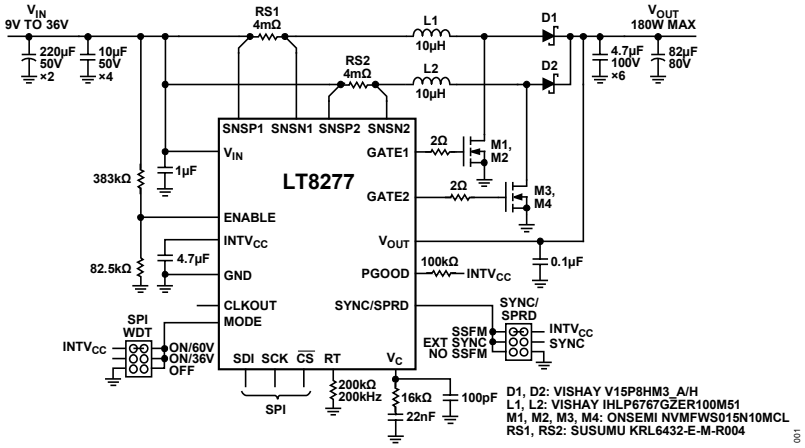

Figure 1. 180W Automotive Pre-Boost Converter with SPI

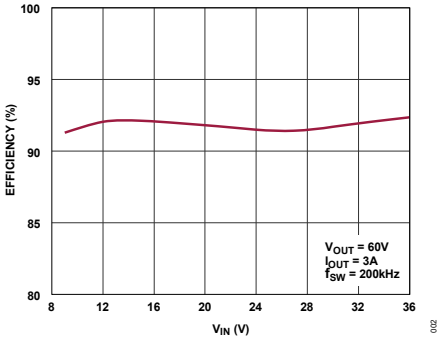

Figure 2. Efficiency vs. Input Voltage

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	NATURE OF CHANGE	PAGE NUMBER
0	10/23	Initial Release	—
A	01/24	Updated Package Outline Drawing Updated Ordering Guide Information	29 30

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{ENABLE} = 12V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{IN} Operating Supply Range	V_{IN_OPR}	This specification is valid over the full operating temperature range		3		40	V
V_{IN} Start-Up Range	V_{IN_START}	This specification is valid over the full operating temperature range		5		40	V
V_{IN} Pin Quiescent Current	I_Q	V_{MODE} = 0V, No SPI Input, No Switching			2	4	mA
V_{IN} Pin Shutdown Current	I_{VIN_SHDN}	V_{ENABLE} = 1.15V				15	µA
		V_{ENABLE} = 0.4V				1	
ENABLE Threshold Voltage (Falling)	$V_{ENABLE\_FALLING}$	This specification is valid over the full operating temperature range		1.16	1.26	1.36	V
ENABLE Rising Hysteresis	V_{ENABLE_HYS}				60		mV
ENABLE Pin Bias Current, Device Off	I_{ENABLE_OFF}	V_{ENABLE} = 1.15V			2.5		µA
ENABLE Pin Bias Current, Device On	I_{ENABLE_ON}	V_{ENABLE} = 1.4V			10	100	nA
Internal LDO Regulator							
$INTV_{CC}$ Regulation Voltage	V_{INTVCC}	I_{INTVCC} = -30mA, V_{MODE} = 0V, No SPI Input	This specification is valid over the full operating temperature range	4.8	5	5.2	V
$INTV_{CC}$ Undervoltage Lockout (Falling)	V_{INTVCC_UVLO}			3.8	4	4.2	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis	$V_{INTVCC\_UVLOHYS}$				170		mV
$INTV_{CC}$ Current Limit	I_{INTVCC_LIM}	V_{IN} = 12V, V_{INTVCC} = 4V			140		mA
Dropout (V_{IN} – V_{INTVCC})		V_{IN} = 5V, I_{INTVCC} = -40mA, Not Switching			300		mV
Current Comparator							
V_{SENSE} (V_{SNSP} – V_{SNSN}) Limit	V_{SENSE_LIM}	This specification is valid over the full operating temperature range		65	75	85	mV

(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{ENABLE} = 12V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{SENSE} Matching		PH1 to PH2 Maximum Current Sense Threshold Mismatch		-5		5	mV
SNSP1, SNSP2 Pin Current		V_C = 1.25V			100		µA
SNSN1, SNSN2 Pin Current		V_C = 1.25V			1	4	µA
Error Amplifier							
Error Amplifier Transconductance	g_{MEA}	Using SPI Code for 60V			100		µS
Error Amplifier Output Resistance	R_{EA}	Using SPI Code for 60V			4		MΩ
V_C Current Mode Gain ($\Delta V_{VC}/\Delta V_{SENSE}$)	G_{VC}	2-Phase Operation (V_C = 1V)			8		V/V
Internal V_C Upper Limit Clamp Voltage	V_{C_CLAMP}			1.38	1.42	1.46	V
V_C Phase 2 Shed Threshold (Falling)	V_{C_SHED}				675		mV
V_C Phase 2 Add Threshold (Rising)	V_{C_ADD}				750		mV
V_C Source Current	I_{VC_SOURCE}				–30		µA
V_C Sink Current	I_{VC_SINK}				30		µA
V_{OUT} Range	V_{OUT}			9		60	V
V_{OUT} Regulation Accuracy		V_{OUT} = 9V Typical	This specification is valid over the full operating temperature range	8.8	9	9.2	V
		V_{OUT} = 60V Typical	This specification is valid over the full operating temperature range	58	60	62	

(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{ENABLE} = 12V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Oscillator							
Switching Frequency	f_{SW}	R_T = 523kΩ	This specification is valid over the full operating temperature range	90	100	110	kHz
		R_T = 11kΩ		1.8	2	2.2	MHz
Minimum Off Time	$t_{GATE\_OFF\_MIN}$	This specification is valid over the full operating temperature range		35	55	77	ns
Minimum On Time	$t_{GATE\_ON\_MIN}$				70		ns
SYNC Input Low	V_{SYNC_IL}					0.4	V
SYNC Input High	V_{SYNC_IH}			1.6			V
Spread Spectrum Frequency Range				100		122	$\%f_{SW}$
Spread Spectrum Modulation Frequency					1.0		kHz
Logic							
PGOOD Output Low	V_{PGOOD_OL}	I_{PGOOD} = 1mA				300	mV
PGOOD Upper Limit		Fraction of Programmed V_{OUT}			105		%
PGOOD Lower Limit		Fraction of Programmed V_{OUT}			95		%
Gate Driver							
Driver Pull-UP $R_{DS(ON)}$	R_{GATE_UP}				1		Ω
Driver Pull-DOWN $R_{DS(ON)}$	R_{GATE_DN}				1		Ω
SPI Interface							
CS, SCK, SDI Input Low Voltage	V_{SPI_IL}					0.8	V
CS, SCK, SDI Input High Voltage	V_{SPI_IH}			1.7			V
t_{CSI}, CS Idle Time	t_{CSI}			500			ns
t_{SC}, CS Setup Time	t_{SC}			300			ns

(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{ENABLE} = 12V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
t_{HC}, CS Hold Time	t_{HC}		300			ns
t_{SD}, SDI Setup Time	t_{SD}		300			ns
t_{HD}, SDI Hold Time	t_{HD}		300			ns
t_{CP}, SCK Clock Period	t_{CP}		750			ns
t_{CW}, SCK Pulse Width	t_{CW}		350			ns
t_{WDT}, Watch Dog Timer Expiration Time	t_{WDT}		20			ms

Timing Diagram

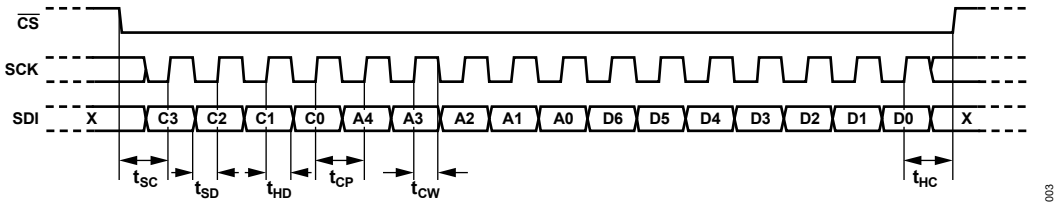


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, ENABLE, SNSP1, SNSP2	40V
SNSP1-SNSN1, SNSP2-SNSN2	±0.3V
V_{OUT}, PGOOD	62V
RT, GATE1, GATE2, CLKOUT, V_C	([1])
SYNC/SPRD	6V
SDI, SCK, $\overline{CS}$, MODE	6V
$INTV_{CC}$	6V
Operating Junction Temperature ([2], [3])	-40°C to 150°C
Storage Temperature Range	-60°C to 150°C

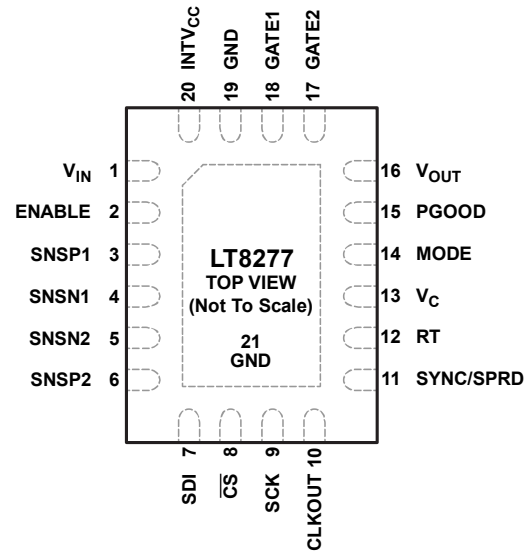
[1] The GATE1, GATE2, and CLKOUT pins are driven either to GND or $INTV_{CC}$ by internal switches. Do not connect these pins or the RT pin externally to a power supply.

[2] The LT8277R is guaranteed to meet performance specifications over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

[3] The LT8277 includes overtemperature protection that is intended to protect the device during momentary overload conditions. The junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. T_{JMAX} = 150°C, θ_{JA} = 52°C/W.
2. EXPOSED PIN. EXPOSED PIN = GND. THE EXPOSED PAD (PIN 21) MUST BE SOLDERED TO PCB GND. PIN 19 IS INCLUDED AS A GROUND PIN FOR ROUTING CONVENIENCE ONLY.

004

Figure 4. Pin Diagram

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	V_{IN}	Input Supply Pin. A minimum 0.1µF local bypass capacitor must be placed close to this pin.
2	ENABLE	Enable and Undervoltage Lockout Pin. When the voltage at this pin falls below 1.26V (typical), switching stops and the part shuts down. A hysteresis of approximately 60mV is included when returning over 1.26V. Drive this pin high with a logic level greater than 1.4V or low with a logic level below 0.3V for simple ON/OFF functionality or tie it through a resistive voltage divider to the V_{IN} for a precise input undervoltage shut-down threshold.
3, 6	SNSP1, SNSP2	Connection Points for the Positive Terminals of the Current Sense Resistors in series with the inductors. These pins must be Kelvin connected to the high side of the sense resistor for each phase. For more information, see the *PCB Layout Guidelines* in the Applications Information section.
4, 5	SNSN1, SNSN2	Connection Points for the Negative Terminals of the Current Sense Resistors in series with the inductors. These pins must be Kelvin connected to the low side of the sense resistor for each phase. For more information, see the *PCB Layout Guidelines* in the Applications Information section.
7	SDI	Data Input Pin for SPI port.

8	$\overline{CS}$	Chip Select Pin for SPI port.
9	SCK	Serial Clock Input Pin for SPI port. All serial data transfers are sampled on rising edges of this clock.
10	CLKOUT	Buffered Version of Internal Clock. The buffered version is either 45° or 90° out-of-phase with the switching clock of phase 1. This pin can be set to high-Z mode if it is not needed.
11	SYNC/ SPRD	The SYNC/SPRD Pin can be used to synchronize the internal oscillator to an external logic level signal. Tie to $INTV_{CC}$ to enable internal spread spectrum frequency modulation, and tie to the ground or leave open if unused.
12	RT	Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND. Do not leave this pin open.
13	V_C	Transconductance Error Amplifier Output Pin used to stabilize the loop with an RC network. Read more in the Applications Information section for details about compensation.
14	MODE	Wake-up and Watchdog Timer Mode Selection Pin. Tie this pin to $INTV_{CC}$ to wake up with V_{OUT} programmed to 60V and return to 60V on watchdog timer expiration. Tie this pin to INTVCC/2 or leave it open to wake up with V_{OUT} set to 36V and return to 36V on watchdog timer expiration. Tie this pin to the ground to disable the watchdog timer and delay wake-up after ENABLE goes high until a valid SPI command has programmed the output voltage target.
15	PGOOD	Power Good Indicator Pin. Open-drain logic output is pulled to GND when the output voltage is more than around ±5% away from the programmed regulation target.
16	V_{OUT}	Output Voltage Sense Pin. Also, it supplies power to $INTV_{CC}$ when the input voltage drops below 5V. The output regulation target is programmed via the SPI port. A minimum 0.1µF local bypass capacitor must be placed close to this pin.
17, 18	GATE2, GATE1	N-Channel MOSFET Gate Driver Output Pin. Switches between $INTV_{CC}$ and GND. Driven to GND when the IC is in thermal shutdown or when $INTV_{CC}$ is below its undervoltage lockout, or the part is shut down by the ENABLE pin.
20	$INTV_{CC}$	Internal Low-Dropout Regulator Output Pin. $INTV_{CC}$ is regulated to 5V and requires a 4.7µF bypass capacitor. This regulator supplies power to internal circuitry, and connecting certain external loads may interfere with the operation of the part.
19, 21	GND	Ground Pin. The exposed pad (pin 21) must be soldered to PCB ground. Pin 19 is included as a ground pin for routing convenience only.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

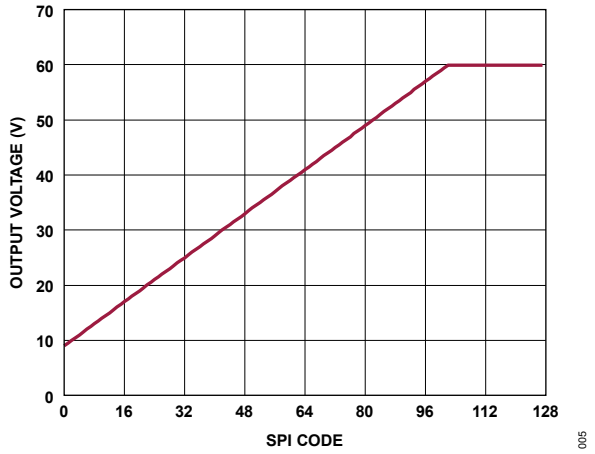


Figure 5. V_{OUT} Regulation Point vs. Programmed SPI Code

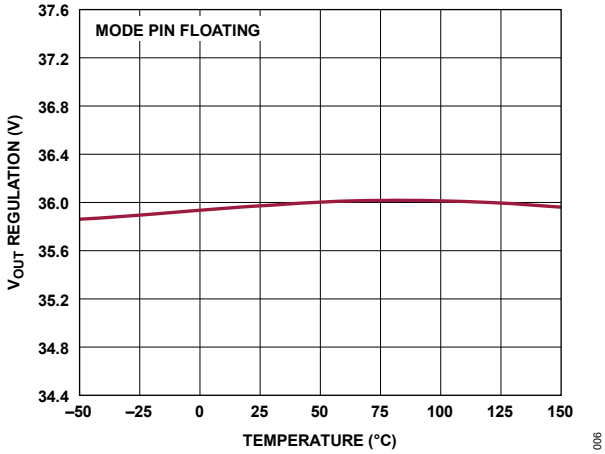


Figure 6. 36V V_{OUT} Regulation vs. Temperature

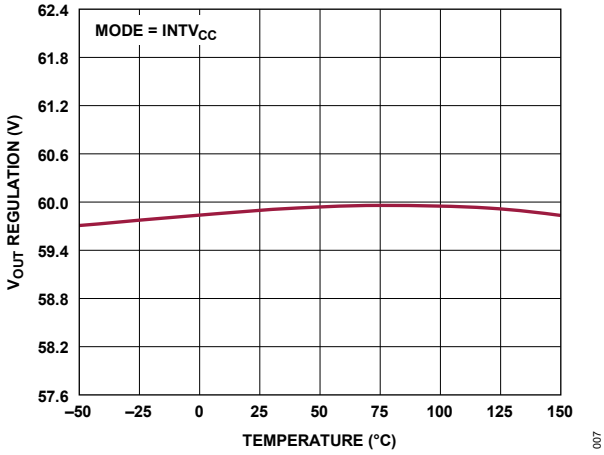


Figure 7. 60V V_{OUT} Regulation vs. Temperature

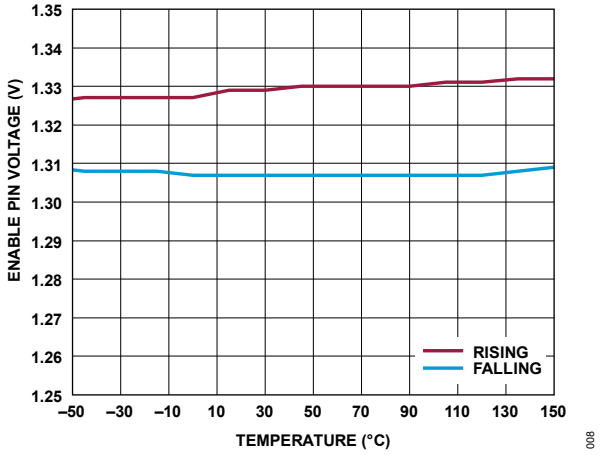


Figure 8. ENABLE Pin Shutdown Threshold vs. Temperature

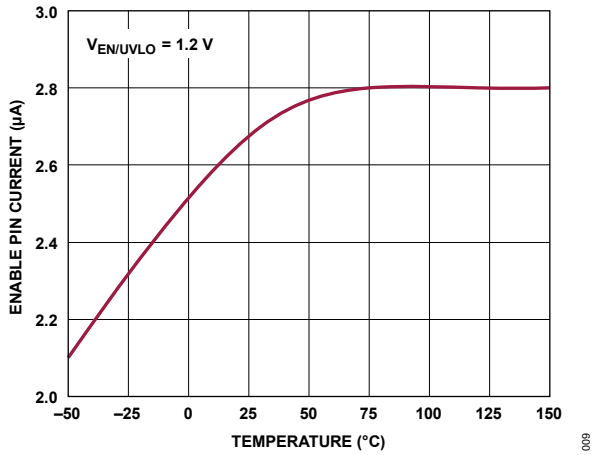


Figure 9. ENABLE Pin Hysteresis Current vs. Temperature

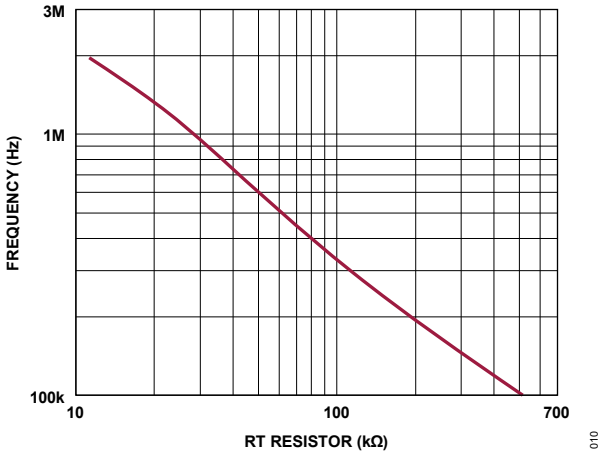


Figure 10. Switching Frequency vs. RT

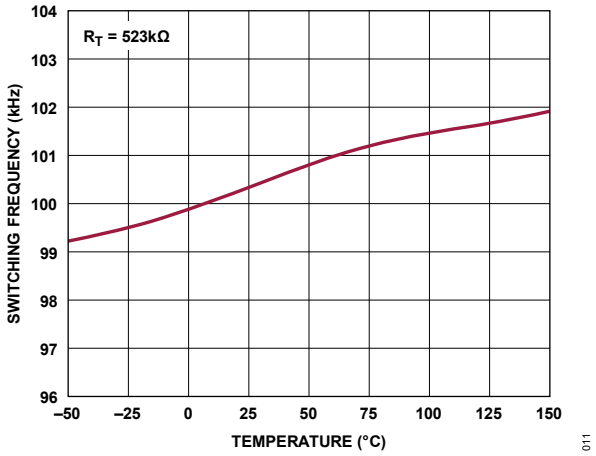


Figure 11. Switching Frequency (100kHz) vs. Temperature

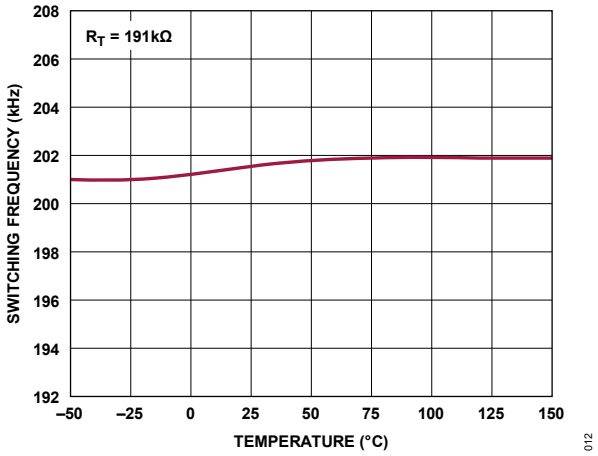


Figure 12. Switching Frequency (200kHz) vs. Temperature

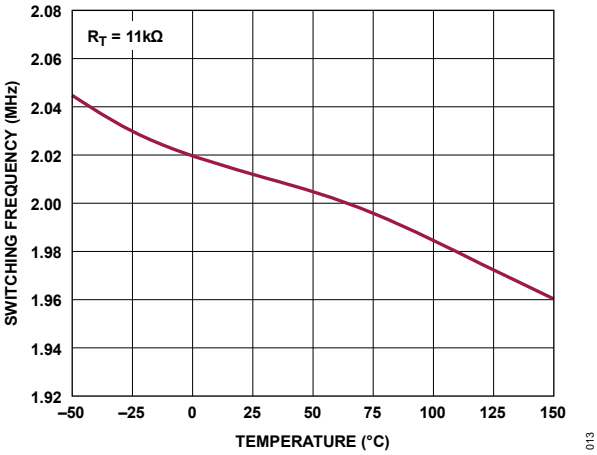


Figure 13. Switching Frequency (2MHz) vs. Temperature

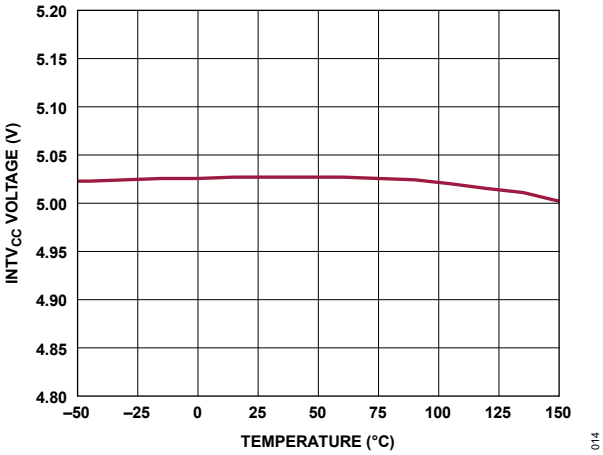


Figure 14. $INTV_{CC}$ Voltage vs. Temperature

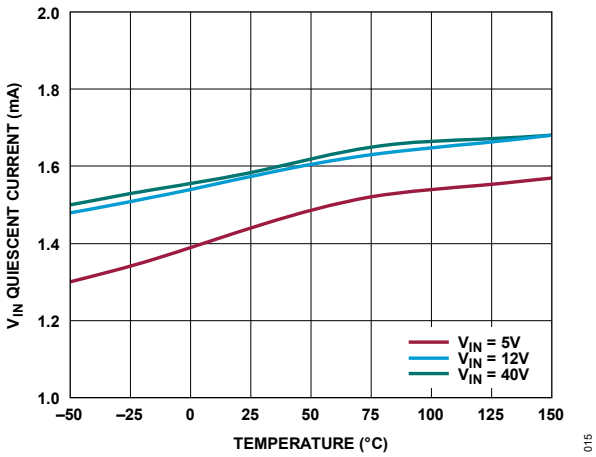


Figure 15. V_{IN} Quiescent Current vs. Temperature

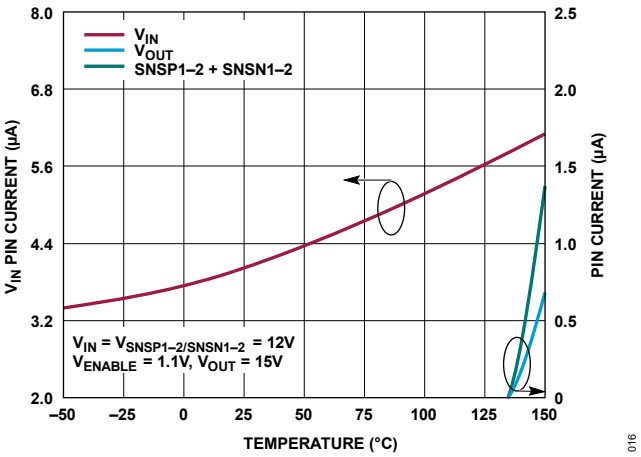


Figure 16. Shutdown Current vs. Temperature

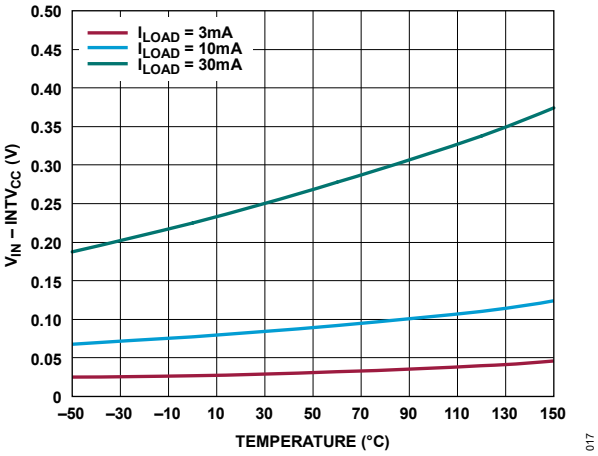


Figure 17. $INTV_{CC}$ Droupout vs. Temperature

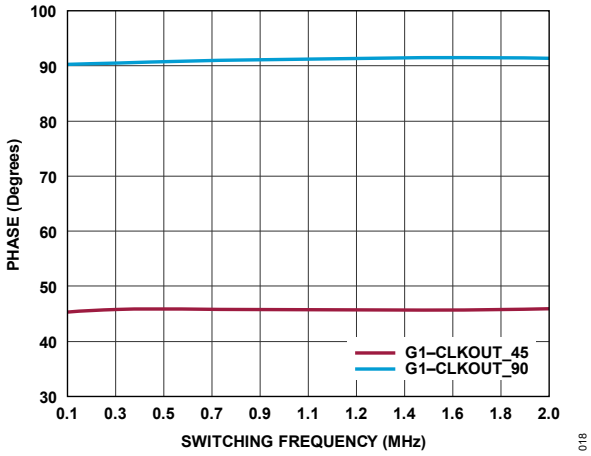


Figure 18. GATE1 to CLKOUT Phase vs. Switching Frequency

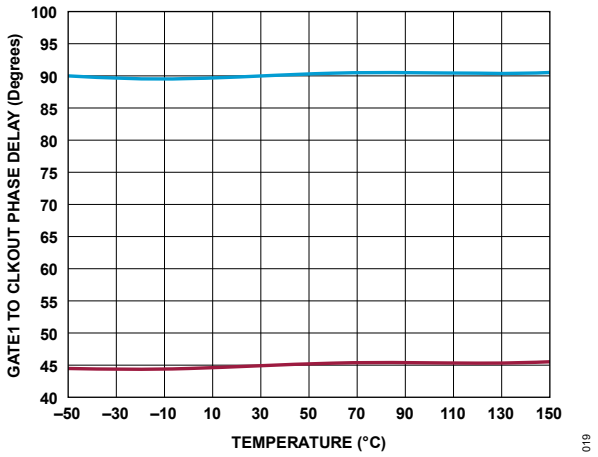


Figure 19. GATE1 to CLKOUT Phase at 100kHz vs. Temperature

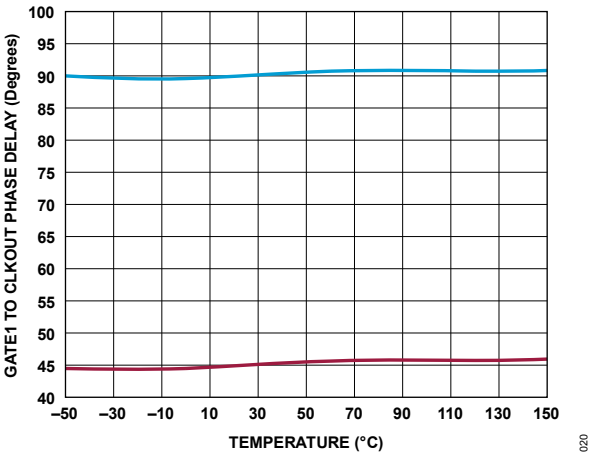


Figure 20. GATE1 to CLKOUT Phase at 200kHz vs. Temperature

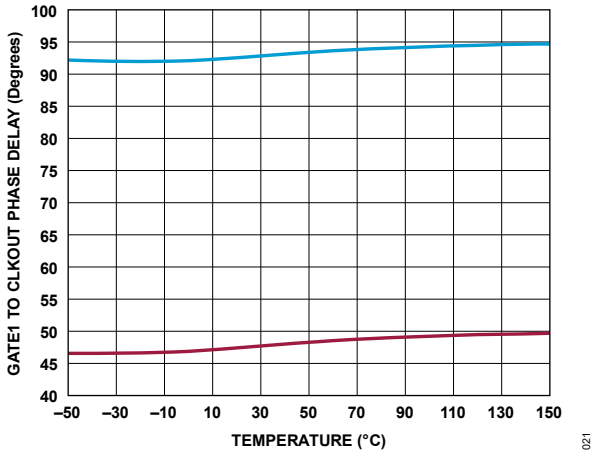


Figure 21. GATE1 to CLKOUT Phase at 2MHz vs. Temperature

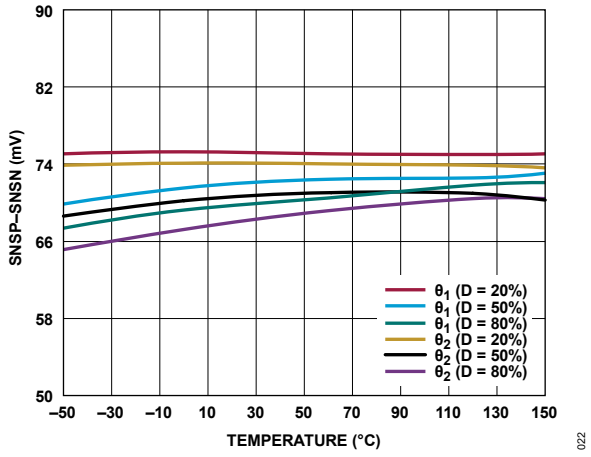


Figure 22. SNSP–SNSN Limit vs. Temperature

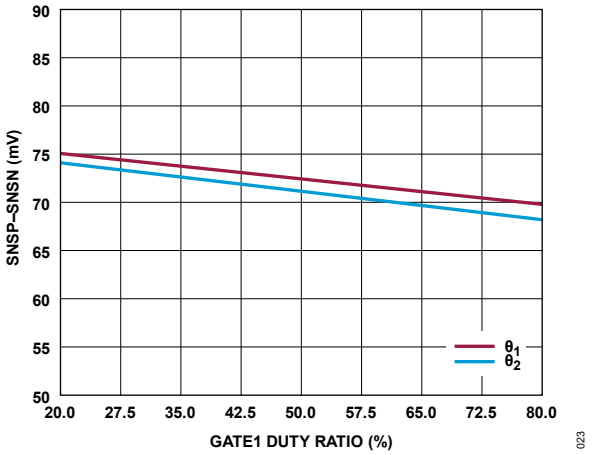


Figure 23. SNSP–SNSN Limit vs. GATE Duty Cycle for Both Phases

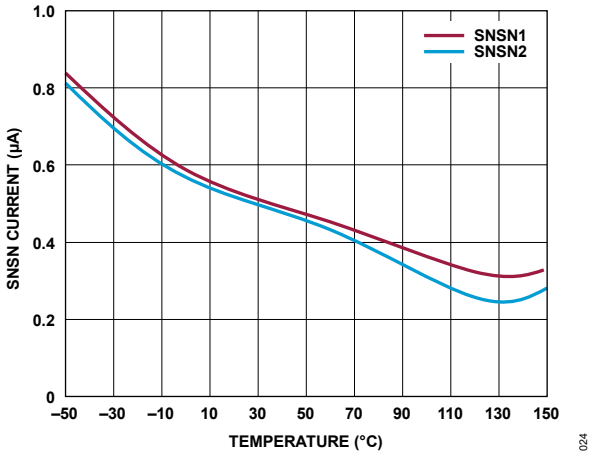


Figure 24. SNSN1 and SNSN2 Pin Current vs. Temperature

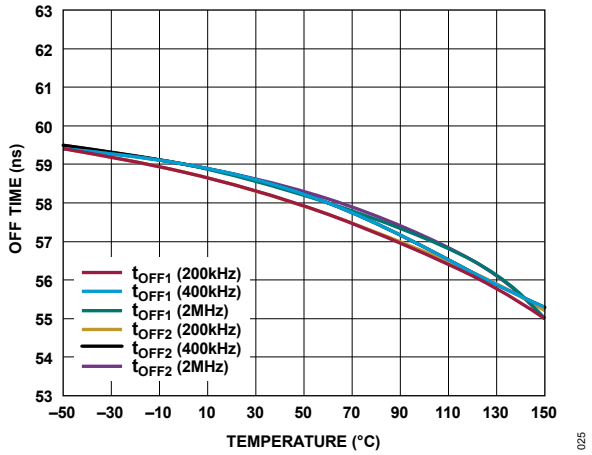


Figure 25. Minimum Off Time vs. Temperature

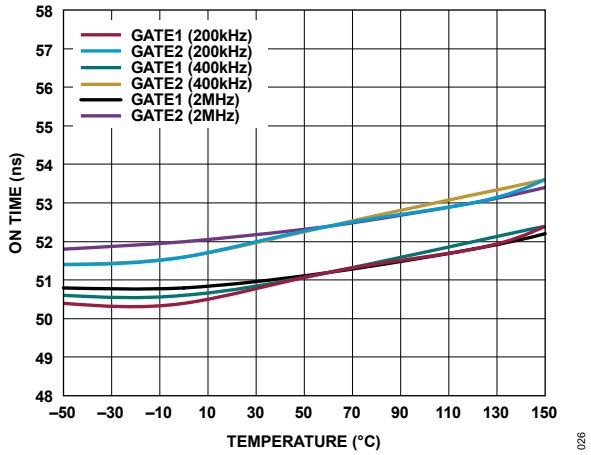


Figure 26. Minimum On Time vs. Temperature

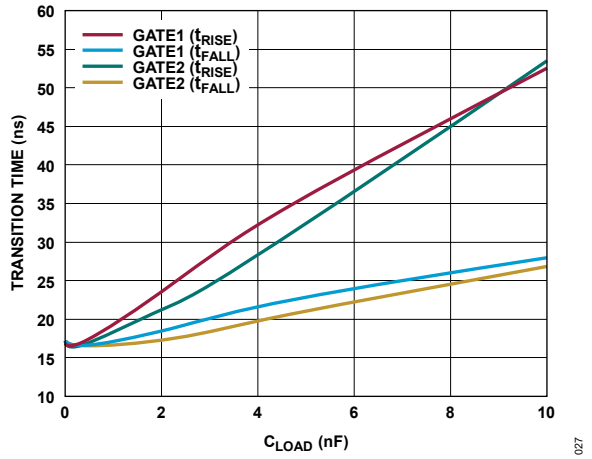


Figure 27. Gate Rise and Fall Time vs. Load Capacitance

BLOCK DIAGRAM

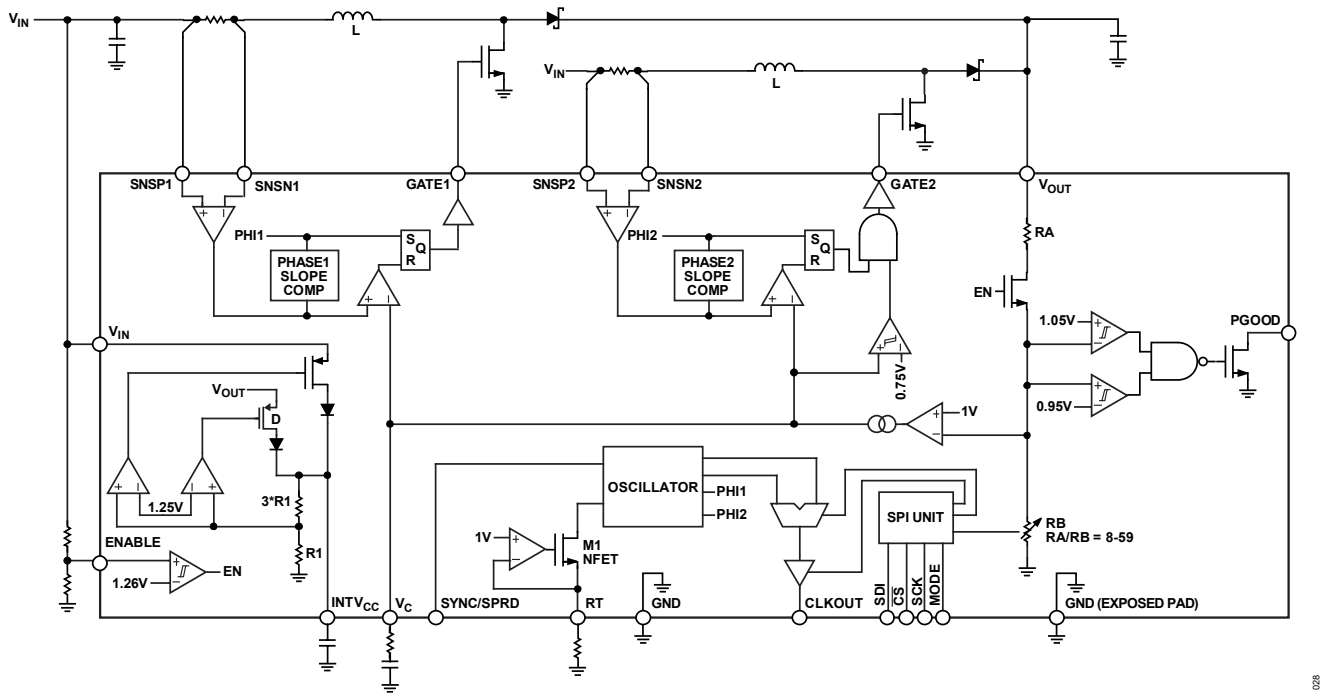


Figure 28. Block Diagram

THEORY OF OPERATION

The LT8277 is a multiphase, constant frequency, peak current mode step-up DC/DC controller. Each LT8277 controls two power stages operated 180° out of phase from one another. Up to 4x LT8277 devices can operate together to enable 4- or 8-phase configurations. To best understand the following discussion, see *Figure 28*.

Each phase contains an SR latch set by a pulse from the clock associated with that phase. While the SR latch remains set, the gate driver turns on the external NMOS switch for that phase. The SR-latch is reset when the voltage difference SNSP-SNSN exceeds the value commanded by the error amplifier. The error amplifier output, V_C, commands current in both phases. The error amplifier compares the output voltage, measured by an internal, programmable, resistive voltage divider, to an internal 1V reference. When the fraction of V_{OUT} seen at the middle of this divider exceeds or falls below 1V, the error amplifier moves the voltage at the V_C node to change the current flowing into the load.

The relationship between V_C and the SNSP-SNSN target is well controlled, allowing multiple LT8277 devices to be connected with V_{IN}, V_{OUT}, and V_C, all tied up in parallel. Adding additional phases can reduce input and output ripple for similar values of input and output capacitance, improve EMI performance, and ease PCB thermal design. To reduce losses at light load, where multiphase operation provides less benefit, LT8277 shuts down the second phase when the voltage at V_C sets the peak inductor current to less than about 12.5% of its programmed limit. The second phase resumes operation when the voltage at V_C sets the peak inductor current over around 25% of its programmed limit.

Two comparators continuously monitor V_{OUT} and assert PGOOD when V_{OUT} remains within 5% (typ.) of the programmed value. The SPI port unit controls the internal voltage divider ratio as well as configures the CLKOUT pin behavior. A multiphase, multichip operation uses the CLKOUT pin of one part to drive the SYNC/SPRD pin of the next.

APPLICATIONS INFORMATION

The aim of LT8277 is to simplify the design of high-power pre-boost power supplies. The simple, flexible interface of the part allows for a wide range of voltage and power levels with minimal off-chip components.

Using the SPI Configuration Interface

The LT8277 provides a minimal write-only SPI interface built around a single 12-bit shift register. This interface provides bits for setting the output voltage, configuring the clock output pin (CLKOUT), configuring soft-start, and toggling phase 2 dropout at light load, organized as a 12-bit command word.

Table 4. SPI Operation Configuration

BIT POSITION	DEFAULT	RESET BY WDT	FUNCTION
11	-	No	Reserved, Set This Bit to 0
10	0	No	Soft-Start Speed (1: 4x Faster; 0: Default Speed)
9	0	No	Phase 2 at Light Load (1: Keep; 0: Drop)
8	0	No	Enable CLKOUT Pin Output (1: Enable; 0: Disable)
7	0	No	CLKOUT Pin Phase (0:90°, 1:45°)
6-0	Set by MODE	Yes	Program This Field as: 2 × (V_{OUT} – 9V)

Commands on the SPI interface are protected by a 4-bit CRC, which is prepended to the command, bringing the total number of bits in the SPI command word to 16. A watchdog timer resets the SPI register to its default configuration if a command with a valid CRC is not completed periodically, at least once every 20ms. Expiration of the WDT returns the programmed output voltage to the startup condition specified by the MODE pin unless the WDT is disabled by tying the MODE pin to GND.

Table 5. MODE Pin Settings

MODE	WATCHDOG TIMER	DEFAULT V_{OUT}
0V	Disabled	–
INTVCC/2	Enabled	36V
INTVCC	Enabled	60V

The 4-bit CRC uses the polynomial $x^4 + x + 1$ and initializes all 4 bits of its shift register to logic 1, thereby ensuring the all-0 command is invalid. This CRC is prepended to a valid command word occupying the lower 12 bits of an unsigned integer by the following C function:

```
unsigned int add_crc(unsigned int in)
{
    unsigned int i = 0,
                 p = 0x9800,
                 x = (in << 3);
    while (i < 12) {
        if ((x ^ p) < x) x ^= p;
```

```
        p >>= 1;
        ++i;
    }
    return ((x ^ 1)<<12) | in;
}
```

Inductor Selection

Select inductors with a saturation current higher than the programmed inductor current limit with some margin. The inductance requirements will change based on switching frequency, programmed current limit, and input voltage. Use Equation 1 to estimate the inductance needed for each phase. Additional margin is recommended.

$$L_X > \frac{V_{IN}}{0.3 I_{LMAX} f_{SW}} \quad (1)$$

If parallel RC current sensing is to be used, be sure to select an inductor with reasonable limits on its equivalent series resistance. A table of manufacturers appears in *Table 6*.

Table 6. Recommended Inductor Vendors

NAME	WEBSITE
Wurth Elektronik	www.we-online.com
TDK	www.tdk.com
Vishay	www.vishay.com
Coilcraft	www.coilcraft.com

Input Capacitor Selection

The input capacitor supplies transient current to the part and power stage. The X7R type ceramic chip capacitor is often the best choice. Choose capacitors with a voltage rating around 60% higher than the maximum input voltage the part will see. For a boost or SEPIC converter, the input capacitor can often be smaller than the output capacitor. Use Equation 2 to choose an input capacitor. This relationship assumes that the inductor was selected using the above guidance. Here, n represents the number of phases. Additional margin is recommended.

$$C_{IN} > \frac{0.15 \cdot I_{L,MAX}}{n \cdot V_{RIPPLE} \cdot f_{SW}} \quad (2)$$

The current flowing in the input capacitor of a boost converter is typically lower than the current flowing in the output capacitor. A normalized plot of peak-to-peak current flowing in the input capacitor appears in *Figure 29*.

$$\text{Normalized to: } \frac{V_{IN}}{L \cdot f_{SW}} \quad (3)$$

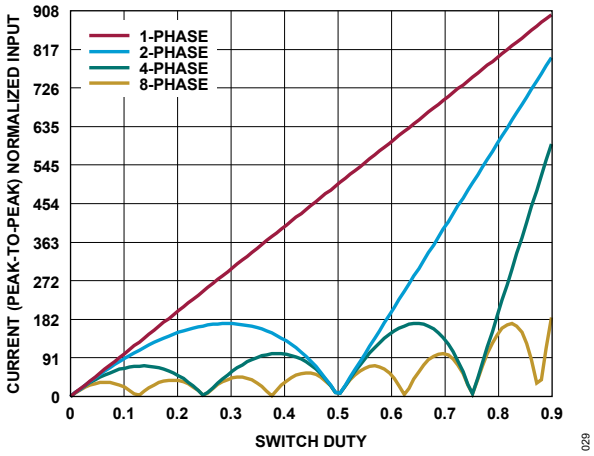


Figure 29. Normalized Input Capacitor Ripple Current for a Boost Converter

Output Capacitor Selection

The output capacitor supplies transient current to the load. The X7R type ceramic chip capacitor is often the best choice. Choose capacitors with a voltage rating around 60% higher than the target output voltage. For a boost or SEPIC converter, the current flowing in the output capacitor can be large. Select the output capacitor based on switching frequency, load current, number of phases (n), and acceptable ripple voltage. Note that increasing the number of phases will decrease the voltage ripple for the same output capacitor and switching frequency. It is best to use a capacitor with low equivalent series resistance and inductance (ESR and ESL) for this role. An additional margin is recommended.

$$C_O > \frac{I_{LOAD} \cdot (V_{OUT} - V_{IN})}{n \cdot V_{OUT} \cdot V_{RIPPLE} \cdot f_{SW}} \quad (4)$$

Keep the current rating in mind when selecting an output capacitor. A plot of output capacitor RMS current over switch duty appears in *Figure 30*. This plot is normalized to the DC load current.

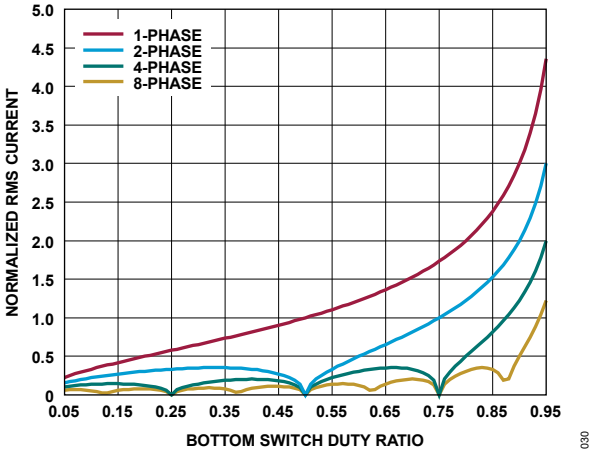


Figure 30. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter

A table of manufacturers appears in *Table 7.*

Table 7. Recommended Capacitors Vendors

NAME	WEBSITE
Panasonic	industrial.panasonic.com/ww
Wurth Elektronik	www.we-online.com
Murata	www.murata.com
Taiyo Yuden	www .yuden.co.jp

Current Sense Structure Selection

Two methods of inductor current sense are available with the LT8277. Note that for both methods, each phase needs its own current sense structure and inductor. The current sense structure programs the inductor current limit. This, in turn, determines the output current limit. If the inductor choice matches the guidelines above, then Equation 5 describes the output current limit. Note that the total output current limit increases with the number of participating phases, n.

$$I_{LIM(OUTPUT)} = 0.85 \cdot I_{L,MAX} \frac{nV_{IN}}{V_{OUT}} \quad (5)$$

The first current sense method uses a resistor connected in series with the inductor on the V_{IN} side. The SNSP and SNSN pins monitor the voltage at this resistor. The inductor current limit using this method is shown in *Figure 31*. Keep the power dissipation capability of the resistor in mind for high-current applications.

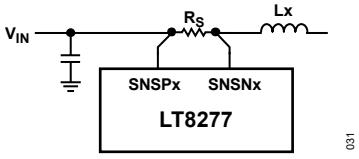


Figure 31. Input Current Limit Programmed by Sense Resistor

$$I_{L,MAX} = \frac{75mV}{R_S} A \quad (6)$$

For some high-current applications, a series-sense resistor may dissipate an unacceptable amount of power. In that case, a parallel RC network can be used to reconstruct the voltage dropped across the inductor's equivalent series resistance (ESR). The components used for this method will not dissipate significant amounts of power, but the accuracy of the inductor current limit can suffer since the tolerance of more components gets introduced to the relationship.

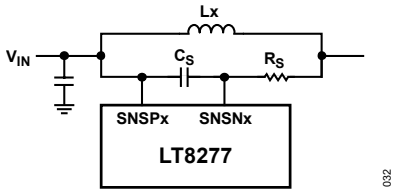


Figure 32. LT8277 DCR Current Sensing

$$I_{L,MAX} = \frac{75\text{mV}}{R_{L,ESR}}\ \text{A} \quad (7)$$

$$R_S C_S = \frac{L}{R_{L,ESR}} \quad (8)$$

This relationship is underspecified, so pick a reasonable pair of R and C values.

Power NMOS Selection

Select a power NMOS for use with LT8277 with a maximum drain-source voltage rating higher than the programmed output voltage and Schottky forward voltage. An additional margin of 10V is recommended. The continuous forward current rating of the switch should exceed the programmed inductor current limit. Keep power dissipation capability in mind for high-power applications. A table of manufacturers appears in *Table 8*.

Table 8. Recommended Power NMOS Vendors

NAME	WEBSITE
Vishay	www.vishay.com
Infineon	www.infineon.com
Renesas	www.renesas.com
ON Semiconductor	www.onsemi.com

Schottky Rectifier Selection

Select a Schottky rectifier for use with the LT8277 with a reverse voltage rating higher than the intended output voltage target. An additional margin of 10V is recommended. The rectifier should have an average forward current rating greater than $I_{LIM(OUTPUT)}/n$, where n is the number of phases, and an instantaneous forward current rating higher than the programmed inductor current limit. A table of manufacturers appears in *Table 9*.

Table 9. Recommended Schottky Vendors

NAME	WEBSITE
Vishay	www.vishay.com
ON Semiconductor	www.onsemi.com
Diodes, Inc.	www.diodes.com
Central Semiconductor	www.centralsemi.com
NXP	www.nxp.com

Loop Compensation

To stabilize the control loop formed by the LT8277 and the associated power stage, connect an RC network between the V_C pin and ground. For many low-frequency applications, a 4.7nF capacitor and 10k resistor will suffice.

If the above values do not satisfy stability requirements, first try adjusting the value of the capacitor. If the response is stable but ringy, try adjusting the value of the resistor. If neither of these works, consider using a lower programmed current limit (if possible), changing the value of the output capacitor, or changing the value of the inductor.

Programming the Switching Frequency

To program the switching frequency for the LT8277, connect a single resistor between the RT pin and the ground. To select a resistor, see *Table 10*. Note that for the same component values, increasing switching frequency will reduce input and output voltage ripple and reduce inductor current ripple, but it can also decrease efficiency.

To synchronize LT8277 to an external clock, drive the SYNC/SPRD pin with that clock. Choose R_T such that the programmed switching frequency is within ±15% of the external clock frequency.

Like all switching converters, the LT8277 can create electromagnetic interference (EMI). One way to reduce the EMI emitted by a switching converter is to use spread spectrum frequency modulation (SSFM). To enable internal SSFM, tie the SYNC/SPRD pin to $INTV_{CC}$.

Table 10. Selected RT values and Switching Frequency

F_{SW} (kHz)	R_T (kΩ)
100	523
200	191
250	143
300	115
400	82.5
500	63.4
1000	28.0
2000	11.0

Soft-Start and PGOOD Reporting

To reduce stress seen by external components, LT8277 uses a soft-start. When switching begins, either after power-on or when recovering from a fault, the output voltage target and switching frequency fall considerably below their nominal values. As the startup proceeds, both constraints relax. The duration of the foldback depends on R_T. The duration of a soft-start can become lengthy for low switching frequency applications. The SPI interface provides a bit to speed up soft-start, decreasing its duration to 25% of the default soft-start time set by R_T.

During soft-start, LT8277 inhibits the PGOOD signal to allow the part to reach a steady state. However, once soft-start is complete, the PGOOD pin will be asserted whenever the output voltage is within 5% of the value programmed using the SPI port. The PGOOD pin is an active-high open-drain signal, and using a resistive pull-up to V_{IN} or $INTV_{CC}$ is recommended to prevent errant assertions of the PGOOD signal while the part is unpowered.

If the output voltage exceeds the programmed value by around 5%, switching will stop, irrespective of the voltage at V_C. If the output falls to less than 30% of the value programmed using the SPI port, switching stops. After a brief cooldown period, the part will attempt to restart as if power had just been applied.

Using ENABLE

For simple on/off functionality, drive the ENABLE pin with a logic signal using V_{IL}= 0.4V and V_{IH} = 1.4V. To create an accurate input undervoltage lockout (UVLO), connect the ENABLE pin to the center of a resistive voltage divider from the input voltage to ground. When the voltage at ENABLE falls below $V_{ENABLE\_FALLING}$, the part will shut down. While the part is shut down, the supply current is significantly reduced, and switching stops. A small current is drawn into the ENABLE pin in the off state to enable programmable hysteresis, as shown in *Figure 33*.

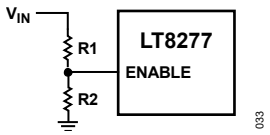


Figure 33. Resistor Network for Accurate UVLO

$$V_{INUVLO,FALLING} = 1.26 \cdot \left(1 + \frac{R1}{R2}\right) \quad (9)$$

$$V_{INUVLO,RISING} = 1.32 \cdot \left(1 + \frac{R1}{R2}\right) + 2.5\mu A \cdot R1 \quad (10)$$

Multichip Operation

Each LT8277 controls two phases of a power converter that are interleaved 180° apart. Note that the two phases are not independent channels; they both provide current to the same output node and, within the specified matching limits, contribute the same current to the load.

The upper and lower limits of the V_C pin range are well controlled, allowing multiple LT8277 devices to share a single compensation network. This allows additional phases to be included, each contributing the same current as in the 2-phase case. A set of small, 100pF or so, capacitors placed locally for each IC in the system between V_C and ground can improve phase-to-phase peak current matching.

To ensure appropriate phase separation, use the CLKOUT pin of one LT8277 to drive the SYNC/SPRD input of a subsequent device, as shown in *Figure 34*. Be sure to configure the SPI interface to enable CLKOUT and select the appropriate phase angle. For a 4-phase operation, choose 90°, and for an 8-phase operation, choose 45°. All phases must receive the same SPI command and monitor the same output voltage. For 4-phase and 8-phase operation, the SYNC/SPRD pin for the first chip in the line acts as the external synchronization and internal SSFM control pin for the system.

Multiphase operation relaxes input and output capacitance requirements for a given switching frequency and ripple voltage. In addition, for high-power applications, having multiple power devices can aid in thermal management and reduce EMI compared to a single-phase case. See the component selection guides for details about multiphase component selection.

Multiphase operation can degrade light-load efficiency and lead to pulse skipping earlier than the single-phase case. To address this, when the voltage at V_C falls below where it would set peak inductor current around 1/8 of the programmed current limit, LT8277 will shut down its second phase. The second phase will resume operation when the voltage at V_C exceeds the point where it will set peak inductor current around 1/4 of the programmed current limit. The SPI interface provides a bit to force the second phase to continue operating at light load. This does not prevent pulse skipping at a very light load for either phase.

PCB Layout Guidelines

The printed circuit board (PCB) layout can significantly improve the performance of the LT8277. Two key areas for focus are heat and electromagnetic interference (EMI). *Figure 35* shows an example of a reference layout. The example layout represents a two-layer PCB; however, a four-layer PCB is recommended.

Even at high efficiency, power dissipated in the PCB can become significant with a heavy load. Use a large, unbroken ground plane to spread the heat around the board to decrease the peak temperature. Layout the switch nodes, which will usually be best able to remove heat from the power NMOS devices, directly above a ground plane and not over signal routing. Use a large area for the output voltage, since this node can often effectively extract heat from the catch diode.

To reduce EMI, pay attention to the hot loop. For more information about hot loops, refer to Application Note AN136: *PCB Layout Considerations for Non-Isolated Switching Power Supplies* and Application Note AN139: *Power Supply Layout and EMI*. Layout the power NMOS and catch diode as close to one another as possible, with the output capacitor making the shortest possible route from the diode cathode to the switch source. Vias in the switch node can significantly worsen EMI performance. A large switch node area can also worsen EMI performance but improve thermal performance. Users must consider the tradeoffs carefully.

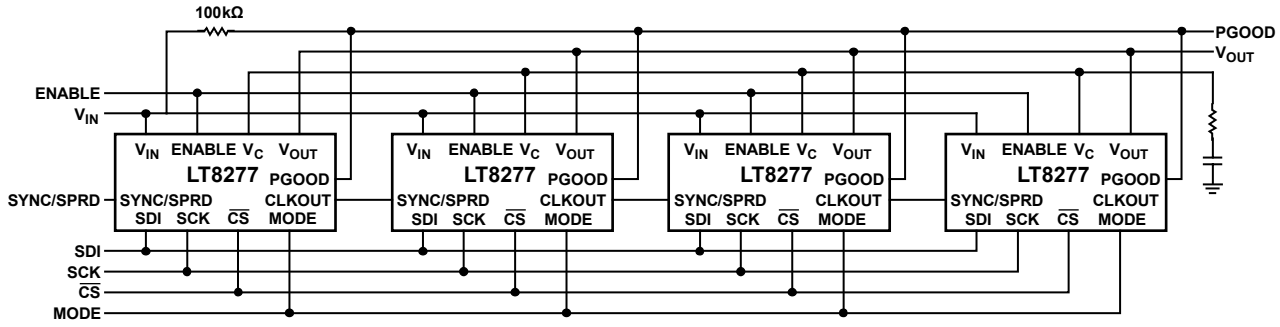


Figure 34. Example of 8-Phase Operation using the Same Interface as the Single-Chip Configuration

Other PCB layout considerations exist. The inductor current sense resistors should be Kelvin connected to their respective SNSP and SNSN lines. These routes should remain in pairs, that is, SNSP1 and SNSN1 should be routed adjacent to one another, and the same is true for phase 2. Keep the $INTV_{CC}$ bypass capacitor close to the IC, and Kelvin connects the V_{OUT} pin to the output capacitor.

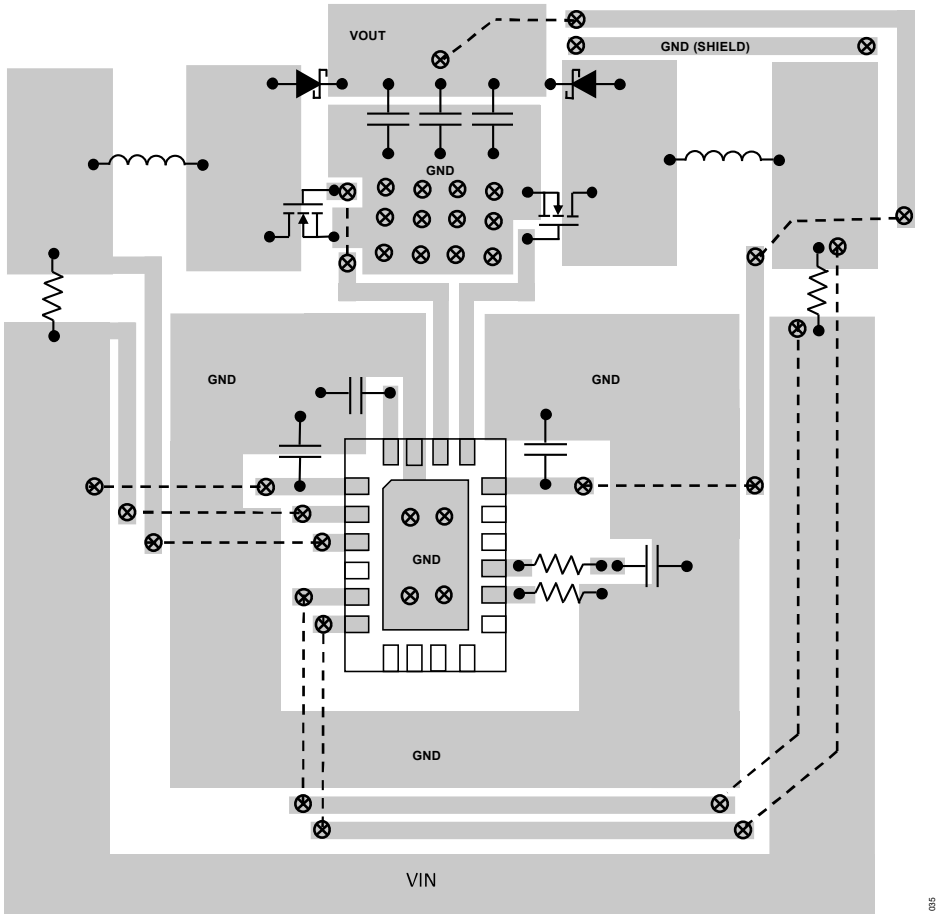


Figure 35. Reference Layout for the LT8277

RELATED PARTS

PART No.	DESCRIPTION	COMMENTS
LTC3862	Multi-phase Current Mode Step-up DC/DC Controller	Up to 12 phases, resistor-programmed output voltage
LTC3787	PolyPhase Synchronous Boost Controller	Synchronous operation, resistor-programmed output voltage, minimum input voltage 2.5V input after start-up
LTC3784	60V PolyPhase Synchronous Boost Controller	Synchronous operation, up to 60V input voltage, resistor-programmed output voltage, low quiescent current

TYPICAL APPLICATIONS CIRCUITS

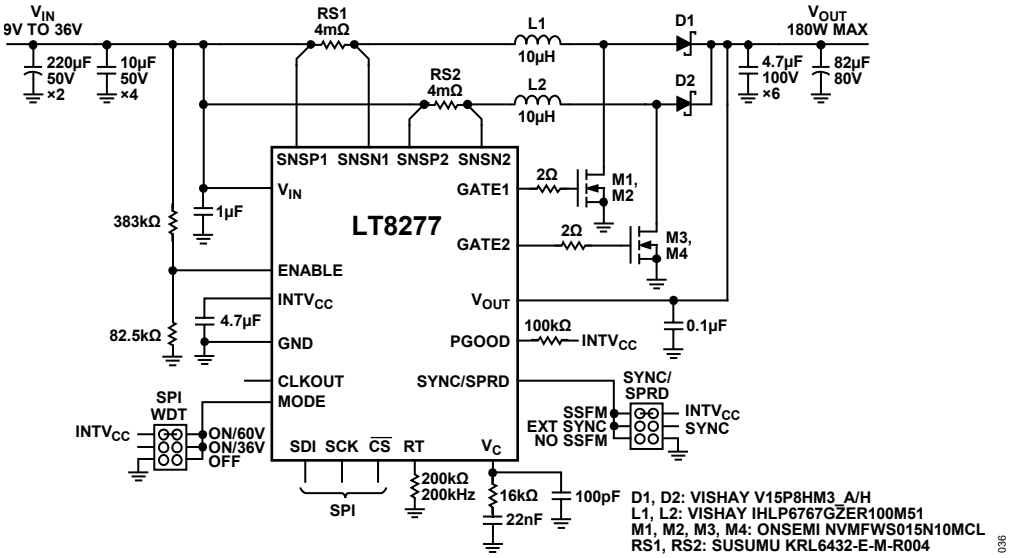


Figure 36. 180W Automotive Pre-Boost Converter with SPI

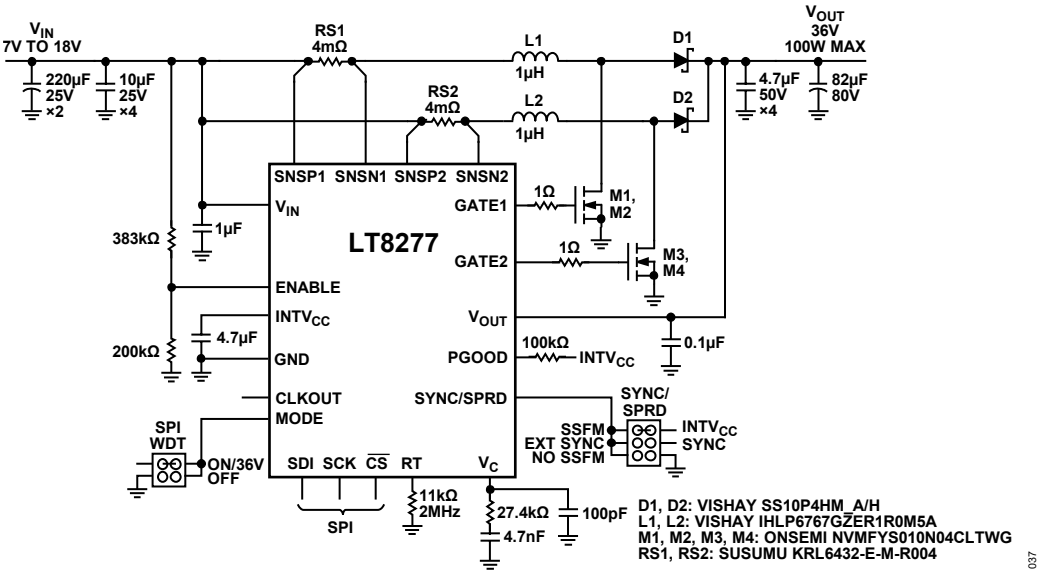


Figure 37. 36V 100W 2MHz Boost Voltage Regulator with SPI

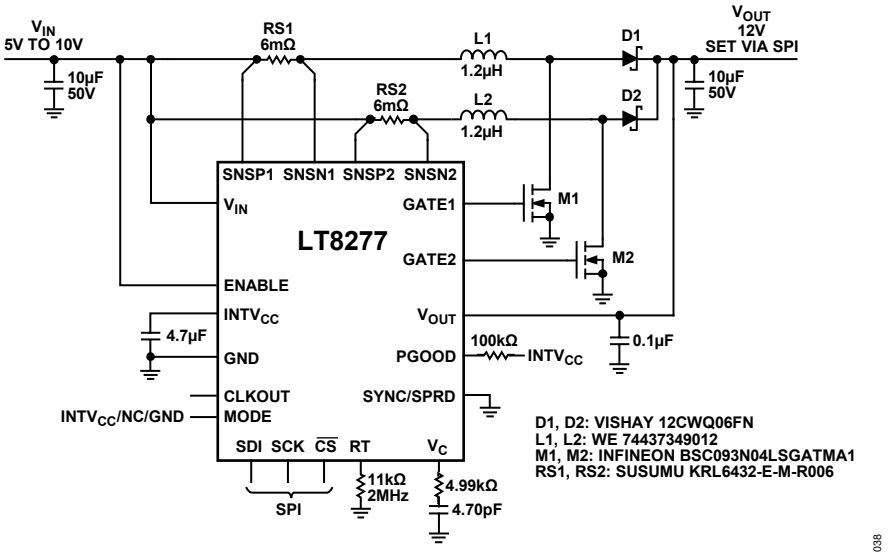


Figure 38. 12V 60W 2MHz Boost Voltage Regulator with SPI

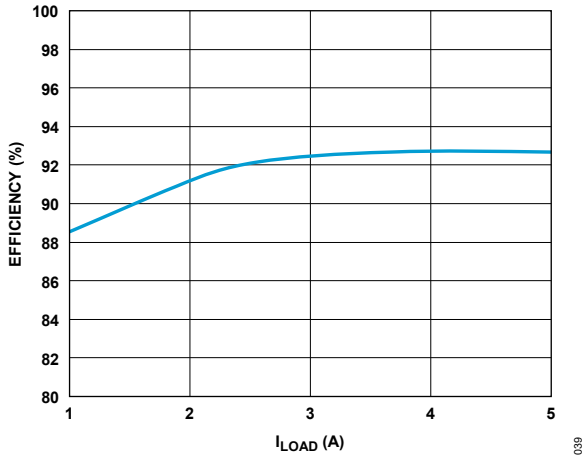


Figure 39. Efficiency vs. Load Current Curve of 12V 60W 2MHz Boost Voltage Regulator

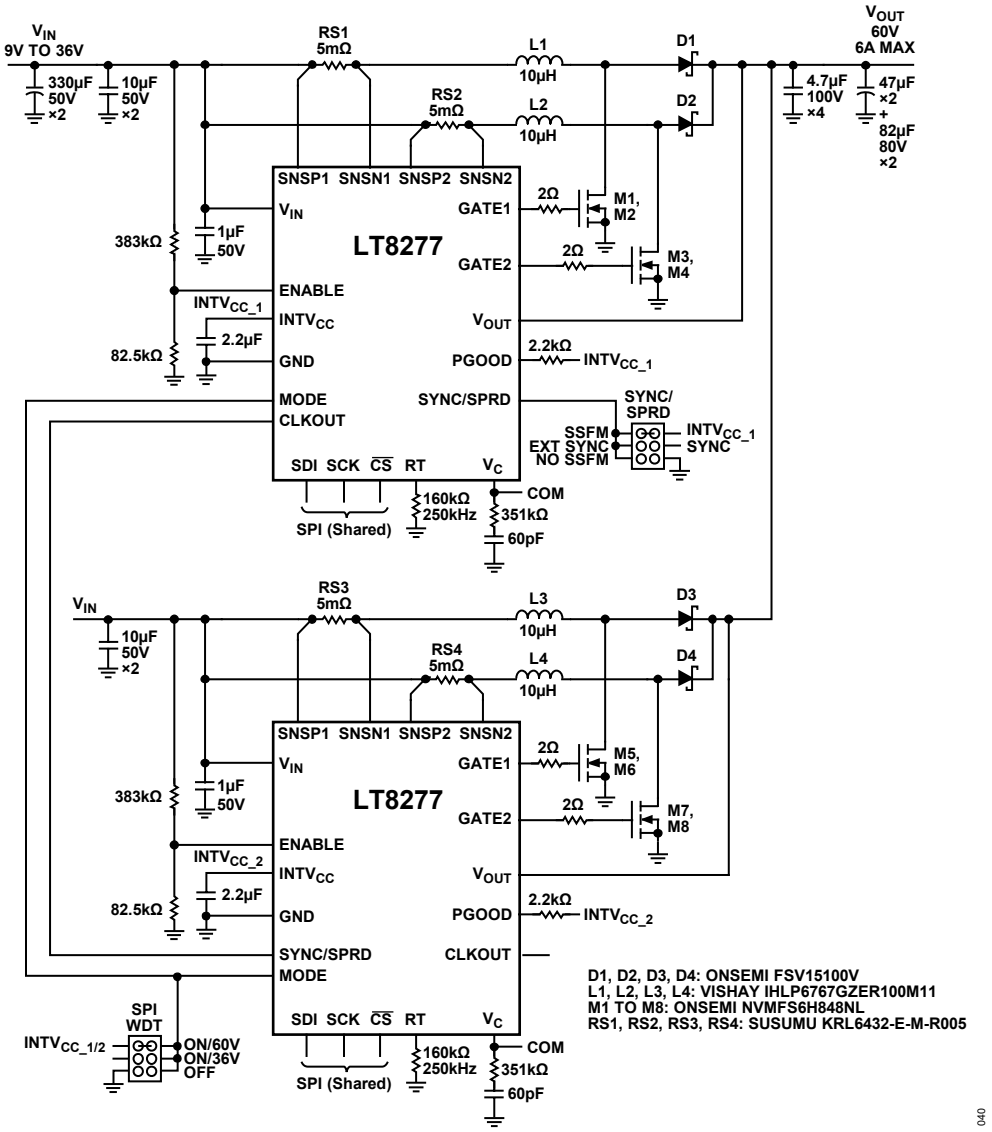


Figure 40. 4-Phase, 60V 360W 250kHz Boost Voltage Regulator with SPI

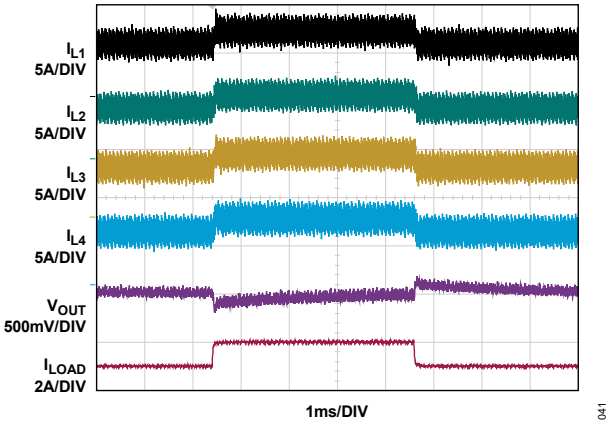


Figure 41. Load Transients of 4-Phase 60V 360W 250kHz Boost Voltage Regulator

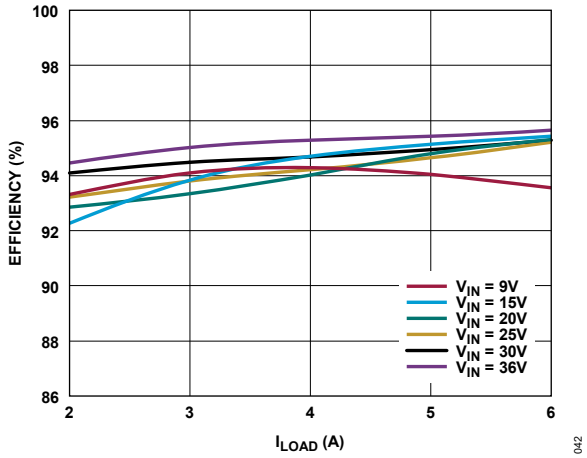
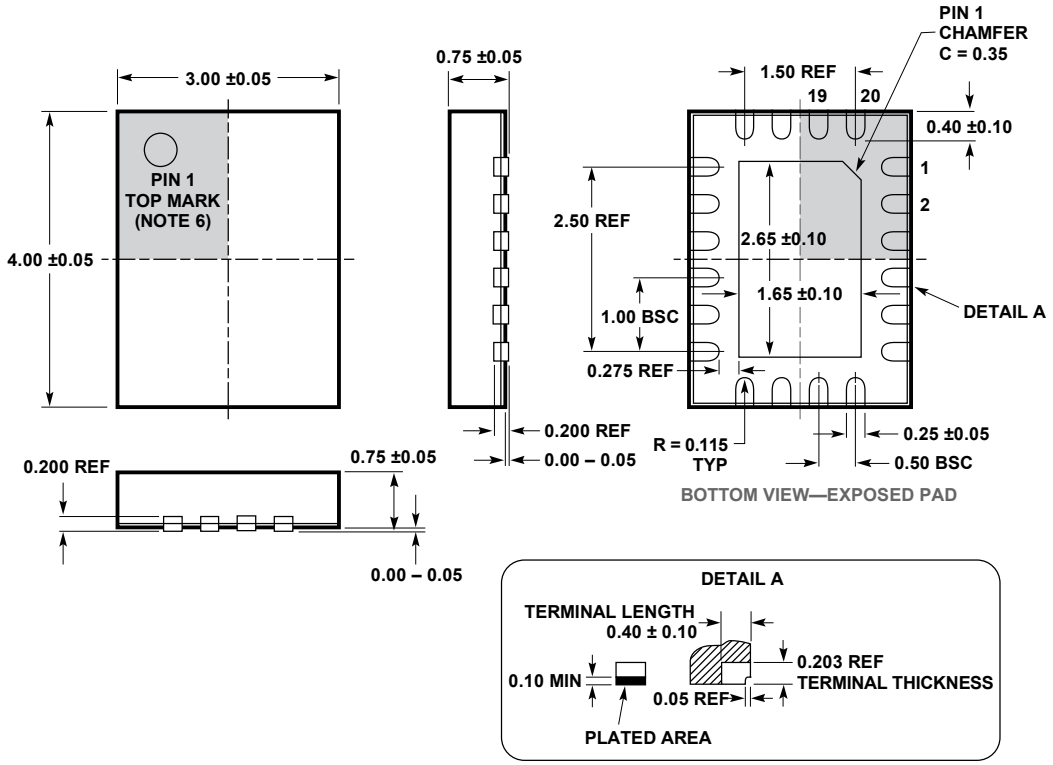


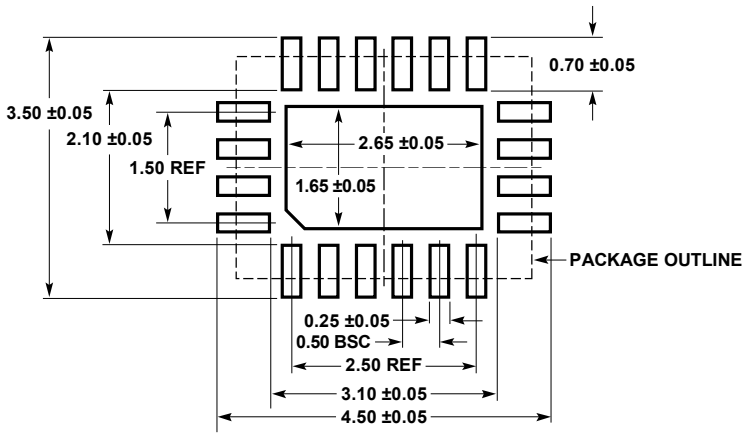
Figure 42. Efficiency vs. Load Current Curve of 4-Phase 60V 360W 250kHz Boost Voltage Regulator

OUTLINE DIMENSIONS

UDCM Package
20-Lead Plastic Side Solderable QFN (3mm × 4mm)
(Reference DWG # 05-08-7020 Rev A)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

(UDCM20) QFN 0722 REV A

ORDERING GUIDE

Table 11. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8277RUDCM#WPBF*	LT8277RUDCM#WTRPBF	LHPB	3mm x 4mm Plastic Side-solderable QFN	-40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges.

*This part has controlled manufacturing to support the quality and reliability requirements of automotive applications. This model is designated with a #W suffix. Only automotive grade products are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability report for this model.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LT8277RUDCM#WTRPBF LT8277RUDCM#WPBF EVAL-LT8277-AZ