Dual Channel 6A, 20V PolyPhase Step-Down Silent Switcher 2 with Digital Power System Management

FEATURES

- Silent Switcher®2 Architecture: Enables Compact, Efficient, low EMI Solution
- PMBus/I²C Serial Interface
  - Telemetry Read Back Includes V_{OUT}, I_{OUT}, V_{IN}, Die Temperature, Faults
  - Programmable Voltage, Current Limit, Digital Soft-Start/Stop, Sequencing, UV/OV, Phase, Frequency (Up to 4MHz), Loop Compensation
  - Integrated EEPROM with Fault Event Log
- Key Parameters May Be Set by Configuration Resistors for Operation without Programming
- ±0.25% Output Voltage Accuracy Over Temperature for 0.6V to 1.375V
- PolyPhase Load Sharing for Up to Eight Phases
- Wide V_{IN} Range: Down to 2.9V, or 1.5V with $EXTV_{CC}$
- Up to 95% Efficiency at 1MHz, $12V_{IN}$ to $3.3V_{OUT}$
- V_{OUT} Range 0.4V to 5.5V (Up to 0.85 • V_{IN})
- Differential Remote V_{OUT} Sense
- External Frequency Synchronization
- 40-lead (5mm × 7mm) LQFN Package

APPLICATIONS

- Communications, Storage, and Industrial Systems
- Data Center and Solid State Drive Power Supplies

DESCRIPTION

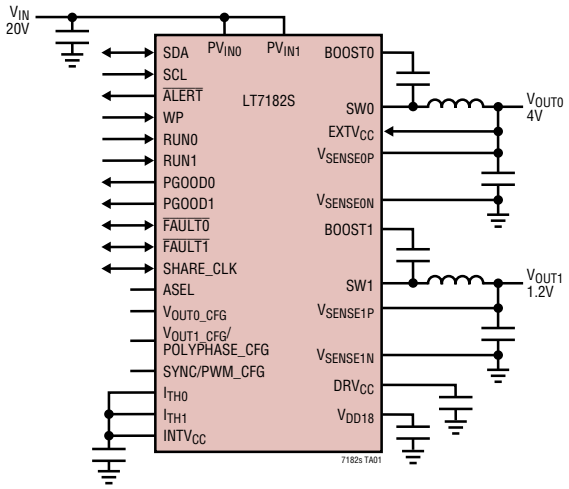
The LT®7182S is a dual-output monolithic PolyPhase DC/DC synchronous step-down regulator that delivers up to 6A of continuous current from both channels simultaneously and supports loads up to 8A from either channel. The LT7182S features the second generation Silent Switcher® architecture with integrated V_{IN} bypass capacitors for fast, clean, low-overshoot switching edges delivering high efficiency at high switching frequencies while minimizing EMI emissions.

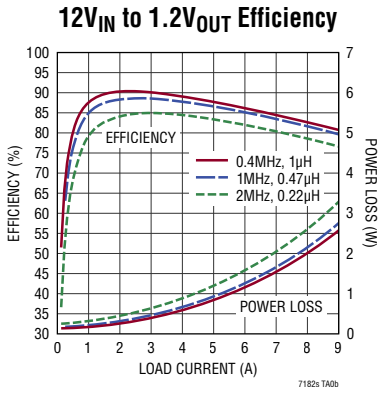
The I²C-based PMBus 1.3 compliant serial interface enables control of device functions and provides telemetry information for system monitoring. The LT7182S is supported by the LTpowerPlay® graphical user interface tool.

Output voltage, frequency, phase, and device address can be configured using resistors for operation without programming. Settings may also be written via the serial interface and/or stored in EEPROM.

The controlled on-time valley current mode control architecture with 20ns (typical) minimum on-time enables high switching frequency at low output voltage with excellent transient response in a small overall solution size.

TYPICAL APPLICATION





TYPICAL APPLICATIONS

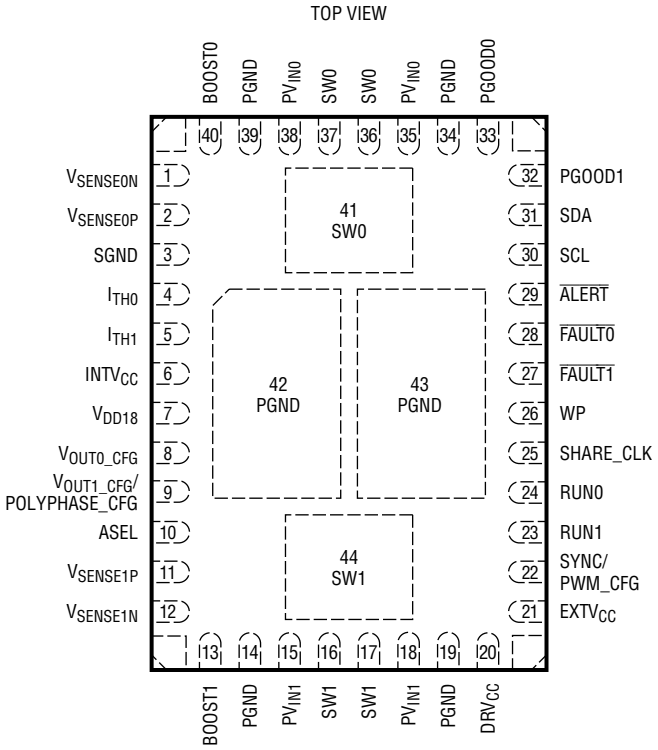
See also, the companion document LT7182S PMBus/I^{2}C Reference Manual. It provides a detailed description of digital functionality including PMBus commands, serial device address selection, and physical interface details.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN0}, PV_{IN1} ..... –0.3V to 25V
$EXTV_{CC}$ ..... –0.3V to 6V
$V_{SENSE0P}$, $V_{SENSE1P}$ ..... –0.3V to 6V
$V_{SENSE0N}$, $V_{SENSE1N}$ ..... –0.3V to 0.3V
I_{TH0}, I_{TH1} ..... –0.3V to 6V
SYNC/PWM_CFG, WP, SHARE_CLK, $\overline{\text{ALERT}}$, SDA, SCL, $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, RUN0, RUN1, PGOOD0, PGOOD1 ..... –0.3V to 6V
Operating Junction Temperature (Note 2)
LT7182SR ..... –40°C to 150°C
ABSMAX T_J ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Peak Reflow (Package Body) Temperature ..... 260°C

PIN CONFIGURATION



LQFN PACKAGE
40-LEAD (5mm × 7mm × 0.9mm)
θ_{JA} = 27°C/W, Ψ_{JT} = 0.28°C/W,
EXPOSED PAD (PINS 41 - 44) MUST BE SOLDERED TO APPROPRIATE PCB NETS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LT7182SRV#PBF	Au (RoHS)	7182S	e4	LQFN	3	–40°C to 150°C

- *Pad or ball finish code is per IPC/JEDEC J-STD-609. The temperature grade is identified by a label on the shipping container.
- **LQFN is Laminate Package with QFN Footprint. The LT7182S package has the same X, Y dimensions as a standard 5mm × 7mm QFN package.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply						
Channel 0 Input Supply Range	$EXTV_{CC}$ = 0V	●	2.9		20	V
Channel 0 Input Supply Range with $EXTV_{CC}$	3V ≤ $EXTV_{CC}$ ≤ 5.5V	●	1.5		20	V
Channel 1 Input Supply Range	PV_{IN0} ≥ 2.9V or $EXTV_{CC}$ ≥ 3V	●	1.5		20	V
Optional $EXTV_{CC}$ Input Supply Range		●	3		5.5	V
$EXTV_{CC}$ + PV_{IN0} + PV_{IN1} Quiescent Current Both channels switching Sleep (Pulse Skip Mode) or Shutdown	f_{SW} = 1MHz, Forced Continuous Mode, V_{IN} = 12V, No Load			21 7		mA mA
Initialization Time (Delay from RESTORE_USER_ALL, MFR_RESET, or Application of PV_{IN0} or $EXTV_{CC}$, Until TON_DELAY Timer Can Begin)	With CFG Pins Enabled (Default) CFG Pins Ignored			13 10		ms ms
Switching Regulator						
V_{OUT} Range	PV_{IN} > 6.1V PV_{IN} ≤ 6.1V	● ●	0.4 0.4		5.5 0.85 • V_{IN}	V V
V_{OUT} Set Point Accuracy	High-Performance Low-V_{OUT} Mode, 0.6V ≤ V_{OUT} ≤ 1.375V 0.4V ≤ V_{OUT} ≤ 5.5V	● ●	–0.25 –0.5		0.25 0.5	% %
V_{OUT} Set-Point Resolution				1		mV
$V_{SENSE0P}$, $V_{SENSE1P}$ Input Resistance	$V_{SENSE0N}$ = $V_{SENSE1N}$ = 0V			30		kΩ
Error Amplifier Transconductance Programming Resolution				3		bits
Error Amplifier Transconductance $g_{m(MAX)}$	Full V_{OUT} Range Mode, 0.4V ≤ V_{OUT} ≤ 5.5V. Includes Internal V_{OUT} Feedback Divider			300		µS
Error Amplifier Transconductance $g_{m(MIN)}$	Full V_{OUT} Range Mode, 0.4V ≤ V_{OUT} ≤ 5.5V. Includes Internal V_{OUT} Feedback Divider			37.5		µS
Error Amplifier Transconductance g_m Step Size	Full V_{OUT} Range Mode, 0.4V ≤ V_{OUT} ≤ 5.5V. Includes Internal V_{OUT} Feedback Divider			37.5		µS
Error Amplifier Transconductance $g_{m(MAX)}$	High-Performance Low-V_{OUT} Mode, 0.4V ≤ V_{OUT} ≤ 1.375V, Includes Internal V_{OUT} Feedback Divider			1.2		mS
Error Amplifier Transconductance $g_{m(MIN)}$	High-Performance Low-V_{OUT} Mode, 0.4V ≤ V_{OUT} ≤ 1.375V, Includes Internal V_{OUT} Feedback Divider			150		µS
Error Amplifier Transconductance g_m Step Size	High-Performance Low-V_{OUT} Mode, 0.4V ≤ V_{OUT} ≤ 1.375V, Includes Internal V_{OUT} Feedback Divider			150		µS
Max Programmable Internal Compensation Resistor $R_{ITH(MAX)}$	Internal Compensation (I_{TH} Tied to $INTV_{CC}$) (Note 5)			120		kΩ
Min Programmable Internal Compensation Resistor $R_{ITH(MIN)}$	Internal Compensation (I_{TH} Tied to $INTV_{CC}$) (Note 5)			5		kΩ
Internal Compensation Capacitor Programming Resolution	Internal Compensation (I_{TH} Tied to $INTV_{CC}$)			3		bits
Internal Compensation Capacitor $C_{ITH(MAX)}$	Internal Compensation (I_{TH} Tied to $INTV_{CC}$)			80		pF
Internal Compensation Capacitor $C_{ITH(MIN)}$	Internal Compensation (I_{TH} Tied to $INTV_{CC}$)			10		pF
Internal Compensation Capacitor C_{ITH} Step Size	Internal Compensation (I_{TH} Tied to $INTV_{CC}$)			10		pF

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Inductor Valley Current Limit ILIM-POS (Note 6) (Sourcing Output Current)	ILIM Range 0 ILIM Range 1 ILIM Range 2 ILIM Range 3	● ● ● ●	2.3 3.5 5 6.5	3 4.5 6.5 8.5	3.7 5.5 8 10.5	A A A A
Negative Inductor Valley Current Limit ILIM-NEG (Note 6) (Sinking Output Current)	ILIM Range 0 ILIM Range 1 ILIM Range 2 ILIM Range 3	● ● ● ●	–3 –4.4 –5 –5.5	–2.3 –3.4 –4 –4.25	–1.6 –2.4 –3 –3	A A A A
Power FET On-Resistance Main Switch (Top) Synchronous Switch (Bottom)				 48 17		 mΩ mΩ
SW Leakage	V_{IN} = 20V, V_{SW} = 0V,20V		–120		120	µA
Minimum On-Time	I_{LOAD} = 1A	●		20	40	ns
Minimum Off-Time		●		60	100	ns
Output Voltage Supervisors						
V_{OUT} Undervoltage (UV) Fault/Warning Programming Range			0.36		5.5	V
V_{OUT} Overvoltage (OV) Fault/Warning Programming Range			0.4		6	V
V_{OUT} UV/OV Fault/Warning Threshold Accuracy	V_{OUT} UV/OV Threshold < 0.6V V_{OUT} UV/OV Threshold ≥ 0.6V	● ●	–12 –2		12 2	mV %
V_{OUT} UV/OV Fault/Warning Programming Step Size				4		mV
V_{OUT} UV/OV Fault/Warning Time	V_{OUT} = 10mV Beyond Threshold	●			25	µs
Input Voltage Supervisors						
ON Threshold Programming Range			1.4		20	V
OFF Threshold Programming Range			1.35		20	V
ON/OFF Threshold Programming Step Size				25		mV
ON/OFF Threshold Set Point Accuracy	$V_{IN\_ON/OFF}$ ≤ 5V	●	–100		100	mV
ON/OFF Threshold Set Point Accuracy	5V ≤ $V_{IN\_ON/OFF}$ ≤ 20V	●	–2		2	%
V_{IN} Overvoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling	●	22 21	23.3 22.3		V V
Oscillator and Phase Locked Loop						
SYNC/PWM_CFG Pin Input Frequency Range		●	0.4		4	MHz
Switching Frequency Programming Range			0.4		4	MHz
Switching Frequency Set Point Accuracy		●	–7.5		7.5	%
Switching Phase Programming Range			0		345	degrees
Switching Phase Programming Resolution				15		degrees
Telemetry Readback						
Telemetry Measurement Period, All Except Die Temperature				6.5		ms
Telemetry Measurement Period, Die Temperature				26		ms
Output Voltage Readback						
READ_VOUT Accuracy	High-Performance Low-V_{OUT} Mode, 0.6V ≤ V_{OUT} ≤ 1.375V	●	–0.15		0.15	%
READ_VOUT Accuracy	0.4V < V_{OUT} < 5.5V	●	–0.35		0.35	%

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PV_{IN0}, PV_{IN1} Input Voltage Readback						
READ_VIN Accuracy	V_{IN} = 1.5V to 2.5V V_{IN} = 2.5V to 20V	● ●	–25 –1		25 1	mV %
Output Current Readback						
READ_IOUT Accuracy	I_{OUT} = 0A to 4A, (V_{OUT}/V_{IN}) ≤ 0.5 I_{OUT} = 4A to 8A, (V_{OUT}/V_{IN}) ≤ 0.5 I_{OUT} = 0A to 4A, (V_{OUT}/V_{IN}) > 0.5 I_{OUT} = 4A to 8A, (V_{OUT}/V_{IN}) > 0.5	● ● ● ●	–200 –5 –600 –15		200 5 600 15	mA % mA %
Input Current Readback						
READ_IIN Accuracy	I_{IIN} = 0A to 1A, I_{IIN} = 1A to 5A	● ●	–250 –25		250 25	mA %
Frequency Readback						
READ_FREQUENCY Accuracy	f_{SW} ≤ 400kHz f_{SW} ≥ 400kHz		–20 –5		20 5	kHz %
EEPROM Characteristics						
Retention	(Note 4)	●	10			years
Endurance	(Note 4)	●	10,000			writes
Mass Write Time (STORE_USER_ALL)		●		250	500	ms
Digital Inputs RUN0, RUN1, $\overline{FAULT0}$, $\overline{FAULT1}$, PGOOD0, PGOOD1, SHARE_CLK, SCL, SDA, $\overline{ALERT}$, WP						
Input High Threshold (V_{IH})		●		1.1	1.35	V
Input Low Threshold (V_{IL})		●	0.8	0.9		V
Hysteresis (V_{HYS})			50	200	400	mV
Leakage Current	Applied Voltage = 0V, 5.5V				±10	µA
Input Capacitance					10	pF
Digital Clock Input SYNC/PWM_CFG						
Peak-to-Peak Input Voltage Swing	SYNC Input Mode	●	1.6		5.5	V
Rise Time	SYNC Input Mode				25	ns
Duty Cycle	SYNC Input Mode		30		70	%
Digital Clock Output SYNC/PWM_CFG						
Output High Voltage	SYNC Output Mode	●	1.6	1.88	1.98	V
Output Low Voltage	SYNC Output Mode	●		0	0.1	V
Current-Limited Open-Drain Output RUN0, RUN1, FAULT0, FAULT1						
Pulldown Current	Applied Voltage = 0.4V to 5.5V	●	1	1.5	2	mA
Open-Drain Outputs PGOOD0, PGOOD1, SHARE_CLK						
Output Low Voltage	I = 6mA	●			0.4	V
Digital I/O SCL, SDA, ALERT						
Output Low Voltage	I = 20mA	●			0.4	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C/PMBus Timing							
f_{SCL}	Serial Bus Operating Frequency		●	10		1000	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	500			ns
$t_{HD:STA}$	Hold Time After repeated Start Condition		●	260			ns
$t_{SU:STA}$	Repeated Start Condition Setup Time		●	260			ns
$t_{SU:STO}$	Stop Condition Setup Time		●	260			ns
$t_{SU:DAT}$	Data Input Setup Time		●	50			ns
$t_{HD:DAT}$	Data Input Hold Time		●	0			ns
	Data Output Hold Time		●	0		450	ns
$t_{TIMEOUT}$	Bus Timeout		●	25		35	ms
t_{LOW}	Serial Clock Low Period		●	0.5		 10000	µs µs
t_{HIGH}	Serial Clock High Period		●	260			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT7182SR is specified over the –40°C to 150°C operating junction temperature range. High Junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LT7182S includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

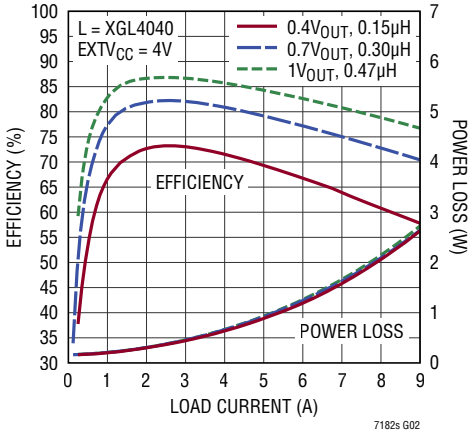
Note 4: EEPROM endurance is guaranteed by design, characterization and correlation with statistical process controls. Data retention is production tested via a high temperature bake at wafer level. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 5: When internal compensation is selected (by connecting I_{TH} to $INTV_{CC}$), eight internal resistor values are available in non-linear increments. See the MFR_PWM_MODE_LT7182S command in the LT7182S PMBus/I²C Reference Manual.

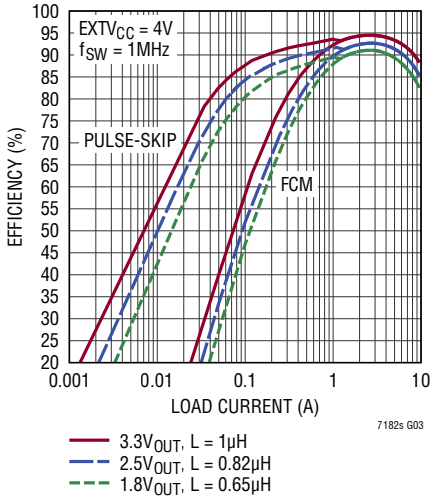
Note 6: The LT7182S switching regulators use valley current mode control so the current limits specified correspond to the valley of the inductor current waveform. Maximum load current is higher and equals the valley current limit plus one half of the inductor ripple current. See Applications Information for more details.

TYPICAL PERFORMANCE CHARACTERISTICS

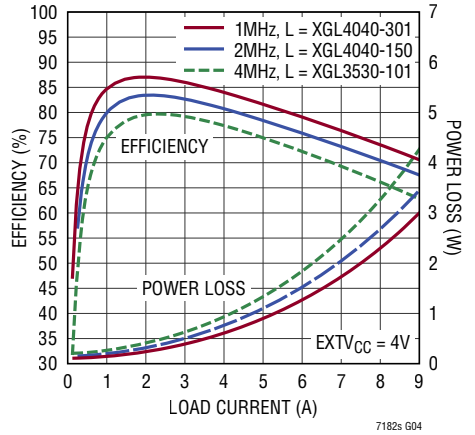
$12V_{IN}$ Efficiency at f_{SW} = 1MHz, Different V_{OUT}



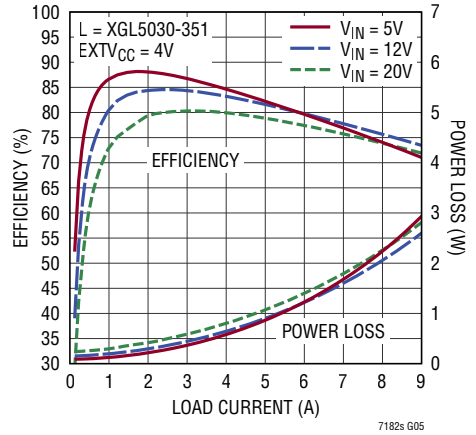
$12V_{IN}$ to Various V_{OUT} Low Load Efficiency



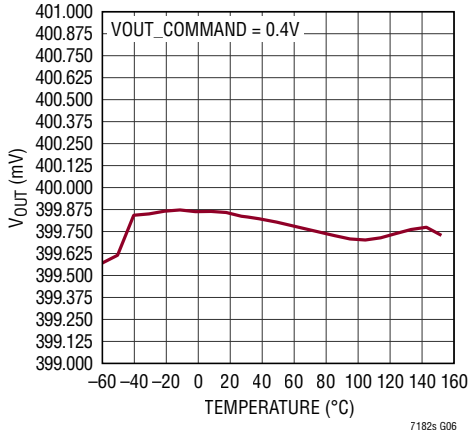
$5V_{IN}$ to $0.8V_{OUT}$ Efficiency at Different f_{SW}



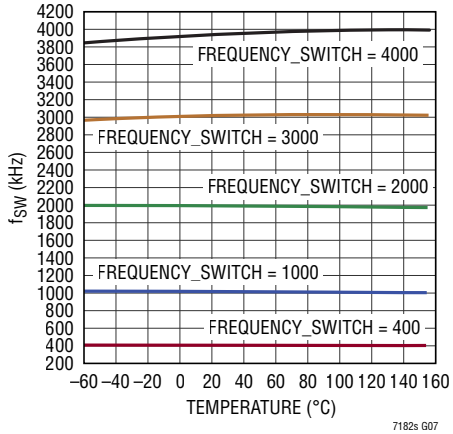
$0.8V_{OUT}$ Efficiency at f_{SW} = 1MHz, Various V_{IN}



V_{OUT} vs Temperature

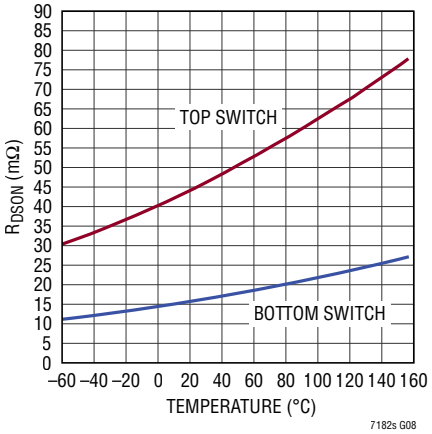


f_{SW} vs Temperature

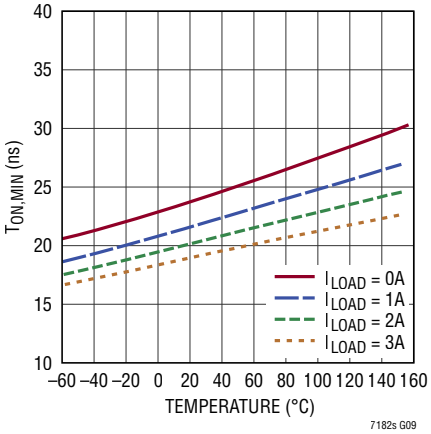


TYPICAL PERFORMANCE CHARACTERISTICS

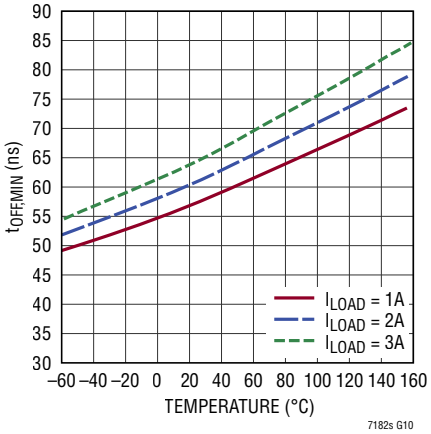
Switch R_{DSON} vs Temperature



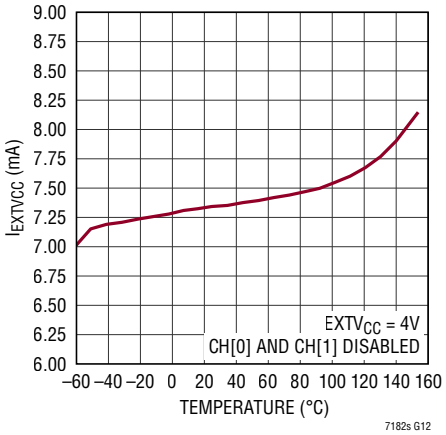
Minimum On-Time



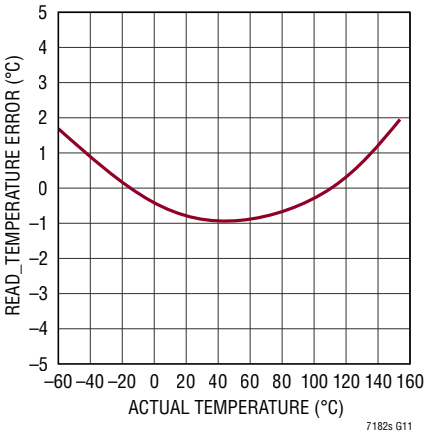
Minimum Off-Time



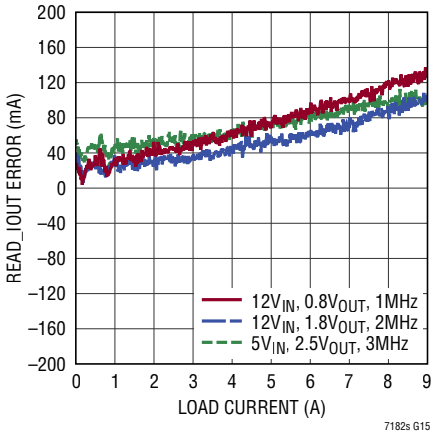
$EXTV_{CC}$ Idle Current vs Temperature



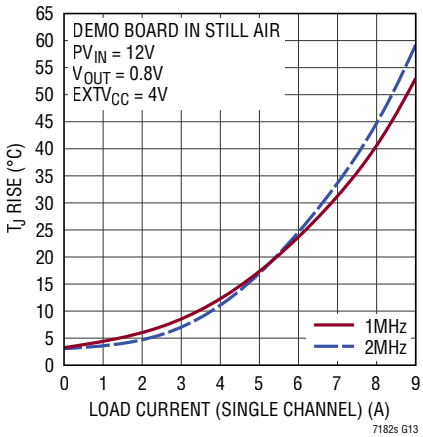
READ_TEMPERATURE Error vs Temperature



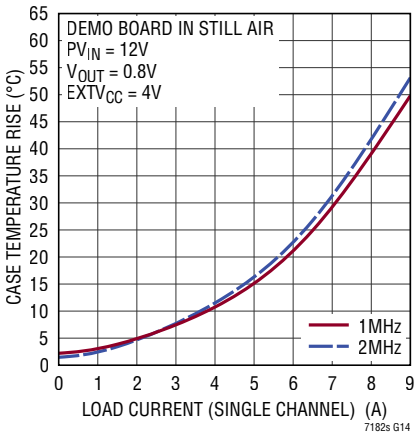
READ_I_{OUT} Error vs I_{OUT}



T_J Rise vs Load

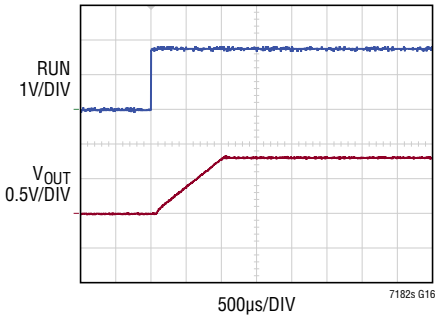


Case Temperature Rise



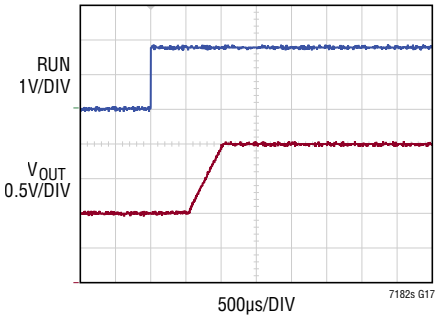
TYPICAL PERFORMANCE CHARACTERISTICS

Soft-Start Ramp



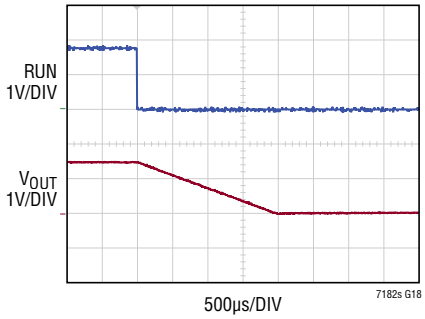
TON_RISE = 1ms
TON_DELAY = 0ms
VOUT_COMMAND = 0.8V

Startup into a Prebiased Load



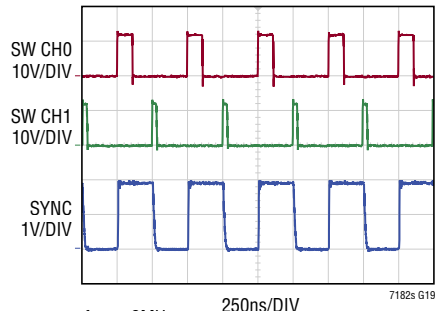
TON_RISE = 1ms
TON_DELAY = 0ms
VOUT_COMMAND = 2V
PREBIASED AT 1V

Soft-Off Ramp



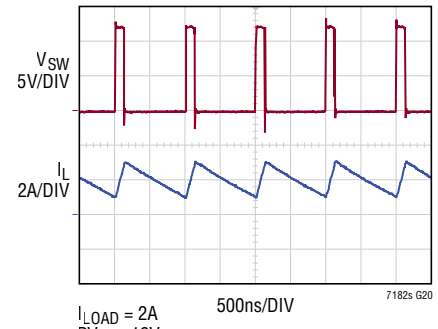
TOFF_FALL = 2ms
TOFF_DELAY = 0ms
VOUT_COMMAND = 1.5V

SW Node and SYNC Output



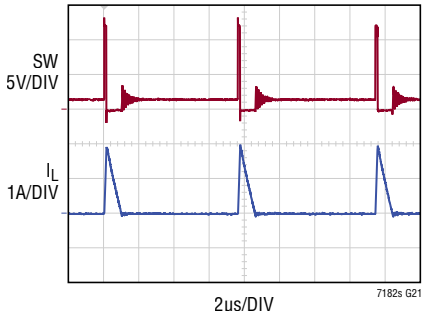
f_{SW} = 2MHz
CH1 MFR_PWM_PHASE = 180

Switching Waveforms in Continuous Conduction



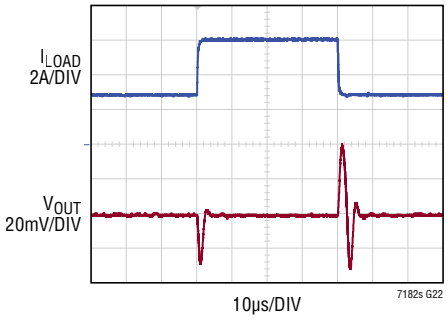
I_{LOAD} = 2A
PV_{IN} = 12V
V_{OUT} = 1.5V

Switching Waveforms in Pulse-Skip Mode



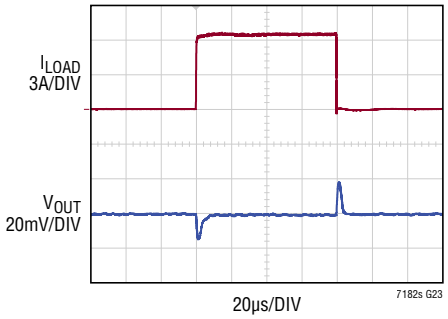
V_{IN} = 12V
V_{OUT} = 1.5V
I_{LOAD} = 100mA

Transient Response: Load Current Stepped 3A to 6A, Internal Compensation



V_{IN} = 12V, V_{OUT} = 0.8V, C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz
R_{COMP} = 10k, C_{COMP} = 80pF, g_{MEA} = 750µS

Transient Response: Dual Phase Stepped 0A to 6A, External Compensation



V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 100µF ×4
FCM, f_{SW} = 1MHz
R_{COMP} = 7k, C_{COMP} = 470pF, g_{MEA} = 1.2mS

PIN FUNCTIONS

$V_{SENSE0N}$, $V_{SENSE1N}$ (Pin 1, Pin 12): Output Voltage Negative Sense Inputs. Connect these pins to the output voltage ground sense points.

$V_{SENSE0P}$, $V_{SENSE1P}$ (Pin 2, Pin 11): Output Voltage Positive Sense Inputs. Connect these pins to the output voltage sense points.

SGND (Pin 3): Signal Ground. This pin should be connected to board ground in exactly one place, directly beneath the LT7182S.

I_{TH0}, I_{TH1} (Pin 4, Pin 5): Error Amplifier Output and Switching Regulator Compensation Points. Connect the appropriate external components between these pins and SGND to compensate the regulator loop frequency response, or connect the I_{TH} pin to $INTV_{CC}$ to select internal compensation for the channel.

$INTV_{CC}$ (Pin 6): Internal 3V LDO Regulator Bypass. This regulator provides the supply current for internal circuitry. This pin must be bypassed to SGND with a 10µF or greater, low ESR ceramic capacitor, as close as possible to the IC. Do not load the $INTV_{CC}$ pin with external circuitry.

V_{DD18} (Pin 7): Internal 1.8V Regulator Bypass. This pin must be bypassed to ground (SGND or PGND) with a 4.7µF or greater, low ESR ceramic capacitor. Do not load the V_{DD18} pin with external circuitry.

V_{OUT0_CFG} (Pin 8): Output Voltage Configuration for Channel 0. Connect a 1% resistor from V_{OUT0_CFG} to ground (SGND or PGND) according to Table 2 in the Applications Information section to select one of sixteen output voltage set points. If left floating or tied to V_{DD18}, the LT7182S will use the value of $V_{OUT\_COMMAND}$ programmed in EEPROM. The V_{OUT0_CFG} pin is read at LT7182S startup and reset.

V_{OUT1_CFG}/POLYPHASE_CFG (Pin 9): Output Voltage Configuration for Channel 1 or Polyphase Configuration. If the SYNC/PWM_CFG pin is NOT configured for Polyphase, then a 1% resistor from V_{OUT1_CFG}/POLYPHASE_CFG to ground (SGND or PGND) selects the voltage set point according to Table 2 in the Applications Information Section. If the SYNC/PWM_CFG pin is configured for Polyphase, then the channel 1 output is set to the same value as channel 0 based on V_{OUT0_CFG} and a 1% resistor from V_{OUT1_CFG}/POLYPHASE_CFG to SGND selects a Polyphase configuration according to Table 4 in the Applications Information section. The V_{OUT1_CFG}/POLYPHASE_CFG pin is read at LT7182S startup and reset.

ASEL (Pin 10): Serial Bus Address Configuration. Connect a 1% resistor from ASEL to ground (SGND or PGND) to select one of sixteen serial bus interface addresses. See the description of MFR_ADDRESS in the LT7182S PMBus/I^2C Reference Manual. The ASEL pin is read at LT7182S startup and reset. If the ASEL pin is left floating, the factory default 7-bit device address is 0x4F. If the ASEL pin is grounded, the factory default device address is 0x40.

BOOST1 (Pin 13): Boosted Floating Driver Supply. Connect a 0.1µF boost capacitor from BOOST1 to SW1 as close as possible to the IC, using the top PCB layer. The normal operation voltage swing of this pin is from DRV_{CC} to PV_{IN1}+DRV_{CC}

PGND (Pins 14, 19, 34, 39, Exposed Pad Pins 42-43): Power Ground. The (–) terminal of the PV_{IN0}, PV_{IN1} input bypass capacitors, and the (–) terminal of the output capacitors, C_{OUT0} and C_{OUT1}, should be tied to these pins with low impedance connections. The PCB must be designed to provide low impedance electrical and thermal contact to power ground.

PIN FUNCTIONS

PV_{IN1} (Pins 15, 18): Power Supply Input for Channel 1. These pins must be tied together and bypassed as close as possible to the LT7182S, with a low ESR capacitor of value 4.7µF or more.

SW1 (Pins 16, 17, Exposed Pad Pin 44): Output of the Channel1 Internal Power Switches. Tie these pins together and connect them to the channel1 inductor and BOOST1 capacitor. This node should be kept small on the PCB for good performance.

DRV_{CC} (Pin 20): Internal 3.5V LDO Regulator Bypass. This regulator provides the supply current for the power FET drivers. This pin must be bypassed to PGND with a 10µF or greater, low ESR ceramic capacitor, as close as possible to the IC, using the top PCB layer. Do not load the DRV_{CC} pin with external circuitry, with the optional exceptions of the pull-up resistor for the SHARE_CLK pin and/or the RUN0, RUN1, $\overline{FAULT0}$, or $\overline{FAULT1}$ pins.

$EXTV_{CC}$ (Pin 21): Optional Power Supply Input. If connected to 3V to 5.5V, this pin will be used to derive the DRV_{CC}, $INTV_{CC}$, and V_{DD18} supplies. If one of the regulator outputs is set to V_{OUT} of 3V or greater, that V_{OUT} may be connected to $EXTV_{CC}$ to reduce power loss. If this pin is not tied to a regulator output, use a 0.1µF or greater local bypass ceramic capacitor on this pin, as close as possible to the LT7182S.

SYNC/PWM_CFG (Pin 22): External Clock Synchronization Input/Output and/or PWM Configuration. When driven with an external clock, an internal phase-locked loop synchronizes the switching regulator output with the rising edge of the external clock. If this pin is to be used as a clock input, then a 1.5nF AC-coupling capacitor must be inserted in series with the clock source, unless the EEPROM is programmed to ignore the configuration resistors (MFR_CONFIG_ALL_LT7182S bit 6 set) in which case the clock source can be connected directly. If configured as an output (MFR_SYNC_CONFIG_LT7182S bit 0 set), the LT7182S will drive the SYNC/PWM_CFG pin output at the switching clock frequency set by FREQUENCY_SWITCH, with a voltage swing of 0V to 1.88V (typical). Connect a 1% resistor from SYNC/PWM_CFG to ground (PGND or SGND) according to Table 3 in Applications Information to select frequency, phase, and mode configurations. The SYNC/PWM_CFG pin is read at LT7182S startup and reset. See Applications Information for more details.

RUN0, RUN1 (Pin 24, Pin 23): Regulator Enable Inputs. Logic high enables the regulators. The RUN0 and RUN1 pins are pulled down with 1.5mA (typical) during POR and reset to facilitate sequencing with other regulators, but may be over-driven high by a digital output of another device. The pins may be tied directly to DRV_{CC} to enable the regulators when input power is present.

SHARE_CLK (Pin 25): Bidirectional Open-Drain Sequence Time Base Share Clock. Nominally 100kHz. Used to align startup and shutdown of regulator outputs among multiple ADI products when PolyPhase or time-based sequencing is employed. A pull-up resistor to 1.6V to 5.5V is required if the SHARE_CLK function is used. If neither PolyPhase nor time-based sequencing are required, SHARE_CLK may be tied to ground if bit 2 of MFR_CHAN_CONFIG_LT7182S is programmed to zero for both channels (to ignore SHARE_CLK).

WP (Pin 26): Write Protect Input. When this pin is high, only the PAGE, OPERATION, MFR_EE_UNLOCK, and CLEAR_FAULTS commands are writable. Clear individual fault bits by writing a 1 to the respective bits in the STATUS commands.

PIN FUNCTIONS

$\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$ (Pin 28, Pin 27): Fault Input/Open-Drain Outputs. The LT7182S pulls the pin down with 1.5mA (typical) when an unmasked fault occurs on the regulator. If another device pulls down on the $\overline{\text{FAULT}}$ pin, the LT7182S regulator will turn off immediately. If PolyPhase configuration is used, tie together the $\overline{\text{FAULT}}$ pins of all PolyPhase channels. If PolyPhase configuration is used, or if $\overline{\text{FAULT}}$ pin reporting or sharing is required, a pull-up resistor of 6.8k or greater to 1.6V to 5.5V is required. $\overline{\text{FAULT}}$ pins may be tied directly to DRV_{CC} if the $\overline{\text{FAULT}}$ pin function is not required.

$\overline{\text{ALERT}}$ (Pin 29): Open Drain Alert Output. If the $\overline{\text{ALERT}}$ pin function is used, a pull-up resistor to 1.6V to 5.5V is required. If the $\overline{\text{ALERT}}$ pin function is not used, the pin may be tied to ground.

SCL (Pin 30): Serial Bus Clock Input and Output. The LT7182S may hold SCL low if clock stretching is enabled (PMBus speeds 400kHz-1MHz only). A pull-up resistor to 1.6V to 5.5V is required for PMBus/I^2C operation. If serial bus operation is not required, SCL may be tied to ground.

SDA (Pin 31): Serial Bus Data Input and Output. A pull-up resistor to 1.6V to 5.5V is required for PMBus/I^2C operation. If serial bus operation is not required, SDA may be tied to ground.

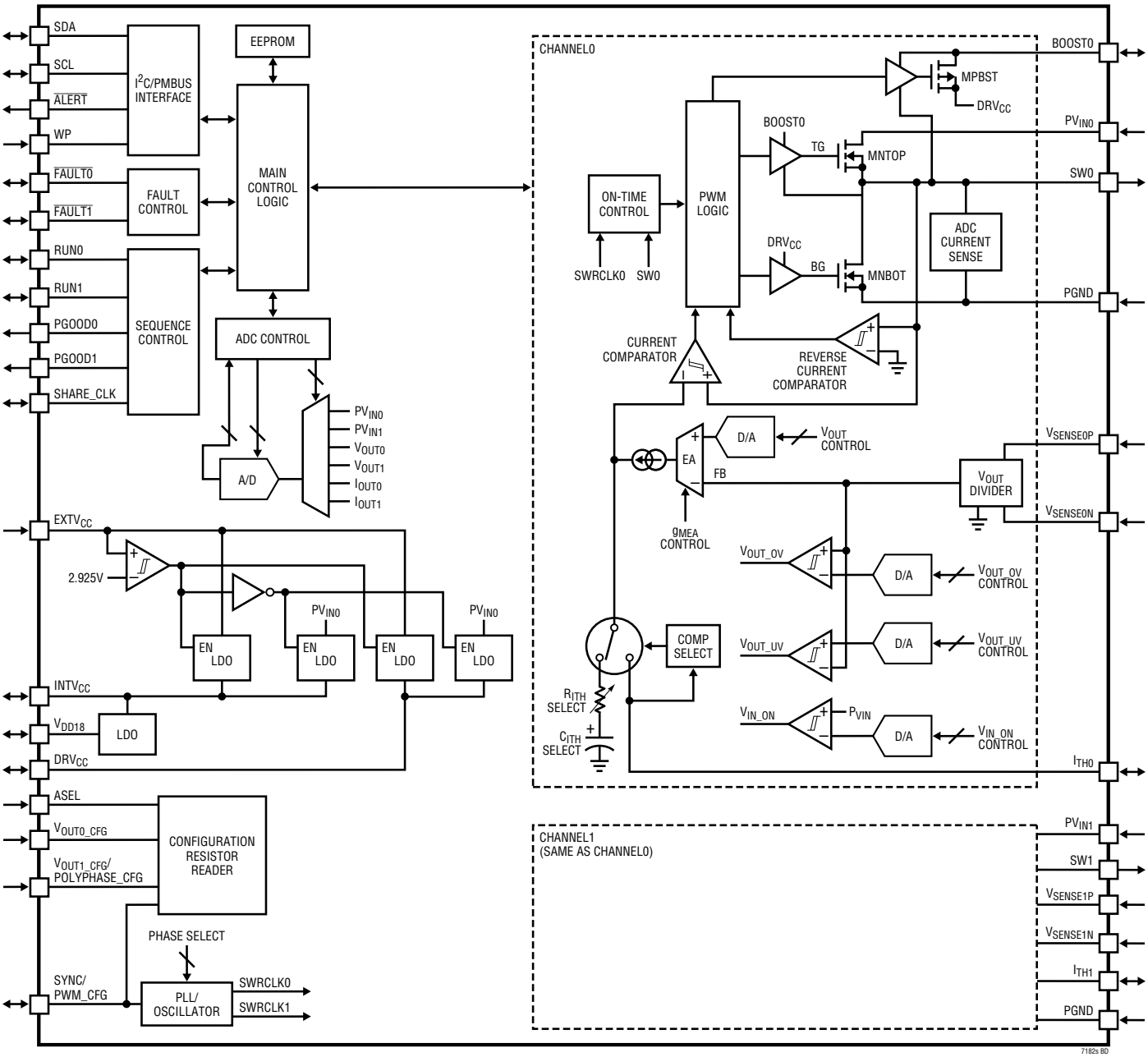
PGOOD0, PGOOD1 (Pin 33, Pin 32): Power Good Indicator Open-Drain Outputs. PGOOD is pulled low when the regulator output is outside of the OV/UV fault thresholds, when the channel is disabled, and during on/off sequencing. The PGOOD output is deglitched by internal configurable timers. If the PGOOD pin function is used, a pull-up resistor to 1.6V to 5.5V is required. If the PGOOD pin function is not used, these pins may tied to PGND.

PV_{IN0} (Pins 35, 38): Power Supply Input for Channel 0 and Internal LDO Regulators. These pins must be tied together and bypassed to PGND as close as possible to the LT7182S, with a low ESR capacitor of value 4.7µF or more. If $EXTV_{CC}$ < 3V, then the internal LDO regulators (for DRV_{CC}, $INTV_{CC}$, and V_{DD18}) pull power from PV_{IN0}.

SW0 (Pins 36, 37, Exposed Pad Pin 41): Output of the Channel0 Internal Power Switches. Tie these pins together and connect them to the channel0 inductor and BOOST0 capacitor. This node should be kept small on the PCB for good performance.

BOOST0 (Pin 40): Boosted Floating Driver Supply. Connect a 0.1µF boost capacitor from BOOST0 to SW0 as close as possible to the IC, using the top PCB layer. The normal operation voltage swing of this pin is from DRV_{CC} to PV_{IN0}+DRV_{CC}.

BLOCK DIAGRAM



OPERATION

OVERVIEW

The LT7182S is a dual-output monolithic PolyPhase DC/DC synchronous step-down regulator. The S in LT7182S refers to the second generation Silent Switcher technology, which provides fast and clean switching edges, reduces overall solution size, improves efficiency, and minimizes EMI emissions. The I^2C-based serial interface is compatible with PMBus 1.3 which supports bus speeds of up to 1MHz.

Major features include:

- Programmable Output Voltage
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable Output Overvoltage and Undervoltage Fault and Warning Thresholds
- Programmable On and Off Delay Times
- Programmable Output Rise/Fall Times
- Programmable Control Loop Compensation
- Programmable Input Undervoltage Threshold
- Dedicated Power Good Pin for Each Channel
- Phase-Locked Loop for Synchronous, PolyPhase Operation (2, 3, 4, 6 or 8 Phases)
- Input and Output Voltage/Current, and Die Temperature Telemetry
- Fully Differential Remote V_{OUT} Sense
- Nonvolatile Configuration Memory with ECC
- Nonvolatile Event-Based Fault Log
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Devices
- WP Pin to Write-Protect Internal Configuration
- Standalone Operation using Configuration Resistors or Nonvolatile Configuration Memory

A variety of mechanisms for fault and warning handling are available. Fault and warning detection capabilities include:

- Output Undervoltage/Overvoltage Fault and Warning
- Internal Overtemperature Fault and Warning
- Communication, Memory or Logic (CML) Fault
- Input Overvoltage Fault and Undervoltage Warning
- Output Overcurrent Fault and Warning
- Average Input Overcurrent Warning
- Internal Reference Fault
- External Fault Detection via the Bidirectional $\overline{FAULT}$ Pins.

A dedicated $\overline{ALERT}$ pin is provided to indicate that faults or warnings have occurred.

Individual status commands enable fault and warning reporting to identify the specific event.

The $\overline{FAULT}$ pins of the LT7182S enable fault sharing between channels and with other ADI power system management products including the LTC3880, LTC2974, LTC2978, LTC4676 µModule®, etc.

Fault reporting and shutdown behavior are fully configurable using the $\overline{FAULT}$ pins and the MFR_FAULT_PROPAGATE_LT7182S command. Faults can be individually masked and the fault responses can be programmed to retry (unlatched) or latch-off the regulator output.

SWITCHING REGULATOR CONTROL LOOP

The LT7182S employs a controlled on-time, valley current mode architecture. In normal operation, the internal top power MOSFET is turned on for an interval determined by an on-time control circuit. When the top power MOSFET turns off, the bottom power MOSFET turns on until the valley current comparator trips, restarting the on-time control circuit and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET when it is on. The voltage on the I_{TH} pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts the I_{TH} voltage by comparing the output voltage

OPERATION

with an internal reference DAC output. If the load current increases, the output voltage drops relative to the internal reference, which causes the I_{TH} voltage to rise until the average inductor current matches that of the load current.

An internal phase-locked loop synchronizes the oscillator frequency to an external clock signal if one is present on the SYNC/PWM_CFG pin. If no external clock is applied, the switching frequency is set by the FREQUENCY_SWITCH command, which may be initialized using configuration resistors (see Applications Information for more details).

LIGHT-LOAD CURRENT OPERATION

The LT7182S has two PWM modes of operation, pulse-skip mode or forced continuous conduction mode. The PWM operating mode is is selected by the MFR_PWM_MODE_LT7182S command bit 0, which can be initialized using configuration resistors as shown in Table 3 and Table 4. Pulse-skip mode is always used during soft-start.

If pulse-skip mode is enabled for a channel, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom switch just before the inductor current reaches zero, preventing it from reversing and going negative. Both power MOSFETs will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current threshold to initiate the next cycle.

In forced continuous mode (FCM), the inductor current is allowed to reverse at light loads or under transient conditions. The inductor valley current is determined by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in pulse-skip mode. However, continuous conduction mode exhibits lower output ripple, more consistent switching frequency, and faster transient response.

EEPROM

The LT7182S contains internal EEPROM to store non-volatile user configuration settings and fault log information.

The integrity of the onboard EEPROM is protected with error correction coding (ECC) and checked with a CRC calculation after a power-on reset or execution of a RESTORE_USER_ALL command. If an invalid CRC is detected, the $\overline{\text{ALERT}}$, SHARE_CLK, PGOOD and RUN pins are pulled low, and both output channels remain disabled until the issue is resolved.

See the LT7182S PMBus/I^2C Reference Manual or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming.

POWER-UP AND INITIALIZATION

The LT7182S is capable of standalone supply sequencing and controlled turn-on and turn-off operation. It operates from either a single input supply or two separate input supplies (PV_{IN0} and PV_{IN1}). To reduce LT7182S power dissipation, $EXTV_{CC}$ can be driven with an external 3V to 5.5V supply or connected to an output of the LT7182S that is providing 3V to 5.5V. If $EXTV_{CC}$ is connected to 3V to 5.5V, the supported PV_{IN0} input operating range is 1.5V to 20V; without $EXTV_{CC}$, the PV_{IN0} operating range is 2.9V to 20V. The PV_{IN1} operating range is 1.5V to 20V. PV_{IN1} and either $EXTV_{CC}$ or PV_{IN0} must be powered in order for channel 1 to operate. $EXTV_{CC}$, PV_{IN0}, and PV_{IN1} may be applied in any order without concern for power supply sequencing of the LT7182S.

The LT7182S is initiliazed upon application of power to PV_{IN0} or $EXTV_{CC}$, or when an MFR_RESET or RESTORE_USER_ALL command is sent. In the initialization step, the LT7182S reads the EEPROM configuration and/or resistor configuration pins to set the intial state of the PMBus commands.

During initialization, the PGOOD pins are held low, SHARE_CLK is held low, the RUN pins are pulled down with 1.5mA (typical), and the $\overline{\text{FAULT}}$ pins are in high impedance state.

If the CFG resistor configuration pins are enabled, the LT7182S initializes certain commands based on the configuration resistor values, which supersede the EEPROM settings. Resistor configuration pins are enabled by factory default. Clear bit 6 of MFR_CONFIG_ALL_LT7182S in EEPROM to disable CFG pins. See Using Resistor Configuration Pins in the Applications Information section for more details. For commands that are not initialized based on the configuration resistors, initial values are determined by EEPROM or factory defaults.

OPERATION

LT7182S initialization typically requires 13ms. If CFG pins are disabled (MFR_CONFIG_ALL_LT7182S bit 6 set to 1 in EEPROM), the initialization time is reduced to 10ms (typical).

After initialization is complete, comparators monitor PV_{IN0} and PV_{IN1}. The PV_{IN} voltage must exceed the channel's programmable V_{IN_ON} threshold for the channel to operate. By default, SHARE_CLK will be held low until PV_{IN0} exceeds V_{IN_ON} for PAGE 0, or if PV_{IN0} falls below V_{IN_OFF}. By default, PV_{IN1} does not affect SHARE_CLK. The default behavior for both channels is to turn off and remain off if SHARE_CLK is low. See the MFR_CHAN_CONFIG_LT7182S command in the LT7182S PMBus/I^2C Reference Manual for information on how to configure this behavior.

The RUN pin pull-down current (1.5mA typical) is released by the LT7182S after the device completes POR initialization and the first time the channel's PV_{IN} potential exceeds the V_{IN_ON} threshold.

SOFT-START

When all conditions required for startup have been met, and a channel is enabled, the LT7182S waits for the commanded turn-on delay and ramps the target output voltage up to the commanded voltage set-point. The soft-start rise time is set by the TON_RISE command, default 1ms. The turn-on delay is set by TON_DELAY, which is 0ms by factory default. The LT7182S PWM always uses pulse-skip mode during soft-start, which allows the regulator to start up into a pre-biased load. If forced continuous conduction mode is selected (MFR_PWM_MODE_LT7182S bit 0 cleared to 0), the channel will transition to continuous conduction mode after the commanded voltage set-point is reached.

SHUTDOWN

The LT7182S can be programmed to turn off immediately or to sequence off.

When sequencing off, the LT7182S waits for the turn-off delay then performs a soft-stop ramp in which the regulation target voltage is ramped down to zero. The turn-off delay is set by the TOFF_DELAY command, default zero. The target voltage ramp-down time is set by TOFF_FALL, default 2ms. By default, the channel will ramp down in forced continuous conduction mode. The ramp-off behavior can be configured using MFR_PWM_MODE_LT7182S.

Sequencing off occurs if OPERATION is set to 0x40, or if the RUN pin is de-asserted and ON_OFF_CONFIG bit 0 is set to 0 and bit 2 is set to 1.

When immediate turn-off occurs, the regulator ramps the inductor current to zero as quickly as possible and then stops switching. In this case, the output voltage will decay based only on the load current and the optional internal 250Ω pull-down. The internal 250Ω pull-down can be disabled by clearing bit 6 of MFR_CHAN_CONFIG_LT7182S. Immediate shutdown occurs in any the following situations:

- PV_{IN} falls below the V_{IN_OFF} threshold
- If the OPERATION command is cleared to 0x00, if ON_OFF_CONFIG bit 3 is set to 1
- A fault condition occurs which causes the output to turn off
- The RUN pin is de-asserted and ON_OFF_CONFIG has been configured such that RUN pin de-assertion causes immediate shutdown (ON_OFF_CONFIG bits 0 and 2 both set to 1)
- The $\overline{FAULT}$ pin for the channel is pulled low externally, unless MFR_FAULT_RESPONSE has been cleared to 0x00.
- Loss of SHARE_CLK, unless bit 2 of MFR_CHAN_CONFIG_LT7182S has been cleared

WARNING AND FAULT HANDLING

The LT7182S continuously monitors the system for fault and warning conditions.

Fault responses are configurable using the corresponding FAULT_RESPONSE commands, such as VOUT_UV_FAULT_RESPONSE, VOUT_OV_FAULT_RESPONSE, etc. Possible fault responses are as follows:

- Continue Operation (Ignore)
- Shut down immediately and retry if fault condition is no longer present

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- Shut down immediately and latch off

The remainder of this section describes the factory default warning and fault behavior. See Table 1.

See the LT7182S PMBus/I^{2}C Reference Manual for details on configuring fault and warning behavior.

All faults and warnings are indicated in PMBus STATUS commands.

When a warning occurs related to output voltage, output current, or temperature, the LT7182S pulls the $\overline{\text{ALERT}}$ pin low, the corresponding bit is set in the appropriate STATUS command(s), and the channel continues to operate.

If the output voltage falls below VOUT_UV_FAULT_LIMIT, the LT7182S responds as follows:

- The channel's PGOOD pin is pulled low
- The $\overline{\text{ALERT}}$ pin is pulled low
- The VOUT_UV fault bit is set in the STATUS_VOUT, STATUS_BYTE, and STATUS_WORD commands.
- The channel continues to operate while limiting the maximum valley current

If a fault occurs due to output overvoltage, or input overvoltage, the LT7182S responds as follows:

- The faulted channel(s) are shut down immediately.
- The channel's $\overline{\text{FAULT}}$ pin and PGOOD pin are pulled low
- The $\overline{\text{ALERT}}$ pin is pulled low
- The corresponding indicator bit(s) are set in the appropriate STATUS command(s)
- After 10ms (time defined by MFR_RETRY_DELAY), the channel attempts to restart when the fault condition is no longer present

If a fault occurs due to overtemperature, the LT7182S responds as follows:

- Both channels are shut down immediately.
- Both channels' $\overline{\text{FAULT}}$ pins and PGOOD pins are pulled low
- The $\overline{\text{ALERT}}$ pin is pulled low
- The overtemperature (OT) bit is set in the appropriate STATUS command(s)
- When the ADC measures that the temperature is below the overtemperature threshold, the channel attempts to restart

The LT7182S periodically compares the primary internal voltage reference against a secondary internal voltage reference using the ADC. If a failure is detected, the LT7182S responds as follows:

- Both channels are shut down immediately.
- The $\overline{\text{FAULT}}$ pins, PGOOD pins, and $\overline{\text{ALERT}}$ pins are pulled low
- The internal reference fault bit is set in the STATUS commands
- Both channels remain off unless the reference recovers (for example due to temperature drift), a RESTORE_USER_ALL or MFR_RESET command is received, or input power is removed from both PV_{IN0} and $EXTV_{CC}$

$\overline{\text{FAULT}}$ Pins

A fault will cause the $\overline{\text{FAULT}}$ pin to pull low if the corresponding FAULT_RESPONSE command is programmed to shut down the regulator output and the MFR_FAULT_PROPAGATE_LT7182S command is configured to propagate the fault to the open-drain $\overline{\text{FAULT}}$ pins.

Once the LT7182S pulls down a $\overline{\text{FAULT}}$ pin, the device will continue to hold the pin low until one of the following occurs:

- The channel retries, for faults that are configured to retry
- The faulted channel is disabled then re-enabled
- A RESTORE_USER_ALL or MFR_RESET command is received
- Input power is removed from both PV_{IN0} and $EXTV_{CC}$

The $\overline{\text{FAULT}}$ pin can also be used as an input to provide a method for the LT7182S to respond to external faults. The channel turns off immediately if the channel's $\overline{\text{FAULT}}$ pin is pulled low externally. This enables coordination of faults among multiple power system management products.

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PGOOD Pins

The open-drain PGOOD pins are each pulled low if the corresponding channel is off for any reason, during soft-start and soft-stop, or if the output voltage is below VOUT_UV_FAULT_LIMIT.

$\overline{\text{ALERT}}$ Pin

The SMBALERT_MASK command configures which warning and fault indicators cause the LT7182S to pull down the open-drain $\overline{\text{ALERT}}$ pin.

Once the LT7182S pulls down the $\overline{\text{ALERT}}$ pin, the device will continue to hold the pin low until one of the following occurs:

- The faulted channel is disabled then re-enabled
- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET command is received
- All unmasked status bits are cleared by writing a 1 to each bit
- The LT7182S successfully transmits its address during a PMBus ARA
- Input power is removed from both PV_{IN0} and $EXTV_{CC}$

Fault Event Logging

If a fault condition occurs that is configured to turn off the regulator output, an event is written in the fault log in EEPROM. Any preceeding warning or fault that is not configured to turn off the output is written as a sub-event when an event is written. A timestamp is written with each event and subevent. The fault log stores up to three fault-off events. The fault log may be read by the MFR_FAULT_LOG command. The fault log is cleared from EEPROM by writing the MFR_FAULT_LOG_CLEAR command. The fault log function is enabled by default and may be disabled by clearing bit 7 of MFR_CONFIG_ALL.

See the MFR_FAULT_LOG command in the LT7182S PMBus/I^2C Reference Manual for more details.

Table 1. Factory-Default Warning and Fault Behavior (Note 1)

WARNING OR FAULT TYPE	DETECTION METHOD	DEFAULT THRESHOLD	DEFAULT REGULATOR RESPONSE	DEFAULT PIN RESPONSE		
				PGOOD	FAULT	ALERT
V_{OUT} UV Warning	Comparator	VOUT_COMMAND –6.5%	Continue Operation			Pull Low
V_{OUT} OV Warning	Comparator	VOUT_COMMAND +7.5%	Continue Operation			Pull Low
V_{OUT} UV Fault	Comparator	VOUT_COMMAND –7%	Continue Operation	Pull Low		Pull Low
V_{OUT} OV Fault	Comparator	VOUT_COMMAND +10%	Shutdown and Retry	Pull Low	Pull Low	Pull Low
V_{IN} OV Fault	Comparator	23.3V	Shutdown and Retry	Pull Low	Pull Low	Pull Low
V_{IN} UV Warning	ADC	–1.0V (Disabled)	Continue Operation			Pull Low
Overtemperature (OT) Warning	ADC	140°C	Continue Operation			Pull Low
OT Fault	ADC	160°C	Shutdown and Retry	Pull Low	Pull Low	Pull Low
I_{OUT} Overcurrent (I_{OUT_OC}) Warning	ADC	I_{AVG} > 8A	Continue Operation			Pull Low
I_{OUT} OC Fault	Valley Comparator	I_{VALLEY} > 6.5A (Note 2)	Continue Operation			
Turn-On Time (t_{ON_MAX}) Fault	Comparator and Timer	5ms without Exceeding VOUT_UV_FAULT_LIMIT	Continue Operation	Pull Low		Pull Low
Turn-Off Time (t_{OFF_MAX}) Warning	ADC and Timer	0 (Disabled)	N/A			
Pin Configuration Error (Note 3)	I/O	N/A	Lock Off Until Next Reset	Pull Low	Pull Low	Pull Low
EEPROM Error	CRC, ECC	N/A	Lock Off Until Next Reset	Pull Low		Pull Low
Internal Reference Fault	ADC and 2nd Reference	±5%	Shutdown and Retry	Pull Low	Pull Low	Pull Low
PMBus/I^2C Communication Error (CML)	Logic	N/A	N/A			Pull Low

Note 1. See the LT7182S PMBus/I^2C Reference Manual for detailed information including configuring thresholds and responses.

Note 2. The IOUT_OC_FAULT valley current threshold is controlled by MFR_PWM_MODE_LT7182S bits [10:9].

Note 3. When a pin configuration error is detected during initialization, the device pulls low the following pins: $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, RUN0, RUN1, SHARE_CLK, PGOOD0, PGOOD1, and $\overline{\text{ALERT}}$.

APPLICATIONS INFORMATION

USING RESISTOR CONFIGURATION PINS

The LT7182S has four resistor configuration pins each utilizing a single ±1% resistor to select key operating parameters. The resistor configuration pins are ASEL, V_{OUT0_CFG}, V_{OUT1_CFG}/POLYPHASE_CFG, and SYNC/PWM_CFG. The resistor configuration pins are measured upon power-up and execution of a RESTORE_USER_ALL or MFR_RESET command. The function of each resistor configuration pin is described in the sections below.

If bit 6 of the MFR_CONFIG_ALL_LT7182S command is set to 1 in EEPROM, the configuration resistors are ignored on CFG pins V_{OUT0_CFG}, V_{OUT1_CFG}/POLYPHASE_CFG, and SYNC/PWM_CFG, while the ASEL resistor is always respected.

See the MFR_ADDRESS command in the LT7182S PMBus/I^{2}C Reference Manual for information about setting the serial interface device address including ASEL configuration resistor selection.

SETTING OUTPUT VOLTAGE

The VOUT_COMMAND PMBus command specifies the output voltage when the channel is enabled.

VOUT_COMMAND can be initialized using resistors on the V_{OUT0_CFG} and V_{OUT1_CFG}/POLYPHASE_CFG pins, based on the values in Table 2. A resistor between V_{OUT0_CFG} and SGND configures channel 0. If channel 1 is configured as an independent output from channel 0, then a resistor between the V_{OUT1_CFG}/POLYPHASE_CFG pin and SGND configures channel 1. If PolyPhase configuration is selected (by connecting a 5.6k ±10% resistor between SYNC/PWM_CFG and ground) then V_{OUT0_CFG} configures both channels 0 and 1.

Table 2. V_{OUTn_CFG} Pin Configuration Resistor Selection (Note 1)

RESISTOR VALUE (±1%)	OUTPUT VOLTAGE SET POINT (V) (Note 2)	V_{OUT} RANGE MODE (Note 3)	REGULATOR ENABLE (Note 4)
Floating or V_{DD18}	Initialized from NVM (Default 0.5V)	Initialized from NVM (Default full V_{OUT} range).	Initialized from NVM (By default, regulator is enabled if RUN pin is asserted high.)
124kΩ	5	Full V_{OUT} range. Supports $0.4V \le V_{OUT} \le 5.5V$.	Regulator is enabled if RUN is asserted high. (OPERATION = 0x80. ON_OFF_CONFIG initialized from NVM, default requires OPERATION = 0x80 and RUN pin asserted.)
107kΩ	3.3		
93.1kΩ	2.5		
80.6kΩ	1.8		
69.8kΩ	1.5		
60.4kΩ	1.35		
51.1kΩ	1.2	High-performance Low-V_{OUT} range. Offers enhanced accuracy and transient response for $V_{OUT} \le 1.375V$.	
43.2kΩ	1.1		
36.5kΩ	1		
30.9kΩ	0.9		
25.5kΩ	0.85		
21kΩ	0.8		
16.5kΩ	0.75		
11.8kΩ	0.7		
6.65kΩ	0.6		
0 (SGND)	Initialized from NVM (Default 0.5V)	Initialized from NVM (default full V_{OUT} range)	Regulator disabled and RUN pin ignored.

Note 1. If the SYNC/PWM_CFG pin is connected to a 5.6kΩ ±10% resistor to select Polyphase operation as per Table 3, then the V_{OUT1_CFG}/POLYPHASE_CFG configuration resistor controls PWM settings including frequency and phase per Table 4.

Note 2. Output voltage set point is controlled by VOUT_COMMAND.

Note 3. V_{OUT} Range Mode selection is controlled by MFR_PWM_MODE_LT7182S bit 1. A value of 1 selects High-Performance Low-V_{OUT} mode.

Note 4. The PMBus ON_OFF_CONFIG command selects whether the RUN pin and/or PMBus OPERATION command enable the regulator.

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If the V_{OUTn_CFG} pin is open or tied to V_{DD18}, the VOUT_COMMAND command is loaded from EEPROM to determine the output voltage. The default EEPROM setting is to initialize with the regulator disabled unless the voltage configuration resistors are installed.

The following commands are initialized based on a percentage of VOUT_COMMAND if the resistor configuration pins are used to initialize the output voltage:

- VOUT_OV_FAULT_LIMIT +10%
- VOUT_OV_WARN_LIMIT +7.5%
- VOUT_MAX +7.5%
- VOUT_MARGIN_HIGH +5%
- VOUT_MARGIN_LOW –5%
- VOUT_UV_WARN_LIMIT –6.5%
- VOUT_UV_FAULT_LIMIT –7%

SWITCHING FREQUENCY AND PHASE

The PWM switching frequency can be established using the internal oscillator or applying an external clock on the SYNC/PWM_CFG pin. An internal phase-locked loop (PLL) synchronizes PWM control to this timing reference, whether the clock is provided internally or externally. The internal oscillator frequency is set by the FREQUENCY_SWITCH command. The MFR_PWM_PHASE_LT7182S command configures the phase of each channel.

The SYNC/PWM_CFG pin is a flexible multi-purpose input/output pin, which can be used as a configuration resistor input as well as a clock input or output.

A configuration resistor connected between SYNC/PWM_CFG and ground (PGND or SGND) may be used to initialize PWM configuration (including frequency, phase, and operating mode) according to Table 3. See Figure 1 for an example of PWM configuration resistor connection for single- and dual-phase applications where no external synchronization input or output clock is required. See Table 2 for PWM_CFG resistor selection options.

The LT7182S will automatically synchronize PWM switching to an external clock input on SYNC/PWM_CFG, unless the LT7182S has been configured as an output driver or has been programmed to ignore the input clock. When an external synchronization clock is used on the SYNC/PWM_CFG pin, the LT7182S automatically uses forced continuous mode on both channels. The LT7182S will continue PWM operation using its own internal oscillator if the external clock signal is lost. If an external synchronization clock is to be used, it is recommended to program the FREQUENCY_SWITCH command or to use a configuration resistor to set the internal oscillator frequency to a similar value to the external clock frequency. This ensures that the PWM switching frequency remains reasonable if the external clock is lost. The LT7182S can be programmed to ignore an external clock by writing a 1 to bit 1 of MFR_SYNC_CONFIG_LT7182S.

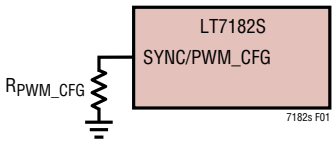

Figure 1. PWM Resistor Configuration with No External Clock

The LT7182S can be configured to provide a synchronizing clock output on the SYNC/PWM_CFG pin to other devices by setting bit 0 of MFR_SYNC_CONFIG_LT7182S to 1.

If the SYNC/PWM_CFG output clock is enabled, the LT7182S will drive the SYNC/PWM_CFG pin as a square wave from 0 to 1.88V (typical) at the frequency programmed in FREQUENCY_SWITCH. The phase of SYNC will lead the phase of the PWM output by the value set in the MFR_PWM_PHASE_LT7182S command. Only one device connected to SYNC/PWM_CFG may be configured as an output.

When a clock is active on SYNC/PWM_CFG, the MFR_PWM_PHASE_LT7182S command specifies the phase relationship between the rising edge of SYNC/PWM_CFG and the rising edge of SW for the channel.

If both the SYNC/PWM_CFG configuration resistor and synchronization clock input functions are utilized, the clock signal must be AC-coupled using a 1.5nF capacitor between the clock source and the LT7182S, as shown in Figure 2. In this case, the clock signal must be inactive during LT7182S initialization to ensure it does not interfere with the resistor configuration function. If the AC-coupled clock source output impedance is less than 50Ω, a 50Ω

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Table 3. SYNC/PWM_CFG Pin Configuration Resistor Selection

RESISTOR VALUE (±1%)	PWM FREQUENCY (Notes 1, 2)	PWM PHASE (Note 3)		PWM MODE (Note 4)	PolyPhase FOLLOWER/ LEADER (Note 5)	INTERNAL COMPENSATION (Note 6)			SYNC/PWM_CFG CLOCK OUTPUT OR INPUT (Note 8)
		Ch 0	Ch 1			INTERNAL C_{ITH}	INTERNAL R_{ITH}	INTERNAL g_{MEA}	
162kΩ	Initialized from NVM (Default 1MHz)	Initialized from NVM (Default 0°)	Initialized from NVM (Default 180°)	Initialized from NVM (Default FCM)	Initialized from NVM (Default 0, Leader)	Initialized from NVM (Default 80pF)	Initialized from NVM (Default 20kΩ)	Initialized from NVM (Note 7)	Initialized from NVM (Default 0, Input)
124kΩ	500kHz	0°	180°	FCM	0 (Leader)	80pF	20kΩ	150µS	0 (Input)
80.6kΩ	1MHz					80pF	40kΩ		
51.1kΩ	2MHz					80pF	40kΩ		
30.9kΩ	4MHz					60pF	40kΩ		
107 kΩ	500kHz	90°	270°			80pF	20kΩ		
69.8kΩ	1MHz					80pF	40kΩ		
43.2kΩ	2MHz					80pF	40kΩ		
93.1kΩ	500kHz	0°	180°	Pulse-skip		80pF	20kΩ		
60.4kΩ	1MHz					80pF	40kΩ		
36.5kΩ	2MHz					80pF	40kΩ		
Clock Active Throughout POR and Reset	Measured at POR/Reset	0°	180°	FCM	NVM (Default 0, Leader)	(Note 9)			
5.6kΩ ±10%	PolyPhase Configuration Select: PWM Configuration is controlled by the V_{OUT1_CFG}/POLYPHASE_CFG pin, as indicated in Table 4. In this configuration, V_{OUT} for both channels is initialized to the value specified by the V_{OUT0_CFG} resistor.								

Note 1. PWM Switching frequency set point is controlled by FREQUENCY_SWITCH, if no SYNC/PWM_CFG input clock is present.

Note 2. If an external synchonrization clock is used as well as a configuration resistor, the clock source must be AC-coupled with a 1.5nF series capacitor, and the clock source must be inactive during initialization of the LT7182S. The configuration resistor value should be chosen to set the internal PWM switching frequency to a similar value to the input clock.

Note 3. Steady-State PWM Switching Phase is controlled by MFR_PWM_PHASE_LT7182S.

Note 4. PWM Mode is controlled by MFR_PWM_MODE_LT7182S bit 0. A value of 1 enables pulse-skip mode.

Note 5. Poly-phase follower/leader mode is controlled by MFR_CHAN_CONFIG_LT7182S bit 8. A value of 1 selects follower mode.

Note 6. Internal compensation is selected by tying I_{TH} to $INTV_{CC}$. For PWM_CFG resistor values ≤ 124kΩ, if external compensation is used, g_{mEA} is set to the maximum value (1.2mS for High-Performance Low-V_{OUT} mode; 300µS for Standard mode). For internal compensation, C_{ITH} is controlled by MFR_PWM_MODE_LT7182S bits [8:6], and R_{ITH} is controlled by MFR_PWM_MODE_LT7182S bits [5:3]. g_{mEA} is controlled by MFR_PWM_MODE_LT7182S bits [13:11].

Note 7. The NVM default for MFR_PWM_MODE_LT7182S bits [11:9] is 0b011, which corresponds to g_{mEA} = 600µS for High-Performance Low-V_{OUT} mode and g_{mEA} = 150µS for Standard mode, regardless of internal or external compensation.

Note 8. The SYNC/PWM_CFG pin is a clock output when MFR_SYNC_CONFIG_LT7182S bit 0 is set to 1.

Note 9. When an external clock is detected during POR/reset of the LT7182S, internal compensation parameters C_{ITH} and R_{ITH} are chosen based on the measured external clock frequency:

- 400kHz to 625kHz: R_{ITH} = 20kΩ, C_{ITH} = 80pF
- 625kHz to 1.25MHz: R_{ITH} = 40kΩ, C_{ITH} = 80pF
- 1.25MHz to 2.5MHz: R_{ITH} = 40kΩ, C_{ITH} = 80pF
- 2.5MHz to 4MHz: R_{ITH} = 40kΩ, C_{ITH} = 60pF

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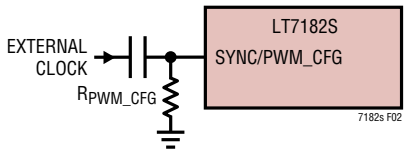

NOTE: EXTERNAL CLOCKMUST BE INACTIVE
DURING LT7182S INITIALIZATION

Figure 2. PWM Resistor Configuration and an External Synchronization Clock

resistor must be added in series with the clock source. See Table 2 for PWM_CFG resistor selections.

For an input clock frequency of 400kHz to 625kHz, it is recommended to use a configuration resistor that selects a PWM frequency of 500kHz. For an input clock frequency of 625kHz to 1.25MHz, it is recommended to use a configuration resistor that selects a PWM frequency of 1MHz. For an input clock frequency of 1.25MHz to 2.5MHz, it is recommended to use a configuration resistor that selects a PWM frequency of 2MHz. For an input clock frequency of 2.5MHz to 4MHz, it is recommended to use a configuration resistor that selects a PWM frequency of 4MHz.

If the SYNC/PWM_CFG pin is used only as a clock input or output and MFR_CONFIG_ALL_LT7182S bit 6 has been written to 1 in EEPROM to disable CFG pins, then no configuration resistor or AC-coupling capacitor is required.

If an external clock is applied to the SYNC/PWM_CFG pin throughout initialization, and the CFG pin function has not been disabled, the LT7182S measures the clock frequency and initializes FREQUENCY_SWITCH to the measured frequency rounded to the nearest 100kHz. In this case, channel 0 MFR_PWM_PHASE is initialized to 0 degrees and channel 1 to 180 degrees and forced continuous mode is selected. Note that, unless CFG pin functionality has been disabled, an external clock applied to SYNC/PWM_CFG must be either active or inactive throughout the entire LT7182S initialization process. If the clock activity changes during initialization, for example if the clock starts after initialization begins but before it completes, the frequency measurement may be inaccurate which could lead to the LT7182S incorrectly initializing FREQUENCY_SWITCH or declaring a pin configuration fault. See MFR_PIN_CONFIG_STATUS in the LT7182S PMBus/I^2C Reference Manual for more information regarding pin configuration faults.

PolyPhase Load Sharing

Multiple LT7182S channels can be connected in parallel to provide a balanced PolyPhase load-share solution. The analog current mode control architecture of the LT7182S ensures that load-sharing remains balanced among the PolyPhase channels.

The corresponding I_{TH}, $\overline{FAULT}$, PV_{IN}, V_{SENSEP} and V_{SENSEN} pins must be connected among all PolyPhase channels, and the SYNC/PWM_CFG and SHARE_CLK pins must be connected among all PolyPhase devices. The phases should be separated by 360/n degrees, where n is the number of phases in the PolyPhase array. In PolyPhase, exactly one device, either an LT7182S or an external clock source, must be configured to drive a clock on SYNC/PWM_CFG.

In a PolyPhase array, exactly one LT7182S channel must be configured as a leader (MFR_CHAN_CONFIG_LT7182S bit 8 value of 0), and all other PolyPhase channels must be configured as followers (value set to 1).

PolyPhase mode can be selected by connecting a 5.6k ±10% resistor from SYNC/PWM_CFG to ground if MFR_CONFIG_ALL_LT7182S bit 6 is not set to ignore CFG pins. Resistor configuration options are available to support 2, 3, 4, or 6 phase PolyPhase solutions. When a 5.6k resistor is connected on SYNC/PWM_CFG, VOUT_COMMAND for channel 1 is set to the same value as channel 0 based on the V_{OUT0_CFG} resistor, and the V_{OUT1_CFG}/POLYPHASE_CFG resistor selects the PolyPhase configuration as shown in Table 4. For 2, 4, or 6 phase operation, the SYNC/PWM_CFG pins of up to three LT7182S devices may be connected together to a single 5.6k resistor, as shown in Figure 3. For two LT7182S devices configured for 3 phase + 1 phase operation, separate SYNC/PWM_CFG configuration resistors are required along with a 1.5nF AC-coupling capacitor between the devices, as shown in Typical Applications. For PolyPhase arrays with 8 or more phases, PMBus programming is required for at least some of the devices, in order to set PolyPhase follower mode (MFR_CHAN_CONFIG_LT7182S bit 8) and select the appropriate phase (MFR_PWM_PHASE_LT7182S).

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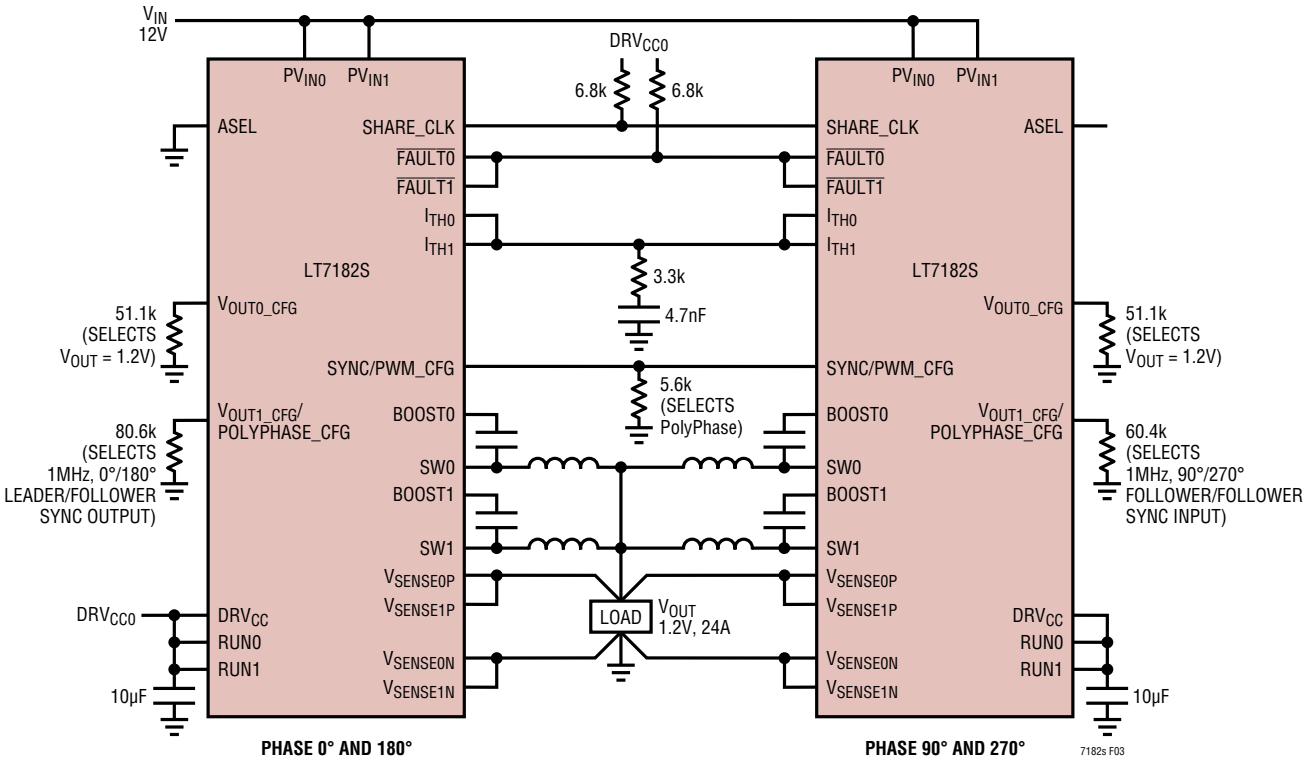

Figure 3. Example Four-Phase PolyPhase 1.2V, 1Mhz, 24A Regulator Using Resistor Configuration Pins with No External Clock

Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used, while the primary disadvantage is lower efficiency.

Minimum On-Time and Minimum Off-Time Considerations

The minimum on-time, $t_{ON(MIN)}$, is the smallest duration of time in which the top power MOSFET can be in its on state. This time is a function of output load, and is typically about 20ns at 1A load. In continuous conduction, the worst-case minimum on-time limit imposes a maximum switching frequency of:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN} \bullet 40ns} \quad (1)$$

Where 40ns corresponds to the worst-case upper limit of $t_{ON(MIN)}$ at no load and maximum junction temperature of 150°C, and $f_{SW(MAX)}$ is the maximum supported switching frequency. If the frequency is set higher than $t_{ON(MIN)}$ allows, the LT7182S valley current control architecture will keep the output voltage in regulation, and the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance. High switching frequencies may be used in the design without causing output overvoltage. However, if frequency synchronization is required (such as in PolyPhase), f_{SW} should be set no higher than the maximum value achievable at the maximum $t_{ON(MIN)}$ of 40ns and the maximum V_{IN} and minimum V_{OUT} for the application.

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LT7182S is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the bottom power MOSFET back off. This time is typically about 60ns . The minimum off-time imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the ratio V_{OUT}/V_{IN} exceeds the maximum duty cycle, for example due to input voltage dropping, then the output voltage will drop out of regulation.

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Table 4. PolyPhase Operation V_{OUT1_CFG}/POLYPHASE_CFG Pin Configuration Resistor Selection (Note 1)

RESISTOR VALUE (±1%)	PWM FREQUENCY (Note 2)	PWM PHASE (Note 3)		PWM MODE (Note 4)	PolyPhase FOLLOWER (Note 5)		SYNC/PWM_CFG CLOCK OUTPUT OR INPUT (Note 6)
		Ch 0	Ch 1		Ch 0	Ch 1	
Floating or V_{DD18}	Initialized from NVM (Default 1MHz)	Initialized from NVM (Default 0°)	Initialized from NVM (Default 180°)	0 (Forced Continuous Mode)	Initialized from NVM (Default 0, Leader)		Initialized from NVM (Default 0, Input)
124kΩ	500kHz	0°	180°		0 (Leader)	1 (Follower)	1 (Output)
80.6kΩ	1MHz						
36.5kΩ	2MHz						
16.5kΩ	4MHz						
107kΩ	500kHz						0 (Input)
69.8kΩ	1MHz						
30.9kΩ	2MHz						
11.8kΩ	4MHz						
93.1kΩ	500kHz	90°	270°		1 (Follower)	1 (Follower)	
60.4kΩ	1MHz						
25.5kΩ	2MHz						
6.65kΩ	4MHz						
51.1kΩ	1MHz	120°	240°				1 (Output)
21.0kΩ	2MHz						
43.2kΩ	1MHz	60°	300°				0 (Input)
0Ω (Grounded)	2MHz						

Note 1. Table 4 applies only if SYNC/PWM_CFG is connected to a 5.6kΩ configuration resistor. Otherwise, V_{OUT1_CFG}/POLYPHASE_CFG controls the output voltage for channel 1 according to Table 2.

Note 2. PWM Switching frequency is controlled by FREQUENCY_SWITCH, if no SYNC/PWM_CFG input clock is present.

Note 3. Steady-State PWM Switching Phase is controlled by MFR_PWM_PHASE_LT7182S.

Note 4. PWM Mode is controlled by MFR_PWM_MODE_LT7182S bit 0. A value of 1 enables pulse-skip mode.

Note 5. PolyPhase follower mode is controlled by MFR_CHAN_CONFIG_LT7182S bit 8. A value of 1 selects follower mode.

Note 6. The SYNC/PWM_CFG pin is a clock output when MFR_SYNC_CONFIG_LT7182S bit 0 is set to 1

To avoid the output voltage dropping out of regulation due to the $t_{OFF(MIN)}$ limitation, the switching frequency should be set no higher than:

$$f_{SW} \leq \frac{1-\frac{V_{OUT(MAX)}}{V_{IN(MIN)}}}{100ns} \quad (2)$$

based on the minimum input voltage and maximum output voltage for the application. Note that 100ns corresponds to the maximum $t_{OFF(MIN)}$ for the LT7182S.

PROGRAMMABLE CURRENT LIMIT

The LT7182S current limit operates by limiting the output current based on the valley of the inductor current ripple waveform, as shown in Figure 4 and Figure 5.

As shown in Figure 4, when positive valley current limit is engaged (providing output current to the load), the inductor valley current is $I_{LIM-POS}$, the average output current is $I_{LIM-POS} + \Delta I_L/2$, and the peak inductor current is $I_{LIM-POS} + \Delta I_L$, where ΔI_L is the inductor ripple current. If $I_{LIM-POS}$ is reached, the IOUT_OC fault STATUS bit will be set. See the STATUS commands in the LT7182S PMBus/I^2C Reference Manual.

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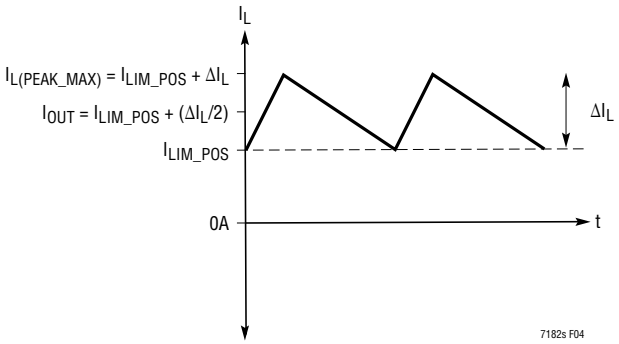

Figure 4. Positive Valley Current Limit

As shown in Figure 5, when negative valley current limit occurs (sinking output current due to the output being pulled up externally), the inductor valley current is $I_{LIM-NEG}$, the average output current is $I_{LIM-NEG} + \Delta I_L/2$, and the peak inductor current is $I_{LIM-NEG} + \Delta I_L$.

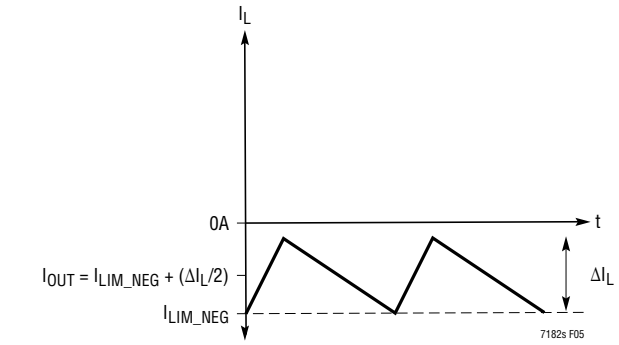

Figure 5. Negative Valley Current Limit

The LT7182S offers four settings for the valley current limit. The current limit selection is controlled by MFR_PWM_MODE_LT7182S bits [10:9] as shown in Table 5. The factory default current limit setting is 6.5A (typical) positive valley current limit, and –4.5A (typical) negative valley current limit. Note that the modulator current sense gain (dI_{OUT}/dV_{ITH}) is also changed as the current limit selection is changed, which must be considered in control loop compensation.

Table 5. Valley Current Limit Selection, MFR_PWM_MODE_LT7182S bits [10:9]

VALUE	POSITIVE VALLEY CURRENT LIMIT I_{LIM_POS} (Typ)	NEGATIVE VALLEY CURRENT LIMIT I_{LIM_NEG} (Typ)	CURRENT SENSE TRANSCONDUCTANCE dI_{OUT}/dV_{ITH} (Typ)
3	8.5A	–4.25A	14.2A/V
2 (Default)	6.5A	–4A	11.7A/V
1	4.5A	–3.4A	8.8A/V
0	3A	–2.3A	5.9A/V

INDUCTOR SELECTION

For a given application input voltage and output voltage, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Lower ripple current reduces losses in the inductor and ESR losses in the output capacitors and reduces output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

The inductor must be chosen such that the inductor current ripple is less than twice the maximum (least negative) negative valley current limit indicated in the Electrical Characteristics table, or an output overvoltage will occur:

$$\Delta I_L \leq 2 \bullet I_{LIM\_NEG(MAX)} \quad (5)$$

An inductor must be chosen with a saturation current (typically labeled I_{SAT}) higher than the maximum peak current when operating in current limit:

$$I_{L(PEAK,MAX)} = I_{LIM\_POS} + \Delta I_L \quad (6)$$

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To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. Preferably, the inductor RMS rating supports the average inductor current in current limit:

$$I_{L(AVG,MAX)} = I_{LIM(POS)} + \frac{\Delta I_L}{2} \quad (7)$$

If the inductor current rating does not support $I_{L(AVG,MAX)}$ described in Equation 7, either select a suitable current limit, or set the VOUT_UV_FAULT_RESPONSE command to disable the channel if the output voltage falls below VOUT_UV_FAULT_LIMIT. The default setting of VOUT_UV_FAULT_RESPONSE is to continue operation at valley current limit while the V_{OUT} UV fault condition is present.

For highest efficiency, the inductor series resistance (DCR) should be minimized and its core material should be intended for high frequency applications.

INPUT AND OUTPUT CAPACITORS

Low ESR ceramic capacitors should be used at both the output and input supplies of the switching regulators. X5R or X7R ceramic capacitors are recommended for best performance over temperature and applied voltage.

See the Typical Applications in this data sheet for suggested capacitor values.

PROGRAMMABLE PWM CONTROL LOOP COMPENSATION

The LT7182S supports internal or external PWM control loop compensation as shown in Figure 6 and Figure 7. For single-phase applicaions, internal compensation is selected by tying the channel's I_{TH} pin to $INTV_{CC}$. PolyPhase operation requires external compensation, and I_{TH} pins of all PolyPhase channels must be connected to one external compensation network.

Control loop compensation parameters can be programmed using the MFR_PWM_MODE_LT7182S command. In either internal or external compensation, the transconductance of the LT7182S PWM error amplifier can be adjusted using MFR_PWM_MODE_LT7182S bits [13:11] as shown in Table 6. When internal compensation is selected, the internal PWM loop compensation resistor R_{ITH} of the LT7182S can be adjusted in non-linear increments from 5k to 120k (typical) using MFR_PWM_MODE_LT7182S bits [5:3] as shown in Table 7. The internal compensation capacitor C_{ITH} can be adjusted in 10pF increments from 10pF to 80pF (typical) using MFR_PWM_MODE_LT7182S bits [8:6] as shown in Table 8.

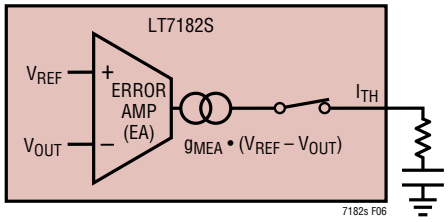


Figure 6. External Compensation, with Programmable g_{MEA}

Table 6. Programmable Error Amp Transconductance g_{MEA}

MFR_PWM_MODE_LT7182S BITS [13:11]	FULL V_{OUT} RANGE MODE	HIGH-PERFORMANCE LOW-V_{OUT} MODE
7	300µS	1.2mS
6	262.5µS	1.05mS
5	225µS	900mS
4	187.5µS	750µS
3	150µS	600µS
2	112.5µS	450µS
1	75µS	300µS
0	37.5µS	150µS

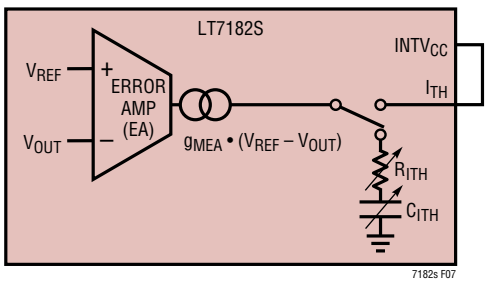


Figure 7. Programmable Internal Compensation

APPLICATIONS INFORMATION

Table 7. Programmable Internal Compensation Lead Resistor R_{ITH}

MFR_PWM_MODE_LT7182S BITS [5:3]	INTERNAL R_{ITH} VALUE
7	120kΩ
6	100kΩ
5	80kΩ
4	60kΩ
3	40kΩ
2	20kΩ
1	10kΩ
0	5kΩ

Table 8. Programmable Internal Compensation Capacitor C_{ITH}

MFR_PWM_MODE_LT7182S BITS [8:6]	INTERNAL C_{ITH} VALUE
7	80pF
6	70pF
5	60pF
4	50pF
3	40pF
2	30pF
1	20pF
0	10pF

SOFTWARE-CONFIGURABLE SEQUENCING

Time-based sequencing offers a software-configurable means of defining a system's power-up and power-down sequence. To employ time-based sequencing, program TON_DELAY to independently delay each channel so that its soft-start ramp begins at the correct point in the sequence. The sequence begins when all channels are commanded on simultaneously using either the OPERATION command or RUN pins. Similarly, turn-off sequencing is coordinated using the TOFF_DELAY command.

When using time-based sequencing among multiple ADI devices, it is recommended that the SHARE_CLK pins of the devices be connected together to a pull-up resistor to 1.6V to 5.5V.

EVENT-BASED SEQUENCING

Event-based sequencing offers a hardware-configurable means of defining a system's power-up and power-down sequence.

The PGOOD pin from one regulator may be connected to the RUN pin of the next regulator in the sequence as shown in Figure 8.

The LT7182S holds the PGOOD pin low until the channel's soft-start ramp is complete and its output voltage exceeds the value set in VOUT_UV_FAULT_LIMT.

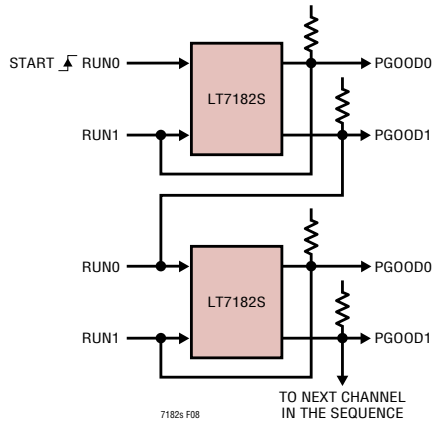


Figure 8. Event-Based Sequencing

LTpowerPlay GUI

LTpowerPlay is a powerful Windows-based development environment that supports Analog Devices digital power system management products including the LT7182S. LTpowerPlay can be used to evaluate Analog Devices products by connecting to a demo board or to the user application board. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build multiple configuration files that can be saved and reloaded at a later time. LTpowerPlay provides valuable diagnostic information during system bring-up to program or adjust the power supplies or to diagnose power issues. LTpowerPlay utilizes Analog Devices's DC1613A USB-to-I^2C/SMBus/PMBus adapter to communicate with one of the many potential targets including the DC2836A demo board. In application, the 3.3V V_{CCIO} supply from the DC1613A can be connected to the $EXTV_{CC}$ pin of the LT7182S for programming without applying PV_{IN}. The LTpowerPlay software also provides an automatic update feature to keep the revision current with the latest set of device drivers and documentation. A great deal of context sensitive help is available within LTpowerPlay along with several tutorial demos. More information is available at:

https://www.analog.com/ltpowerplay

APPLICATIONS INFORMATION

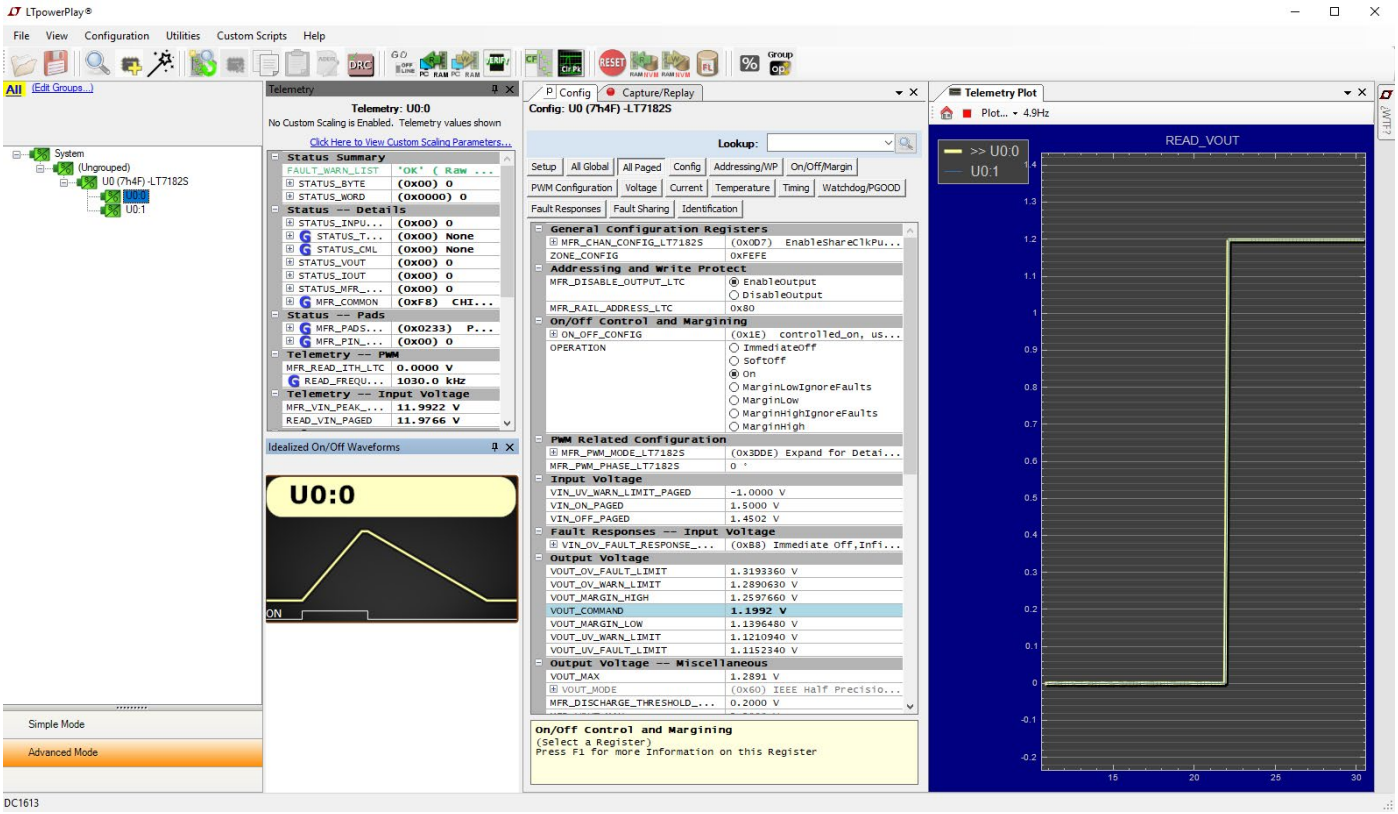


Figure 9. LTpowerPlay GUI Screen Shot

PMBUS COMMAND SUMMARY

PMBus/I²C SERIAL INTERFACE SUMMARY

This data sheet provides an overview of some key features available via the LT7182S serial interface, but it is not exhaustive. The companion document LT7182S PMBus/I²C Reference Manual provides a detailed description of the available digital functionality. Below is a table containing the supported PMBus commands.

The data format abbreviations are described at the end of this command summary. Floating point values listed in the DEFAULT VALUE column are half-precision IEEE floating point numbers.

Paged commands control and report telemetry for the selected channel. See PMBus Specification Revision 1.3.1 for more information.

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
PAGE	0x00	Provides integration with multi-page PMBUS devices.	R/W Byte	N	Reg			0x00
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N				

PMBUS COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N				
ZONE_CONFIG	0x07	Assigns current page to specified zone number for ZONE_WRITE operations.	W Word	Y	Reg		Y	0xFEFE
ZONE_ACTIVE	0x08	Selects active zone for ZONE_WRITE operations.	W Word		Reg			0xFEFE
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xD8
QUERY	0x1A	Asks if a given command is supported, and what data formats are supported.	Block R/W	N	Reg			
SMBALERT_MASK	0x1B	Masks ALERT activity.	Block R/W	Y	Reg		Y	
VOUT_MODE	0x20	Output voltage format and exponent.	R Byte	N	Reg			0x60
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	IEEE/ UL16	V	Y	0.5 0x3800
VOUT_MAX	0x24	Upper limit on the commanded output voltage.	R/W Word	Y	IEEE/ UL16	V	Y	0.537 0x384C
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point.	R/W Word	Y	IEEE/ UL16	V	Y	0.525 0x3833
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point.	R/W Word	Y	IEEE/ UL16	V	Y	0.475 0x379A
VOUT_TRANSITION_RATE	0x27	Rate the output changes when V_{OUT} commanded to a new value.	R/W Word	Y	IEEE/ L11	V/ms	Y	0.25 0x3400
FREQUENCY_SWITCH	0x33	Switching frequency of the regulator.	R/W Word	N	IEEE/ L11	kHz	Y	1000.0 0x63D0
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	Y	IEEE/ L11	V	Y	Ch. 0: 1.5 0x3E00 Ch. 1: 1.4 0x3D9A
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	Y	IEEE/ L11	V	Y	Ch. 0: 1.45 0x3DCD Ch. 1: 1.35 0x3D66
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	IEEE/ L11	V	Y	0.55 0x3866
VOUT_OV_FAULT_ RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	IEEE/ L11	V	Y	0.537 0x384C
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	IEEE/ L11	V	Y	0.467 0x3779
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	IEEE/ L11	V	Y	0.465 0x3771
VOUT_UV_FAULT_ RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x00
IOUT_OC_FAULT_ RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

PMBUS COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	IEEE/ L11	A	Y	8.0 0x4800
OT_FAULT_LIMIT	0x4F	Internal overtemperature fault limit.	R/W Word	N	IEEE/ L11	C	Y	160.0 0x5900
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an internal overtemperature fault is detected.	R/W Byte	N	Reg		Y	0xC0
OT_WARN_LIMIT	0x51	Internal overtemperature warning limit.	R/W Word	N	IEEE/ L11	C	Y	140.0 0x5860
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	Y	IEEE/ L11	V	Y	-1.0 0xBC00
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	Y	IEEE/ L11	A	Y	8.0 0x4800
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	IEEE/ L11	ms	Y	0.0 0x0000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the V_{OUT} commanded value.	R/W Word	Y	IEEE/ L11	ms	Y	1.0 0x3C00
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for V_{OUT} to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	IEEE/ L11	ms	Y	5.0 0x4500
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_ MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0x00
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	IEEE/ L11	ms	Y	0.0 0x0000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	IEEE/	ms	Y	2.0 0x4000
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below MFR_DISCHARGE_THRESHOLD.	R/W Word	Y	IEEE/ L11	ms	Y	0.0 0x0000
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	Y	Reg			
STATUS_TEMPERATURE	0x7D	Internal temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	N	Reg			
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			
READ_VIN	0x88	Measured input supply voltage.	R Word	Y	IEEE/ L11	V		
READ_IIN	0x89	Measured input supply current.	R Word	Y	IEEE/ L11	A		
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	IEEE/ UL16	V		

PMBUS COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
READ_IOUT	0x8C	Measured output current.	R Word	Y	IEEE/ L11	A		
READ_TEMPERATURE_1	0x8D	Measured internal temperature.	R Word	N	IEEE/ L11	C		
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	IEEE/ L11			
READ_POUT	0x96	Calculated output power.	R Word	Y	IEEE/ L11			
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.3.	R Byte	N	Reg			0x33
MFR_ID	0x99	The manufacturer ID in ASCII.	R Block	N				“ADI”
MFR_MODEL	0x9A	The part number in ASCII.	R Block	N				“LT7182S”
MFR_REVISION	0x9B	Part revision number.	R Block	N				
MFR_SERIAL	0x9E	Unique part serial number.	R Block	N				
IC_DEVICE_ID	0xAD	Identification of the IC in ASCII.	R Block	N				“LT7182S”
IC_DEVICE_REV	0xAE	Revision of the IC.	R Block	N				
MFR_EE_UNLOCK	0xBD	Contact factory.						
MFR_EE_ERASE	0xBE	Contact factory.						
MFR_EE_DATA	0xBF	Contact factory.						
MFR_USER_DATA_00	0xC9	EEPROM word available for user.	R/W Word	N	Reg		Y	0x0000
MFR_USER_DATA_01	0xCA	EEPROM word available for user.	R/W Word	N	Reg		Y	0x0000
MFR_USER_DATA_02	0xCB	EEPROM word available for user.	R/W Word	N	Reg		Y	0x0000
MFR_USER_DATA_03	0xCC	EEPROM word available for user.	R/W Word	N	Reg		Y	0x0000
MFR_READ_EXTVCC	0xCD	Measured $EXTV_{CC}$ voltage, when enabled.	R Word	N	IEEE/ L11	V		
MFR_READ_ITH	0xCE	Measured I_{TH} voltage, when enabled.	R Word	Y	IEEE/ L11	V		
MFR_CHAN_CONFIG_ LT7182S	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	Ch. 0: 0x00D7 Ch. 1: 0x0057
MFR_CONFIG_ALL_ LT7182S	0xD1	General configuration bits.	R/W Word	N	Reg		Y	0x0100
MFR_FAULT_PROPAGATE_ LT7182S	0xD2	Configuration that determines which faults are propagated to the $\overline{FAULT}$ pin.	R/W Word	Y	Reg		Y	0xE0D7
MFR_PWM_MODE_ LT7182S	0xD4	Configuration for the PWM engine.	R/W Word	Y	Reg		Y	0x1DD4
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the $\overline{FAULT}$ pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_ IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	IEEE/ L11	A		
MFR_ADC_CONTROL_ LT7182S	0xD8	Configures the update rate of the measurements taken by the ADC.	R/W Byte	N	Reg		Y	0x00
MFR_RETRY_DELAY	0xDB	Retry interval during fault retry mode.	R/W Word	Y	IEEE/ L11	ms	Y	10.0 0x4900

PMBUS COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LT7182S.	R/W Word	Y	IEEE/ L11	ms	Y	10.0 0x4900
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R/W Word	Y	IEEE/ UL16	V		
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R/W Word	Y	IEEE/ L11	V		
MFR_TEMPERATURE_1_ PEAK	0xDF	Maximum measured value of internal temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R/W Word	N	IEEE/ L11	C		
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				
MFR_DISCHARGE_ THRESHOLD	0xE4	Output voltage used to determine output has decayed sufficiently to re-enable the channel.	R/W Word	Y	IEEE/ L11		Y	0.2 0x3266
MFR_PADS_LT7182S	0xE5	Digital status of the I/O pads.	R Word	N	Reg			
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Word	N	Reg		Y	0x4F
MFR_SPECIAL_ID	0xE7	ID code used by manufacturer.	R Word	N	Reg			0x1C1D
MFR_FAULT_LOG_ TIMESTAMP_MSBS	0xE8	Sets the fault log timestamp upper 13 bits, clears lower 32 (read and write first)	R/W 32	N				
MFR_FAULT_LOG_ TIMESTAMP_LSBS	0xE9	Sets the fault log timestamp lower 32 bits.	R/W 32	N				
MFR_FAULT_LOG_STORE	0xEA	Force a fault log entry to be written.	Send Byte	N				
MFR_FAULT_LOG_CLEAR	0xEC	Erases all fault log entries, if any.	Send Byte	N				
MFR_FAULT_LOG	0xEE	Read contents of fault log, if any.	R Block	N	Reg			
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with EEPROM.	Send Byte	N				
MFR_CHANNEL_STATE	0xF1	Returns the state of the channel.	R Byte	Y	Reg			
MFR_PGOOD_DELAY	0xF2	Time output voltage must be between UV and OV before PGOOD transitions high.	R/W Word	Y	IEEE/ L11	ms	Y	1.0 0x3C00
MFR_NOT_PGOOD_DELAY	0xF3	Time output voltage must be below UV or above OV before PGOOD transitions low.	R/W Word	Y	IEEE/ L11	ms	Y	0.1 0x2E66
MFR_PWM_PHASE_ LT7182S	0xF5	Set PWM phase.	R/W Word	Y	IEEE/ L11	Degrees	Y	Ch. 0: 0.0 0x0000 Ch. 1: 180.0 0x59A0
MFR_SYNC_CONFIG_ LT7182S	0xF6	SYNC pin input/output configuration.	R/W Byte	N	Reg		Y	0x00
MFR_PIN_CONFIG_STATUS	0xF7	Pin configuration fault status.	R Byte	N	Reg			
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80
MFR_DISABLE_OUTPUT	0xFB	Disables regulator outputs until reset.	R/W Byte	N	Reg			0x00
MFR_EE_USER_WP	0xFC	Disables commands that write user NVM.	R/W Byte	N	Reg		Y	0x00
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				

PMBUS COMMAND SUMMARY

Abbreviations of Supported Data Formats

	PMBus			
	TERMINOLOGY	**SPECIFICATION REFERENCE**	**DEFINITION**	**EXAMPLE**
L11	Linear11	Rev 1.3.1 Part II 7.3	Floating point 16-bit data: value = Y • 2^N, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers.	b[15:0] = 0x9807 = 7 • 2^{-13} = 8.54 • 10^{-4}
UL16	ULinear16	Rev 1.3.1 Part II 8.4.1.1	Fixed point 16-bit data: value = Y • 2^{-12}, where Y = b[15:0], an unsigned integer.	b[15:0] = 0x4C00 = 19456 • 2^{-12} = 4.75
Reg			Per-bit meaning defined in command description in the LT7182S PMBus/I^{2}C Reference Manual	PMBus STATUS_BYTE command.
IEEE	IEEE-754 Half Precision Floating Point	Rev 1.3.1 Part II 8.4.4	Floating point 16-bit data: for normal values, $\text{value} = (-1)^S \bullet 2^{N-15} \bullet \left(1+\frac{M}{1024}\right)$, where S = b[15], N = b[14:10], M = b[9:0].	$b[15:0] = 0x4580 = (-1)^0 \bullet 2^{17-15} \bullet \left(1+\frac{384}{1024}\right) = 5.5$

BOARD LAYOUT CONSIDERATIONS

LAYOUT CONSIDERATIONS

Note that large, switched currents flow in the LT7182S PV_{IN} and PGND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the PV_{IN} and PGND pins.

The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. SGND should be connected to PCB ground at exactly one point, directly under the LT7182S adjacent to the SGND pin.

The SW and BOOST nodes should be as small as possible.

For more detail and PCB design files refer to the Demo Board guide for the LT7182S.

THERMAL CONSIDERATIONS

Care should be taken in the layout of the PCB to ensure good heat dissipation from the LT7182S. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT7182S. Placing additional vias can reduce thermal resistance further. The maximum load current must be derated as the ambient temperature approaches the maximum junction rating.

Temperature rise of the LT7182S is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level.

The internal junction temperature of the LT7182S is reported via the READ_TEMPERATURE_1 command.

BOARD LAYOUT CONSIDERATIONS

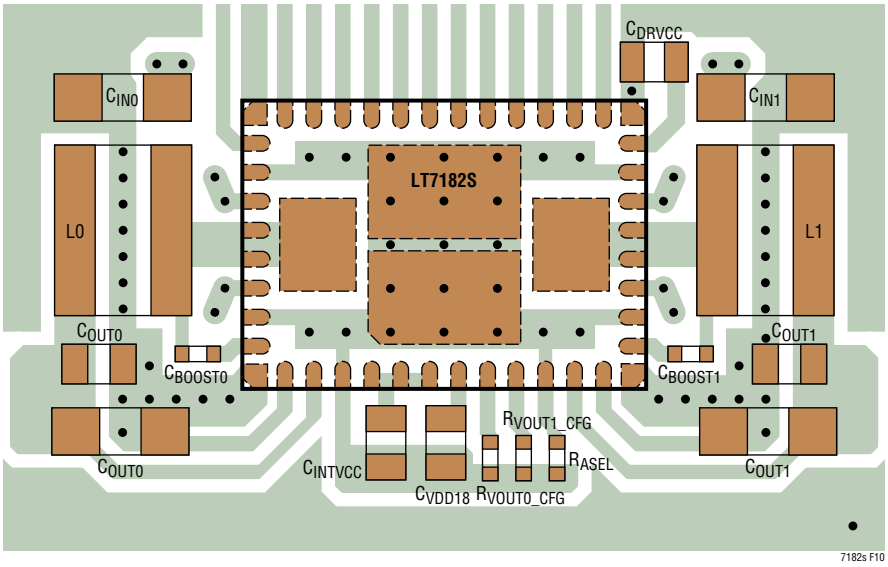
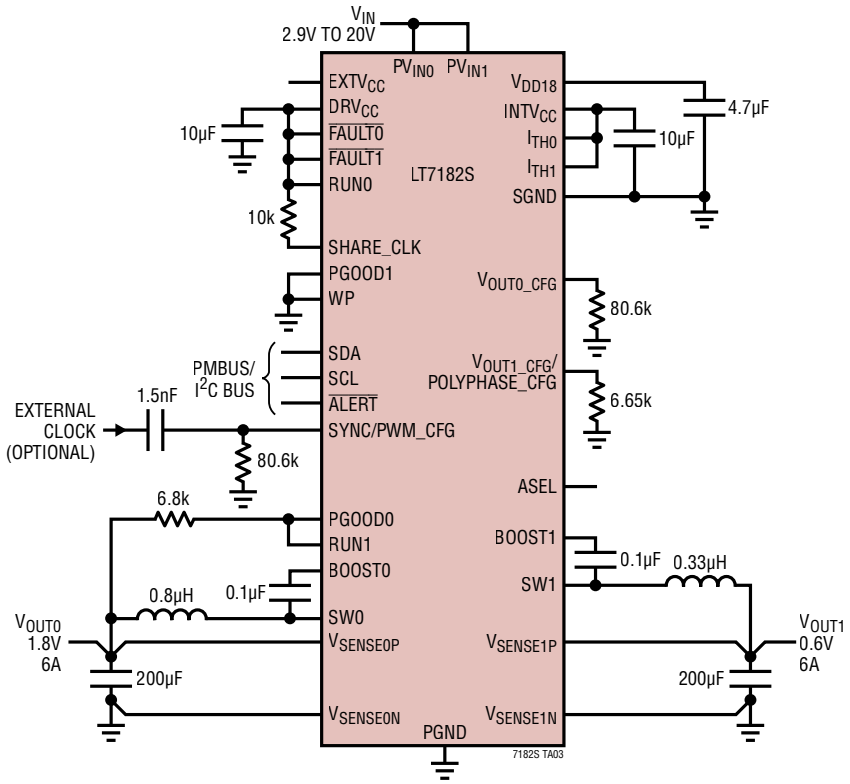


Figure 10. Recommended PCB Layout

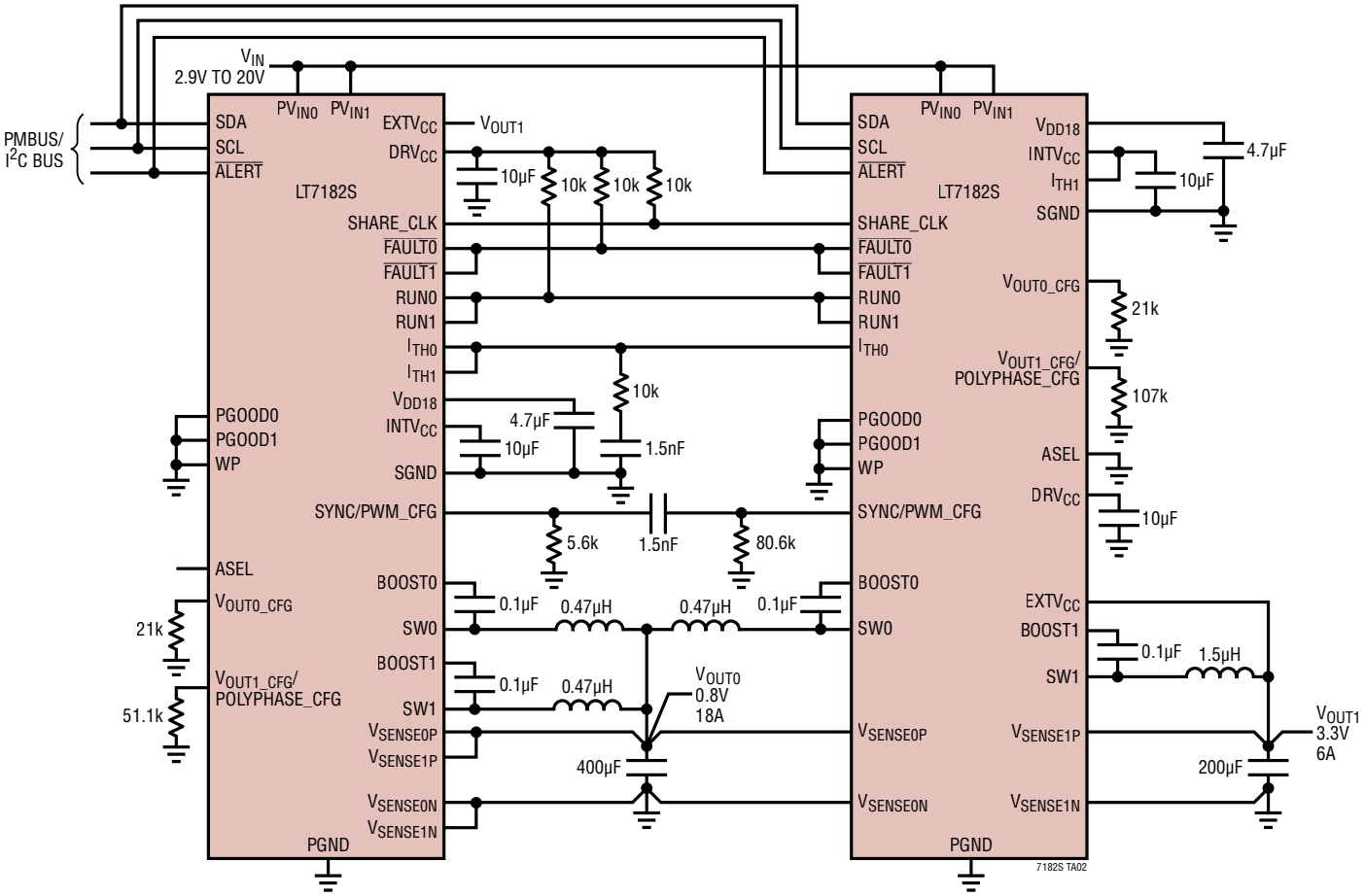
TYPICAL APPLICATIONS

1.8V, 0.6V 1MHz 6A Regulator with Pin-Strap Output Sequencing



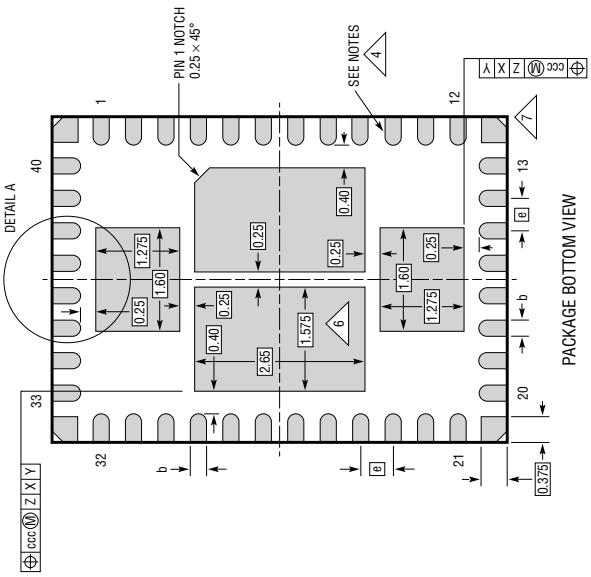
TYPICAL APPLICATIONS

Three-Phase 0.8V, 18A, 1MHz Regulator and Single-Phase 3.3V, 6A, 1MHz Regulator

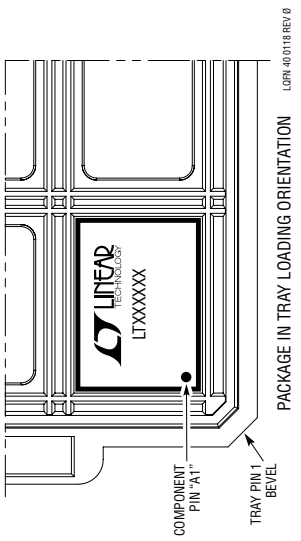


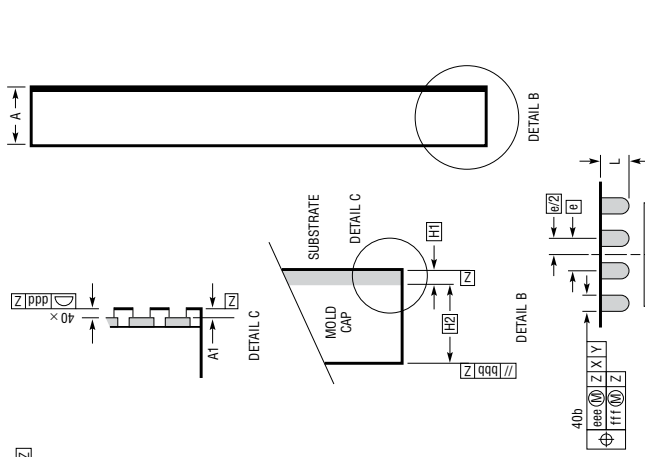
PACKAGE DESCRIPTION

LQFN Package
40-Lead (7mm × 5mm × 0.9mm)
(Reference LTC DWG # 05-08-1607 Rev Ø)

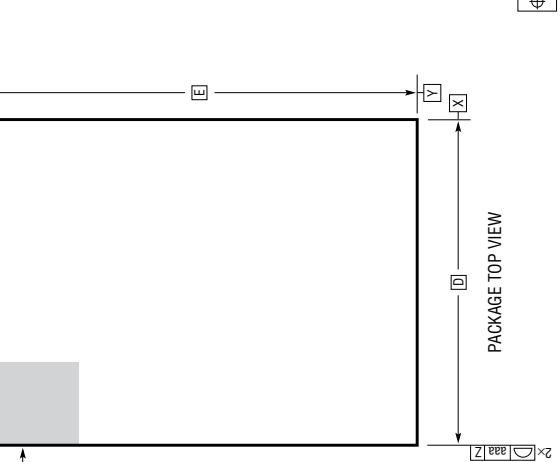


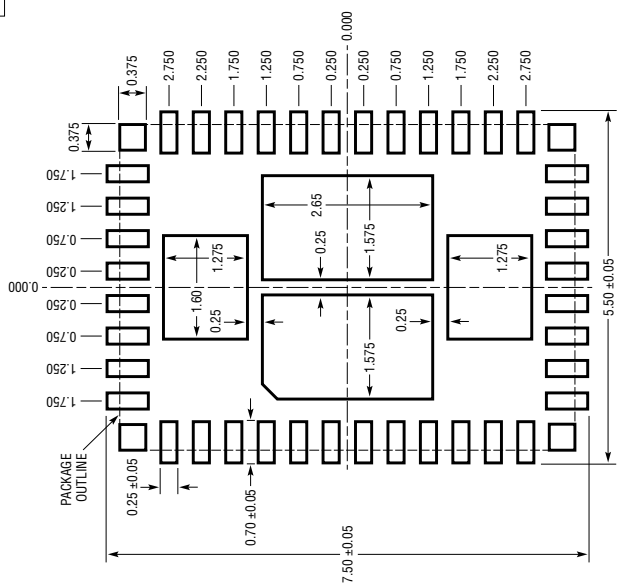
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.80	0.90	1.00	
A1	0.02	0.03	0.04	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		5.00		
E		7.00		
e		0.50		
H1		0.20		
H2		0.70		
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

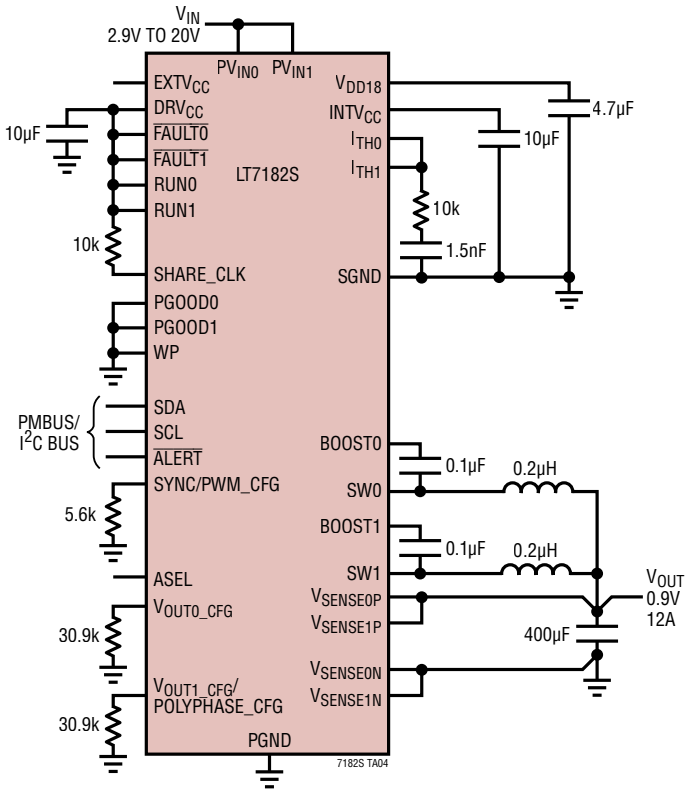




Rev. 0

TYPICAL APPLICATION

Dual-Phase 0.9V 2MHz 12A Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8652S	Dual Channel 8.5A, 18V, Synchronous Step-Down Silent Switcher 2 with 16µA Quiescent Current	V_{IN}: 3V to 18V, $V_{OUT(MIN)}$ = 0.6V, 4mm × 6mm LQFN-32 package
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2	V_{IN}: 3V to 18V, $V_{OUT(MIN)}$ = 0.6V, 4mm × 4mm LQFN-24 package
LTC7150S	20V, 20A Synchronous Step-Down Silent Switcher 2	V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, 5mm × 6mm BGA-42 package
LTC7151S	20V, 15A Synchronous Step-Down Silent Switcher 2	V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, 4mm × 5mm LQFN-28 package
LTC3636	Dual Channel 6A, 20V Monolithic Synchronous Step-Down Regulator	V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, 4mm × 5mm QFN-28 package
LT8650S	Dual Channel 4A, 42V, Synchronous Step-Down Silent Switcher 2 with 6.2µA Quiescent Current	V_{IN}: 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, 4mm × 6mm LQFN-32 package
LT8640S	42V, 6A Synchronous Step-Down Silent Switcher 2 with 2.5µA Quiescent Current	V_{IN}: 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, 4mm × 4mm LQFN-24 package
LTC3887	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	4.5V ≤ V_{IN} ≤ 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, ±0.5% V_{OUT} Accuracy, I^2C/PMBus Interface with EEPROM and 16-Bit ADC.
LTM4700	Dual 50A or Single 100A Step-Down DC/DC µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤16V; 0.5V ≤ V_{OUT} ≤ 1.8V, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface, 15mm × 22mm × 7.87mm BGA Package PMBus Interface, 16mm × 16mm × 5.01mm, BGA Package

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