40V, 2.1A Low Dropout Adjustable Linear Regulator with Monitoring and Cable Drop Compensation

FEATURES

- **Wide Input Voltage Range: 1.4V to 40V**
- **1 Resistor Sets Output Voltage: 0.4V to 32V**
- **Output Current: 2.1A**
- **±2% Tolerance Over Line, Load and Temperature**
- **Output Current Monitor: $I_{MON} = I_{OUT}/1000$**
- **Temperature Monitor with Programmable Thermal Limit**
- **Programmable Cable Drop Compensation**
- **Parallel Multiple Devices for Higher Current**
- **Dropout Voltage: 330mV**
- 1 Capacitor Soft-Starts Output and Decreases Noise
- Low Output Noise: 40μV_{RMS} (10Hz to 100kHz)
- Precision, Programmable External Current Limit
- Power Good Flag with Programmable Threshold
- Ceramic Output Capacitors: 10μF Minimum
- Quiescent Current in Shutdown: <1μA
- Reverse-Battery, -Current and -Output Protection
- Available in 5mm × 4mm 16-Lead DFN, 16-Lead TSSOP, 7-Lead DD-Pak and 7-Lead TO-220.

APPLICATIONS

- Programmable Linear Regulator
- Post Regulator for Switching Supplies
- USB Power Supplies
- High Reliability Power Supplies

DESCRIPTION

The LT®3086 is a multi-feature, low dropout, low noise 2.1A linear regulator that operates over a 1.4V to 40V input supply range. Dropout voltage at 2.1A is typically 330mV. One resistor sets output voltage from 0.4V to 32V. Output voltage tolerance is guaranteed to ±2% over line, load and temperature. The LT3086 is stable with ceramic output capacitors, requiring a minimum of 10μF.

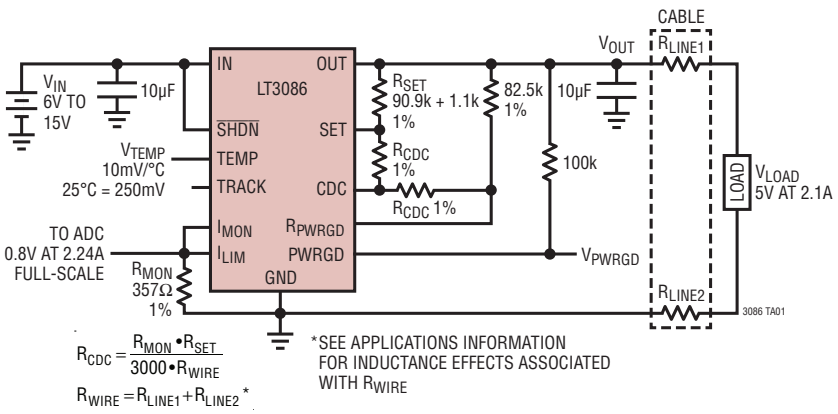
The LT3086's programmable cable drop compensation cancels output voltage errors caused by resistive connections to the load. A master/slave configuration allows paralleling of multiple devices for higher load current and heat spreading without external ballast resistor requirements.

Output current and temperature monitoring along with a power good flag provide system diagnostic and debug capability. Internal fault circuitry includes thermal shutdown and current limit with foldback. Thermal limit and current limit are also externally programmable.

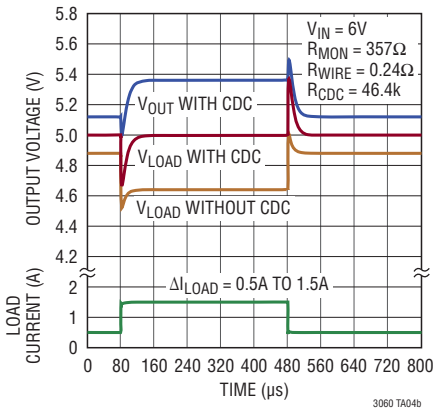
Packages include the thermally enhanced 16-lead (5mm × 4mm) DFN, 16-lead TSSOP, 7-lead DD-Pak and 7-lead TO-220.

TYPICAL APPLICATION

5V, 2.1A USB Supply with Cable Drop Compensation



Transient Response with Cable Drop Compensation (CDC)

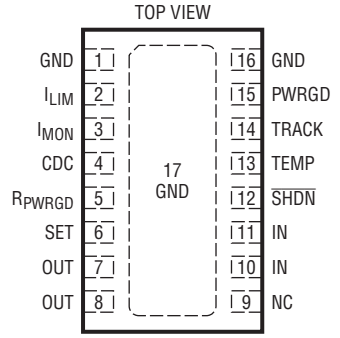


Rev. C

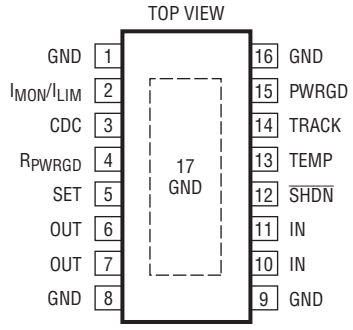
ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage .....±45V
OUT Pin Voltage.....±36V
Input-to-Output Differential Voltage (Note 2) .....±45V
SET Pin Voltage .....–0.3, 36V
$\overline{SHDN}$ Pin Voltage .....±45V
CDC Pin (Internally Clamped, Current into Pin).....<8mA
I_{MON} Pin Voltage .....–0.3, 7V
I_{LIM} Pin Voltage.....–0.3, 2V
TRACK Pin Voltage .... –0.3, Internally Clamped at 1.25V
TEMP Pin Voltage 0V, 5V
PWRGD Pin Voltage.....–0.3, 36V
R_{PWRGD} Pin Voltage.....–0.3, 36V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature (Notes 3, 5, 12)
E-Grade, I-Grade.....–40°C to 125°C
MP-Grade .....–55°C to 125°C
H-Grade .....–40°C to 150°C
Storage Temperature Range .....–65 to 150°C
Lead Temperature (Soldering, 10 sec)
(TSSOP, DD-Pak, TO-220 Only) .....300°C

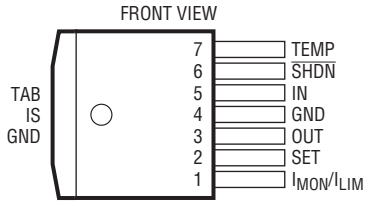
PIN CONFIGURATION



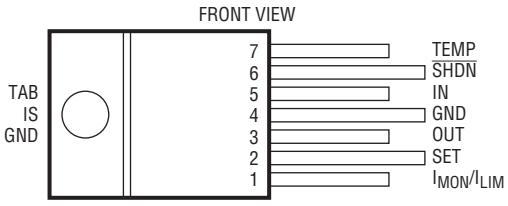
DHD PACKAGE
16-LEAD (5mm × 4mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 25°C/W TO 33°C/W*, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 25°C/W TO 33°C/W*, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



R PACKAGE
7-LEAD PLASTIC DD
T_{JMAX} = 125°C, θ_{JA} = 15°C/W TO 19°C/W*, θ_{JC} = 3°C/W



T7 PACKAGE
7-LEAD PLASTIC TO-220
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W

*See Applications Information section.

ORDER INFORMATION

http://www.analog.com/product/LT3086#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3086EDHD#PBF	LT3086EDHD#TRPBF	3086	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LT3086IDHD#PBF	LT3086IDHD#TRPBF	3086	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LT3086EFE#PBF	LT3086EFE#TRPBF	3086FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3086IFE#PBF	LT3086IFE#TRPBF	3086FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3086MPFE#PBF	LT3086MPFE#TRPBF	3086FE	16-Lead Plastic TSSOP	–55°C to 125°C
LT3086HFE#PBF	LT3086HFE#TRPBF	3086FE	16-Lead Plastic TSSOP	–40°C to 150°C
LT3086ER#PBF	LT3086ER#TRPBF	LT3086R	7-Lead Plastic DD-Pak	–40°C to 125°C
LT3086IR#PBF	LT3086IR#TRPBF	LT3086R	7-Lead Plastic DD-Pak	–40°C to 125°C
LT3086MPR#PBF	LT3086MPR#TRPBF	LT3086R	7-Lead Plastic DD-Pak	–55°C to 125°C
LT3086ET7#PBF	N/A	LT3086T7	7-Lead Plastic TO-220	–40°C to 125°C
LT3086IT7#PBF	N/A	LT3086T7	7-Lead Plastic TO-220	–40°C to 125°C
LT3086MPT7#PBF	N/A	LT3086T7	7-Lead Plastic TO-220	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.adi.com/leadfree/

For more information on tape and reel specifications, go to: http://www.adi.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Note 4)		I_{LOAD} = 2.1A, ΔV_{OUT} = –1%	●		1.4	1.55	V
Reference Voltage (Notes 3, 5)	V_{SET}	V_{IN} = 1.55V, I_{LOAD} = 1mA		396	400	404	mV
		1.55V < V_{IN} < 40V, 1mA < I_{LOAD} < 2.1A (T_J < 125°C)	●	392	400	408	mV
		1.55V < V_{IN} < 40V, 1mA < I_{LOAD} < 2.1A (H-Grade, T_J > 125°C)		388	400	408	mV
Reference Current	I_{SET}	V_{IN} = 1.55V, I_{LOAD} = 1mA		49.5	50	50.5	µA
		1.55V < V_{IN} < 40V, 1mA < I_{LOAD} < 2.1A	●	49	50	51	µA
Line Regulation	V_{SET}	V_{IN} = 1.55V to 40V, I_{LOAD} = 1mA (T_J < 125°C)	●		0.1	0.8	mV
	V_{SET}	V_{IN} = 1.55V to 40V, I_{LOAD} = 1mA (H-Grade, T_J > 125°C)				1	mV
	I_{SET}	V_{IN} = 1.55V to 40V, I_{LOAD} = 1mA	●	–0.12	–0.03		µA
Load Regulation (Notes 6, 7)	V_{SET}	I_{LOAD} = 1mA to 2.1A, V_{IN} = V_{OUT} + 0.55V (T_J < 125°C)	●		0.25	1	mV
	V_{SET}	I_{LOAD} = 1mA to 2.1A, V_{IN} = V_{OUT} + 0.55V (H-Grade, T_J > 125°C)		–8		1	mV
	I_{SET}	I_{LOAD} = 1mA to 2.1A, V_{IN} = V_{OUT} + 0.55V (T_J < 125°C)	●		0.02	0.08	µA
	I_{SET}	I_{LOAD} = 1mA to 2.1A, V_{IN} = V_{OUT} + 0.55V (H-Grade, T_J > 125°C)		–0.16		0.08	µA
Minimum Load Current (Note 16)			●			1	mA
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$, (Notes 7, 8)		I_{LOAD} = 1mA			10	65	mV
			●			100	mV
		I_{LOAD} = 100mA			100	135	mV
			●			160	mV
		I_{LOAD} = 500mA			150	195	mV
			●			235	mV
		I_{LOAD} = 1.5A			260	335	mV
			●			425	mV
		I_{LOAD} = 2.1A			330	415	mV
			●			540	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ + 0.55V, (Notes 7, 9)	I_{LOAD} = 0µA I_{LOAD} = 1mA I_{LOAD} = 100mA I_{LOAD} = 500mA I_{LOAD} = 1.5A I_{LOAD} = 2.1A	● ● ● ● ● ●		1.2 1.3 1.8 4.5 23 44	2.4 2.6 3.6 9 46 88	mA mA mA mA mA mA
Quiescent Current in Shutdown	V_{IN} = 40V, $V_{\overline{SHDN}}$ = 0V			0.1	1	µA
Output Voltage Noise	C_{SET} = 0.01µF , C_{OUT} = 10µF, I_{LOAD} = 2.1A V_{OUT} = 5V, BW = 10Hz to 100kHz			40		μV_{RMS}
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	1.12 0.85	1.22 1.03	1.32	V V
$\overline{SHDN}$ Pin Current (Note 10) 1.55V < V_{IN} < 40V	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 40V	● ●		 15	1 35	µA µA
TEMP Voltage (Note 13)	T_J = 25°C T_J = 125°C			0.25 1.25		V V
TEMP Error (Note 13)	0°C < T_J < 125°C, I_{TEMP} = 0 0°C < T_J < 125°C, I_{TEMP} = 0µA to 80µA		–0.09 –0.1		0.09	V V
I_{TEMP} Thermal Limit Current Threshold	25°C < T_J < 125°C		95	100	105	µA
I_{MON} Output Current $V_{IN} = V_{OUT(NOMINAL)}$ + 0.55V (Note 15)	I_{LOAD} = 20mA, R_{MON} = 1kΩ I_{LOAD} = 500mA, R_{MON} = 330Ω I_{LOAD} = 1A, R_{MON} = 330Ω I_{LOAD} = 1.5A, R_{MON} = 330Ω I_{LOAD} = 2.1A, R_{MON} = 330Ω	● ● ● ● ●	5 440 0.95 1.43 2.02	20 500 1.00 1.50 2.10	75 560 1.05 1.57 2.18	µA µA mA mA mA
Output Current Sharing Error (Note 14)	R_{MON} = 330Ω, $I_{OUT(MASTER)}$ = 2.1A		–10	0	10	%
TRACK Pin Pull-Up Current	V_{TRACK} = 750mV	●	7	15	25	µA
R_{PWRGD} Reference Voltage	1.55V < V_{IN} < 40V	●	390	400	410	mV
R_{PWRGD} Reference Current	1.55V < V_{IN} < 40V	●	48.75	50	51.25	µA
R_{PWRGD} Reference Voltage Hysteresis	1.55V < V_{IN} < 40V			2.4		mV
R_{PWRGD} Reference Current Hysteresis	1.55V < V_{IN} < 40V			300		nA
PWRGD V_{OL}	I_{PWRGD} = 200µA (Fault Condition)	●		55	200	mV
PWRGD Internal Time Delay	V_{OL} TO V_{OH} (Rising Edge)	●	8	17	25	µs
PWRGD Pin Leakage Current	V_{PWGRD} = 32V, V_{RPWGRD} = 500mV	●			1	µA
CDC Reference Voltage	1.55V < V_{IN} < 40V, I_{MON} = 0V	●	390	400	410	mV
CDC/V_{IMON} Voltage Gain	1.55V < V_{IN} < 40V, 0 < I_{CDC} < 20µA, V_{IMON} = 800mV to 0	●	0.320	0.333	0.343	V/V
Ripple Rejection	V_{IN} = 1.9V (AVG), V_{RIPPLE} = 0.5V_{P-P}, V_{OUT} = 1V f_{RIPPLE} = 120Hz, I_{LOAD} = 2.1A		65	80		dB
Internal Current Limit	V_{IN} = 1.55V $V_{IN} = V_{OUT(NOMINAL)}$ + 0.55V (Notes 7, 12), ΔV_{OUT} = –5%	● ●	2.2 2.2	2.4	2.9	A A
I_{LIM} Threshold Voltage	1.55V < V_{IN} < 40V	●	775	800	825	mV
Input Reverse-Leakage Current	V_{IN} = –40V, V_{OUT} = 0	●			2	mA
Reverse-Output Current (Note 11)	V_{OUT} = 32V, V_{IN} = 0, $V_{\overline{SHDN}}$ = 0			1	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 45V, the OUT pin may not be pulled below 0V. The total IN to OUT differential voltage must not exceed ±45V.

Note 3: The LT3086 is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3086E is 100% production tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3086I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3086MP is 100% tested over the –55°C to 125°C operating junction temperature range. The LT3086H is 100% tested

ELECTRICAL CHARACTERISTICS

at the 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The LT3086 is tested and specified for these conditions with the SET pin connected to the OUT pin, V_{OUT} = 0.4V.

Note 5: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at large input-to-output voltage differentials. Limit the input-to-output voltage differential if operating at maximum output current. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit vs $V_{IN} – V_{OUT}$ in the Typical Performance Characteristics section.

Note 6: Load regulation is Kelvin-sensed at the package.

Note 7: To satisfy minimum input voltage requirements, the LT3086 is tested and specified for these conditions with a 32k resistor between OUT and SET for a 2V output voltage.

Note 8: Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: $(V_{IN} – V_{DROPOUT})$. For low output voltages and certain load conditions, minimum input voltage requirements limit dropout voltage. See the Minimum Input Voltage curve in the Typical Performance Characteristics section.

Note 9: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ + 0.55V and PWRGD pin floating. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 10: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 11: Reverse-output current is tested with the IN pin grounded and the OUT pin forced to a voltage. The current flows into the OUT pin and out of the GND pin.

Note 12: The IC includes overtemperature protection circuitry that protects the device during momentary overload conditions. Junction temperature exceeds 125°C (LT3086E, LT3086I, LT3086MP) or 150°C (LT3086H) when the overtemperature circuitry is active unless thermal limit is externally set by loading the TEMP pin. Continuous operation above the specified maximum junction temperature may impair device reliability.

Note 13: The TEMP output voltage represents the average die temperature next to the power transistor while the center of the transistor can be significantly hotter during high power conditions. Due to power dissipation and temperature gradients across the die, the TEMP output voltage measurement does not guarantee that absolute maximum junction temperature is not exceeded.

Note 14: Output current sharing error is the difference in output currents of a slave relative to its master when two LT3086 regulators are paralleled. The device is tested as a slave with V_{TRACK} = 0.693V, R_{MON} = 330Ω and V_{SET} = 0.4V, conditions when an ideal master is outputting 2.1A. The specification limits account for the slave output tracking error from 2.1A and the worst-case error that can be contributed by a master: the maximum deviation of V_{SET} from 0.4V and I_{MON} from 2.1mA.

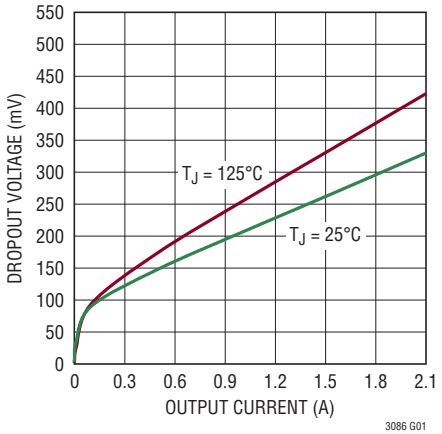
Note 15: The LT3086 is tested and specified for these conditions with the I_{MON} and I_{LIM} pins tied together.

Note 16: The LT3086 requires a minimum load current to ensure proper regulation and stability.

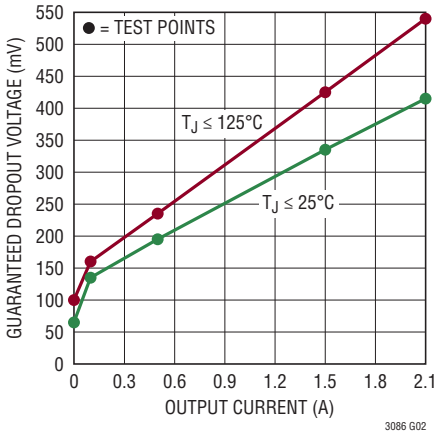
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

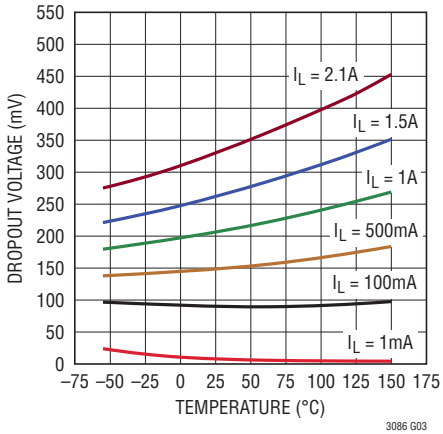
Typical Dropout Voltage



Guaranteed Dropout Voltage

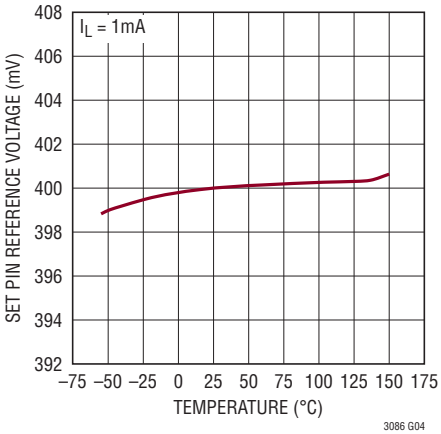


Dropout Voltage

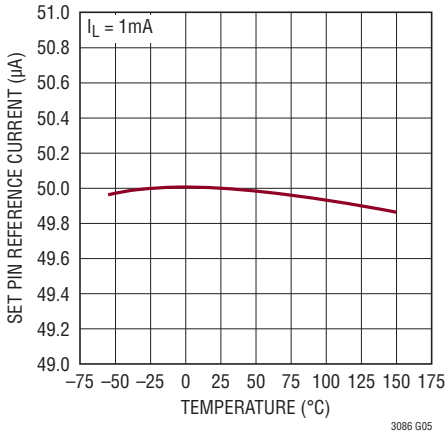


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

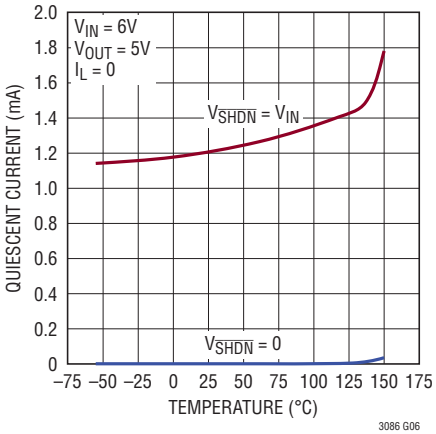
SET Pin Reference Voltage



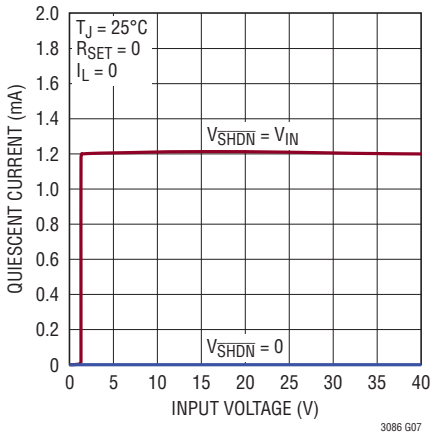
SET Pin Reference Current



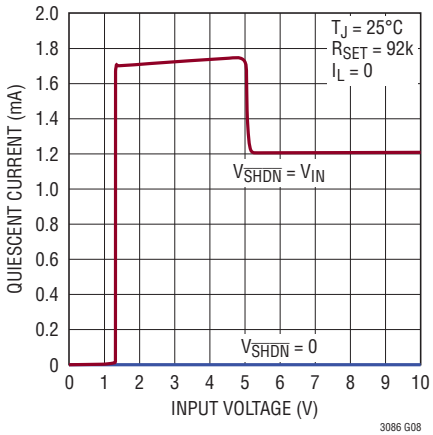
Quiescent Current



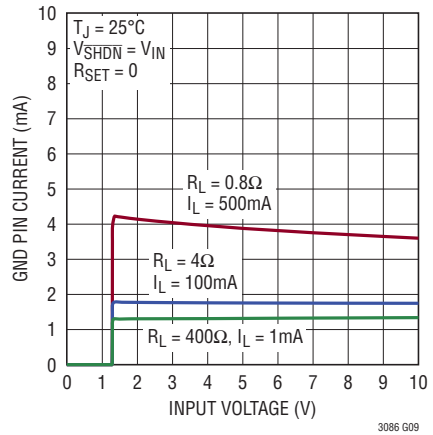
Quiescent Current, V_{OUT} = 0.4V



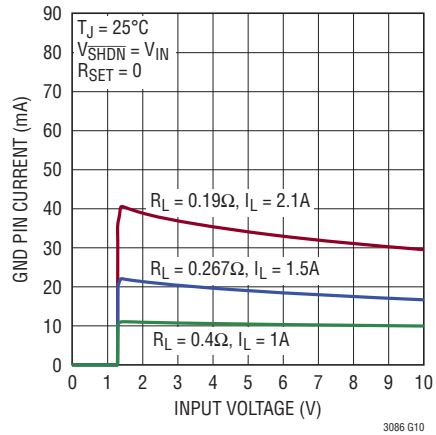
Quiescent Current, V_{OUT} = 5V



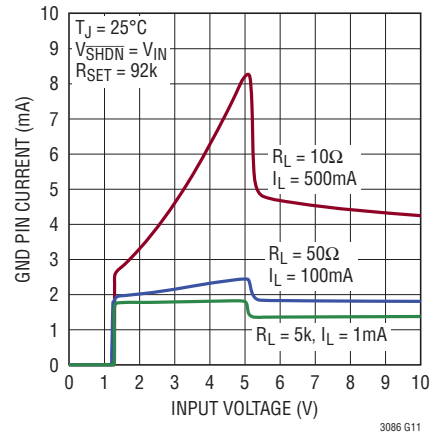
GND Pin Current, V_{OUT} = 0.4V (Light Load)



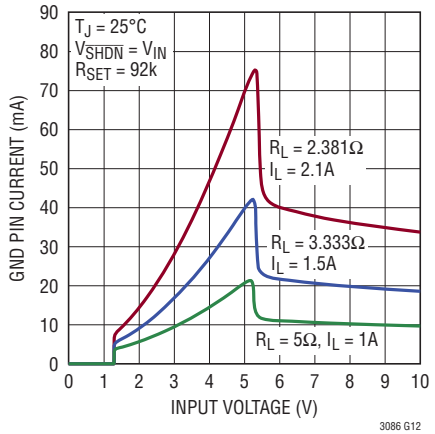
GND Pin Current, V_{OUT} = 0.4V (Heavy Load)



GND Pin Current, V_{OUT} = 5V (Light Load)

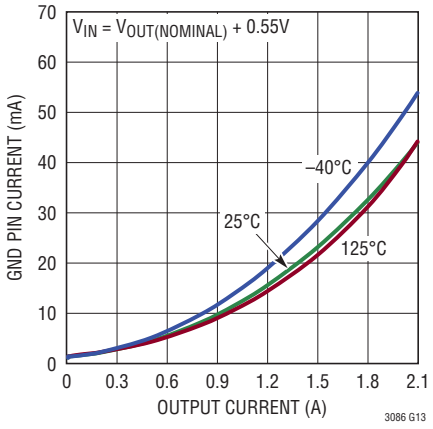


GND Pin Current, V_{OUT} = 5V (Heavy Load)

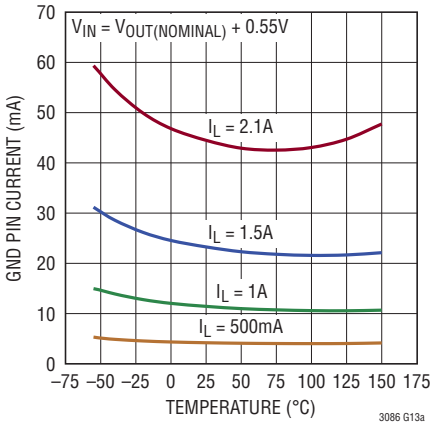


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

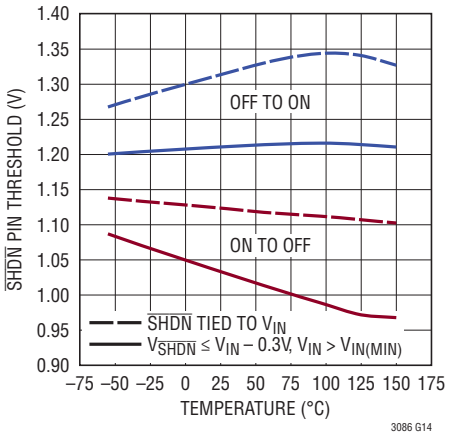
GND Pin Current vs I_{LOAD}



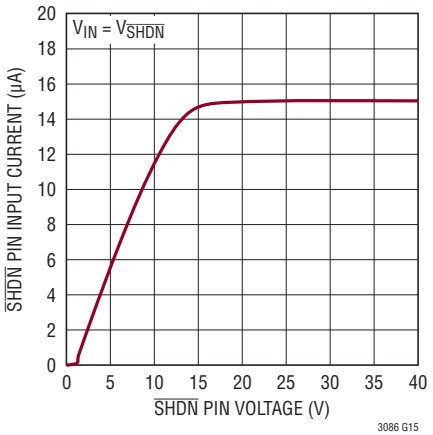
GND Pin Current vs Temperature



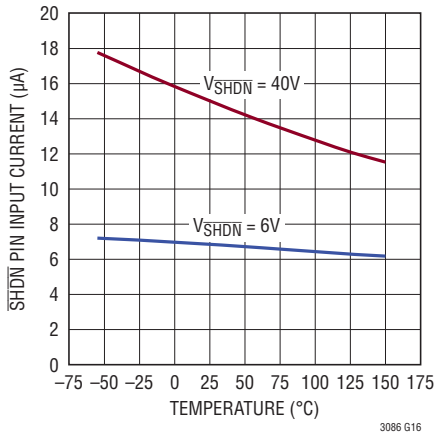
$\overline{SHDN}$ Pin Threshold



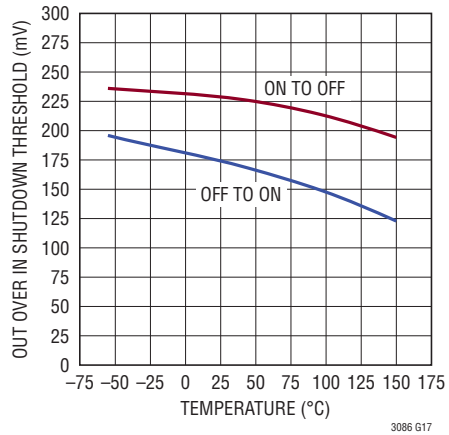
$\overline{SHDN}$ Pin Input Current



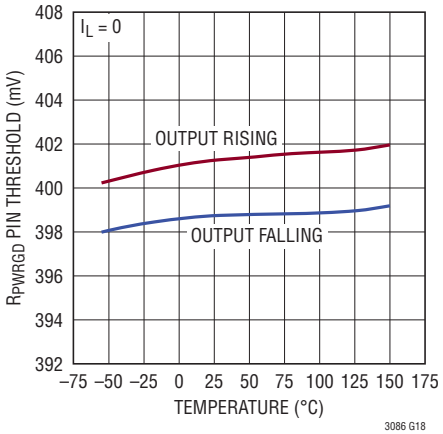
$\overline{SHDN}$ Pin Input Current



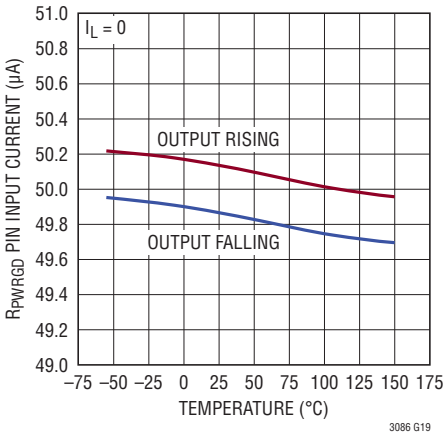
OUT Over IN Shutdown Threshold



R_{PWRGD} Pin Threshold

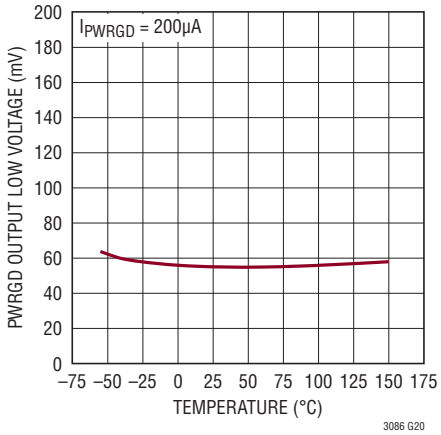


R_{PWRGD} Pin Input Current

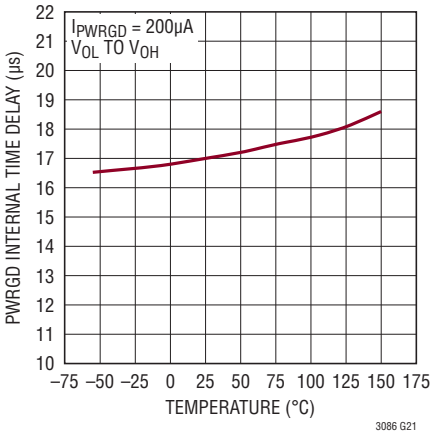


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

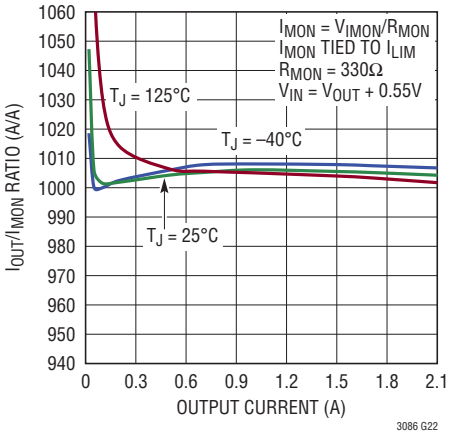
PWRGD Output Low Voltage



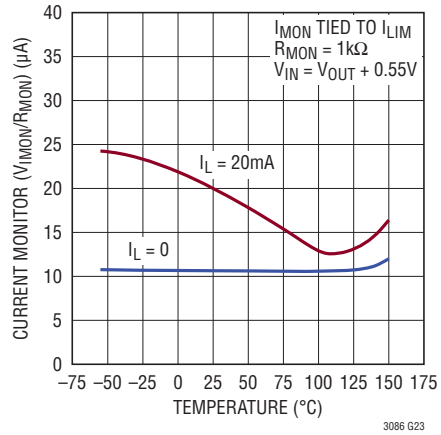
PWRGD Internal Time Delay



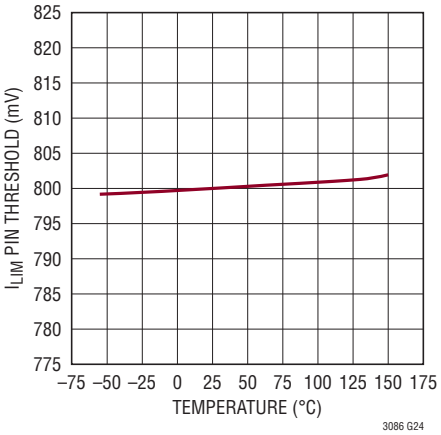
I_{OUT}/I_{MON} Ratio



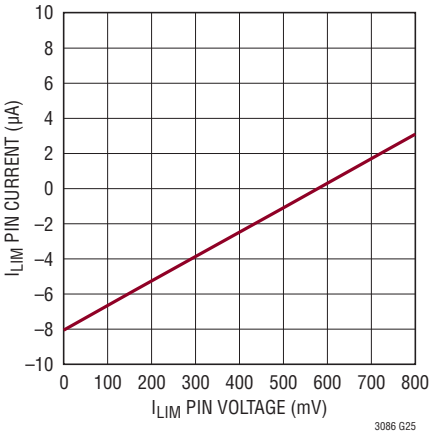
Current Monitor at Light Load



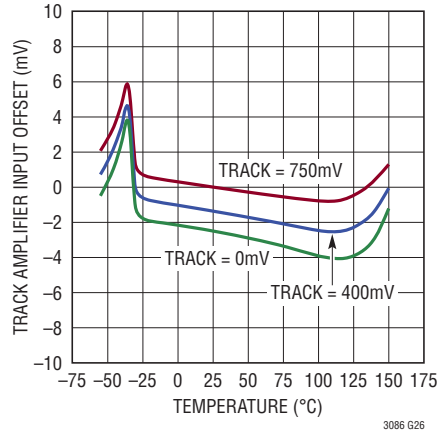
I_{LIM} Pin Threshold Voltage



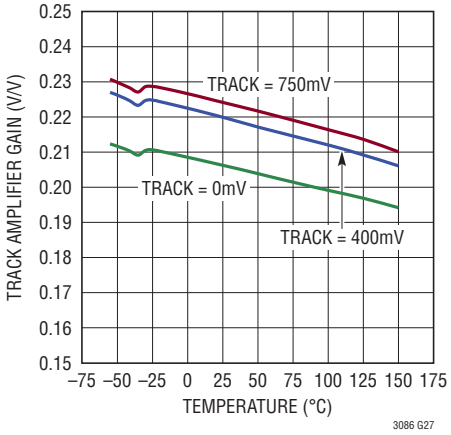
I_{LIM} Pin Input Current



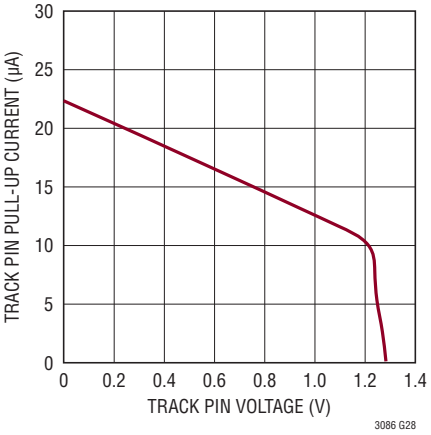
TRACK Amplifier Input Offset



TRACK Amplifier Gain

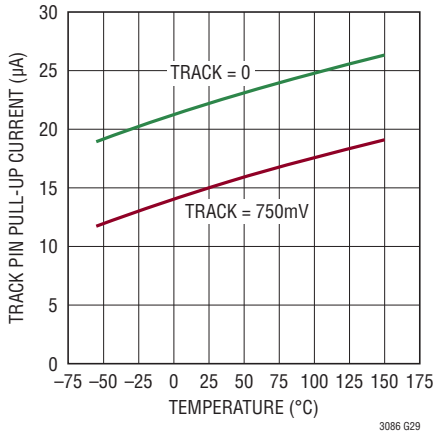


TRACK Pin Pull-Up Current

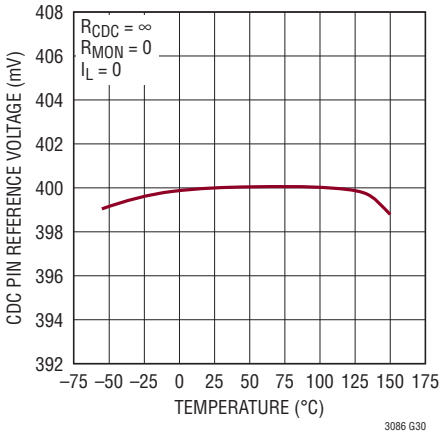


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

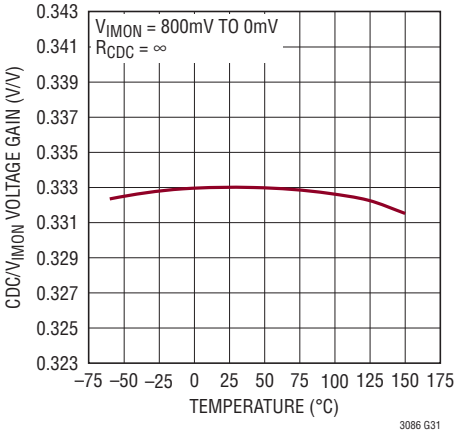
TRACK Pin Pull-Up Current



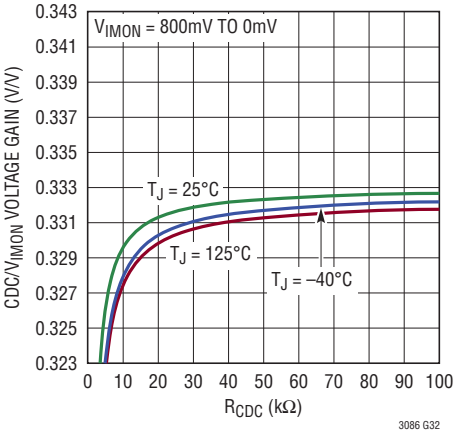
CDC Pin Reference Voltage



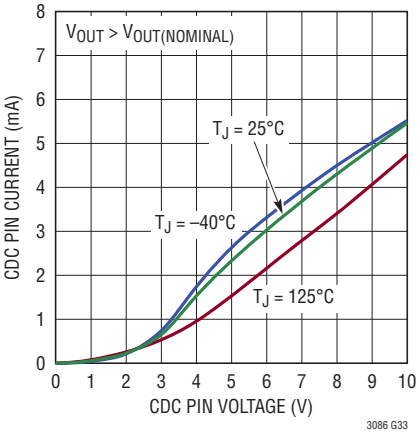
CDC Amplifier Gain



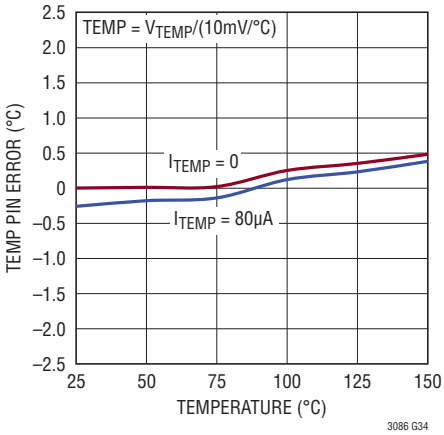
CDC Amplifier Gain



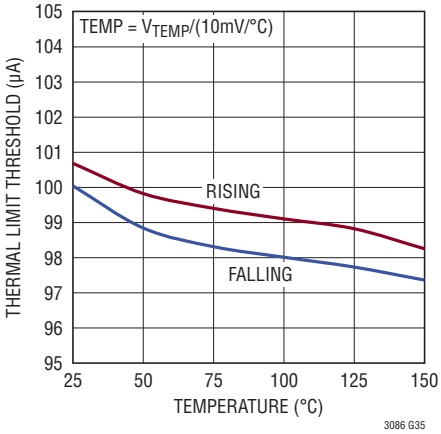
CDC Pin Internal Clamp Fault Current



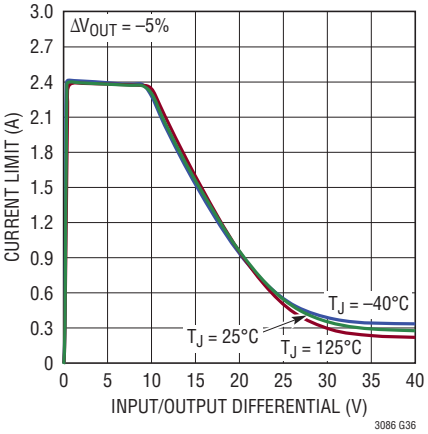
TEMP Pin Error



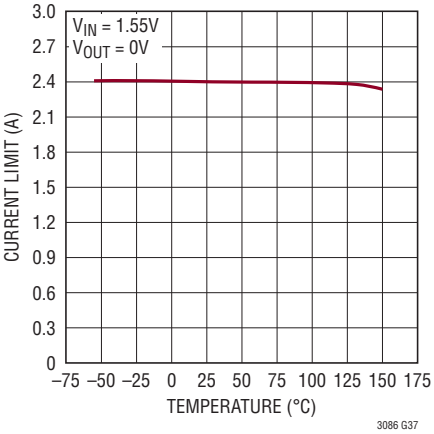
I_{TEMP} Thermal Limit Threshold



Internal Current Limit vs $V_{IN} - V_{OUT}$

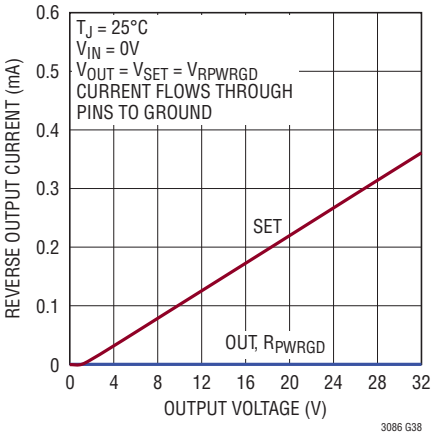


Internal Current Limit vs Temperature

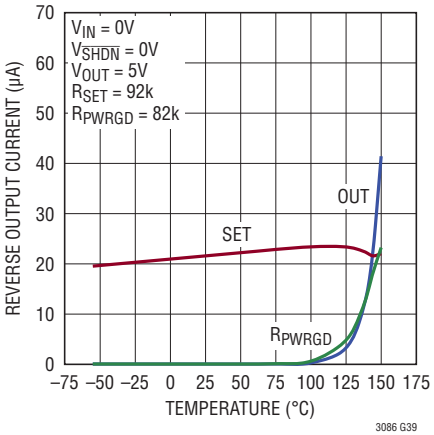


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

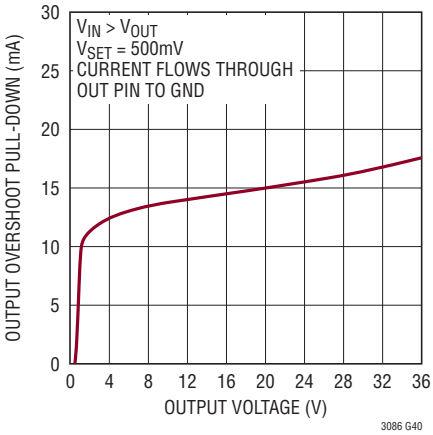
Reverse-Output Current



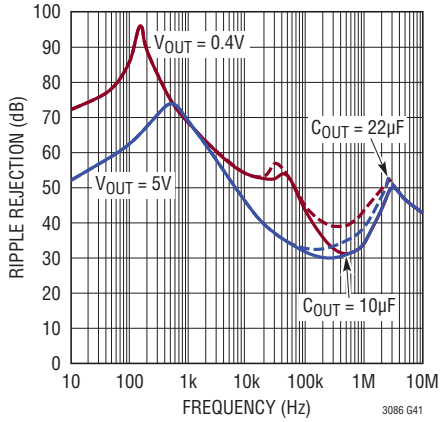
Reverse-Output Current



Overshoot Pull-Down Current

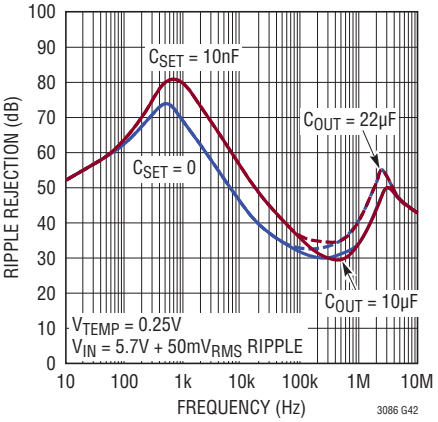


Input Ripple Rejection

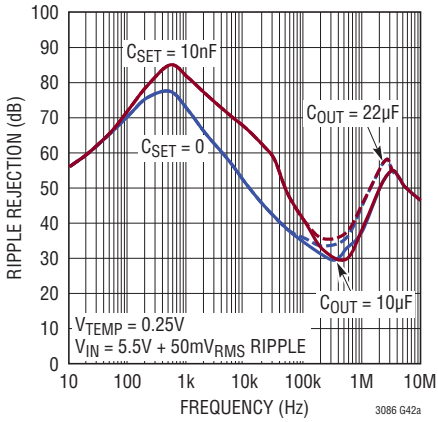


I_L = 2.1A, C_{SET} = 0, V_{TEMP} = 0.25V,
V_{IN} = 1.6V + 50mV_{RMS} RIPPLE (FOR V_{OUT} = 0.4V)
V_{IN} = 5.7V + 50mV_{RMS} RIPPLE (FOR V_{OUT} = 5V)

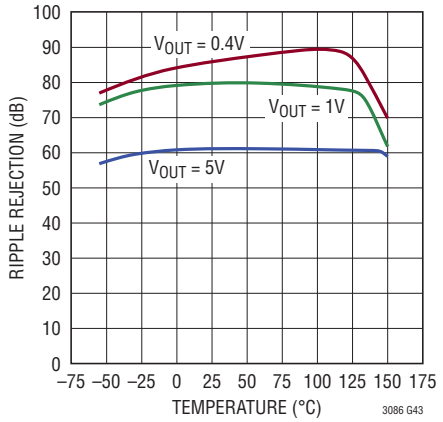
5V, 2.1A Input Ripple Rejection



5V, 1A Input Ripple Rejection

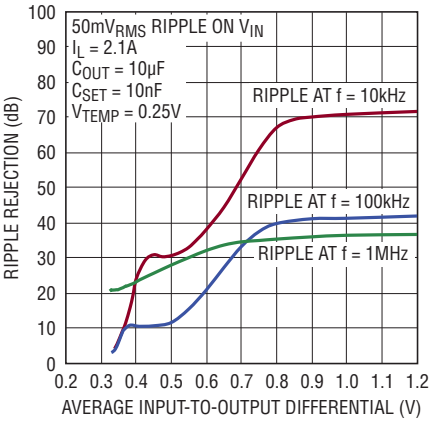


Ripple Rejection vs Temperature

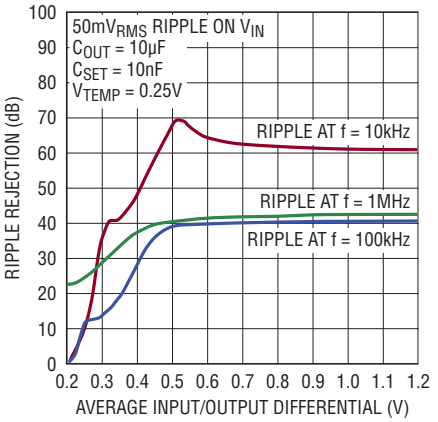


I_L = 2.1A, C_{SET} = 0, V_{TEMP} = 0.25V,
V_{IN} = 1.9V + 0.5V_{P-P} RIPPLE (FOR V_{OUT} = 0.4V, 1V)
V_{IN} = 5.9V + 0.5V_{P-P} RIPPLE (FOR V_{OUT} = 5V)
RIPPLE AT f = 120Hz

5V, 2.1A Ripple Rejection vs $V_{IN} - V_{OUT}$

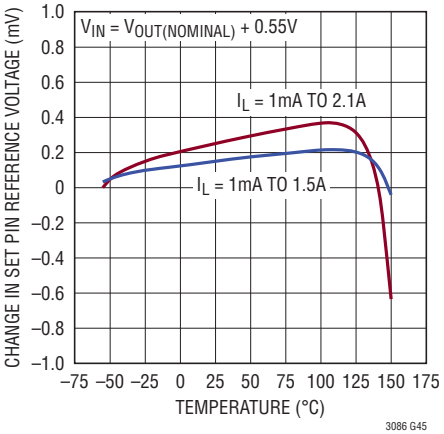


5V, 1A Ripple Rejection vs $V_{IN} - V_{OUT}$

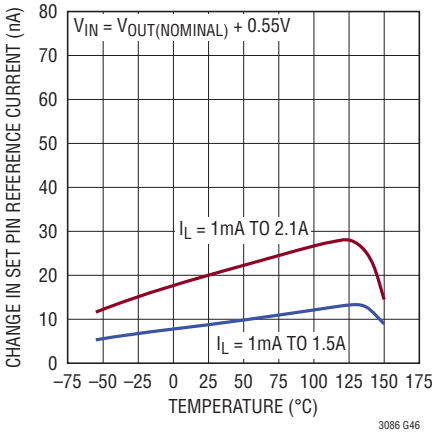


TYPICAL PERFORMANCE CHARACTERISTICS

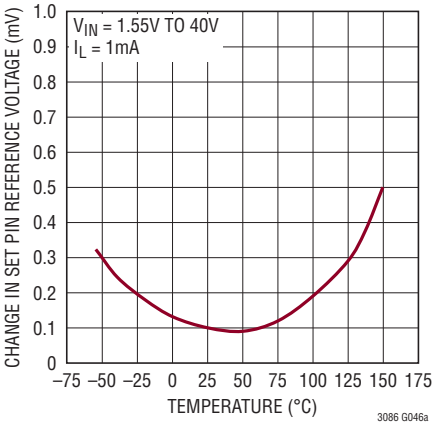
Reference Voltage Load Regulation



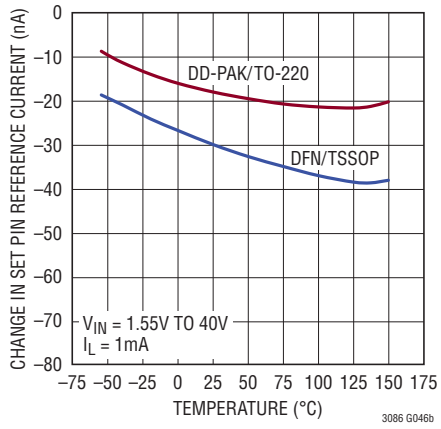
Reference Current Load Regulation



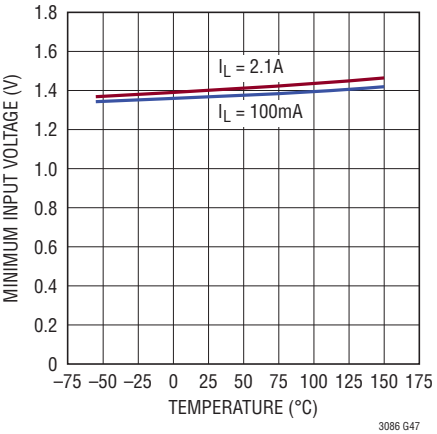
Reference Voltage Line Regulation



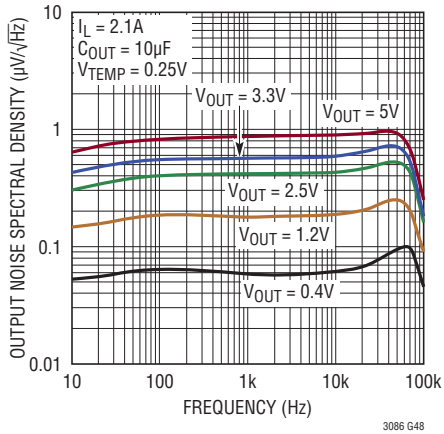
Reference Current Line Regulation



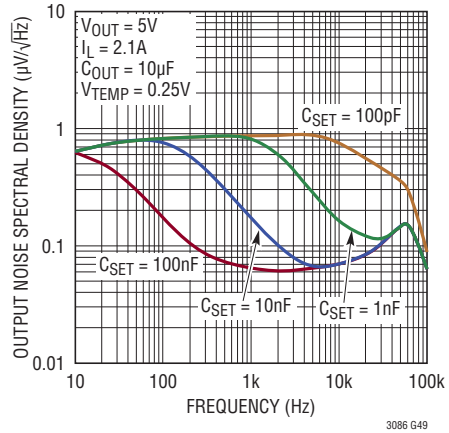
Minimum Input Voltage



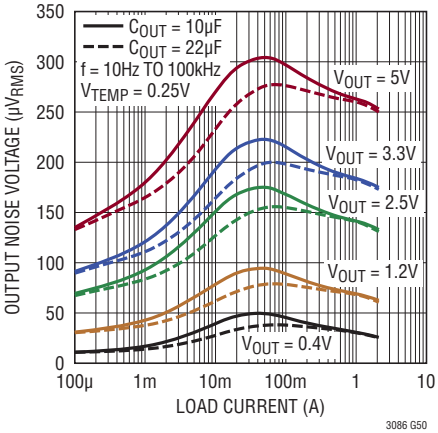
Output Noise Spectral Density, C_{SET} = 0



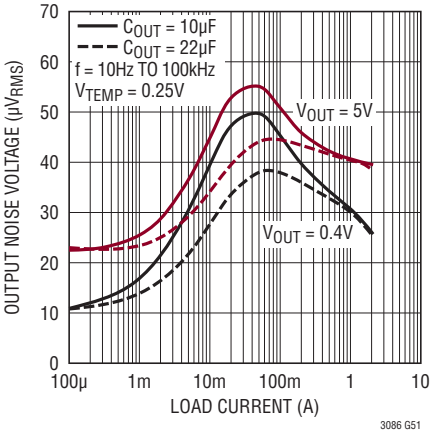
Output Noise Spectral Density vs C_{SET}



RMS Output Noise vs Load Current, C_{SET} = 0

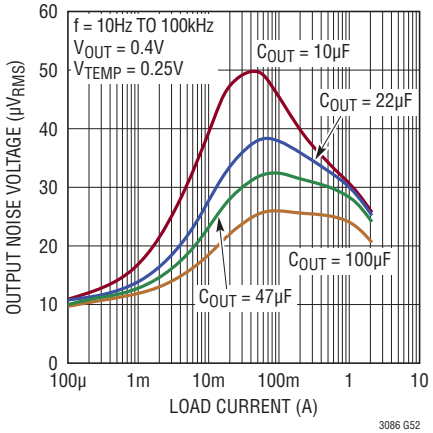


RMS Output Noise vs Load Current, C_{SET} = 10nF

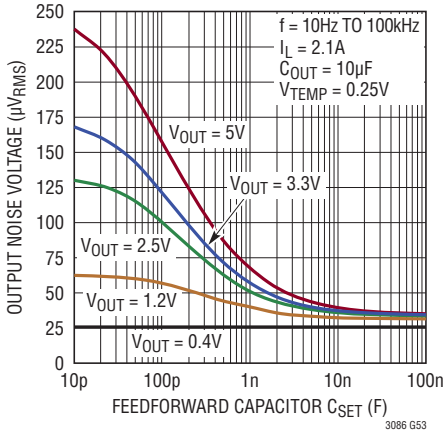


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

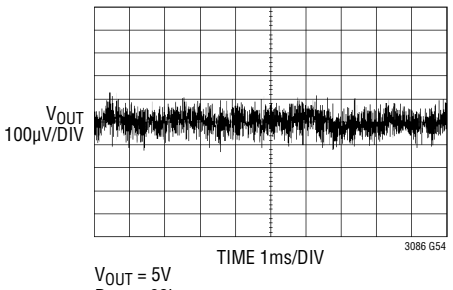
RMS Output Noise vs Load Current



RMS Output Noise vs Feedforward Capacitor (C_{SET})

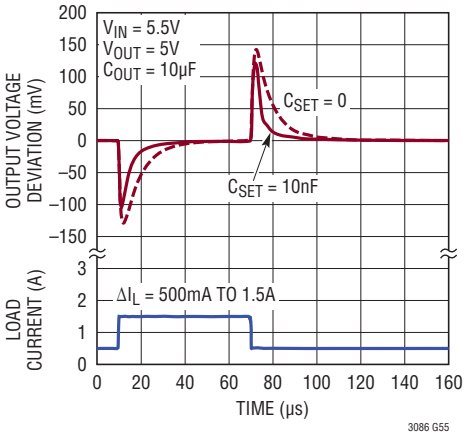


Output Voltage Noise

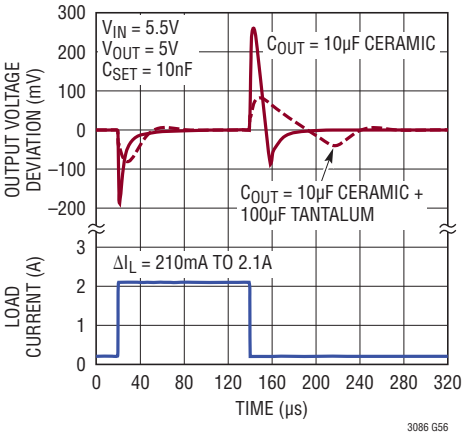


VOUT = 5V
RSET = 92k
CSET = 10nF
COUT = 10µF
IL = 2.1A
f = 10Hz TO 100kHz

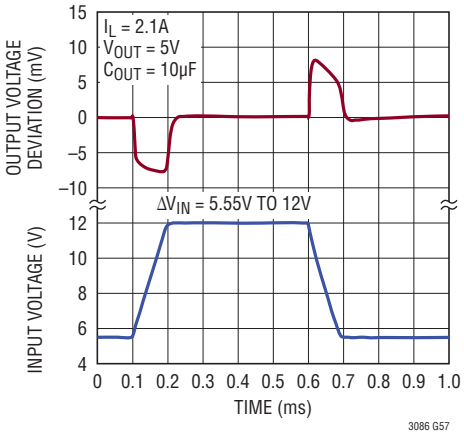
Load Transient Response



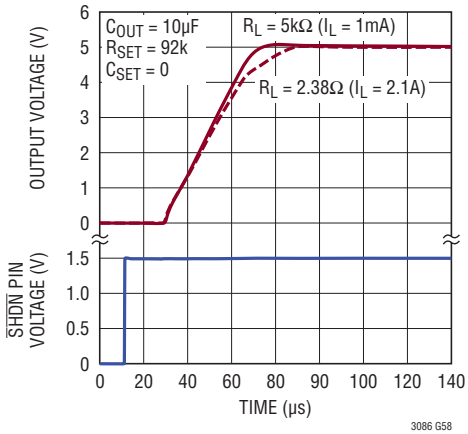
Load Transient Response



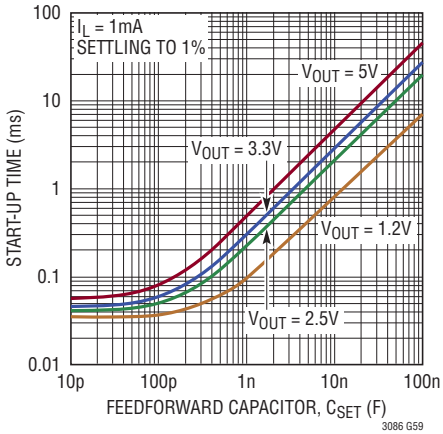
Line Transient Response



Start-Up Response



Start-Up Time vs C_{SET}



Rev. C

PIN FUNCTIONS (DFN/TSSOP/DD-Pak/TO-220)

GND (Pins 1, 16, Exposed Pad Pin 17/Pins 1, 8, 9, 16, Exposed Pad Pin 17/Pin 4/Pin 4): Ground. The exposed pad of the DFN and TSSOP packages as well as the Tab of the DD-Pak and TO-220 packages is an electrical connection to GND. To ensure proper electrical and thermal performance, tie the exposed pad or tab directly to the remaining GND pins of the relevant package and the PCB ground. GND pin current is typically 1.2mA at zero load and increases to about 44mA at full load.

I_{LIM} (Pin 2/Pin 2/Pin 1/Pin 1): External Current Limit Programming. This pin externally programs current limit if connected to I_{MON} and a resistor to GND. Current limit activates if the voltage at I_{LIM} equals 0.8V. Current limit equals: 1000 • (0.8V/R_{MON}). An internal clamp typically limits the I_{LIM} voltage to 1V. *If external current limit is set to less than 1A, connect a series 1k-10nF network in parallel with the R_{MON} resistor for stability.* Internal current limit foldback overrides externally programmed current limit if $V_{IN} – V_{OUT}$ differential voltage is excessive. If external current limit programming is not used, then ground this pin.

I_{MON} (Pin 3/Pin 2/Pin 1/Pin 1): Output Current Monitor. This pin sources a current equal to 1/1000 of output load current. Connecting a resistor from I_{MON} to GND programs a load current dependent voltage for monitoring by an ADC. If I_{MON} connects to I_{LIM}, current limit is externally programmable.

CDC (Pin 4/Pin 3/NA/NA): Cable Drop Compensation. Connecting a single resistor (R_{CDC}) between the CDC and SET pins provides programmable cable drop compensation that cancels output voltage errors caused by resistive connections to the load. A resistor (R_{MON}) from I_{MON} to GND is also required to enable Cable Drop Compensation. Choose R_{MON} first based on required current limit.

$$R_{MON} = 0.8V \bullet 1000/I_{LIM}$$

Calculate the value of R_{CDC} with this formula:

$$R_{CDC} = (R_{MON} \bullet R_{SET})/(3000 \bullet R_{WIRE})$$

where R_{WIRE} is the total cable or wire resistance to and from the load. From a practical application standpoint, LTC recommends limiting cable drop compensation to 20% of V_{OUT} for applications needing good regulation. The limiting factor is variations in wire temperature as copper wire resistance changes about 19% for a 50°C temperature change. If output regulation requirements are loose (e.g., when using a secondary regulator), cable drop compensation of up to 50% may be used.

R_{PWRGD} (Pin 5/Pin 4/NA/NA): Power Good Threshold Voltage Programming. This pin is the input to the power good comparator. Connecting a resistor between OUT and R_{PWRGD} programs an adjustable power good threshold voltage. The threshold voltage is 0.4V on the R_{PWRGD} pin, and a 50µA current source is connected from R_{PWRGD} to GND. If the voltage at R_{PWRGD} is less than 0.4V, the PWRGD flag asserts and pulls low. If the voltage at R_{PWRGD} is greater than 0.4V, the PWRGD flag de-asserts and becomes high impedance. For most applications, PWRGD is pulled high with a pull-up resistor. Calculate the value of R_{PWRGD} with this formula:

$$R_{PWRGD} = (X \bullet V_{OUT(NOMINAL)} – 0.4V)/50\mu A$$

where X is normally in the 85% to 95% range.

A 17µs deglitching filter suppresses false tripping of the PWRGD flag at the rising edge of PWRGD with instant reset. Hysteresis at the R_{PWRGD} pin is typically 0.6% on the 0.4V threshold and the 50µA current source.

SET (Pin 6/Pin 5/Pin 2/Pin 2): Output Voltage Programming. This pin is the error amplifier's inverting terminal. It regulates to 0.4V and a 50µA current source is connected from SET to GND. Connecting a single resistor from OUT to SET programs output voltage. Calculate the value of the required resistor from the formula:

$$R_{SET} = (V_{OUT} – 0.4V)/50\mu A$$

Connecting a capacitor in parallel with R_{SET} provides output voltage soft-start capability, improves transient response and decreases output voltage noise.

The LT3086 error amplifier design is configured so that the regulator always operates in unity-gain.

OUT (Pins 7, 8/Pins 6, 7/Pin 3/Pin 3): Output. These pin(s) supply power to the load. Connect all OUT pins together on the DHD and FE packages for proper operation. Stability requirements demand a minimum 10µF ceramic output capacitor with an ESR less than 100mΩ to prevent oscillations. Large load transients require larger output capacitance to limit peak voltage transients. Permissible

PIN FUNCTIONS (DFN/TSSOP/DD-Pak/TO-220)

output voltage range is 0.4V to 32V. ***The LT3086 requires a 1mA minimum load current to ensure proper regulation and stability.***

IN (Pins 10, 11/Pins 10, 11/Pin 5/Pin 5): Input. These pin(s) supply power to the device. Connect all IN pins together on the DHD and FE packages for proper operation. The LT3086 requires a local IN bypass capacitor if it is located more than a few inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery powered circuits is advisable. A 10µF minimum input capacitor generally suffices. The IN pin(s) withstand a reverse voltage of 45V. The device limits current flow and no negative voltage appears at OUT. The device protects itself and the load against batteries that are plugged in backwards.

$\overline{\text{SHDN}}$ (Pin 12/Pin 12/Pin 6/Pin 6): Shutdown/UVLO. Pulling the $\overline{\text{SHDN}}$ pin typically below 1V puts the LT3086 into a low power state and turns the output off. Quiescent current in shutdown is typically less than 1µA. The $\overline{\text{SHDN}}$ pin turn-on threshold is typically 1.22V. This pin may either be used as a shutdown function or as an undervoltage lockout function. If using this pin as an undervoltage lockout function, use a resistor divider between IN and GND with the tap point tied to $\overline{\text{SHDN}}$. If using the pin as a shutdown function, drive the pin with either logic or an open-collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open-collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 10µA at 6V. If unused, connect the $\overline{\text{SHDN}}$ pin to IN.

TEMP (Pin 13/Pin 13/Pin 7/Pin 7): Die Junction Temperature. This pin outputs a voltage indicating the LT3086 average die junction temperature. At 25°C, this pin typically outputs 250mV. The TEMP pin slope equals 10mV/°C so that at 125°C, this pin typically outputs 1.25V. This pin does not read temperatures less than 0°C. The TEMP pin is not meant to be an accurate temperature sensor, but is useful for debug, monitoring and calculating thermal resistance of the package mounted to the PCB. The TEMP pin also incorporates the ability to program a thermal limit temperature lower than the internal typical thermal shutdown temperature of 165°C. Tying a resistor from TEMP to GND programs the thermal limit temperature with a 100µA trip point. Calculate the value of the resistor from the formula:

$$R_{TEMP} = \frac{\left(T_{SHDN} \bullet \frac{10mV}{°C}\right)}{100\mu A}$$

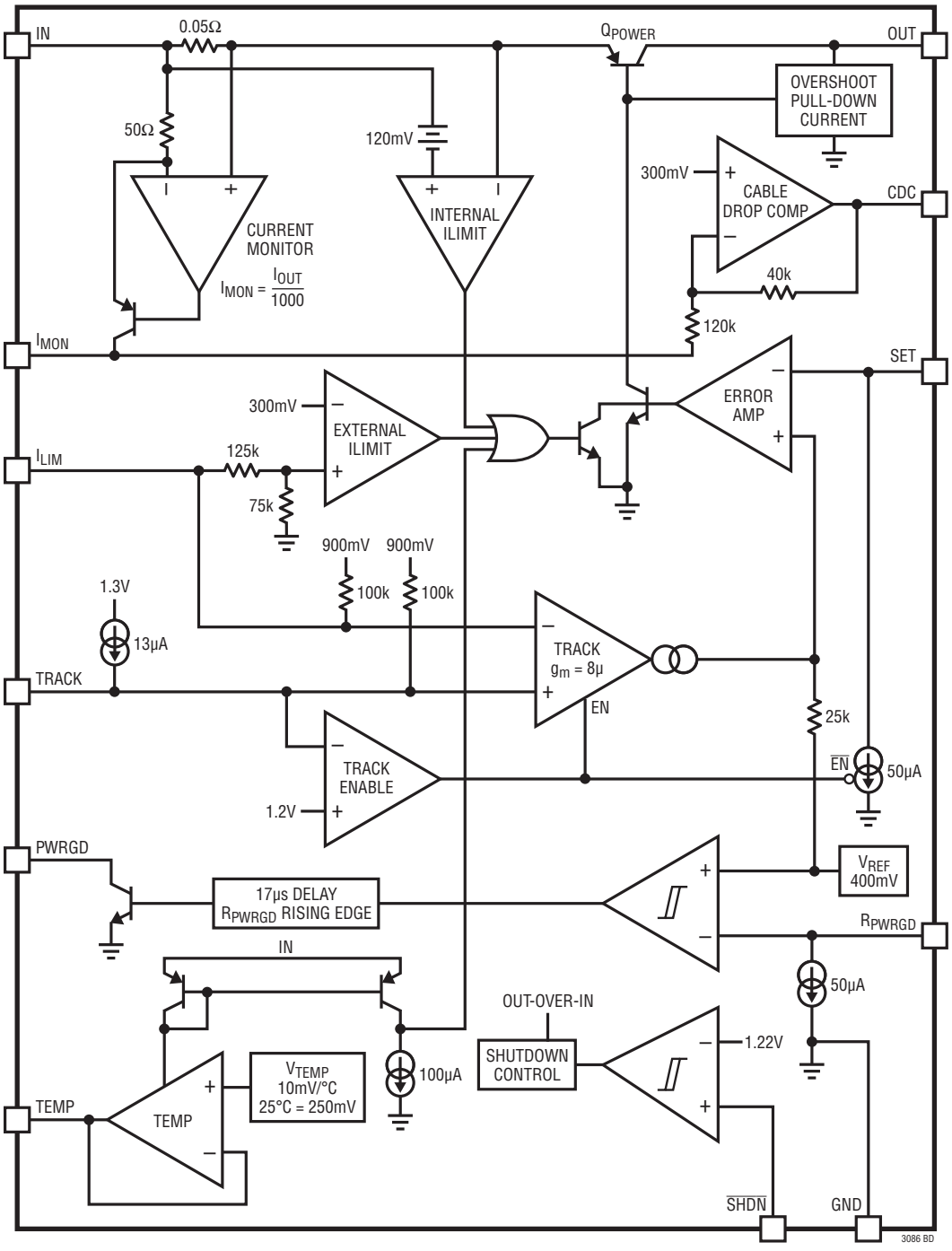
where T_{SHDN} is the desired die thermal limit temperature.

There are several degrees of hysteresis in the thermal shutdown that cycles the regulator output on and off. Limit the capacitance on the TEMP pin to less than 100pF. To prevent saturation in the TEMP output device, ensure that V_{IN} is higher than V_{TEMP} by 250mV.

TRACK (Pin 14/Pin 14/NA/NA): Track pin for paralleling. The TRACK pin allows multiple LT3086s to be paralleled in a master/slave(s) configuration for higher output current applications. This also allows heat to be spread out on the PCB. This circuit technique does not require ballast resistors and does not degrade load regulation. Tying the TRACK pin of the slave device(s) to the I_{MON}/I_{LIM} pins of the master device enables this function. If the TRACK function is unused, TRACK is in a default clamped high state. A TRACK pin voltage below 1.2V on slave device (s) shuts off the internal 50µA reference current at SET such that only the 50µA reference current of the master device is active. All SET pins must be tied together in a master/slave configuration.

PWRGD (Pin 15/Pin 15/NA/NA): Power Good Flag. The PWRGD pin is an open-collector logic pin connected to the output of the power good comparator. PWRGD asserts low if the R_{PWRGD} pin is less than 400mV. The maximum low output level of 200mV over temperature is defined for 200µA of sink current. If R_{PWRGD} is greater than 400mV, the PWRGD pin de-asserts and becomes high impedance. The PWRGD pin may be pulled to 36V without damaging any internal circuitry regardless of the input voltage.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT3086 is a multifunction, low dropout, low noise, linear regulator with shutdown, and adjustable power good. The device supplies 2.1A with a typical dropout voltage of 330mV and operates over a wide 1.4V to 40V input supply range.

The operating quiescent current is 1.2mA and drops to less than 1µA in shutdown. The LT3086 regulator optimizes stability and transient response with a minimum low ESR 10µF ceramic output capacitor. A single resistor sets the output voltage from 0.4V to 32V. Similarly, a single resistor sets the power good threshold. The regulator typically provides 0.1% line regulation and 0.1% load regulation.

The LT3086 has convenient programmable diagnostic features. An output current monitor, that is typically 1/1000 of the output current, can set the current limit lower than the typical 2.4A internal limit. A temperature monitor, that is typically 10mV/°C where 250mV = 25°C, can set the thermal limit lower than the typical 165°C internal thermal limit.

For applications where the voltage error at the load is caused by the resistance in the connections between the LT3086 and the load, programmable cable drop compensation cancels the error with a single resistor. Multiple LT3086 regulators can be paralleled for higher load currents and heat spreading without the need for external ballast resistors.

During load transients where the output overshoots (regulated output voltages of 0.8V or higher), an internal pull-down current activates pulling about 15mA from the OUT pin to ground. The pull-down current is disabled when the output is at or below regulation. The regulator and the output overshoot pull-down turn off when the output voltage is pulled higher than the input by typically 225mV. Curves of OUT Over IN Shutdown Threshold appear in the Typical Performance Characteristics section.

Internal protection circuitry includes reverse-battery protection, reverse-output protection, reverse-current protection, current limit with foldback and thermal shutdown.

Programming Output Voltage

The LT3086 has an output voltage range of 0.4 to 32V. The output voltage is programmed with a single resistor, R_{SET}, connected from OUT to the SET pin, as shown in Figure 1. The SET pin has an internal 50µA current source to ground that generates a voltage drop across R_{SET}. The device servos the output to maintain the SET pin voltage at 0.4V referenced to ground. Calculate the output voltage using the formula in Figure 1. Curves of SET Pin Reference Voltage and Current vs Temperature appear in the Typical Performance Characteristics section.

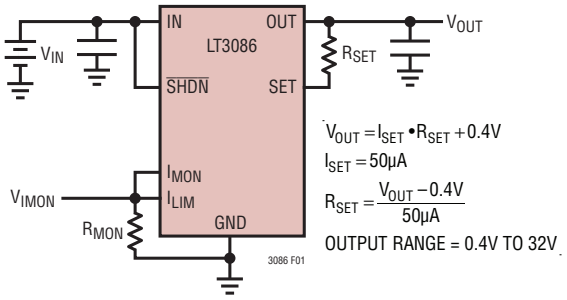


Figure 1. Programming Output Voltage

Table 1. Output Voltage R_{SET} Values

V_{OUT} (V)	R_{SET} (Ω) IDEAL	R_{SET} (Ω) SINGLE 1%	R_{SET} (Ω) DUAL 1%	V_{OUT} ERROR FOR SINGLE 1%
1	12k	12.1k	11.8k + 200	0.5%
1.2	16k	16.2k	15.8k + 200	0.8%
1.5	22k	22.1k	21.5k + 511	0.3%
1.8	28k	28k	N/A	0%
2	32k	32.4	31.6k + 383	1.0%
2.5	42k	42.2k	41.2k + 825	0.4%
3.3	58k	57.6k	57.6k + 383	–0.6%
5	92k	90.9k	90.9k + 1.1k	–1.1%
12	232k	232k	N/A	0%

Table 1 shows the nearest 1% resistor values for some common output voltages, along with the output error caused by not using the ideal resistance value. These errors can be as high as 1% because of the 2% spacing between standard 1% resistors. If tighter output tolerance is required, consider using more accurate resistors. Alternatively, the resistance of R_{SET} can be fine-tuned by adding a low value 1% resistor in series, see Table 1 dual 1% column.

Programming Power Good

The adjustable power good threshold is programmed with a single resistor, R_{PGSET}, similar to how the output voltage is programmed by R_{SET}. Similar to the SET pin, R_{PWRGD} determines the power good threshold with the

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combination of a 0.4V reference voltage and a precision 50µA pull-down current. The power good signal pulls high if the voltage on R_{PWRGD} increases above 0.4V. Built-in hysteresis of typically 0.6% exist for both the 0.4V voltage threshold and the 50µA current source. Connecting a resistor between the RPWRGD and PWRGD pins can increase the power good hysteresis. See the Application circuits for an example.

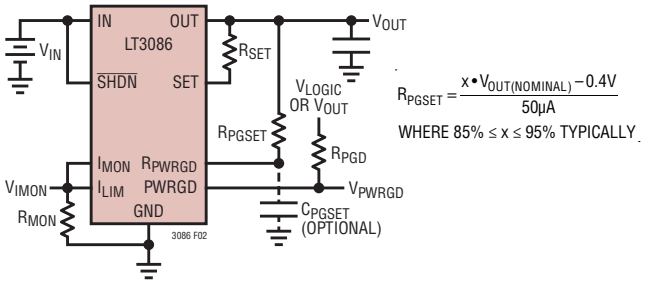

Figure 2. Programming Power Good

The PWRGD pin is the power good open-collector logic output. An internal delay of typically 17µs exists only for the rising edge (when the regulator output voltage rises above the power good threshold) to reject noise or chatter during startup. If the power good function is not needed, leave the R_{PWRGD} and PWRGD pins floating.

The power good threshold is typically programmed to 85% to 95% of the regulated output voltage. Due to variations in regulator parameters and resistor variations, it is not practical to set the power good threshold greater than 95% of the output voltage. Account for load transients where the output voltage droops momentarily before recovering. If increasing output capacitance to reduce output voltage undershoot or if setting the power good threshold lower is not possible, a capacitor, C_{PGSET}, from R_{PWRGD} to ground can filter and delay the output signal. This allows for a configurable deglitching period before the power good threshold trips. For example, consider an application with a nominal 1V output using 10µF of output capacitance and the power good threshold set for 90% of $V_{OUT(NOMINAL)}$. A 1.5A output load current step momentarily undershoots V_{OUT} below the 90% threshold for more than 4µs, thus triggering the PWRGD pin to pull low. Using a C_{PGSET} of greater than 270pF deglitches the power good comparator and prevents the PWRGD pin from pulling low for undershoot events less than 4µs in duration.

For applications using cable drop compensation and requiring a power good signal, calculate the value of R_{PGSET} based on the voltage at the load rather than the LT3086's output voltage. In order for the power good threshold to be independent of the cable drop compensation's modulation of the LT3086's output voltage as a function of load current, connect a resistor between CDC and R_{PWRGD} with the same value as R_{CDC}, the resistor between CDC and SET. This technique avoids connecting the R_{PGSET} resistor to the load voltage through a long trace/wire and eliminates potential stray signal coupling into the R_{PWRGD} pin. See the front page Typical Application circuit as an example.

Output Voltage Noise and Transient Response

The LT3086 regulator provides low output voltage noise over a 10Hz to 100kHz bandwidth while operating at full load. Output voltage noise is approximately 65nV/√Hz over this frequency bandwidth at the unity gain output voltage of 0.4V at 2.1A.

To lower output voltage noise for higher output voltages, include a feedforward capacitor, C_{SET}, from OUT to the SET pin, as shown in Figure 3. A good quality, low leakage capacitor is recommended. This capacitor bypasses the voltage setting resistor, R_{SET}, providing a low frequency noise pole. With the use of 10nF for C_{SET}, output voltage noise decreases from 280µV_{RMS} to 40µV_{RMS} at 2.1A when the output voltage is set to 5V.

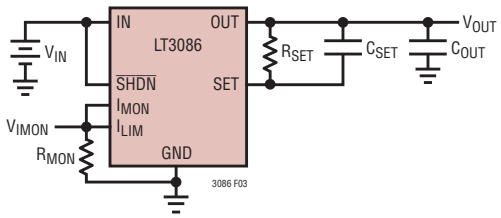

Figure 3. Feedforward Capacitor for Improved Transient Response

Higher values of output voltage noise are often measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby active signal traces may induce unwanted noise onto the LT3086's output. Power supply ripple rejection must also be considered. The LT3086 regulator does not have unlimited power supply rejection and will pass a small portion of the input noise to the output.

Using a feedforward capacitor, C_{SET}, has the added benefit of improving transient response for output voltages greater than 0.4V. With no feedforward capacitor, the settling time

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and output voltage transients increase as the output voltage is set above 0.4V. See Figure 4 and Transient Response curves in the Typical Performance Characteristics section.

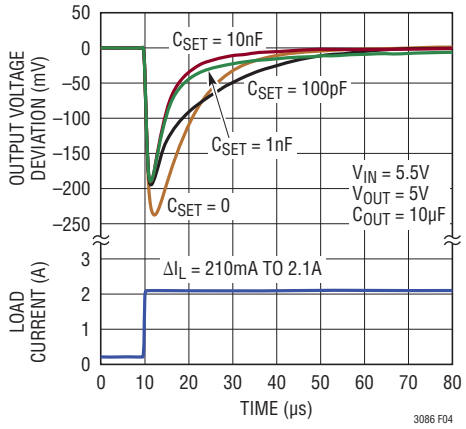

Figure 4. Transient Response vs Feedforward Capacitor

Start-up time is affected by the use of a C_{SET} feedforward capacitor. Start-up time is directly proportional to the size of the feedforward capacitor and output voltage. Settling time to 1% is approximately:

$$t_{SETTLE} = \frac{4.2 \bullet V_{OUT} \bullet C_{SET}}{50\mu A}$$

See the Start-Up Time vs C_{SET} curve in the Typical Performance Characteristics section. **If the LT3086 is configured for cable drop compensation, LTC does not recommend using a feedforward capacitor because C_{SET} filters the CDC correction signal and transient response to load current changes degrades.**

Output Current Monitor and External Current Limit

Current out of the I_{MON} pin is typically equal to 1/1000 of the regulator's output current. The output current monitor maintains accuracy across the full input voltage range, even during dropout. A resistor, R_{MON}, placed from I_{MON} to ground, sets the voltage scale factor for use with analog-to-digital converters, as shown in Figure 5. For example, with 442Ω for R_{MON}, V_{IMON} is set for 0.663V when I_{OUT} = 1.5A.

External current limit activates if the voltage on the I_{LIM} pin exceeds the typical 0.8V threshold. Tying the I_{MON} and I_{LIM} pins together allows the user to program a desired current limit based on the output current. An internal current limit, typically 2.4A, is always active and limits output current even if the I_{LIM} pin is grounded. In addition, internal current limit foldback overrides external current limit if the $V_{IN} – V_{OUT}$ differential voltage becomes excessive.

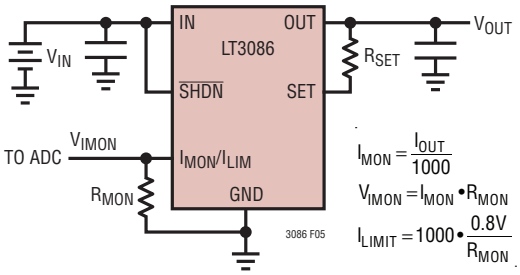

Figure 5. Output Current Monitor and External Current Limit

Note that the output current monitor represents not just the load current, but the current into the output capacitor as well. During startup and large load transients, the output current monitor indicates the current required to charge the output capacitor in addition to the load current. To prevent external current limit from engaging prematurely, set the external current limit above the maximum load current to allow the output capacitor to recover without being current limited.

For external current limits set for less than 1A, connect a series 1k-10nF RC network from I_{LIM} to ground to ensure current limit loop stability. Adding an RC network from I_{LIM} to ground also delays the current monitor signal, allowing output currents higher than the external current limit for a limited duration. This is useful for applications with large output capacitance that would otherwise trigger external current limit during startup and large load transients, slowing output voltage recovery. To guarantee external current limit stability, ensure that the RC network from I_{LIM} to GND has a capacitor value equal to or greater than 10nF and the resistor value is between $0.01 \bullet C^{-0.6}$ and 1k. C is the capacitor value in units of farads. LTC does not recommend an RC network other than the 1k-10nF combination if using the cable drop compensation and paralleling functions.

To configure the output current monitor and external current limit correctly, decide on the necessary current limit and full-scale monitor output voltage. Voltage is limited to 0.8V if I_{MON} is tied to I_{LIM}. External current limit is typically set 10% to 20% above maximum load current to allow for

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large transient events and I_{LIM} threshold variations. For example, if the maximum load current is 1.5A and both I_{MON} and I_{LIM} pins are tied together, an R_{MON} scaling resistor of 442Ω yields an external current limit of 1.8A.

If higher output current monitor voltages are needed, the DFN package offers the ability to separate the I_{MON} and I_{LIM} pins with a resistor, as shown in Figure 6. To prevent saturation in the I_{MON} output device, choose R_{MON} so that V_{IMON} is at least 0.6V less than V_{IN}. If external current is not needed, ground the I_{LIM} pin.

Output current monitor accuracy for very low output currents is limited by the offset in the current monitor amplifier and parasitic current paths. The equivalent circuit of the parasitic current paths are shown in Figure 7. With zero output load current, the current into R_{MON} is typically 11µA when the I_{MON} and I_{LIM} pins are tied together. As a result, load currents between 0mA and 11mA typically cannot be measured. See Current Monitor Offset curves in the Typical Performance Characteristics section.

Load Regulation and Cable Drop Compensation

Output load regulation for the LT3086 is typically 0.1%. Optimal regulation is obtained when the R_{SET} feedback resistor is connected to the OUT pin of the regulator. In high current applications, small voltage drops appear due to the resistances of PCB traces or wires between the regulator and the load. These drops may be eliminated by connecting R_{SET} directly to the output at the load as shown in Figure 8. Note that the voltage drop across R_{OUT} and R_{RTN} add to the dropout voltage of the regulator. The voltage drop across R_{GND} should also be minimized to reduce output voltage error due to ground pin current. See GND Pin Current curves in the Typical Performance Characteristics section.

The LT3086 has cable drop compensation (CDC) functionality that allows delivery of well regulated voltage to remote loads using only two wires of known fixed resistance. Compensation is user programmed by connecting a resistor, R_{CDC}, between the SET and CDC pins, as shown in Figure 9.

At zero load current, the CDC pin typically regulates to the same voltage as the SET pin. The voltage decreases at a rate equal to 1/3 of the change in I_{MON} voltage. For example, if V_{IMON} increases from 0 to 0.6V, V_{CDC} decreases

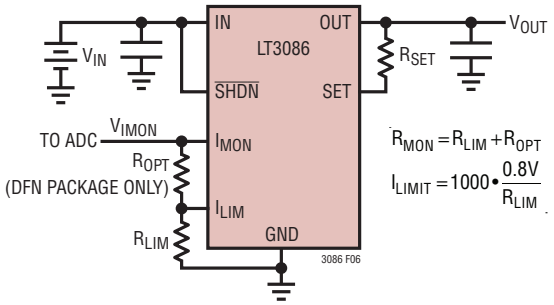

Figure 6. Separate I_{MON} and I_{LIM} (DFN Package Only)

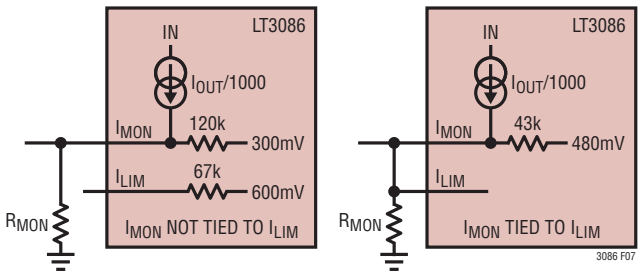

Figure 7. Equivalent Circuits of I_{MON} and I_{LIM}

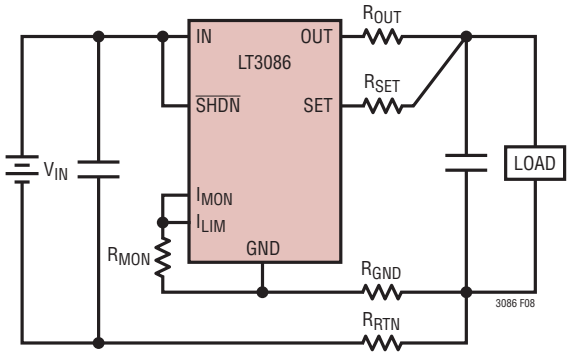

Figure 8. Kelvin Sense Connection

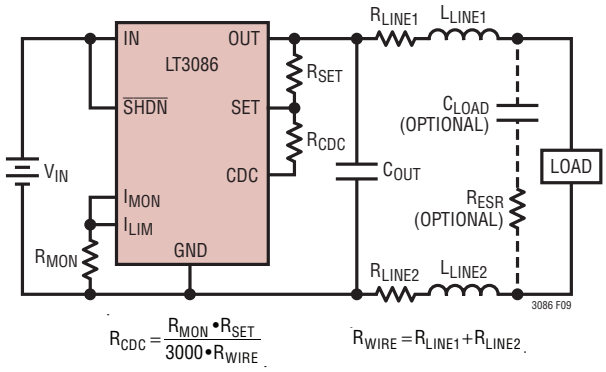

Figure 9. Cable Drop Compensation

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by 0.2V. As a result, the current that flows through R_{CDC} is proportional to load current which increases the voltage across R_{SET}, effectively increasing output voltage. R_{CDC} is selected using the following equation so that the voltage at the OUT pin increases to cancel the voltage drop in the cables connected to the load.

$$R_{CDC} = \frac{R_{MON} \bullet R_{SET}}{3000 \bullet R_{WIRE}}$$

where R_{WIRE} is the total resistance of the supply and return cabling connecting the LT3086 to the load.

Figure 10 shows the transient response with cable drop compensation. With compensation, the output voltage at the load remains nearly constant. Note that the transient voltage droop in output voltage is about the same as the voltage droop with no compensation, but with the output voltage returning to the correct compensated voltage.

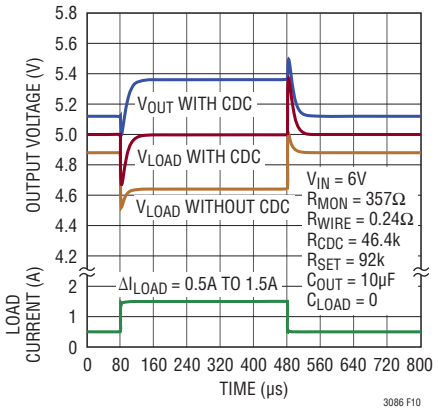

Figure 10. Transient Response with Cable Drop Compensation

If long cables are used, an additional supply bypass capacitor, C_{LOAD}, should be added directly to the load to handle large load transient conditions. C_{OUT} must still directly connect to the OUT pin to ensure stable operation of the LT3086, minimizing output capacitor ESR and ESL. Long cables have inductance where a resonance forms between the wire inductance, L_{WIRE} and C_{LOAD}. Damping is accomplished by adding series resistance, R_{ESR}, to C_{LOAD}. The value of R_{ESR} is approximately:

$$R_{ESR} = \sqrt{2 \bullet \frac{L_{WIRE}}{C_{LOAD}}}$$

There are limits to the amount of voltage drop that can be compensated using cable drop compensation. Using cable drop compensation subjects load regulation to the variability of the current monitor voltage output and the cabling resistance. LTC recommends limiting cable drop compensation to 20% of V_{OUT} for applications needing good regulation. The limiting factor is variations in wire temperature as copper wire resistance changes about 19% for a 50°C temperature change. If output regulation requirements are loose (e.g., when using a secondary regulator), cable drop compensation of up to 50% may be used.

Noise from the current monitor output affects noise seen at the output. Filtering the current monitor output with an RC network from I_{LIM} to ground is effective at reducing this noise source, especially at light loads. Consult the Output Current Monitor and External Current Limit section for more information

Paralleling Multiple Regulators

The LT3086 has been specifically designed to make paralleling multiple regulators together easy. Paralleling enables applications to increase total output current and to spread heat dissipated by the regulator over a wider area on the PCB. The parallel scheme is based on a master/slave principle, where one LT3086 is designated as master, and the other regulators act as slaves with active sharing of total load current, as shown in Figure 11. The slave's internal current tracking amplifier compares the current monitor output from the master with the current monitor output seen at the slave's I_{LIM} pin, and servos the slave's output current to match the master's.

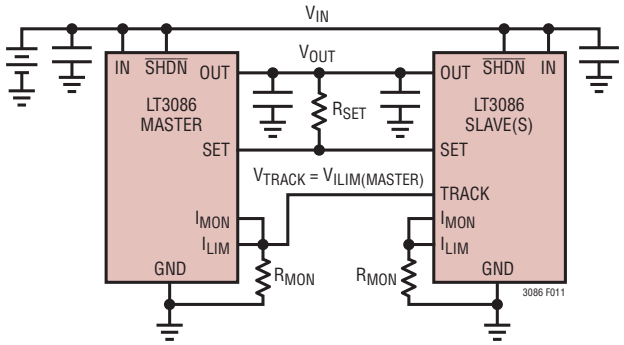

Figure 11. Master/Slave(s) Configuration for Paralleling

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The master LT3086 is connected exactly the same as a single regulator where its output current monitor voltage seen at its I_{LIM} pin is used as the common current tracking signal. The slave devices connect this signal to their TRACK pins to make their output current equal to the master's.

The TRACK pin has an internal pull-up current that is typically 15µA at 0.75V. When the TRACK pin is unused, the pin is pulled up and clamped at 1.25V, disabling the current tracking amplifier. When the TRACK pin is connected to the master current tracking signal, the TRACK pin voltage is pulled below the 1.2V threshold, enabling the current tracking amplifier and disabling the slave's 50µA reference current, I_{SET}. Disabling the reference current ensures that the master is the only device controlling the output voltage. Set the maximum master current tracking signal to less than 0.8V to prevent external current limit from triggering prematurely. To prevent the slave current tracking amplifier from ever being disabled, the slave TRACK pin must be tied to the master I_{LIM} pin. The master I_{LIM} pin has an internal 1V clamp that is below the slave 1.2V current tracking amplifier enable threshold.

When multiple slaves are used, a smaller master R_{MON} resistor should be used to compensate for the pull-up currents from all the TRACK pins of the slaves. For example, a master sourcing 2.1A typically has 0.697V at its I_{LIM} pin with an R_{MON} resistor of 332Ω. Referring to the TRACK pin pull-up current curve in the Typical Performance Characteristics, with 0.697V on the TRACK pin, each slave typically adds 15µA to the master's 2.1mA I_{MON} output. For an application with 3 slaves connected, decrease R_{MON}'s value to:

$$R_{MON} = \frac{0.697V}{[2.1mA + (3 \bullet 15\mu A)]} = 325\Omega$$

The closest 1% resistor value equals 324Ω.

All slave regulators must have their SET pins connected to the master SET pin. The TRACK amplifier operates by adjusting the slave internal reference voltage slightly as a function of the difference in master and slave current monitor voltages. This has a strong effect on the slave output current, which forces the slave output current to match the master.

Mismatch between master and slave internal reference voltages and current monitor outputs, offset in the slave TRACK amplifier and TRACK pin pull-up currents all contribute to output current sharing error. In the case of negative offset, a slave runs less current than the master. At very light loads, negative offset enables the slave output overshoot pull-down circuit, forcing the master to supply current to keep the output voltage within regulation. As a result, quiescent current may increase for very light loads in the master/slave configuration.

In some applications, multiple regulators may be spaced some distance apart to optimize heat distribution. That makes the use of low resistance traces important to connect each regulator to the local ground system and to avoid ground loops created by load currents. Ground currents can be as high as 30mA at 1.5A and 50mA at 2.1A, for each regulator. Limiting differential ground pin voltages to less than 10mV minimizes tracking errors. Ground trace resistance between master and slaves should be less than 10mV/30mA = 0.33Ω at 1.5A load, and 10mV/50mA = 0.2Ω for 2.1A load.

Output Capacitance

The LT3086 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 10µF with an ESR of 0.1Ω or less to prevent oscillations. The output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. For applications with large load current transients, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response. For example, a 47µF tantalum capacitor with ESR = 0.1Ω in parallel with the 10µF ceramic capacitor with ESR < 0.01Ω reduces output deviation by about 2:1 for large transient loads and increases loop phase margin.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics

APPLICATIONS INFORMATION

provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figures 12 and 13. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied, and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor.

The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance changes due to DC bias is less with X5R and X7R capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

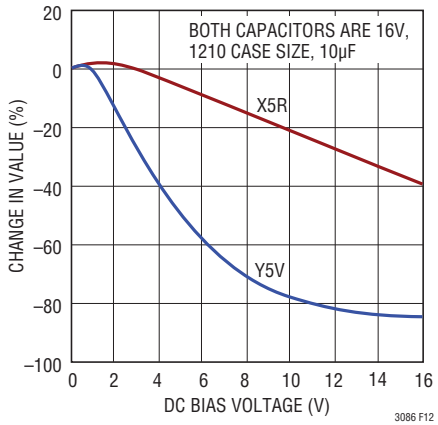

Figure 12. Ceramic Capacitor DC Bias Characteristics

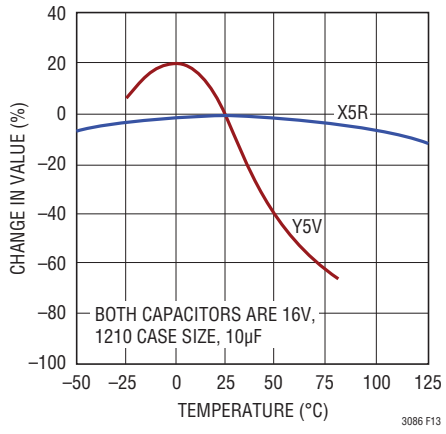

Figure 13. Ceramic Capacitor Temperature Characteristics

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise.

Input Capacitance

Low ESR ceramic input bypass capacitors are acceptable for applications with short input and ground leads. However, applications connecting a power supply to the LT3086 using long wires are prone to voltage spikes, reliability concerns and application-specific board oscillations.

The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic capacitor, forms a high-Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications are then required. This behavior is not indicative of LT3086 instability, but is a common application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has approximately 465nH of self-inductance. Two methods can reduce wire self-inductance. One method divides the current flowing towards the LT3086 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires connects two equal inductors in parallel, but placing them in close proximity creates mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward

APPLICATIONS INFORMATION

and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward- and return-current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If a battery, mounted in close proximity, powers the LT3086, a 10µF input capacitor suffices for stability. However, if a distant supply powers the LT3086, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3086's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3086 input bypassing. Series resistance between the supply and the LT3086 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to add additional input capacitance with higher ESR at the input, such as tantalum or electrolytic capacitors, or by adding resistance in series with a low ESR ceramic capacitor.

Overload Recovery

Like many IC power regulators, the LT3086 has safe operating area protection. The safe operating area protection decreases current limit as input-to-output voltage increases, and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT3086 provides some output current at all values of input-to-output voltage up to the specified 45V operational maximum. Current limit foldback overrides external current limit (if used) if $V_{IN} – V_{OUT}$ voltage differential becomes excessive.

When power is first applied, the input voltage rises and the output follows the input; allowing the regulator to start-up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein the removal of an output short will not allow the output to recover. Other regulators, such as the LT1083/LT1084/LT1085 family and LT1764A also exhibit this phenomenon, so it is not unique to the LT3086. The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage is already turned on. The load line intersects the output current curve at two points creating two stable output operating points for the regulator. With this double intersection, the input power supply needs to be cycled down to zero and brought up again for the output to recover.

Thermal Considerations

The power handling capability of the LT3086 is limited by the maximum rated junction temperature (125°C for LT3086E, LT3086I, LT3086MP or 150°C for LT3086H). Three components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differential:

   $I_{OUT} • (V_{IN} – V_{OUT})$,

2. GND pin current multiplied by the input voltage:

   $I_{GND} • V_{IN}$, and

3. Current monitor current multiplied by the input/current monitor voltage differential:

   $I_{MON} • (V_{IN} – V_{IMON})$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation equals the sum of the three components listed above.

The LT3086 regulator has internal thermal limiting that protects the device during overload conditions. For continuous normal conditions, the maximum junction temperature of 125°C (E-grade, I-grade, MP-grade) or 150°C (H-grade) must not be exceeded. Carefully consider all sources of thermal resistance from junction-to-ambient including other heat sources mounted in proximity to the LT3086.

The underside of the LT3086 DFN and TSSOP packages have exposed metal (10.5mm^2) from the lead to the die attachment. These packages allow heat to directly transfer from the die junction to the printed circuit board metal. The dual-in-line pin arrangement allows metal to extend

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beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3086 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes also can spread the heat generated by power devices.

Tables 2 and 3 list thermal resistance for several topside copper areas on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz top/bottom external trace planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. Achieving low thermal resistance necessitates attention to detail and careful PCB layout. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-12 and JESD51-7. The use of thermal vias, increased copper weight, and air flow, will improve the resultant thermal resistance.

Table 2. Measured Thermal Resistance for DHD and FE Package

COPPER AREA			
TOPSIDE* (mm^2)	BACKSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500	2500	2500	25°C/W
1000	2500	2500	26°C/W
225	2500	2500	28°C/W
100	2500	2500	33°C/W

*Device is mounted on topside

Table 3. Measured Thermal Resistance for R Package

COPPER AREA			
TOPSIDE* (mm^2)	BACKSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500	2500	2500	15°C/W
1000	2500	2500	16°C/W
225	2500	2500	19°C/W

*Device is mounted on topside

Measured Thermal Resistance for T7 Package

Thermal resistance (junction-to-case) = 3°C/W.

The LT3086 has the ability to check thermal performance by observing the output current and temperature monitor pins. The effects of heat sinking, the enclosure, and any air movement can be instantly analyzed without special instrumentation.

Calculating Junction Temperature

Example: Given an output voltage of 5V, an input voltage range of 6V ±5%, a maximum output current range of 1A with 698Ω for R_{MON}, and a maximum ambient temperature of 75°C, what will the maximum junction temperature be?

The power dissipated by the device equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)} + I_{MON(MAX)} \bullet (V_{IN(MAX)} - V_{IMON(MAX)})$$

where,

$I_{OUT(MAX)} = 1A$

$V_{IN(MAX)} = 6.3V$

I_{GND} at ($I_{OUT} = 1A$, $V_{IN} = 6.3V$) = 11mA

V_{IMON} at ($I_{OUT} = 1A$, $R_{MON} = 698\Omega$) = 0.698V

So:

$$P = 1A \bullet (6.3V - 5V) + 11mA \bullet 6.3V + 1mA \bullet (6.3V - 0.698V) = 1.38W$$

Using a DFN package, the thermal resistance will be in the range of 25°C/W to 33°C/W depending on the topside copper area. So the junction temperature rise above ambient approximately equals:

$$1.38W \bullet 30°C/W = 41.4°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

$$T_{JMAX} = 75°C + 41.4°C = 116.4°C$$

Protection Features

The LT3086 regulator incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features

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associated with monolithic regulators, such as current limiting and thermal limiting, the devices also protect against reverse-input voltages, reverse-output voltages, and reverse-output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at the output of the device. The typical thermal shutdown temperature is 165°C and incorporates about 7°C of hysteresis. For normal operation, do not exceed the maximum rated junction temperature of 125°C (LT3086E, LT3086I, LT3086MP) or 150°C (LT3086H).

The LT3086 IN pin withstands reverse voltages of 45V. The device limits current flow to less than 2mA (typically less than 1µA) and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

The LT3086 incurs no damage if its output is pulled below ground. If the input is left open-circuit or grounded, the output can be pulled below ground by 36V. No current flows through the pass transistor from the output. However, current flows in (but is limited by) the feedback resistors R_{SET}, that sets the output voltage, and R_{RPWRGD}, that sets the power good threshold. Current flows from the internal clamps in the SET and R_{PWRGD} pins to the external circuitry pulling OUT below ground. If the input is powered by a voltage source, the device protects itself by turning off the power device when the internal clamps activate. If Schottky diodes are used to prevent the SET and R_{PWRGD} pins from activating their internal clamps, the output sources current equal to its current limit capability and the LT3086 protects itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin turns off the device and stops the output from sourcing current. Reverse current flow follows the curve shown in Figure 14.

The LT3086 incurs no damage if the SET and R_{PWRGD} pins are pulled above ground up to 36V. If the input is left open-circuit or grounded, the SET pin performs like a large resistor (typically 80k) in series with a diode.

In circuits where a secondary supply raises the output voltage above the regulated voltage set by R_{SET}, the output overshoot circuitry pulls current from the output pin to ground as long as the output voltage is below the input voltage. Output overshoot current follows the curve shown in Figure 15. When the output voltage is pulled above the input by typically 225mV, the LT3086 shuts down as shown in Figure 16 and the 15mA overshoot pull-down current source turns off.

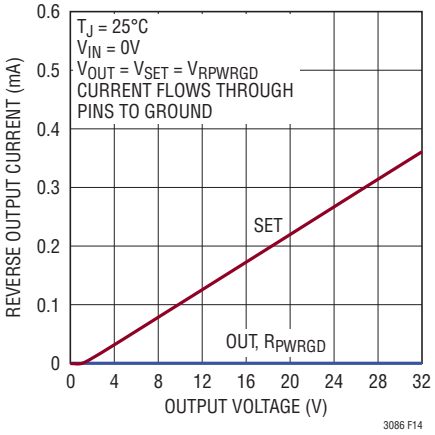


Figure 14. Reverse-Output Current

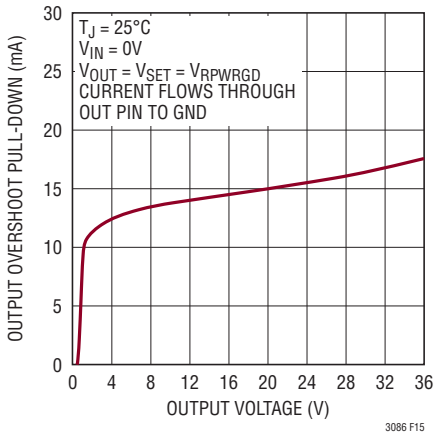


Figure 15. Output Overshoot Pull-Down Current

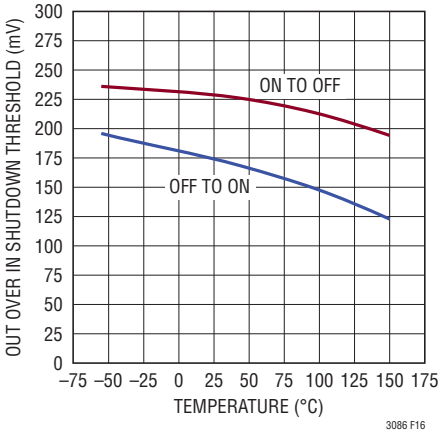
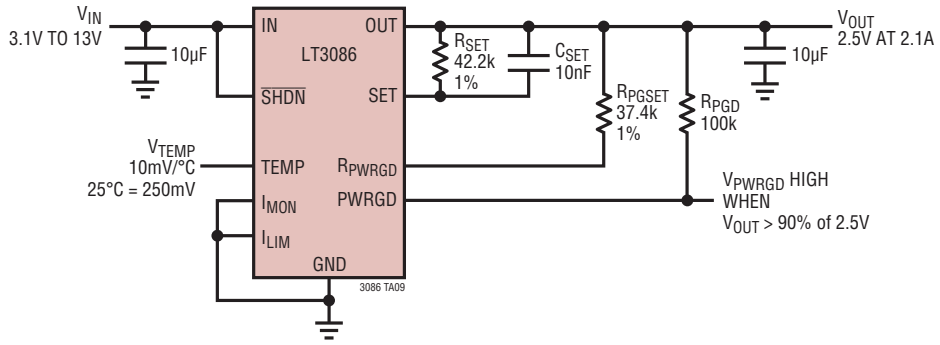


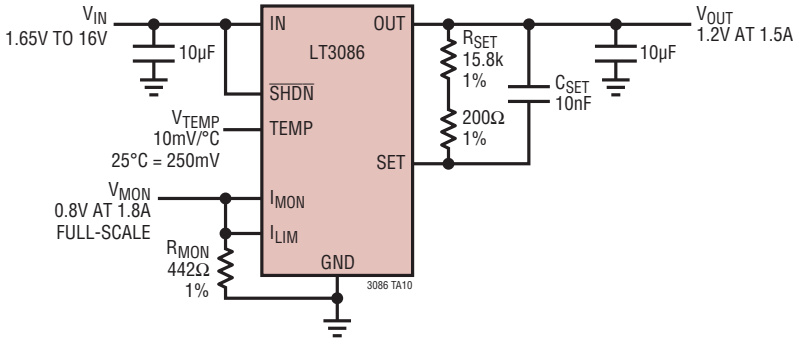
Figure 16. OUT Over IN Shutdown Threshold

TYPICAL APPLICATIONS

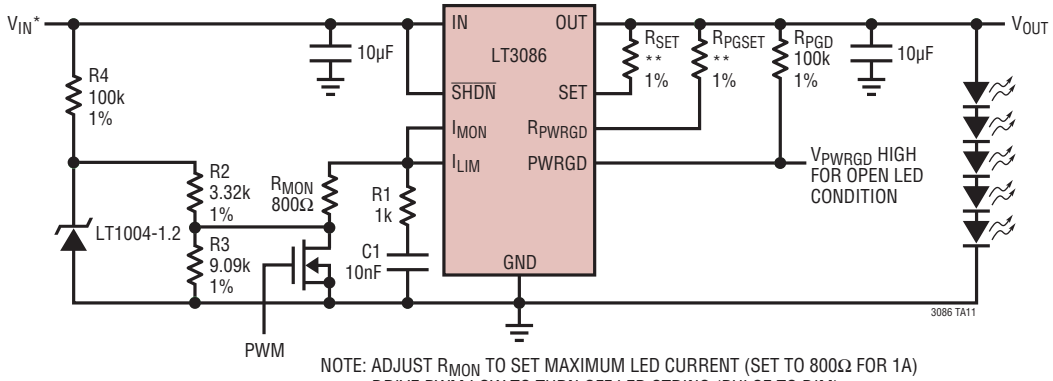
2.5V Low Noise Regulator with Power Good



1.2V, 1.5A Low Noise Regulator with 1.8A External Current Limit



5 White LED Driver with PWM Dimming and LED Open Detection



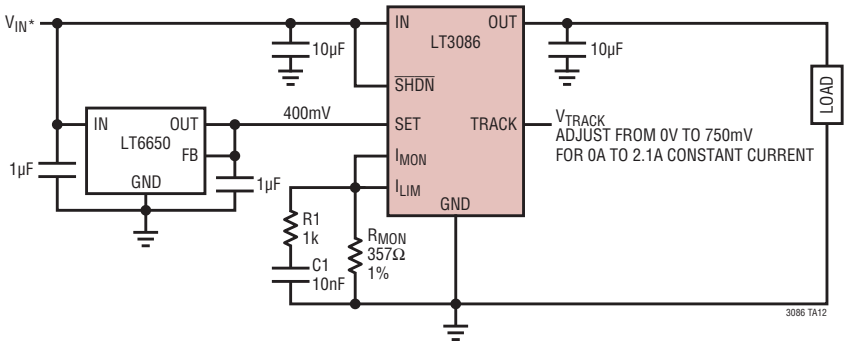
NOTE: ADJUST R_{MON} TO SET MAXIMUM LED CURRENT (SET TO 800Ω FOR 1A)
DRIVE PWM LOW TO TURN OFF LED STRING (PULSE TO DIM)

*INPUT VOLTAGE REQUIRED IS DEPENDENT ON THE LED STRING VOLTAGE

**CHOOSE R_{SET} AND R_{PGSET} BASED ON LED STRING

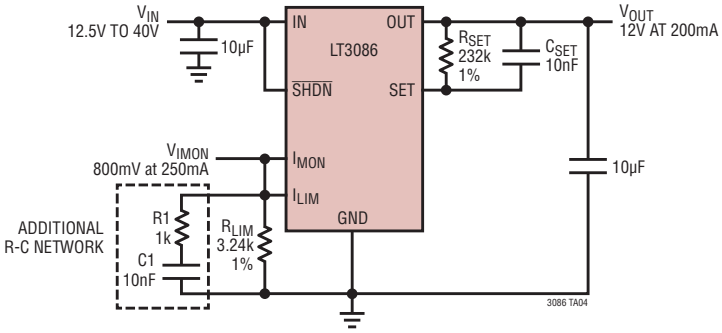
TYPICAL APPLICATIONS

Adjustable Voltage Controlled Current Source

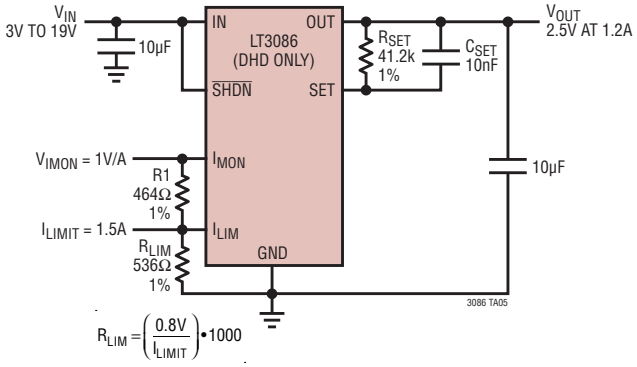


*RESTRICT INPUT VOLTAGE RANGE TO LIMIT POWER DISSIPATION AND PREVENT FOLDBACK CURRENT LIMIT FROM INTERFERING WITH PROPER OPERATION

Ensuring External Current Limit Stability for $I_{LIM} \leq 1A$

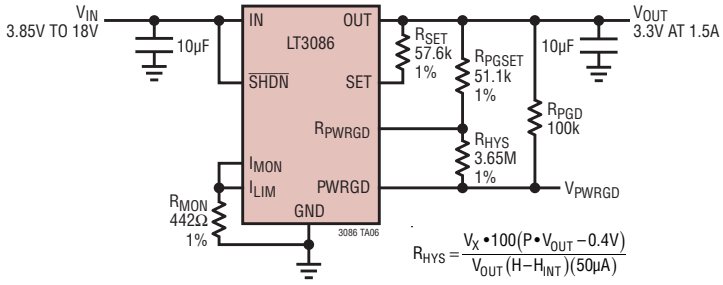


Increasing Current Monitor Output Voltage



$$R_{LIM} = \left(\frac{0.8V}{I_{LIMIT}}\right) \bullet 1000$$

Increasing Power Good Hysteresis (Ex: 2%)



$$R_{HYS} = \frac{V_X \bullet 100(P \bullet V_{OUT} - 0.4V)}{V_{OUT}(H - H_{INT})(50\mu A)}$$

WHERE, V_X = R_{PGD} TERMINATION VOLTAGE = V_{OUT}

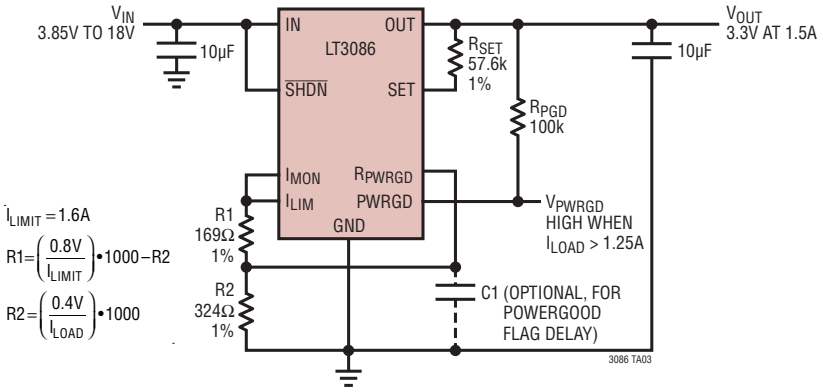
P = POWER GOOD TRIP THRESHOLD (% OF V_{OUT})

H = DESIRED PERCENTAGE HYSTERESIS

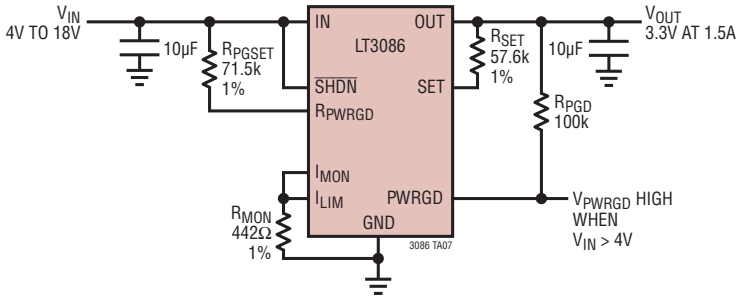
H_{INT} = 0.6 (INTERNAL PERCENTAGE HYSTERESIS)

TYPICAL APPLICATIONS

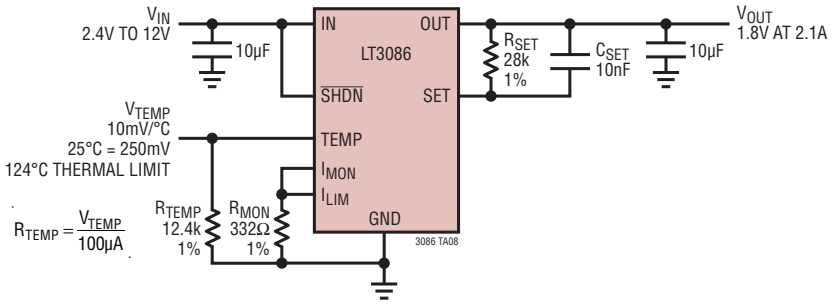
Load Current Monitoring Using Power Good



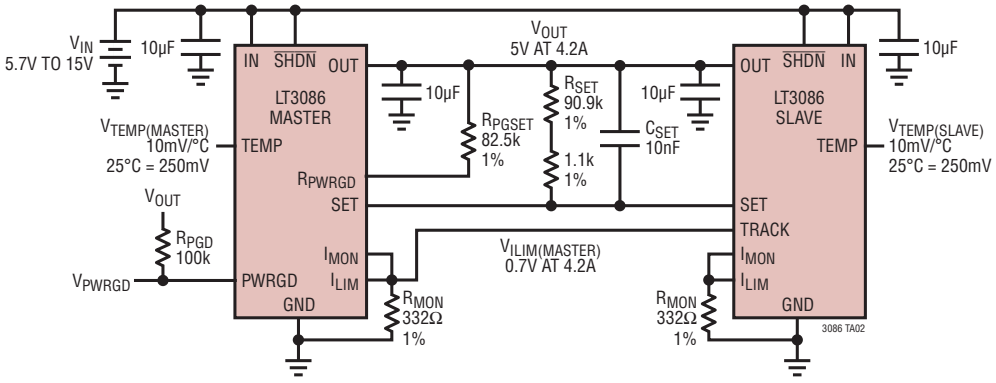
Input Undervoltage Detector Using Power Good



Programming Thermal Limit Temperature



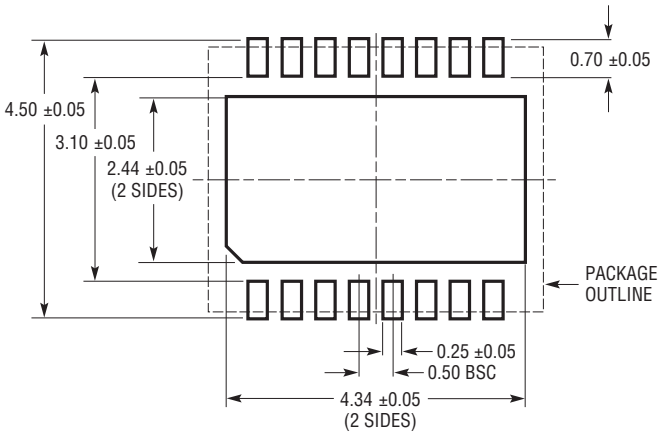
Paralleling Two Regulators for 5V, 4.2A



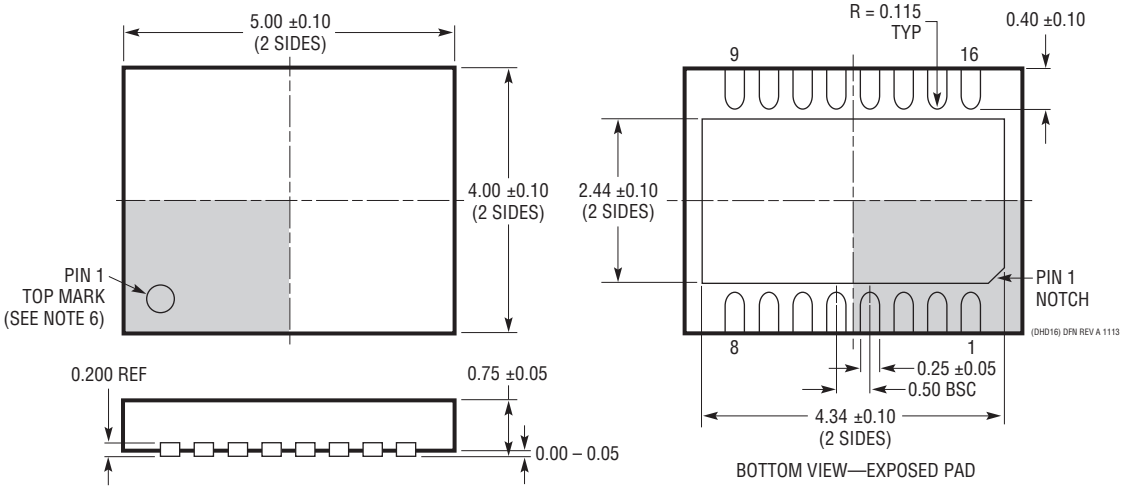
PACKAGE DESCRIPTION

Please refer to http://www.adi.com/designtools/packaging/ for the most recent package drawings.

DHD Package
16-Lead Plastic DFN (5mm × 4mm)
(Reference LTC DWG # 05-08-1707 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



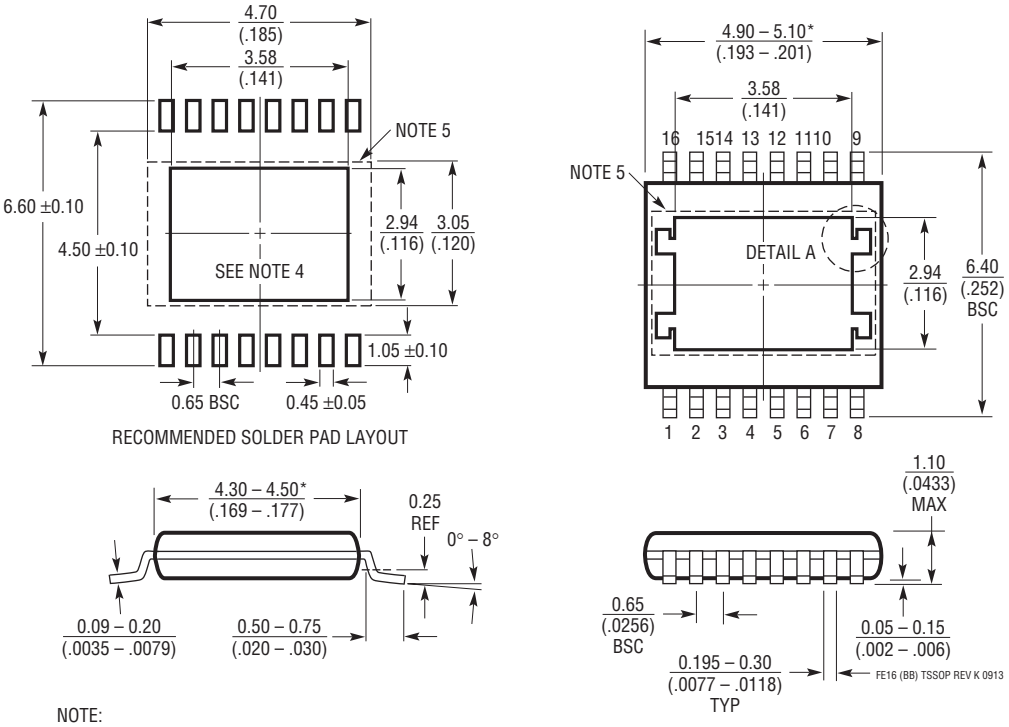
BOTTOM VIEW—EXPOSED PAD

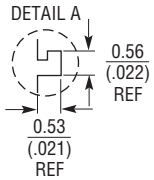
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.adi.com/designtools/packaging/ for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation BB





DETAIL A IS THE PART OF THE LEAD FRAME FEATURE FOR REFERENCE ONLY
NO MEASUREMENT PURPOSE

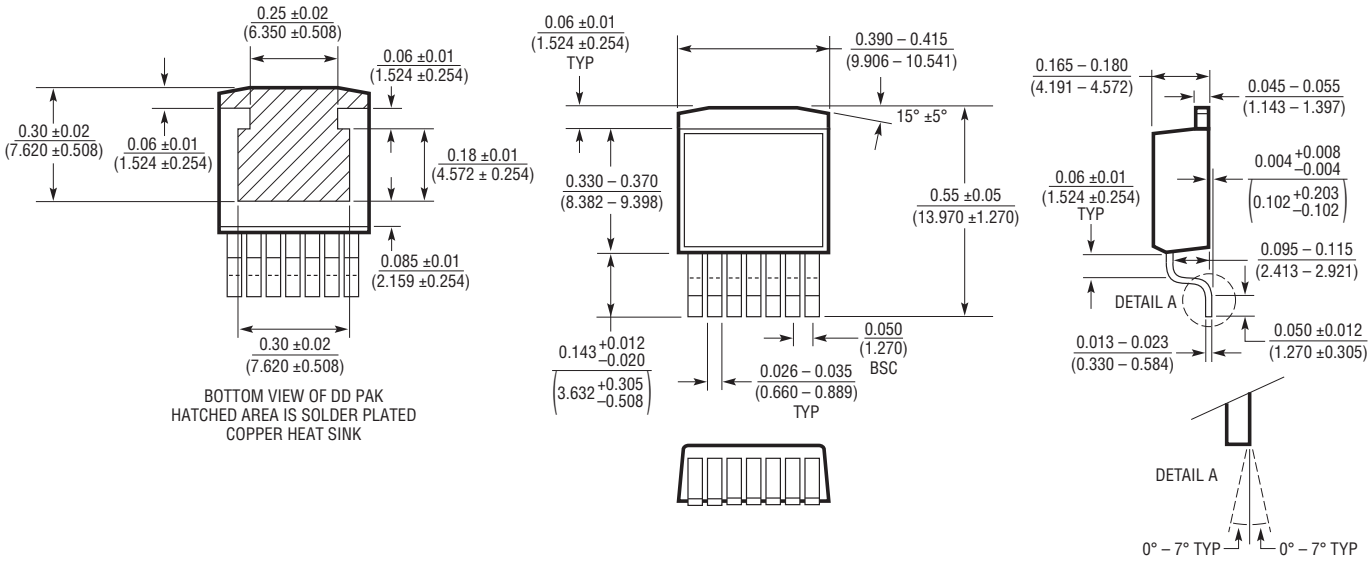
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
5. BOTTOM EXPOSED PADDLE MAY HAVE METAL PROTRUSION IN THIS AREA. THIS REGION MUST BE FREE OF ANY EXPOSED TRACES OR VIAS ON PBC LAYOUT

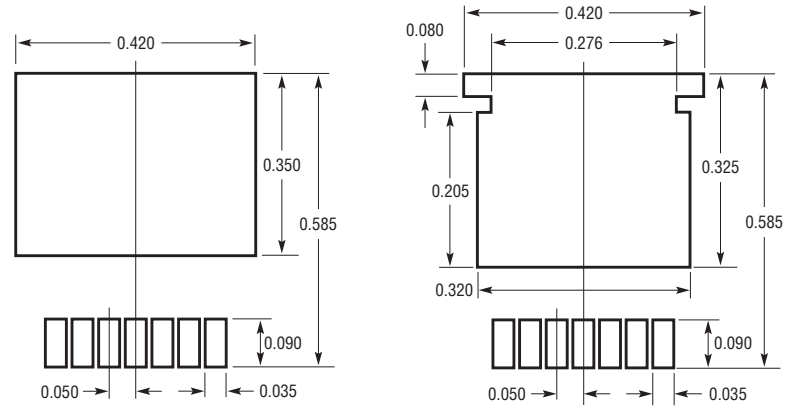
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.adi.com/designtools/packaging/ for the most recent package drawings.

R Package
7-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1462 Rev G)





RECOMMENDED SOLDER PAD LAYOUT

RECOMMENDED SOLDER PAD LAYOUT
FOR THICKER SOLDER PASTE APPLICATIONS

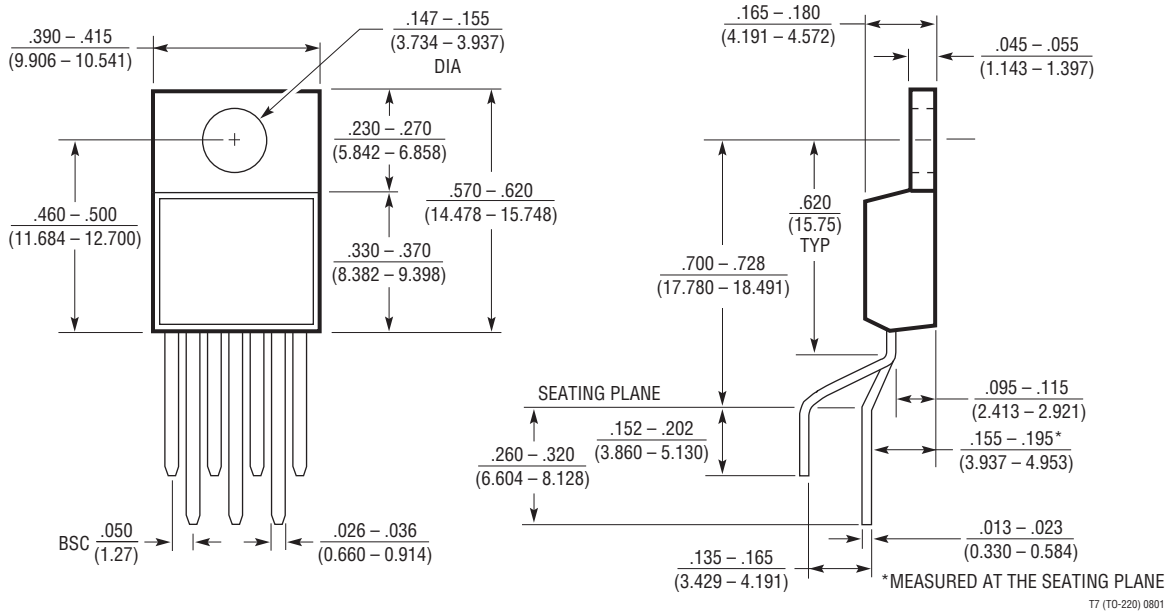
R (DD7) 0416 REV G

NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

PACKAGE DESCRIPTION

Please refer to http://www.adi.com/designtools/packaging/ for the most recent package drawings.

T7 Package
7-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1422)

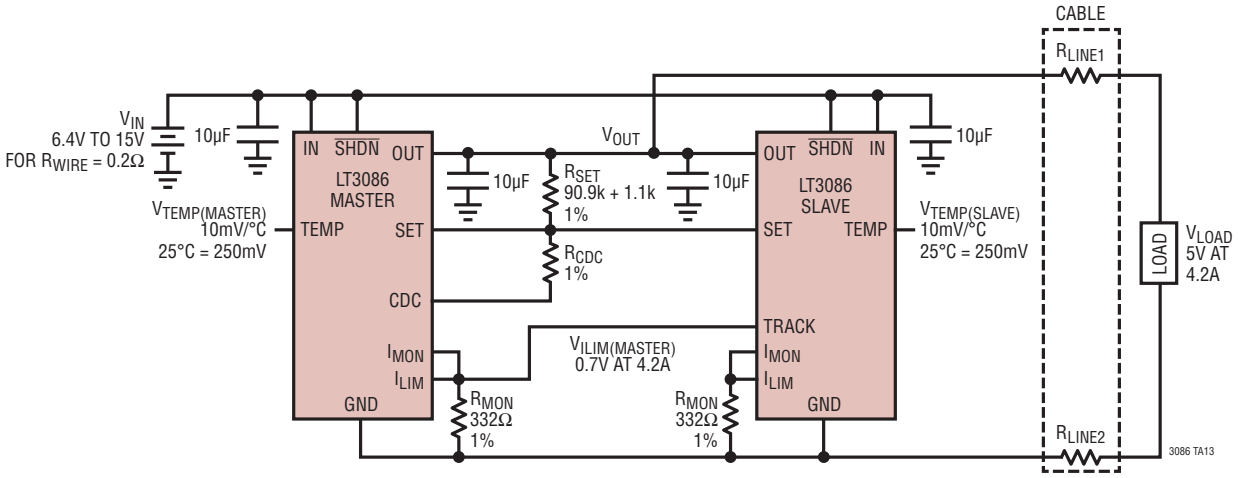


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/14	Added MP-grade for TSSOP, DD-Pak, and TO-220 packages	2 to 4
		Added EC Table line item for Minimum Load Current and Note 16	3, 5
		Added and modified two GND Pin Current curves, two PSRR at 1A curves, two Line Regulation curves and modified V_{OUT} Noise curve	7 to 12
		Updated Thermal Resistance for DHD, FE and R packages	2, 24
		Updated DHD Package Description	29
B	8/16	Added H-grade for TSSOP package	2 to 5, 23, 25
C	3/24	Updated Block Diagram	15

TYPICAL APPLICATION

Paralleling Two Regulators for 5V, 4.2A with Cable Drop Compensation (CDC)



$$R_{CDC} = \frac{R_{MON} \bullet R_{SET}}{(X+1) \bullet 3000 \bullet R_{WIRE}}$$

$R_{WIRE} = R_{LINE1} + R_{LINE2}$

WHERE X = NUMBER OF SLAVES

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1764/ LT1764A	3A, Fast Transient Response, Low Noise LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 2.7V to 20V, TO-220 and DD Packages, -A Version Stable Also with Ceramic Capacitors
LT1963/ LT1963A	1.5A, Low Noise, Fast Transient Response LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 2.5V to 20V, -A Version Stable with Ceramic Capacitors, TO-220, DD-Pak, SOT-223 and SO-8 Packages
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	310mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DD-Pak, MSOP and 3mm × 3mm DFN Packages
LT3022	1A, Low Voltage VLDO Linear Regulator	145mV Dropout Voltage, V_{IN}: 0.9V to 10V, V_{OUT}: 0.2V to 9.5V, Stable with Low ESR, Ceramic Output Capacitors, 16-Pin DFN (5mm × 3mm) and 16-Lead MSOP Packages
LT3070	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Digital Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Digital Output Margining: ±1%, ±3% or ±5%, Low Output Noise: 25µV_{RMS}; Directly Parallelable, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package
LT3071	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Analog Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Analog Margining: ±10%, Low Output Noise: 25µV_{RMS}; Directly Parallelable, I_{MON} Output Current Monitor, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, DD-Pak, SOT-223, MSOP and 3mm × 3mm DFN-8 Packages; -1 Version Has Integrated Internal Ballast Resistor
LT3081	1.5A, Single Resistor Rugged Linear Regulator with Monitors	Extended Safe Operating Area, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 34.5V, Current-Based Reference, Programmable Current Limit, Output Current and Temperature Monitors
LT3083	3A, Parallelable, Low Noise, Low Dropout Linear Regulator	310mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 23V, V_{OUT}: 0V to 22.6V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, DD-Pak, TSSOP, 4mm × 4mm DFN-12 Packages
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; MS8E and 2mm × 3mm DFN-6 Packages

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