

FEATURES

- Fully Enhances N-Channel Power MOSFETs
- 12 μ A Standby Current
- Operates at Supply Voltages from 9V to 24V
- Short Circuit Protection
- Easily Protected Against Supply Transients
- Controlled Switching ON and OFF Times
- No External Charge Pump Components
- Compatible With Standard Logic Families
- Available in 8-Pin SOIC

APPLICATIONS

- Solenoid Drivers
- DC Motor Drivers
- Stepper Motor Drivers
- Lamp Drivers/Dimmers
- Relay Drivers
- Low Frequency H-Bridge
- P-Channel Switch Replacement

DESCRIPTION

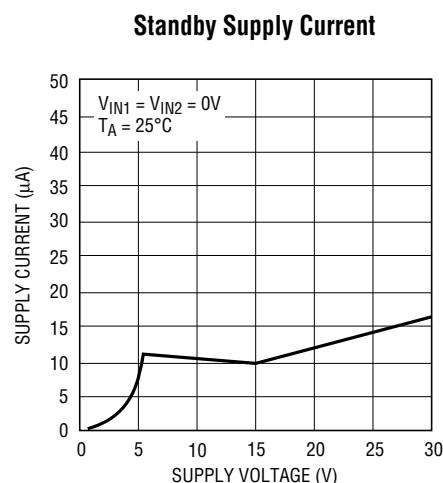
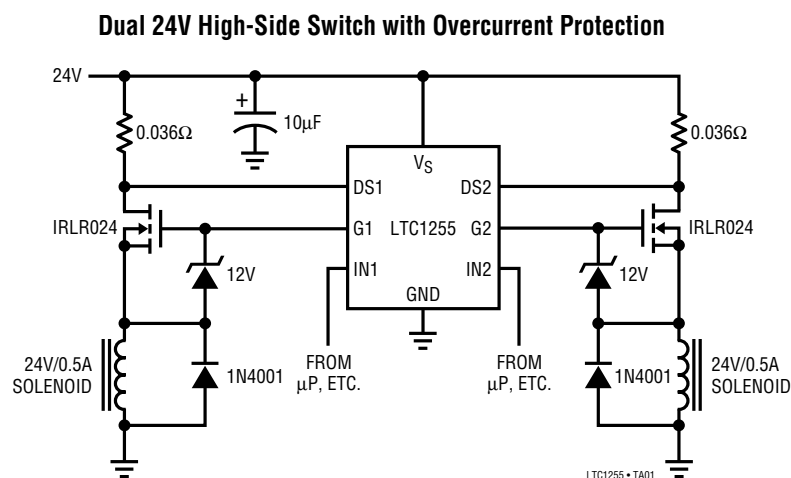
The LTC1255 dual high-side driver allows using low cost N-channel FETs for high-side industrial and automotive switching applications. An internal charge pump boosts the gate drive voltage above the positive rail, fully enhancing an N-channel MOS switch with no external components. Low power operation, with 12 μ A standby current, allows use in virtually all systems with maximum efficiency.

Included on-chip is independent overcurrent sensing to provide automatic shutdown in case of short circuits. A time delay can be added to the current sense to prevent false triggering on high in-rush current loads.

The LTC1255 operates from 9V to 24V supplies and is well suited for industrial and automotive applications.

The LTC1255 is available in both an 8-pin DIP and an 8-pin SOIC.

TYPICAL APPLICATION



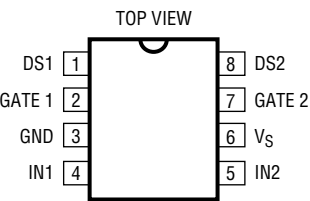
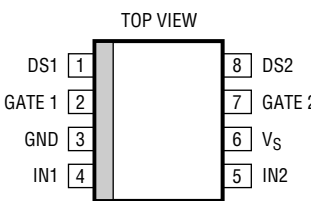
ABSOLUTE MAXIMUM RATINGS

Supply Voltage -0.3V to 30V
 Transient Supply Voltage ($< 10\text{ms}$) 40V
 Input Voltage $(V_S + 0.3\text{V})$ to $(\text{GND} - 0.3\text{V})$
 Gate Voltage $(V_S + 20\text{V})$ to $(\text{GND} - 0.3\text{V})$
 Current (Any Pin) 50mA

Operating Temperature Range

LTC1255C 0°C to 70°C
 LTC1255I -40°C to 85°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

| | | | |
|---|-------------------|---|-------------------|
|  <p>N8 PACKAGE 8-LEAD PLASTIC DIP $T_{J\text{MAX}} = 100^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$</p> | ORDER PART NUMBER |  <p>S8 PACKAGE 8-LEAD PLASTIC SOIC $T_{J\text{MAX}} = 100^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$</p> | ORDER PART NUMBER |
| | LTC1255CN8 | | LTC1255CS8 |
| | LTC1255IN8 | | LTC1255IS8 |
| | | | S8 PART MARKING |
| | | | 1255 |
| | | | 1255I |

ELECTRICAL CHARACTERISTICS $V_S = 9\text{V}$ to 24V , $T_A = 25^\circ\text{C}$, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|-------------------------------|---|-----|-----|-----------|---------------|
| I_Q | Quiescent Current OFF | $V_S = 10\text{V}$, $V_{IN} = 0\text{V}$ (Note 1) | | 12 | 40 | μA |
| | | $V_S = 18\text{V}$, $V_{IN} = 0\text{V}$ (Note 1) | | 12 | 40 | μA |
| | | $V_S = 24\text{V}$, $V_{IN} = 0\text{V}$ (Note 1) | | 12 | 40 | μA |
| | | | | | | |
| | Quiescent Current ON | $V_S = 10\text{V}$, $V_{\text{GATE}} = 22\text{V}$, $V_{IN} = 5\text{V}$ (Note 2) | | 160 | 400 | μA |
| | | $V_S = 18\text{V}$, $V_{\text{GATE}} = 30\text{V}$, $V_{IN} = 5\text{V}$ (Note 2) | | 350 | 800 | μA |
| | | $V_S = 24\text{V}$, $V_{\text{GATE}} = 36\text{V}$, $V_{IN} = 5\text{V}$ (Note 2) | | 600 | 1200 | μA |
| | | | | | | |
| V_{INH} | Input High Voltage | | ● | 2 | | V |
| V_{INL} | Input Low Voltage | | ● | | 0.8 | V |
| I_{IN} | Input Current | $0\text{V} \leq V_{IN} \leq V_S$ | ● | | ± 1 | μA |
| C_{IN} | Input Capacitance | | | 5 | | pF |
| V_{SEN} | Drain Sense Threshold Voltage | | ● | 80 | 100 | mV |
| | | | ● | 75 | 100 | mV |
| I_{SEN} | Drain Sense Input Current | $0\text{V} \leq V_{SEN} \leq V_S$ | ● | | ± 0.1 | μA |
| $V_{\text{GATE}} - V_S$ | Gate Voltage Above Supply | $V_S = 9\text{V}$ | ● | 7.5 | 10.5 | V |
| I_{GATE} | Gate Output Drive Current | $V_S = 18\text{V}$, $V_{\text{GATE}} = 30\text{V}$ | ● | 5 | 20 | μA |
| | | $V_S = 24\text{V}$, $V_{\text{GATE}} = 36\text{V}$ | ● | 5 | 23 | μA |

ELECTRICAL CHARACTERISTICS $V_S = 9V$ to $24V$, $T_A = 25^\circ C$, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|-----------------------------|---|----------|------------|------------|--------------------|
| t_{ON} | Turn-ON Time | $V_S = 10V$, $C_{GATE} = 1000pF$ (Note 3) Time for $V_{GATE} > V_S + 2V$ Time for $V_{GATE} > V_S + 5V$ | 30 75 | 100 250 | 300 750 | μs μs |
| | | $V_S = 18V$, $C_{GATE} = 1000pF$ (Note 3) Time for $V_{GATE} > V_S + 5V$ Time for $V_{GATE} > V_S + 10V$ | 40 75 | 120 250 | 400 750 | μs μs |
| | | $V_S = 24V$, $C_{GATE} = 1000pF$ (Note 3) Time for $V_{GATE} > V_S + 10V$ | 50 | 180 | 500 | μs |
| t_{OFF} | Turn-OFF Time | $V_S = 10V$, $C_{GATE} = 1000pF$, (Note 3, 4) | 10 | 24 | 60 | μs |
| | | $V_S = 18V$, $C_{GATE} = 1000pF$, (Note 3, 4) | 10 | 21 | 60 | μs |
| | | $V_S = 24V$, $C_{GATE} = 1000pF$, (Note 3, 4) | 10 | 19 | 60 | μs |
| t_{SC} | Short-Circuit Turn-OFF Time | $V_S = 10V$, $C_{GATE} = 1000pF$, (Note 3, 4) | 5 | 16 | 30 | μs |
| | | $V_S = 18V$, $C_{GATE} = 1000pF$, (Note 3, 4) | 5 | 16 | 30 | μs |
| | | $V_S = 24V$, $C_{GATE} = 1000pF$, (Note 3, 4) | 5 | 16 | 30 | μs |

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Quiescent current OFF is for both channels in OFF condition.

Note 2: Quiescent current ON is per driver and is measured independently.

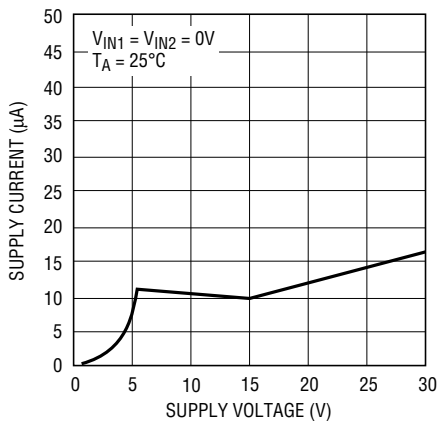
The gate voltage is clamped to 12V above the rail to simulate the effects of protection clamps connected across the GATE-SOURCE of the power MOSFET.

Note 3: Zener diode clamps must be connected across the GATE-SOURCE of the power MOSFET to limit V_{GS} . 1N5242A (through hole) or MMBZ5242A (surface mount) 12V Zener diodes are recommended. All Turn-ON and Turn-OFF tests are performed with a 12V Zener clamp in series with a small-signal diode connected between V_S and the GATE output to simulate the effects of a 12V protection Zener clamp connected across the GATE-SOURCE of the power MOSFET.

Note 4: Time for V_{GATE} to drop below 1V.

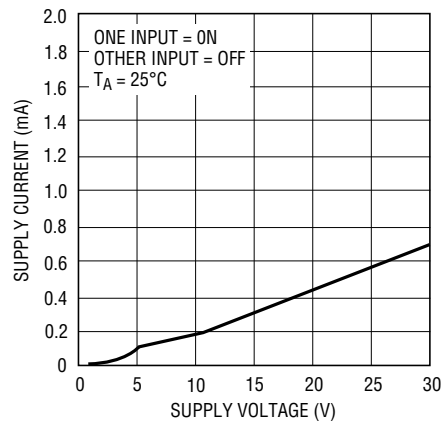
TYPICAL PERFORMANCE CHARACTERISTICS

Standby Supply Current



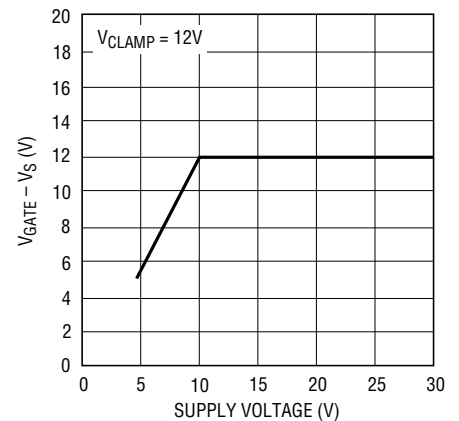
LTC1255 • TPC01

Supply Current per Driver (ON)



LTC1255 • TPC02

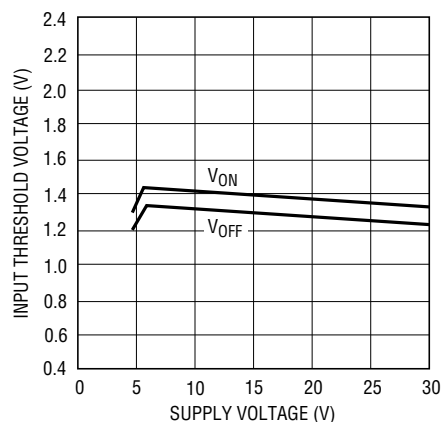
Gate Voltage Above Supply



LTC1255 • TPC03

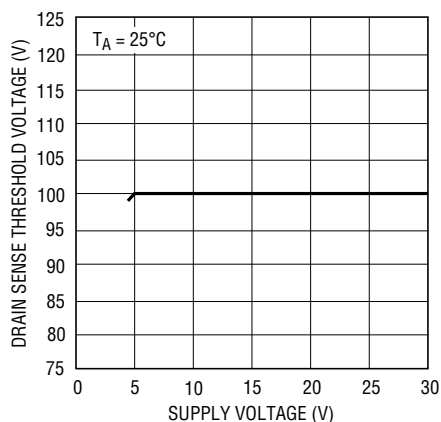
TYPICAL PERFORMANCE CHARACTERISTICS

Input Threshold Voltage



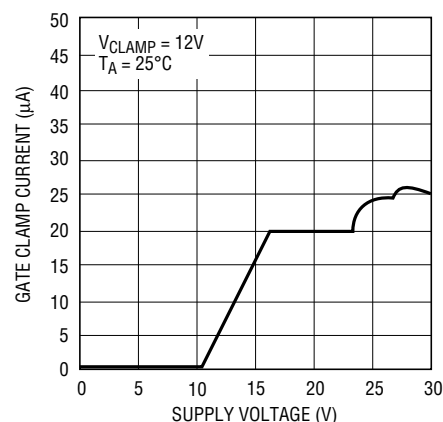
LTC1255 • TPC04

Drain Sense Threshold Voltage



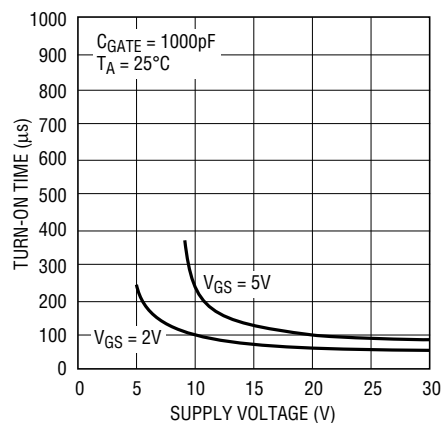
LTC1255 • TPC05

Gate Clamp Current



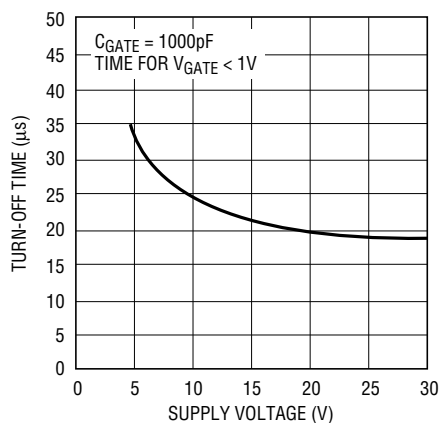
LTC1255 • TAO6

Turn-ON Time



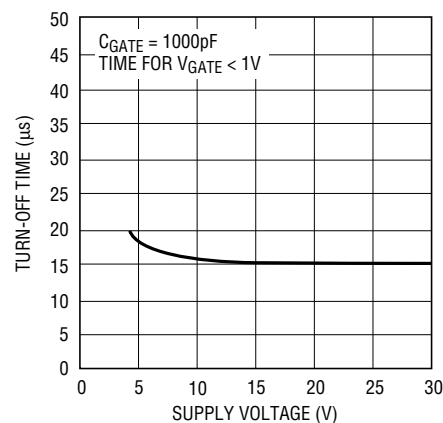
LTC1255 • TAO7

Turn-OFF Time



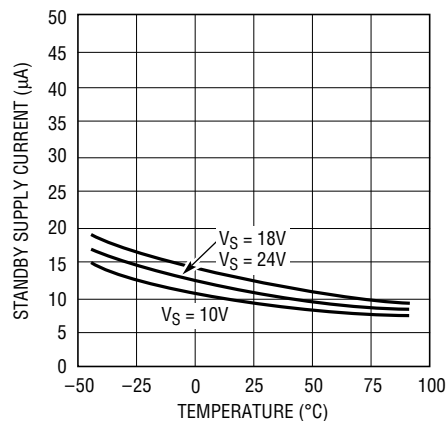
LTC1255 • TAO8

Short-Circuit Turn-OFF Delay Time



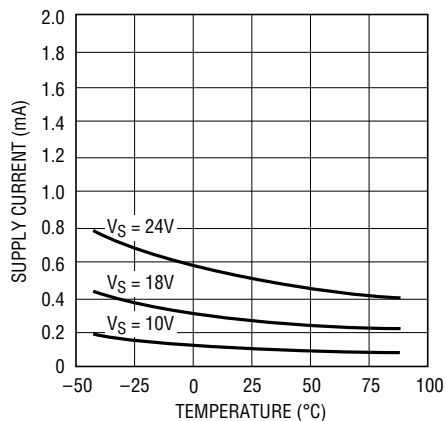
LTC1255 • TAO9

Standby Supply Current



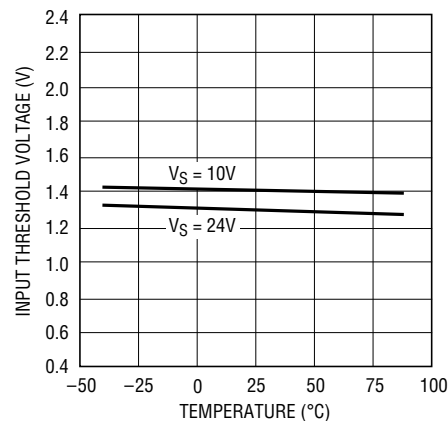
LTC1255 • TA10

Supply Current per Channel (ON)



LTC1255 • TA11

Input ON Threshold



LTC1255 • TA12

PIN FUNCTIONS

Input Pin

The LTC1255 input pin is active high and activates all of the protection and charge pump circuitry when switched ON. The LTC1255 logic and shutdown inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails. The input pin should be held low during the application of power to properly set the input latch.

Gate Drive Pin

The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is of relatively high impedance when driven above the rail (the equivalent of a few hundred k Ω). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

The supply pin of the LTC1255 serves two vital purposes. The first is obvious; it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious; it provides a Kelvin connection to the top of the drain sense resistor for the internal 100mV reference.

The supply pin of the LTC1255 should never be forced below ground as this may result in permanent damage to the device. A 100 Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

The LTC1255 is designed to be continuously powered so that the gate of the MOSFET is actively driven at all times. If it is necessary to remove power from the supply pin and then reapply it, the input pin should be cycled (low to high) a few milliseconds *after* the power is reapplied to reset the input latch and protection circuitry. Also, the input pin should be isolated from the controlling logic by a 10k resistor if there is a possibility that the input pin will be held high after the supply has been removed.

Drain Sense Pin

The drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will be reset and the MOSFET gate will be quickly discharged. Cycle the input to reset the short-circuit latch and turn the MOSFET back on.

This pin is also a high impedance CMOS gate with ESD protection and therefore should not be forced outside of the power supply rails. To defeat the overcurrent protection, short the drain sense pin to the supply pin.

Some loads, such as large supply capacitors, lamps or motors require high in-rush currents. An RC time delay can be added between the sense resistor and the drain sense pin to ensure that the drain sense circuitry does not false trigger during startup. This time constant can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET at risk of being destroyed by a short-circuit condition (see Applications Information section).

OPERATION

The LTC1255 is a dual 24V MOSFET driver with built-in protection and gate charge pump. The LTC1255 consists of the following functional blocks:

TTL and CMOS Compatible Inputs and Latches

The LTC1255 inputs have been designed to accommodate a wide range of logic families. Both input thresh-

olds are set at about 1.3V with approximately 100mV of hysteresis. A low standby current regulator provides continuous bias for the TTL-to-CMOS converter.

The input/protection latch should be set after initial power-up, or after reapplication of power, by cycling the input low to high.

OPERATION

Internal Voltage Regulation

The output of the TTL-to-CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the power MOSFET is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on-chip and therefore no external components are required to generate the gate drive. The charge pump is designed to drive a 12V Zener diode clamp connected across the gate and source of the MOSFET switch.

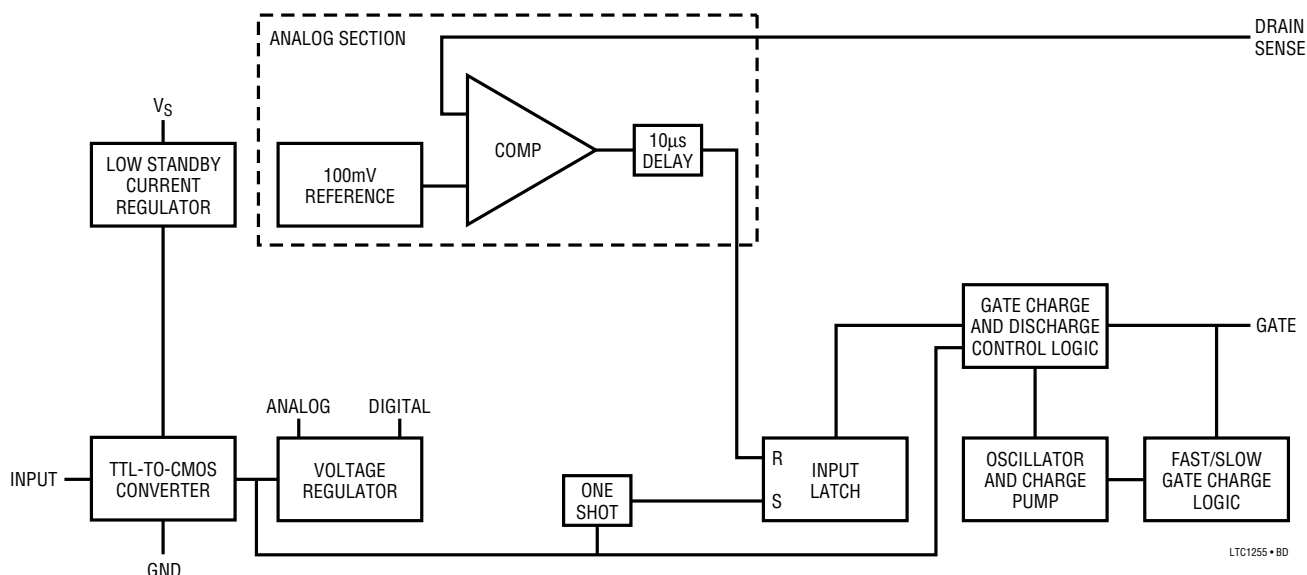
Drain Current Sense

The LTC1255 is configured to sense the current flowing into the drain of the power MOSFET in a high-side application. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.10Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged via a relatively large N-channel transistor.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions in normal operation. If a short circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.

BLOCK DIAGRAM (One Channel)



APPLICATIONS INFORMATION

MOSFET AND LOAD PROTECTION

The LTC1255 protects the power MOSFET switch by removing drive from the gate as soon as an overcurrent condition is detected. Resistive and inductive loads can be protected with no external time delay in series with the drain sense pin. Lamp loads, however, require that the overcurrent protection be delayed long enough to start the lamp but short enough to ensure the safety of the MOSFET.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The drain sense circuitry has a built-in delay of approximately 10 μ s to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to “mask” short load current transients and the starting of a small capacitor (< 1 μ F) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 1.

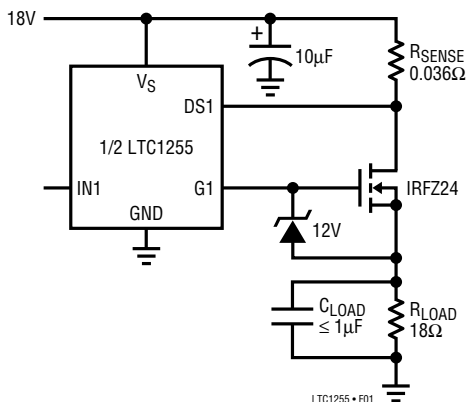


Figure 1. Protecting Resistive Loads

Inductive Loads

Loads that are primarily inductive, such as relays, solenoids and stepper motor windings, should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The built-in 10 μ s delay will ensure that the overcurrent protection is not false triggered by a supply or load transient. No external delay components are required as shown in Figure 2.

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load, as shown in Figure 2, to safely divert the stored energy.

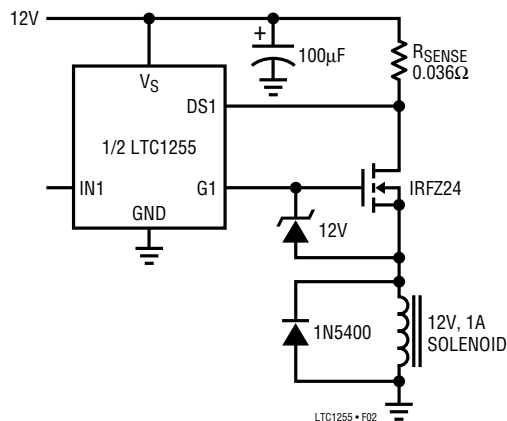


Figure 2. Protecting Inductive Loads

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 3. The gate drive to the power MOSFET is passed through an RC delay network, R1 and C1, which greatly reduces the turn-on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the startup current flowing into the supply capacitor(s) which, in turn, reduces supply transients and allows for slower activation

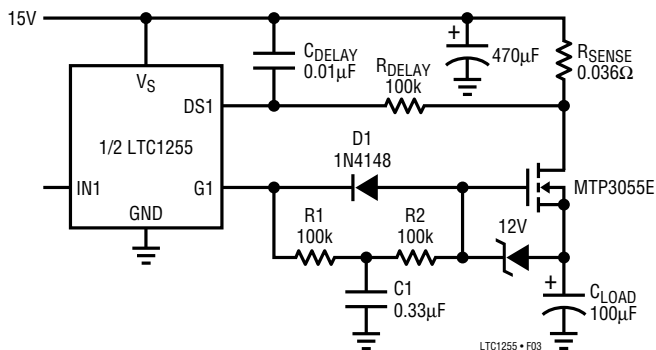


Figure 3. Powering Large Capacitive Loads

APPLICATIONS INFORMATION

of sensitive electrical loads. (Resistor R2, and the diode D1, provide a direct path for the LTC1255 protection circuitry to quickly discharge the gate in the event of an overcurrent condition.)

The RC network, R_{DELAY} and C_{DELAY} , in series with the drain sense input should be set to trip based on the expected characteristics of the load after startup, i.e., with this circuit, it is possible to power a large capacitive load and still react quickly to an overcurrent condition. The ramp rate at the output of the switch as it lifts off ground is approximately:

$$dV/dt = (V_{\text{GATE}} - V_{\text{TH}})/(R1 \times C1)$$

Therefore, the current flowing into the capacitor during startup is approximately:

$$I_{\text{STARTUP}} = C_{\text{LOAD}} \times dV/dt$$

Using the values shown in Figure 3, the startup current is less than 100mA and does not false trigger the drain sense circuitry which is set at 2.7A with a 1ms delay.

Lamp Loads

The in-rush current created by a lamp during turn-on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 4 shifts the current limit threshold up by a factor of 11:1 (to 30A) for a short period of time while the bulb is turned on. The current limit then drops down to 2.7A after the in-rush current has subsided.

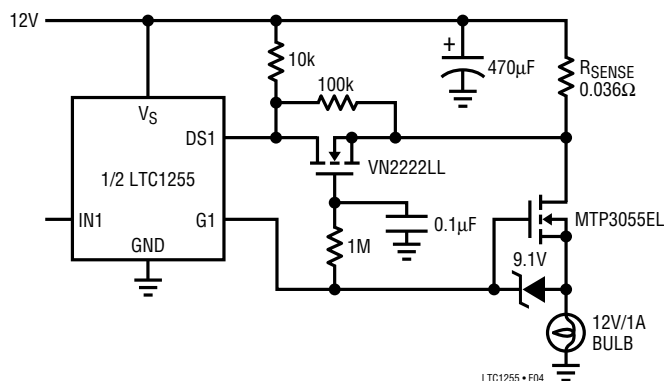


Figure 4. Lamp Driver With Delayed Protection

Selecting R_{DELAY} and C_{DELAY}

Figure 5 is a graph of normalized overcurrent shutdown time versus normalized MOSFET current. This graph is used to select the two delay components, R_{DELAY} and C_{DELAY} , which make up a simple RC delay between the drain sense input and the drain sense resistor.

The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the set current. (The set current is defined as the current required to develop 100mV across the drain sense resistor.)

Note that the shutdown time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the manufacturer for safe operation. (See MOSFET data sheet for further S.O.A. information.)

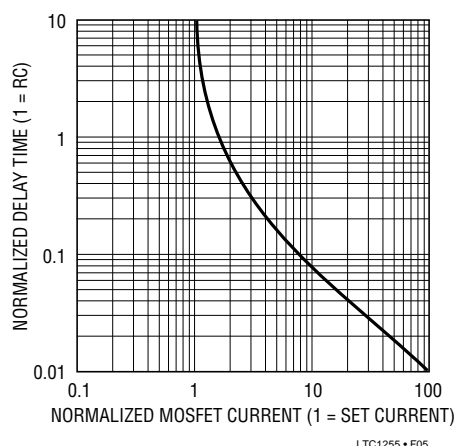


Figure 5. Normalized Delay Time vs MOSFET Current

Using a Speed-Up Diode

Another way to reduce the amount of time that the power MOSFET is in a short-circuit condition is to “bypass” the delay resistor with a small signal diode as shown in Figure 6. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the MOSFET is in an overload condition. The drain sense resistor value is selected to limit the maximum DC current to 4A.



Linear regulators with small output capacitors are the most difficult to protect as they can “switch” from a voltage mode to a current limited mode very quickly.



Because the LTC1255 is micropower in both the standby and ON state, the voltage drop across the supply filter is very small (typically $<6\text{mV}$) and does not significantly alter the accuracy of the drain sense threshold voltage which is typically 100mV .

The LTC1255 can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 8. The resistor limits the supply current to less than 120mA with -12V applied. Since the LTC1255 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 5V μP (or controlling logic) is protected by the 10k resistors in series with the input.



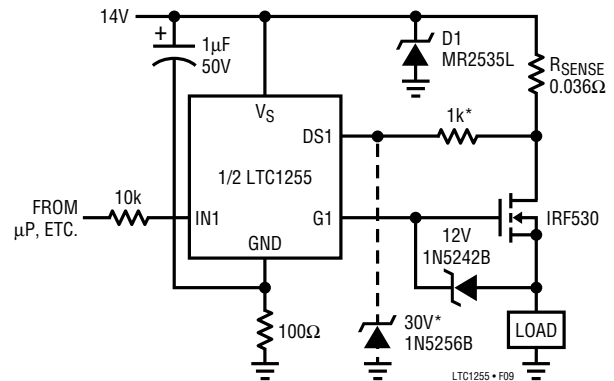
A common scheme used to limit overvoltage transients on a 14V nominal automotive power bus is to clamp the supply to the module containing the high-side MOSFET switches with a large transient suppressor diode, D1 in Figure 9. This diode limits the supply voltage to 40V under worse case conditions. The LTC1255 is designed to survive short (10ms) 40V transients and return to normal operation after the transient has passed.

APPLICATIONS INFORMATION

The switches can either be turned OFF by the controlling logic during these transients or latched OFF above 30V by holding the drain sense pin low as shown in Figure 9.

Switch status can be ascertained by means of an XNOR gate connected to the input and switch output through 100k current limiting resistors (see Typical Applications section for more detail on this scheme). The switch is reset after the overvoltage event by cycling the input low and then high again.

The power MOSFET switch should be selected to have a breakdown voltage sufficiently higher than the 40V supply clamp voltage to ensure that no current is conducted to the load during the transient.

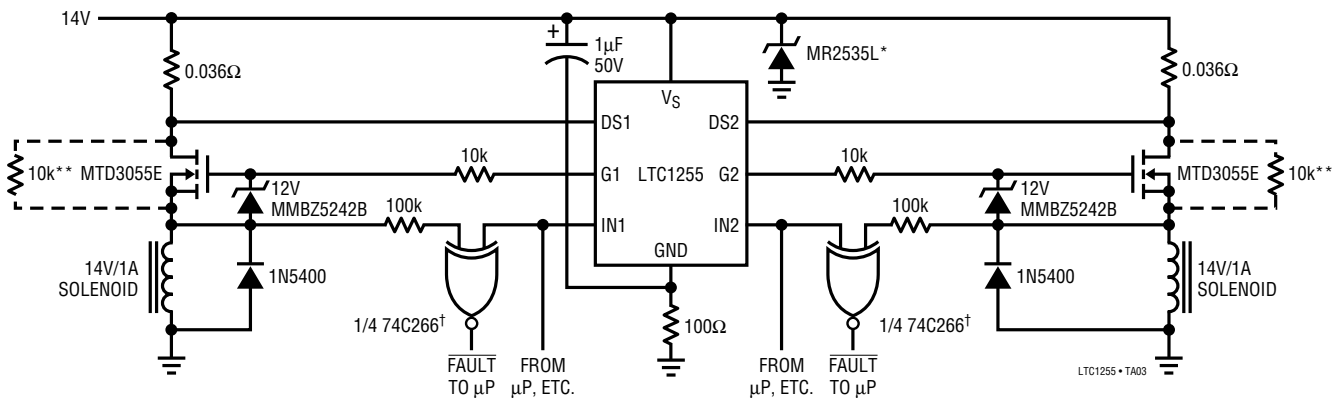


*OPTIONAL OVERVOLTAGE (30V) LATCH-OFF COMPONENTS

Figure 9. Overvoltage Transient Protection

TYPICAL APPLICATIONS

Dual Automotive High-Side Switch with Overvoltage Protection, XNOR Status and 12μA Standby Current



TRUTH TABLE

| IN | OUT | CONDITION | FAULT |
|----|-----|-------------|-------|
| 0 | 0 | SWITCH OFF | 1 |
| 1 | 0 | OVERCURRENT | 0 |
| 0 | 1 | OPEN LOAD** | 0 |
| 1 | 1 | SWITCH ON | 1 |

* LIMITS V_S TRANSIENTS TO <40V. SEE MANUFACTURER DATA SHEET FOR FURTHER DETAIL.

** OPTIONAL OPEN LOAD DETECTION REQUIRES 10k PULL-UP RESISTORS. (ULTRA LOW STANDBY QUIESCENT CURRENT IS SACRIFICED)

† POWER FROM 5V LOGIC SUPPLY.

The schematic diagram illustrates a battery-powered system. It features a 18V to 30V battery pack connected to a 9.1V MMBZ5239BL diode and an IN5400 diode. The 9.1V diode is connected to a 10k resistor, which is in series with a 2N2222 transistor. The transistor's base is connected to a 10k resistor, and its emitter is grounded. The collector is connected to the V_{LOGIC} pin of a microcontroller (μP OR CONTROL LOGIC). The microcontroller's V_{LOGIC} pin is also connected to a 100k resistor, which is in series with a 10k resistor. The microcontroller's IN1 pin is connected to a 100k resistor, and its IN2 pin is connected to a 100k resistor. The microcontroller's GND pin is connected to ground. The V_S pin of the LTC1255 is connected to the 9.1V MMBZ5239BL diode. The G1 pin of the LTC1255 is connected to a 0.033Ω resistor, which is in series with a 0.22μF capacitor. The G2 pin of the LTC1255 is connected to a 1N4148 diode. The output of the LTC1255 is connected to a 100k resistor, which is in series with a 1k resistor. The output of the 1k resistor is connected to the gate of an MTD3055EL MOSFET. The MOSFET's source is connected to ground, and its drain is connected to the V_{OUT} pin of a HIGH[†] EFFICIENCY SWITCHING REGULATOR. The regulator's V_{IN} pin is connected to a 12V MMBZ5242BL diode. The regulator's output is connected to a 100μF capacitor. The regulator's output is also connected to a 5V/1A (SWITCHED) output. The regulator's output is connected to a 100μF capacitor. The regulator's output is connected to a 5V/1A (SWITCHED) output. The regulator's output is connected to a 5V/1A (SWITCHED) output.

*OPTIONAL 3A OVERCURRENT SHUTDOWN
[†]SEE LTC1149 DATA SHEET FOR CIRCUIT DETAILS

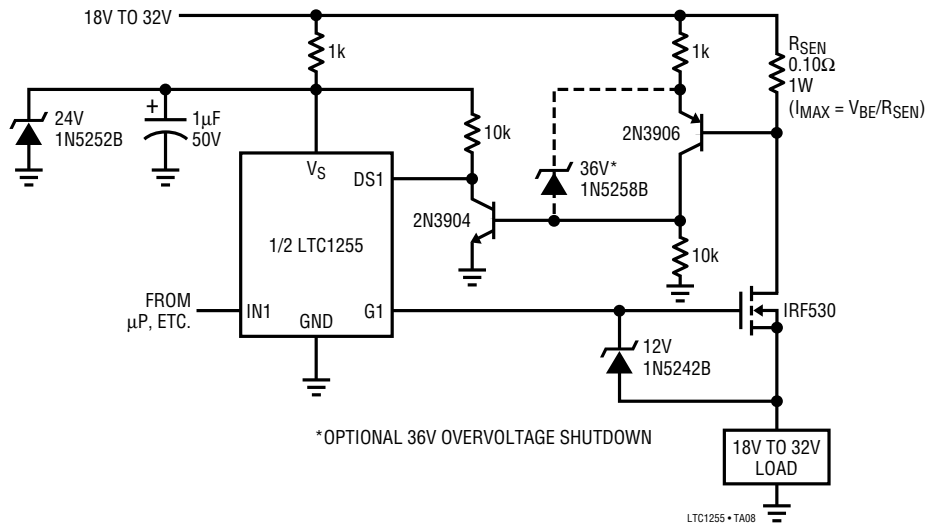
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The circuit diagram illustrates a motor speed controller. It features a 14V power supply connected to a 10μF 50V electrolytic capacitor and a 0.1μF 50V ceramic capacitor. The power supply is also connected to a 0.01Ω sense resistor. The control input section includes a 1N4148 diode, a 60k resistor, and a 30k resistor, with a 15k resistor and a 1k resistor connected to the LMC555 timer. The LMC555 timer is configured with its 1 pin to ground, 2 pin to a 0.01μF capacitor, 5 pin to ground, 6 pin to a 0.1μF capacitor, and 8 pin to the 14V supply. The timer's output (pin 3) drives the gate of an N-channel MOSFET (IRFR024) through a 100kΩ resistor. The MOSFET's source is connected to ground, and its drain is connected to the motor. The motor is represented by a circle with a plus sign and a 14V label. The MOSFET is protected by a 22V MMBZ5251BL Zener diode. The LTC1255 MOSFET driver is connected with its VS pin to the 14V supply, its IN1 pin to the LMC555 output, and its IN2 pin to ground. The driver's G1 pin is connected to the MOSFET gate, and its G2 pin is connected to ground. The driver's DS1 and DS2 pins are connected to the 14V supply and ground, respectively. The driver is protected by a 22V MMBZ5251BL Zener diode. The motor is connected to the 14V supply through a 0.01Ω sense resistor.

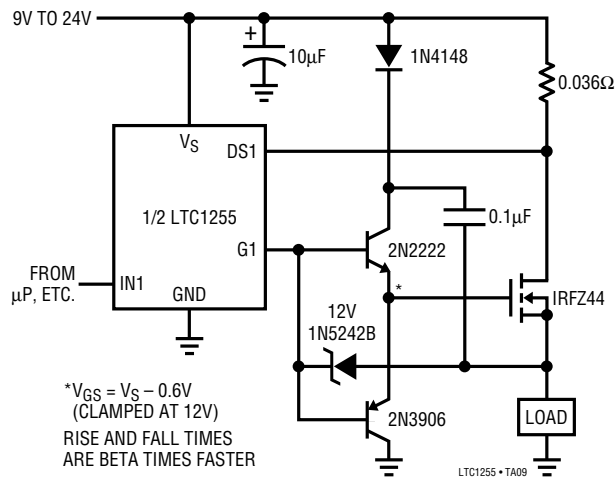
The circuit diagram shows a 14V LED driver. It starts with a 14V input. A pulse width adjust section uses an LMC555 timer, controlled by a 5.6V source and a 100k potentiometer. The LMC555 output drives the gate of an LTC1255 MOSFET. The MOSFET's source is grounded, and its drain is connected to a 14V LED load. The circuit includes various passive components like capacitors (10µF, 0.1µF, 0.01µF) and resistors (9.1k, 100k, 30k, 100k, 0.05Ω, 100Ω, 1k). Diodes include MR2535L, 1N4148, and MMBZ5242B. A 12V LED load is also shown. The circuit is powered by a 14V source and includes a 5.6V reference voltage.

TYPICAL APPLICATIONS

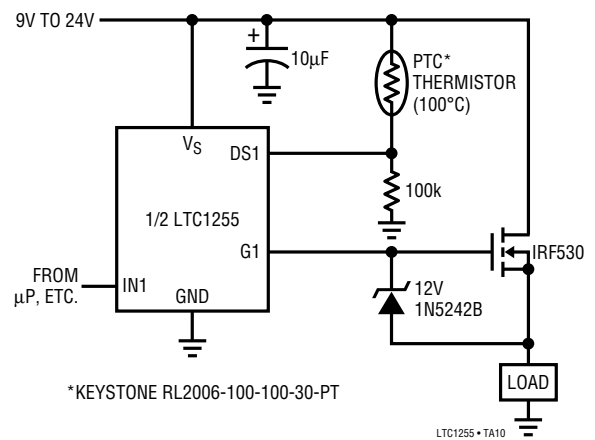
18V to 32V Operation with Overcurrent Shutdown and Optional Overvoltage Shutdown



Bootstrapped Gate Driver ($100\text{Hz} < f_0 < 10\text{kHz}$)

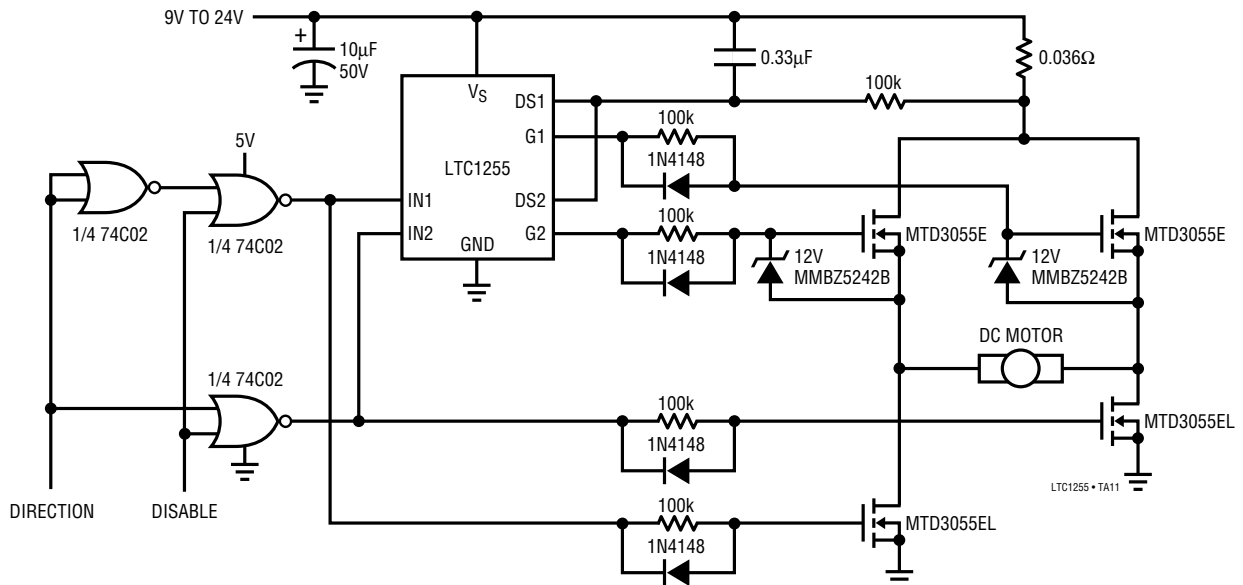


High-Side Switch with Thermal Shutdown (PTC Thermistor)

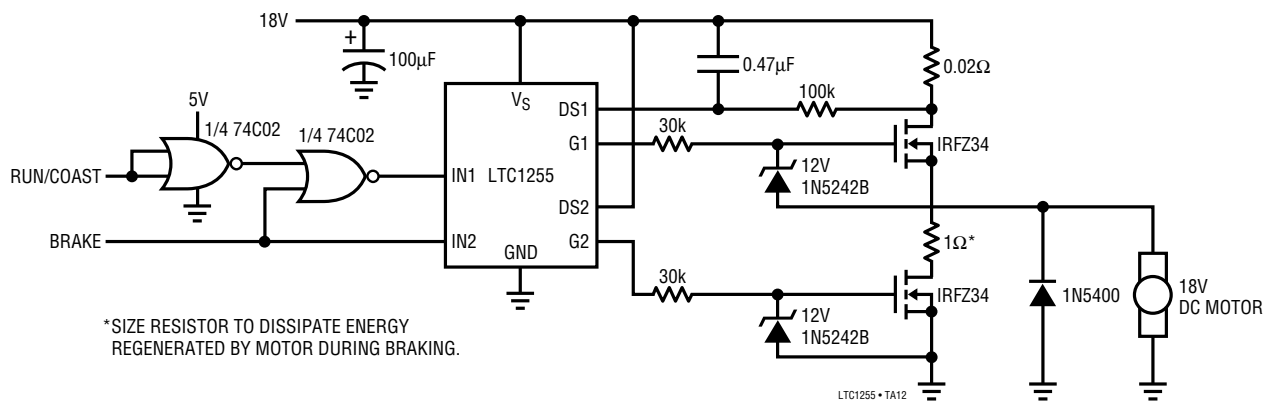


TYPICAL APPLICATIONS

**H-Bridge DC Motor Driver
(Direction and ON/OFF Control)**



**High-Side DC Motor Driver With Electronic Braking and
Stalled Motor Shutdown**



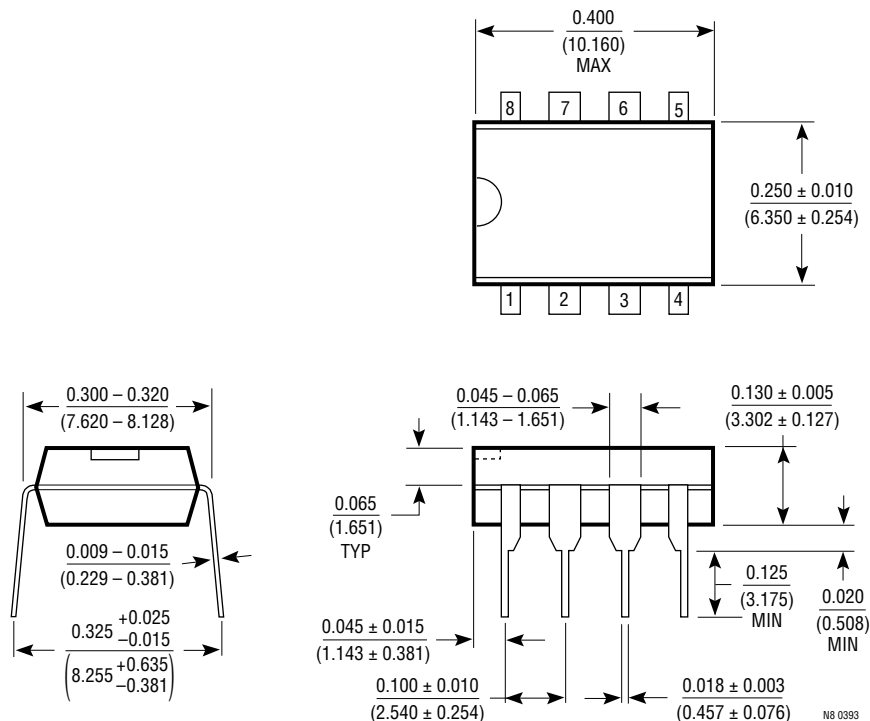


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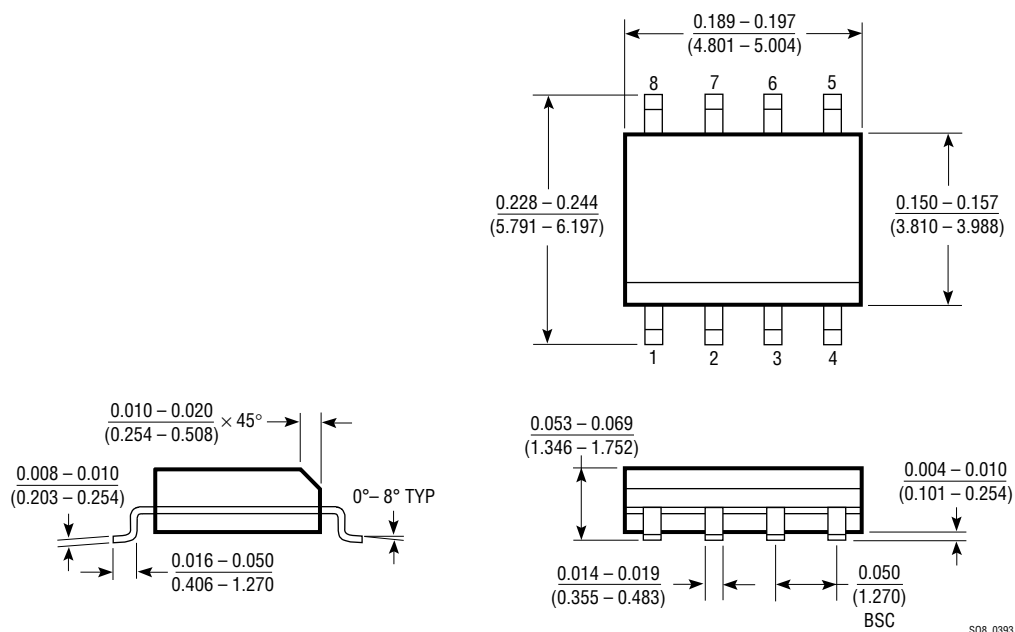
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead Plastic DIP



S8 Package 8-Lead SOIC



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