0.1 GHz to 24 GHz, Low Noise, Programmable Divider

Data Sheet **HMC862A**

FEATURES

- Low noise floor: −153 dBc/Hz at 100 kHz offset
- Programmable frequency divider (N)
  - N = 1, 2, 4, or 8
- Wide bandwidth: 0.1 GHz to 24 GHz
- Low current consumption: 81 mA in the N = 8 divide state
- HBM ESD sensitivity, Class 2 classification
- FICDM ESD sensitivity, Class C3 classification
- 16-lead, 3 mm × 3 mm LFCSP package: 9 mm²

APPLICATIONS

- Satellite communication systems
- Point to point and point to multipoint radios
- Military applications
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

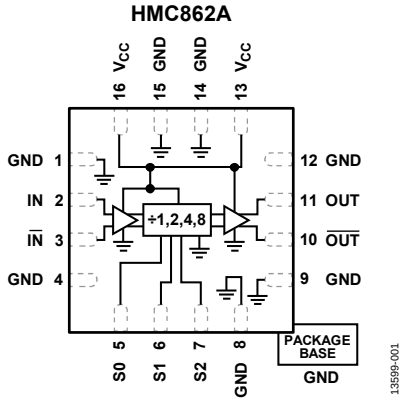

Figure 1.

GENERAL DESCRIPTION

The HMC862A is a low noise, programmable frequency divider in a 3 mm × 3 mm, leadless, surface-mount package. The frequency divider, N, can be programmed to divide from 1, 2, 4, or 8 in the 0.1 GHz to 24 GHz input frequency range.

The low phase noise, wide frequency range, and flexible division ratio make this device ideal for high performance and wideband communication systems.

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REVISION HISTORY

4/2019—Rev. 0 to Rev. A

Added Thermal Resistance Section and Table 4 ... 5
Changes to Theory of Operation Section ... 12
Changes to Ordering Guide ... 15

10/2017—Revision 0: Initial Version

SPECIFICATIONS

RF SPECIFICATIONS

V_{CC} = 5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT CHARACTERISTICS					
RF Input Frequency					
Maximum	Sine wave or square wave input				
N = 1		18			GHz
N = 2, 4, 8		24			GHz
Minimum	Square wave input[1]			0.1	GHz
RF Input Power Range					
N = 1, 2	0.1 GHz< f_{IN} < 18 GHz, sine or square wave input[1]	−15		+10	dBm
N = 2	18 GHz < f_{IN} < 24 GHz, sine or square wave input	−5		+10	dBm
N = 4, 8	0.1 GHz < f_{IN} < 20 GHz, sine or square wave input[1]	−15		+10	dBm
	20 GHz < f_{IN} < 24 GHz, sine or square wave input	−5		+10	dBm
Reverse Leakage					
N = 1	f_{IN} = 6 GHz, input power (P_{IN}) = 0 dBm		−10		dBm
N = 2	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−55		dBm
N = 4, 8	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−70		dBm
RF OUTPUT CHARACTERISTICS, N = 1					
Output Power, Single-Ended	0.1 GHz < f_{IN} < 10 GHz	−1	+3	+5	dBm
	10 GHz < f_{IN} < 15 GHz	−5	−2	+3	dBm
	15 GHz < f_{IN} < 18 GHz	−11	−6	0	dBm
Single-Sideband (SSB) Residual Phase Noise at 100 kHz Offset	f_{IN} = 12 GHz, P_{IN} = 5 dBm		−155		dBc/Hz
Second Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−27		dBm
Third Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−6		dBm
RF OUTPUT CHARACTERISTICS, N = 2					
Output Power, Single-Ended	0.1 GHz < f_{IN} < 18 GHz	0	3	5	dBm
	18 GHz < f_{IN} < 24 GHz	−3	0	+3	dBm
SSB Residual Phase Noise at 100 kHz Offset	f_{IN} = 12 GHz, P_{IN} = 5 dBm		−153		dBc/Hz
Second Harmonic (Feedthrough)	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−28		dBm
Third Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−7		dBm
RF OUTPUT CHARACTERISTICS, N = 4					
Output Power, Single-Ended	0.1 GHz < f_{IN} < 18 GHz	0	2	4	dBm
	18 GHz < f_{IN} < 24 GHz	−1	+3	+6	dBm
SSB Residual Phase Noise at 100 kHz Offset	f_{IN} = 12 GHz, P_{IN} = 5 dBm		−154		dBc/Hz
Second Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−35		dBm
Third Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−6		dBm
RF OUTPUT CHARACTERISTICS, N = 8					
Output Power, Single-Ended	0.1 GHz < f_{IN} < 24 GHz	0	2	4	dBm
SSB Residual Phase Noise at 100 kHz Offset	f_{IN} = 12 GHz, P_{IN} = 5 dBm		−155		dBc/Hz
Second Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−45		dBm
Third Harmonic	f_{IN} = 6 GHz, P_{IN} = 0 dBm		−7		dBm

[1] A square wave input is recommended to be below 650 MHz for best phase noise performance. If a sine wave input below 650 MHz is used, it is recommended that the drive level be >5 dBm for best operation, including phase noise. Refer to the Typical Performance Characteristics section.

DC SPECIFICATIONS

V_{CC} = 5 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES					
V_{CC}	Analog supply	4.75	5	5.25	V
CURRENT CONSUMPTION, I_{CC}					
N = 1		55	61	71	mA
N = 2		64	73	84	mA
N = 4		68	78	90	mA
N = 8		71	81	94	mA
DIGITAL INPUT S (S0, S1, S2)					
Logic Voltage					
Low		0		0.4	V
High		3		5	V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
RF Input Power (IN, $\overline{IN}$)	13 dBm
Supply Voltage (V_{CC})	5.5 V
Logic Inputs (S0, S1, S2)	−0.5 V to (0.5 V + V_{CC})
Storage Temperature Range	−65°C to +125°C
Reflow Temperature	260°C
Operating Temperature Range (T_A)	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM), JS-001-2012	Class 2
Field Induced Charged Device Model (FICDM), JS-002	Class C3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal impedance simulated values are based on the use of the EV1HMC862ALP3 evaluation board with the exposed pad soldered to GND. V_{CC} = 5 V and Divider Ratio (N) = 8.

Table 4.

Package Type	Thermal Impedance (θ_{JB})	Unit
HCP-16-1	34	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

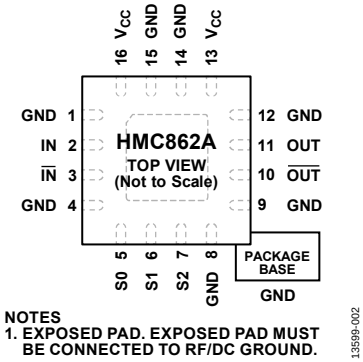


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 8, 9, 12, 14, 15	GND	Ground. The backside of the package has an exposed metal ground slug that must be connected to RF/dc ground.
2	IN	RF Input. This pin must be dc blocked.
3	$\overline{IN}$	RF Input, 180° Out of Phase with Pin 2 for Differential Operation. This pin must be ac grounded for single-ended operation. DC block this pin for differential operation.
5, 6, 7	S0, S1, S2	CMOS Compatible Division Ratio Control Bits. See Table 6.
10	$\overline{OUT}$	Divider Output, 180° Out of Phase with Pin 11. This RF output must be dc blocked. See Figure 31 for proper termination.
11	OUT	Divided Output. This RF output must be dc blocked. See Figure 31 for proper termination.
13, 16	V_{CC}	Supply Voltage Pins, 5 V. Connect both V_{CC} pins to a 5 V supply. These pins are internally connected.
	EPAD	Exposed Pad. Exposed pad must be connected to RF/dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

DIVIDE BY 1

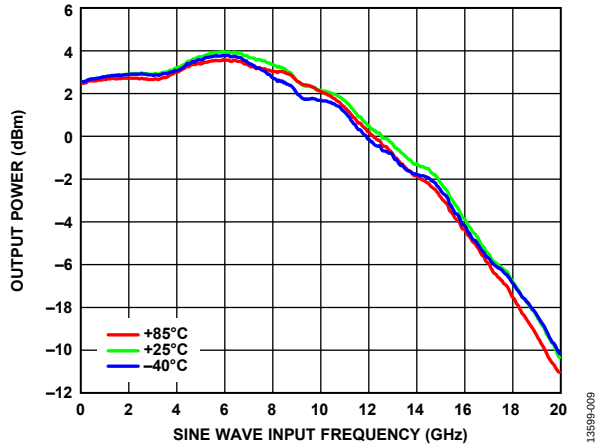


Figure 3. Output Power vs. Sine Wave Input Frequency for Various Temperatures, P_{IN} = 0 dBm

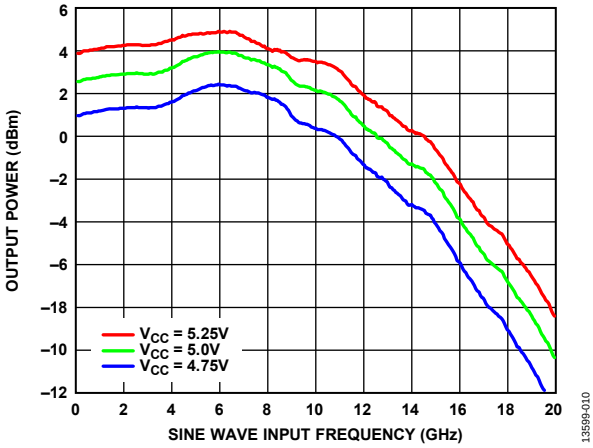


Figure 6. Output Power vs. Sine Wave Input Frequency for Various V_{CC} Voltages, P_{IN} = 0 dBm

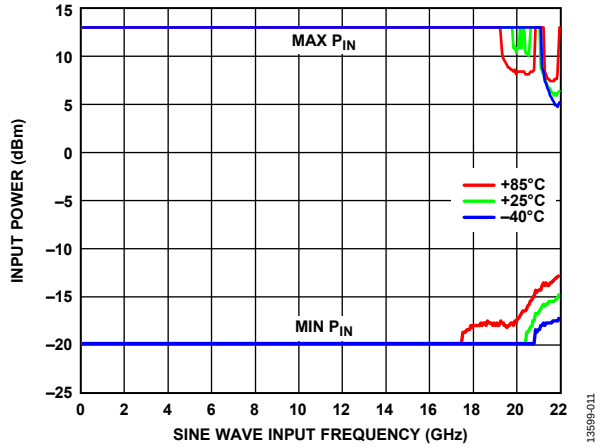


Figure 4. Allowable Range of Input Power vs. Sine Wave Input Frequency for Various Temperatures

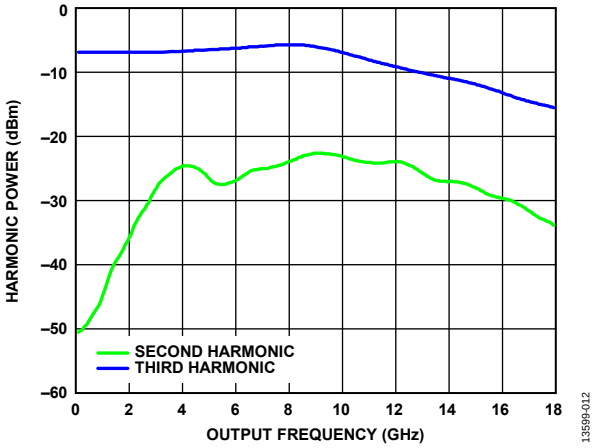


Figure 7. Output Harmonics, P_{IN} = 0 dBm, T_A = 25°C

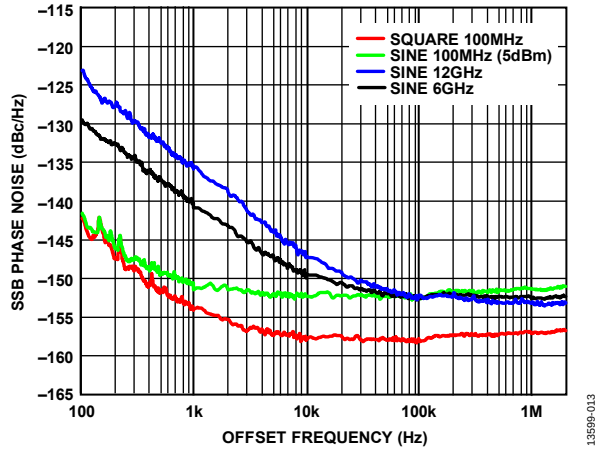


Figure 5. SSB Phase Noise vs. Offset Frequency for Various Input Frequencies, P_{IN} = 0 dBm, T_A = 25°C

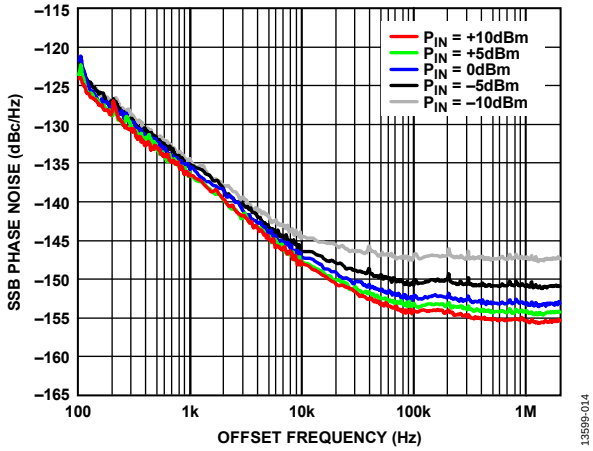


Figure 8. SSB Phase Noise vs. Offset Frequency for Various Input Power (P_{IN}) Levels, f_{IN} = 12 GHz Sine Wave, T_A = 25°C

DIVIDE BY 2

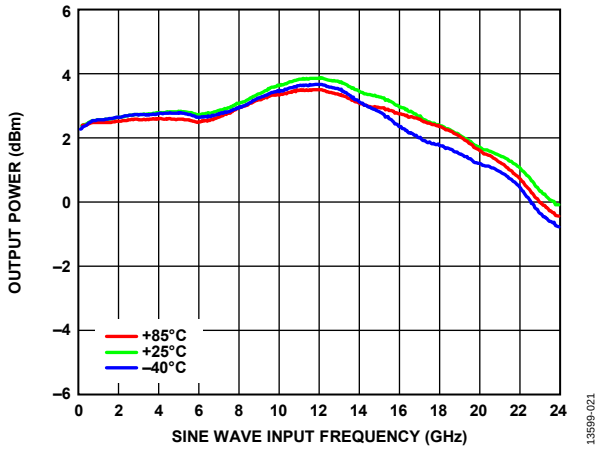


Figure 9. Output Power vs. Sine Wave Input Frequency for Various Temperatures, P_{IN} = 0 dBm

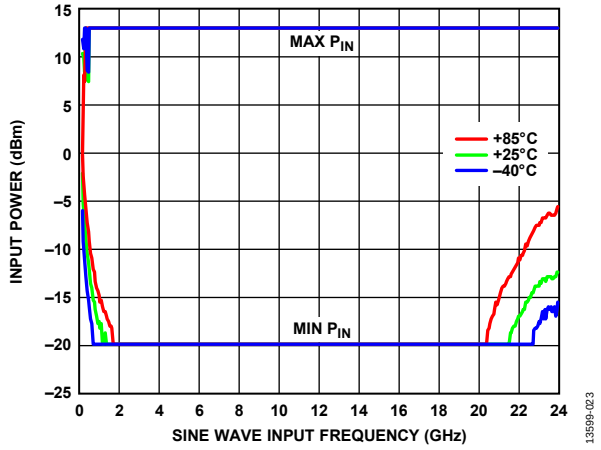


Figure 10. Allowable Range of Input Power vs. Sine Wave Input Frequency for Various Temperatures

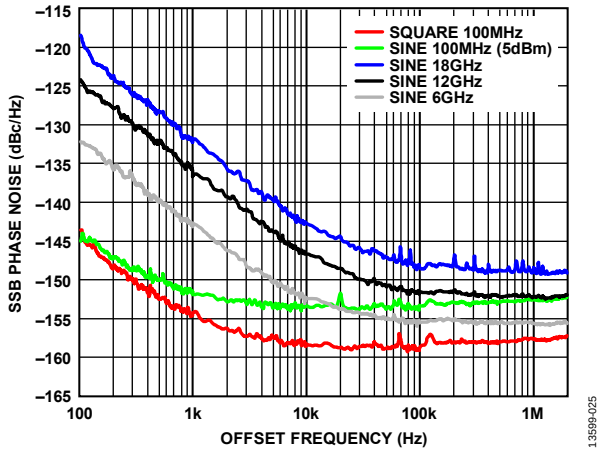


Figure 11. SSB Phase Noise vs. Offset Frequency for Various Input Frequencies, P_{IN} = 0 dBm, T_A = 25°C

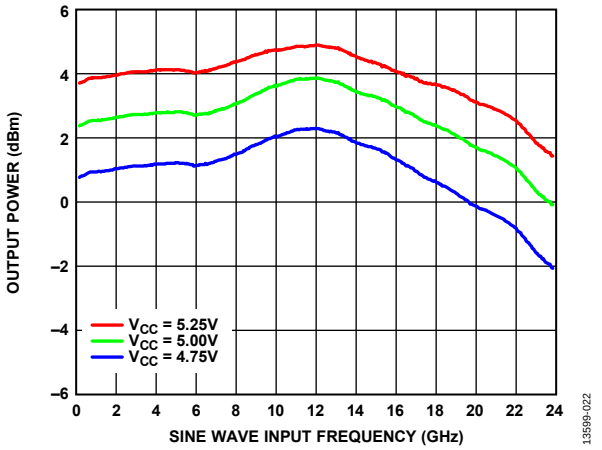


Figure 12. Output Power vs. Sine Wave Input Frequency for Various V_{CC} Voltages, P_{IN} = 0 dBm

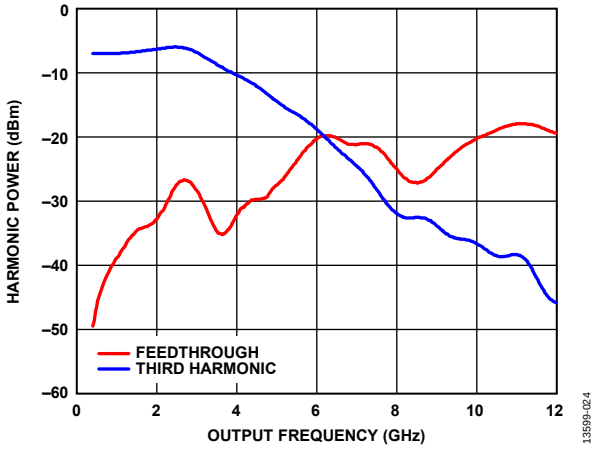


Figure 13. Output Harmonics, P_{IN} = 0 dBm, T_A = 25°C

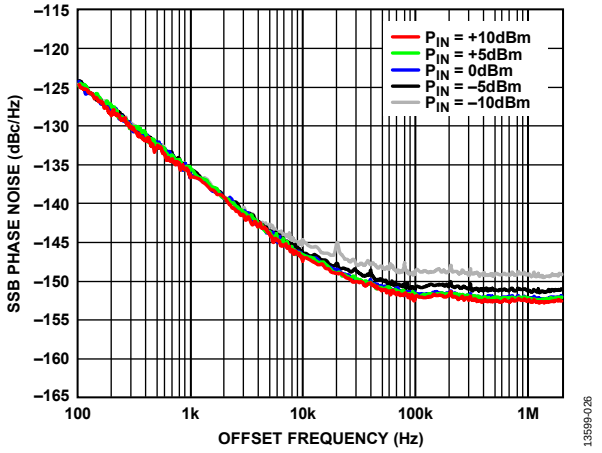


Figure 14. SSB Phase Noise vs. Offset Frequency for Various Input Power (P_{IN}) Levels, f_{IN} = 12 GHz Sine Wave, T_A = 25°C

DIVIDE BY 4

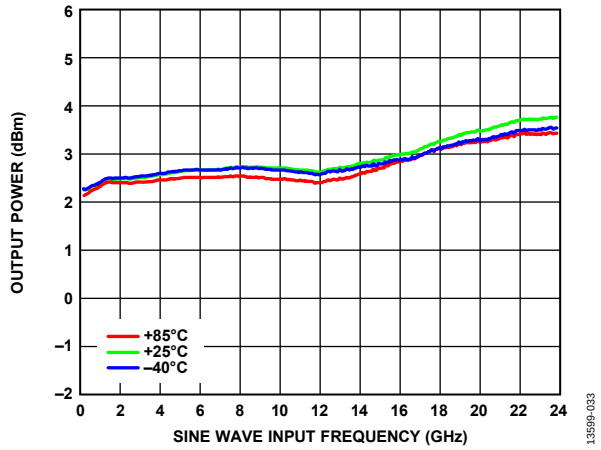


Figure 15. Output Power vs. Sine Wave Input Frequency for Various Temperatures, P_{IN} = 0 dBm

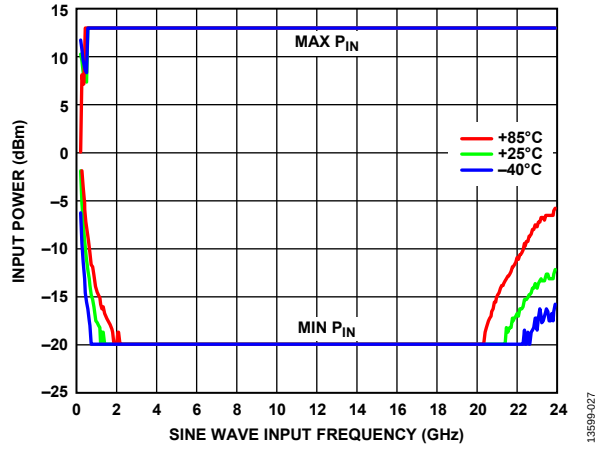


Figure 16. Allowable Range of Input Power vs. Sine Wave Input Frequency for Various Temperatures

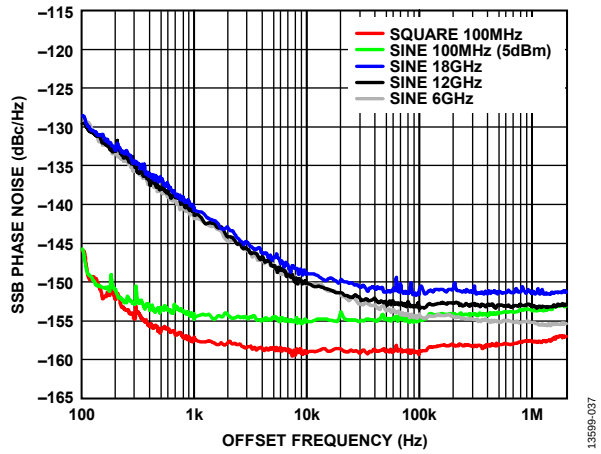


Figure 17. SSB Phase Noise vs. Offset Frequency for Various Input Frequencies, P_{IN} = 0 dBm, T_A = 25°C

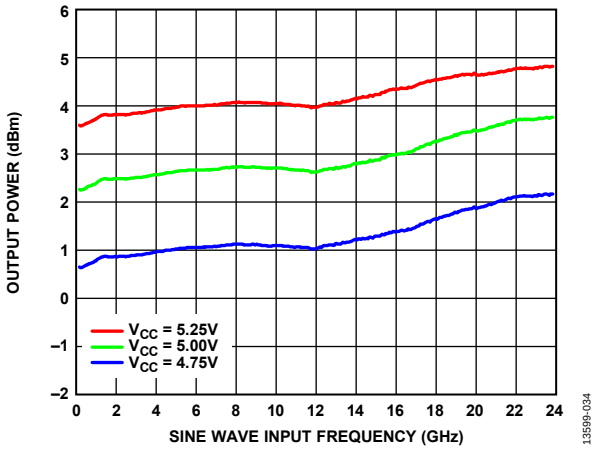


Figure 18. Output Power vs. Sine Wave Input Frequency for Various V_{CC} Voltages, P_{IN} = 0 dBm

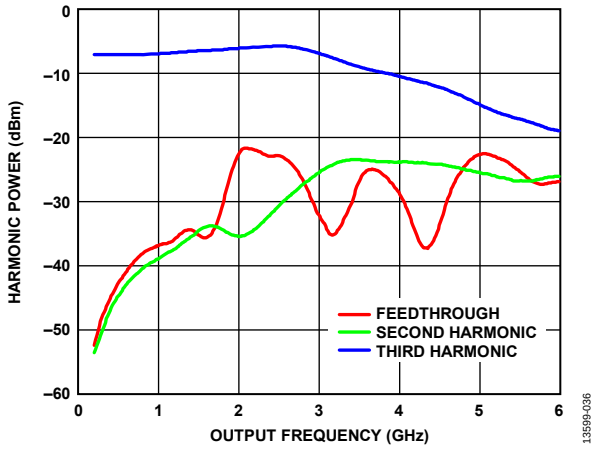


Figure 19. Output Harmonics, P_{IN} = 0 dBm, T_A = 25°C

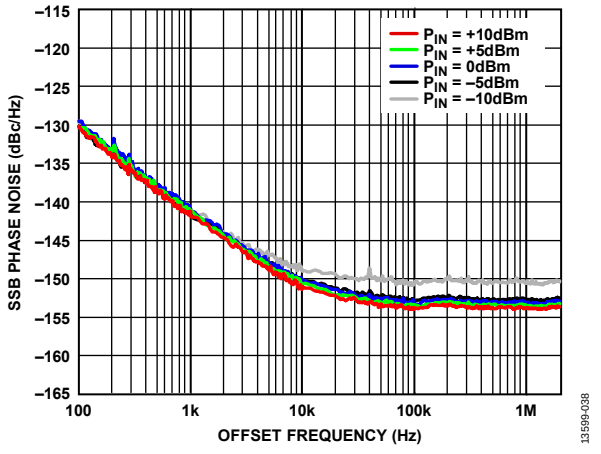


Figure 20. SSB Phase Noise vs. Offset Frequency for Various Input Power (P_{IN}) Levels, f_{IN} = 12 GHz Sine Wave, T_A = 25°C

DIVIDE BY 8

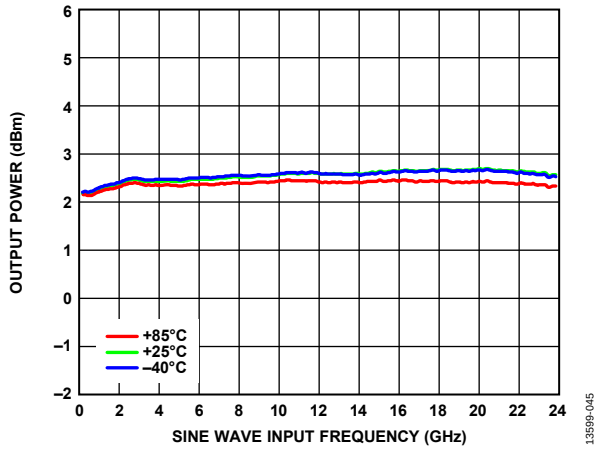


Figure 21. Output Power vs. Sine Wave Input Frequency for Various Temperatures, P_{IN} = 0 dBm

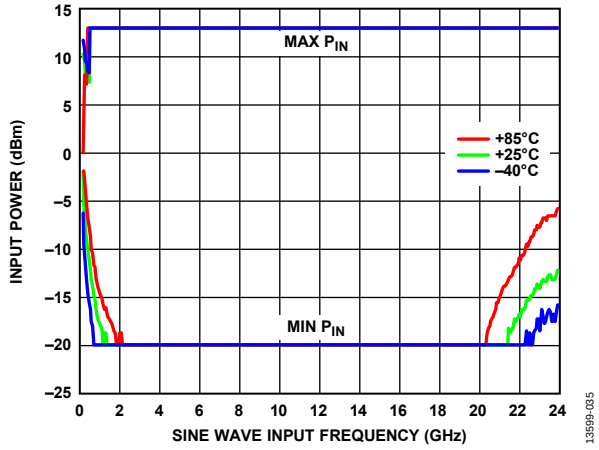


Figure 22. Allowable Range of Input Power vs. Sine Wave Input Frequency for Various Temperatures

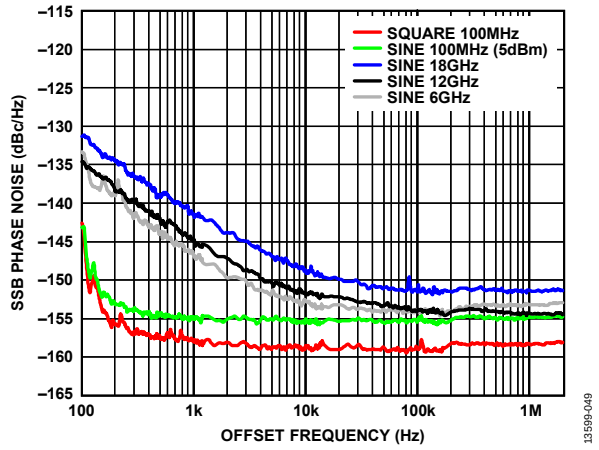


Figure 23. SSB Phase Noise vs. Offset Frequency for Various Input Frequencies, P_{IN} = 0 dBm, T_A = 25°C

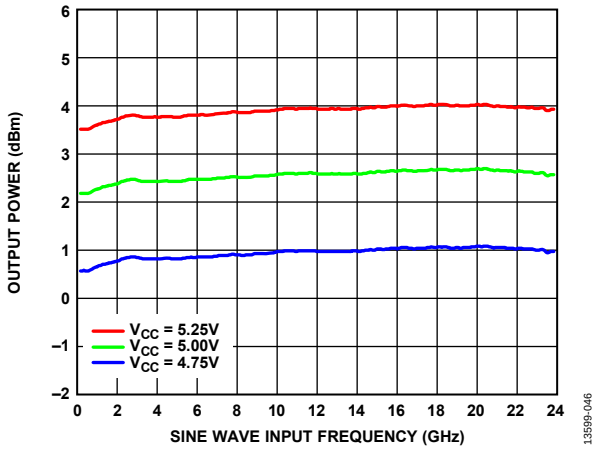


Figure 24. Output Power vs. Sine Wave Input Frequency for Various Vcc Voltages, P_{IN} = 0 dBm

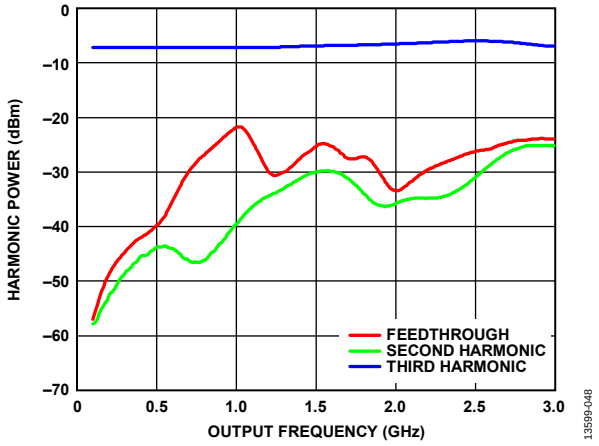


Figure 25. Output Harmonics, P_{IN} = 0 dBm, T_A = 25°C

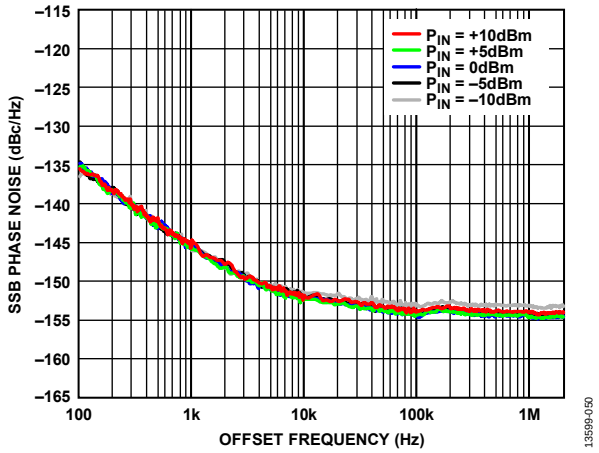


Figure 26. SSB Phase Noise vs. Offset Frequency for Various Input Power (P_{IN}) Levels, f_{IN} = 12 GHz Sine Wave, T_A = 25°C

CURRENT CONSUMPTION (I_{CC})

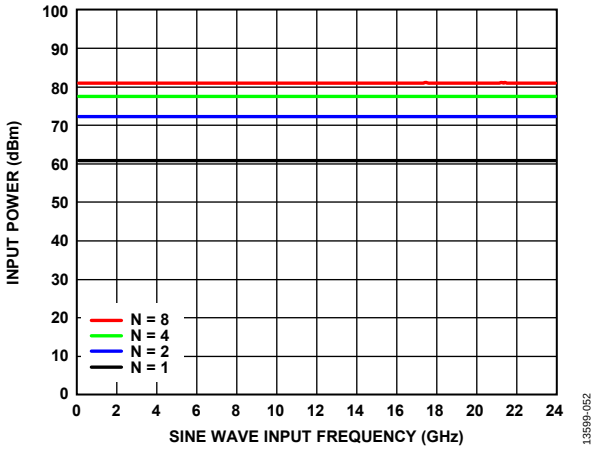


Figure 27. Input Power vs. Sine Wave Input Frequency

THEORY OF OPERATION

The HMC862A is a wideband, configurable RF divider with minimal additive phase noise.

The divide ratio, N, can be programmed to N = 1, 2, 4, or 8 by setting the digital input pins—S0, S1, and S2—to the logic high (1) or logic low (0) states indicated in Table 6.

Table 6. Programming Truth Table for Frequency Division Ratios[1]

S0	S1	S2	Divide Ratio (N)
0	0	0	1
1	0	0	2
1	1	0	4
1	1	1	8

[1] 0 means logic low and 1 means logic high.

The HMC862A does not support any other combination of the S0, S1, and S2 programming states other than those listed in Table 6. Using other programming states causes the HMC862A to generate an unstable output.

Enable the HMC862A by applying a voltage (V_{CC}) to the supply pins, V_{CC}. These pins are internally connected.

Note that the V_{CC} voltage must be applied before the logic level signals (S0, S1, and S2) can be driven to a logic high to prevent the ESD diodes from turning on.

The HMC862A toggles on the rising edge of the IN input for all divide ratios where N = 1, 2, 4, or 8.

INPUT INTERFACE

The HMC862A can be driven by differential or single-ended input signals, and can provide differential or single-ended output signals.

Figure 28 shows the input interface schematic for the IN and $\overline{IN}$ pins.

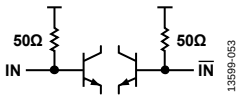


Figure 28. Input Interface Schematic

For differential input signals, ac couple the IN and $\overline{IN}$ pins as shown in Figure 29. Off-chip termination is not required because the IN and $\overline{IN}$ pins have internal 50 Ω termination resistors.

For single-ended input signals, ac couple the IN input. AC ground the $\overline{IN}$ pin as close to the $\overline{IN}$ pin as possible.

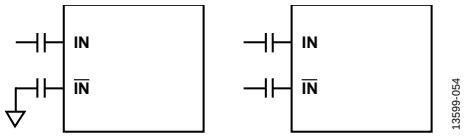


Figure 29. Recommended Input Configuration for Single-Ended Operation (Left) and Differential Operation (Right)

OUTPUT INTERFACE

Figure 30 shows the output interface schematic for the OUT and $\overline{OUT}$ pins.

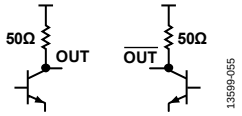


Figure 30. Output Interface Schematic

To provide a differential output or two single-ended outputs, ac couple the OUT and $\overline{OUT}$ pins. Off-chip termination is not required because the OUT and $\overline{OUT}$ pins have internal 50 Ω termination resistors.

If only one output pin is used, connect the unused output pin to ground through a capacitor and a 50 Ω termination

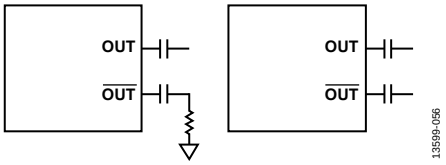


Figure 31. Recommended Output Configuration for Single-Ended Operation (Left) and Differential Operation (Right)

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD (PCB)

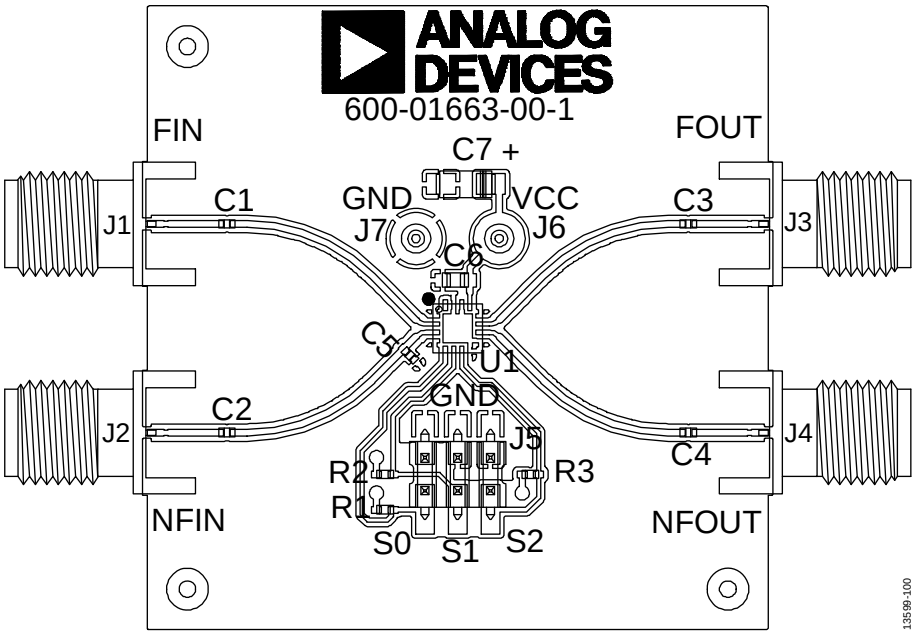


Figure 32. Evaluation PCB

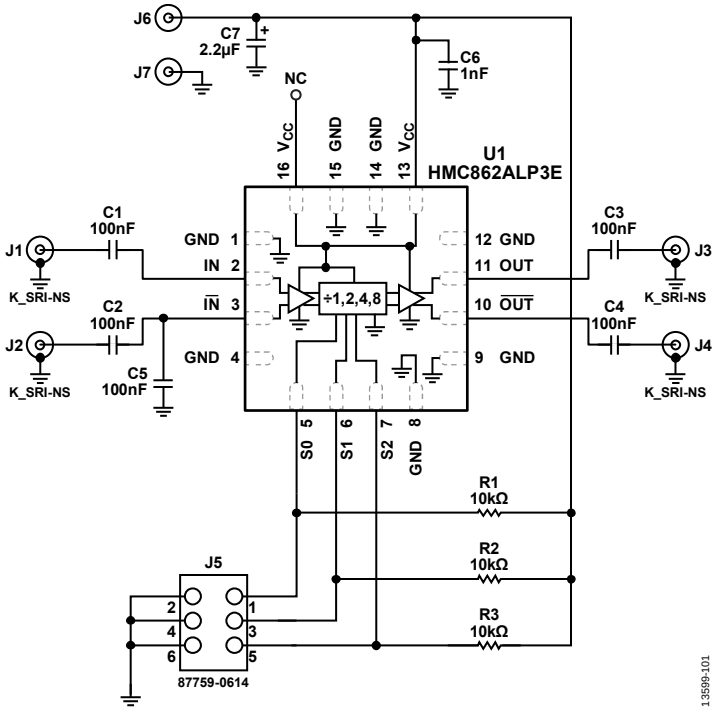


Figure 33. Evaluation PCB Schematic

EVALUATION BOARD OVERVIEW

Use the EV1HMC862ALP3 evaluation board to evaluate the HMC862A.

The HMC862A is enabled by applying 5 V between J6 (V_{CC}) and J7 (GND). Note that J6 only provides power to Pin 13 on the HMC862A; however, because Pin 13 and Pin 16 are internally connected, both V_{CC} pins receive power.

The divide ratio, N, is selected by inserting pin jumpers on Component J5, as shown in Table 7. When installed, a jumper pulls the digital input pin to ground and sets a logic low. When removed, the R1, R2, and R3 pull-up resistors pull the digital input to V_{CC} and set a logic high.

Table 7. Jumper Configuration for EV1HMC862ALP3

Divide Ratio (N)	S0 Jumper	S1 Jumper	S2 Jumper
1	Installed	Installed	Installed
2	Open	Installed	Installed
4	Open	Open	Installed
8	Open	Open	Open

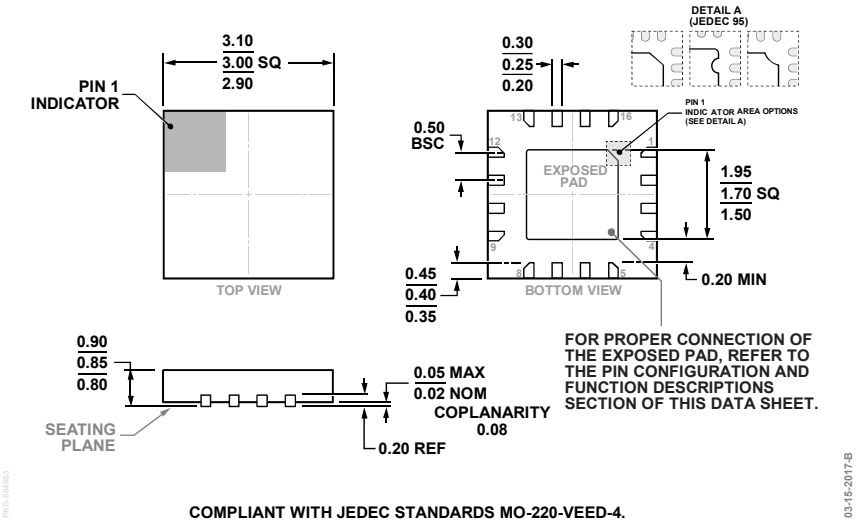
By default, the evaluation board is set up to accept a single-ended input and provide a differential output. A differential input can be used by removing Component C5; a single-ended output can be generated by terminating J4 with a 50 Ω termination.

It is recommended that the circuit board used in the application use RF circuit design techniques with a 50 Ω impedance on the signal lines and with the package ground leads and backside ground pad connected directly to the ground plane. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, Inc., upon request.

Table 8. List of Materials for EV1HMC862ALP3

Item	Description
J1 to J4	PCB-mount K connector
J5	DC connector header, Molex 2 mm
C1 to C5	ATC550L104KTT, 100 nF, 16 V, broadband capacitor, 0402 package
C6	1000 pF capacitor, 0603 package
C7	2.2 µF capacitor, tantalum, 3216 package
R1 to R3	10 kΩ resistor, 0402 package
J6, J7	Mill-Max 0.040 inch diameter PC pin, 3101-2-00-21-00-00-08-0
U1	HMC862A, programmable divider
Heatsink	Custom heatsink, alumimum
PCB	600-01663-00-1 evaluation board

OUTLINE DIMENSIONS



COMPLIANT WITH JEDEC STANDARDS MO-220-VEED-4.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(HCP-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Lead Finish	MSL Rating[2]	Package Option
HMC862ALP3E	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	100% Matte Sn	MSL3	HCP-16-1
HMC862ALP3ETR	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	100% Matte Sn	MSL3	HCP-16-1
EV1HMC862ALP3		Evaluation Board			

[1] The HMC862ALP3E and HMC862ALP3ETR are RoHS compliant.
[2] The maximum peak reflow temperature is 260°C. See the Absolute Maximum Ratings section for more information.

D13599-0-4/19(A)

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Analog Devices Inc.:

HMC862ALP3ETR HMC862ALP3E EV1HMC862ALP3