GaAs MMIC ×2 Active Frequency Multiplier, 22 GHz to 42 GHz Output

Data Sheet

HMC8342

FEATURES

- High output power: 15 dBm (typical) at RFIN = 16 GHz
- Low input power drive: 5 dBm (typical)
- Fundamental RF input isolation at RF output: −23 dBc at RFOUT = 30 GHz
- 16-terminal, 6 mm × 6 mm LCC_HS package, 36 mm²

APPLICATIONS

- Clock generation
- Point to point and very small aperture terminal (VSAT) radios
- Test instrumentation
- Military and space

FUNCTIONAL BLOCK DIAGRAM

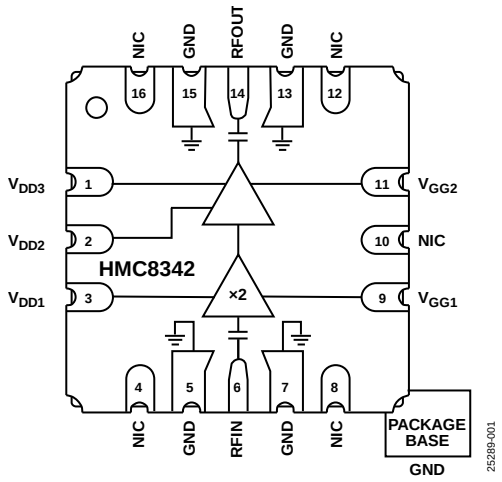

Figure 1.

GENERAL DESCRIPTION

The HMC8342 is a gallium arsenide (GaAs), monolithic microware integrated circuit (MMIC), ×2 active broadband frequency multiplier. When driven by a 5 dBm signal, the multiplier provides 15 dBm typical output power. The output frequency range is from 22 GHz to 42 GHz, and the input fundamental and third harmonic isolations measured at the output are −23 dBc and −20 dBc, respectively, at an output frequency of 30 GHz. The HMC8342 is ideal for use in LO multiplier chains for point to point and VSAT radios, resulting in a reduced parts count vs. traditional design approaches.

Table 1. Related Devices

Device No.	Description
HMC598	×2 active frequency multiplier, 22 GHz to 46 GHz output, bare die

Rev. A
Document Feedback

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REVISION HISTORY

6/2021—Revision A: Initial Version

SPECIFICATIONS

V_{DDx} = V_{DD1} = V_{DD2} = V_{DD3} = 5 V, V_{GG1} = −1.25 V, V_{GG2} = −0.8 V, GND = 0 V, dBm referred to 50 Ω, 5 dBm drive level, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
Input	11		21	GHz	
Output	22		42	GHz	
OUTPUT POWER	4	14		dBm	RFIN = 11 GHz
	10	15		dBm	RFIN = 16 GHz
	2	10		dBm	RFIN = 21 GHz
ISOLATION					RFOUT = 30 GHz
Fundamental Input Frequency Isolation		−23		dBc	With respect to output level, measured at RF output
Input Frequency Third Harmonic Isolation		−20		dBc	With respect to output level, measured at RF output
RETURN LOSS					
Input		−10		dB	
Output		−13		dB	
SUPPLY CURRENT					
V_{DD1} Current (I_{DD1})		17		mA	
V_{DD2} Current (I_{DD2})		55		mA	
V_{DD3} Current (I_{DD3})		97		mA	
V_{GG1} Current (I_{GG1})		−4.5		µA	
V_{GG2} Current (I_{GG2})		−2.5		µA	
RESIDUAL PHASE NOISE					
100 kHz Offset		−138		dBc/Hz	RFIN = 12 GHz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
RF Input (V_{DDx} = 5 V)	10 dBm
Supply Voltage (V_{DD1} = V_{DD2} = V_{DD3})	6 V dc
Channel Temperature	175°C
Nominal Channel Temperature (T = 85°C)	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
EH-16-1	41.9	17.1	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P test board. Refer to JEDEC standard JESD51 for additional information.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for HMC8342

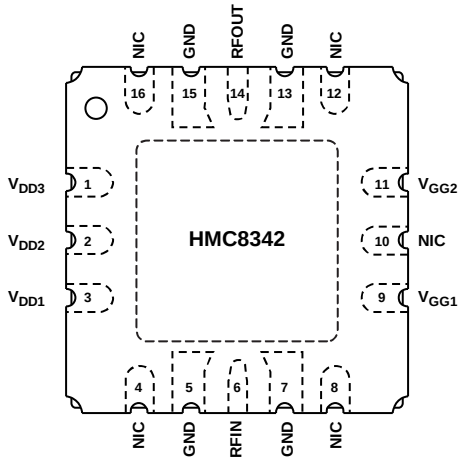
Table 5. HMC8342, 16-Terminal LCC_HS

ESD Model	Withstand Threshold (V)	Class
HBM	±125	0B
CDM	±125	C0B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD OR GROUND PADDLE ON THE BACKSIDE OF THE PACKAGE MUST BE TIED TO RF OR DC GROUND FOR ELECTRICAL, MECHANICAL, AND THERMAL REASONS.

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 3	V_{DD3}, V_{DD2}, V_{DD1}	Power Supply Voltage. 5 V ± 5%. Place three parallel capacitors as close as possible to each of the V_{DD1}, V_{DD2}, and V_{DD3} pins: 4.7 µF, 10 nF, and 100 pF.
4, 8, 10, 12, 16	NIC	Not Internally Connected. These pins can be connected to RF or dc ground without affecting the performance.
5, 7, 13, 15	GND	Ground.
6	RFIN	RF Input. The RFIN pin is ac-coupled and matched to 50 Ω.
9, 11	V_{GG1}, V_{GG2}	Gate Control for Active Multiplier. Place three parallel capacitors as close as possible to each of the V_{GG1} and V_{GG2} pins: 4.7 µF, 10 nF, and 100 pF. V_{GG1} (−1.25 V ± 5%) and V_{GG2} (−0.8 V ± 5%) must be applied before application of V_{DD1}, V_{DD2}, and V_{DD3}. See the Applications Information section for more information.
14	RFOUT	RF Output. The RFOUT pin is ac-coupled and matched to 50 Ω.
	EP	Exposed Pad. The exposed pad or ground paddle on the backside of the package must be tied to RF or dc ground for electrical, mechanical, and thermal reasons.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

Figure 4. EP Interface Schematic

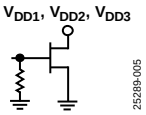


Figure 5. V_{DDx} Interface Schematic

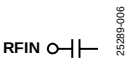


Figure 6. RFIN Interface Schematic

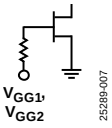


Figure 7. V_{GGx} Interface Schematic

Figure 8. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

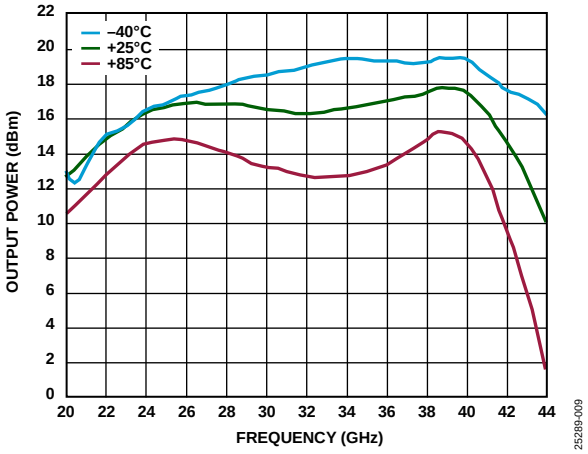


Figure 9. Output Power vs. Frequency at Various Temperatures, 5 dBm Drive Level

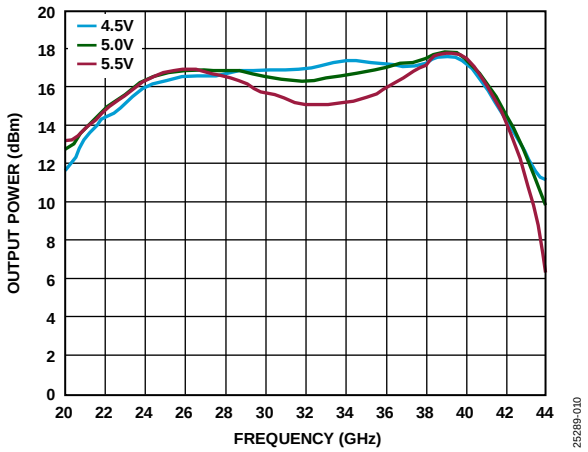


Figure 10. Output Power vs. Frequency at Various Supply Voltages, 5 dBm Drive Level

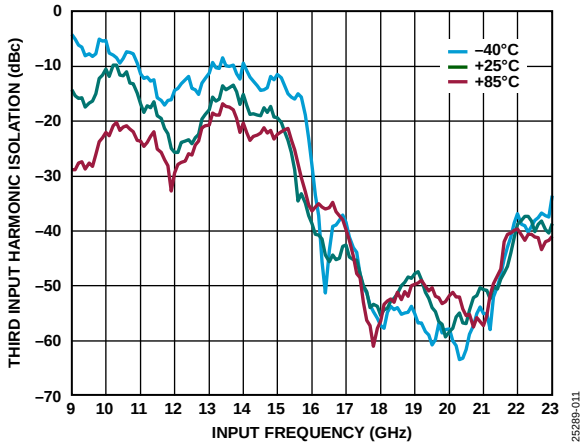


Figure 11. Third Input Harmonic Isolation vs. Input Frequency at Various Temperatures, 5 dBm Drive Level

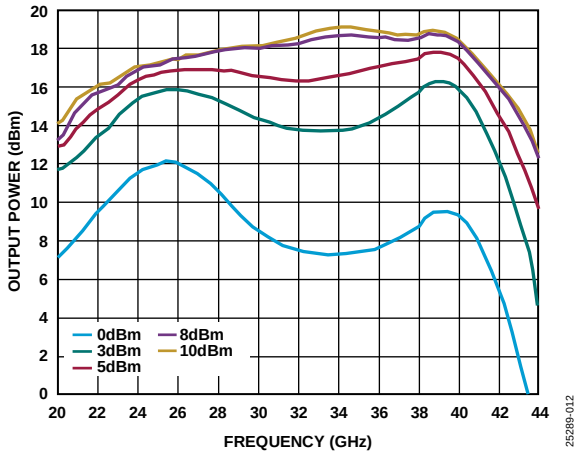


Figure 12. Output Power vs. Frequency at Various Drive Levels

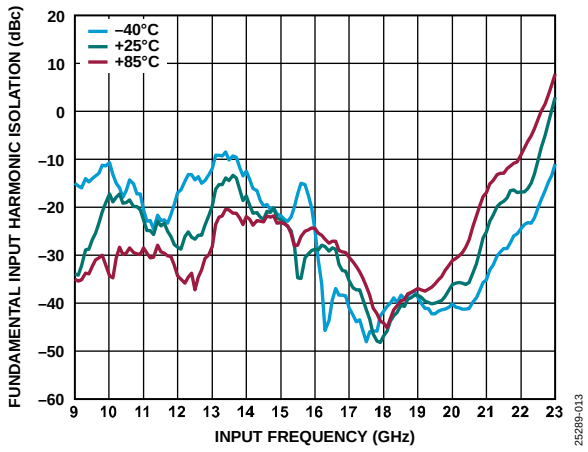


Figure 13. Fundamental Input Harmonic Isolation vs. Input Frequency at Various Temperatures, 5 dBm Drive Level

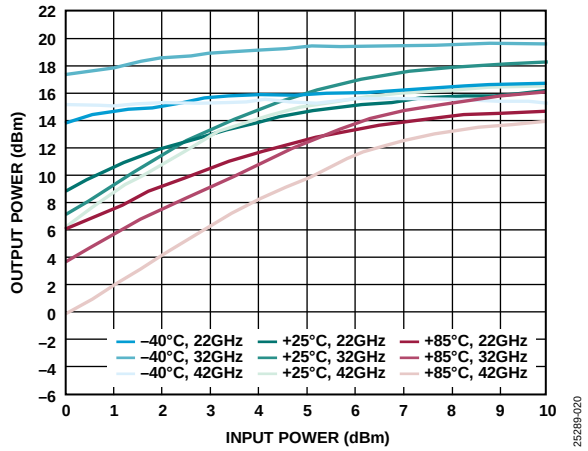


Figure 14. Output Power vs. Input Power, 5 dBm Drive Level

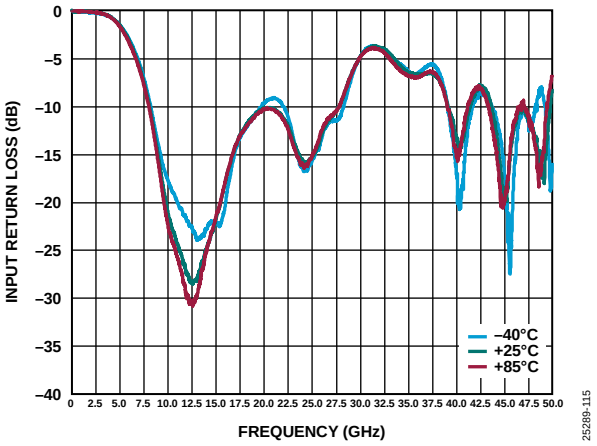


Figure 15. Input Return Loss vs. Frequency at Various Temperatures

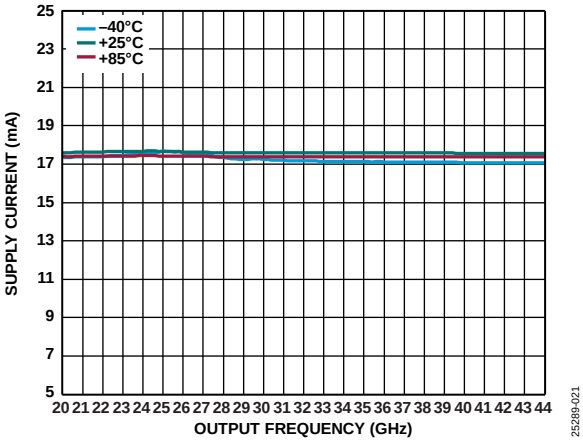


Figure 18. Supply Current (I_{DD1}) vs. Output Frequency at Various Temperatures, 5 dBm Drive Level

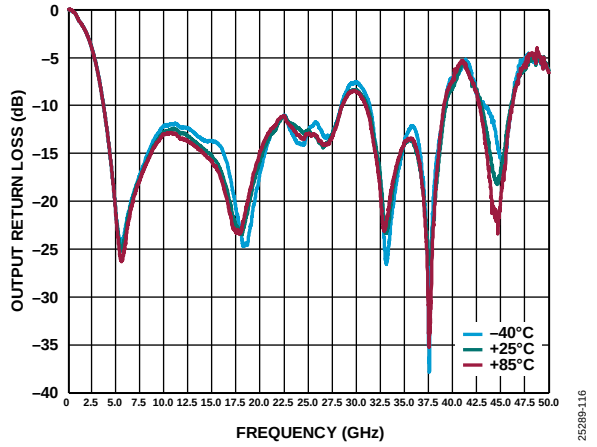


Figure 16. Output Return Loss vs. Frequency at Various Temperatures

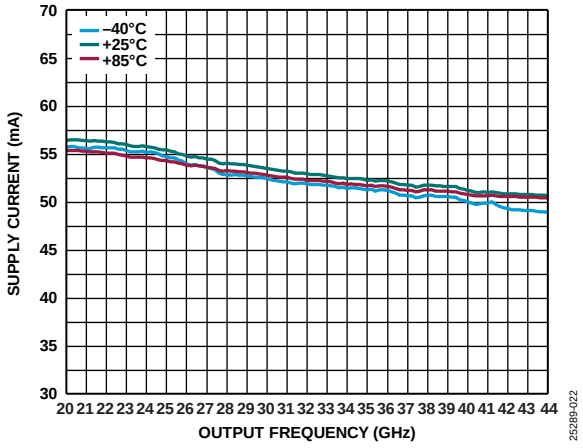


Figure 19. Supply Current (I_{DD2}) vs. Output Frequency at Various Temperatures, 5 dBm Drive Level

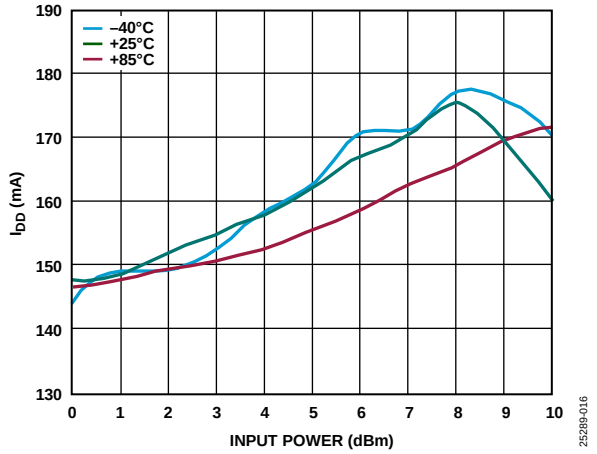


Figure 17. Total Supply Current (I_{DD}) vs. Input Power at Various Temperatures

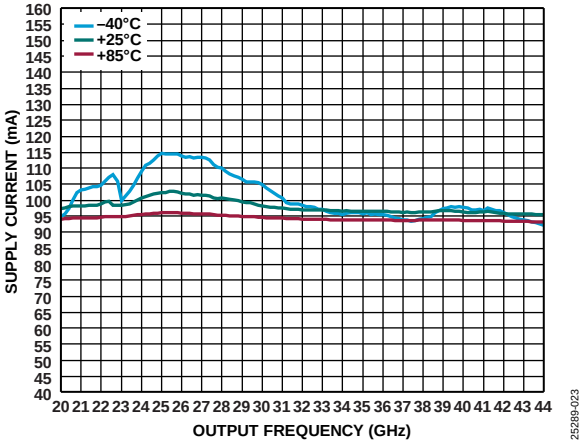


Figure 20. Supply Current (I_{DD3}) vs. Output Frequency at Various Temperatures, 5 dBm Drive Level

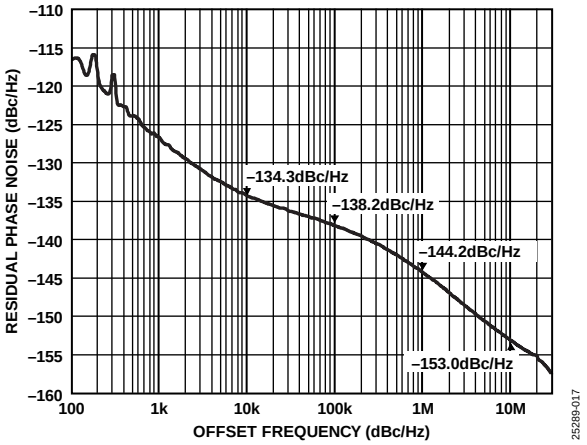


Figure 21. Residual Phase Noise, RFIN = 12 GHz, 5 dBm Drive Level

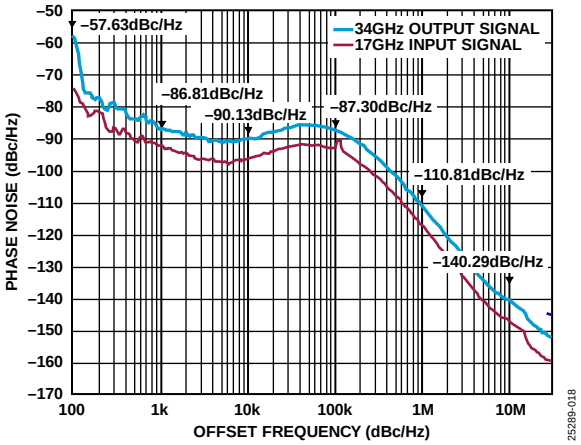


Figure 22. Phase Noise with ADF41513 PLL and HMC8362 VCO, 17 GHz Input, 3 dBm Drive Level

THEORY OF OPERATION

The HMC8342 is a GaAs, MMIC, ×2 active broadband frequency multiplier. The output frequency range is from 22 GHz to 42 GHz. The input frequency range is from 11 GHz to 21 GHz. The HMC8342 can accept input signals with a drive level between 0 dBm and 10 dBm. The output power of the HMC8342 is highly dependent on the input drive level. See the Typical Performance Characteristics section for information on the expected output power for a particular configuration.

Independent supplies of the same voltage can be used for the drain (V_{DDx}) pins, or they can alternatively be tied to a single supply.

The EV1HMC8342LS6 evaluation kit can be used to test and optimize performance for a given application.

APPLICATIONS INFORMATION

V_{GG1} and V_{GG2} are the gate controls for the HMC8342. To prevent damage to the device, it is important to follow the correct bias sequence and to ensure the gate supplies are set before the drain (V_{DDx}) supplies. −3 V is the lowest voltage that can be applied to either of the gate supplies without damaging the device.

From Figure 1, the amplifier circuitry of the HMC8342 is biased by a single gate voltage, V_{GG2}. The multiplier portion of the HMC8342 has two drain supplies, V_{DD2} and V_{DD3}, which are both biased by V_{GG1}.

As per the electrical specifications, V_{GG1} is typically set to bias at −1.25 V and V_{GG2} is typically set to bias at −0.8 V.

To ensure the performance given in the Specifications section is met, follow this straightforward biasing procedure:

1. Set the V_{DDx} supplies to 0 V.
2. Set V_{GG2} to −0.8 V and V_{GG1} to −1.25 V.
3. Set V_{DDx} to 5 V.

This biasing procedure provides acceptable performance for many applications. However, because the exact optimum bias values change based on the RFIN drive level and, to a lesser extent, frequency, it is possible to optimize output power and isolation for a specific application by adjusting the V_{GG2} and V_{GG1} settings.

A procedure to find the optimum gate bias values with minimal risk of damage to the device follows:

1. Apply 0 V to the drain supplies, V_{DDx}.
2. Set both V_{GG1} and V_{GG2} to approximately −2 V to control when the amplifier and multiplier sections can draw current. When V_{GG1} and V_{GG2} are both set to around −2 V, there is minimal current draw.
3. Apply an input signal to RFIN.
4. Apply 5 V to all drain supplies, V_{DDx}.
5. Set V_{GG2}. Increase the voltage until the total current draw of the V_{DDx} supplies is between 125 mA and 145 mA (assuming a 5 dBm input signal).
6. Adjust V_{GG1} so that the RFOUT power and the isolation are optimized for the application.
7. If the drain current is still low, adjust V_{GG2} so that there is a current draw of approximately 160 mA. Recheck the RFOUT power and isolation.

It may be necessary to alternate between adjusting V_{GG1} and V_{GG2} to achieve optimum performance.

The current values given in the preceding example assume a 15 GHz input signal at a 5 dBm drive level.

It is recommended to verify these levels for several devices across the expected temperature range. Then, an active bias controller can potentially be used to automatically perform the bias sequencing.

OUTLINE DIMENSIONS

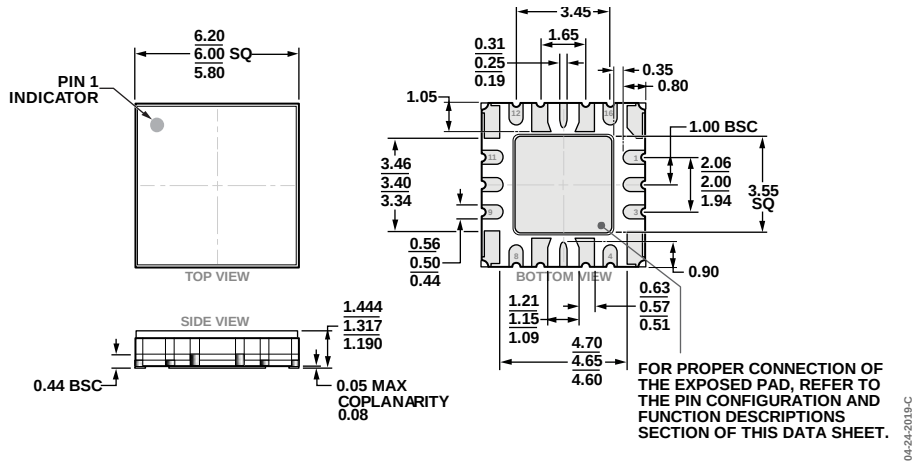


Figure 23. 16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]
6 mm × 6 mm
(EH-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC8342LS6	−40°C to +85°C	16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-16-1
HMC8342LS6TR	−40°C to +85°C	16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-16-1
EV1HMC8342LS6		Evaluation Board	

[1] The HMC8342LS6, HMC8342LS6TR, and EV1HMC8342LS6 are RoHS compliant parts.

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