



## 14 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP

### Typical Applications

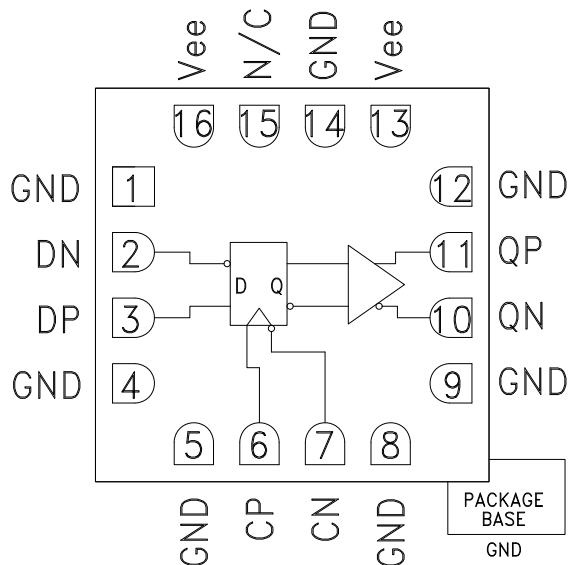
The HMC727LC3C is ideal for:

- 16 G Fiber Channel
- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Digital Logic Systems up to 14 GHz

### Features

- Supports High Data Rates: up to 14 Gbps
- Differential or Single-Ended Operation
- Fast Rise and Fall Times: 19 / 17 ps
- Low Power Consumption: 260 mW typ.
- Propagation Delay: 105 ps
- Single Supply: -3.3 V
- 16 Lead Ceramic 3x3 mm SMT Package: 9 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC727LC3C is a D-Type Flip-Flop designed to support data transmission rates of up to 14 Gbps, and clock frequencies as high as 14 GHz. During normal operation, data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications.

All differential inputs to the HMC727LC3C are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. The differential CML outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC727LC3C operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{ee} = -3.3\text{ V}$

| Parameter                | Conditions                 | Min. | Typ.    | Max  | Units |
|--------------------------|----------------------------|------|---------|------|-------|
| Power Supply Voltage     |                            | -3.6 | -3.3    | -3.0 | V     |
| Power Supply Current     |                            |      | 80      |      | mA    |
| Maximum Data Rate        |                            |      | 14      |      | Gbps  |
| Maximum Clock Rate       |                            |      | 14      |      | GHz   |
| Input Voltage Range      |                            | -1.5 |         | 0.5  | V     |
| Input Differential Range |                            | 0.1  |         | 2.0  | Vp-p  |
| Input Return Loss        | Frequency <14 GHz          |      | 10      |      | dB    |
| Output Amplitude         | Single-Ended, peak-to-peak |      | 550     |      | mVp-p |
|                          | Differential, peak-to-peak |      | 1100    |      | mVp-p |
| Output High Voltage      |                            |      | -10     |      | mV    |
| Output Low Voltage       |                            |      | -560    |      | mV    |
| Output Rise / Fall Time  | Differential, 20% - 80%    |      | 19 / 17 |      | ps    |

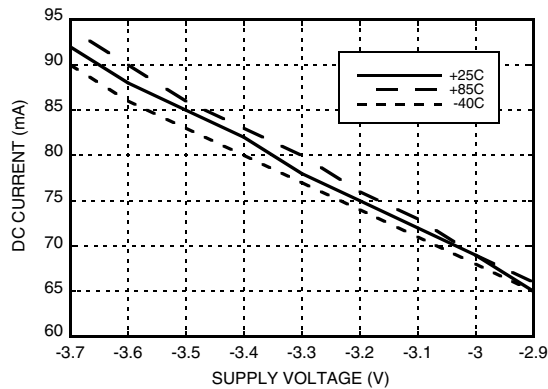
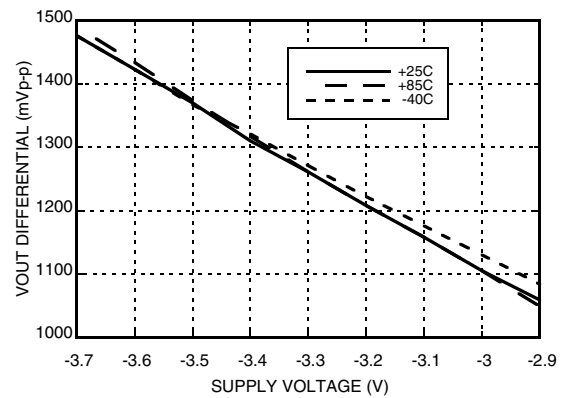
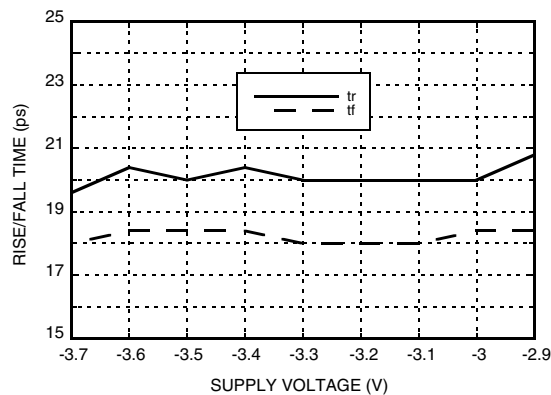
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D-TYPE FLIP-FLOP**
**Electrical Specifications (continued)**

| Parameter                           | Conditions                                      | Min. | Typ. | Max | Units   |
|-------------------------------------|---|------|------|-----|---------|
| Output Return Loss                  | Frequency <14 GHz                               |      | 10   |     | dB      |
| Random Jitter Jr                    | rms   |      |      | 0.2 | ps rms  |
| Deterministic Jitter, Jd            | peak-to-peak, 2 <sup>15</sup> -1 PRBS input [1] |      | 2    |     | ps, p-p |
| Propagation Delay Clock to Data, td |   |      | 105  |     | ps      |
| Clock Phase Margin                  | 13 GHz  |      | 320  |     | deg     |
| Set Up & Hold Time, t <sub>SH</sub> |   |      | 6    |     | ps      |

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2<sup>15</sup>-1 PRBS input, and a single-ended output

**DC Current vs. Supply Voltage [1]**

**Output Differential Voltage vs. Supply Voltage [2]**

**Rise / Fall Time vs. Supply [1]**


[1] Data rate = 13 Gbps

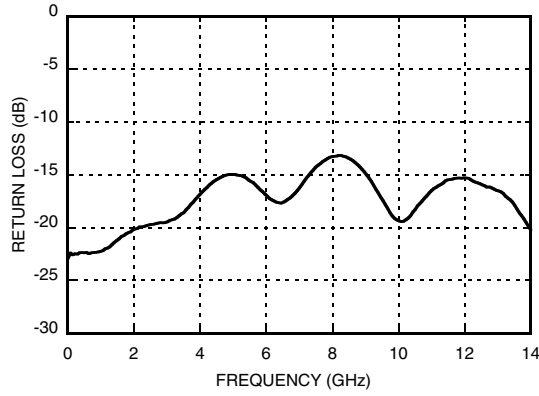
[2] Frequency = 10 GHz

[3] Vee = -3.3 V

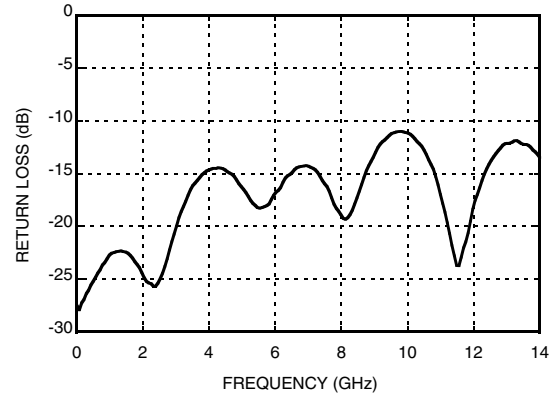


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**Output Return Loss vs. Frequency**



**Input Return Loss vs. Frequency**



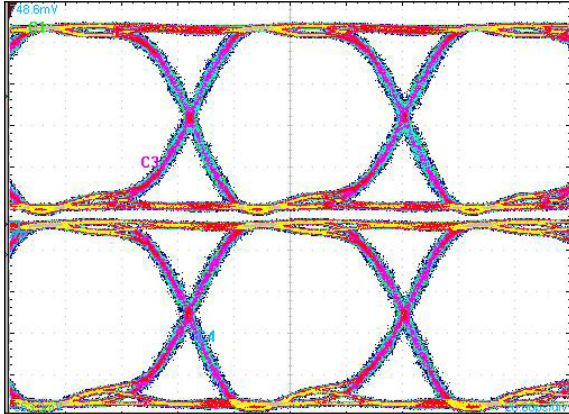
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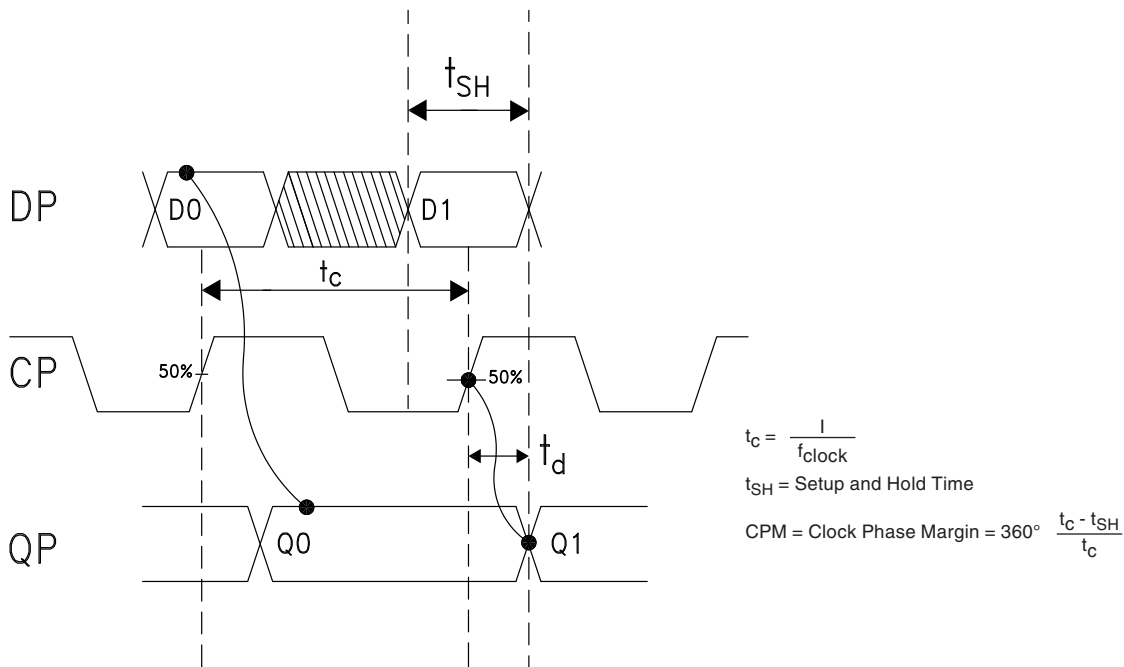
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**Eye Diagram**



[1] Test Conditions:  
 Pattern generated with an Agilent N4903A Serial BERT.  
 Eye Diagram presented on a Tektronix CSA 8000.  
 Device input = 13 Gbps PN code, Vin = 300 mVp-p differential.  
 Both output channels shown.

**Timing Diagram**



**Truth Table**

| Input |        | Outputs |
|-------|--------|---------|
| D     | C      | Q       |
| L     | L -> H | L       |
| H     | L -> H | H       |

Notes:  
 D = DP - DN  
 C = CP - CN  
 Q = QP - QN  
 H - Positive voltage level  
 L - Negative voltage level



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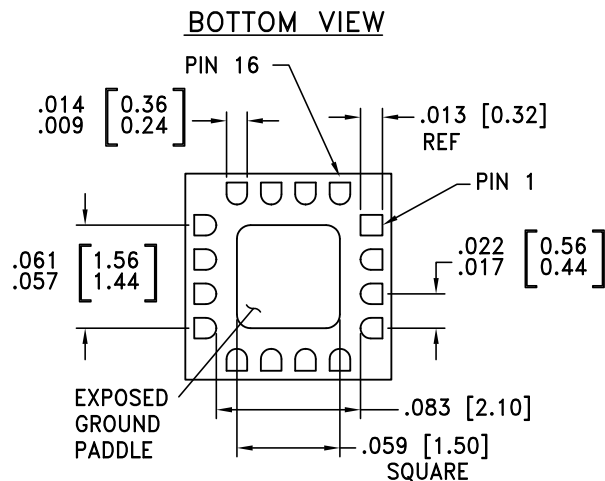
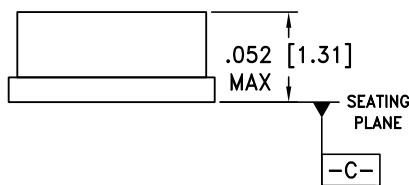
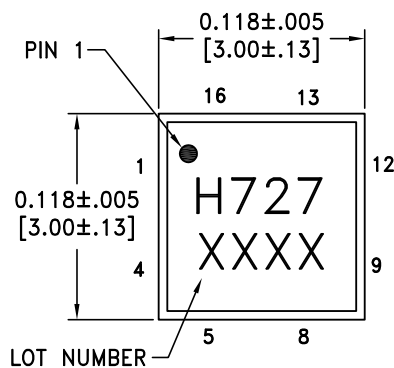
### Absolute Maximum Ratings

|   |                   |
|---|-------------------|
| Power Supply Voltage (Vee)  | -3.75 V to +0.5 V |
| Input Signals   | -2 V to +0.5 V    |
| Output Signals  | -1.5 V to +1 V    |
| Continuous Pdiss (T = 85 °C)<br>(derate 17 mW/°C above 85 °C)                   | 0.68 W            |
| Thermal Resistance (R <sub>th j-p</sub> ) Worst case junction to package paddle | 59 °C/W           |
| Maximum Junction Temperature  | 125 °C            |
| Storage Temperature   | -65 °C to +150 °C |
| Operating Temperature   | -40 °C to +85 °C  |
| ESD Sensitivity (HBM)   | Class 1C          |



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

### Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:  
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

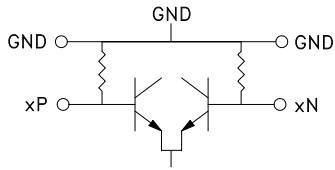
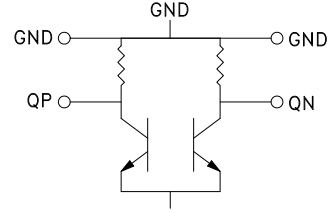

### Package Information

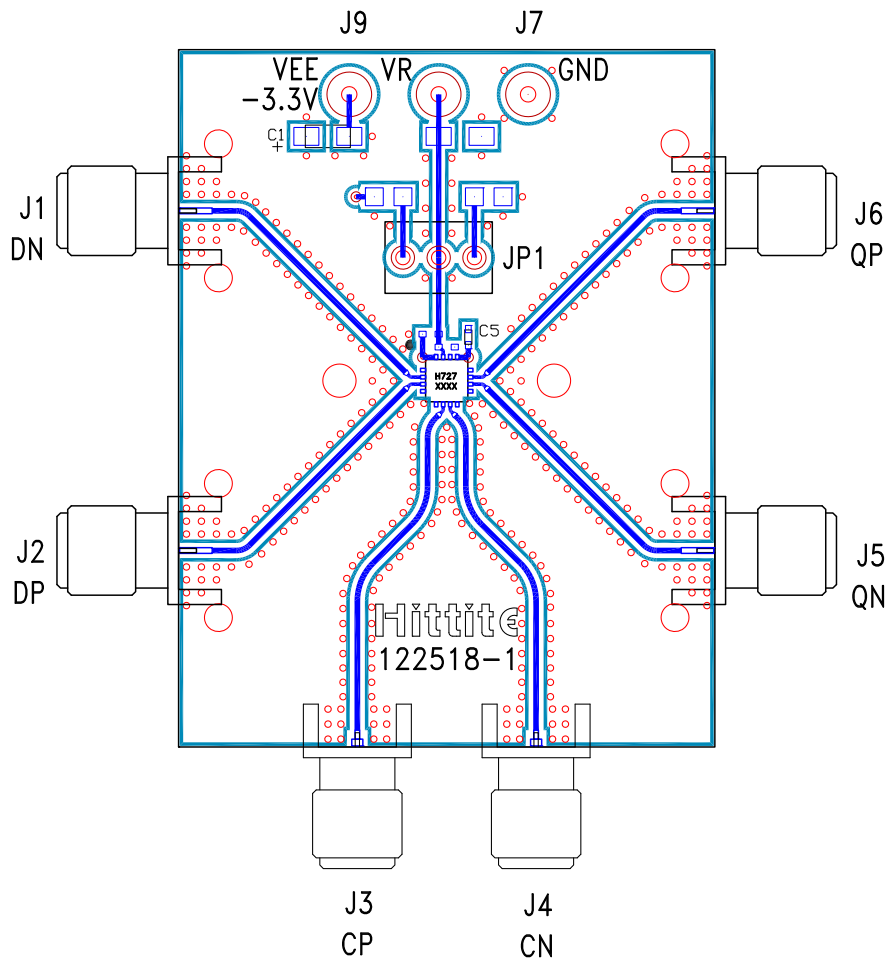
| Part Number | Package Body Material | Lead Finish      | MSL Rating          | Package Marking <sup>[2]</sup> |
|-------------|-----------------------|------------------|---------------------|--------------------------------|
| HMC727LC3C  | Alumina, White        | Gold over Nickel | MSL3 <sup>[1]</sup> | H727<br>XXXX                   |

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX


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**Pin Descriptions**

| Pin Number          | Function         | Description  | Interface Schematic  |
|---------------------|------------------|--|--|
| 1, 4, 5, 8, 9, 12   | GND              | Signal Grounds   |   |
| 2, 3<br>6, 7        | DN, DP<br>CP, CN | Differential Data Inputs: Common Mode Logic (CML) referenced to positive supply.                 |   |
| 10, 11              | QN, QP           | Differential Data Outputs: Common Mode Logic (CML) referenced to positive supply.                |   |
| 13, 16              | Vee              | Negative Supply  |  |
| 14,<br>Package Base | G                | GND  |  |
| 15                  | N/C              | No Connection required. This pin may be connected to RF/DC ground without affecting performance. |  |


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**Evaluation PCB**

**List of Materials for Evaluation PCB 122520 [1]**

| Item    | Description                                      |
|---------|--|
| J1 - J6 | PCB Mount SMA RF Connectors                      |
| J7, J9  | DC Pin   |
| C1      | 4.7 $\mu$ F Capacitor, Tantalum                  |
| C5      | 100 pF Capacitor, 0402 Pkg.                      |
| U1      | HMC727LC3C<br>High Speed Logic, D-Type Flip-Flop |
| PCB [2] | 122518 Evaluation Board                          |

[1] Reference this number when ordering complete evaluation PCB

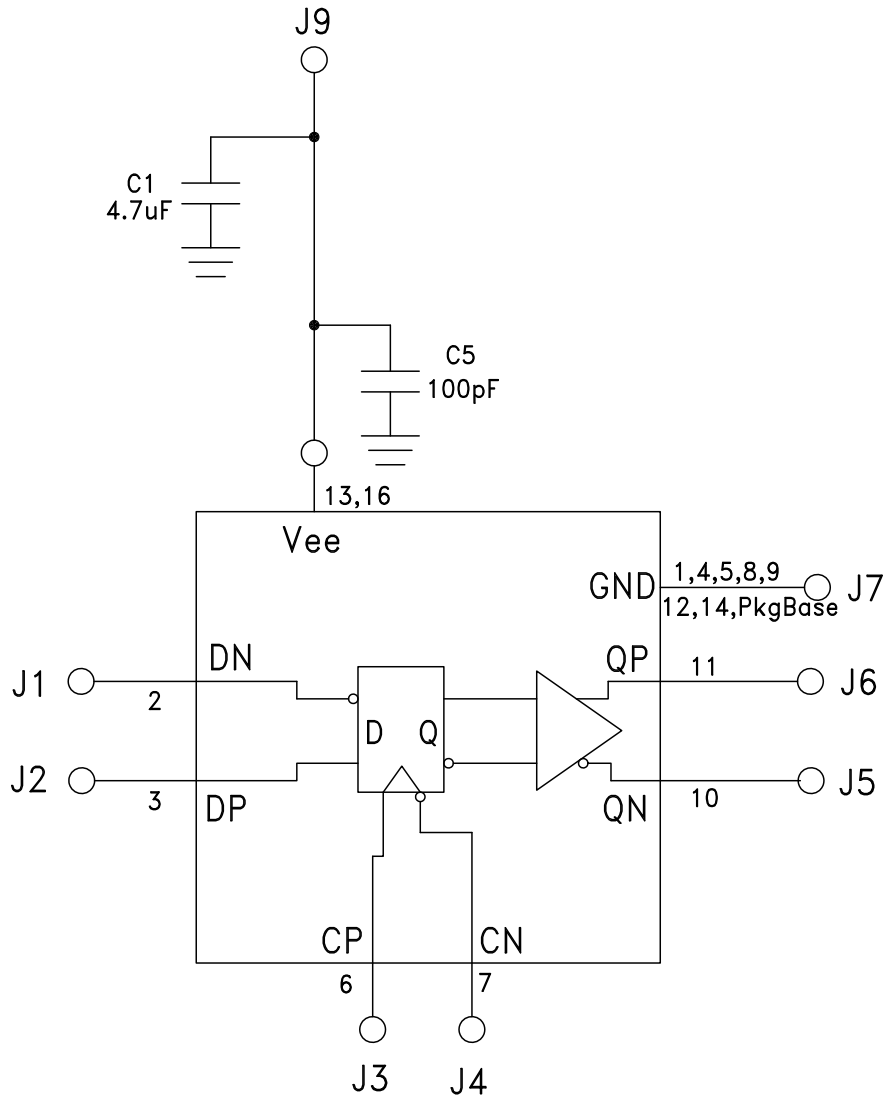
[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



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**Application Circuit**





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