

Evaluating the ADL8141 GaAs, pHEMT, MMIC, Low Noise Amplifier, 14 GHz to 24 GHz

FEATURES

- ▶ 4-layer, Rogers 4003C and Isola 370HR evaluation board
- ▶ End launch 2.4 mm RF connectors
- ▶ Through calibration path (depopulated)

EVALUATION KIT CONTENTS

- ▶ ADL8141-EVALZ evaluation board

EQUIPMENT NEEDED

- ▶ RF signal generator
- ▶ RF spectrum analyzer
- ▶ RF network analyzer
- ▶ 2 V, 100 mA power supply

GENERAL DESCRIPTION

The ADL8141-EVALZ is a 4-layer printed circuit board (PCB) fabricated from 8 mil thick, Rogers 4003C and Isola 370HR, copper clad, forming a nominal thickness of 62 mils. The RFIN and RFOUT ports on the ADL8141-EVALZ are populated with female coaxial 2.4 mm connectors, and the corresponding RF traces have a 50 Ω characteristic impedance. The ADL8141-EVALZ is populated with components suitable for use over the entire -40°C to $+85^{\circ}\text{C}$ operating temperature range of the [ADL8141](#). To calibrate board trace losses, a through calibration path is provided between the J1 and J2 connectors. J1 and J2 must be populated with 2.4 mm RF connectors to use the through calibration path. Refer to [Table 1](#) and [Figure 3](#) for the through calibration path performance.

Connect ground and power to ADL8141-EVALZ using the surface-mount technology (SMT) test point connectors, GND and VDD. A supplementary test point for VBIAS is included for simple access on the RBIAS pin (see [Figure 5](#) for the test point assembly).

The package ground leads and the exposed pad connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction.

The power supply decoupling capacitors on the ADL8141-EVALZ represent the configuration used to characterize and qualify the device.

For full details on the ADL8141, see the ADL8141 data sheet, which must be consulted in conjunction with this user guide when using the ADL8141-EVALZ evaluation board.

EVALUATION BOARD PHOTOGRAPHS

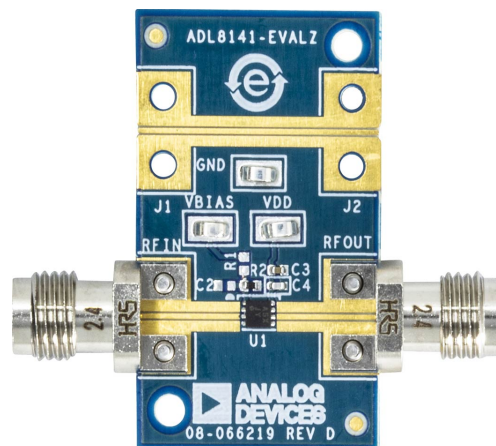


Figure 1. ADL8141-EVALZ Top

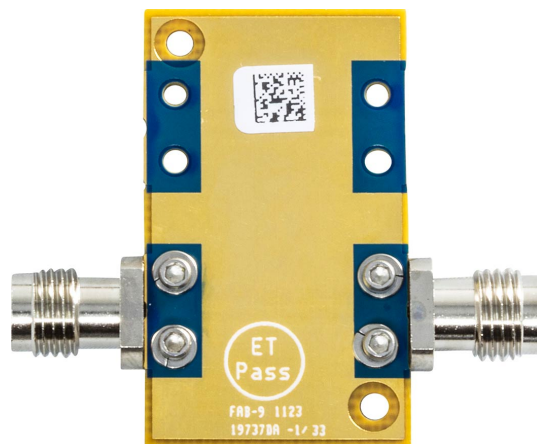


Figure 2. ADL8141-EVALZ Bottom

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REVISION HISTORY

7/2023—Revision 0: Initial Version

OPERATING THE ADL8141-EVALZ

A 2 V, 100 mA power supply is required to provide the bias to the ADL8141 when using the ADL8141-EVALZ. Connect the 2 V power supply to the SMT test point, VDD. Connect the ground reference to the GND test point. Apply the RF power after V_{DD} is turned on and remove the RF power before V_{DD} is turned off.

Refer to the ADL8141 data sheet for the recommended resistor values to achieve different supply currents. The following bias conditions are recommended to achieve optimal performance: $V_{DD} = 2$ V and quiescent current (I_{DQ}) = 25 mA. I_{DQ} is typically achieved using a 768 Ω value for the bias resistance (R_{BIAS}).

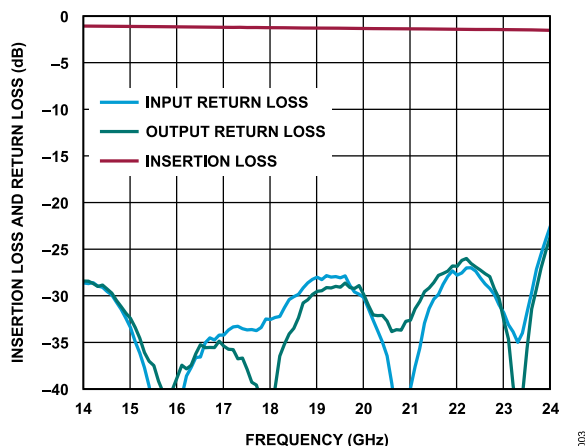


Figure 3. Insertion Loss and Return Loss of the Through Calibration Path, 14 GHz to 24 GHz

Table 1. Insertion Loss and Return Loss of the Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)	Input Return Loss (dB)	Output Return Loss (dB)
14	-1.1	-28.6	-28.4
15.5	-1.1	-42.7	-37.5
16	-1.2	-44	-38.8
16.5	-1.2	-36.6	-35.2
17	-1.2	-34.2	-35.4
17.5	-1.2	-33.7	-37.9
18	-1.2	-32.5	-42.1
18.5	-1.3	-30.1	-33.5
19	-1.3	-28	-29.5
19.5	-1.3	-28.1	-29.1
20	-1.3	-30.2	-29.9
20.5	-1.4	-36.4	-32.7
21	-1.4	-39.9	-32.6
21.5	-1.4	-30.4	-28.6
22	-1.4	-27.8	-26.8
22.5	-1.4	-28.1	-27.3
23	-1.5	-31.8	-32.6
23.5	-1.5	-31.8	-35.7
24	-1.5	-22.5	-23.6

RECOMMENDED BIAS SEQUENCING

During Power-Up

To power up the ADL8141-EVALZ, take the following bias sequencing steps:

1. Connect the VDD power supply.
2. Set the VDD supply to 2 V.
3. Apply the RF input signal.

During Power-Down

To power down the ADL8141-EVALZ, take the following bias sequencing steps:

1. Turn off the RF input signal.
2. Set the VDD supply to 0 V.

EVALUATION BOARD SCHEMATIC AND ARTWORK

The bias current (see [Figure 4](#)) can either be set by placing a resistor in Position R2 or by placing a resistor in Position R1 and by applying an adjustable voltage to the VBIAS pin (in this case R2 must be open).

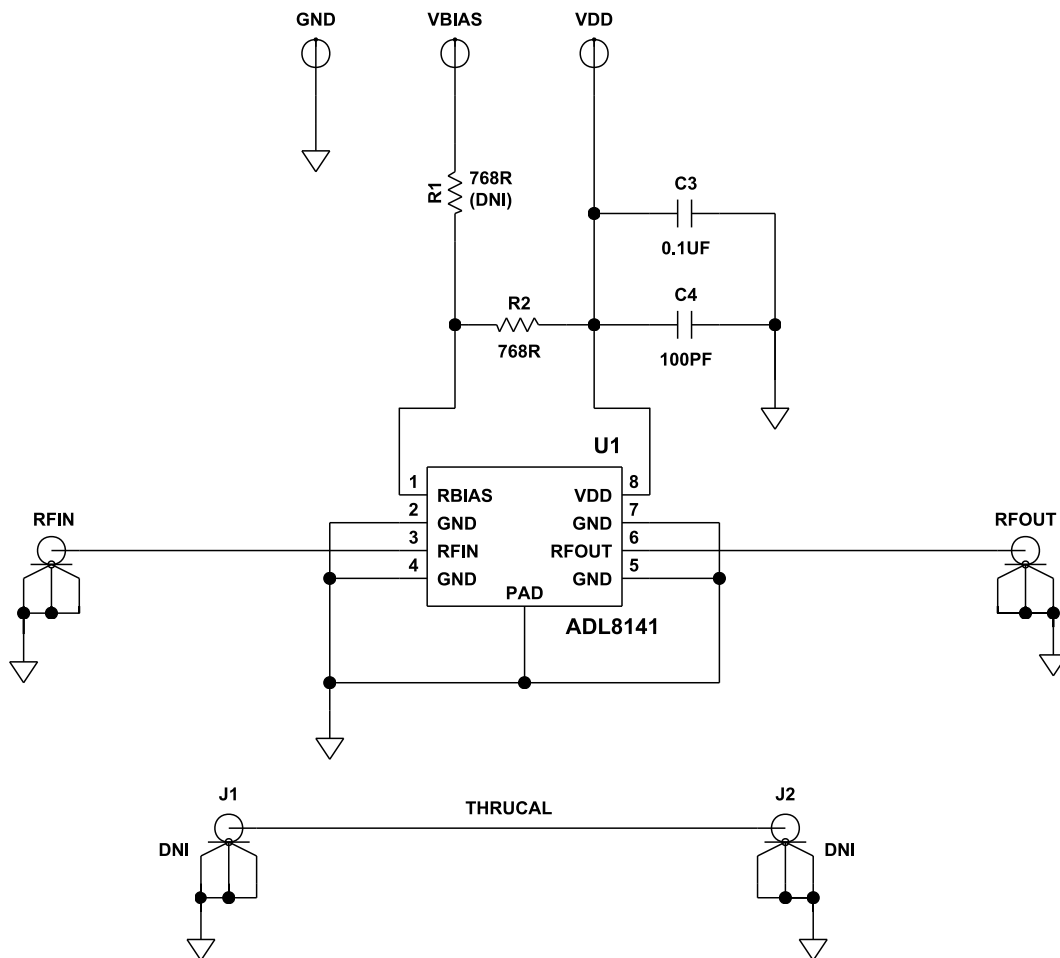


Figure 4. ADL8141-EVALZ Evaluation Board Schematic

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EVALUATION BOARD SCHEMATIC AND ARTWORK

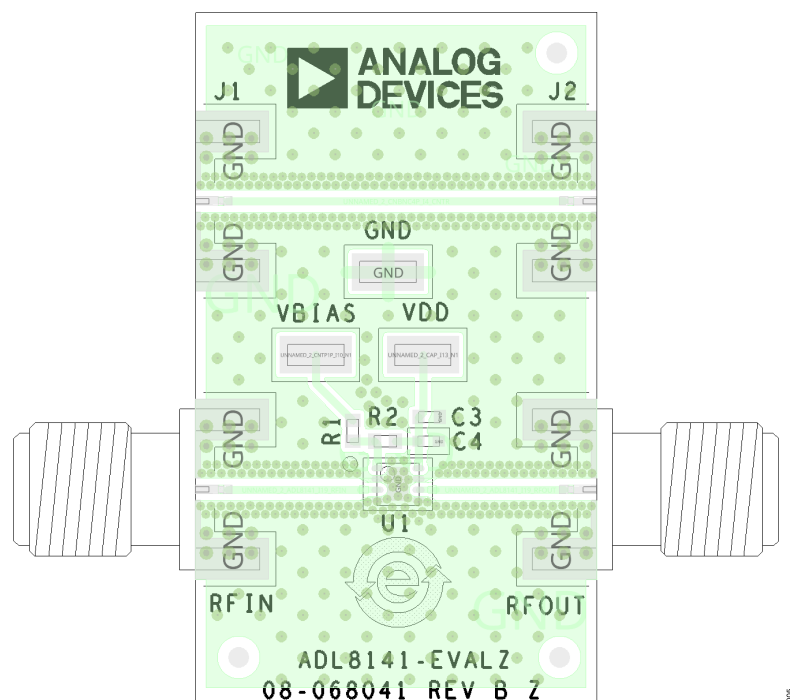


Figure 5. ADL8141-EVALZ Assembly Drawing (J1 and J2 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C3	0.1 μ F ceramic capacitor, 16 V, 10%, X7R, 0402	Samsung	CL05B104K05NNNC
C4	100 pF ceramic capacitor, 50 V, 5%, C0G, 0402, extreme low equivalent series resistance (ESR)	Kemet	C0402C101J5GACTU
GND, VBIAS, VDD	Connector, printed circuit boards (PCBs), surface-mounted technology (SMT) test points	Keystone Electronics	5015
R2	768 Ω resistor, surface-mounted device (SMD), 1%, 1/10 W, 0402	Panasonic	ERJ-2RKF7680X
RFIN, RFOUT	Connector PCBs, 2.4 mm coax for frequency test measurements, 50 Ω , 50 GHz	Hirose Electric, Co	H2.4-LR-SR2(12)
J1, J2	Connector PCBs, 2.4 mm coax for frequency test measurements, 50 Ω , 50 GHz (DNI)	Hirose Electric, Co	H2.4-LR-SR2(12)
R1	768 Ω resistor, SMD, 1%, 1/10 W, 0402 (DNI)	Panasonic	ERJ-2RKF7680X

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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