QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 948
MOSFET-CONTROLLED POWER SUPPLY TRACKER
LTC2926

DESCRIPTION

The demonstration circuit board DC948A is intended to evaluate the performance of the LTC2926 MOSFET-Controlled Power Supply Tracker. The board contains one LTC2926 Tracker, three power MOSFETs for tracking and sequencing three power supply rails, a few resistors for configuring tracking profiles and one small signal MOSFET for voltage drop compensation in the "master" rail. As assembled, DC948A operates with +5.0V as the "master" rail, and +3.3V and +2.5V as "slave" rails. The board features "master" supply slew rate of S_M=100V/s, and "slave" supply slew rates of S_S=150V/s. The first "slave" supply power up starts 12.5ms later than "master" supply and second "slave" starts 25ms later.

The LTC2926 is designed to provide compensation for voltage drop across each power MOSFET and its traces, when an individual power supply is used for each rail. This compensation is achieved with automatic remote sense switching. Two integrated switches for "slave" supplies and a control signal source for the external switch are implemented in the LTC2926.

The power supply tracking and sequencing profiles known as coincident tracking, ratiometric tracking, offset tracking, or supply sequencing are accomplished by selection of the four resistor values per channel (RTA, RTB, RFA, and RFB).

Design files for this circuit board are available. Call the LTC factory.

PERFORMANCE SUMMARY

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Voltage	Operating Range	2.9	3.3	5.5	V
$V_{CC(UVLO)}$	Input Supply Undervoltage Lockout	V_{CC} Rising	2.2	2.4	2.6	V
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	1.20	1.23	1.26	V
$V_{ON(CLR)}$	ON Pin Fault Clear Threshold Voltage	$V_{ON\ FALLING}$	0.465	0.500	0.535	V
V_{MASTER}	Master Supply Voltage			5.0		V
V_{SLAVE1}	Slave Supply 1 Voltage			3.3		V
V_{SLAVE2}	Slave Supply 2 Voltage			2.5		V
S_{MGATE}	Master Gate Voltage Slew Rate			100		V/s
S_{SLAVE1}	Slave Supply 1 Slew Rate			150		V/s
S_{SLAVE2}	Slave Supply 2 Slew Rate			150		V/s
$I_{S\ MIN}$	Slave Supply Minimal Load Current			20		mA

OPERATING PRINCIPLES

The "master" rail is controlled like a typical hot swap circuit, where the "master" gate voltage slew rate defines the output slew rate. With the 10uA gate driver current capability, 0.1uF gate capacitor CMGATE placed on the board, and negligible MOSFET gate capacitance (1.5nF) the "master" slew rate is 100V/s.

For managing each "slave" rail the LTC2926 Tracker contains individual tracking and gate controller cells.

The tracking cell servos the TRACK pin to 0.8V by providing the required current into the Track resistor to keep the voltage on the TRACK pin equal to 0.8V. The current supplied by the TRACK pin is mirrored to the feedback FB pin. The TRACK pin node is connected to the RAMPBUF pin and GND with external resistors RTB and RTA respectively.

The gate controller cell servos the FB pin to 0.8V by driving the gate of the external N-channel power MOSFET. This establishes the "slave" output voltage based on the TRACK pin current and the feedback divider resistors. This cell is a bang-bang control system with the inner command (reference) signal equal to 0.8V and feedback provided from the feedback pin node, which is connected to two resistors: RFA to GND and RFB to the "slave" rail output. When the "slave" output reaches its nominal output, the feedback divider should provide the FB pin with a voltage a little bit lower than the inner command. In this case, the gate controller cell develops maximum gate voltage to enhance the external MOSFET.

Figure 1, borrowed from the Data Sheet, demonstrates the structure of the tracking and gate controller cells and simplifies understanding their interaction.

The "slave" output voltage slew rate is defined as:

$$S_{SLAVE}=S_{MASTER} \bullet RFB/RTB.$$

The relation RFB/RTB for initially installed components for both channels equals 1.5.

The master signal ramps up and the slave supplies track the master signal, when the ON pin signal rises above 1.23V.

The board allows two options for V_{CC} source selection. Jumper JP1 ON position connects the master supply to V_{CC} node, and the OFF position allows the use of an external voltage source.

There are also two options for the RAMP pin signal source. Jumper JP2 placed in the MASTER position connects master rail output voltage to the RAMP pin. Jumper JP2 EXTERNAL position allows the use of an external source.

After master and slave gate drivers reach their maximum voltages, the LTC2926 closes integrated remote sense switches and pulls up the external FET gate with a 10uA current source as an external remote switch control signal.

For the proper LTC2926 operation, each "slave" rail output should be loaded to consume a current, which exceeds 50-100 times the steady state individual feedback divider current. Initially populated DC948A requires a 100-150 Ohm resistive load or 150-200uF capacitive load.

Refer to the LTC2926 data sheet for detailed equations and design examples.

QUICK START PROCEDURE

Demonstration circuit DC948A is easy to set up to evaluate the performance of the LTC2926. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions:

JP1 in position ON

JP2 in position MASTER

2. With power off, connect the +5.0V power supply to the SUPPLY0 and GND turrets, the +3.3V supply to the SUPPLY1 and GND turrets, the +2.5V supply to the SUPPLY2 and GND turrets.

3. Connect the ON signal source with the ON/OFF turret.

4. Load each output rail (MASTER, SLAVE1, and SLAVE2 turrets) with a 50-Ohm resistor or equivalent electronic load..

5. Place the scope probes on the output loads (MASTER, SLAVE1, and SLAVE2) and ON/OFF turret. Be sure that the ON control signal is low.

6. Turn on the +5.0V, +3.3V, and +2.5V supplies.

7. Switch the ON signal from low to high.

8. The power-up output voltages should correlate with the transient shown in Figure 3. Acceptable tolerance in the slew rate value and timing position is ±30%.

9. Switch the ON signal from high to low.

10. The power-down output voltages should correlate with transient shown in Figure 4. Acceptable tolerance in the slew rate value and timing position is ±30%.

11. With any other “master” voltage and “slave” voltages set, calculate the following component parameters: RTA1, RTB1, RFA1, RFB1, RTA2, RTB2, RFA2, RFB2, and CMGATE based on the required profiles and timing.

12. Replace the appropriate components on the board and repeat the described above actions.

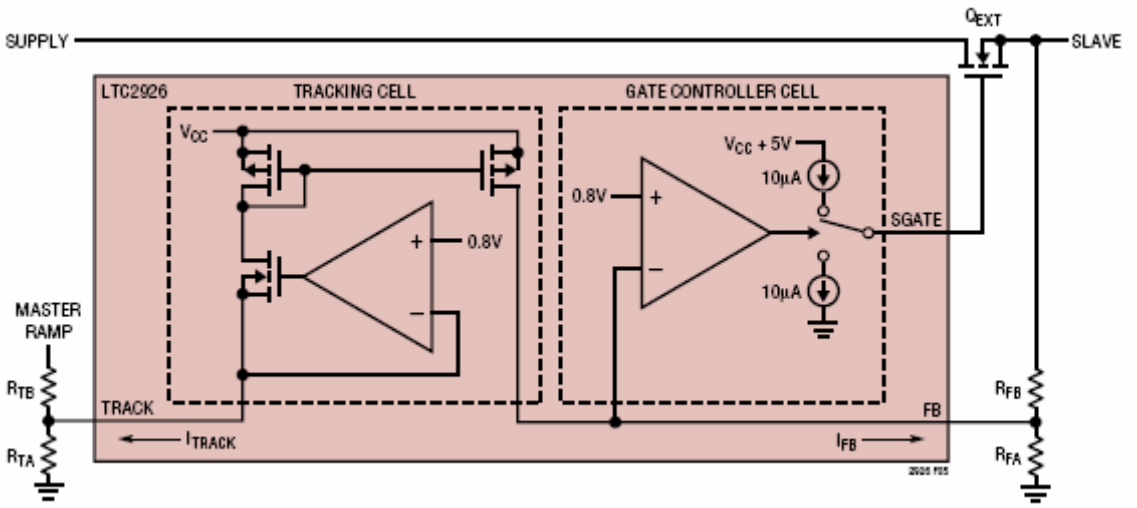


Figure 1. Simplified Tracking Cell and Gate Controller Cell Structure

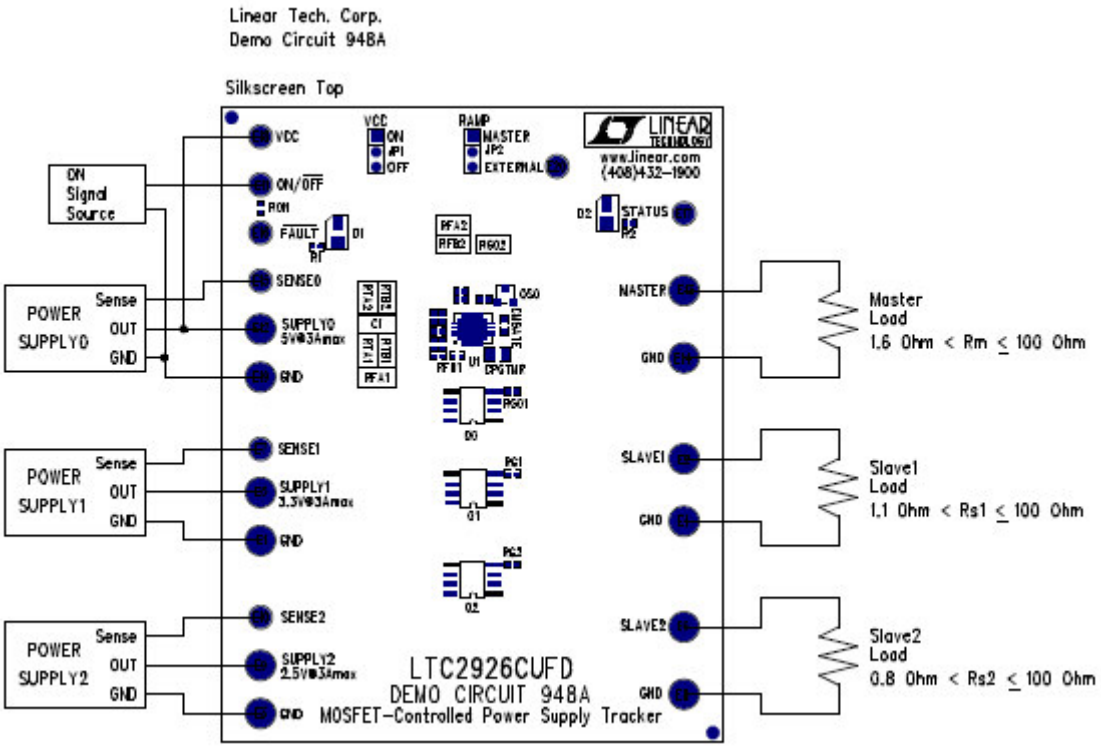


Figure 2. The DC948A connection with Power Supplies, loads, and ON signal source

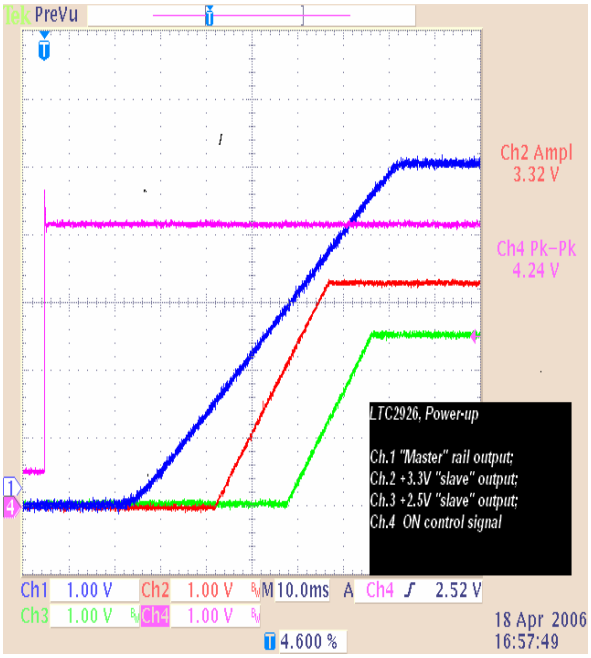


Figure 3. Power-up mode

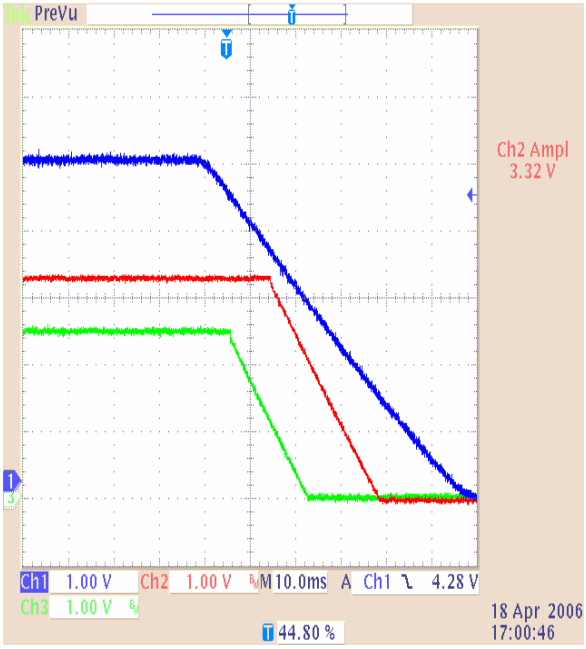
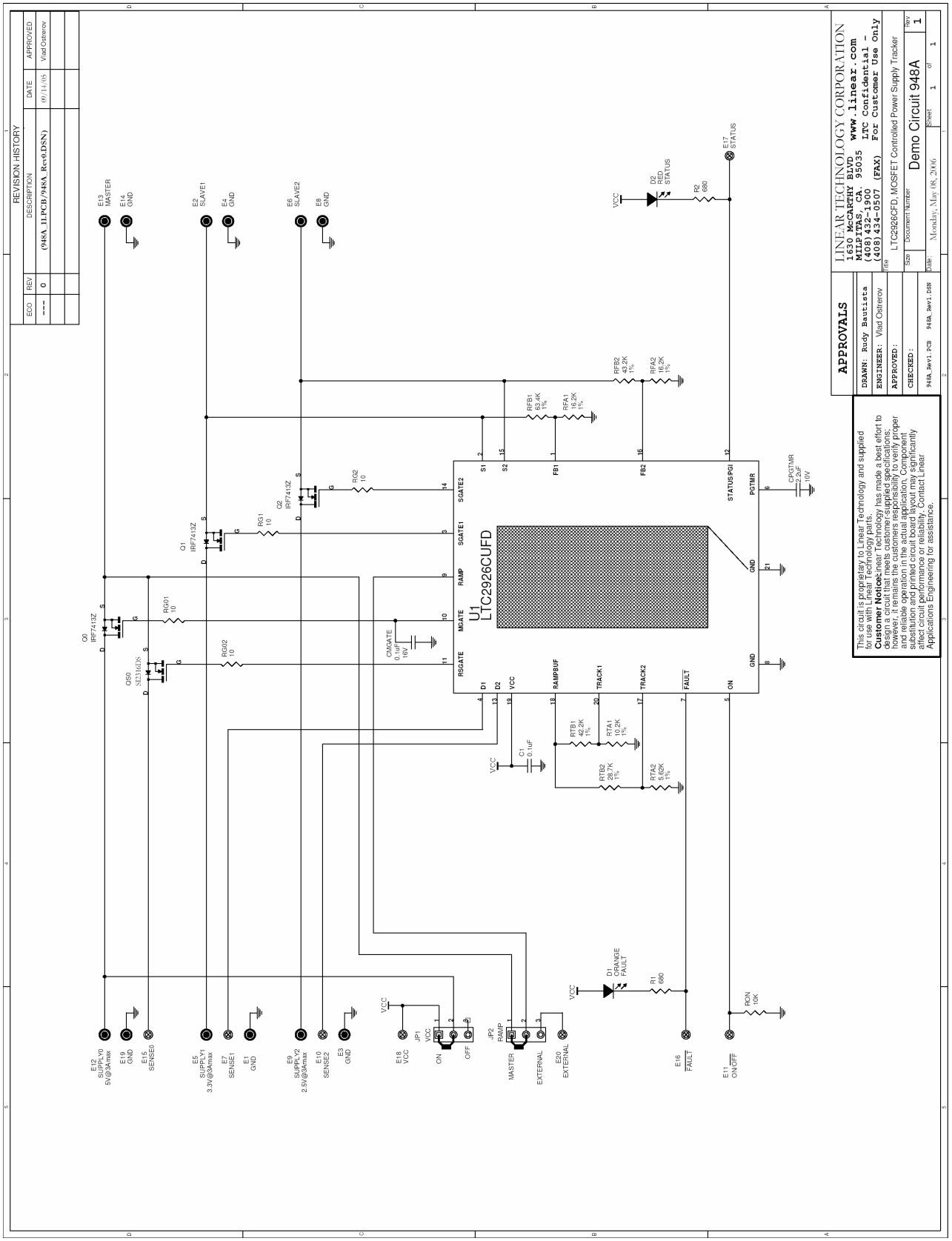


Figure 4. Power-down mode


REVISION HISTORY
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DESCRIPTION
DATE
APPROVED
--- 0 (948A_1LPCB/948A_Rev0.DSN) 09/14/05 Vlad Osterov
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DRAWN: Rudy Bautista
ENGINEER: Vlad Osterov
APPROVED:
CHECKED:
Title
LTC2926CFD, MOSFET Controlled Power Supply Tracker
Size
Document Number
Demo Circuit 948A
Rev
1
Date:
Monday, May 08, 2006
Sheet 1 of 1
948A_Rev1.PCB
948A_Rev1.DSN
This circuit is proprietary to Linear Technology and supplied for use with Linear Technology parts.
Customer Notice: Linear Technology has made a best effort to design a circuit that meets customer-supplied specifications; however, it remains the customers responsibility to verify proper and reliable operation in the actual application. Component substitution and printed circuit board layout may significantly affect circuit performance or reliability. Contact Linear Applications Engineering for assistance.
U1
LTC2926CUFD
Q0 IRF7413Z
Q1 IRF7413Z
Q2 IRF7413Z
QS0 SI2316DS
RG01 10
RG1 10
RG2 10
RG02 10
CMGATE 0.1uF 16V
C1 0.1uF
CPGTMR 2.2uF 10V
RFB1 63.4K 1%
RFA1 16.2K 1%
RFB2 43.2K 1%
RFA2 16.2K 1%
RTB1 42.2K 1%
RTA1 10.2K 1%
RTB2 28.7K 1%
RTA2 5.62K 1%
R1 680
R2 680
RON 10K
D1 ORANGE FAULT
D2 RED STATUS
VCC
E12 SUPPLY0 5V@4Amax
E19 GND
E15 SENSE0
E5 SUPPLY1 3.3V@3Amax
E7 SENSE1
E1 GND
E9 SUPPLY2 2.5V@3Amax
E10 SENSE2
E3 GND
E18 VCC
JP1 VCC ON OFF
JP2 RAMP MASTER EXTERNAL
E20 EXTERNAL
E16 FAULT
E11 ON/OFF
E17 STATUS
E13 MASTER
E14 GND
E2 SLAVE1
E4 GND
E6 SLAVE2
E8 GND
S1 S2 FB1 FB2 STATUS/PGI PGTMR SGATE2 SGATE1 RAMP MGATE RSGATE D1 D2 VCC RAMPBUF TRACK1 TRACK2 FAULT ON GND

REQUIRED CIRCUIT COMPONENTS				
Item	**Qty**	**Reference**	**Part Description**	**Manufacturer / Part #**
1	1	CMGATE	Cap., X7R 0.1uF 16V 20%	Taiyo Yuden EMK107BJ104MA
2	1	CPGTMR	Cap., X5R 2.2uF 10V 20%	Taiyo Yuden LMK212BJ225MG
3	1	C1	Cap., X5R 0.1uF 10V 20%	AVX 0402ZD104MAT2A
4	1	QS0	Mosfet N-Chan., 30V	Siliconix SI2316DS
5	3	Q1,Q2,Q0	N-Chan. Mosfet, 30V	International Rect. IRF7413Z
6	2	RFA1,RFA2	Res., Chip 16.2K 1/16W 1%	AAC CR05-1622FM
7	1	RFB1	Res., Chip 63.4K 1/16W 1%	AAC CR05-6342FM
8	1	RFB2	Res., Chip 43.2K 1/16W 1%	AAC CR05-4322FM
9	4	RG1,RG01,RG2,RG02	Res., Chip 10 0.06W 5%	AAC CR05-100JM
10	1	RON	Res., Chip 10K 0.06W 5%	VISHAY CRCW0402103J
11	1	RTA1	Res., Chip 10.2K 0.06W 1%	AAC CR05-1022FM
12	1	RTA2	Res., Chip 5.62K 1/16W 1%	AAC CR05-5621FM
13	1	RTB1	Res., Chip 42.2K 1/16W 1%	VISHAY CRCW040242K2FRT6
14	1	RTB2	Res., Chip 28.7K 0.06W 1%	AAC CR05-2872FM
15	1	U1	I.C., Volt Reg.	Linear Technology Corp. LTC2926CUFD
ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS				
1	1	D1	LED, ORANGE	Panasonic LN1851CTR
2	1	D2	LED, RED	Panasonic LN1251-C-TR
3	2	R2,R1	Res., Chip 680 0.06W 5%	AAC CR05-681JM
HARDWARE FOR DEMO BOARD ONLY				
1	12	E1-E6,E8,E9,E12-E14,E19	Turret, Testpoint	Mill Max 2501-2
2	8	E7,E10,E11,E15-E18,E20	Turret, Testpoint	Mill Max 2308-2
3	2	JP1,JP2	Headers, 3 Pins 2mm Ctrs.	Samtec TMM-103-02-L-S
4	2	XJP1,XJP2	Shunt, 2mm Ctrs.	Samtec 2SN-BK-G

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