LTC1877/LTC1878
Monolithic Synchronous Step-Down Regulator

DESCRIPTION

Demonstration circuit DC290 is a constant-frequency step-down converter using an LTC®1877 or an LTC1878 monolithic synchronous regulator. The LTC1878 has an input voltage range of 2.65V < V_{IN} < 6V and the LTC1877 has an input voltage range of 2.65V < V_{IN} < 10V. The LTC1878 is optimized for low voltage operation and is ideally suited for single Li-Ion cell or 3-NiCd/NiMH cell applications. The LTC1877, with its higher voltage capability, is ideally suited for two Li-Ion cells or 4- to 6-NiCd/NiMH cell applications.

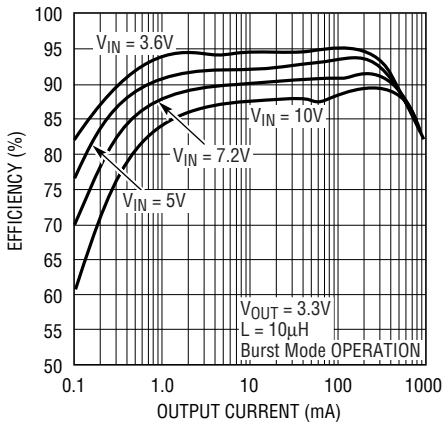
The exclusive use of low profile surface mount components on this demo board results in a highly efficient application in a small volume. The output voltage can be selected from 1.5V, 2.5V, 3.3V or a user programmable voltage, by means of a jumper. The frequency is internally set at 550kHz or can be synchronized with an external clock. The internal switches allow up to 600mA of output current in an MSO8 package, providing a space-efficient solution for battery-powered applications. The DC supply current is typically only 10µA at no load and less than 1µA in shutdown. In switching-noise sensitive applications, Burst Mode™ operation can be inhibited by grounding the SYNC/MODE pin with a jumper or synchronizing it with an external clock. **Gerber files for this circuit board are available. Call the LTC factory.**

PERFORMANCE SUMMARY

SYMBOL	PARAMETER	CONDITIONS	JUMPER POSITION	VALUE
V_{IN}	Input Voltage Range	LTC1877 LTC1878	All (Note 1) All	2.65V to 10V 2.65V to 6V
V_{OUT}	Output Voltage	V_{IN} = 5V, SYNC/MODE = 0V, RUN = 5V, I_{OUT} = 0mA V_{IN} = 5V, SYNC/MODE = 0V, RUN = 5V, I_{OUT} = 0mA V_{IN} = 5V, SYNC/MODE = 0V, RUN = 5V, I_{OUT} = 0mA V_{IN} = 5V, SYNC/MODE = 0V, RUN = 5V, I_{OUT} = 0mA	JP1 = U, JP2 = L, JP3 = “1.5V” JP1 = U, JP2 = L, JP3 = “2.5V” JP1 = U, JP2 = L, JP3 = “3.3V” JP1 = U, JP2 = L, JP3 = “OPEN”	1.51V ± 0.05V 2.52V ± 0.08V 3.33V ± 0.10V (Note 2)

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

EFFICIENCY CURVE



DEMO BOARD

PERFORMANCE SUMMARY

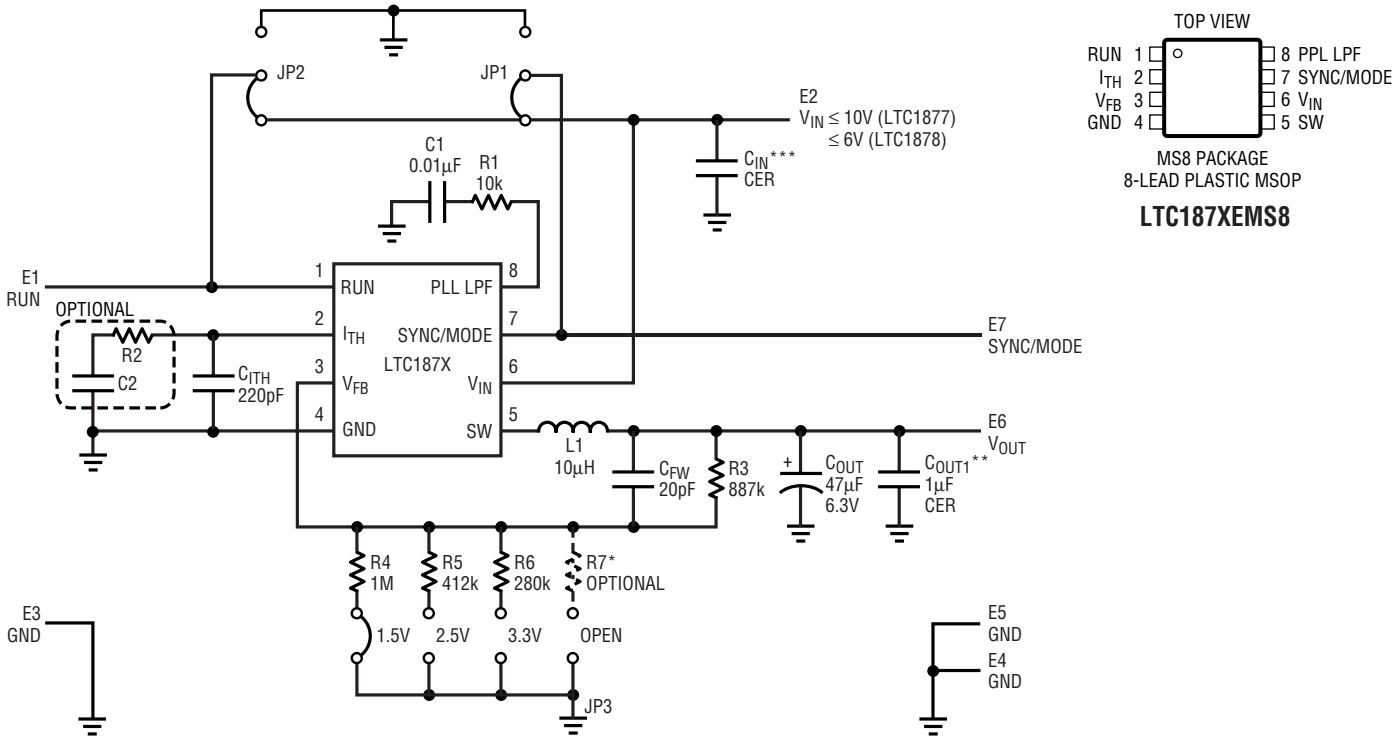
SYMBOL	PARAMETER	CONDITIONS	JUMPER POSITION	VALUE
I_Q	Burst Mode Operation Enabled Supply Current	V_{IN} = 5V, SYNC/MODE = RUN = 5V, I_{OUT} = 0mA	JP1 = JP2 = L, JP3 = "1.5V"	10µA (Note 3)
	Pulse Skipping Mode Supply Current Shutdown Current	V_{IN} = 5V, SYNC/MODE = 0V, RUN = 5V, I_{OUT} = 0mA V_{IN} = 5V, RUN = 0V	JP1 = U, JP2 = L JP2 = U	230µA <1µA
I_{OUT}	Maximum Output Current	V_{IN} = 5V, V_{OUT} = 2.5V (LTC1877) V_{IN} = 4V, V_{OUT} = 2.5V (LTC1878)	JP2 = L, JP3 = "1.5V" JP2 = L, JP3 = "1.5V"	600mA 600mA
f_{OSC}	Operating Frequency	Unsynchronized Synchronized	JP2 = L JP1 = OPEN, JP2 = L	550kHz 400kHz to 700kHz
V_{RIPPLE}	Typical Output Ripple	I_{OUT} = 600mA, V_{IN} = 5V, V_{OUT} = 2.5V	JP2 = L, JP3 = "2.5V"	20mV_{P-P}
V_{OUT}	Typical Load Regulation	0mA < I_{OUT} < 0.6A, V_{IN} = 5V, SYNC/MODE = 0V	JP1 = U, JP2 = L	0.3%
V_{SYNC}	Synchronize Threshold Voltage		All	1.2V
V_{RUN}	Minimum Shutdown Threshold Voltage		All	0.4V

NOTE 1: JP1 and JP2 connect RUN (E1) and SYNC/MODE (E7) to either GND (E3) or V_{IN} (E2). When JP1 or JP2 is in the lower position (L), then RUN or SYNC/MODE is connected to V_{IN}. Alternatively, if JP1 or JP2 is in the upper position (U), then RUN or SYNC/MODE is connected to GND. If external sources drive RUN or SYNC/MODE, then JP1, JP2 or both must be removed.

NOTE 2: Programmable via optional R7. V_{OUT} = 0.8V(1+ 887kΩ/R7)

NOTE 3: With V_{IN} = 5V, the external feedback resistor contributes 0.24µA with JP3 = "1.5V" selected, 0.95µA with JP3 = "2.5V" selected and 1.85µA with JP3 = "3.3V" selected.

PACKAGE AND SCHEMATIC DIAGRAMS



* SPACE PROVIDED FOR AN OPTIONAL RESISTOR TO PROGRAM A CUSTOM OUTPUT VOLTAGE. THE OUTPUT VOLTAGE MUST NOT EXCEED 3.3V.
** C_{OUT1} IS AN OPTIONAL CAPACITOR TO FILTER OUT VERY HIGH FREQUENCY SWITCHING NOISE.
*** C_{IN} = 10µF FOR LTC1877 AND C_{IN} = 22µF FOR LTC1878

Figure 1. LTC1877/LTC1878 Constant Frequency, High Efficiency Converter

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C_{FW}	1	06035A200JAT	20pF 50V Chip NPO Capacitor	AVX	(843) 946-0362
C_{ITH}	1	06035A221JAT	220pF 50V Chip NPO Capacitor	AVX	(843) 946-0362
C1	1	06035C103MAT	0.01µF 50V Chip X7R Capacitor	AVX	(843) 946-0362
C_{IN} (LTC1877)	1	LMK325BJ106MN	10µF 10V Chip X7R Capacitor	TAIYO-YUDEN	(408) 573-4150
C_{IN} (LTC1878)	1	JMK325BJ226MM	22µF 6.3V Chip X5R Capacitor	TAIYO-YUDEN	(408) 573-4150
C_{OUT}	1	6TPA47M	47µF 6V POSCAP Capacitor	SANYO	(619) 661-6835
C_{OUT1}	1	LMK107F105ZA	1µF 10V Chip Y5V Capacitor	TAIYO-YUDEN	(408) 573-4150
E1 to E7	7	2501-2	Turret, Testpoint	Mill-Max	(516) 922-6000
JP1, JP2	2	2802S-03-G1	0.079" Single Row Header	COMM CON	(626) 301-4200
JP3	1	2202S-08-G1	0.079" Double Row Header	COMM CON	(626) 301-4200
JP1 to JP3	3	CCIJ2MM-138G	0.079" Center Shunt	COMM CON	(626) 301-4200
L1	1	A920CY-100M	10µH 20% Inductor	TOKO	(847) 699-3430
R1	1	CR16-103JM	10K 5% 1/16W Chip Resistor	TAD	(714) 255-9123
R3	1	CR16-8873FM	887K 1% 1/16W Chip Resistor	TAD	(714) 255-9123
R4	1	CR16-1004FM	1M 1% 1/16W Chip Resistor	TAD	(714) 255-9123
R5	1	CR16-4123FM	412K 1% 1/16W Chip Resistor	TAD	(800) 508-1521
R6	1	CR16-2803FM	280K 1% 1/16W Chip Resistor	TAD	(800) 508-1521
U1	1	LTC1877/8EMS8	Monolithic Synchronous Step-Down Regulator	LTC	(408) 432-1900
C2			Optional		
R2, R7			Optional		

QUICK START GUIDE

This demonstration board is easily set up to evaluate the performance of the LTC1877 or LTC1878 IC. Please follow the procedure outlined below for proper operation.

- Refer to Figure 5 for proper connection of monitoring equipment to ensure correct measurement.
- Connect the input power supply to the V_{IN} and GND terminals on the left-hand side of the board. Do not increase V_{IN} over its rated maximum supply voltage or the part will be damaged. For the LTC1877 the maximum V_{IN} is 10V and for the LTC1878 the maximum V_{IN} is 6V.
- Connect the load between the V_{OUT} and GND terminals on the right side of the board.
- Select the desired operating mode using JP1 and JP2, as shown in Table 1. JP1 connects SYNC/MODE to GND in the upper position, and connects it to V_{IN} in the lower position. JP2 connects RUN to GND in the upper position, and connects it to V_{IN} in the lower position. If a signal is applied at RUN (E1) or SYNC/MODE (E7), then jumper JP1 or JP2, respectively, must be removed.
- Set the desired output voltage with jumper JP3 as shown in Figure 2.

Table 1. Operating Mode Selection With Jumpers JP1 and JP2

JP2	JP1	OPERATING MODE
UPPER	X	SHUTDOWN
LOWER	UPPER	PULSE SKIPPING
LOWER	LOWER	BURST MODE
LOWER	OPEN	EXTERNAL CLOCK AT SYNC/MODE
OPEN	X	EXTERNAL SIGNAL AT RUN

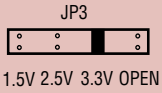


Figure 2. Output Voltage Selection (JP3) (3.3V Position Shown)

OPERATION

INTRODUCTION

The circuit in Figure 1 highlights the capabilities of the LTC1877 and the LTC1878. The LTC1877 and the LTC1878 are high efficiency monolithic synchronous step-down regulators using a fixed-frequency architecture.

This demo board is set up for a variety of output voltages. Output voltages including 1.5V, 2.5V and 3.3V or user programmable voltages can be obtained by selecting the appropriate jumper position. For other output voltages, select the "OPEN" position and add the appropriate resistor value in the space provided. The output voltage must never exceed 3.3V because the output capacitor may be damaged. The input supply can range from 2.65V to 10V for the LTC1877 and 2.65V to 6V for the LTC1878.

The operating frequency of this demo circuit is 550kHz. For other frequencies, JP1 must be removed and SYNC/MODE (E7) synchronized with an external clock. Burst Mode operation is automatically disabled when SYNC/MODE is externally driven. Grounding SYNC/MODE also disables Burst Mode operation, potentially reducing noise and RF interference.

This demonstration board is intended for the evaluation of the LTC1877 and the LTC1878 switching regulator ICs and was not designed for any other purpose.

Main Control Loop (Refer to Functional Diagram)

The LTC1877 and the LTC1878 use a constant frequency, current mode step-down architecture. Their main and synchronous switches, consisting of a top (main) P-channel and a bottom (synchronous) N-channel power MOSFET, are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. The V_{FB} pin allows EA to receive an output feedback voltage from an external resistive divider. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.8V reference, which, in turn, causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{RCMP}, or until the beginning of the next clock cycle.

Comparator OVDET guards against transient overshoots as well as other more serious conditions that may cause an overvoltage condition on the output (> 6.25%). When this condition is sensed, both MOSFETs are turned off until the fault is removed.

Burst Mode Operation

The LTC1877 and the LTC1878 are capable of Burst Mode operation, in which the internal power MOSFETs operate intermittently based on load demand. To enable Burst Mode operation, simply position jumper JP1 in the lower position to connect SYNC/MODE to V_{IN} . To disable Burst Mode operation and enable PWM pulse skipping mode, position JP1 in the upper position to connect SYNC/MODE to GND (see Figure 5). In this mode, the efficiency is lower at light loads, but becomes comparable to Burst Mode operation when the output load exceeds 50mA. The advantage of pulse skipping mode is lower output ripple and less interference to audio circuitry.

When the converter is in Burst Mode operation, the peak current of the inductor is set to approximately 250mA, even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below approximately 0.45V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs. The I_{TH} pin is then disconnected from the output of the EA amplifier and parked a diode above ground.

In sleep mode, both power MOSFETs are held off and the internal circuitry is partially turned off, reducing the quiescent current to 10µA. The load current is now being supplied from the output capacitor. When the output voltage drops, the I_{TH} pin reconnects to the output of the EA amplifier and the top MOSFET is again turned on and this process repeats.

OPERATION

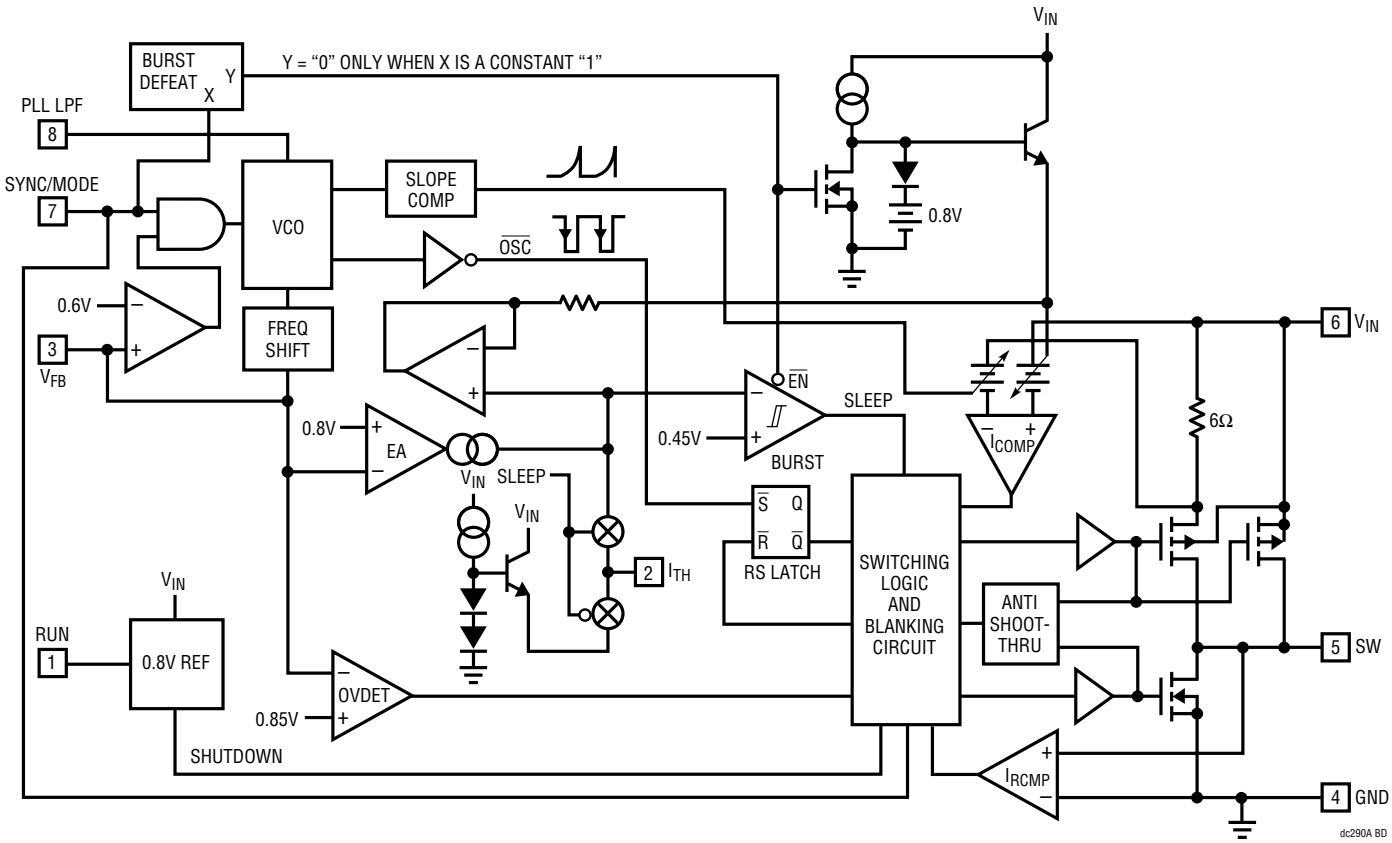


Figure 3. Functional Block Diagram

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 80kHz, one-seventh of the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 550kHz (or the synchronized frequency) when V_{FB} rises above 0.3V.

Frequency Synchronization

A phase-locked loop (PLL) is available on the LTC1877 and the LTC1878 to allow the oscillator to be synchronized to an external source connected to the SYNC/MODE pin. The output of the phase detector at the PLL LPF pin operates over a 0V to 2.4V range, corresponding to 400kHz to 700kHz. When locked, the PLL aligns the turn-on of the MOSFETs to the rising edge of the synchronizing signal.

When the LTC1877 or the LTC1878 is clocked by an external source, Burst Mode operation is disabled; the LTC1877 or the LTC1878 then operates in PWM pulse skipping mode. In this mode, when the output load is very low, the current comparator, I_{COMP}, may remain tripped for several cycles and force the main switch to stay off for the same number of cycles. Increasing the output load slightly allows constant frequency PWM operation to resume.

Frequency synchronization is inhibited when the feedback voltage, V_{FB}, is below 0.6V. This prevents the external clock from interfering with the frequency foldback for short-circuit protection.

OPERATION

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

Low Supply Operation

The LTC1877 and the LTC1878 can function on an input supply voltage as low as 2.65V. The maximum allowable output current is reduced at this low voltage because the $R_{DS(ON)}$ of the P-channel switch increases. Therefore, the user should calculate the power dissipation when the LTC1877 or the LTC1878 is used at 100% duty cycle with low V_{IN}. See the LTC1877 or the LTC1878 data sheet for additional information.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished by internally adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. As a result, the maximum inductor peak current is reduced for duty cycles >40%. See the inductor peak current as a function of duty cycle graph in Figure 4.

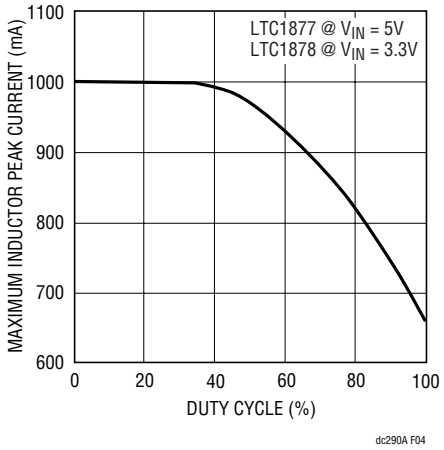


Figure 4. Maximum Inductor Peak Current vs Duty Cycle

How To Measure Voltage Regulation

When trying to measure voltage regulation, remember that all measurements must be taken at the point of regulation. This point is where the LTC1877's and LTC1878's control loop looks for the information to keep the output voltage constant. In this demonstration board, this point occurs between V_{OUT} (E6) and GND (E4). Measurements should be taken at these points and not at the end of test leads at the load. Refer to Figure 5 for the proper monitoring equipment configuration.

This applies to line regulation (input-to-output voltage regulation) as well as load regulation tests. In doing the line regulation tests, always look at the input voltage across the input terminals, V_{IN} (E2) and GND (E3) .

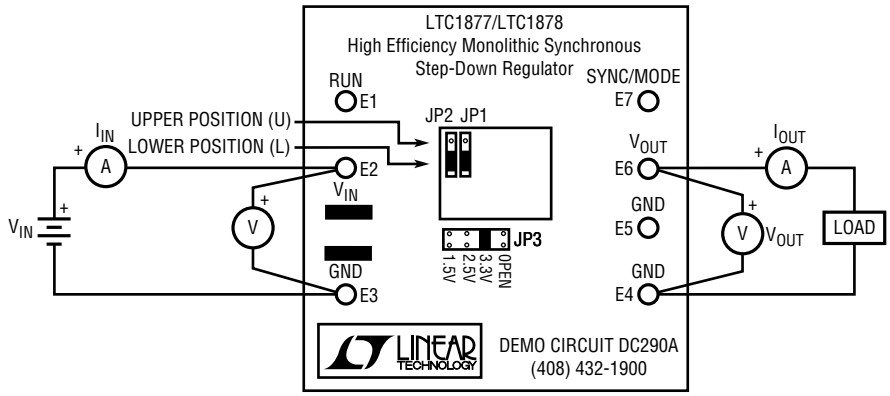


Figure 5. Proper Measurement Setup

For the purposes of these tests, the demonstration circuit should be powered from a regulated DC bench supply, so that variations on the DC input do not add errors to the regulation measurements.

Another source of error may be the use of small spring-clip leads when testing this circuit. Small spring-clip leads are very convenient for small-signal bench testing and voltage measurements, but should not be used with this circuit. Soldered wire connections are required to properly ascertain the performance of the PC board.

Checking Transient Response

Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing, which would indicate a stability problem. The external components shown in Figure 1 will prove adequate for most applications.

Long supply leads connected to V_{IN} and GND may induce ringing at V_{IN} and V_{OUT} resembling loop instability. This is actually caused by the inductance of the long wires resonating with the input ceramic capacitor. This phenomenon is particularly pronounced when a ceramic output capacitor is used. When using short leads to connect V_{IN} and GND is impractical, a 100µF electrolytic bulk capacitor can be soldered onto the board between V_{IN} and GND. This should eliminate all ringing associated with long V_{IN} and GND leads. Space is provided on the PC board for this purpose, as shown in Figure 6.

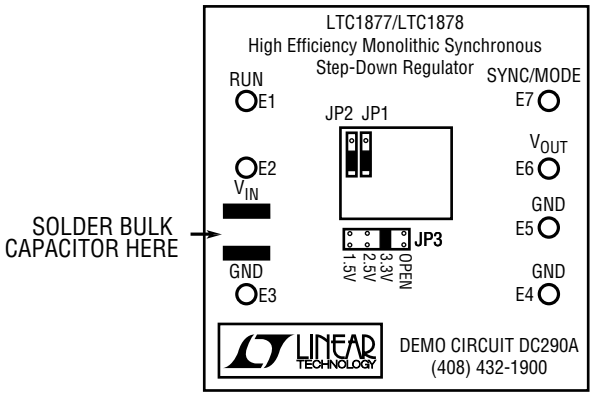


Figure 6. Space Provided for a Bulk Capacitor

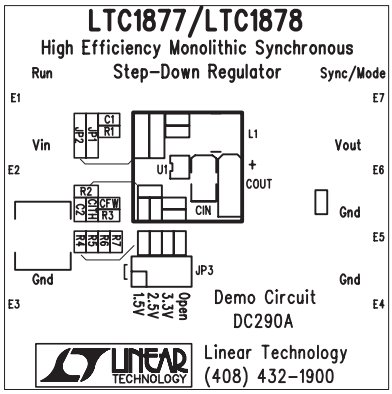
Component Manufacturers

Table 2 is a partial list of manufacturers of components that can be used in LTC1877 and LTC1878 applications. Using components other than the ones supplied on the demonstration board will require careful analysis to verify that all component specifications are not exceeded. Finally, recharacterizing the circuit for efficiency is necessary.

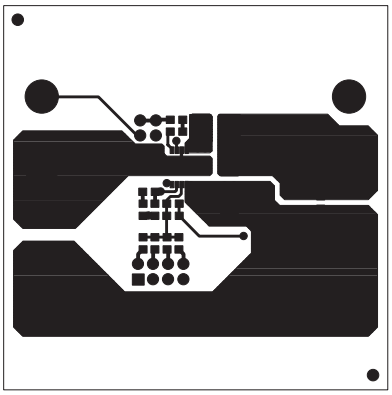
Table 2. List of Alternative Component Manufacturers

MANUFACTURER	DEVICE	PHONE	FAX
Central Semiconductor	Diodes	(516) 435-1110	(516) 435-1824
Coilcraft	Inductors	(847) 639-6400	(847) 639-1469
Coiltronics	Inductors	(561) 241-7876	(561) 241-9339
Dale	Inductors	(605) 665-9301	(605) 665-0817
International Rectifier	Diodes	(310) 322-3331	(310) 322-3332
ON Semiconductor	Diodes	(602) 244-6600	(602) 244-4015
Zetex	Diodes	(631) 543-7100	(631) 864-7630
Murata-Erie	Capacitors	(770) 436-1300	(770) 436-3030
Sprague	Capacitors	(207) 324-4140	(603) 244-1430
Sumida	Inductors	(847) 956-0667 [81] 03-3607-5111	(847) 956-0702 [81] 03-3607-5114
TDK	Inductors	(847) 803-6100	[81] 03-3278-5358

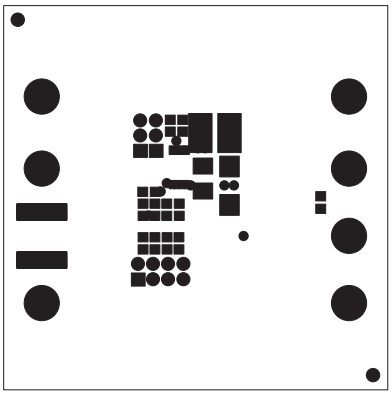
PCB LAYOUT AND FILM



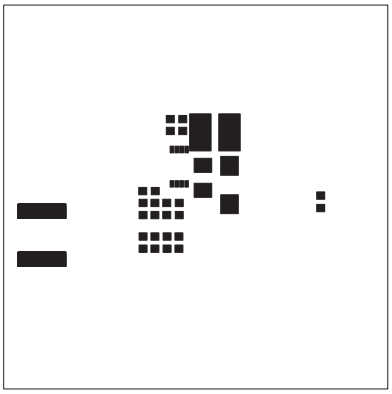
Silkscreen Top



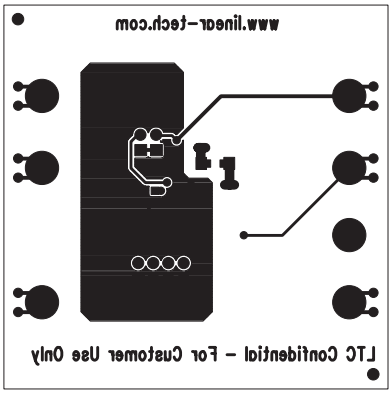
Component Side



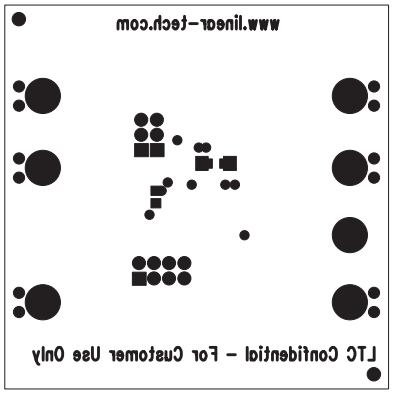
Solder Mask Top



Paste Mask Top

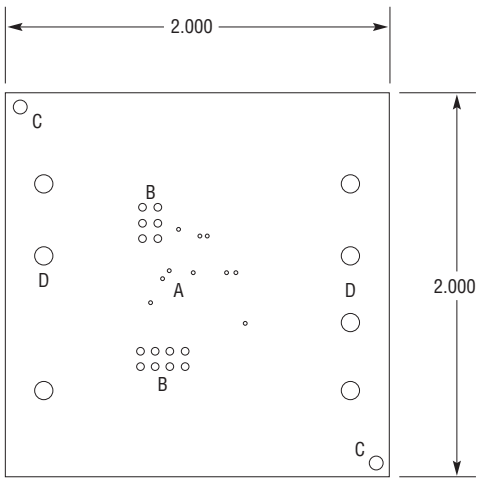


Solder Side



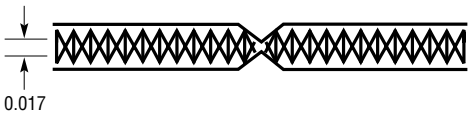
Solder Mask Bottom

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL; FR4 OR EQUIVALENT EPOXY, 2 OZ COPPER CLAD THICKNESS 0.031 ± 0.006 TOTAL OF 2 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015 MAX COPPER PLATE ELECTRODEPOSITED TIN-LEAD COMPOSITION BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK; BOTH SIDES USING GREEN PC-401 OR EQUIVALENT
4. SILKSCREEN; USING WHITE NONCONDUCTIVE EPOXY INK
5. ALL DIMENSIONS ARE IN INCHES
6. SCORING:



SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.020	10	YES
B	0.040	14	YES
C	0.072	2	NO
D	0.095	7	YES

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