

# LT6372-1/LT6372-0.2 Precision, Low Drift, Low Noise Instrumentation Amplifiers

## DESCRIPTION

Demonstration circuit 2746A is a blank/un-stuffed evaluation board to be used to facilitate prototyping of [LT<sup>®</sup>6372-1](#) and [LT6372-0.2](#) instrumentation amplifiers in the MSOP-16 package. The board is designed to be as flexible as possible by providing many stuffing options and jumpers to configure. This board can be used with either LT6372-1 (for gains  $\geq 1\text{V/V}$  amplification) or LT6372-0.2 (for gains as low as  $0.2\text{V/V}$  attenuation).

Below are some of the capabilities of the board using board jumper selection or stuffing option.

1. Single or dual supply operation.
2. Flexible connections of REF1 and REF2 instrumentation amplifier reference voltage inputs. Options are: Both references to be tied together or separately driven, or grounded.

3. Common mode or differential input.
4. Input CM and differential filtering caps if needed.
5. Upper and lower clamp pins driven externally or disabled.
6. Output drive filtering and isolation resistor and cap.
7. Prototyping area provided for SO-8 device to be used if needed. This prototype footprint can be run using the LT6372 power supplies or could be powered by different supply rails applied to the board.

**Design files for this circuit board are available.**

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## BOARD PHOTO

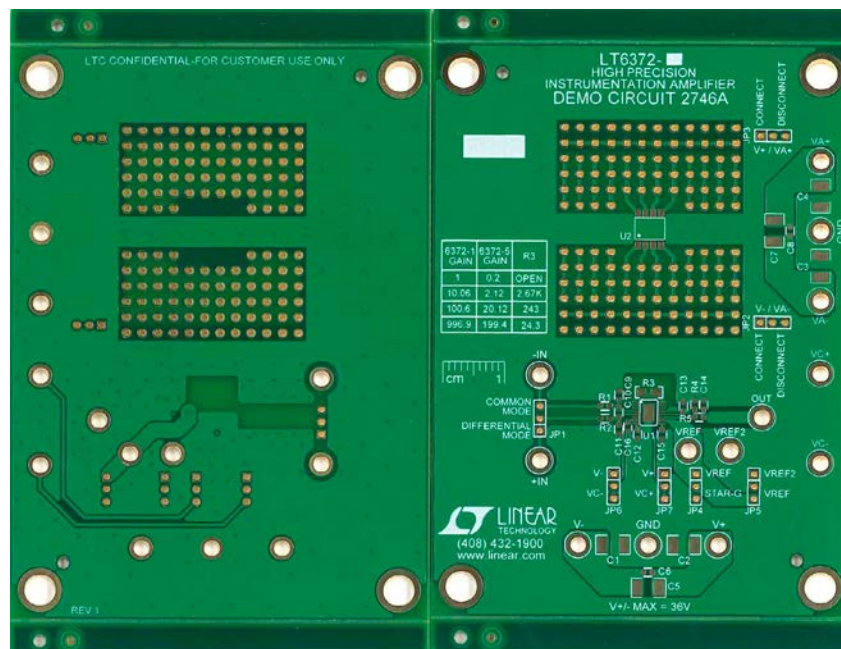


Figure 1. DC2746A Top and Bottom Board Views

## QUICK START PROCEDURE

Here are some of the highlights of operating the DC2746A to evaluate the LT6372.

1. **Gain:** Set by setting the value of R3.
2. **LT6372 Operating Supplies:** For dual supply operating, apply complimentary power supplies to  $V^-$  and  $V^+$  test points. Do not exceed  $\pm 18V$ .

For single positive supply operation,  $V^-$  can be tied to GND and  $V^+$  should be driven by external positive power supply.

3. **Inputs:** To be brought in at +IN and -IN test points. CM filtering can be implemented by using C8, and C11. Differential mode filtering is with C10 if needed. Use JP1 to switch between differential mode (normal In-Amp operation) or common mode (for testing the LT6372 CM rejection) configuration. If the input is single ended, put JP1 in differential mode (or unstuffed) and ground either  $IN^+$  (or  $IN^-$ ) and apply the input to the other  $IN^-$  (or  $IN^+$ ).
4. **Reference Inputs:** REF1 pin can be driven externally ( $V_{REF}$  test point) with JP4 set to  $V_{REF}$  (or unstuffed). To ground REF1, move JP4 to STAR-G position.

REF2 pin can be driven externally ( $V_{REF2}$  test point) with JP5 set to  $V_{REF2}$  or unstuffed. To run REF2 with the same voltage as REF1, move JP5 to  $V_{REF}$  position.

5. **Output:** Available at OUT test point. R5, and R4 can be used to set any output isolation or load if needed. C14 can be used to do some low pass filtering with R5, if needed. When used to drive an ADC at OUT test point, C14 can be used for charge storage to improve the ADC analog input settling time due to ADC input charge kick back.
6. **Clamps:** For positive/high side clamping, apply the appropriate clamp voltage to CLHI test point and move JP7 to CLHI position. To disable positive clamping, move JP7 to the  $V^+$  position.

For negative/low side clamping, apply the appropriate clamp voltage to CLLO test point and move JP6 to CLLO position. To disable negative clamping, move JP6 to the  $V^-$  position.

### Example Configuration Setup

As an example, Figure 2, is a typical application using DC2746A. Figure 2 shows the LT6372-x configured to drive an ADC with clamps set to limit the output swing.

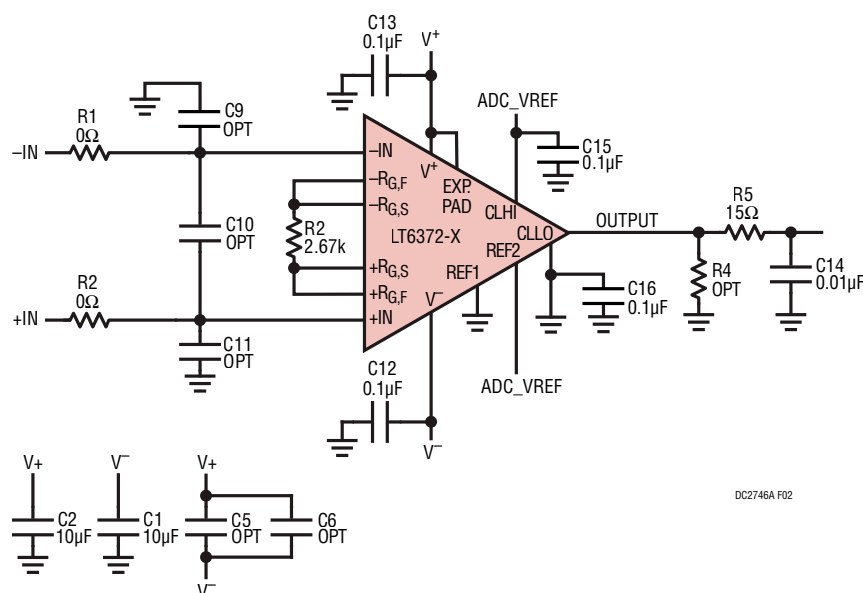
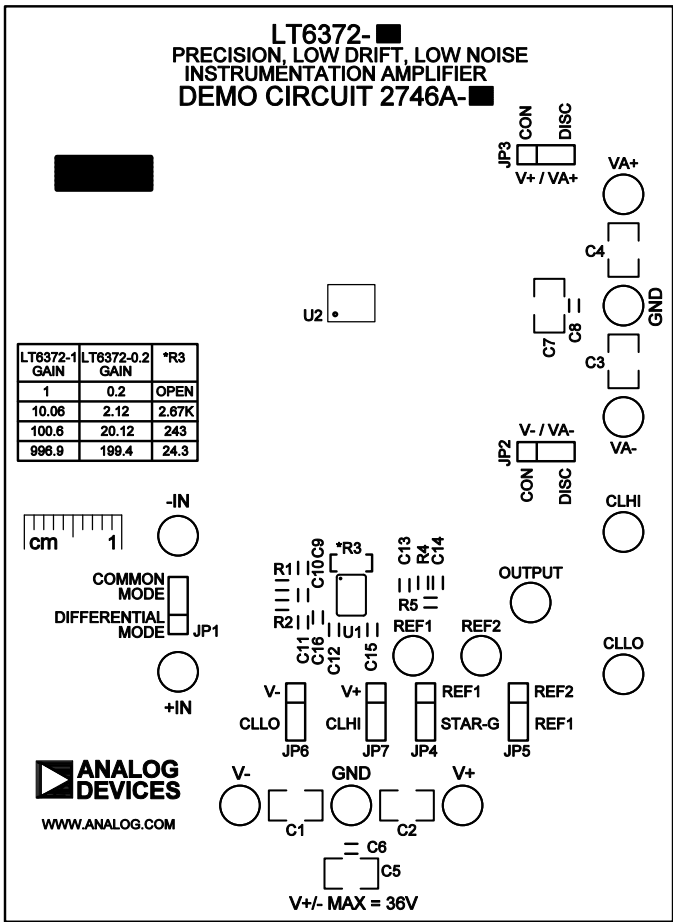


Figure 2. Typical LT6372-X Example Configuration to Drive an ADC

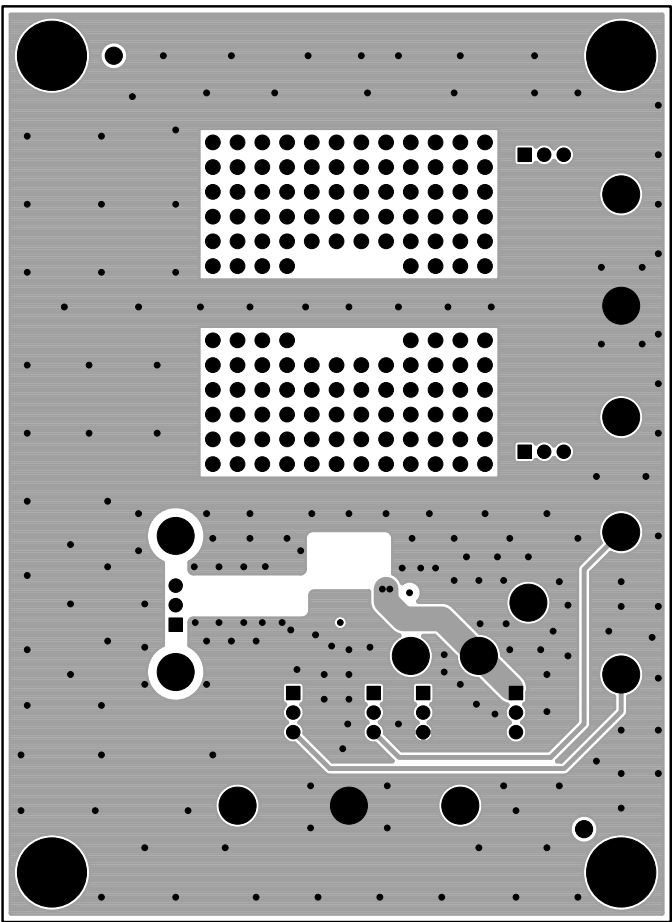
QUICK START PROCEDURE

Table 1. Jumper Settings to Configure the DC2746A Demo Board to the Schematic (Figure 2)

CONDITION/SETUP	JUMPER	SET	NOTES
Diff Input	JP1	Differential	Allows Diff Input to the In-Amp
REF1 Grounded	JP4	STAR_G	Grounds REF1 Pin
REF2 Tied to ADC_VREF	JP5	REF2/Open	Apply Ext ADC_VREF to REF2 Test Point
Clamp HI to ADC_VREF	JP7	CLHI	Apply Ext ADC_VREF to CLHI Test Point
Clamp LO to GND	JP6	CLLO	Apply GND to CLLO Test Point
Proto-Board Area Powered by LT6372-X Power Supplies	JP2/JP3	Connect	Opt Device in U2 Footprint Powered from LT6372 Supplies



SILKSCREEN TOP  
DEMO CIRCUIT 2746A-A/B-2



BOTTOM SIDE  
DEMO CIRCUIT 2746A-A/B-2

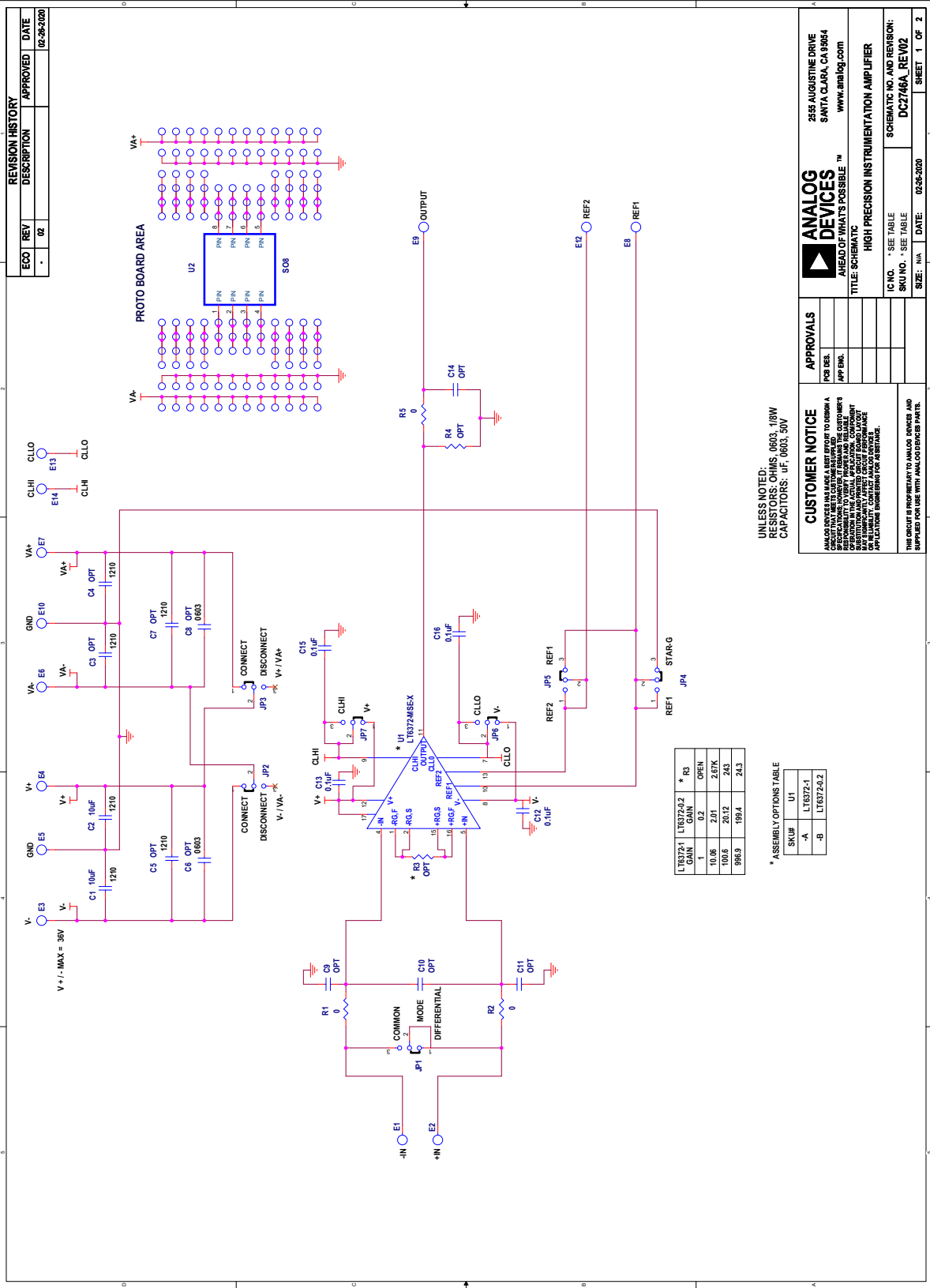
Figure 3. DC2746A PCB Layout Drawing (Top and Bottom View)

# DEMO MANUAL DC2746A

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	2	C1, C2	CAP. CHIP, X7R, 10µF, 50V, 10%, 1210	SAMSUNG, CL32B106KBJNFNE
2	0	C3, C4, C5, C7	CAP. CHIP, 1210	OPT
3	0	C6, C8	CAP. CHIP, 0603	OPT
4	0	C9-C11, C14	CAP. CHIP, 0805	OPT
5	2	C12, C13	CAP. CHIP, X7R, 0.1µF, 50V, 10%, 0603	AVX, 06035C104KAT2A
6	3	R1, R2, R5	RES. CHIP, 0Ω, 1%, 0805	VISHAY, CRCW08050000Z0EA
7	0	R3, R4	RES. CHIP, 0805	OPT
8	7	JP1-JP7	HEADER, 3PINS, 2mm	WURTH, 62000311121
9	7	JP1-JP7	SHUNT 2mm 1×3	WURTH, 60800213421
10	10	E1-E10	TURRET, 0.09" DIA	MILL-MAX, 2501-2
11	1	U1	LT6372	ANALOG DEVICES, LT6372-X
12	0	U2	OPTIONAL BREAD-BOARDING AREA/DEVICE	OPT

SCHEMATIC DIAGRAM



# DEMO MANUAL DC2746A

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## ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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