Demo Board DC245 Quick Start Guide

Demo board DC245 features the LTC1668 16-bit high speed, current output DAC in combination with an LT1460-2.5 reference, an output transformer, bypass, termination or provision for termination on the digital inputs and the analog outputs, as well as various jumpers for configuration. The board uses SMA connectors for the analog output, reference and clock input. The digital signals are received on a 40-pin, dual-row 0.1" header, allowing various flat cable connectors to be used.

Clock Input

Although the clock can be received on the 40-pin header (Pin 35/J3), the performance of the DAC is very dependent on a low jitter clock. Best results will be achieved by providing the clock signal to the SMA connector (J6) labeled EXT CLK. This input is terminated with 50Ω. A clock source with 50Ω output impedance must be configured to produce full TTL/CMOS logic levels at J6, taking into consideration the 50Ω load. Care should be taken to ensure that the clock input, as well as the data inputs, are not overdriven. For the clock line, a cable with well-controlled impedance must be used or reflections from impedance discontinuities can rapidly degrade the phase jitter performance if the clock waveform exhibits any variable artifacts within several transit times prior to crossing the threshold region.

For example, the slew rate of the clock signal is modulated by power supply voltage, a common effect in canned oscillators or logic gates. The signal exhibits nominally 1ns from the root to the transition region; a transmission line length of about 8.5 inches will place the first reflections of the initial artifacts of the edge at the DAC just as it passes through the transition region. If the transmission line length is 4.25 inches, the 2nd reflection will arrive at the DAC just as the clock crosses the transition region. If the cable is much longer, the reflections of previous edges, and hence duty cycle variation, may compromise jitter performance. For example, if a 50MHz clock is used and the cable is 28 inches long, the 2nd reflection of the previous edge will arrive back at the DAC during the transition region It is advisable that the cable length for 2ns rise-time clock signals be greater than 8.5 inches, but less than 28in or even 20in. If the reflections arrive in the transition region of a 2ns rise time, a reflection with a 7mV amplitude will produce a shift in timing of 3ps. This timing shift, if static, will not create a discernable effect. However, the arrival of the reflections in the neighborhood of the threshold region of the clock driver will result in an exaggeration of any slew-rate variation or threshold variation due to power supply noise. The resulting phase noise will degrade the signal-to-noise ratio and could be misinterpreted as poor power supply rejection. The above assumes a propagation speed of 69% of the speed of light, which is approximately what is seen in 50Ω coaxial cables, and somewhat less than that of 75Ω strip-line traces on printed circuit boards. Both transmission-line geometry and dielectric constants in the neighborhood of the conductor determine propagation speed. Reflections from impedance discontinuities can be minimized if the impedance at the driven end of the transmission line is well matched to the characteristic impedance of the transmission line. Some other

effects that can contribute to phase jitter include:

❏ Supply variation at the DAC, which will shift the thresholds

❏ Ringing effects in lead inductance in conjunction with lumped capacitance

❏ Digital noise within the clock driver, modifying the substrate potential

❏ RFI pick-up on the clock line

❏ Noise from switching supplies

❏ Digital signals that are directly coupled into traces carrying the clock

❏ Piezoelectric effects in ceramic capacitors, appearing as ringing in the MHz region

The jitter requirements of the external clock generator must be understood in terms of the degradation introduced in the SNR of the waveform being produced. As an example, if the part generates a 5MHz sine wave, 1ps RMS jitter will limit the signal-to-noise ratio to 90dB, assuming a full-scale signal. If an oscillator with commonly available 15ps phase jitter specs is used, the resulting signal-to-noise ratio will be degraded to 66.5dB. If the output frequency is closer to Nyquist, phase jitter becomes even more critical.

Note that the clock cable should be short, as longer cables increase the likelihood of reflections from impedance discontinuities degrading performance. Be aware that "Y" or "T" connections to other instruments, retiming stages or monitors can introduce a transmission line stub or impedance discontinuity that will degrade results.

Power Requirements

The board requires ±5V supplies for operation. The +5V supply is brought out separately for both analog and digital power. The –5V supply is required for the analog output. The analog power supply should be well bypassed and regulated; the digital power supply should emulate that of the target system.

Output Transformer

DC245 is provided with an output transformer that demonstrates the operation of the LTC1668 into a load via a transformer. This transformer-coupled output appears on J4. As configured, this output is intended to operate into an external 50Ω load. R8, shown as 50Ω on the schematic, is not installed.
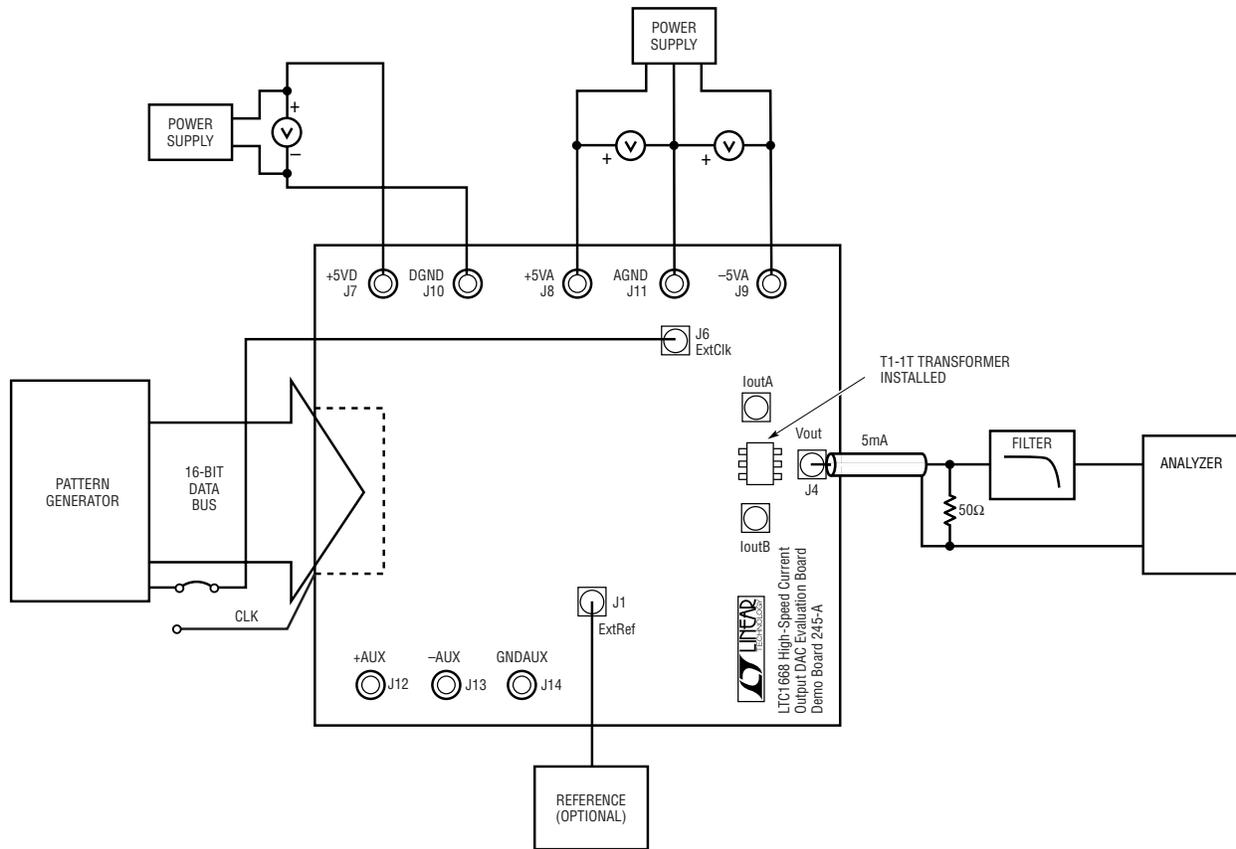
Figure 1. DC245 Connection Diagram

The board is populated with very low profile socket pins to allow substitution of a suitable transformer for your application. You must evaluate the DAC with a transformer that is appropriate for your application. This transformer output has an isolated ground, allowing you to determine the effect of primary-to-secondary coupling effects in your transformer. In some systems or with some transformers, this ground is best left floating; however, in other cases, it is best grounded to the analog plane. These connections must be made with soldered links using braid or copper tape. Make the connection from the pins of J4 to the pins of J2 and J5. The best transformers for isolated operation will likely have double Guassian shields.

Note that the choice of transformer can have a strong effect on harmonic distortion and intermodulation distortion performance, as well as impedance, and signal levels. The output voltage is determined by the turns ratio, as well as the line impedance reflected into the DAC.

If you need further information of the suitability of various types of transformers, contact Linear Technology, or consult the available literature on impedance matching and transformer characteristics.

If the DAC is to be used without an output transformer, for example connected to op amp I-V converters, cascode stages or low impedance loads, directly or via cables, the transformer must be removed. The direct outputs appear on J2 (I_{OUT}^+) and J5 (I_{OUT}^-). JP6 and JP7 allow 50Ω loads

(R9 and R10) to be placed at the outputs. If terminators are located at the far end of coaxial lines or other transmission lines, these jumpers need not be installed. If the impedance at the receiving end of a transmission line is greater than 50Ω (for example, a twisted pair), R5 and R6 can be used to reduce the impedance seen by the DAC to a 50Ω level.

Patterns or Waveform Data

Note that your success with transformer coupled operation is in part determined by the patterns you send to the DAC. If you send a waveform that does not have balanced volt-seconds, you will develop a net magnetic bias in the transformer that can degrade results due to saturation effects. Transformers with larger cores will be less affected by this imbalance. If you find that intermodulation distortion and harmonic distortion are changing over time, you should examine your data word patterns for this imbalance.

Appropriate test waveforms are very much determined by your application, as well as by your means for evaluating the output. If you are using an FFT-based spectrum analysis system, your waveforms and clock will likely need to be coherent with the sampling of the output waveform.

Your data collection may need to take multiple samples and average the output spectrum in order to determine spurious free dynamic range, which will often be hidden below the noise floor dictated by the phase jitter on the clock. If the DAC is feeding wide-band I-V converters, it is very likely that spurs or harmonics will be hidden below the noise floors of the amplifiers.

Digital Inputs

The 40-pin flat cable connector interleaves ground and power with signals such that flat cables with individual twisted pairs can be considered. Alternatively, shielded flat cables or flat cables with integral ground planes can be used. The digital lines have 22Ω termination in series with the DAC input capacitance. At the highest frequency component of a 50MHz data rate, this produces an impedance that is close to the characteristic impedance of the traces, as well as that of the twisted pair cable. The board also has provision for pull-down/-up SIP resistor networks prior to (RN1, 2, 7, 8) or after (RN3, 4, 9, 10) the 22Ω series resistors to allow for optimization for different characteristic impedance or signal levels. Excessive signal amplitude or slew rates may have detrimental effects. Buffers with controlled slew rates may be best. Note that digital feed-through effects may occur if long cables are placed carelessly. Digital signals can radiate noise that can be received by other portions of your setup. Placing all elements of your setup on a conductive plane may produce the best results. In any case, the digital cable should be as short as possible. Shielding digital portions of your setup from the analog may be advisable. The data port connector should be designed to mate with an AMP 102159-9 connector (male).

Timing

Data set-up and hold times must be respected or results will be severely compromised. Data from low end equipment may need to be retimed with the low jitter clock source, possibly necessitating a FIFO in order to allow a lower precision instrument or phase-locked loop to maintain lock without compromising phase noise. If the low jitter clock originates in the instrument producing EXT CLK, the data may not need retiming. In the event that a low jitter clock is used to retime the data, reverse feedthrough from a complex device such as a FPGA may compromise the clock presented to the DAC. Also, the introduction of a CMOS buffer in the clock line from a low jitter oscillator may compromise the phase jitter performance to the extent that the DAC performance is significantly affected. If a clock buffer introduces jitter in the data, relative to the low jitter clock, and set-up and hold times are not compromised, results should be acceptable.

If the clock source under evaluation cannot drive 50Ω, you may use the connection at J3/pin 35 or, alternatively, the demo board can be mounted on a breadboard, with the 50Ω clock termination removed and a very short SMA cable (1–2 inches) to J6, or a direct connection can be wired to EXTCLK.

Jumpers

JP1 allows the selection of the external reference, LT1460 (U1) or REFOUT.

JP2 allows the insertion of a common pull-up to +5V (R4) (common point TP3).

JP3 and JP4 allow the introduction of pull-up resistors R5 and R6 (not installed) at the output.

TP3 allows the voltage at this common point to be controlled or measured. The node at TP3 is bypassed to ground in order to maintain a low AC impedance.

JP5 allows the LADCOM node to be disconnected from ground for test purposes.

JP6 and JP7 allow ground-referred load resistors to be introduced in the output.

JP8 allows disconnection of the transformer center-tap from ground and, via TP4, permits the introduction of an alternate voltage or allows current monitoring. The node at TP4 is bypassed to Ground.

JP9 allows the selection of EXT CLK or clock input from the data port (J3, pin 35).

Other Test Points

TP2: 2.5V V_{REF} (after jumper)

TP6: +5V digital

TP7: +5V analog

TP8: –5V analog

R2 is a potentiometer to allow full scale adjustment of I_{REF}.

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