LTC2261-14 and LTC6409 12-/14-Bit, 25Msps to 150Msps ADC Combo Board

DESCRIPTION

Demonstration circuit 1760A supports a family of 14-/12-bit 25Msps to 150Msps ADCs and an LTC®6409 low noise amplifier. Each assembly features a device from the LTC2261-14 family of high dynamic range 1.8V ADCs and a LTC6409 low noise amplifier.

Demonstration circuit 1760A supports the LTC2261-14 family full rate CMOS and DDR CMOS output mode. The circuitry on the analog inputs is optimized for analog input frequencies from DC to 100MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage—ADC	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 150mA	Optimized for 3.3V [3.0V ⇔ 3.5V Min/Max]
Supply Voltage—Amplifier	Depending on Supply Voltage Used, This Supply Must Provide Up to 25mA	Optimized for 3.0V [2.7V ⇔ 5.0V Min/Max]
Analog Input Range	Depending On Sense Pin Voltage	$1V_{P-P}$ to $2V_{P-P}$
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (OV_{DD} = 1.8V)	Minimum High Level Output Voltage	1.750V (1.790V Typical)
	Maximum Low Level Output Voltage	0.050V (0.010V Typical)
Sampling Frequency (Convert Clock Frequency)	Depending on ADC This Can Vary Between 20Msps and 125Msps	LTC2261-14 = 125Msps
Convert Clock Level	Single-Ended Encode Mode (ENC^- Tied To Gnd)	0V to 3.6V
Convert Clock Level	Differential Encode Mode (ENC^- Not Tied to GND)	0.2V to 3.6V
Resolution	14 Bits	
Input Frequency Range	DC-100MHz	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1760A is easy to set up to evaluate the performance of the LTC2261-14 family of A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC890 QuikEval™-II data acquisition and collection system was supplied with the DC1760A demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1760A and to a PC.

DC1760A Demonstration Circuit Board Jumpers

The DC1760A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1).

PAR/SER: Selects parallel or serial programming mode (Default: Serial).

Duty Cycle Stabilizer (DCS): In parallel programming mode enables/disable Duty Cycle Stabilizer (Default: Enable).

SHDN: In parallel programming mode enables and disables the LTC2261-14 (Default: Enable).

LVDS: In parallel programming mode selects between CMOS and LVDS outputs. (Default: LVDS, required for serial programming mode. When using parallel mode the required setting is CMOS).

AMP_SHDN: Enables and disables the LTC6409. (Default: Enable)

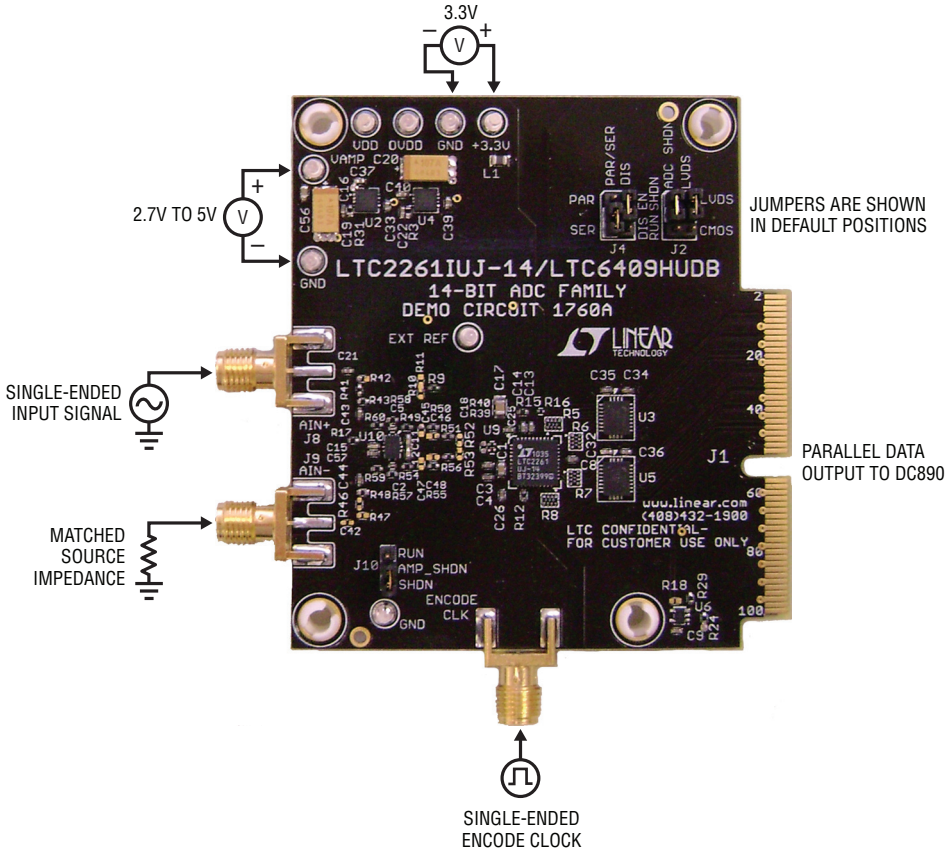


Figure 1. DC1760 Setup (Zoom for Detail)

QUICK START PROCEDURE

Applying Power and Signals To The FT996 Demonstration Circuit

If a DC890 is used to acquire data from the DC1760A, the DC890 must **first** be connected to a powered USB port or provided an external 6V to 9V **before** applying 3.0V to 6.0V across the pins marked +3.3V and GND, or 2.7V to 3.5V on the V_AMP pin on the DC1760A. The DC1760A requires 3.3V on the ADC input for proper operation, regulators on the board produce the voltages required for the ADC. The voltage applied to the amplifier is not regulated. The DC1760A demonstration circuit requires up to 150mA on the ADC input depending on the sampling rate and the A/D converter supplied, and up to 25mA on the amplifier power input.

The DC890 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an unpowered hub in which case it must be supplied an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

Analog Input Network

The DC1760A can be driven from a differential or single-ended source. If the DC1760A is driven from a single-ended source applied to the AIN+ connector (J8), the equivalent impedance characteristic should be seen on the AIN– connector (J9). If there is a difference in the impedance characteristic between the two input ports common mode noise sources in the amplifier will translate to differential mode noise and will raise the noise floor.

For optimal distortion and noise performance the filter network can be optimized for different analog input frequencies. Refer to the LTC6409 data sheet for information on setting the gain and input impedance of the LTC6409.

In almost all cases, filters will be required on both analog input and encode clock to produce maximum SNR. In the case of the DC1760A the bandpass filter used for the clock should be used prior to the DC1075A clock divide board. The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

Encode Clock

Note: Apply an encode clock to the SMA connector on the DC1760A demonstration circuit board marked J7. As a default the DC1760A is populated to have a single-ended input.

For the best noise performance, the encode input must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2261-14 ADC family.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1760A a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

Apply the analog input signal of interest to the SMA connectors on the DC1760A demonstration circuit board marked J5 and J3. This combo board is currently populated to receive a differential signal.

An internally generated conversion clock output is available on J1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval-II Data Acquisition Board using PScope™ software.

QUICK START PROCEDURE

Software

The DC890 is controlled by the PScope system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if PScope.exe, is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1760A demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1760A, and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.

Under the Configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options, see Figure 2:

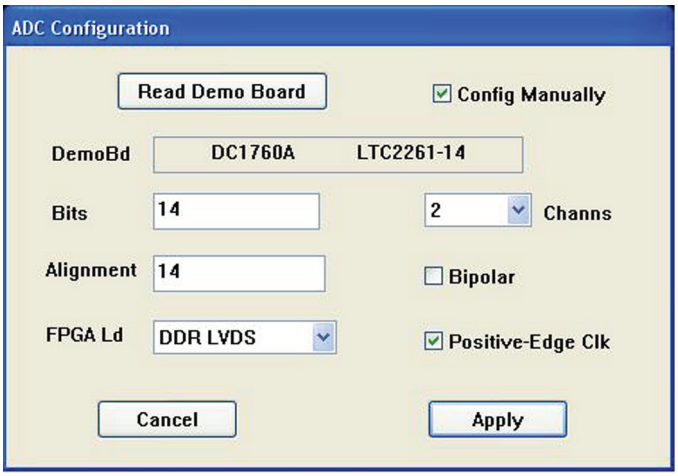


Figure 2. ADC Configuration

Manual configuration settings:

Bits: 14

Alignment: 14

FPGA Ld: CMOS

Channs: 2

Bipolar: Un-checked

Positive-Edge Clk: Checked

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

Serial Programming

PScope has the ability to program the DC1760A board serially through the DC890. There are several options available in the LTC2261-14 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

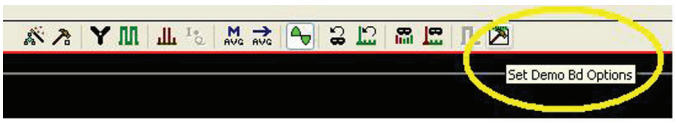


Figure 3: PScope Toolbar

This will bring up the menu shown in Figure 4.

QUICK START PROCEDURE

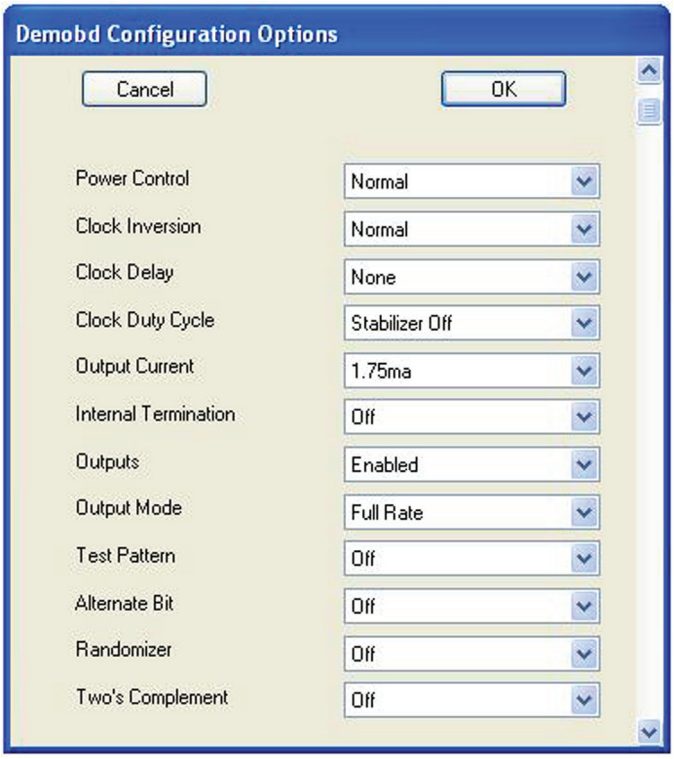


Figure 4: Demobd Configuration Options.

This menu allows any of the options available for the LTC2261-14 family to be programmed serially. The LTC2261-14 family has the following options:

Power Control: Selects between normal operation, nap and sleep modes.

- Normal (Default) – Entire ADC is powered, and active.
- Nap – ADC core powers down while references stay active.
- Shutdown – The entire ADC is powered down.

Clock Inversion: Selects the polarity of the CLKOUT signal:

- Normal (Default) – Normal CLKOUT polarity
- Inverted – CLKOUT polarity is inverted

Clock Delay: Selects the phase delay of the CLKOUT signal:

- None (Default) – No CLKOUT delay
- 45° – CLKOUT delayed by 45°
- 90° – CLKOUT delayed by 90°
- 135° – CLKOUT delayed by 135°

Clock Duty Cycle: Enables or disables Duty Cycle Stabilizer.

- Stabilizer off (Default) – Duty Cycle Stabilizer disabled
- Stabilizer on – Duty Cycle Stabilizer enabled

Output Current: Selects the LVDS output drive current. This option is not used on the FT1370.

- 1.75mA (Default) - LVDS output driver current
- 2.1mA - LVDS output driver current
- 2.5mA - LVDS output driver current
- 3.0mA - LVDS output driver current
- 3.5mA - LVDS output driver current
- 4.0mA - LVDS output driver current
- 4.5mA - LVDS output driver current

Internal Termination: Enables LVDS internal termination This option is not used on the FT1370.

- Off (Default) – Disables internal termination
- On – Enables internal termination

Outputs: Enables Digital Outputs.

- Enabled (Default) – Enables digital outputs
- Disabled – Disables digital outputs

QUICK START PROCEDURE

Output Mode: Selects Digital output mode.

- Full Rate (Default) – Full rate CMOS output mode (This mode is not supported by the DC1760A).
- Double LVDS – double data rate LVDS output mode
- Double CMOS – double data rate CMOS output mode (This mode is not supported by the DC1760A).

Test Pattern: Selects Digital output test patterns.

- Off (Default) – ADC data presented at output
- All out =1 – All digital outputs are 1
- All out = 0 – All digital outputs are 0
- Checkerboard - OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.
- Alternating – Digital outputs alternate between all 1's and all 0's on alternating samples.

Alternate Bit: Alternate Bit Polarity (ABP) mode.

- Off (Default) – Disables alternate bit polarity
- On – Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

Randomizer: Enables Data Output Randomizer.

- Off (Default) – Disables data output randomizer
- On – Enables data output randomizer

Two's Complement: Enables two's complement mode.

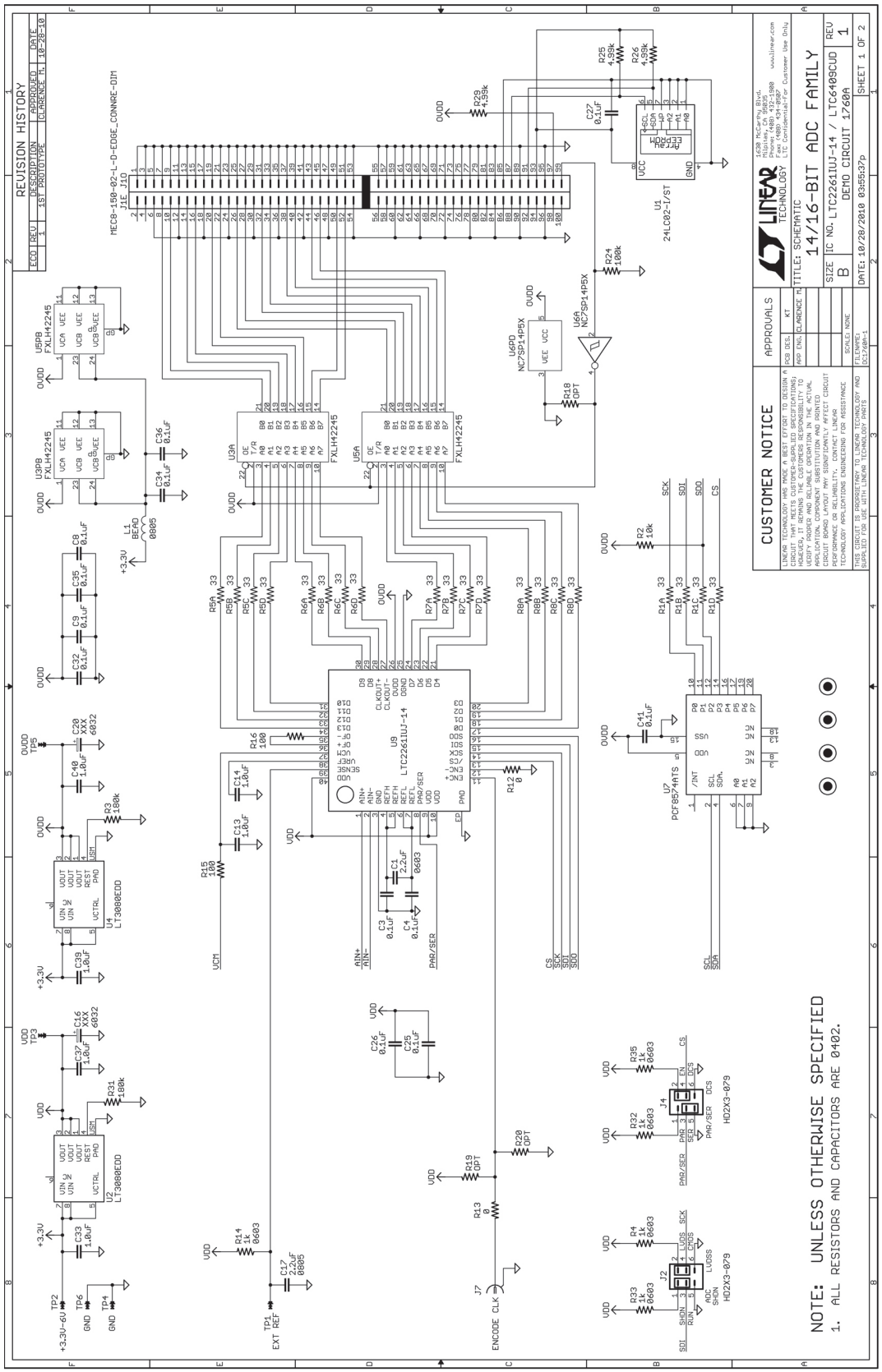
- Off (Default) – Selects offset binary mode
- On – Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1760A demo board.

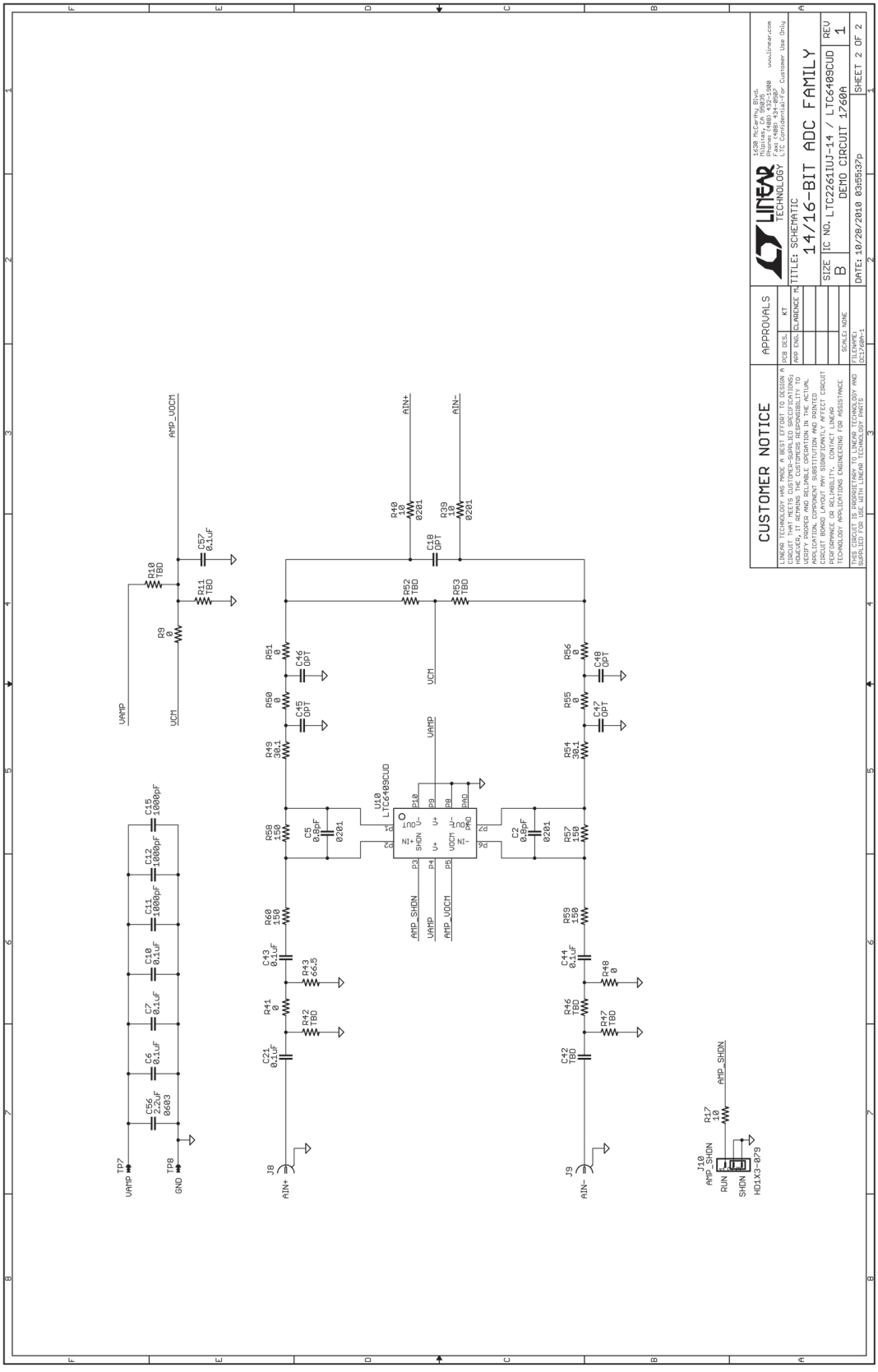
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	2	C1, C56	CAP., 0603 2.2µF 6.3V 20% X5R	AVX, 06036D255MAT2A
2	3	C11, C12, C15	CAP., 0402 1000pF 5% 50V COG	MURATA, GRM1555C1H102JA01
3	6	C13, C14, C33, C37, C39, C40	CAP., 0402 1µF 10V 10% X5R	AVX, 0402ZD105KAT2A
4	2	C16, C20	CAP., Tant., 100µF, 10V, 20% 6032	AVX, TAJW107M010R
5	1	C17	CAP., 0805 2.2µF 10V 20% X5R	AVX, 0805ZD225MAT
6	0	C18, C45, C46, C47, C48	CAP., 0402	OPT
7	2	C2, C5	CAP., 0201 0.8pF 25V ±0.1pF NP0	AVX, 02013A0R8BAT2A
8	19	C3, C4, C6-C10, C21,C25-C27, C32, C34-C36, C41, C43, C44, C57	CAP., 0402 0.1µF 10V 10% X5R	AVX, 0402ZD104KAT
9	0	C42	CAP., 0402	TBD
10	1	J10	HEADER, 3-PIN 0.079 SINGLE ROW	SAMTEC, TMM-103-02-L-S
11	2	J2, J4	HEADER, 2 × 3 PIN 0.079 DOUBLE ROW	SAMTEC, TMM-103-02-L-D
12	3	J7, J8, J9	CONN., SMA 50Ω EDGE-LANCH	CONNEX, 132357 / 142-0701-851
13	1	L1	IND., BEAD, 60Ω Impedance 0805	MURATA, BLM21BB600SN1D
14	5	R1, R5, R6, R7, R8	RES., ARRAY, 33Ω 0402 5%	VISHAY, CRA04S08333R0JTD
15	0	R10, R11, R42, R46, R47, R52, R53	RES., 0402	TBD
16	1	R15	RES., 0402 100Ω 1% 1/16W	VISHAY, CRCW0402100RFKED
17	1	R16	RES., 0201 100Ω 1% 1/20W	VISHAY, CRCW0201100RFNED
18	1	R17	RES., 0402 10Ω 1% 1/16W	VISHAY, CRCW040210R0FKED
19	0	R18, R19, R20	RES., 0402	OPT
20	1	R2	RES., 0402 10k 1% 1/16W	VISHAY, CRCW040210K0FKED
21	1	R24	RES., 0402 100k 1% 1/16W	VISHAY, CRCW0402100KFKED
22	3	R25, R26, R29	RES., 0402 4.99k 1% 1/16W	VISHAY, CRCW04024K99FKED
23	2	R3, R31	RES., 0402 180k 1% 1/16W 5%?	VISHAY, CRCW0402180KFKED
24	2	R39, R40	RES., 0201 10Ω 5% 1/20W	VISHAY, CRCW020110R0JNED
25	5	R4, R14, R32, R33, R35	REA., 0603 1k 5% 1/16W	VISHAY, CRCW06031K00FKEA
26	1	R43	RES., 0402 66.5Ω 1% 1/16W	VISHAY, CRCW040266R5FKED
27	2	R49, R54	RES., 0402 30.1Ω 1% 1/16W	VISHAY, CRCW040230R1FKED
28	4	R57, R58, R59, R60	RES., 0402 150Ω 5% 1/16W	VISHAY, CRCW0402150RJNED
29	9	R9, R12, R13, R41, R48, R50, R51, R55, R56	RES., 0402 0Ω JUMPER	VISHAY, CRCW04020000Z0ED
30	8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	TP, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
31	1	U1	I.C., Serial EEPROM TSSOP-8	MICROCHIP, 24LC025-I/ST
32	1	U10	IC, LT6409 QFN-3MM × 2MM	LINEAR, LTC6409CUD#PBF
33	2	U2, U4	IC, LT3080EDD	LINEAR, LT3080EDD#PBF
34	2	U3, U5	IC, FXLH42245 DFN-8X4	FAIRCHILD, FXLH42245MPX
35	1	U6	IC, NC7SP17P5X SC70-5	FAIRCHILD, NC7SP17P5X
36	1	U7	IC, PCF8574 SSOP20	PHILLIPS, PCF8574TS
37	1	U9	IC, LTC2262IUJ, TQFN-6 × 6-40PIN	LINEAR, LTC2262IUJ-14#PBF
38		SHUNTS		
39	4	MTG1, MTG2, MTG3, MTG4	STAND-OFF, NYLON (SNAP ON), 0.25" TALL	KEYSTONE, 8831(SNAP ON)
40	2	STENCILS FOR BOTH SIDES		STENCIL DC1760A-1

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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