

LT6350CMS8

Low Noise Single-Ended to Differential Amplifier SAR ADC Driver

DESCRIPTION

Demonstration Circuit 1538A supports the LT6350, a Low Noise Single Ended to Differential Amplifier / SAR ADC Driver. The LT6350 contains an un-dedicated open-loop “Opamp1”, and a dedicated inverting “Opamp2” in a gain of -1. Opamp1 has Rail to Rail inputs and output. Opamp2 has a Rail to Rail output. See Figure 1.

Design files for this circuit board are available. Call the LTC factory.

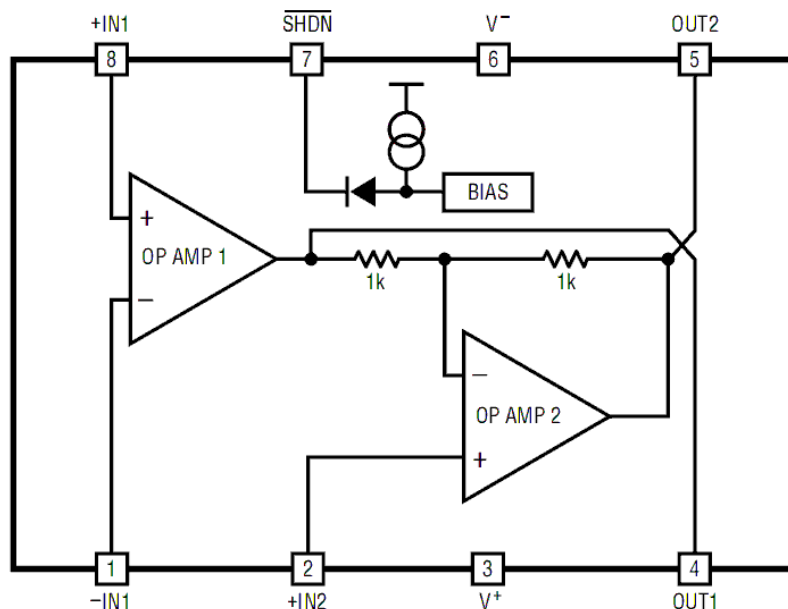
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PERFORMANCE SUMMARY

Specifications are typical at $T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$

SYMBOL	PARAMETER	CONDITIONS, COMMENTS	TYP	UNITS
V_S	Supply Voltage Range	Single Supply	2.7V to 12V	V
		Split Supply	$\pm 1.35\text{V}$ to $\pm 6\text{V}$	V
V_{cm}	Input Voltage Range	Op Amp 1	Rail to Rail	V
		Op Amp 2	$V_{S-} + 1.5\text{V}$ to $V_{S+} - 0.1\text{V}$	V
BW	-3dB Bandwidth	Small signal, differential output	33	MHz
V_{out}	Output Voltage Swing	Each output, to either rail, no load	55	mV
I_{CC}	Supply Current	$V_S = \pm 5\text{V}$	4.8	mA

Figure 1. LT6350 Block Diagram . Opamp1 is an undedicated low noise opamp. Opamp2 is a dedicated inverter.



OPERATING PRINCIPLES

Conversion of single ended signals to differential is a basic function. It may be desired for improved transmission characteristics over twisted pair, or for driving SAR ADCs which prefer differential inputs. The LT6350 makes the single-ended to conversion easy by providing

an already connected internal inverter, Opamp2. In the simplest configuration, with Opamp1 in a gain of 1, the conversion to differential causes an effective gain of 2 overall.

QUICK START PROCEDURE

Demonstration circuit 1538 is shipped with the jumpers set for Single Supply, DC coupled operation, with Opamp1 configured in a gain of 1 (OUT1 shorted to $-IN1$). As the intended application is for single ended inputs, only one input BNC connector is installed (J1) and this is the excitation path for Opamp1's non-inverting input $+IN1$. To support Opamp1 in inverting or other applications, a footprint for another BNC was included (J3) for user installation.

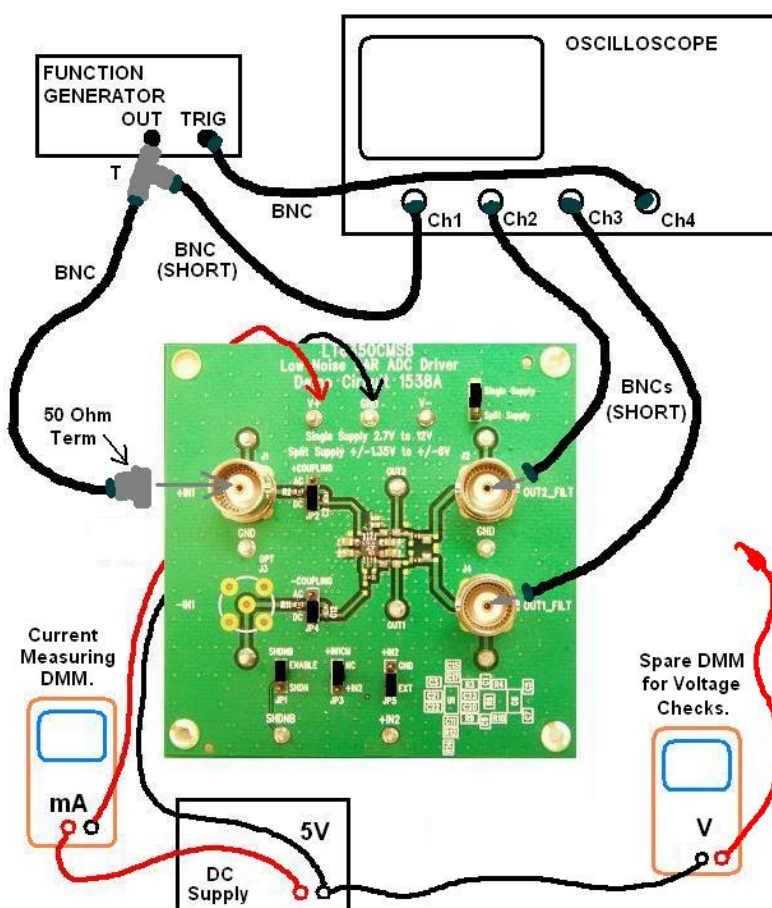


Figure 2. Proper Connections for Single Supply Operation (DMMs optional). The function generator should be set up to operate around a positive 2V DC offset. For split supply operation, set JP6 to "Split Supply" and connect a negative supply to the V- turret.

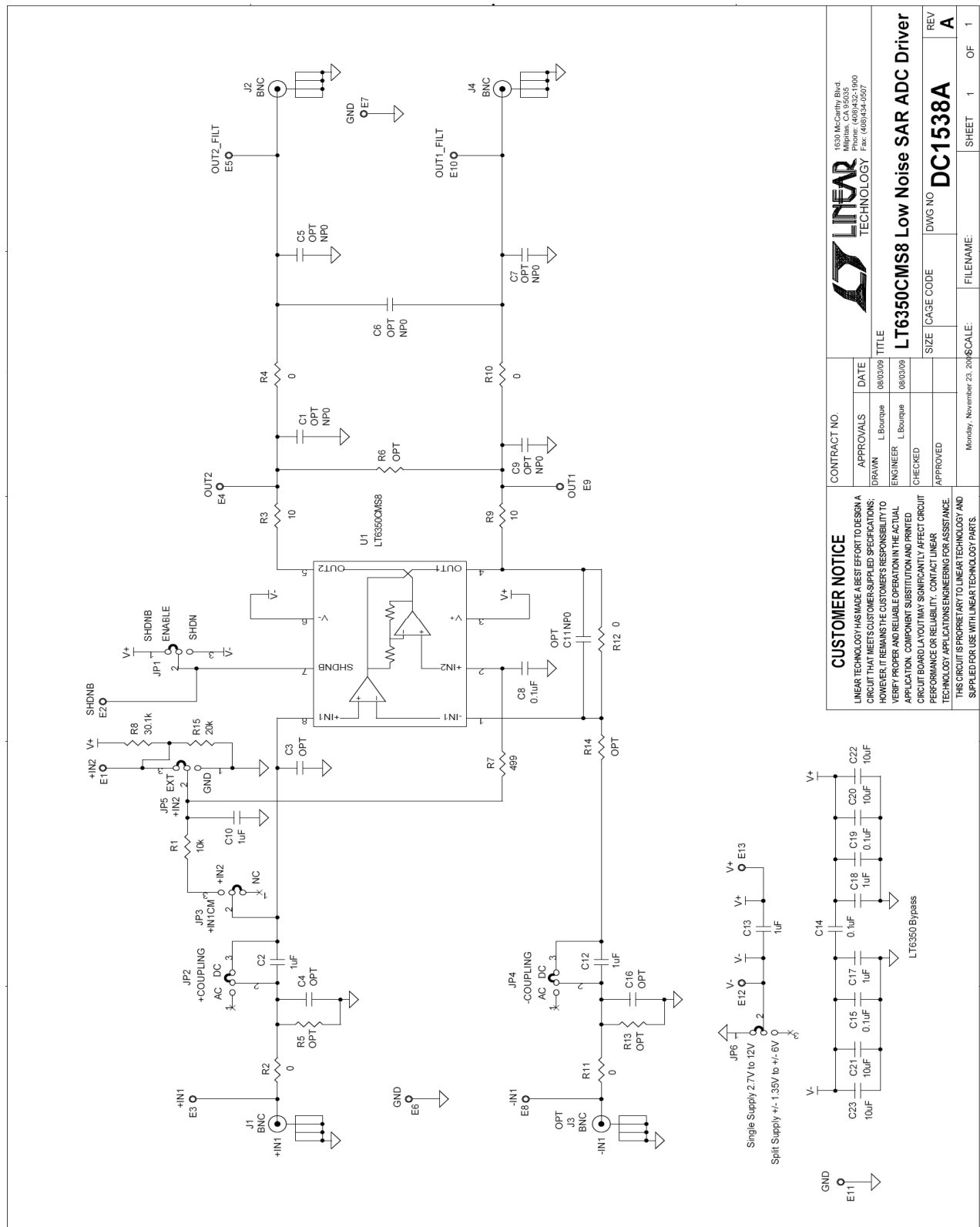


Figure 3. Circuit Schematic

Item	Qty	Ref - Des	Part Description	Manufacturer, Part #
REQUIRED CIRCUIT COMPONENTS:				
1	6	C2,C10,C12,C13,C17,C18	CAP., X7R, 1uF, 16V, 10% 0603	AVX, 0603YC105KAT2A
2	4	C8,C14,C15,C19	CAP., X7R, 0.1uF, 25V, 10% 0603	AVX, 06033C104KAT2A
3	4	C20,C21,C22,C23	CAP., X5R, 10uF, 16V, 10% 0805	MURATA, GRM21BR61C106KE15L
4	1	R1	RES., CHIP, 10K, 1/10W, 1% 0603	VISHAY, CRCW060310K0FKEA
5	5	R2,R4,R10,R11,R12	RES., CHIP, 0, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
6	2	R3,R9	RES., CHIP, 10, 1/10W, 1% 0603	VISHAY, CRCW060310R0FKEA
7	1	R7	RES., CHIP, 499, 1/10W, 1% 0603	VISHAY, CRCW0603499RFKEA
8	1	R8	RES., CHIP, 30.1K, 1/10W, 1% 0603	VISHAY, CRCW060330K1FKEA
9	1	R15	RES., CHIP, 20K, 1/10W, 1% 0603	VISHAY, CRCW060320K0FKEA
10	1	U1	Low Noise SAR ADC Driver	Linear Tech., LT6350CMS8#TRPBF
ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS:				
1	5	C1,C5,C7,C9,C11 (opt.)	CAP., 0603, NP0	
2	1	C3 (opt.)	CAP., 0603	
3	3	C4,C6,C16 (opt.)	CAP., 1206, NP0	
4	2	R5,R13 (opt.)	RES., 1206	
5	2	R6,R14 (opt.)	RES., 0603	
HARDWARE				
1	13	E1-E13	TESTPOINT, TURRET, .065" pbf	MILL-MAX, 2308-2-00-80-00-00-07-0
2	4	J1,J2,J3,J4	CONN, BNC, 5 PINS	CONNEX, 112404
3	6	JP1,JP2,JP3,JP4,JP5,JP6	HEADER, 3PINS, 2mm	SAMTEC, TMM-103-02-L-S
4	6	JP1,JP2,JP3,JP4,JP5,JP6	SHUNT, 2MM CENTER	SAMTEC, 2SN-BK-G
5	4	MH1,MH2,MH3,MH4	STAND-OFF, NYLON 0.25"	KEYSTONE, 8831(SNAP ON)

Figure 4. Bill of Materials

Mouser Electronics

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[DC1538A](#)