LTM4601AEV
20V, 12A DC/DC µModule® Regulator

DESCRIPTION

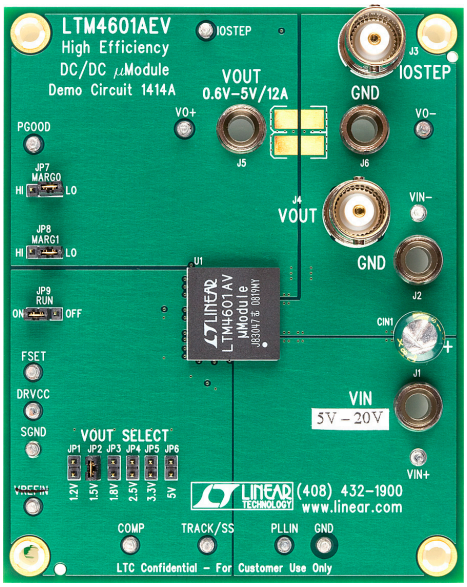
Demonstration circuit 1414 features the LTM®4601AEV, a high efficiency, high density switch mode step-down power module. The DC1414A accepts an input voltage from 5V to 20V to deliver a jumper selectable output voltage from 1.2V to 5V at up to 12A. As shown in the data sheet, derating is necessary for certain V_{IN}, V_{OUT}, and thermal conditions. The LTM4601A allows the user to program output ramp-up and ramp-down through the TRACK/SS pin. The output can be set to coincidentally or ratiometrically track with another voltage rail. This board also supports demonstration of the output voltage margining function by ±5% from nominal which is determined by the state of the MARGN0 and MARGN1 pins. Refer to the LTM4601A data-sheet for additional information.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

PARAMETER	CONDITION	VALUE
Input Voltage Range		5V to 20V
Output Voltage V_{OUT}	Jumper Selectable (Open for 0.6V)	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V
Maximum Continuous Output Current	Derating is Necessary for Certain V_{IN}, V_{OUT}, and Thermal Conditions	$12A_{DC}$
Default Operating Frequency		850kHz
External Synchronous Clock Frequency Range	Please Refer to Data Sheet for Minimum t_{ON} and t_{OFF} Requirement.	600kHz to 1000kHz
Efficiency	V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 12A	89.5%, See Figure 2

BOARD PHOTO



QUICK START PROCEDURE

Demonstration circuit 1414 is easy to set up to evaluate the performance of the LTM4601AEV. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical $1.5V_{OUT}$ application:

V_{OUT} SELECT	RUN	MARG0	MARG1
1.5V	ON	LO	LO

2. With the power off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply between 5V to 20V.
3. Turn on the power at the input. The output voltage should be 1.5V ± 1%.
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters. Output ripple should be measured at J4 with a BNC cable.
5. (Optional) To review load transient performance, apply an adjustable pulse signal between IOSTEP (E3) and GND pins. Pulse amplitude sets the current step. The pulse signal should have very small duty cycle (<15%) to limit the thermal stress on the transient load circuit. The output transient current can be monitored at BNC connector J3 (10mV/A).
6. (Optional) To implement output voltage margining, place jumpers MARG0 and MARG1 in the configuration shown according to the table below. The output voltage measured at J4 will respond accordingly.

MARG1	MARG0	ΔV_{OUT}
LO	LO	0
LO	HI	5%
HI	LO	–5%
HI	HI	0

QUICK START PROCEDURE

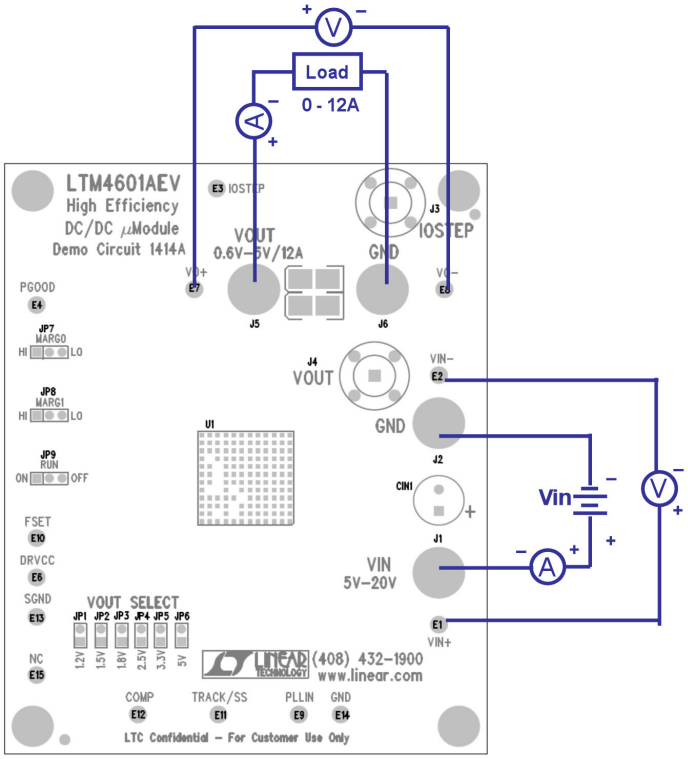


Figure 1. Test Setup of DC1414A

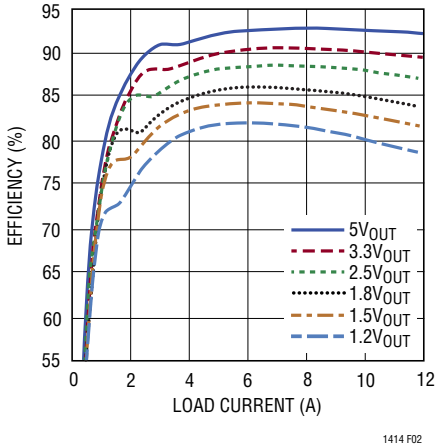
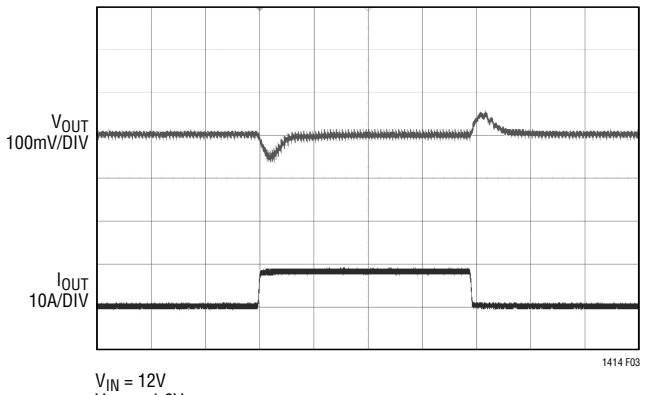


Figure 2. Measuring Supply Efficiency with Different V_{OUT} (V_{IN} = 12V)



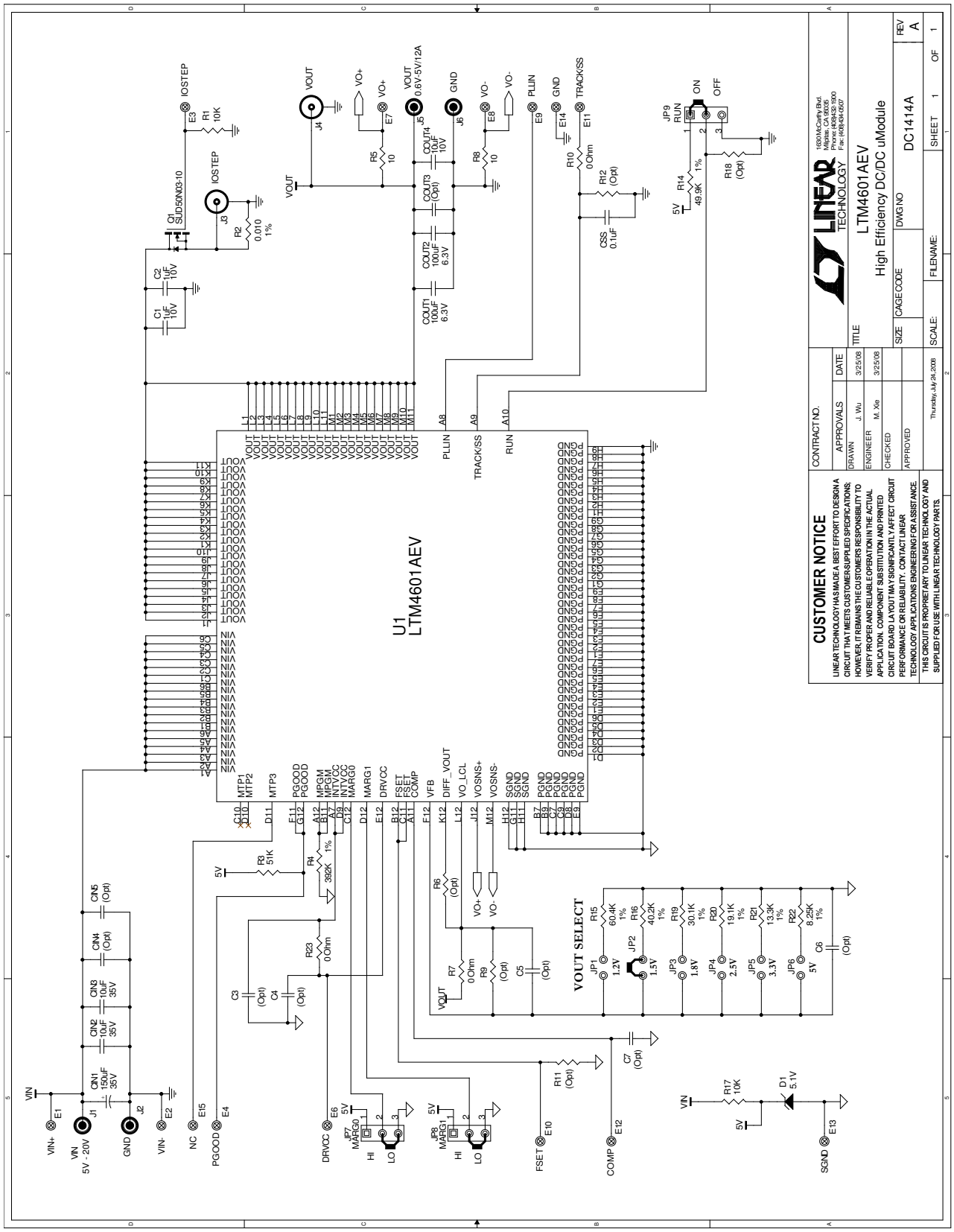
V_{IN} = 12V
V_{OUT} = 1.2V
2A TO 10A LOAD STEP
C_{OUT}: 2 × 100µF/3.6V/X5R/1812 CERAMIC 1 × 22µF/10V/X5R/1206 CERAMIC

Figure 3. Measured Load Transient Response

PARTS LIST

ITEM	QUANTITY	REFERENCE-DESCRIPTION	DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	Cap, Alum 150µF 35V 20%	Sanyo 35ME150WXV+TS
2	2	CIN2, CIN3	Cap, X7R 10µF 35V 20%	Taiyo Yuden GMK316BJ106ML-T
3	2	COUT1, COUT2	Cap, X5R 100µF 6.3V 20%, 1210/1812	TDK C4532X5R0J107M
4	1	COUT4	Cap, X5R 10µF 10V 10%	Taiyo Yuden LMK316BJ106KL-T
5	1	CSS	Cap, X7R 0.1µF 16V 20%	AVX 0603YC104MAT2A
6	1	D1	Zener Diode, 5.1V	On Semiconductor MMBZ5231B
7	1	R17	Res, Chip 10k 0.1W 5%	Vishay CRCW060310K0JNEA
8	1	R3	Res, Chip 51k 0.1W 5%	Vishay CRCW060351K0JNEA
9	1	R4	Res, Chip 392k 0.1W 1%	Vishay CRCW0603392KFKEA
10	1	R14	Res, Chip 49.9k 0.1W 1%	Vishay CRCW060349K9FKEA
11	1	R16	Res, Chip 40.2k 0.1W 1%	Vishay CRCW060340K2FKEA
12	1	U1	IC, Voltage Regulator	Linear Technology LTM4601AEV
Additional Demo Board Circuit Components				
1	0	CIN4, CIN5 (OPT)	Cap, 1206 TBD	
2	0	COUT3 (OPT)	Cap, 1210 TBD	
3	2	C1, C2	Cap, X5R 1µF 10V 10%	Taiyo Yuden LMK107BJ105KA
4	0	C3, C4, C5, C6, C7 (OPT)	Cap, 0603 TBD	
5	1	Q1	MOSFET, N-Channel 30V	Vishay SUD50N03-09P-E3
6	1	R1	Res, Chip 10k 0.1W 5%	Vishay CRCW060310K0JNEA
7	1	R2	Res, LRF, 0.010, 2W, 1%, 2512	IRC LRF2512LF-01-R010-F
8	2	R8, R5	Res, Chip 10 0.1W 5%	Vishay CRCW060310R0JNEA
9	0	R6, R9, R11, R12, R18 (OPT)	Res, 0603 TBD	
10	3	R7, R10, R23	Res/Jumper, Chip 0Ω 1/16W 1 AMP	Vishay CRCW06030000Z0EA
11	1	R15	Res, Chip 60.4k 0.1W 1%	Vishay CRCW060360K4FKEA
12	1	R19	Res, Chip 30.1k 0.1W 1%	Vishay CRCW060330K1FKEA
13	1	R20	Res, Chip 19.1k 0.1W 1%	Vishay CRCW060319K1FKEA
14	1	R21	Res, Chip 13.3k 0.1W 1%	Vishay CRCW060313K3FKEA
15	1	R22	Res, Chip 8.25k 0.1W 1%	Vishay CRCW06038K25FKEA
Hardware for Demo Board Only				
1	14	E1 to E4, E6 to E13, E14, E15	Turret, Testpoint	Mill Max 2308-02-00-80-00-00-07-0
2	6	JP1, JP2, JP3, JP4, JP5, JP6	2 Pin 0.079 Single Row Header	Samtec TMM102-02-L-S
3	3	JP7, JP8, JP9	3 Pin 0.079 Single Row Header	Samtec TMM103-02-L-S
4	4	XJP2, XJP7, XJP8, XJP9	Shunt, 0.079 Center	Samtec 2SN-BK-G
5	4	J1, J2, J5, J6	Connector, Banana Jack	Keystone 575-4
6	2	J3, J4	BNC Connector	Connex 112404
7	4		Stand Off, Nylon, 0.5” Tall	Keystone 8833 (Snap On)

SCHEMATIC DIAGRAM



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