QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1278

6-CHANNEL, 14-BIT, 1.5MSPS SIMULTANEOUS SAMPLING ADC

LTC2351-14

DESCRIPTION

Demonstration circuit 1278 features the LTC2351-14 6-channel, 14-Bit, simultaneous sampling ADC. Total throughput is 1.5MSPS; 250KSPS per channel, with a typical channel-to-channel aperture skew of 200ps. The board is designed to be used with the DC890B Fast DAACS data collection board to show the AC performance of the LTC2351-14. Alternatively, the board can be directly connected to an application to evaluate the ADC's performance.

Design files for this circuit board are available. Call the LTC factory.

QUICK START PROCEDURE

BASIC CONNECTIONS

Connect DC1278 to a DC890B USB High Speed Data Collection Board using connector J2. Connect DC890B to a host PC with a standard USB A/B cable. Apply 5-7V DC to the VIN and GND terminals. Apply a 25MHz 3.3Vp-p sine wave or square wave to connector J3. Note that J3 has a 50 ohm termination resistor to ground. CH0-CH5 are provided through connector J1 (See schematic for details.). Run the QuickEval II (Pscope.exe) evaluation software supplied with DC890 or download it from www.linear.com/software.

Figure 1. CONNECTION DIAGRAM

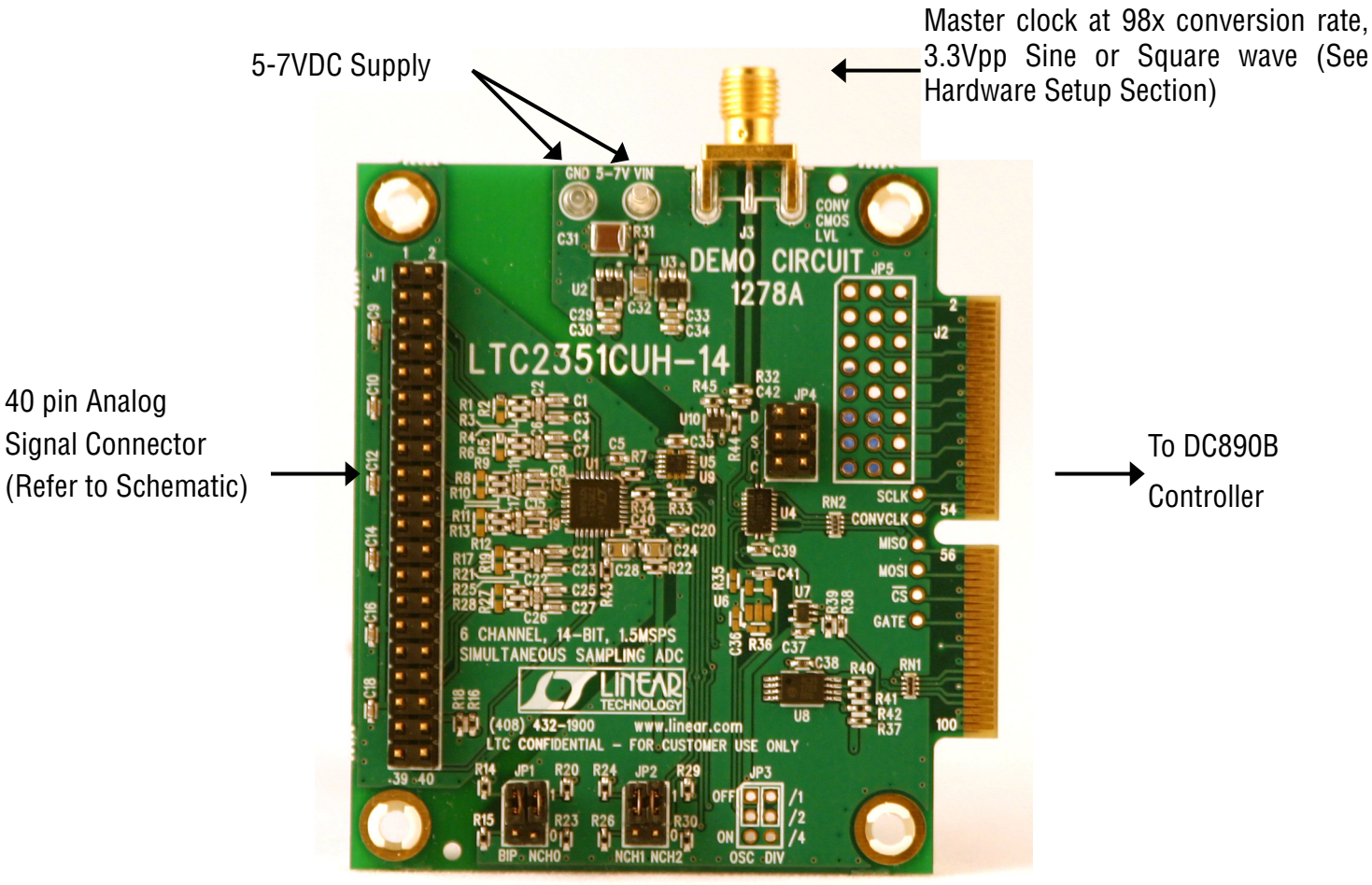


Figure 2. SOFTWARE SCREENSHOT

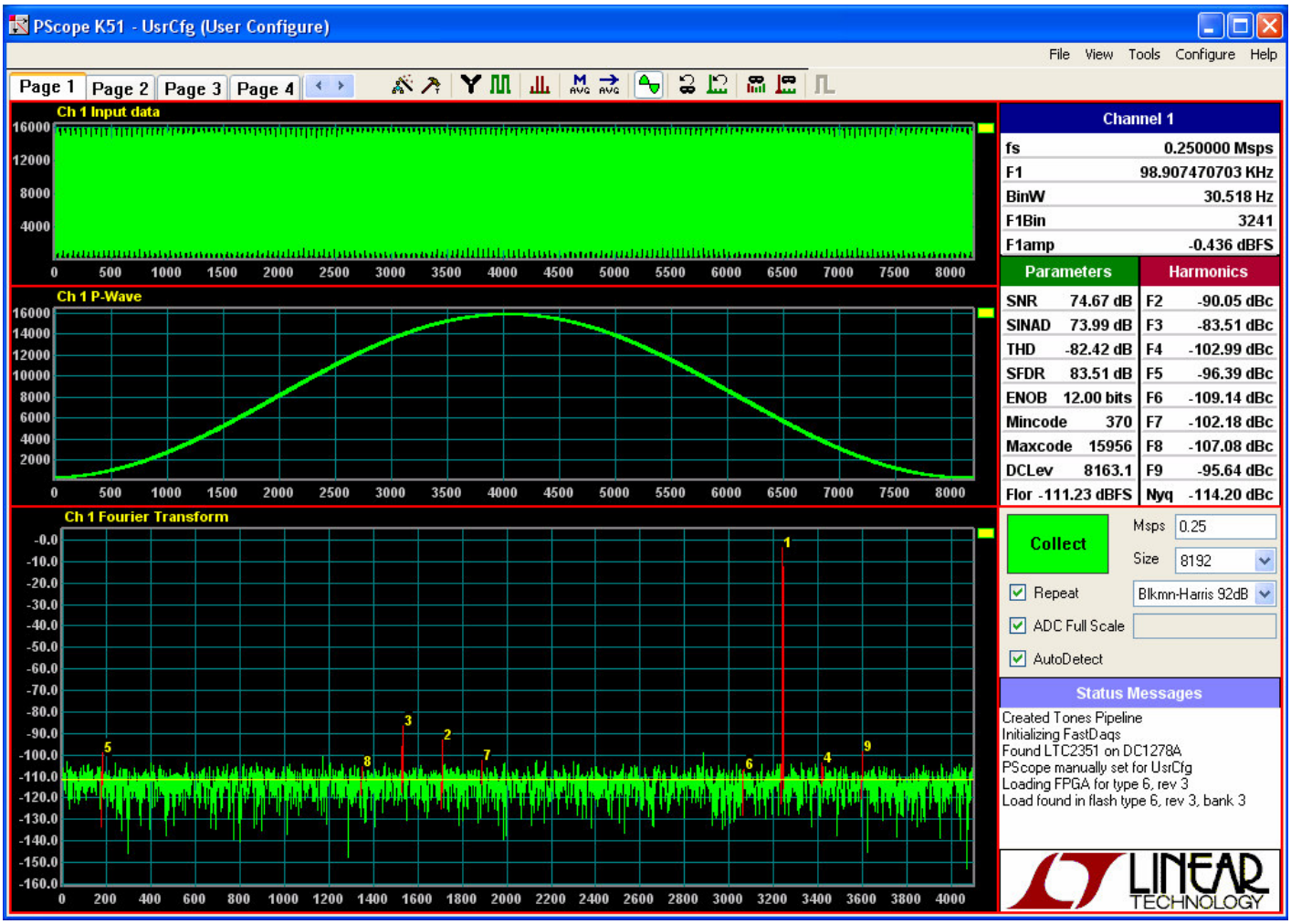
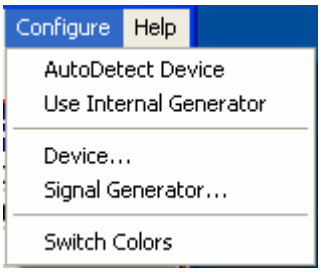
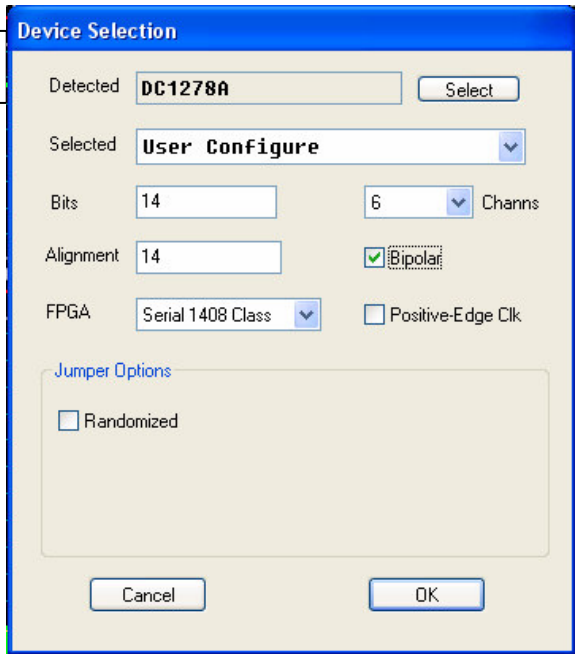


Figure 3. CONFIGURE MENUS





SOFTWARE CONFIGURATION

CONFIGURE DEVICE

The Pscope software should automatically configure itself after detecting the demo board. To change from Bipolar to Unipolar mode it will be necessary to manually configure the software. In the CONFIGURE menu (See Figure 3) select Device, which will bring up another window. In this window, select User Configure and adjust the other settings as follows:

Bits: 14

Alignment: 14

Bipolar: Checked if BIP jumper is set high, Un-Checked if BIP jumper is set to low. (Default is checked)

Channels: 6

Positive Edge Clk: UN-Checked

FPGA: Serial 1408 Class.

CONFIGURE SOFTWARE SCREEN

The software interface is highly configurable and displays any combination of time domain data, frequency domain data, primitive wave and performance parameters (SNR, THD, SINAD, etc.). The screen can be broken into multiple panes as shown in Figure 2. Complete documentation on configuring PSCOPE can be found in the help file.

Click the COLLECT button to begin acquiring data.

Complete software documentation is available from the Help menu item, as features may be added periodically.

HARDWARE SET-UP

JUMPERS

JP1, JP2 - Select number of channels to convert and Unipolar / Bipolar selection. NCH2, NCH1, NCH0 are set to 111 which selects all six channels. These switches should be left in this position when running Pscope software. UNI/BIP selection applies to all channels. Refer to Figure 4.

JP3 – Enable Oscillator and Oscillator Division. Presently not used. This may be used in the future as serial clock, to allow a convert signal at 1X the conversion rate.

JP4 – Digital Interface Header. Provides direct connection to the LTC2351-14 CONV, SDO, and SCK pins. This can be used to either monitor signals with a logic analyzer or to drive the LTC2351-14 directly from the customer's test equipment or prototype circuitry. DC890B should be disconnected before driving the LTC2351-14 externally with JP4. Note that R34 should be removed if the CONV signal is being driven externally.

JP5 – Currently not used

SIGNAL CONNECTIONS

J1 – 40 pin connector with CH0-CH5 differential inputs, multiple grounds, a mid-supply bias voltage and Vref. Refer to schematic for pin out. The mid-supply bias voltage can be used to bias the minus ADC inputs for bipolar conversions.

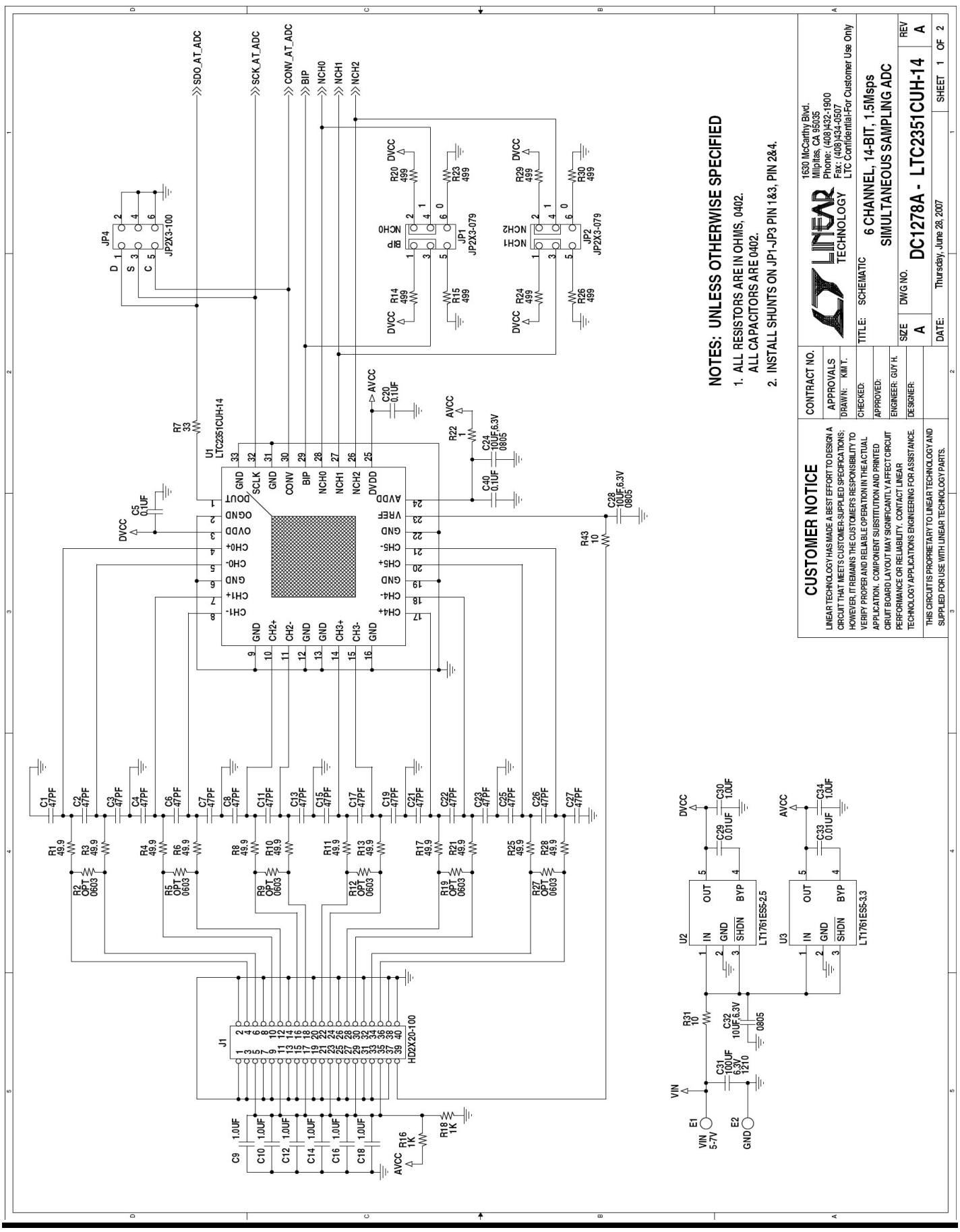
J2 – Data connections to DC890B collection board.

J3 – Conversion Clock Input. This input has a 50 ohm termination resistor, and is intended to be driven by a 3.3Vpp sine or square wave. This clock is divided by 98 in the DC890B collection board to control the serial interface and convert pulse. To run the LTC2351-14 at maximum conversion rate, apply a 25MHz signal to this input.

GROUNDING AND POWER CONNECTION

Connect a 5V to 7V power supply to the Vin and GND turret posts. For optimum performance, this supply should be floating with respect to any signal generators connected to the analog inputs.

Figure 4 – JP1, JP2 CONFIGURATION


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0402.
ALL CAPACITORS ARE 0402.
2. INSTALL SHUNTS ON JP1-JP3 PIN 1&3, PIN 2&4.
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
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APPROVED:
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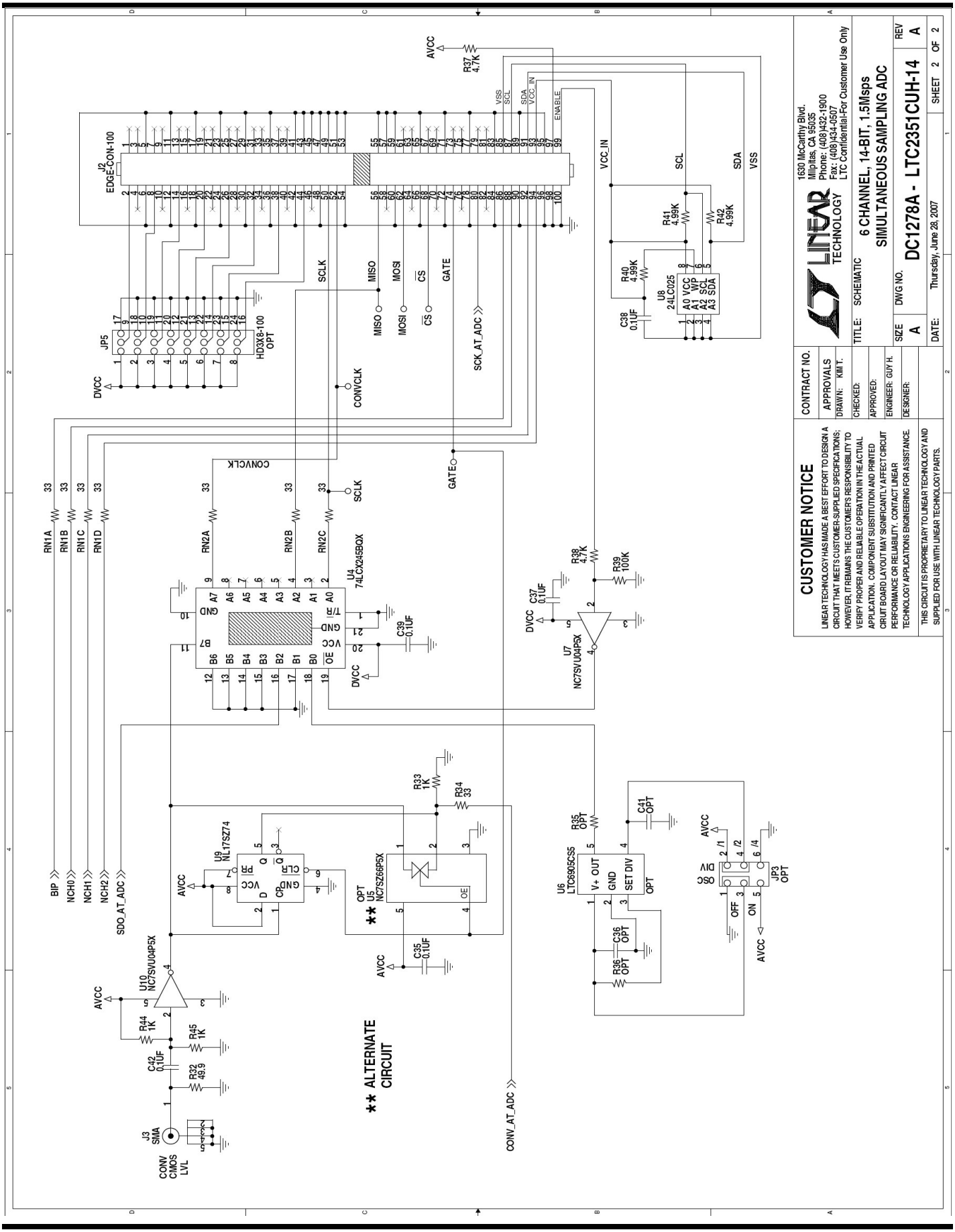
LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
6 CHANNEL, 14-BIT, 1.5Msps
SIMULTANEOUS SAMPLING ADC
SIZE A
DWG NO. DC1278A - LTC2351CUH-14
REV A
DATE: Thursday, June 28, 2007
SHEET 1 OF 2
U1 LTC2351CUH-14
J1 HD2X20-100
JP1 JP2X3-079
JP2 JP2X3-079
JP4 JP2X3-100
U2 LT1761ES5-2.5
U3 LT1761ES5-3.3
SDO_AT_ADC
SCK_AT_ADC
CONV_AT_ADC
BIP
NCH0
NCH1
NCH2
AVCC
DVCC
VIN


AVCC
R37 4.7K
J2 EDGE-CON-100
VSS
SCL
SDA
VCC_IN
ENABLE
VCC_IN
SCL
SDA
VSS
R41 4.99K
R42 4.99K
R40 4.99K
U8 24LC025
A0 VCC
A1 WP
A2 SCL
A3 SDA
C38 0.1UF
JP5
HD3X8-100 OPT
DVCC
CONVCLK
SCLK
MISO
MOSI
CS
GATE
SCK_AT_ADC
RN1A 33
RN1B 33
RN1C 33
RN1D 33
RN2A 33
RN2B 33
RN2C 33
U4 74LCX245BQX
C39 0.1UF
C37 0.1UF
R38 4.7K
R39 100K
U7 NC7SV U04P5X
R33 1K
R34 33
U9 NL17SZ74
U5 NC7SZ66P5X
OPT
C35 0.1UF
R35 OPT
C41 OPT
U6 LTC6905CS5
V+ OUT
GND
SET DIV
C36 OPT
R36 OPT
OSC DIV
JP3 OPT
OFF
ON
BIP
NCH0
NCH1
NCH2
SDO_AT_ADC
CONV_AT_ADC
U10 NC7SV U04P5X
R44 1K
R45 1K
C42 0.1UF
R32 49.9
J3 SMA
CONV CMOS LVL
** ALTERNATE CIRCUIT
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SHEET 2 OF 2

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