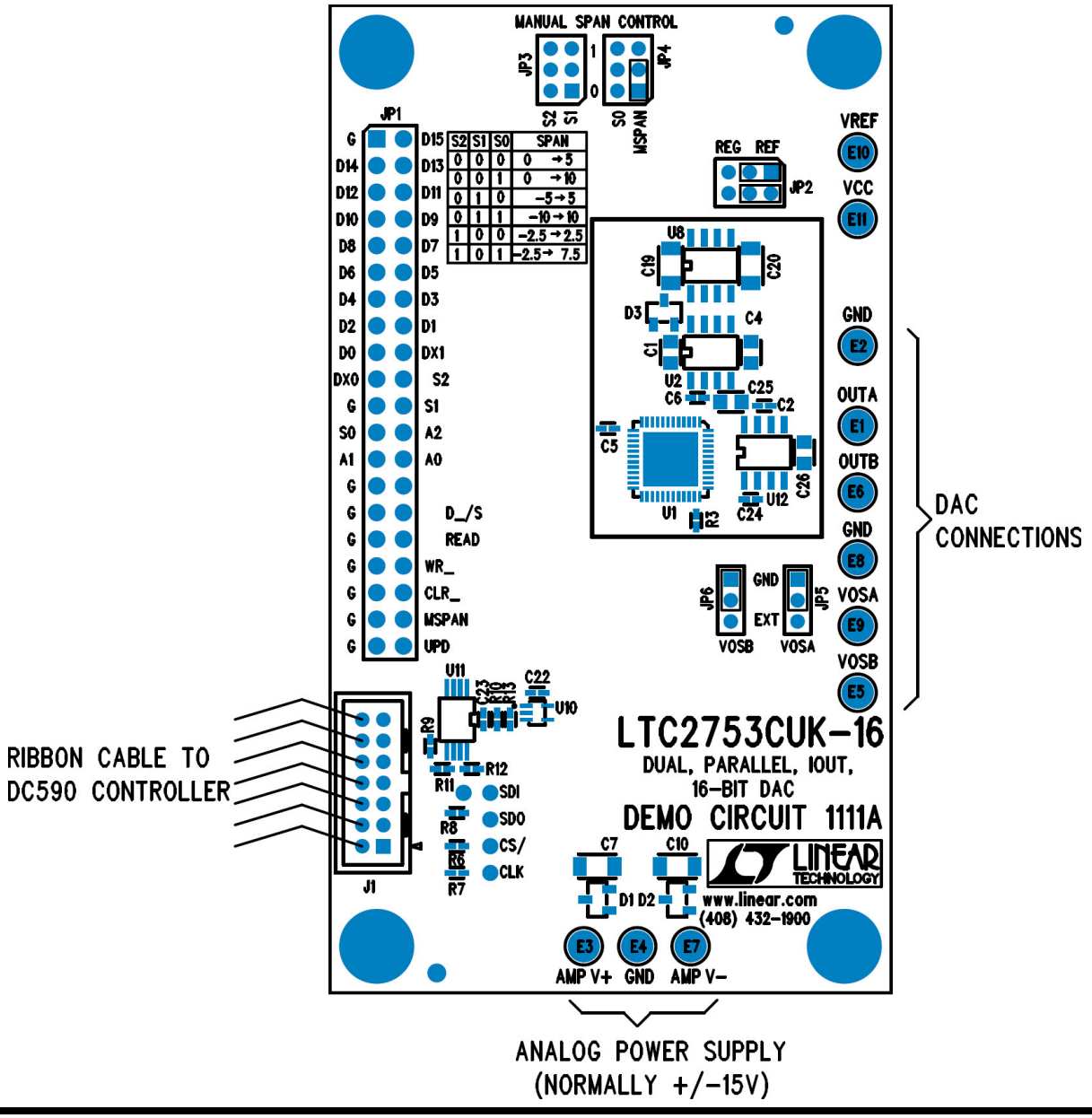
DESCRIPTION

Demonstration circuit 1111 features the LTC2753 Dual 16-Bit SoftSpan Iout DAC. This device features six output ranges, 0 to 5V, 0 to 10V, +/- 5V, +/- 10V, +/- 2.5V, and -2.5V to + 7.5V. The DAC has an offset adjust input pin and a compensation pin to allow optimization of transient response.

Design files for this circuit board are available. Call the LTC factory.

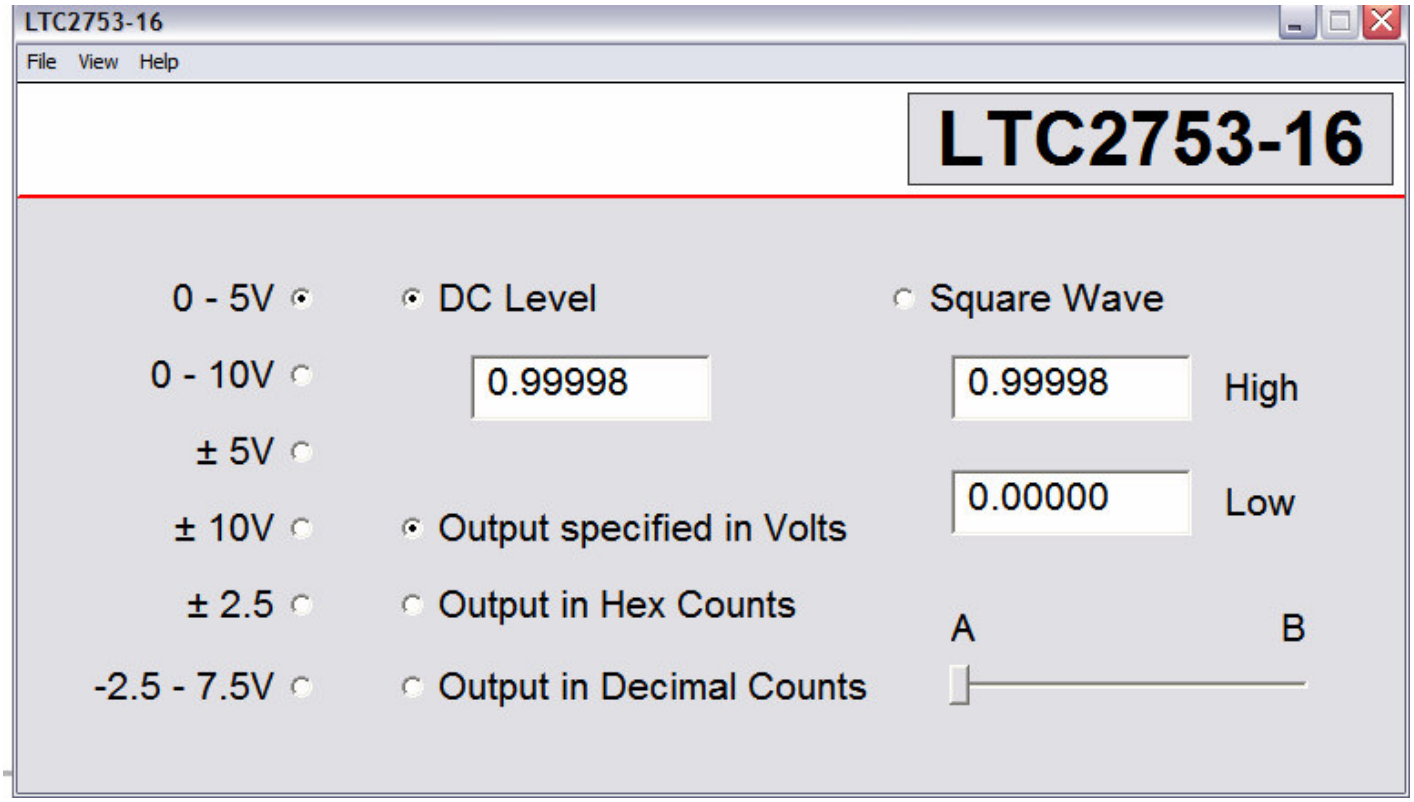
Figure 1. Proper Measurement Equipment Setup



QUICK START PROCEDURE

Connect a clean +/-15V power supply to the turret posts at the bottom edge of the DC1111 board. Connect J1 to a DC590 USB serial controller using the supplied 14 conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or download it from the website, www.linear.com/software. The correct control panel will be loaded automatically. The software automatically sets the LTC2753 outputs according to the entries in the control panel. A square wave option is available to test settling time. MSPAN jumper should be low if software span control is desired.

Additional software documentation may be available from the Help menu item, as features may be added periodically.



USING THE PARALLEL CONNECTOR

PROTOCOL

The DC1111 can also be used without the DC590 system. If a DC590 demo board is not connected the shift registers on the DC1111 are disabled, allowing the user to clock in data through the parallel connector (JP1).

The data input register is loaded directly from the 16-bit microprocessor bus (D0-D15 on the parallel connector) by holding the _D/S pin low and then pulsing the _WR pin low. The second register (DAC register) is loaded by pulsing the UPD pin high, which copies the data held in the input register into the DAC register. Note that updates always include both data and span; but the DAC register values will not change unless the input register values have been changed by writing.

Loading the span input register is accomplished in a similar manner, by holding the _D/S pin high and then bringing the _WR pin low. The span and data register structures are the same except for the number of parallel bits the span registers have three bits, while the data registers have 12, 14, or 16 bits.

Please see the LTC2753 datasheet for in depth timing diagrams and more information about the communication protocol.

PARALLEL PIN DESCRIPTIONS

A0-A1: DAC address bits. Determine which DAC(s) respond to parallel commands. A0 = A1 = 0 will address, DACA. A0 = 1, A1 = 0 will address DACB. A0 = A1 = 1 will address both DAC's on a write and DACA on a read.

A2: Unused.

D0-D15: DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D15 is the MSB. D0 is the LSB.

S0-S2: Span I/O Bit 0. Pins S0, S1 and S2 are used to program and to read back the output range of the DAC.

_D/S: Data/Span Select. This pin is used to select activation of the data or span I/O pins (D0 to D15 or S0 to S2, respectively), along with their respective dedicated registers, for write or read operations. Update operations ignore _D/S, since all updates affect both data and span registers. For single-span operation, tie _D/S to GND.

READ: Read Pin. When READ is asserted high, the data I/O pins (D0-D15) or span I/O pins (S0-S2) output the contents of the selected register (see Table 1). For single-span operation, readback of the span I/O pins is disabled.

UPD: Update and Buffer Select Pin. When READ is held low and UPD is asserted high, the contents of the input registers (both data and span) are copied into their respective DAC registers. The output of the DAC is updated, reflecting the new DAC register values. When READ is held high, the update function is disabled and the UPD pin functions as a buffer selector—logic low to select the input register, high for the DAC register.

_WR: Active Low Write Pin. A Write operation copies the data present on the data or span I/O pins (D0 - D15 or S0 - S2, respectively) into the input register. When READ is high, the Write function is disabled.

MSPAN: Manual Span Control Pin. MSPAN is used to configure the LTC2753 for operation in a single, fixed output range.

G: Ground Pin. (Note: if an IDE cable is used, pin 21 is often keyed on the connector and may be trimmed)

HARDWARE SET-UP

JUMPERS

MSPAN – Manual Span Control Pin. MSPAN is used to configure the LTC2753 for operation in a single, fixed output range. If MSPAN is high it will be configured for single span use. If MSPAN is low it will be set through the Quick Eval Software. Default position is 0 (low).

S0, S1, S2 – Used to set the fixed output range if MSPAN is high. Default is all jumpers removed, allowing software span control.

S2	S1	S0	Span
0	0	0	0-5 V
0	0	1	0-10V
0	1	0	+/- 5V
0	1	1	+/- 10V
1	0	0	+/- 2.5 V
1	0	1	-2.5V to 7.5V

VREF – Voltage reference selection for the DAC, either 5V for the onboard LT1236 reference or EXT if an external reference source is connected to the VREF turret post.

VOSA, VOSB – offset adjustment selection for DACA and DACB. If no offset adjustment is required, select GND. Selecting EXT connects the offset pin to the turret allowing external adjustment of offset.

VCC – Select source for 5V Vcc supply. Set to 5V for supply by onboard LT1236 reference (recommended). Set to REG to be supplied by regulated supply from DC590 Controller and remove the jumper to supply externally.

ANALOG CONNECTIONS (TURRET POSTS)

OUTA, OUTB – DAC voltage outputs.

VREF – DAC Reference voltage. If the onboard LT1236 references are selected, the voltage may be measured at these points. If a remote reference is selected, then an external reference must be applied to these points.

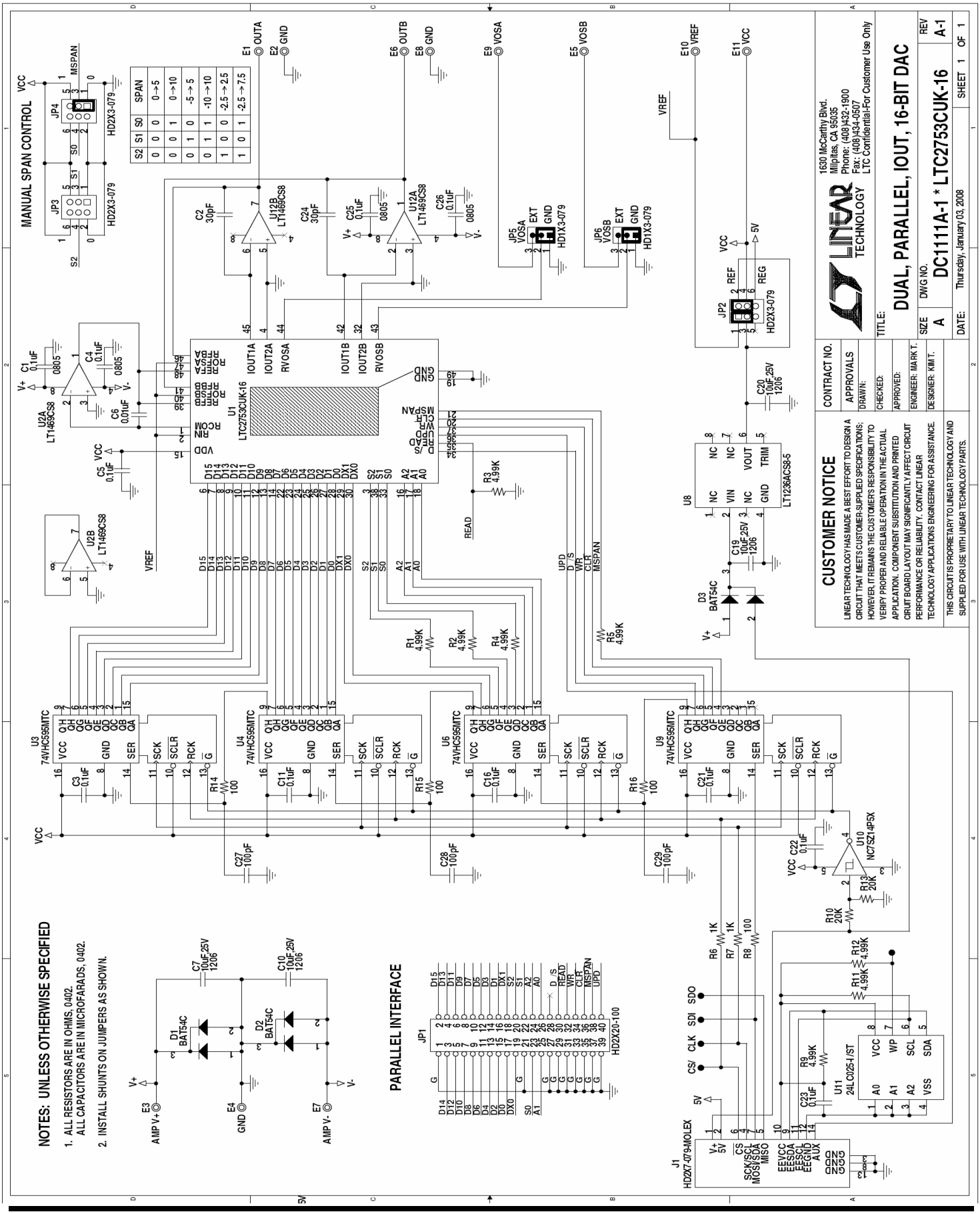
VOSA, VOSB – DAC Offset Adjust inputs, use only if VOSA/VOSB jumpers are set to EXT. Nominal input range is ±5V.

POWER AND GROUND CONNECTIONS

Analog Power – The +15V, -15V, and GND turret posts are the analog supplies for the internal DAC amplifiers. These should be connected to a well regulated, low noise power supply.

Vcc – Connection to Vcc. See schematic and description for VCC jumper.

Grounding – Separate power and signal grounds are provided. Signal GND are the turrets closest to OUTA and OUTB, use these for measurement ground and output return. Power GND is between AMPV+ and AMPV- turrets.


MANUAL SPAN CONTROL
PARALLEL INTERFACE
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0402.
ALL CAPACITORS ARE IN MICROFARADS, 0402.
2. INSTALL SHUNTS ON JUMPERS AS SHOWN.
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DUAL, PARALLEL, IOUT, 16-BIT DAC
SIZE A
DWG NO. DC1111A-1 * LTC2753CUK-16
REV A-1
DATE: Thursday, January 03, 2008
SHEET 1 OF 1
CONTRACT NO.
APPROVALS
DRAWN:
CHECKED:
APPROVED:
ENGINEER: MARK T.
DESIGNER: KIM T.
U1 LTC2753CUK-16
U2 LT1469CS8
U3 74VHC595MTC
U4 74VHC595MTC
U6 74VHC595MTC
U9 74VHC595MTC
U8 LT1236ACS8-5
U10 NC7SZ14P5X
U11 24LC025-I/ST
U12 LT1469CS8
JP1 HD2X20-100
JP2 HD2X3-079
JP3 HD2X3-079
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