Isolated Amplifier with Adjustable Gain and Single-Ended Output

FEATURES

- High-Impedance input for isolated voltage measurement
- Low offset error and drift (output offset voltage): ±6 mV (Max) at 25°C and −22 µV/°C (Typ)
- Low gain error and drift: ±0.5% (max) and ±27 ppm/°C (max)
- Voltage-supply range
  - V_{DD1}: 4.5 V to 5.5 V
  - V_{DD2}: 4.5 V to 5.5 V
- Bandwidth: 210 kHz
- Isolation voltage: 3000 V rms for ADuM3195
- Safety and regulatory approvals (pending)
  - UL recognition (pending): 3000 V rms for 1 minute per UL 1577
  - CSA (pending)
  - VDE certificate of conformity (pending)
    - DIN VDE V 0884-11:2017-01
    - V_{IORM} = 636 V peak (reinforced)
- Wide temperature range
  - −40°C to +125°C ambient operation
  - 150°C maximum junction temperature
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Inverters
- DC to DC converters
- On-board chargers

GENERAL DESCRIPTION

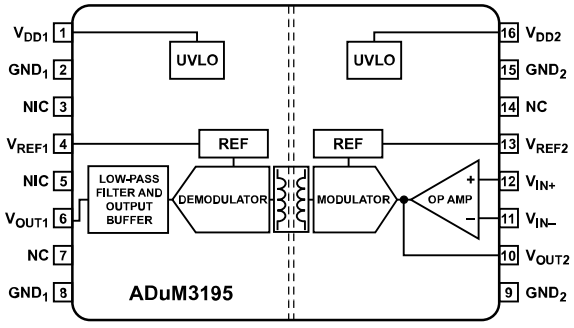
The ADuM3195[1] are isolation amplifiers based on Analog Devices, Inc., *i*Coupler® technology. The ADuM3195 have very low offset and gain error, making them ideal for many isolated voltage sensing applications.

Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over lifetime and at high temperatures, the ADuM3195 transfer functions do not change over lifetime, and are stable over a wide temperature range of −40°C to +125°C.

Included in the ADuM3195 are wideband operational amplifiers useful for a variety of commonly used applications. Included in the ADuM3195 are two high accuracy 2.5 V references outputs.

The ADuM3195 is packaged in a 16-lead quarter small outline package (QSOP) for a 3000 V rms isolation voltage rating.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. NC = NO CONNECT.

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Figure 1.

[1] Protected by U.S. Patents 5,952,849, 6,873,065 and 7,075,329. Other patents pending.

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REVISION HISTORY

4/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{DD1} = V_{DD2} = 4.5 V to 5.5 V for T_A = T_{MIN} to T_{MAX}. All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V, unless otherwise noted.

Table 1. Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
OPERATIONAL AMPLIFIER (OP AMP)					
Input Offset Voltage (V_{OS})	−0.5		+1.5	mV	
Input Offset Drift	−11		+11	µV/°C	
Input Op Amp Gain	85			dB	
Input Common-Mode Range[1]	0.25		V_{DD2} − 0.7	V	
Gain-Bandwidth Product		15		MHz	
Common-Mode Rejection		−85		dB	
Input Resistance		10		GΩ	
Input Capacitance		5		pF	
Input-Bias Current[2]	−0.2		+0.2	nA	T_A = 25°C V_{IN+} or V_{IN-} = 2.5 V
Input-Bias Current Drift	−25		+75	pA/°C	
Op Amp Output Voltage Range[1]	0.1		V_{DD2}	V	
REFERENCE					
Output Voltage, V_{REF1}, V_{REF2}					0 mA to 1 mA load
	2.49	2.50	2.51	V	T_A = 25°C
	2.47	2.50	2.53	V	T_A = T_{MIN} to T_{MAX}
Reference Temperature Coefficient (Tempco)		±25		ppm/°C	
Output Current	1.0			mA	
OUTPUT CHARACTERISTICS					
Linear Output Voltage Range[1]	0.25		V_{DD2} − 0.7	V	
Output Offset Voltage	−6.0		+6.0	mV	V_{OUT1} − V_{IN+} (op amp in buffer configuration), V_{IN+} = 2.5 V−, T_A = 25°C
Output Offset Drift		−22		µV/°C	V_{IN+} = 2.5 V, T_A = −40 to 125°C
Output Gain[3]		1			V_{OUT1}/V_{IN+} (op amp in buffer configuration)
Output Gain Error	−0.5		+0.5	%	
Output Gain Error Drift	−27		+27	ppm/°C	
Output −3 dB Bandwidth		210		kHz	From V_{OUT1} to V_{IN+}
Output Delay		3		µs	50% input to 50% output within V_{IN+} = 1 V to 4 V
Output Rise and Fall time		2		µs	10% to 90% within V_{IN+} = 1 V to 4 V
Output Noise		540		µV rms	f_{IN} = 1 kHz, bandwidth = 100 kHz
		1		mV rms	f_{IN} = 1 kHz, bandwidth = 200 kHz
SNR		69		dB	f_{IN} = 1 kHz, bandwidth = 100 kHz
		64		dB	f_{IN} = 1 kHz, bandwidth = 200 kHz
Total Harmonic Distortion Plus Noise (THD + N) Ratio		−54		dB	f_{IN} = 1 kHz, bandwidth = 100 kHz
		−56		dB	f_{IN} = 1 kHz, bandwidth = 200 kHz
Signal-to-Noise-and-Distortion (SINAD) Ratio		57		dB	f_{IN} = 1 kHz, bandwidth = 100 kHz
		56		dB	f_{IN} = 1 kHz, bandwidth = 200 kHz
Power-Supply Rejection Ratio (PSRR)		−60		dB	DC, V_{DD1} = V_{DD2} = 4.5 V to 5.5 V
Output Resistive Load	10			kΩ	
Output Capacitive Load			100	pF	
Common-Mode Transient Immunity (CMTI)[2, 4]	100	150		kV/µs	$\|GND_1 - GND_2\|$ = 1.5 kV
POWER SUPPLY					
Operating Range, Side 1	4.5	5.0	5.5	V	V_{DD1}

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
Undervoltage Lockout (UVLO) Positive Going Threshold		4.2		V	
UVLO Negative Going Threshold		4.0		V	
Operating Range, Side 2	4.5	5.0	5.5	V	V_{DD2}
UVLO Positive Going Threshold		4.2		V	
UVLO Negative Going Threshold		4.0		V	
V_{OUT1} Impedance		35		Ω	V_{DD1} = 5 V, V_{DD2} < UVLO threshold
		3.7		kΩ	V_{DD1} < UVLO threshold
Supply Current					
I_{DD1}		4.1	4.9	mA	
I_{DD2}		5.9	7.3	mA	

[1] For a maximum deviation of ±1.25% from the best-fit line over the specified input range of 1 V to 3.5 V. Op amp in buffer configuration.

[2] Guaranteed by design and characterization. Not production tested.

[3] Output gain defined as the slope of the best-fit line over the specified input range, with the offset error adjusted out.

[4] CMTI error is an output disturbance greater than 100 mV lasting more than 2 µs.

PACKAGE CHARACTERISTICS

Table 2. Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE						
Input-to-Output[1]	R_{I-O}		10^{13}		Ω	
CAPACITANCE						
Input-to-Output[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC JUNCTION-TO-AMBIENT THERMAL RESISTANCE						
16-Lead QSOP	θ_{JA}		83		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device; Pins 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

[2] Input capacitance is from any input data pin to ground.

SPECIFICATIONS

REGULATORY INFORMATION

Table 3. ADuM3195 Regulatory Information (Pending)

UL	CSA[1]	VDE[2]
Recognized Under 1577 Component Recognition Program[3]		Certified according to DIN VDE V 0884-11:2017-01
Single Protection, 3000 V rms Isolation Voltage, 16-Lead QSOP	Basic insulation per CSA 62638-1-03 and IEC 62638-1, 350 V rms (495 V peak) maximum working voltage Reinforced insulation per CSA 62638-1-03 and IEC 62638-1, 175 V rms (247 V peak) maximum working voltage	Reinforced insulation, 636 V peak V_{IOTM} = 4200 V pk, V_{IOSM} = 6250 V pk
File E214100 (pending)	File (pending)	(pending)

[1] Working voltages are quoted for Pollution Degree 2, Material Group III.

[2] In accordance with DIN VDE V 0884-11:2017-01, each ADuM3195 is proof tested by applying an insulation test voltage ≥ 1192 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11:2017-01 approval.

[3] In accordance with UL 1577, each ADuM3195 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec (current leakage detection limit = 5 µA).

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	3.2	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	3.2	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	3.8	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the printed circuit board (PCB) mounting plane
Minimum Internal Gap (Internal Clearance)		0.041	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Material Group		II		Material Group DIN VDE 0110, 1/89, Table 1

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
OPERATING TEMPERATURE	T_A	−40	+125	°C
SUPPLY VOLTAGES[1]	V_{DD1}, V_{DD2}	4.5	5.5	V

[1] All voltages are relative to their respective grounds.

SPECIFICATIONS

DIN VDE V 0884-11:2017-01 INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The asterisk (*) marking branded on the package denotes DIN VDE V 0884-11:2017-01 approval (pending).

Table 6. ADuM3195 VDE V 0884-11 Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic[1]	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	636	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	1192	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	954	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	763	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4200	V_{PEAK}
Surge Isolation Voltage	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6250	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.51	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN VDE V 0884-11:2017-01.

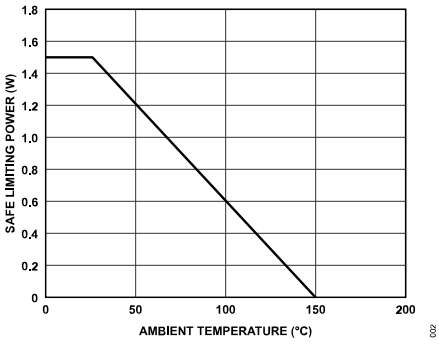

Figure 2. Thermal Derating Curve for the ADuM3195, Dependence of Safety Limiting Values on Case Temperature, Per DIN VDE V 0884-11:2017-01

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7. Absolute Maximum Ratings

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Junction Temperature (T_J)	−40°C to +150°C
Supply Voltages	
V_{DD1}, V_{DD2}[1]	−0.5 V to +7.0 V
Input Voltages	
V_{IN+}, V_{IN-}	−0.5 V to V_{DD2} +0.5 V
Output Voltages	
V_{REF1}, V_{OUT1}, V_{REF2}, V_{OUT2}	−0.5 V to V_{DD1} +0.5 V, −0.5 V to V_{DD2} +0.5 V
Output Current per Output Pin	−11 mA to +11 mA
Common-Mode Transients[2]	−200 kV/µs to +200 kV/µs

1 All voltages are relative to their respective grounds.

2 Refers to the common-mode transients across the insulation barrier. The common-mode transients exceeding the absolute maximum ratings may cause latchup or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. Maximum Continuous Working Voltage for the RQ-16 (QSOP) Package

Parameter[1]	Rating	Constraint
AC Voltage Bipolar Waveform		
Basic Insulation	450 V_{rms}	Basic insulation rating per IEC 60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	225 V_{rms}	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
DC Voltage		
Basic Insulation	450 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
Reinforced Insulation	225 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.

1 Refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

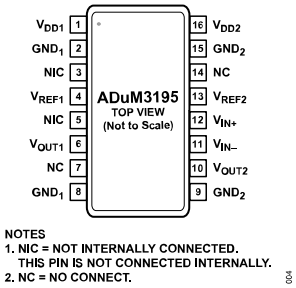

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Side 1, Pin 1 to Pin 8 (4.5 V to 5.5 V). Connect a 0.1 µF and a 1 µF capacitor between V_{DD1} and GND_1.
2	GND_1	Ground Reference for Side 1.
3	NIC	Not Internally Connected. This pin is not connected internally. Connect this pin to V_{DD1}, GND_1, or leave floating.
4	V_{REF1}	Reference Output Voltage for Side 1. The maximum capacitance for this pin ($C_{REFOUT1}$) must not exceed 15 pF.
5	NIC	Not Internally Connected. This pin is not connected internally. Connect this pin to V_{DD1}, GND_1, or leave floating.
6	V_{OUT1}	Isolated Output Voltage.
7	NC	No Connect. Connect this pin to GND_1. Do not leave it floating.
8	GND_1	Ground Reference for Side 1.
9	GND_2	Ground Reference for Side 2 (Pin 9 to Pin 16).
10	V_{OUT2}	Output of the Op Amp.
11	V_{IN-}	Inverting Op Amp Input.
12	V_{IN+}	Noninverting Op Amp Input.
13	V_{REF2}	Reference Output Voltage for Side 2. The maximum capacitance for this pin (C_{REFOUT}) must not exceed 22 nF.
14	NC	No Connect. Connect this pin to GND_2. Do not leave it floating.
15	GND_2	Ground Reference for Side 2.
16	V_{DD2}	Supply Voltage for Side 2 (4.5 V to 5.5 V). Connect a 0.1 µF and a 1 µF capacitor between V_{DD1} and GND_1.

TYPICAL PERFORMANCE CHARACTERISTICS

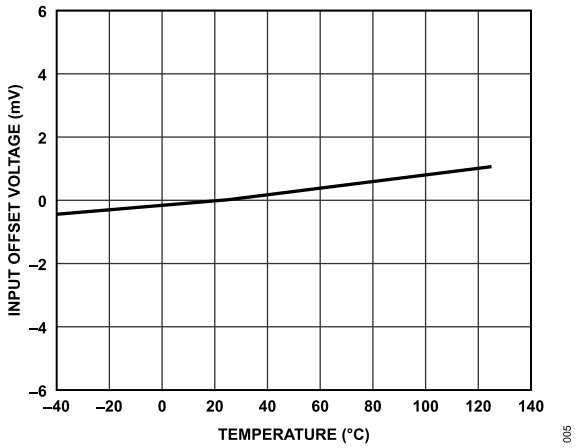

Figure 4. Op Amp Input Offset Voltage vs. Temperature

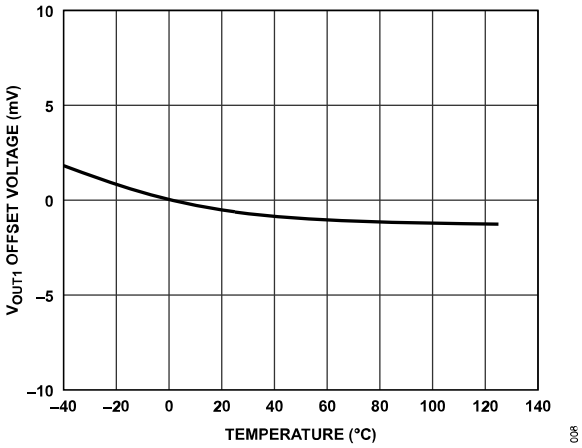

Figure 7. V_{OUT1} Offset Voltage vs. Temperature

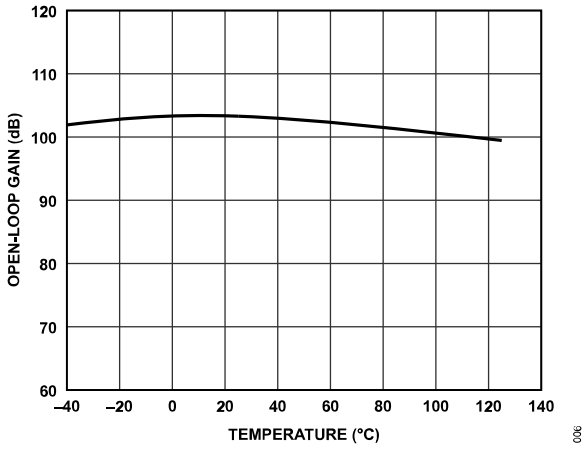

Figure 5. Op Amp Open-Loop Gain vs. Temperature

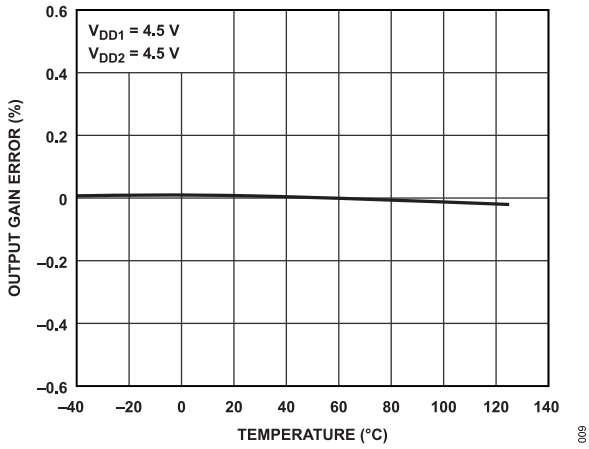

Figure 8. Output Gain Error vs. Temperature

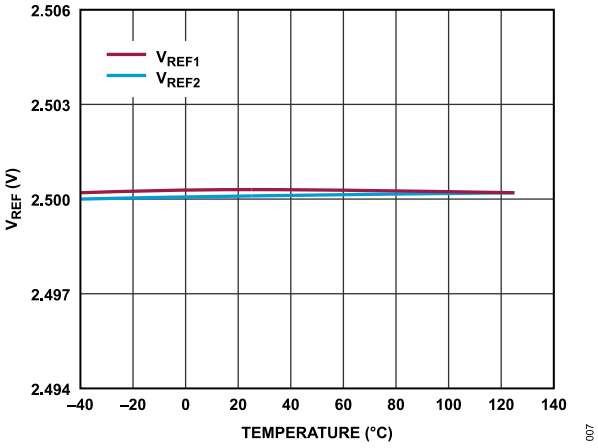

Figure 6. V_{REF} vs. Temperature

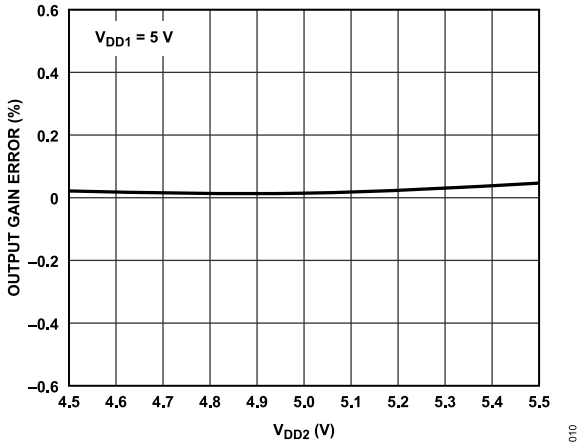

Figure 9. Output Gain Error vs. V_{DD2}

TYPICAL PERFORMANCE CHARACTERISTICS

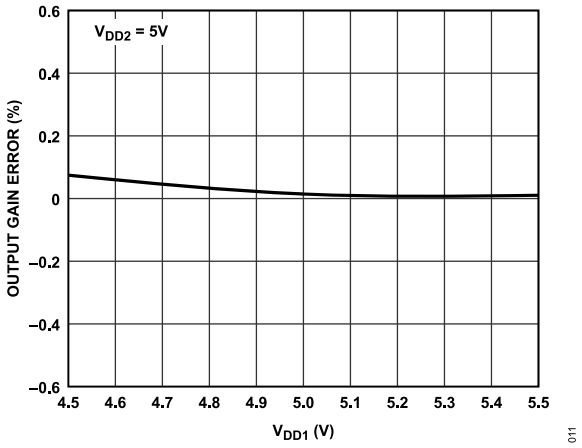

Figure 10. Output Gain Error vs. V_{DD1}

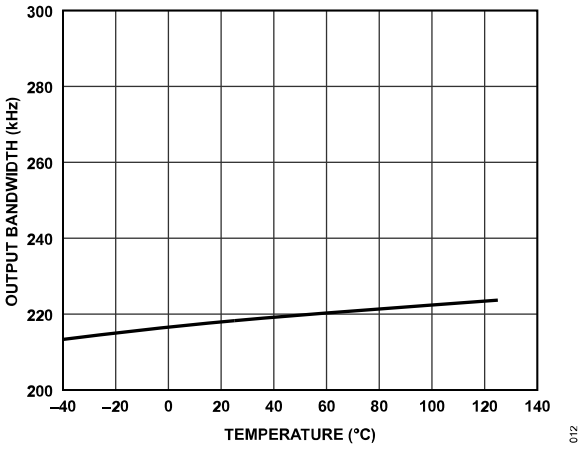

Figure 11. Output Bandwidth vs. Temperature

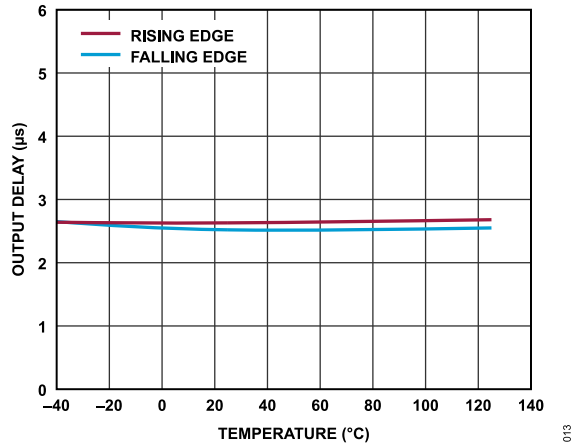

Figure 12. Output Delay vs. Temperature

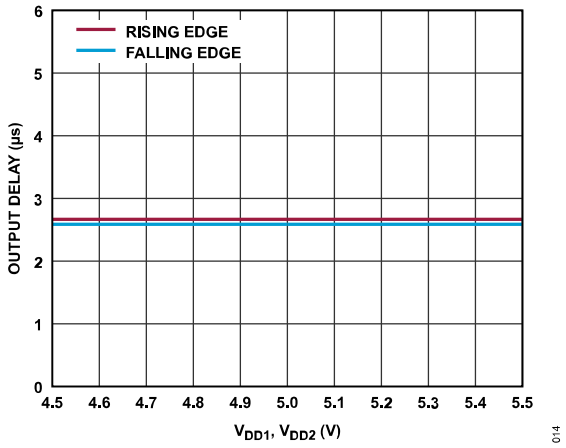

Figure 13. Output Delay vs. Supply Voltage

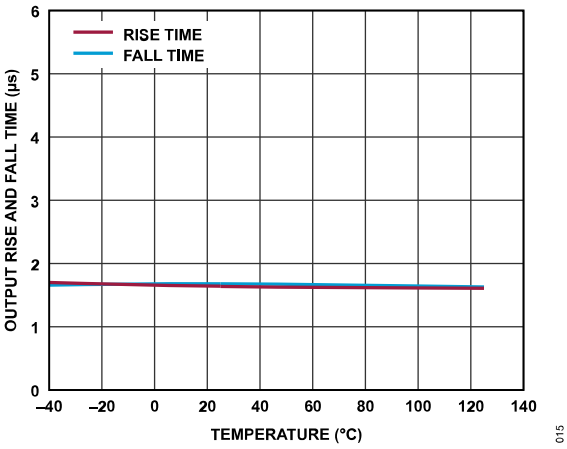

Figure 14. Output Rise and Fall Time vs. Temperature

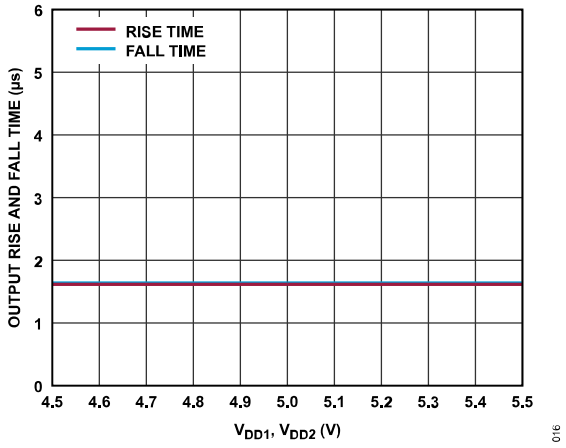

Figure 15. Output Rise and Fall Time vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

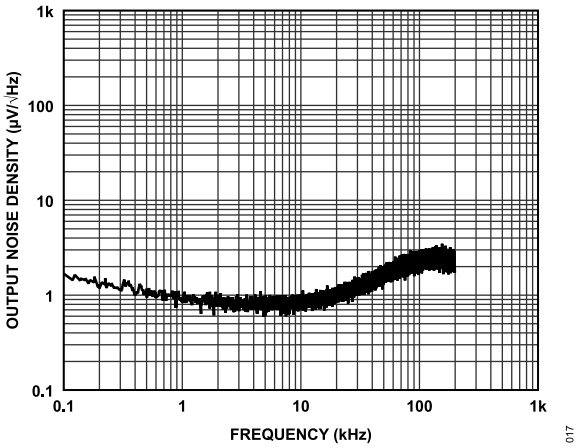

Figure 16. Output Noise Density vs. Frequency

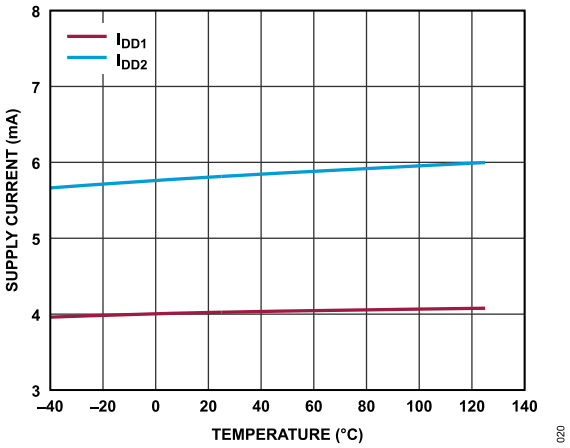

Figure 19. Supply Current vs. Temperature

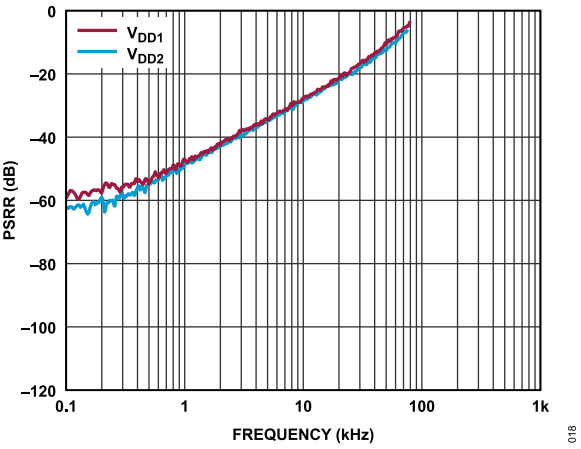

Figure 17. PSRR vs. Frequency

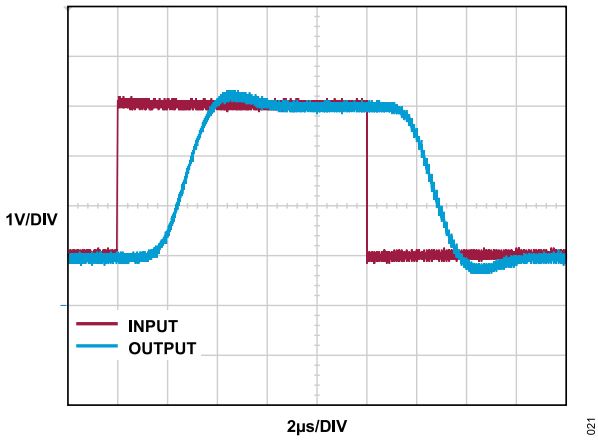

Figure 20. Output Square-Wave Response

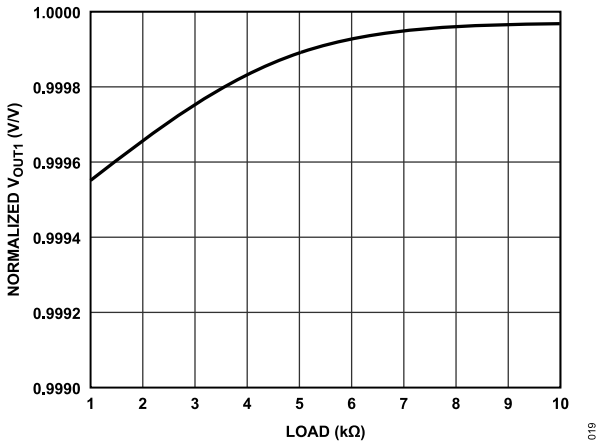

Figure 18. Normalized V_{OUT1} vs. Load

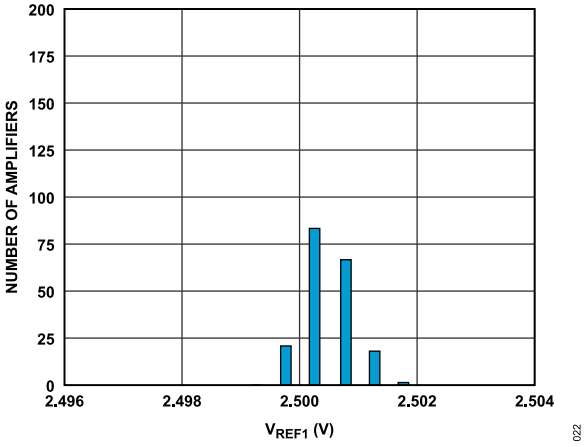

Figure 21. V_{REF1} Distribution at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

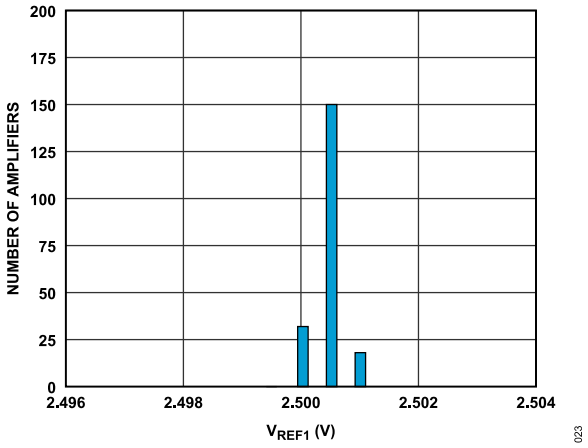

Figure 22. V_{REF1} Distribution at 125°C

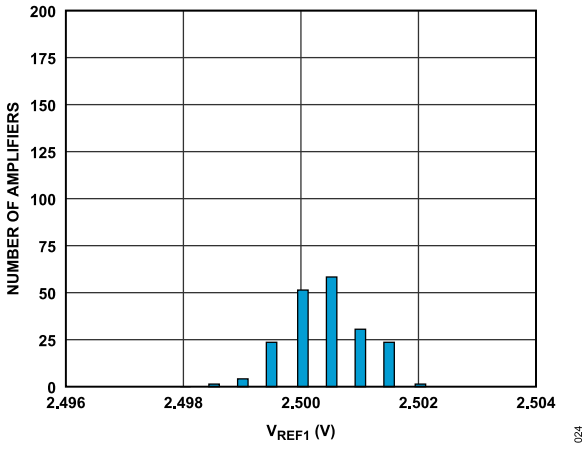

Figure 23. V_{REF1} Distribution at −40°C

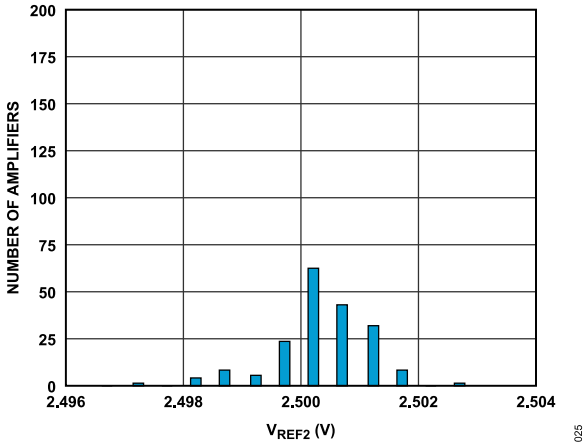

Figure 24. V_{REF2} Distribution at 25°C

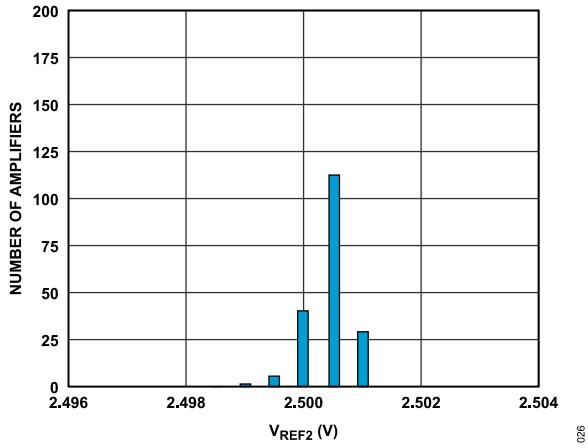

Figure 25. V_{REF2} Distribution at 125°C

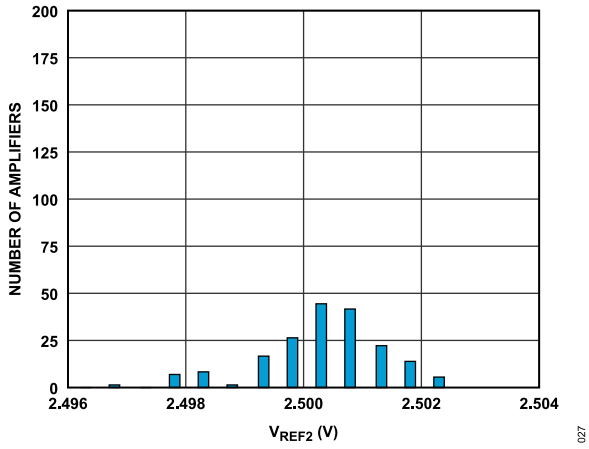

Figure 26. V_{REF2} Distribution at −40°C

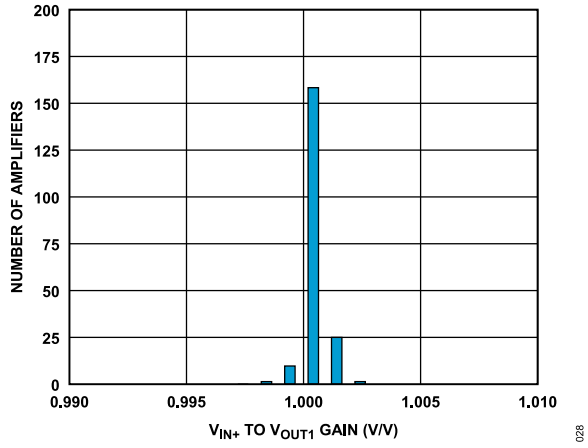

Figure 27. V_{IN+} to V_{OUT1} Gain Distribution at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

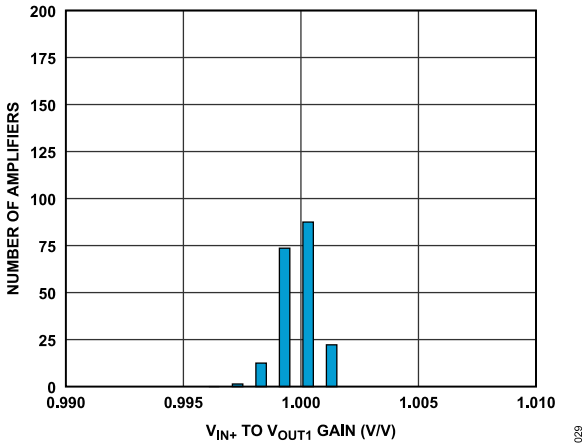

Figure 28. V_{IN+} to V_{OUT1} Gain Distribution at 125°C

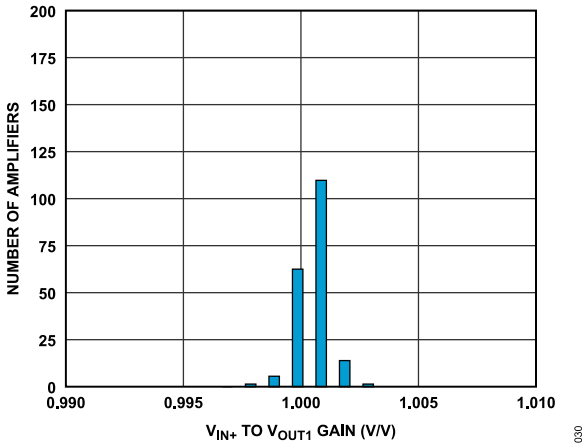

Figure 29. V_{IN+} to V_{OUT1} Gain Distribution at −40°C

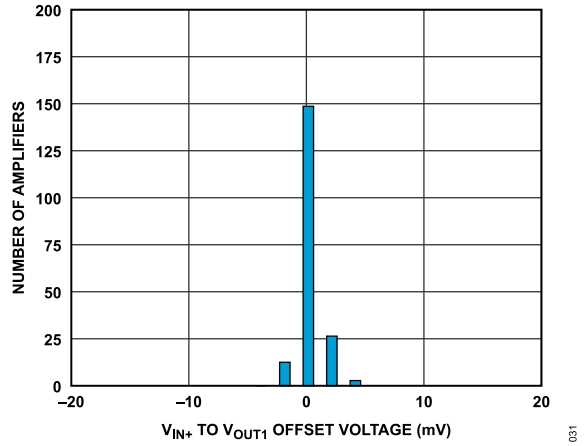

Figure 30. V_{IN+} to V_{OUT1} Offset-Voltage Distribution at 25°C, Output Offset Voltage for V_{IN+} = 2.5 V Op Amp in Buffer Configuration

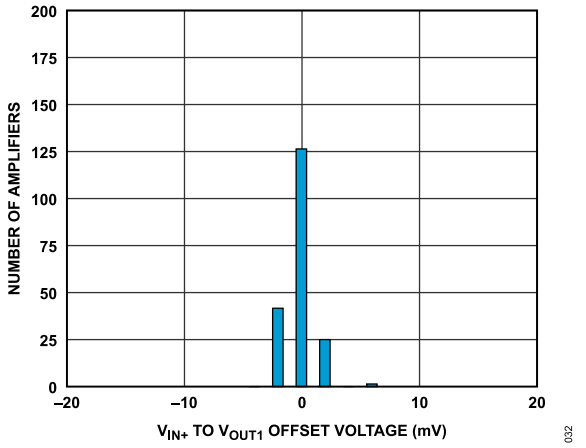

Figure 31. V_{IN+} to V_{OUT1} Offset-Voltage Distribution at 125°C

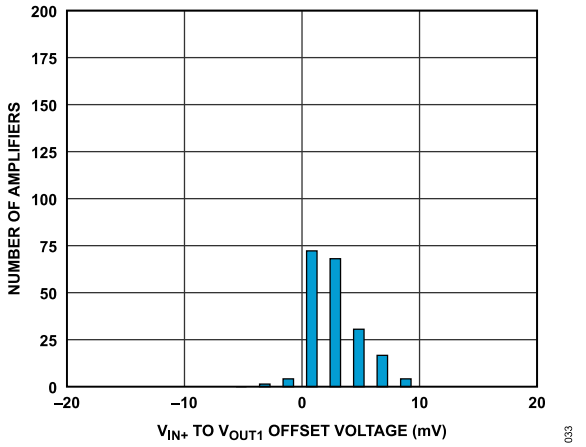

Figure 32. V_{IN+} to V_{OUT1} Offset-Voltage Distribution at −40°C

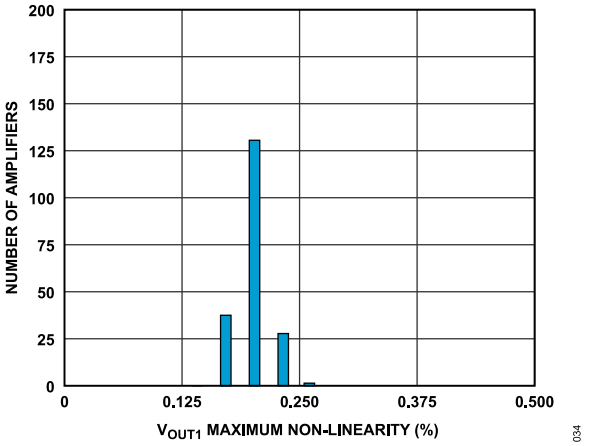

Figure 33. V_{OUT1} Maximum Non-Linearity Distribution at 25°C, Maximum Non-Linearity Defined Within V_{IN+} Input Range: 1 V to 3.5 V, as an Absolute Value

TYPICAL PERFORMANCE CHARACTERISTICS

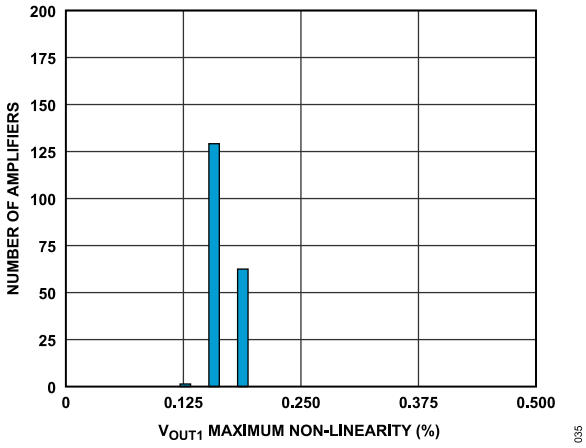

Figure 34. V_{OUT1} Maximum Non-Linearity Distribution at 125°C

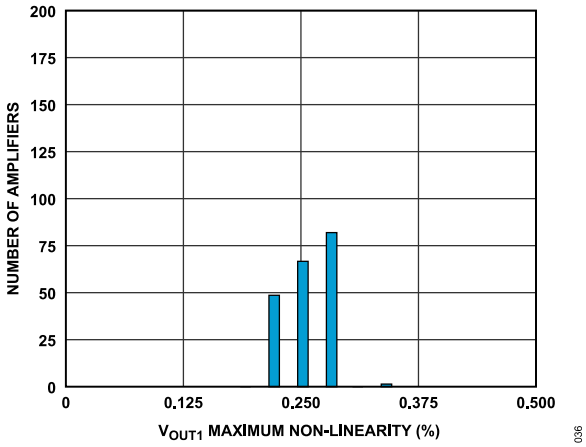

Figure 35. V_{OUT1} Maximum Non-Linearity Distribution at −40°C, Maximum Non-Linearity Defined Within V_{IN+} Input Range: 1 V to 3.5 V, as an Absolute Value

THEORY OF OPERATION

The ADuM3195 is an isolated amplifier (IA) based on Analog Devices, Inc., iCoupler® technology. The input side of the IA consists of an operational amplifier with input pins V_{IN+} and V_{IN-}, and output pin V_{OUT2}. The V_{IN+}, V_{IN-}, and V_{OUT2} pins can be used to configure the IA for a wide range of applications such as IA with configurable gain, inverting IA, or as a voltage controller in isolated feedback loops for power supplies. A highly linear pulse width modulation (PWM) compares the output of the operational amplifier to the internal voltage reference V_{REF2} and sends the duty cycle (ratio) information to the demodulator through a coreless transformer. On the output side of the IA, the demodulator uses the ratio information and the reference voltage V_{REF1} to reconstruct the output voltage, which is then low-pass filtered, buffered, and presented at output pin V_{OUT1}. Thus, with the input operational amplifier configured as a voltage follower, the overall signal gain of the IA defaults to 1.

APPLICATIONS INFORMATION

APPLICATION BLOCK DIAGRAM

Figure 36 shows a typical application for the ADuM3195 as an isolated voltage monitor. The ADuM3195 offers unique linearity, high common-mode noise immunity, low gain errors, and temperature drift. These features make it a robust and high performance isolated amplifier for industrial applications with high-voltage sensing required. The high-voltage bus is sensed by the R1 voltage divider and the R2 voltage divider. As the input op amp of the IA is configured as a unity-gain amplifier, the voltage on the V_{OUT2} is equal to the sensed bus voltage multiplied by the voltage-divider ratio. Due to the very high input impedance of the V_{IN+} pin, the current through the resistive divider can be kept low without sacrificing accuracy, therefore allowing for a low-power dissipation on the resistors. For very high voltages on the VBUS however, possible pollution on the PCB must also be taken into consideration when planning to design for the low input currents. Also, protective elements (such as diodes or Zener-diodes) in parallel with the R2 voltage divider may negatively affect the accuracy of the voltage divider and must be selected for the lowest reverse leakage currents over the desired temperature range. In such a case, a capacitive protection method as shown in Figure 36 may be a more viable approach.

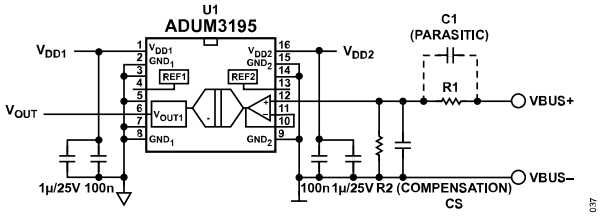

Figure 36. DC Bus Voltage Monitoring Using ADuM3195

The high-voltage bus is sensed by a voltage divider, which consists of the R1 and the R2. As described in the previous section, the V_{OUT1} voltage follows the V_{IN+} with a typical gain of 1.

When monitoring very high bus voltages, the parasitic capacitances of the R1 can impose a risk of overvoltage spikes on the V_{IN+} during switching events on the VBUS. The recommendation is to connect a compensation capacitor C2 in parallel to the R2. Proper compensation is achieved by selecting C2 such that

$$C2 = R1 \times C1/R2 \quad (1)$$

The value of C2 is not critical but must be selected slightly higher than the calculated value to suppress any overshoot on the V_{IN+} during the switching events on the VBUS. For example, if $VBUS_{max}$ = 1 kV DC and V_{OUT} = 4.3 V, the required divider ratio is approximately 1/233, where R1 = 2 MΩ and R2 = 8.62 kΩ. With an estimated parasitic capacitance C1 of approximately 10 pF, the compensation capacitance becomes C2 ≥ 2.3 nF.

Figure 37 shows an AC voltage monitoring application. In Figure 37, the V_{REF2} (Pin 13) is used to create a 2.5 V bias voltage for the input op amp. The bias resistor R3 with the coupling capacitor C3, form the AC coupling circuit and high-pass filter to the AC input divider of the circuit. With R3 at least an order of magnitude larger than R2, a compensation capacitor in parallel with R2 provides a flat, high-frequency response when tuned to R1 × C1 = R2 × C2. The low-frequency roll-off is then defined by R3 and C3.

With the supplies V_{DD2} and V_{DD1} = 5 V DC, the acceptable AC input voltage range across R2 is approximately V_{R2} = 3.6 V (peak-to-peak) or 1.27 V (rms).

Note that in this configuration V_{OUT1} is also biased to V_{REF}, therefore an upstream analog-to-digital converter (ADC) can be fed directly without further biasing.

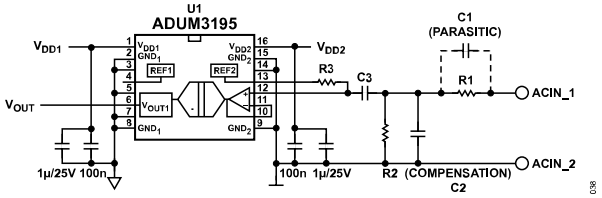

Figure 37. AC Voltage Monitoring Using ADuM3195

On occasions, it may be necessary to invert the monitored bus voltage. In such a case, the input stage of the ADuM3195 can be configured as an inverting amplifier as shown in Figure 38.

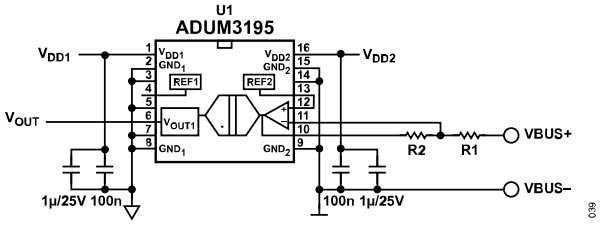

Figure 38. ADuM3195 Configured as Inverting Amplifier

With the V_{REF2} directly wired to the V_{IN+}, the V_{OUT2} can be calculated as

$$V_{OUT2} = V_{REF2} - R2/R1 \times (VBUS - V_{REF2}) \quad (2)$$

Figure 39 shows another typical application for the ADuM3195 as an isolated error amplifier in a DC to DC power converter.

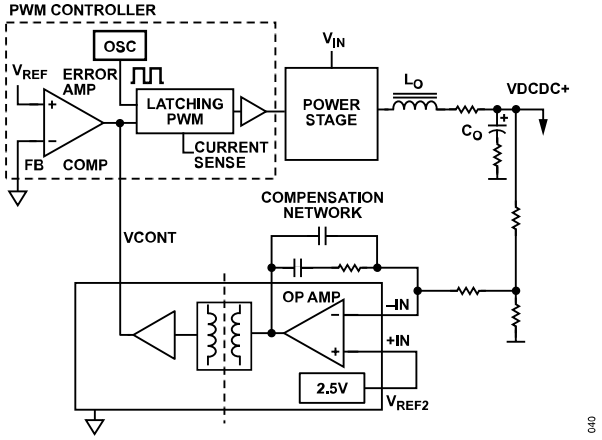

Figure 39. Isolated DC to DC Converter Application Diagram

APPLICATIONS INFORMATION

The output voltage of the converter is sensed though a voltage divider and then connected to the V_{IN-} to compare with the V_{REF2} (see Figure 40). The error between the sensed voltage and the V_{REF2} is accumulated by the compensation network and transmitted to the voltage on V_{OUT1}. V_{OUT1} is then used to generate the PWM signals in a PWM controller. The PWM signals drive the power switches in the converter's power stage to regulate the output voltage.

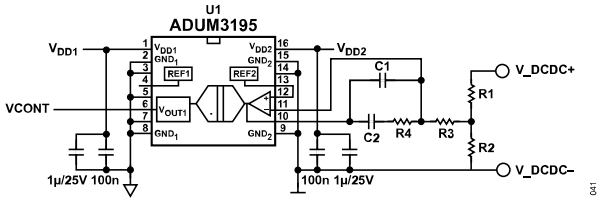

Figure 40. DC to DC Converter V_{OUT} Setting

The output of the DC to DC power converter, V_{DCDC}, can be determined by the following equation, where V_{REF2} = 2.5 V:

$$V_{DCDC} = V_{REF2} \times (R_1 + R_2)/R_2 \quad (3)$$

DESIGN EXAMPLE

For a typical DC bus voltage monitoring application, as shown in Figure 37, the following design procedure can be used:

Table 10. Example Design Parameters

Parameter	Value	Comment
V_{DD2} (min)	5.0 V DC	Lowest V_{DD2} supply
VBUS (max)	1000 V DC	Highest expected bus voltage
I_{DIV}	500 µA	Limit power loss in divider to 0.5 W

Determine the minimum V_{DD2} in your system. This in turn determines the maximum V_{IN} that can be linearly transmitted across the isolation barrier.

$$V_{IN} (max) = V_{DD2} (min) – 0.7 V = 5.0 V – 0.7 V = 4.3 V \quad (4)$$

Determine the ratio 1/K of the voltage divider R1 and R2 for a given maximum of VBUS (max), so that 1/K is about 0 to 10% larger than the VBUS (max)/V_{IN} (max).

$$1/K = (R1 + R2)/R2 = VBUS (max)/V_{IN} (max), \quad (5)$$

$$1/K = 1 ... 1.1 \times (1000 V/4.3 V) = 232.558 ... 255.814 \quad (6)$$

For the given I_{DIV}, the minimum divider input resistance (R_{IN}) must meet as follows:

$$R_{IN} = (R1 + R2) > VBUS (max)/I_{DIV} = 1 kV DC/500 µA = 2 MΩ \quad (7)$$

Also, the ratio of R1/R2 can be expressed as

$$R1/R2 = (1/K) – 1 = 231.558 ... 254.814 \quad (8)$$

Thus, when selecting R1 as two 1 MΩ high-voltage resistors in a series, R2 can be calculated as

$$R2 = 2 MΩ \times K = 8.6k Ω ... 7.82 kΩ \quad (9)$$

The divider's output resistance, R_{OUT}, with the input bias current, I_{BIAS}, defines the amount of bias error, which adds to the total error of the system. Bias error can be avoided by selecting R1 and R2 so that

$$R_{OUT} = R1||R2 < 100 kΩ, \quad (10)$$

with above calculated resistors R1 and R2,

$$R_{OUT} = 2 MΩ||7.82 kΩ = 7.8 kΩ, \quad (11)$$

which is well below the limit for R_{OUT}.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM3195 is highly immune to the external magnetic fields. The limitation on the ADuM3195 magnetic field immunity is set by the condition whereby the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 4.5 V operating condition of the ADuM3195 is examined because it represents the most susceptible mode of operation. The decoder can tolerate up to a 1.6 V noise induced by an external magnetic field. Assuming that there is a 50% margin, the decoder can safely operate with up to a 0.8 V induced noise. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \Sigma\pi rn^2, n = 1, 2,..., N \quad (12)$$

where:
β is the magnetic field strength (Gs).
rn is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3195 and an imposed requirement that the induced voltage be, at most, 50% of the 1.6 V threshold at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 41.

APPLICATIONS INFORMATION

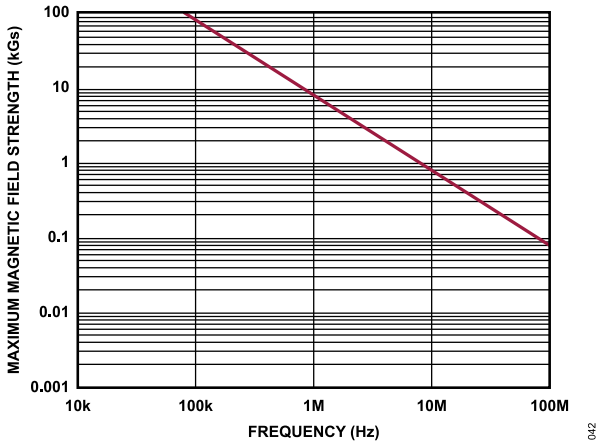

Figure 41. Maximum Allowable External Magnetic Field Strength

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 8 kGs induces a voltage of 0.8 V at the receiving coil. This is approximately 50% of the decoder threshold and does not cause a faulty output transition. The preceding magnetic field strength values correspond to the specific current magnitudes at given distances away from the ADuM3195 transformers. Figure 42 shows these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 43, the ADuM3195 is immune and can be affected only by extremely large currents operating at a high frequency very close to the component. For the 1 MHz example, a 20 kA current must be placed 5 mm away from the ADuM3195 to affect the operation of the device.

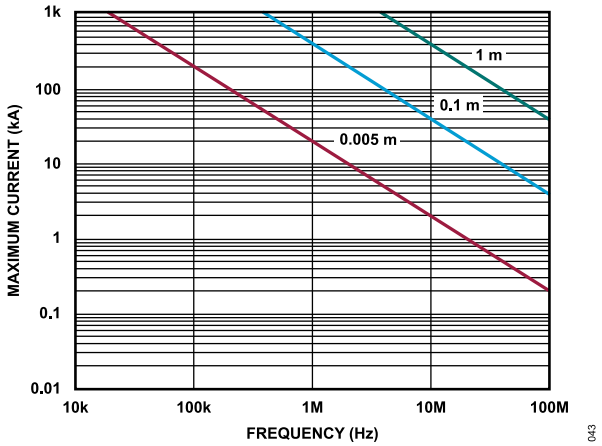

Figure 42. Maximum Allowable Current for Various Current-to-ADuM3195 Spacings

LAYOUT CONSIDERATIONS

VDD_1 and VDD_2 must be decoupled to their respective GND_1 and GND_2 with capacitors of at least 1 µF in parallel with 100 nF. In applications involving fast common-mode transients, ensure that the board coupling across the isolation barrier is minimized. To fully use the specified isolation properties of the ADuM3195, the top and bottom copper layers of the PCB must not reach underneath the package, but must instead only reach as far as the solder-pad area. Place any decoupling used as close to the supply pins as possible. See Figure 43 for component placement suggestion.

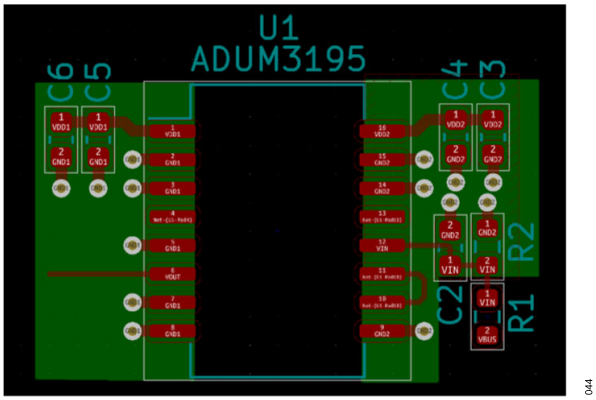

Figure 43. Placement of Decoupling Capacitors and Ground Planes GND_1

OUTLINE DIMENSIONS

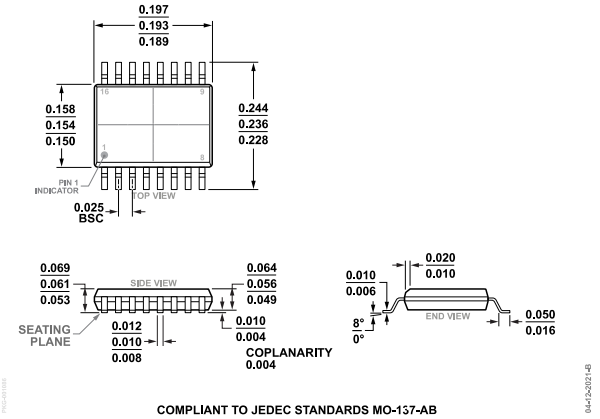

Figure 44. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADuM3195BRQZ	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM3195BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM3195WBRQZ	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM3195WBRQZ-RL7	−40°C to +125°C	16-Lead QSOP	RQ-16

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

EVALUATION BOARD

Model[1]	Description
EVAL-ADUM3195EBZ	ADuM3195 Evaluation Board

[1] Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The ADuM3195 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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