



Precision Analog Microcontroller, 14-Bit Analog I/O with MDIO Interface, Arm Cortex-M3

Data Sheet

ADuCM320i

FEATURES

Analog input/output

- Multichannel, 14-bit, 1 MSPS analog-to-digital converter (ADC)
- Up to 16 ADC input channels
- 0 V to V_{REF} analog input range
- Fully differential and single-ended modes
- AV_{DD} and IOV_{DD} monitors
- 12-bit voltage output digital-to-analog converters (VDACs)
- 8 VDACs with a range of 0 V to 2.5 V or AV_{DD} outputs
- 12-bit current output DACs (IDACs)
- 4 IDACs with a range of 0 mA to 150 mA outputs
- Voltage comparator

Microcontroller

- Arm Cortex-M3 processor, 32-bit RISC architecture
- Serial wire port supports code download and debug

Clocking options

- 80 MHz PLL with programmable divider
- Trimmed on-chip oscillator ($\pm 3\%$)
- External 16 MHz crystal option
- External clock source up to 80 MHz

Memory

- 2 × 128 kB independent Flash/EE memories
- 10,000 cycle Flash/EE endurance
- 20-year Flash/EE retention
- 32 kB SRAM

In circuit reprogrammability via I²C

On-chip peripherals

- MDIO slave up to 4 MHz
- 2 × I²C, 2 × SPI, UART
- Multiple general-purpose input/output (GPIO) pins: 3.6 V compliant
- 7 × 1.2 V compatible when used for MDIO
- 32-element programmable logic array (PLA)
- 3 general-purpose timers
- Wake-up timer
- Watchdog timer
- 16-bit pulse width modulator (PWM)

Power

- Supply range: 2.9 V to 3.6 V, and 1.8 V to 2.5 V for IDACs
- Flexible operating modes for low power applications

Package and temperature range

- 6 mm × 6mm, 96-ball CSP_BGA package
- Fully specified for -40°C to +105°C ambient operation

Tools

- Low cost QuickStart development system
- Full third party support

APPLICATIONS

Optical networking

Rev. A

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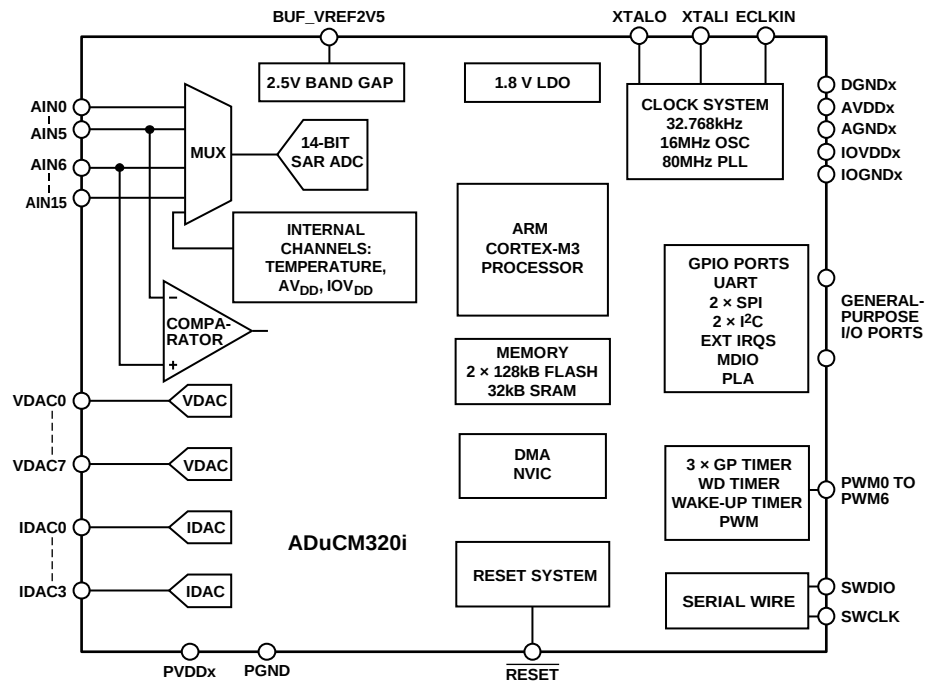
REVISION HISTORY

4/2018—Rev. 0 to Rev. A

Change to Features Section	1
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8/2015—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



13422-001

GENERAL DESCRIPTION

The [ADuCM320i](#) is a fully integrated single package device that incorporates high performance analog peripherals together with digital peripherals controlled by an 80 MHz Arm® Cortex™-M3 processor and integral flash for code and data.

The ADC on the [ADuCM320i](#) provides 14-bit, 1 MSPS data acquisition on up to 16 input pins that can be programmed for single-ended or differential operation. The voltage at the IDAC output pins can also be measured by the ADC, which is useful for controlling the power consumption of the current DACs. Additionally, chip temperature and supply voltages can be measured.

The ADC input voltage is 0 V to V_{REF} . A sequencer is provided, which allows a user to select a set of ADC channels to be measured in sequence without software involvement during the sequence. The sequence can optionally repeat automatically at a user selectable rate.

Up to eight VDACS are provided with output ranges that are programmable to one of two voltage ranges.

Four IDAC sources are provided. The output currents are programmable with a range of 0 mA to 150 mA. A low drift band gap reference and voltage comparator completes the analog input peripheral set.

The [ADuCM320i](#) can be configured so that the digital and analog outputs retain their output voltages and currents through a watchdog or software reset sequence. Thus, a product can remain functional even while the [ADuCM320i](#) is resetting itself.

The [ADuCM320i](#) has a low power Arm Cortex-M3 processor and a 32-bit RISC machine that offers up to 100 MIPS peak performance. Also integrated on chip are 2×128 kB Flash/EE memory and 32 kB of SRAM. The flash comprises two separate 128 kB blocks supporting execution from one flash block and simultaneous writing/erasing of the other flash block.

The [ADuCM320i](#) operates from an on-chip oscillator or a 16 MHz external crystal and a PLL at 80 MHz. This clock can optionally be divided down to reduce current consumption. Additional low power modes can be set via software. In normal operating mode, the [ADuCM320i](#) digital core consumes about 300 μ A per MHz.

The device includes an MDIO interface capable of operating at up to 4 MHz. The capability to simultaneously execute from one flash block and write/erase the other flash block makes the [ADuCM320i](#) ideal for 10G, 40G, and 100G optical applications. User programming is eased by incorporating PHYADR and DEVADD hardware comparators. In addition, the nonerasable kernel code plus flags in user flash provide assistance by allowing user code to robustly switch between the two blocks of user flash code and data spaces.

The [ADuCM320i](#) integrates a range of on-chip peripherals that can be configured under software control, as required in the application. These peripherals include $1 \times$ UART, $2 \times$ I²C, and $2 \times$ SPI serial input/output (I/O) communication controllers, GPIO, 32-element programmable logic array, 3 general-purpose timers, plus a wake-up timer and system watchdog timer. A 16-bit PWM with seven output channels is also provided.

GPIO pins on the device power up in high impedance input mode. In output mode, the software chooses between open-drain mode and push-pull mode. The pull-up resistors can be disabled and enabled in software. In GPIO output mode, the inputs can remain enabled to monitor the pins. The GPIO pins can also be programmed to handle digital or analog peripheral signals, in which case the pin characteristics are matched to the specific requirement.

A large support ecosystem is available for the Arm Cortex-M3 processor to ease product development of the [ADuCM320i](#). Access is via the Arm serial wire debug port (SW-DP). On-chip factory firmware supports in-circuit serial download via I²C. These features are incorporated into a low cost QuickStart™ development system supporting this precision analog microcontroller family.

Note that throughout this data sheet, multifunction pins, such as VDACC0/P5.3, are referred to either by the entire pin name or by a single function of the pin, for example, VDACC0, when only that function is relevant.

SPECIFICATIONS

MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AV_{DD} (the voltage applied to the AVDD3 and AVDD4 pin) = IOV_{DDx} (the voltage applied to the IOVDDx pins (IOVDD0, IOVDD1, IOVDD2)) = V_{DD1} (the voltage applied to the VDD1 pin) = 2.9 V to 3.6 V (see Figure 14) maximum difference between supplies = 0.3 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 80 MHz, T_A = -40°C to $+105^{\circ}\text{C}$, unless otherwise noted. PV_{DDx} (the voltage applied to the PVDDx pins (PVDD0, PVDD1, PVDD2, PVDD3)) for IDACs = 1.8 V to 2.5 V. Power-up sequence must be VDD1, IOVDDx, AVDDx, and then PVDDx, but no delays in the sequence are required.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments	
ADC BASIC SPECIFICATIONS							
ADC Power-Up Time	f _{SAMPLE}		5		μs	Single-ended mode, unless otherwise stated	
Data Rate				1	MSPS		
DC Accuracy ¹			14			Bits	1 LSB = 2.5 V/2 ¹⁴
Resolution ¹			16			Bits	Number of data bits
Integral Nonlinearity	INL		±1.75		LSB	2.5 V internal reference; 1 LSB = 2.5 V/2 ¹⁴	
			±1.75		LSB	2.5 V external reference; 1 LSB = 2.5 V/2 ¹⁴	
Differential Nonlinearity	DNL	−0.99	±0.75	+1	LSB	2.5 V internal reference; 1 LSB = 2.5 V/2 ¹⁴	
			±0.75		LSB	2.5 V external reference; 1 LSB = 2.5 V/2 ¹⁴	
DC Code Distribution			±3		LSB	ADC input 1.25 V; 1 LSB = 2.5 V/2 ¹⁴	
ADC ENDPOINT ERRORS							
Offset Error					μV	Using 2.5 V external reference	
Input Buffer Off			±200		μV/°C		
Drift ¹		−2.25		+1.2	μV/°C		
Input Buffer On			−250		μV	Using 2.5 V external reference	
Drift ¹		−2.6		+2	μV/°C		
Match			±1		LSB		Matching compared to AIN8
Full-Scale Error							
Input Buffer Off			±400		μV	Full-scale error drift minus offset error drift	
Gain Drift ¹		−4		+2	μV/°C		
Input Buffer On			−350		μV		Full-scale error drift minus offset error drift
Gain Drift ¹		−4.5		+3	μV/°C		
Match			±1		LSB		
ADC DYNAMIC PERFORMANCE							
Signal-to-Noise Ratio	SNR					f _{IN} = 665.25 Hz sine wave, f _{SAMPLE} = 100 kSPS; input filter = 15 Ω, 2 nF Includes distortion and noise components	
Input Buffer							
Disabled			80		dB		
Enabled			74		dB		
Total Harmonic Distortion	THD						
Input Buffer							
Disabled			−86		dB		
Enabled			−83		dB		
Peak Harmonic or Spurious Noise			−88		dB		
Channel-to-Channel Crosstalk			−90		dB	Measured on adjacent channels	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUT						Input buffer not enabled
Input Voltage Ranges						
Single-Ended Mode ¹		AGND4		V _{REF}		
Differential Mode ¹		−V _{REF}		+V _{REF}	V	Voltage between differential pins
Compliance ¹		AGND4		AV _{DD4}		
Common Mode ¹		0.9		1.6	V	
Leakage Current						
AIN0 to AIN4, AIN6 to AIN15			±1.5		nA	
AIN5			±20		nA	Pin shared with comparator
Input Current			±9		μA/V	At 1 MSPS; buffer off
			±6		μA/V	≤800 kSPS; buffer off
			±4		μA/V	500 kSPS; buffer off; ADCCNVC[25:16] = 0x1E
Input Capacitance			20		pF	During ADC acquisition
ADC INPUT BUFFER ²						When enabled by software
Voltage Compliance ¹		0.15		2.5	V	Reduced accuracy below 0.15 V
Input Current			±100		nA	V _{IN} = 0.15 V to 2.5 V, ADC converting
ON-CHIP VOLTAGE REFERENCE			2.51		V	0.47 μF from VREF_1V2 to AGND4; reference is measured with all ADCs, VDACS, and IDACS enabled
Accuracy				±5	mV	T _A = 25°C
Reference Temperature Coefficient ¹		−34	−15	+4	ppm/°C	
Power Supply Rejection Ratio	PSRR		60		dB	
Internal V _{REF} Power-On Time			50		ms	
EXTERNAL REFERENCE INPUT						
Range ¹		1.8		2.5	V	ADC
Input Current			200		μA	
BUFFERED REFERENCE OUTPUT						
Output Voltage			2.504		V	
Accuracy			±8		mV	T _A = 25°C, load = 1.2 mA
Reference Temperature Coefficient ¹		−55	−5	+40	μV/°C	100 nF from BUF_VREF2V5 to AGND4
Output Impedance			10		Ω	T _A = 25°C
Load Current ¹				1.2	mA	
VDAC CHANNEL SPECIFICATIONS						R _L = 5 kΩ, C _L = 100 pF ³
DC Accuracy ¹		12			Bits	1 LSB = 2.5 V/2 ¹²
Resolution ¹		12			Bits	Number of data bits
Relative Accuracy ⁴	INL		±4		LSB	1 LSB = 2.5 V/2 ¹²
Differential Nonlinearity ⁴	DNL	−0.99		+1	LSB	Guaranteed monotonic, 1 LSB = 2.5 V/2 ¹²
Offset Error			±3	±15	mV	2.5 V internal reference, DAC Output Code 0
Drift			±13		μV/°C	
Gain Error ⁵			±0.3	±0.85	%	0 V to internal V _{REF} range
			±0.4	±1	%	0 V to AV _{DD} range
Drift			6.5		ppm/°C	Excluding reference drift
Mismatch			0.1		%	% of full scale on DAC0

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Analog Outputs						
Output Voltage Range 1 ¹		0.15		2.5	V	
Output Voltage Range 2 ¹		0.15		$AV_{DDx} - 0.15$	V	
Output Impedance			2		Ω	
DAC AC Characteristics						
Output Settling Time			10		μ s	Settled to ± 1 LSB
Glitch Energy			± 20		nV-sec	1 LSB change when the maximum number of bits changes simultaneously in the DACxDAT register
IDAC CHANNEL SPECIFICATIONS						
Resolution ¹		14			Bits	Combination of overlapping 11 bits and 5 bits
Full-Scale Output ¹			150		mA	
Supply Voltage Each Channel ¹		1.8		2.5	V	Separate PV_{DDx} supply for each channel
Output Compliance Range						
IDAC0, IDAC1		0.4		$PV_{DDx} - 0.4$	V	See Figure 11
IDAC2, IDAC3		0.4		$PV_{DDx} - 0.25$	V	See Figure 11
Full-Scale Error						IDAC set to 85% of full scale
IDAC0, IDAC1				± 0.75	%	25°C to 105°C range
				± 3.5	%	–40°C to +105°C range
IDAC2, IDAC3				± 0.75	%	–40°C to +105°C range
Full-Scale Error Drift						Internal V_{REF}
IDAC0, IDAC1			25		μ A/°C	
–40°C to +85°C			5		μ A/°C	
25°C to 85°C			2		μ A/°C	Internal V_{REF}
IDAC2, IDAC3						
Integral Nonlinearity	INL		± 3	± 6	LSB	1 LSB = 150 mA/2 ¹¹
Differential Nonlinearity	DNL	–0.99		+1.5	LSB	Guaranteed 11-bit monotonic, 1 LSB = 150 mA/2 ¹¹
Zero-Scale Error			± 50		μ A	
Zero-Scale Error Drift						
IDAC0, IDAC1			± 300		nA/°C	
IDAC2, IDAC3			± 800		nA/°C	
Noise Current			2		μ A	IDACxCON[5:2] = 0
Pull-Down Current		–220	–165	–100	μ A	When enabled
Settling Time						IDACxCON[5:2] = 0
To 0.1%			100		μ s	± 4 mA change from midscale
To 1%			50		μ s	± 4 mA change from midscale
Full Scale to 0 mA			20		μ s	Pull-down enabled
Overheat Shutdown			135		°C	Junction temperature
PVDD ACPSRR						IDACxCON[5:2] = 0
100 Hz			51		dB	
1 kHz			45		dB	
10 kHz			25		dB	
100 kHz			10		dB	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
COMPARATOR						
Input						
Offset Voltage			± 10		mV	
Bias Current			1		nA	
Voltage Range ¹		AGNDx		$AV_{DDx} - 1.2$	V	
Capacitance			7		pF	
Hysteresis ¹		8.5		15	mV	When enabled in software
Response Time			7		μ s	AFECOMP[2:1] = 0
TEMPERATURE SENSOR						
Resolution			0.5		°C	Indicates die temperature, see Figure 9
Accuracy ¹		1.34		1.43	V	When precision calibrated by the user ⁶ ADC measured voltage for temperature sensor channel without calibration, $T_A = 25^\circ\text{C}$
POWER-ON RESET	POR		2.85	2.9	V	
PIN RESET						
Minimum Time To Reset			1.2		μ s	
Maximum Time Not To Reset			0.5		μ s	
WATCHDOG TIMER	WDT					
Timeout Period			32		sec	Default at power-up
FLASH/EE MEMORY						
Endurance ¹		10,000			Cycles	
Data Retention ¹		20			Years	$T_J = 85^\circ\text{C}$
DIGITAL INPUTS						
Input Leakage Current						
Logic 1 GPIO			1		nA	$V_{IH} = IOV_{DD}$, pull-up resistor disabled
Logic 0 GPIO			10		nA	$V_{IL} = 0\text{V}$, pull-up resistor disabled
PRTADDRx, MCK			1		μ A	Pull-up disabled
Input Capacitance			16		μ A	Pull-up to 1.8V enabled
MCK, PRTADDRx			10		pF	
MDIO			6.5		pF	
XTALI			8.5		pF	
XTALO			5		pF	
All Other Pins			5		pF	
All Other Pins			10		pF	
LOGIC INPUTS						
GPIO Input Voltage						
Low	V_{INL}			$0.25 \times IOV_{DDx}$	V	
High	V_{INH}	$0.58 \times IOV_{DDx}$			V	
MDIO						
PRTADDRx Input Voltage						
Low	V_{INL}			0.36	V	
High	V_{INH}	0.84			V	
MCK, MDIO Input Voltage						
Low	V_{INL}			0.36	V	
High	V_{INH}	0.84			V	Setup time $\geq 10\text{ ns}$; hold time $\geq 10\text{ ns}$; MCK/MDIO

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
XTALI Input Voltage						
Low	V_{INL}		1.1		V	
High	V_{INH}		1.7		V	
Pull-Up Current		30		120	μ A	$V_{IN} = 0$ V, see Figure 10
Pull-Down Current		30		100	μ A	$V_{IN} = 3.3$ V, see Figure 10
LOGIC OUTPUTS						
GPIO Output Voltage ⁷						All digital outputs excluding XTALO
High	V_{OH}	$IOV_{DDx} - 0.4$			V	$I_{SOURCE} = 2$ mA
Low	V_{OL}			0.4	V	$I_{SINK} = 2$ mA
GPIO Short-Circuit Current ¹			11		mA	See Figure 13
MDIO						
Output Voltage						
High	V_{OH}	1.0			V	$I_{SOURCE} = 4$ mA
Low	V_{OL}			0.2	V	$I_{SINK} = 4$ mA
Delay Time				100	ns	MCK to MDIO out
OSCILLATORS						
Internal System Oscillator			16		MHz	
Accuracy			± 0.5	± 3	%	
System PLL			80		MHz	Main system clock
External Crystal Oscillator			16		MHz	Can be selected in place of internal oscillator
32 kHz Internal Oscillator			32.768		kHz	Use for watchdog
Accuracy			± 5	± 20	%	
External Clock		0.05		80	MHz	Can be selected in place of PLL
START-UP TIME						
At Power-On			40		ms	Processor clock = 80 MHz
After Other Reset			1.5		ms	POR to first user code execution
From All Power-Down Modes			1.25		μ s	Reset to first user code execution
PROGRAMMABLE LOGIC ARRAY						
Propagation Delay	PLA					
Pin			17		ns	From input pin to output pin
Element			1.5		ns	Per PLA cell
EXTERNAL INTERRUPTS						
Pulse Width ¹						
Level Triggered		7			ns	
Edge Triggered		1			ns	
POWER REQUIREMENTS ⁸						
Power Supply Voltage Range						
AVDDx to AGNDx and IOVDDx to DGNDx ¹		2.9	3.3	3.6	V	
Analog Power Supply Currents						
AVDDx Current			6.3		mA	Analog peripherals in idle mode
Digital Power Supply Current						
IOVDDx Current in Normal Mode			4		mA	All GPIO pull-up resistors enabled

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
VDDx Current						
Normal Mode			29		mA	CD = 0 (80 MHz clock) executing typical code
			20		mA	CD = 1 executing typical code
			10		mA	CD = 7 executing typical code
CORE_SLEEP Mode			16		mA	
SYS_SLEEP Mode			8		mA	
Hibernate Mode			6.6		mA	
Additional Power Supply Currents						
ADC			4.1		mA	Continuously converting at 100 kSPS
ADC Input Buffer			4.0		mA	Both buffers enabled
IDAC			16.5		mA	Excluding load current
DAC			340		μA	Per powered up DAC, excluding load current
Total Supply Current		35	40	45	mA	VDD1, IOVDDx, AVDDx connected together; condition when entering user code: peripheral clocks on, peripherals idle, no load currents
Thermal Performance						
Impedance, Junction to Ambient			45		°C/W	JEDEC 2S2P

¹ These numbers are not production tested but are guaranteed by design and/or characterization data at production release.

² Enabling the input buffer changes the ADC input characteristics as described in these specifications (the ADC Input Buffer specifications).

³ The data in the Microcontroller Electrical Specifications section also applies for a load of $R_L = 1 \text{ k}\Omega$ and $C_L = 100 \text{ pF}$ to ground but only for 0 V to 2.5 V. However, this is not production tested.

⁴ DAC linearity is calculated using a reduced code range of 100 to 3900.

⁵ DAC gain error is calculated using a reduced code range of 100 to an internal $2.5 \text{ V } V_{REF}$.

⁶ Due to self heating, internal temperature measurements cannot be used to predict external temperatures. This value is only relevant after user calibration and only for internal and external conditions identical to those at calibration.

⁷ The average current from all GPIO pins must not exceed 3 mA per pin.

⁸ Power specifications exclude any load currents to external circuits.

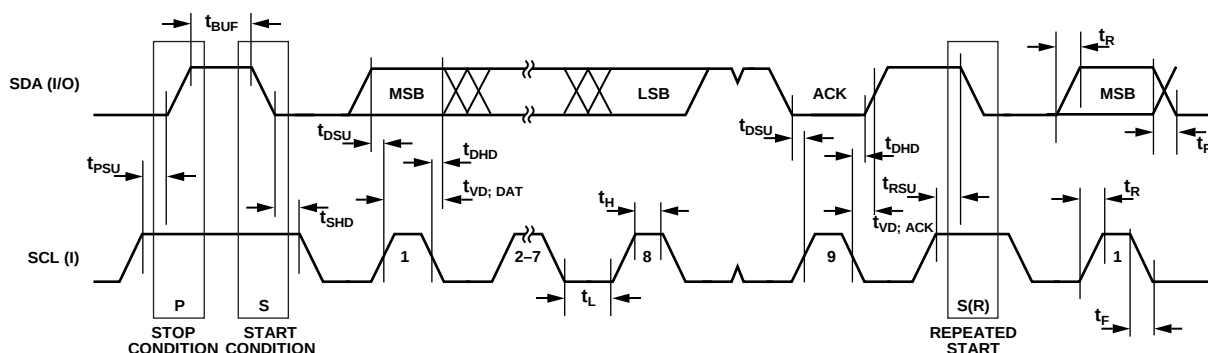
TIMING SPECIFICATIONS

*I²C Timing*Table 2. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Slave			Unit
		Min	Typ	Max	
t_L	SCL low pulse width	4.7			μ s
t_H	SCL high pulse width	4.0			ns
t_{SHD}	Start condition hold time	4.0			μ s
t_{DSU}	Data setup time	250			ns
t_{DHD}	Data hold time (SDA held internally for 300 ns after falling edge of SCL)	0		3.45	μ s
t_{RSU}	Setup time for repeated start	4.7			μ s
t_{PSU}	Stop condition setup time	4.0			μ s
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7			μ s
t_R	Rise time for both SCL and SDA			1	μ s
t_F	Fall time for both SCL and SDA		15	300	ns
$t_{VD; DAT}$	Data valid time			3.45	μ s
$t_{VD; ACK}$	Data valid acknowledge time			3.45	μ s

Table 3. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Slave			Unit
		Min	Typ	Max	
t_L	SCL low pulse width	1.3			μ s
t_H	SCL high pulse width	0.6			ns
t_{SHD}	Start condition hold time	0.6			μ s
t_{DSU}	Data setup time	100			ns
t_{DHD}	Data hold time (SDA held internally for 300 ns after falling edge of SCL)	0			μ s
t_{RSU}	Setup time for repeated start	0.6			μ s
t_{PSU}	Stop condition setup time	0.6			μ s
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			μ s
t_R	Rise time for both SCL and SDA	20		300	ns
t_F	Fall time for both SCL and SDA		15	300	ns
$t_{VD; DAT}$	Data valid time			0.9	μ s
$t_{VD; ACK}$	Data valid acknowledge time			0.9	μ s

Figure 2. I²C-Compatible Interface Timing

13422-002

SPI Timing**Table 4. SPI Master Mode Timing (Phase Mode = 1)**

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width		$(SPIDIV + 1) \times t_{HCLK}/2$		ns
t_{SH}	SCLK high pulse width		$(SPIDIV + 1) \times t_{HCLK}/2$		ns
t_{DAV}	Data output valid after SCLK edge	0	3		ns
t_{DSU}	Data input setup time before SCLK edge		$\frac{1}{2}$ SCLK		ns
t_{DHD}	Data input hold time after SCLK edge		SCLK		ns
t_{DF}	Data output fall time		SCLK		ns
t_{DR}	Data output rise time		25		ns
t_{SR}	SCLK rise time		25		ns
t_{SF}	SCLK fall time		20		ns

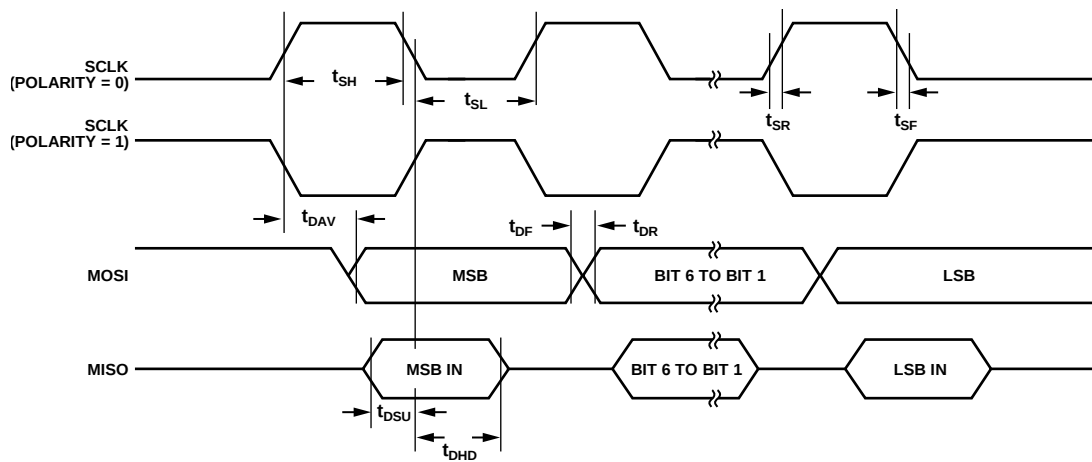


Figure 3. SPI Master Mode Timing (Phase Mode = 1)

13422-003

Table 5. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width		$(SPIDIV + 1) \times t_{HCLK}/2$		ns
t_{SH}	SCLK high pulse width		$(SPIDIV + 1) \times t_{HCLK}/2$		ns
t_{DAV}	Data output valid after SCLK edge	0	3		ns
t_{DOSU}	Data output setup before SCLK edge		$\frac{1}{2}$ SCLK		ns
t_{DSU}	Data input setup time before SCLK edge		SCLK		ns
t_{DHD}	Data input hold time after SCLK edge		SCLK		ns
t_{DF}	Data output fall time		25		ns
t_{DR}	Data output rise time		25		ns
t_{SR}	SCLK rise time		20		ns
t_{SF}	SCLK fall time		20		ns

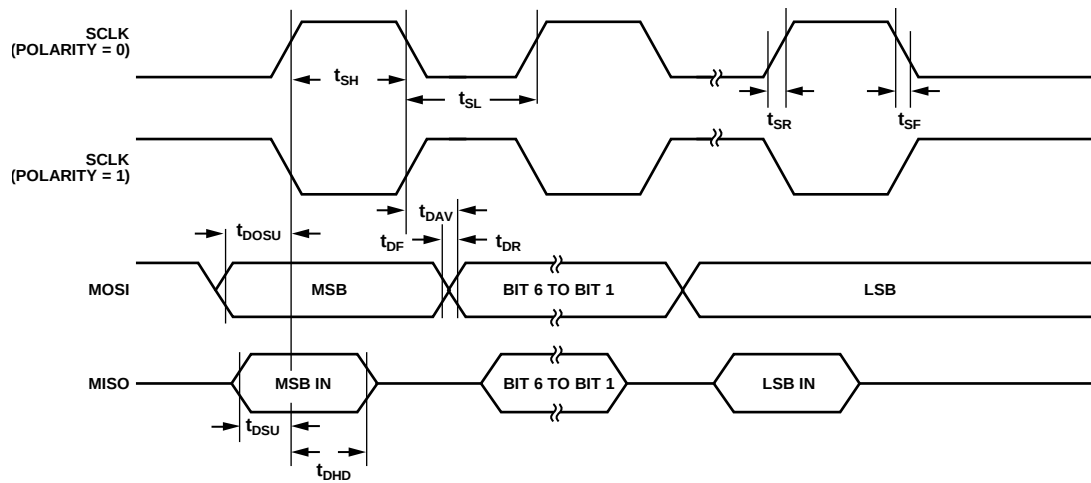


Figure 4. SPI Master Mode Timing (Phase Mode = 0)

13422-004

Table 6. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	10			ns
t_{SL}	SCLK low pulse width		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge		20		ns
t_{DSU}	Data input setup time before SCLK edge	10			ns
t_{DHD}	Data input hold time after SCLK edge	10			ns
t_{DF}	Data output fall time		25		ns
t_{DR}	Data output rise time		25		ns
t_{SR}	SCLK rise time	1			ns
t_{SF}	SCLK fall time	1			ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	20			ns

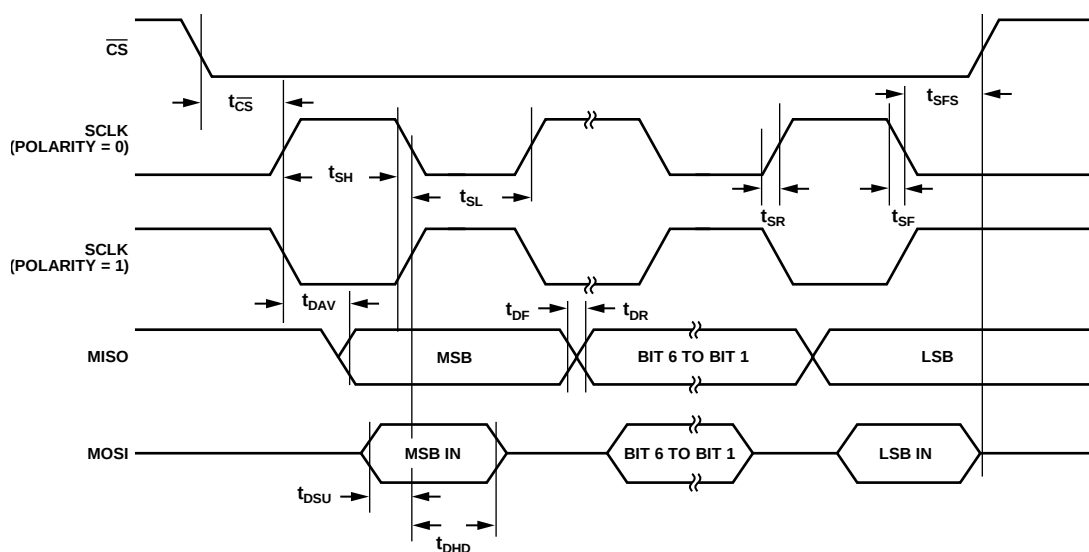


Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

13422-005

Table 7. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	10			ns
t_{SL}	SCLK low pulse width		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge		20		ns
t_{DSU}	Data input setup time before SCLK edge	10			ns
t_{DHD}	Data input hold time after SCLK edge	10			ns
t_{DF}	Data output fall time		25		ns
t_{DR}	Data output rise time		25		ns
t_{SR}	SCLK rise time	1			ns
t_{SF}	SCLK fall time	1			ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge	20			ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	10			ns

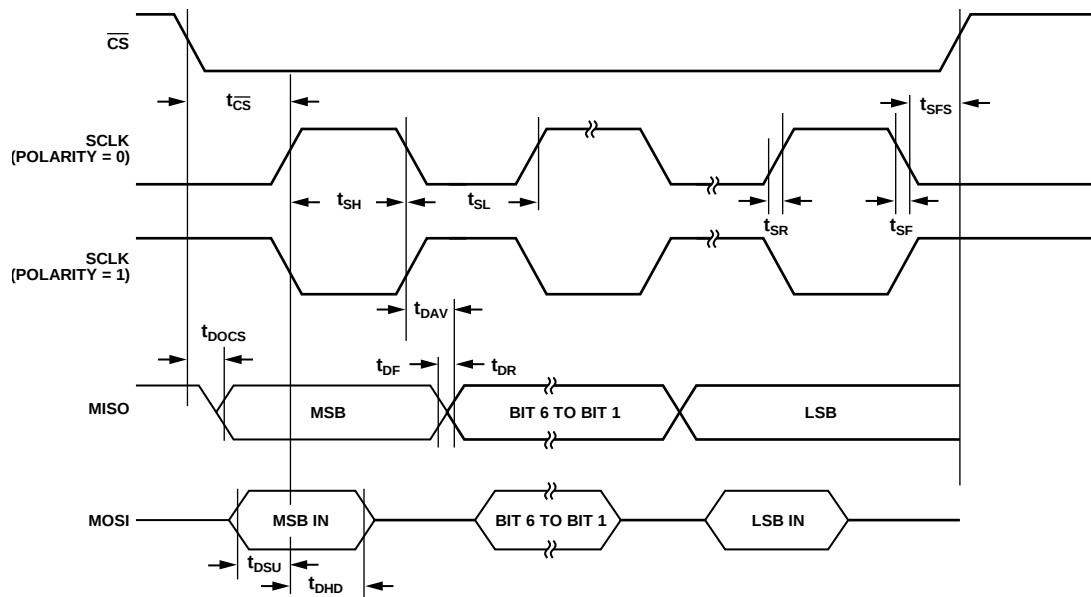


Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

13422-006

Table 8. MDIO vs MCK Timing

Parameter	Description	Min	Typ	Max	Unit
t _{SETUP}	MDIO setup before MCK edge	10			ns
t _{HOLD}	MDIO valid after MCK edge	10			ns
t _{DELAY}	Data output after MCK edge			100	ns

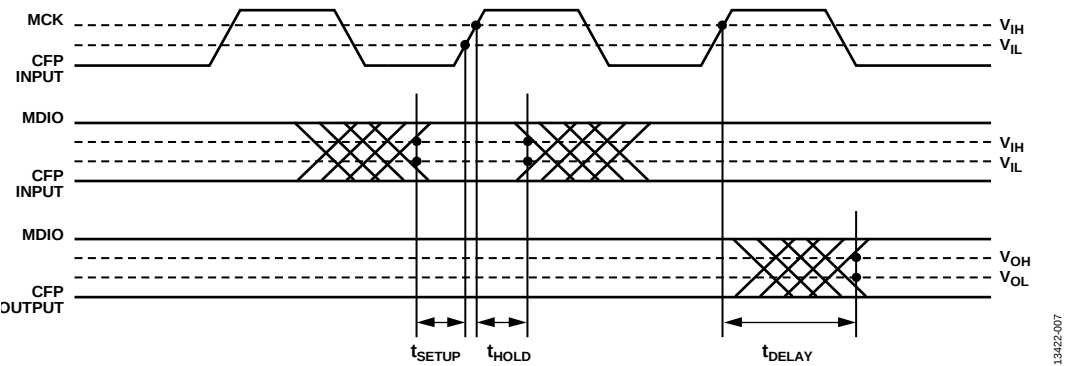


Figure 7. MDIO Timing

ABSOLUTE MAXIMUM RATINGS

All requirements applicable to each pin must be met. Where multiple limits apply to a pin each one must be met individually. The limits apply according to the functionality of the pins at the time. Pins that can be either analog or digital, that is, that have two types indicated in the pin descriptions, must meet the limits for both types. For pin types, see Table 10.

When powered up, all ground pins and ADC_REFN must be connected together to a node referred to as GND in Table 9. The limits that are listed must be reduced by any difference between any GNDx pin. Also, AVDD3 must be connected to AVDD4 and IOVDD1 must be connected to IOVDD3.

Table 9.

Parameter	Rating
Any Pin to GND	−0.3 V to +3.9 V
Any PVDDx Pin to GND	−0.3 V to +2.8 V
MDIO ¹ , MCK, and PRTADDR0 to PRTADDR4 in MDIO Mode to GND	−0.3 V to +2.1 V
Between Any of AVDDx, IOVDDx, and VDD1 Pins	−0.3 V to +0.3 V
Any Type I Pin to GND ²	−0.3 V to IOVDDx + 0.3 V
Any Type AI or AO Pin to GND ³	−0.3 V to AVDDx + 0.3 V
Any IDACx, CDAMPx, IDAC_TST, IREF to GND	−0.3 V to PVDDx + 0.3 V
ADC_REFP to GND	−0.3 V to AVDDx + 0.3 V
Total Positive GPIO Pin Currents	0 mA to 30 mA
Total Negative GPIO Pin Currents	−30 mA to 0 mA
Maximum Power Dissipation	1 W
Operating Ambient Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +160°C
Operating Junction Temperature Range	−40°C to +150°C
ESD HBM	4 kV
ESD FICDM	1 kV

¹ Note that this pin is always in MDIO mode.

² This limit does not apply if no current can be drawn by external circuits on IOVDDx because, in this case, IOVDD follows to a suitable level.

³ This limit does not apply if no current can be drawn by external circuits on AVDDx because, in this case, AVDD follows to a suitable level.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11
A	IDAC_TST	IDAC0	PVDD0	PVDD2	IDAC2	PGND	IDAC3	PVDD3	PVDD1	IDAC1	IREF
B	IOVDD1	RESET	P3.3/ PRTADDR3/ PLAI[15]	CDAMP0	CDAMP2	PGND	CDAMP3	CDAMP1	P1.0/SIN/ ECLKIN/ PLAI[4]	P1.1/SOUT/ PLACLK1/ PLAI[5]	P1.2/ PWM0/ PLAI[6]
C	IOGND1	P0.0/ SCLK0/ PLAI[0]	P2.3/BM	P2.2/ IRQ4/POR/ CLKOUT/ PLAI[10]	P2.0/IRQ2/ PWMTRIP/ PLACLK2/ PLAI[8]	P1.3/ PWM1/ PLAI[7]	P1.4/ PWM2/ SCLK1/ PLAO[10]	P1.5/ PWM3/ MISO1/ PLAO[11]	P1.6/ PWM4/ MOSI1/ PLAO[12]	P1.7/IRQ1/ PWM5/ CS1/ PLAO[13]	P3.4/ PRTADDR4/ PLAO[26]
D	P0.2/ MOSI0/ PLAI[2]	P0.1/ MISO0/ PLAI[1]	P3.2/ PRTADDR2/ PLAI[14]	ADuCM320i TOP VIEW (Not to Scale)					P2.4/IRQ5/ ADCCONV/ PWM6/ PLAO[18]	DGND2	IOVDD2
E	P0.5/ SDA0/ PLAO[3]	P0.4/ SCL0/ PLAO[2]	P0.3/ IRQ0/CS0/ PLACLK0/ PLAI[3]						SWCLK	SWDIO	IOGND2
F	P2.6/ IRQ7/ PLAO[20]	P0.7/ SDA1/ PLAO[5]	P0.6/ SCL1/ PLAO[4]						AVDD_ REG0	AVDD_ REG1	VREF_1V2
G	P2.7/ IRQ8/ PLAO[21]	P3.1/ PRTADDR1/ PLAI[13]	P3.0/ PRTADDR0/ PLAI[12]						AIN15/ P4.7	AIN13/ P4.5	AVDD4
H	P3.5/ MCK/ PLAO[27]	XTALO	MDIO						AIN14/ P4.6	AIN12/ P4.4	AGND4
J	IOVDD3	XTALI	VDAC7/ P5.2	VDAC4	AGND1	AIN0	AIN1	AIN2	AIN7	AIN10	AIN11/ BUF_ VREF2V5
K	IOGND3	DVDD_2V5	VDAC6/ P5.1	VDAC3/ P5.0	VDAC1	VDD1	AGND2	AIN3	AIN6	AIN9/ P4.3	ADC_ REFP
L	DGND1	DVDD_1V8	VDAC5	VDAC2/ P3.7/ PLAO[29]	VDAC0/ P5.3	AVDD3	AGND3	AIN4	AIN5	AIN8/ P4.2	ADC_ REFN

DIGITAL
 IDAC
 ANALOG

Figure 8. Pin Configuration

13422-008

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
B2	RESET	I	Reset Input (Active Low). An internal pull-up resistor is included.
C2	P0.0/SCLK0/PLAI[0]	I/O	Digital I/O Port 0.0 (P0.0). SPI0 Clock (SCLK0). Input to PLA Element 0 (PLAI[0]).
D2	P0.1/MISO0/PLAI[1]	I/O	Digital I/O Port 0.1 (P0.1). SPI0 Master Input, Slave Output (MISO0). Input to PLA Element 1 (PLAI[1]).
D1	P0.2/MOSI0/PLAI[2]	I/O	Digital I/O Port 0.2 (P0.2). SPI0 Master Output, Slave Input (MOSI0). Input to PLA Element 2 (PLAI[2]).
E3	P0.3/IRQ0/CS0/PLACLK0/PLAI[3]	I/O	Digital I/O Port 0.3 (P0.3). External Interrupt 0 (IRQ0). SPI0 Chip Select 0 (CS0). When using SPI0, configure this pin as CS0. PLA Clock 0 (PLACLK0). Input to PLA Element 3 (PLAI[3]).
E2	P0.4/SCL0/PLAO[2]	I/O	Digital I/O Port 0.4 (P0.4). I ² C0 Serial Clock (SCL0). Output of PLA Element 2 (PLAO[2]).

Pin No.	Mnemonic	Type ¹	Description
E1	P0.5/SDA0/PLAO[3]	I/O	Digital I/O Port 0.5 (P0.5). I ² C0 Serial Data (SDA0). Output of PLA Element 3 (PLAO[3]).
F3	P0.6/SCL1/PLAO[4]	I/O	Digital I/O Port 0.6 (P0.6). I ² C1 Serial Clock (SCL1). Output of PLA Element 4 (PLAO[4]).
F2	P0.7/SDA1/PLAO[5]	I/O	Digital I/O Port 0.7 (P0.7). I ² C1 Serial Data (SDA1). Output of PLA Element 5 (PLAO[5]).
B9	P1.0/SIN/ECLKIN/PLAI[4]	I/O	Digital I/O Port 1.0 (P1.0). UART Input (SIN). External Input Clock (ECLKIN). Input to PLA Element 4 (PLAI[4]).
B10	P1.1/SOUT/PLACK1/PLAI[5]	I/O	Digital I/O Port 1.1 (P1.1). UART Output (SOUT) PLA Clock 1 (PLACK1). Input to PLA Element 5 (PLAI[5]).
B11	P1.2/PWM0/PLAI[6]	I/O	Digital I/O Port 1.2 (P1.2). PWM Output 0 (PWM0). Input to PLA Element 6 (PLAI[6]).
C6	P1.3/PWM1/PLAI[7]	I/O	Digital I/O Port 1.3 (P1.3). PWM Output 1 (PWM1). Input to PLA Element 7 (PLAI[7]).
C7	P1.4/PWM2/SCLK1/PLAO[10]	I/O	Digital I/O Port 1.4 (P1.4). PWM Output 2 (PWM2). SPI1 Clock (SCLK1). Output of PLA Element 10 (PLAO[10]).
C8	P1.5/PWM3/MISO1/PLAO[11]	I/O	Digital I/O Port 1.5 (P1.5). PWM Output 3 (PWM3). SPI1 Master Input, Slave Output (MISO1). Output of PLA Element 11 (PLAO[11]).
C9	P1.6/PWM4/MOSI1/PLAO[12]	I/O	Digital I/O Port 1.6 (P1.6). PWM Output 4 (PWM4). SPI1 Master Output, Slave Input (MOSI1). Output of PLA Element 12 (PLAO[12]).
C10	P1.7/IRQ1/PWM5/CS1/PLAO[13]	I/O	Digital I/O Port 1.7 (P1.7). External Interrupt 1 (IRQ1). PWM Output 5 (PWM5). SPI1 Chip Select 1 (CS1). When using SPI1, configure this pin as CS1. Output of PLA Element 13 (PLAO[13]).
C5	P2.0/IRQ2/PWMTRIP/PLACK2/PLAI[8]	I/O	Digital I/O Port 2.0 (P2.0). External Interrupt 2 (IRQ2). PWM Trip (PWMTRIP). PLA Input Clock 2 (PLACK2). Input to PLA Element 8 (PLAI[8]).
C4	P2.2/IRQ4/ $\overline{\text{POR}}$ /CLKOUT/PLAI[10]	I/O	Digital I/O Port 2.2 (P2.2). External Interrupt 4 (IRQ4). Reset Output ($\overline{\text{POR}}$). Clock Output (CLKOUT). Input to PLA Element 10 (PLAI[10]).

Pin No.	Mnemonic	Type ¹	Description
C3	P2.3/BM	I/O	Digital I/O Port 2.3 (P2.3). Boot Mode (BM). This pin determines the start-up sequence after every reset. Pull-up is enabled at power-up.
D9	P2.4/IRQ5/ADCCONV/PWM6/PLAO[18]	I/O	Digital I/O Port 2.4 (P2.4). External Interrupt 5 (IRQ5). External Input to Start ADC Conversions (ADCCONV). PWM Output 6 (PWM6). Output of PLA Element 18 (PLAO[18]).
F1	P2.6/IRQ7/PLAO[20]	I/O	Digital I/O Port 2.6 (P2.6). External Interrupt 7 (IRQ7). Output of PLA Element 20 (PLAO[20]).
G1	P2.7/IRQ8/PLAO[21]	I/O	Digital I/O Port 2.7 (P2.7). External Interrupt 8 (IRQ8). Output of PLA Element 21 (PLAO[21]).
G3	P3.0/PRTADDR0/PLAI[12]	I/O	Digital I/O Port 3.0 (P3.0). MDIO Port Address Bit 0 (PRTADDR0). See the digital inputs parameter in Table 1 for details. Input to PLA Element 12 (PLAI[12]).
G2	P3.1/PRTADDR1/PLAI[13]	I/O	Digital I/O Port 3.1 (P3.1). MDIO Port Address Bit 1 (PRTADDR1). See the digital inputs parameter in Table 1 for details. Input to PLA Element 13 (PLAI[13]).
D3	P3.2/PRTADDR2/PLAI[14]	I/O	Digital I/O Port 3.2 (P3.2). MDIO Port Address Bit 2 (PRTADDR2). See the digital inputs parameter in Table 1 for details. Input to PLA Element 14 (PLAI[14]).
B3	P3.3/PRTADDR3/PLAI[15]	I/O	Digital I/O Port 3.3 (P3.3). MDIO Port Address Bit 3 (PRTADDR3). See the digital inputs parameter in Table 1 for details. Input of PLA Element 15 (PLAI[15]).
C11	P3.4/PRTADDR4/PLAO[26]	I/O	Digital I/O Port 3.4 (P3.4). MDIO Port Address Bit 4 (PRTADDR4). See the digital inputs parameter in Table 1 for details. Output of PLA Element 26 (PLAO[26]).
H1	P3.5/MCK/PLAO[27]	I/O	Digital I/O Port 3.5 (P3.5). MDIO Clock (MCK) See the digital inputs parameter in Table 1 for more details. Output of PLA Element 27 (PLAO[27]).
H3	MDIO	I/O	MDIO Data.
E9	SWCLK	I	Serial Wire Debug Clock.
E10	SWDIO	I/O	Serial Wire Bidirectional Data.
F11	VREF_1V2	S	1.2 V Reference. This pin cannot be used to source current externally. Connect VREF_1V2 to AGNDx via a 470 nF capacitor.
A11	IREF	AI	IDAC Reference Current. This pin generates the reference current for the IDACs and is set by an external resistor, R _{EXT} . Connect R _{EXT} from IREF to AGND4.
J6	AIN0	AI	Analog Input 0.
J7	AIN1	AI	Analog Input 1.
J8	AIN2	AI	Analog Input 2.
K8	AIN3	AI	Analog Input 3.
L8	AIN4	AI	Analog Input 4.
L9	AIN5	AI	Analog Input 5. AIN5 can be the negative input for the comparator.
K9	AIN6	AI	Analog Input 6. AIN6 is also the positive input for the comparator.
J9	AIN7	AI	Analog Input 7.

Pin No.	Mnemonic	Type ¹	Description
L10	AIN8/P4.2	AI/I/O	Analog Input 8 (AIN8). Digital I/O Port 4.2 (P4.2).
K10	AIN9/P4.3	AI/I/O	Analog Input 9 (AIN9). Digital I/O Port 4.3 (P4.3).
J10	AIN10	AI	Analog Input 10.
J11	AIN11/BUF_VREF2V5	AI/AO	Analog Input 11 (AIN11). Buffered 2.5 V Bias (BUF_VREF2V5). The maximum load is 1.2 mA. Connect BUF_VREF2V5 to AGNDx via a 100 nF capacitor.
H10	AIN12/P4.4	AI/I/O	Analog Input 12 (AIN12). Digital I/O Port 4.4 (P4.4).
G10	AIN13/P4.5	AI/I/O	Analog Input 13 (AIN13). Digital I/O Port 4.5 (P4.5).
H9	AIN14/P4.6	AI/I/O	Analog Input 14 (AIN14). Digital I/O Port 4.6 (P4.6).
G9	AIN15/P4.7	AI/I/O	Analog Input 15 (AIN15). Digital I/O Port 4.7 (P4.7).
L5	VDAC0/P5.3	AO/I/O	Voltage DAC0 Output (VDAC0). Digital I/O Port 5.3 (P5.3).
K5	VDAC1	AO	Voltage DAC1 Output.
L4	VDAC2/P3.7/PLAO[29]	AO/I/O	Voltage DAC2 Output (VDAC2). Digital I/O Port 3.7 (P3.7). Output of PLA Element 29 (PLAO[29]).
K4	VDAC3/P5.0	AO/I/O	Voltage DAC3 Output (VDAC3). Digital I/O Port 5.0 (P5.0).
J4	VDAC4	AO	Voltage DAC4 Output (VDAC4).
L3	VDAC5	AO	Voltage DAC5 Output (VDAC5).
K3	VDAC6/P5.1	AO/I/O	Voltage DAC6 Output (VDAC6). Digital I/O Port 5.1 (P5.1).
J3	VDAC7/P5.2	AO/I/O	Voltage DAC7 Output (VDAC7). Digital I/O Port 5.2 (P5.2).
A2	IDAC0	AO	IDAC0. 0 mA to 150 mA full-scale output.
A3	PVDD0	S	Power for IDAC0.
B4	CDAMP0	AI	Damping Capacitor 0. Connect a damping capacitor from this pin to PVDD0.
A10	IDAC1	AO	IDAC1. 0 mA to 150 mA full-scale output.
A9	PVDD1	S	Power for IDAC1.
B8	CDAMP1	AI	Damping Capacitor 1. Connect a damping capacitor from this pin to PVDD1.
A5	IDAC2	AO	IDAC2. 0 mA to 150 mA full-scale output.
A4	PVDD2	S	Power for IDAC2.
B5	CDAMP2	AI	Damping Capacitor 2. Connect a damping capacitor from this pin to PVDD2.
A7	IDAC3	AO	IDAC3. 0 mA to 150 mA full-scale output.
A8	PVDD3	S	Power for IDAC3.
B7	CDAMP3	AI	Damping Capacitor 3. Connect a damping capacitor from this pin to PVDD3.
B6	PGND	S	Power Supply Ground for IDACs.
A6	PGND	S	Power Supply Ground for IDACs.
A1	IDAC_TST	AI/AO	Pin for IDAC Test Purposes. Leave IDAC_TST unconnected.
L2	DVDD_1V8	AO	1.8 V Digital Supply. A 470 nF capacitor to DGND1 must be connected to this pin to stabilize the internal 1.8 V regulator that supplies flash memory and the Arm Cortex-M3 processor.
K2	DVDD_2V5	AO	2.5 V Digital Supply. A 470 nF capacitor to IOGND3 must be connected to this pin to stabilize the internal 2.5 V regulator that supplies the analog digital control.

Pin No.	Mnemonic	Type ¹	Description
F9	AVDD_REG0	AO	Analog Regulator 0 Supply. A 470 nF capacitor to AGND4 must be connected to this pin to stabilize the internal 2.5 V regulator that supplies the ADC.
F10	AVDD_REG1	AO	Analog Regulator 1 Supply. Output of 2.5 V on-chip LDO regulator. A 470 nF capacitor to AGND4 must be connected to this pin. This regulator supplies the IDACs.
L1	DGND1	S	Digital Ground 1 for DVDD_1V8.
D10	DGND2	S	Digital Ground 2. Connect to DGND1.
B1	IOVDD1	S	3.3 V GPIO Supply.
D11	IOVDD2	S	3.3 V GPIO Supply and Interdie Communications.
J1	IOVDD3	S	3.3 V GPIO Supply.
C1	IOGND1	S	Ground for IOVDD1.
E11	IOGND2	S	Ground for IOVDD2.
K1	IOGND3	S	Ground for IOVDD3 and Interdie Communications.
J5	AGND1	S	Analog Ground for VDD1.
K7	AGND2	S	ESD Ground for Pad Ring.
L7	AGND3	S	Ground for AVDD3.
H11	AGND4	S	Ground for AVDD4, AVDD_REG0, and AVDD_REG1.
K6	VDD1	S	3.3 V Supply for Digital Die.
L6	AVDD3	S	VDAC and IDAC Supply (3.3 V).
G11	AVDD4	S	ADC Supply (3.3 V).
L11	ADC_REFN	AO/A	Negative Decoupling Capacitor Connection for ADC Reference Buffer. Connect this pin to AGND4.
K11	ADC_REFP	AO/A	Positive Decoupling Capacitor Connection for ADC Reference Buffer. Connect this pin to a 4.7 μ F capacitor to the ADC_REFN pin. ADC_REFP can be overdriven by an external reference.
H2	XTALO	O	Output from the Crystal Oscillator Inverter. When not using an external crystal, leave XTALO unconnected.
J2	XTALI	I	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. When not using an external crystal, connect XTALI to DGNDx.

¹ I is digital input, O is digital output, S is supply, AI is analog input, and AO is analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

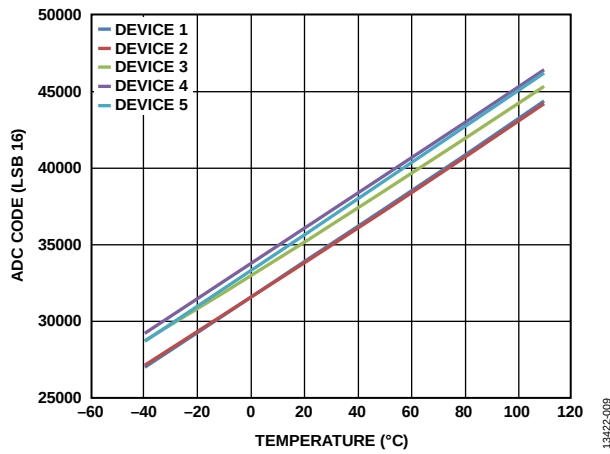


Figure 9. Typical Temperature Measurement (ADC Code) vs. Internal Temperature ($V_{DD} = 3.3\text{ V}$, 50 kSPS)

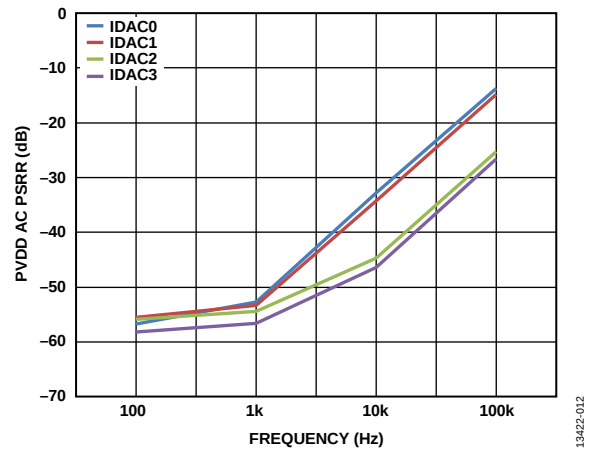


Figure 12. Typical PVDD AC PSRR vs. Frequency

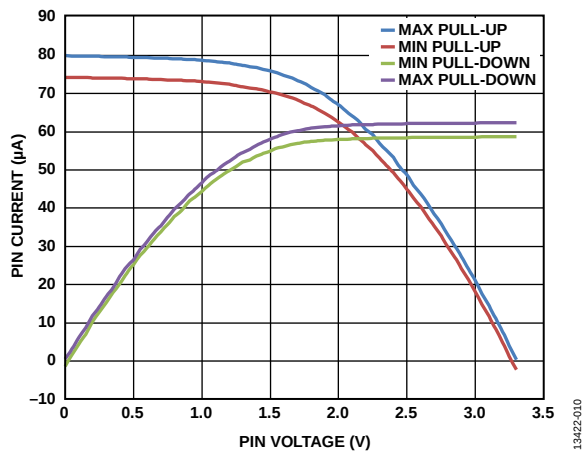


Figure 10. Typical Pull-Up/Pull-Down Pin Current vs. Pin Voltage ($V_{DD} = 3.3\text{ V}$, 25°C)

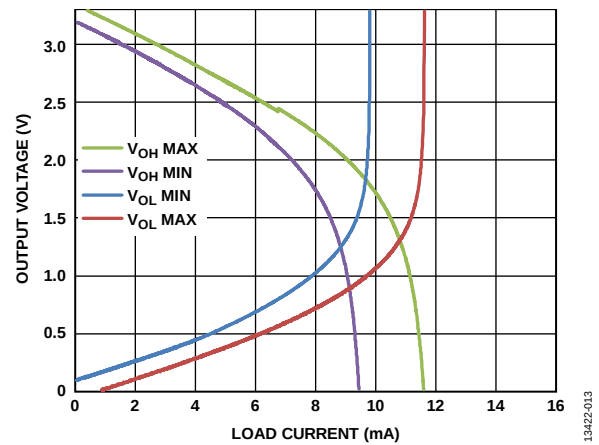


Figure 13. Typical Output Voltage vs. Load Current

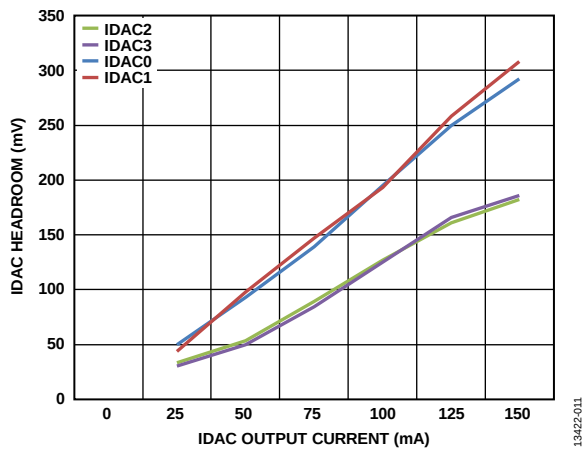


Figure 11. Typical IDAC Headroom vs. IDAC Output Current

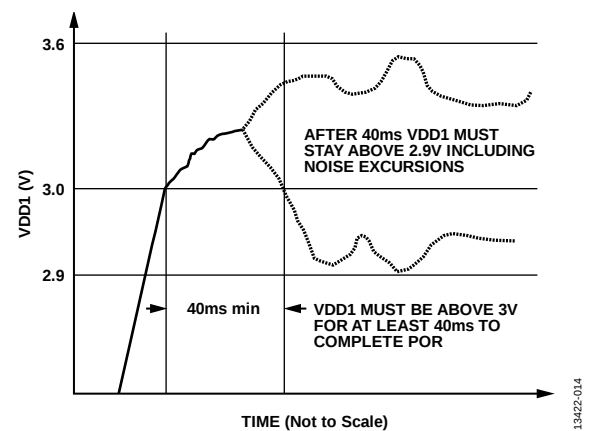


Figure 14. VDD1 Power-On Requirements

APPLICATIONS INFORMATION

RECOMMENDED CIRCUIT AND COMPONENT VALUES

Figure 15 shows a typical connection diagram for the [ADuCM320i](#).

Supplies and regulators must be adequately decoupled with capacitors connected between the AVDDx, PVDDx, DVDD_x, AVDD_REGx, IOVDDx, and VDD1 balls and their associated GND balls (AGNDx, PGND, IOGNDx, and DGNDx). Table 10 indicates which ground balls are paired with which supply balls.

There are four digital supply balls, IOVDD1, IOVDD2, IOVDD3, and VDD1. Decouple these balls with a 100 nF capacitor placed as near as possible to each of the four balls and their associated GND balls (IOGNDx and AGND1, respectively). In addition, place a 10 μ F capacitor conveniently near to these balls.

Similarly, the analog supply pins, AVDD3 and AVDD4, each require a 100 nF capacitor placed as near as possible to each ball and its associated AGNDx ball, and place a 10 μ F capacitor conveniently near to these balls.

The IDACs source their output currents from the PVDDx supply balls. Each PVDDx supply ball must have a 100 nF

capacitor near to each ball and their associated GND balls (PGND). In addition, place at least one 10 μ F capacitor at the source of the PVDDx supply.

The IDAC output filters depend on a 10 nF capacitor being placed between the CDAMPx and PVDDx pins.

The ADC reference requires a 4.7 μ F capacitor placed between ADC_REFP and ADC_REFN and located as near as possible to each ball. ADC_REFN must be connected directly to AGND4.

The [ADuCM320i](#) contains four internal regulators. These regulators require external decoupling capacitors. The DVDD_1V8 and DVDD_2V5 balls each require a 470 nF capacitor to DGND1 and IOGND3, respectively. AVDD_REG0 and AVDD_REG1 each require a decoupling capacitor to AGND4.

To generate an accurate and low drift reference current, connect the IREF ball to AGND4 via a low ppm 3.16 k Ω resistor.

Take care in the layout to ensure that currents flowing from the ground end of each decoupling capacitor to its associated ground ball share as little track as possible with other ground currents on the printed circuit board.

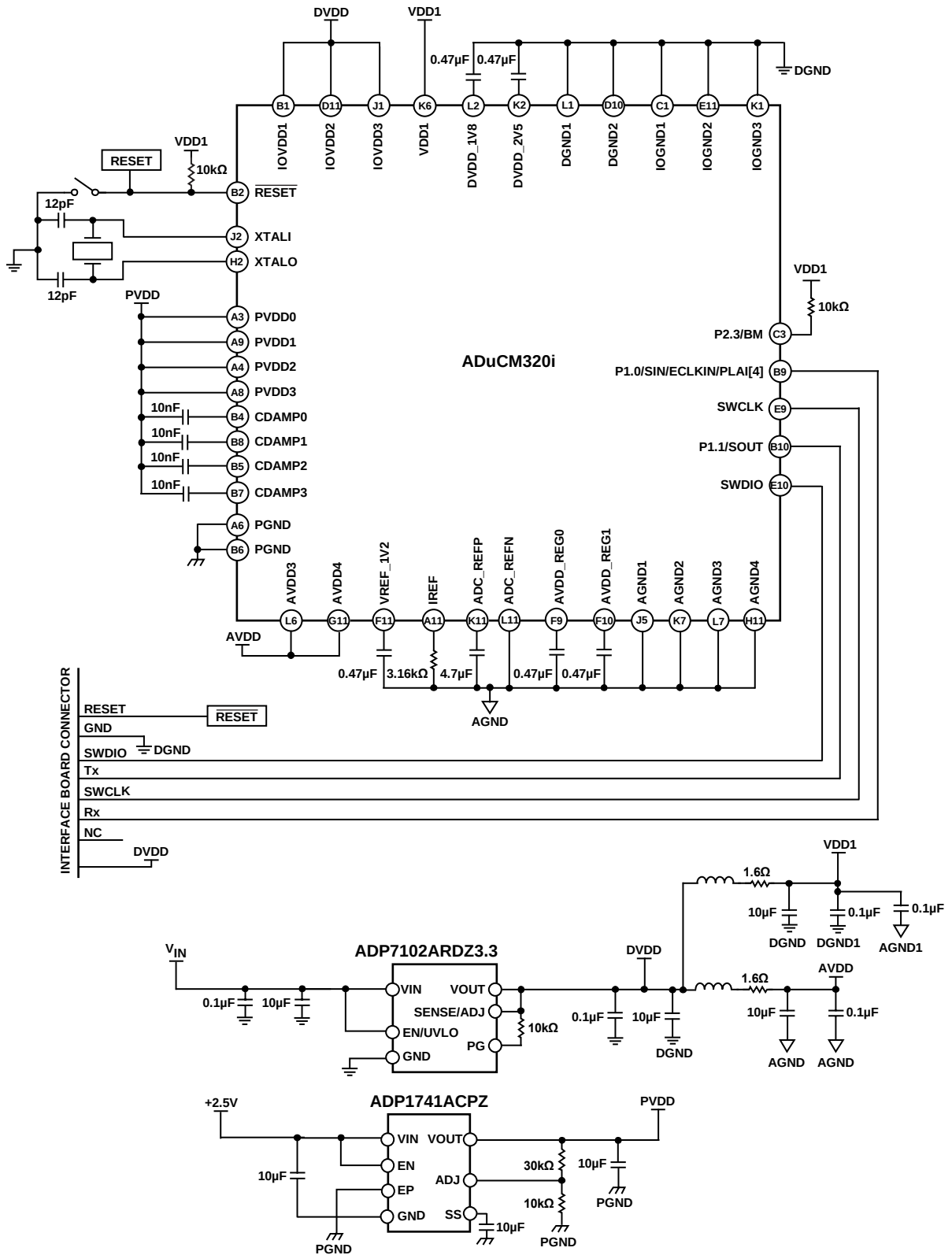
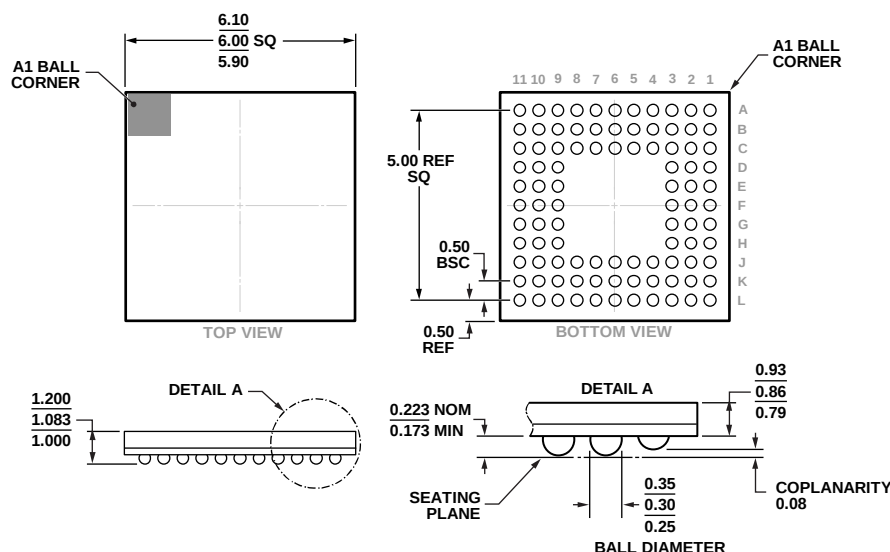


Figure 15. Recommended Circuit and Component Values

13422-015

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-195-AC
WITH THE EXCEPTION TO BALL COUNT.

Figure 16. 96-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-96-2)

Dimensions shown in millimeters

04-02-2013-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity
ADUCM320BBCZI	–40°C to +105°C	96-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-96-2	429
ADUCM320BBCZI-RL	–40°C to +105°C	96-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-96-2	2,500
EVAL-ADUCM320IQSPZ		Evaluation Board with QuickStart Development System		1

¹ Z = RoHS Compliant Part.

¹²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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