

Silicon Digital Attenuator, 2-Bit, 1 MHz to 30 GHz

**FEATURES**

- ▶ Ultrawideband frequency range: 1 MHz to 30 GHz
- ▶ Attenuation range: 16 dB typical steps to 48 dB
- ▶ Low insertion loss
  - ▶ 1.5 dB to 8 GHz
  - ▶ 2.0 dB to 18 GHz
  - ▶ 2.8 dB to 30 GHz
- ▶ Attenuation accuracy
  - ▶  $\pm(0.20 + 2.3\%$  of attenuation state) dB typical up to 8 GHz
  - ▶  $\pm(0.30 + 3.2\%$  of attenuation state) dB typical up to 18 GHz
  - ▶  $\pm(0.30 + 6.5\%$  of attenuation state) dB typical up to 30 GHz
- ▶ Typical step error
  - ▶  $\pm 0.8$  dB typical up to 8 GHz
  - ▶  $\pm 1.3$  dB typical up to 18 GHz
  - ▶  $\pm 3.3$  dB typical up to 30 GHz
- ▶ High input linearity
  - ▶ P0.1dB insertion loss state: 30 dBm typical
  - ▶ P0.1dB other attenuation states: 30 dBm typical
  - ▶ IP3 insertion loss state: 51 dBm typical
  - ▶ IP3 other attenuation state: 49 dBm typical
- ▶ High RF power handling
  - ▶ Input at ATTIN and ATTOUT
    - ▶ 30 dBm typical steady state average
    - ▶ 33 dBm typical steady state peak
- ▶ RF amplitude settling time (0.1 dB of final RF<sub>OUT</sub>): 6.6  $\mu$ s typical
- ▶ Single-supply operation supported
- ▶ Tight distribution in relative phase
- ▶ No low frequency spurious signals
- ▶ Parallel mode control, CMOS/LVTTL-compatible
- ▶ 20-terminal, 3 mm x 3 mm, land grid array [LGA] package

**APPLICATIONS**

- ▶ Industrial scanners
- ▶ Test and instrumentation
- ▶ Cellular infrastructure: 5G millimeter wave
- ▶ Military radios, radars, and electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

**FUNCTIONAL BLOCK DIAGRAM**

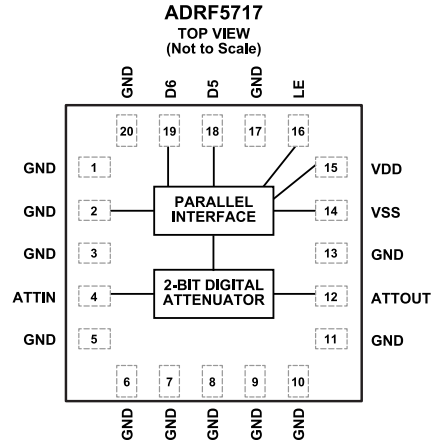


Figure 1. Functional Block Diagram

**GENERAL DESCRIPTION**

The ADRF5717 is a silicon, 2-bit digital attenuator with 48 dB attenuation range in 16 dB steps supporting glitch-free operation.

The ADRF5717 operates from 1 MHz to 30 GHz with better than 2.8 dB of insertion loss and better than 3.3 dB attenuation accuracy. The ATTIN and ATTOUT port of the ADRF5717 have an RF power handling capability of a 30 dBm steady state average and a 33 dBm steady state peak.

The ADRF5717 requires a dual-supply voltage of +3.3 V and -3.3 V. The device features parallel mode control and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5717 can also operate with a single positive supply voltage (V<sub>DD</sub>) applied while the negative supply voltage (V<sub>SS</sub>) is tied to ground. See the [Theory of Operation](#) section for more details.

The ADRF5717 RF ports are designed to match a characteristic impedance of 50  $\Omega$ . The ADRF5717 comes in a [20-terminal, 3 mm x 3 mm, RoHS compliant, LGA package](#) and operates from -40°C to +105°C.

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**REVISION HISTORY****5/2024—Rev. 0 to Rev. A**

Changes to Input at ATTIN or ATTOUT Parameter, Table 1.....	3
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**12/2023—Revision 0: Initial Version**

## SPECIFICATIONS

Positive supply voltage ( $V_{DD}$ ) = +3.3 V, negative supply voltage ( $V_{SS}$ ) = -3.3 V, control voltages ( $V_{CTRL}$ ) = 0 V or  $V_{DD}$ , and case temperature ( $T_{CASE}$ ) = 25°C with a 50  $\Omega$  system, unless otherwise noted.  $V_{CTRL}$  refers to the control voltages on the LE, D5, and D6 pins.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
FREQUENCY RANGE	f		1		30,000	MHz	
INSERTION LOSS		100 MHz to 8 GHz		1.5		dB	
		8 GHz to 18 GHz		2.0		dB	
		18 GHz to 30 GHz		2.8		dB	
RETURN LOSS		ATTIN and ATTOUT, attenuation state					
		100 MHz to 8 GHz		18		dB	
		8 GHz to 18 GHz		20		dB	
		18 GHz to 30 GHz		20		dB	
ATTENUATION	Range	Between minimum and maximum attenuation states		48		dB	
	Step Size	Between any successive attenuation states		16		dB	
	Accuracy		Referenced to insertion loss				
			100 MHz to 8 GHz		$\pm(0.20 + 2.3\% \text{ of state})$		dB
			8 GHz to 18 GHz		$\pm(0.30 + 3.2\% \text{ of state})$		dB
			18 GHz to 30 GHz		$\pm(0.30 + 6.5\% \text{ of state})$		dB
	Step Error	Between any successive attenuation states					
		100 MHz to 8 GHz		$\pm 0.8$		dB	
		8 GHz to 18 GHz		$\pm 1.3$		dB	
		18 GHz to 30 GHz		$\pm 3.3$		dB	
RELATIVE PHASE		Referenced to insertion loss					
		100 MHz to 8 GHz		35		Degrees	
		8 GHz to 18 GHz		81		Degrees	
		18 GHz to 30 GHz		175		Degrees	
SWITCHING	Rise Time and Fall Time	$t_{RISE}, t_{FALL}$	All attenuation states at input power ( $P_{IN}$ ) = 10 dBm		2	$\mu s$	
	On Time and Off Time	$t_{ON}, t_{OFF}$	10% to 90% of RF output ( $RF_{OUT}$ )		4	$\mu s$	
	RF Amplitude Settling Time		50% triggered control to 90% of $RF_{OUT}$				
		0.1 dB	50% triggered control to 0.1 dB of final $RF_{OUT}$		6.6		$\mu s$
	0.05 dB	50% triggered control to 0.05 dB of final $RF_{OUT}$		8.5		$\mu s$	
	RF Phase Settling Time		f = 1 GHz				
		5°	50% triggered control to 5° of final $RF_{OUT}$		44		$\mu s$
1°	50% triggered control to 1° of final $RF_{OUT}$		45		$\mu s$		
INPUT LINEARITY <sup>1</sup>	0.1 dB Power Compression	P0.1dB	100 MHz to 30 GHz				
	Insertion Loss State				30	dBm	
	Other Attenuation States				30	dBm	
	Third-Order Intercept	IP3	Two-tone $P_{IN}$ = 20 dBm per tone, $\Delta f$ = 1 MHz, all attenuation states				
	Insertion Loss State				51	dBm	
Other Attenuation States				49	dBm		

## SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DIGITAL CONTROL INPUTS</b>						
LE, D5, and D6						
Voltage						
Low	$V_{INL}$		0		0.8	V
High	$V_{INH}$		1.2		3.3	V
Current						
Low	$I_{INL}$			-33		$\mu$ A
High	$I_{INH}$			<1		$\mu$ A
<b>SUPPLY CURRENT</b>						
VDD and VSS						
Positive Supply Current						
LE, D5, and D6 = 0 V				230		$\mu$ A
LE, D5, and D6 = 3.3 V <sup>2</sup>				130		$\mu$ A
Negative Supply Current				500		$\mu$ A
<b>RECOMMENDED OPERATING CONDITIONS</b>						
Supply Voltage						
Positive	$V_{DD}$		3.15		3.45	V
Negative	$V_{SS}$		-3.45		-3.15	V
Digital Control Voltage			0		$V_{DD}$	V
RF Power Handling <sup>3</sup>		$f = 100 \text{ MHz to } 30 \text{ GHz}, T_{CASE} = 85^\circ\text{C}^4$				
Input at ATTIN or ATTOUT					30	dBm
					33	dBm
					27	dBm
					30	dBm
Case Temperature	$T_{CASE}$		-40		+105	$^\circ\text{C}$

<sup>1</sup> Input linearity performance degrades over frequency, see Figure 16 to Figure 19.

<sup>2</sup> If LE, D5, and D6 are in a different combination of states, the positive supply current is between 130  $\mu$ A and 230  $\mu$ A.

<sup>3</sup> For power derating over frequency, see Figure 3 and Figure 2. Applicable for all ATTIN and ATTOUT power specifications.

<sup>4</sup> For 105 $^\circ\text{C}$  operation, the power handling degrades from the  $T_{CASE} = 85^\circ\text{C}$  specifications by 3 dB.

## SPECIFICATIONS

## SINGLE-SUPPLY OPERATION

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted.

The small signal and bias characteristics are maintained for the single-supply operation.

**Table 2. Single-Supply Operation Specifications**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f	1		30,000	MHz
SWITCHING	All attenuation states at $P_{IN} = 10\text{ dBm}$				
Rise Time and Fall Time	$t_{RISE}$ , $t_{FALL}$ 10% to 90% of $RF_{OUT}$		8.6		$\mu\text{s}$
On Time and Off Time	$t_{ON}$ , $t_{OFF}$ 50% triggered control to 90% of $RF_{OUT}$		8.9		$\mu\text{s}$
RF Amplitude Settling Time 0.1 dB	50% triggered control to 0.1 dB of final $RF_{OUT}$		23		$\mu\text{s}$
RF Phase Settling Time 5°	f = 1 GHz 50% triggered control to 5° of final RF output		70		ns
1°	50% triggered control to 1° of final RF output		75		ns
INPUT LINEARITY	100 MHz to 30 GHz				
0.1 dB Power Compression	P0.1dB		21		dBm
Insertion Loss State			21		dBm
Other Attenuation States					
Third-Order Intercept	IP3 Two-tone $P_{IN} = 20\text{ dBm}$ per tone, $\Delta f = 1\text{ MHz}$ , all attenuation states				
Insertion Loss State			36		dBm
Other Attenuation States			34		dBm
RECOMMENDED OPERATING CONDITIONS					
RF Power Handling	f = 100 MHz to 30 GHz, $T_{CASE} = 85^\circ\text{C}$				
Input at ATTIN and ATTOUT	Average			18	dBm
	Peak			18	dBm
	Hot switching average			18	dBm
	Hot switching peak			18	dBm
Case Temperature	$T_{CASE}$	-40		+105	$^\circ\text{C}$

**ABSOLUTE MAXIMUM RATINGS**

For recommended operating conditions, see [Table 1](#) and [Table 2](#).

**Table 3. Absolute Maximum Ratings**

Parameter	Rating
V <sub>DD</sub>	-0.3 V to +3.6 V
V <sub>SS</sub>	-3.6 V to +0.3 V
Digital Control Input	
Voltage	-0.3 V to V <sub>DD</sub> + 0.3 V
Current	3 mA
RF Input Power <sup>1</sup>	
Dual Supply (V <sub>DD</sub> = +3.3 V, V <sub>SS</sub> = -3.3 V, f = 100 MHz to 30 GHz, T <sub>CASE</sub> = 85°C <sup>2</sup> )	
Average	31 dBm
Peak	34 dBm
Hot Switching Average	28 dBm
Hot Switching Peak	31 dBm
Single Supply (V <sub>DD</sub> = 3.3 V, V <sub>SS</sub> = 0 V, f = 100 MHz to 30 GHz, T <sub>CASE</sub> = 85°C)	
Average	19 dBm
Peak	19 dBm
Hot Switching Average	19 dBm
Hot Switching Peak	19 dBm
Under Unbiased Condition (V <sub>DD</sub> and V <sub>SS</sub> = 0 V)	14 dBm
Temperature	
Junction (T <sub>J</sub> )	135°C
Storage Range	-65°C to +150°C
Reflow	260°C

<sup>1</sup> For power derating over frequency, see [Figure 2](#) and [Figure 3](#). Applicable for all ATTIN and ATTOUT power specifications.

<sup>2</sup> For 105°C operation, the power handling degrades from the T<sub>CASE</sub> = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**THERMAL RESISTANCE**

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

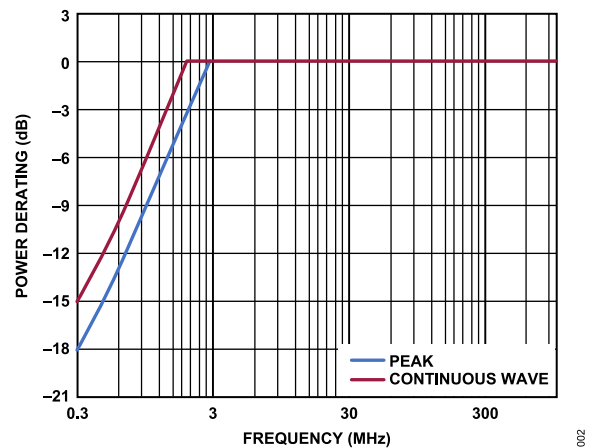
θ<sub>JC</sub> is the junction to case bottom (channel to package bottom) thermal resistance.

**Table 4. Thermal Resistance**

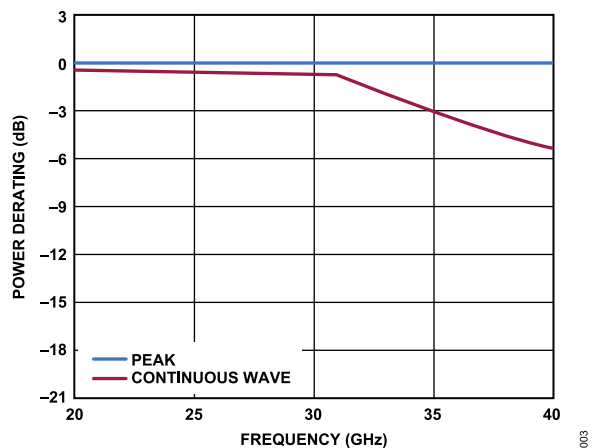
Package Type	θ <sub>JC</sub> <sup>1</sup>	Unit
CC-20-9	50	°C/W

<sup>1</sup> θ<sub>JC</sub> was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

**POWER DERATING CURVES**



**Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T<sub>CASE</sub> = 85°C**



**Figure 3. Power Derating vs. Frequency, High Frequency Detail, T<sub>CASE</sub> = 85°C**

**ABSOLUTE MAXIMUM RATINGS****ELECTROSTATIC DISCHARGE (ESD) RATINGS**

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

**ESD Ratings for ADRF5717**

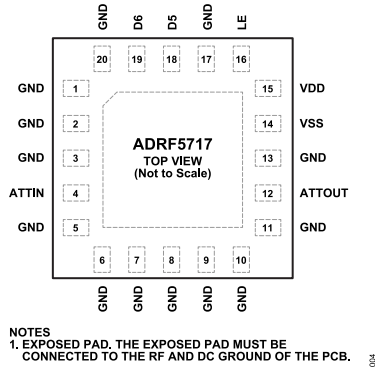
*Table 5. ADRF5717, 20-Terminal LGA*

ESD Model	Withstand Threshold (V)	Class
HBM		
ATTIN and ATTOUT Pins	1000	1C
Supply and Control Pins	2000	2
CDM	500	C2A

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**



**Figure 4. Pin Configuration (Top View)**

**Table 6. Pin Function Descriptions**

Pin No.	Mnemonic	Description
1 to 3, 5 to 11, 13, 17, 20	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
4	ATTIN	Attenuator Input. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See <a href="#">Figure 5</a> for the interface schematic.
12	ATTOUT	Attenuator Output. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See <a href="#">Figure 5</a> for the interface schematic.
14	VSS	Negative Supply Input. See <a href="#">Figure 8</a> for the interface schematic.
15	VDD	Positive Supply Input. See <a href="#">Figure 7</a> for the interface schematic.
16	LE	Latch Enable Input. See the <a href="#">Theory of Operation</a> section for more information. See <a href="#">Figure 6</a> for the interface schematic.
18	D5	Parallel Control Input for 16 dB Attenuation Bit. See the <a href="#">Theory of Operation</a> section for more information. See <a href="#">Figure 6</a> for the interface schematic.
19	D6	Parallel Control Input for 16 dB Attenuation Bit. See the <a href="#">Theory of Operation</a> section for more information. See <a href="#">Figure 6</a> for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

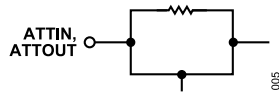


Figure 5. ATTIN and ATTOUT Interface Schematic

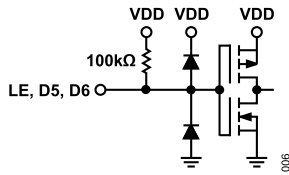


Figure 6. LE, D5, and D6 Interface Schematic

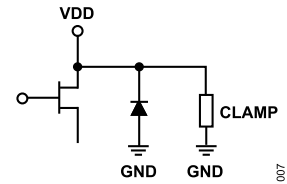


Figure 7. VDD Interface Schematic

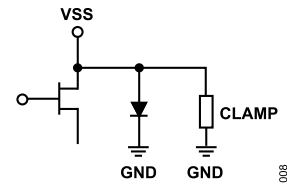


Figure 8. VSS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

$V_{DD} = +3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted.

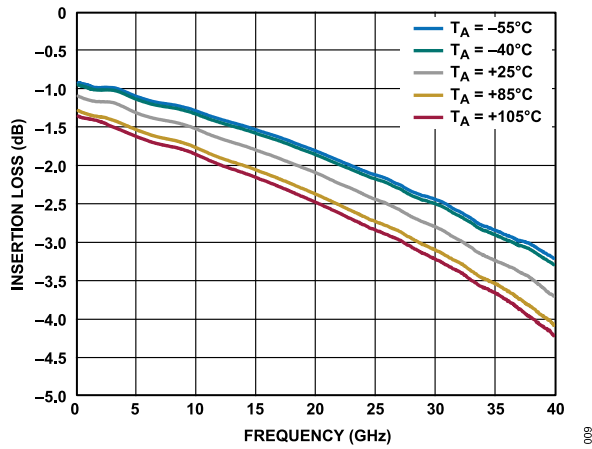


Figure 9. Insertion Loss vs. Frequency over Temperature

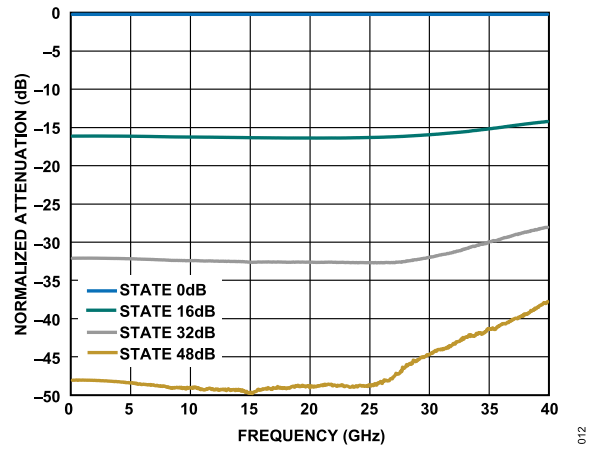


Figure 12. Normalized Attenuation vs. Frequency for All States

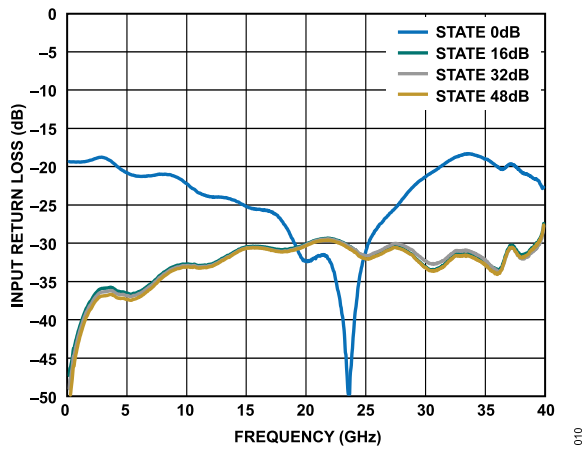


Figure 10. Input Return Loss vs. Frequency

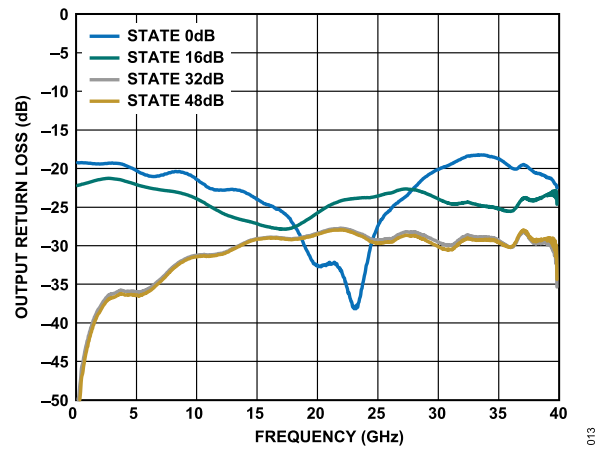


Figure 13. Output Return Loss vs. Frequency

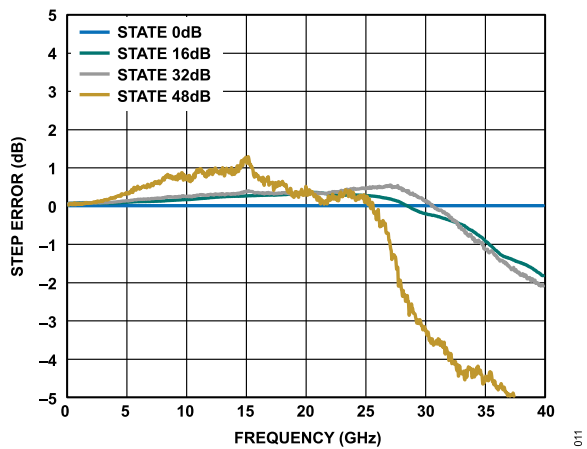


Figure 11. Step Error vs. Frequency

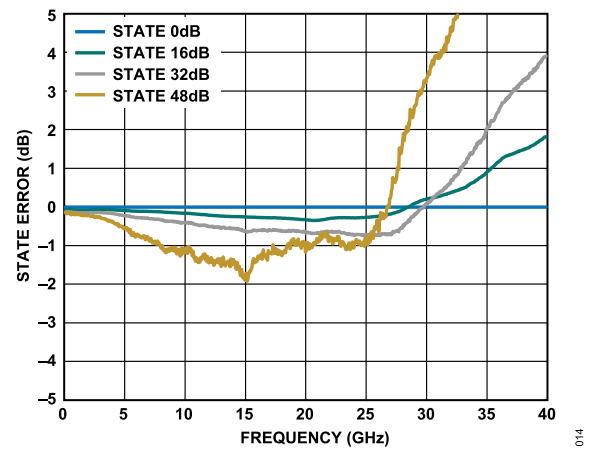


Figure 14. State Error vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

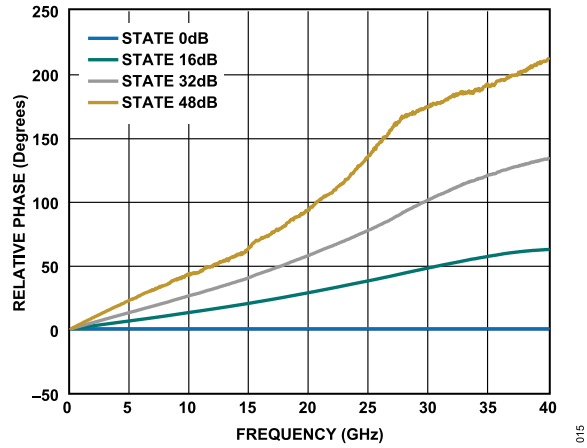


Figure 15. Relative Phase vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = +3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted.

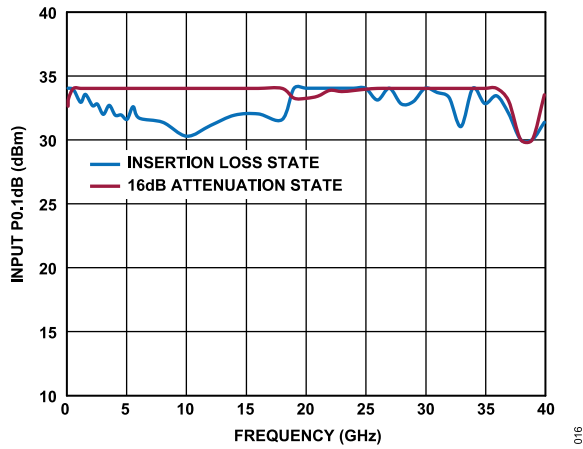


Figure 16. Input P0.1dB vs. Frequency

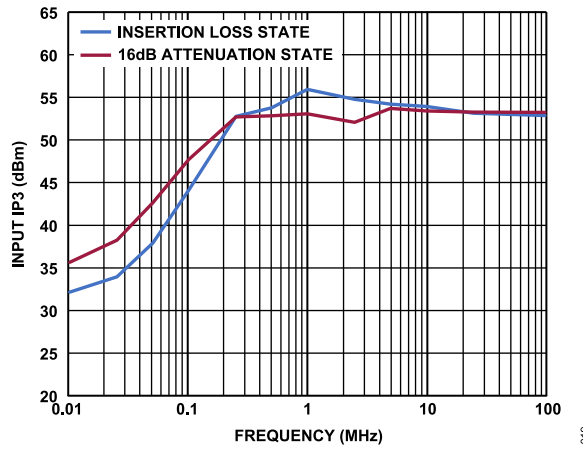


Figure 19. Input IP3 vs. Frequency, Low Frequency Detail

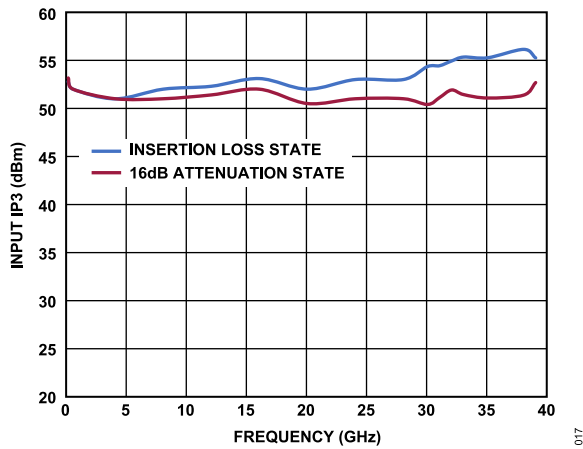


Figure 17. Input IP3 vs. Frequency

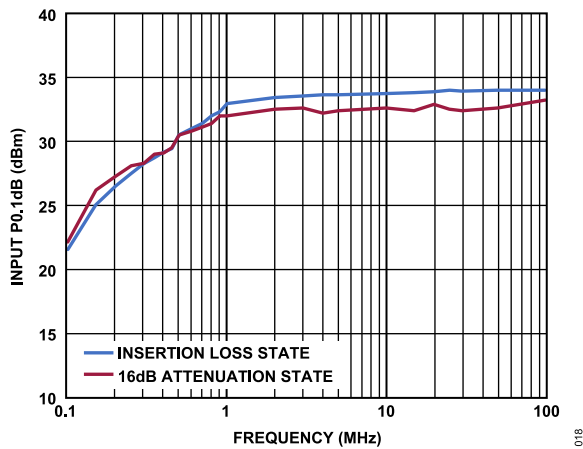


Figure 18. Input P0.1dB vs. Frequency, Low Frequency Detail

## THEORY OF OPERATION

The ADRF5717 incorporates a 2-bit fixed attenuator array that offers an attenuation range of 48 dB in 16 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5717 has two digital control inputs, D5 (LSB) and D6 (MSB), to select the desired attenuation state in parallel mode, as shown in Figure 20. See Table 7 for the truth table.

Table 7. Truth Table

Digital Control Input		Attenuation State (dB)
D5	D6	
Low	Low	0 (reference)
High	Low	16
Low	High	32
High	High	48

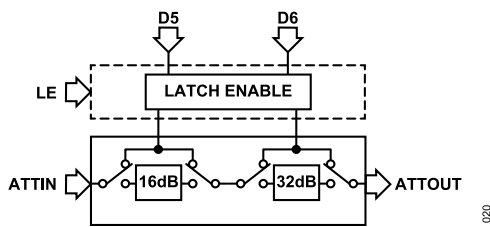


Figure 20. Simplified Circuit Diagram

### RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0 V. No DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50  $\Omega$ . Therefore, external matching components are not required.

The ADRF5717 supports bidirectional operation at the same power level. The power handling of the ATTIN and ATTOUT ports are the same. Refer to the RF input power specifications in Table 1.

The ADRF5717 can operate with a single positive supply voltage applied to the VDD pin and the VSS pin connected to ground. However, some performance degradations can occur in the input compression and input third-order intercept (see Table 2).

### POWER SUPPLY

The ADRF5717 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply the digital control input. However, powering the digital control input before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 k $\Omega$  resistor to limit the current flowing into the control pins. Use pull-up or pull-down resistors if the controller output is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal to ATTIN or ATTOUT.

The ideal power-down sequence is the reverse order of the power-up sequence.

### PARALLEL MODE INTERFACE

There are two modes of parallel operation: direct parallel and latched parallel.

#### Direct Parallel Mode

To enable direct parallel mode, the LE pin must be kept high. To change the attenuation state, use the control voltage inputs (D5 and D6) directly.

#### Latched Parallel Mode

To enable latched parallel mode, keep the LE pin low when changing the control voltage inputs (D5 and D6) to set the attenuation state. When the desired state is set, toggle LE high to transfer the data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change.

**APPLICATIONS INFORMATION**

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a trace width of 16 mil and a ground clearance of 6 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines. On the VDD and VSS supply traces, a 100 pF bypass capacitor filters high frequency noise.

Figure 21 shows the simplified application circuit for the ADRF5717.

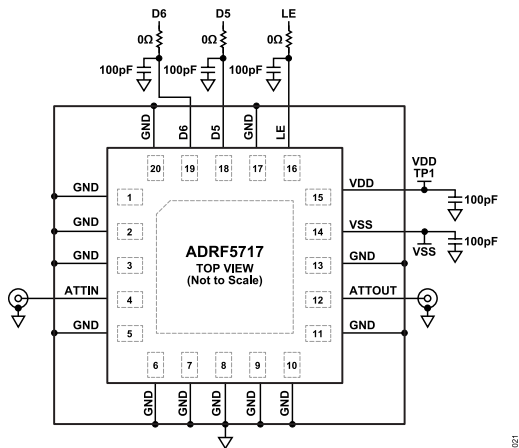


Figure 21. Simplified Application Circuit

**RECOMMENDATIONS FOR PCB DESIGN**

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a CPWG with a 50 Ω characteristic impedance on the PCB. Figure 22 shows the referenced CPWG RF trace design for an RF substrate with 12 mil thick Rogers RO4003 dielectric material. The RF trace with a 16 mil width and a 6 mil clearance is recommended for 2.2 mil finished copper thickness.

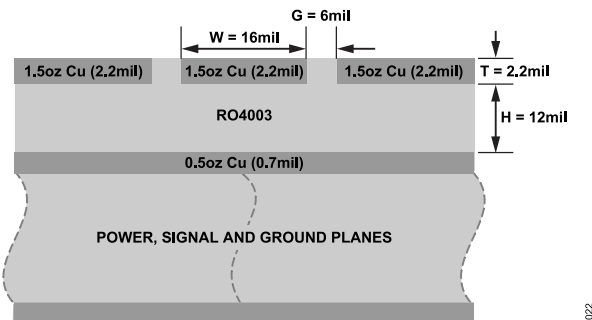


Figure 22. Example PCB Stackup

Figure 23 shows the routing of the RF traces, supply, and control signals from the ADRF5717. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

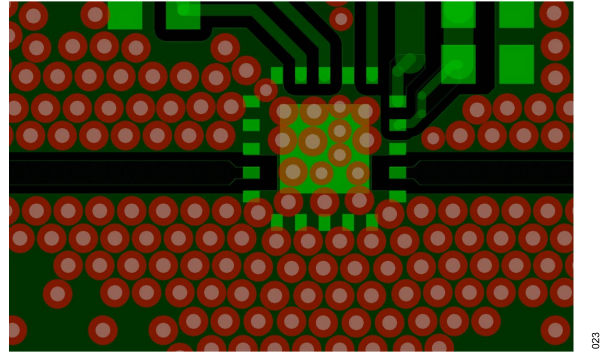


Figure 23. PCB Routings

Figure 24 shows the recommended layout from the ATTIN and ATTOUT pins of the ADRF5717 to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width 2 mils and tapered with 90° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

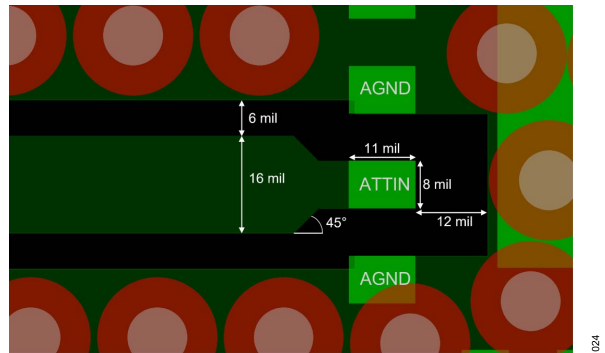


Figure 24. Recommended ATTIN Pin and ATTOUT Pin Transitions

For alternate PCB stackups with different dielectric thickness and CPWG design, contact [Analog Devices, Inc., Technical Support Request](https://www.analog.com) for further recommendations.

OUTLINE DIMENSIONS

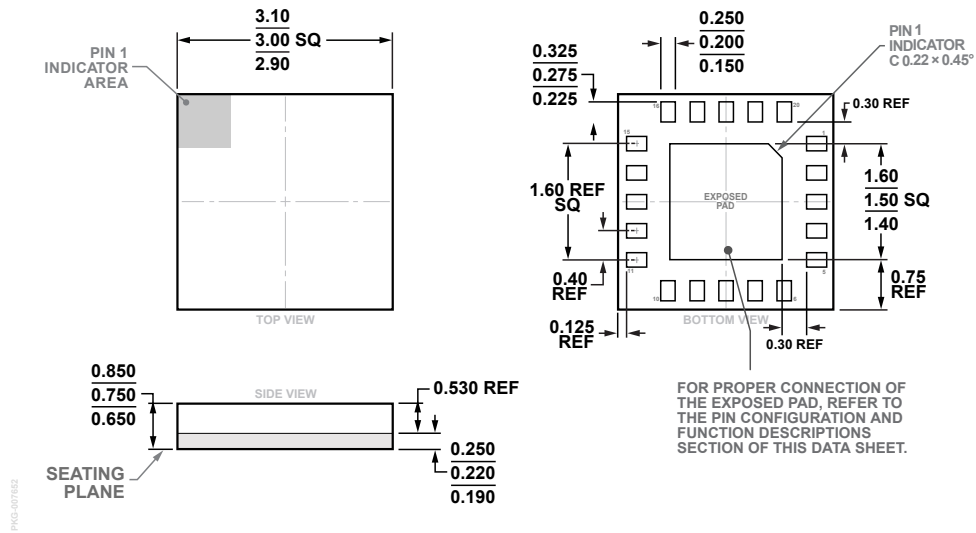


Figure 25. 20-Terminal Land Grid Array [LGA] (CC-20-9)  
Dimensions shown in millimeters

Updated: May 02, 2024

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5717BCCZN	-40°C to +105°C	20-lead LGA (3mm × 3mm)	Cut Tape, 500	CC-20-9
ADRF5717BCCZN-R7	-40°C to +105°C	20-lead LGA (3mm × 3mm)	Cut Tape, 500	CC-20-9

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Model <sup>1</sup>	Description
ADRF5717-EVALZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.

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