Silicon SPDT Switch, Nonreflective, 100 MHz to 44 GHz

Enhanced Product

ADRF5026-EP

FEATURES

- Ultrawideband frequency range: 100 MHz to 44 GHz
- Nonreflective design
- Low insertion loss: 1.2 dB to 18 GHz, 1.7 dB to 26 GHz, 2.4 dB to 40 GHz, 3.8 dB to 44 GHz
- High isolation: 55 dB to 18 GHz, 53 dB to 26 GHz, 50 dB to 40 GHz, 45 dB to 44 GHz
- High input linearity: 27 dBm typical P1dB, 53 dBm typical IP3
- High power handling: 24 dBm insertion loss path, 24 dBm isolation path
- All off state control
- No low frequency spurious signals
- 0.1 dB RF settling time: 40 ns typical
- 20-terminal, 3 mm × 3 mm LGA package
- Pin compatible with ADRF5027, low frequency cutoff version

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +105°C)
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

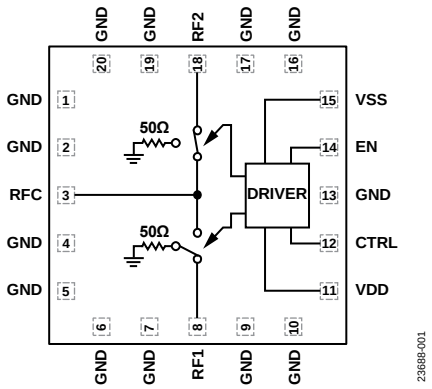

Figure 1.

GENERAL DESCRIPTION

The ADRF5026-EP is a nonreflective, single-pole, double-throw (SPDT) RF switch manufactured in a silicon process.

The ADRF5026-EP operates from 100 MHz to 44 GHz with better than 3.8 dB of insertion loss and 45 dB of isolation. The ADRF5026-EP features an all off control, where both RF ports are in an isolation state. The ADRF5026-EP has a nonreflective design and both of the RF ports are internally terminated to 50 Ω.

The ADRF5026-EP requires a dual-supply voltage of +3.3 V and −3.3 V. The device employs CMOS and low voltage transistor transistor logic (LVTTL)-compatible controls.

The ADRF5026-EP is pin compatible with the ADRF5027 low frequency cutoff version, which operates from 9 kHz to 44 GHz.

The ADRF5026-EP RF ports are designed to match a characteristic impedance of 50 Ω. For ultrawideband products, impedance matching on the RF transmission lines can further optimize high frequency insertion loss and return loss characteristics. Refer to the ADRF5026 data sheet for an example of a matched circuit that achieves a flat insertion loss response of 2.4 dB from 28 GHz to 43 GHz.

The ADRF5026-EP comes in a 20-terminal, 3 mm × 3 mm, RoHS compliant, land grid array (LGA) package and can operate from −55°C to +105°C.

Additional application and technical information can be found in the ADRF5026 data sheet.

Rev. 0 Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

10/2020—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, CTRL pin voltage (V_{CTRL}) = EN pin voltage (V_{EN}) = 0 V or VDD, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		44,000	MHz
INSERTION LOSS	IL					
Between RFC and RF1/RF2		100 MHz to 18 GHz		1.2		dB
		18 GHz to 26 GHz		1.7		dB
		26 GHz to 35 GHz		2.2		dB
		35 GHz to 40 GHz		2.4		dB
		40 GHz to 44 GHz[1]		3.8		dB
RETURN LOSS	RL					
RFC and RF1/RF2 (On)		100 MHz to 18 GHz		22		dB
		18 GHz to 26 GHz		12		dB
		26 GHz to 35 GHz		9		dB
		35 GHz to 40 GHz		10		dB
		40 GHz to 44 GHz[1]		7		dB
RF1/RF2 (Off)		100 MHz to 18 GHz		23		dB
		18 GHz to 26 GHz		23		dB
		26 GHz to 35 GHz		21		dB
		35 GHz to 40 GHz		13		dB
		40 GHz to 44 GHz[1]		12		dB
ISOLATION						
Between RFC and RF1/RF2		100 MHz to 18 GHz		55		dB
		18 GHz to 26 GHz		53		dB
		26 GHz to 35 GHz		53		dB
		35 GHz to 40 GHz		50		dB
		40 GHz to 44 GHz		45		dB
Between RF1 and RF2		100 MHz to 18 GHz		63		dB
		18 GHz to 26 GHz		60		dB
		26 GHz to 35 GHz		60		dB
		35 GHz to 40 GHz		63		dB
		40 GHz to 44 GHz		55		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		3		ns
On and Off Time	t_{ON}, t_{OFF}	50% of triggered V_{CTRL} to 90% of RF output		14		ns
RF Settling Time						
0.1 dB		50% of triggered V_{CTRL} to 0.1 dB of final RF output		40		ns
0.05 dB		50% of triggered V_{CTRL} to 0.05 dB of final RF output		45		ns
INPUT LINEARITY		100 MHz to 40 GHz				
1 dB Compression	P1dB			27		dBm
Third-Order Intercept	IP3	Two-tone input power = 12 dBm each tone, Δf = 1 MHz		53		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive	I_{DD}			2		µA
Negative	I_{SS}			100		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUTS		CTRL and EN pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High Current	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	VDD		3.15		3.45	V
Negative	VSS		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}, V_{EN}		0		VDD	V
RF Input Power[2]	P_{IN}	f = 100 MHz to 40 GHz, T_{CASE} = 85°C[3]				
Insertion Loss Path		RF signal is applied to RFC or through connected RF1/RF2			24	dBm
Isolation Path		RF signal is applied to terminated RF1/RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			24	dBm
Case Temperature	T_{CASE}		−55		+105	°C

[1] Impedance matching on RF transmission lines improves high frequency performance. Refer to the ADRF5026 data sheet for more information.
[2] For power derating vs. frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path, isolation path, and hot switching power specifications.
[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Inputs	
Voltage	−0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power[1] (100 MHz to 40 GHz at T_{CASE} = 85°C[2])	
Insertion Loss Path	26 dBm
Isolation Path	25 dBm
Hot Switching	25 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	
RFC, RF1, RF2 Pins	500 V
Digital Pins	2000 V
Charged Device Model (CDM)	1250 V

[1] For power derating vs. frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path, isolation path, and hot switching power specifications.
[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-20-4		
Through Path	423	°C/W
Terminated Path	241	°C/W

POWER DERATING CURVES

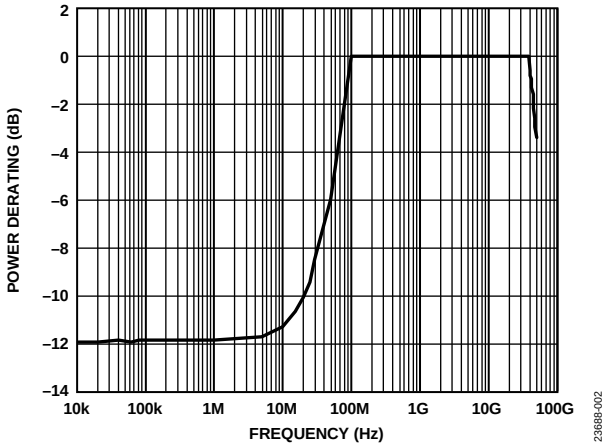

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

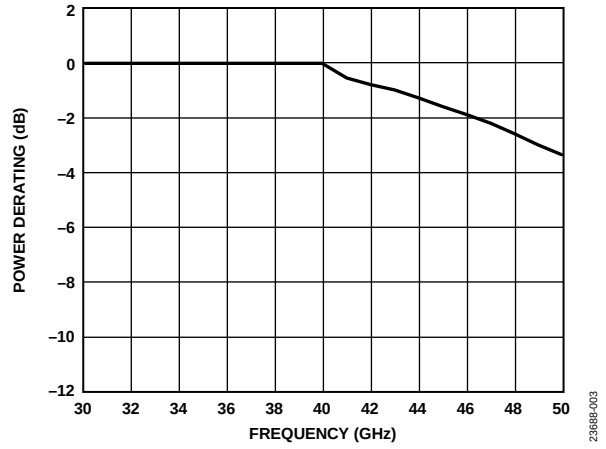

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

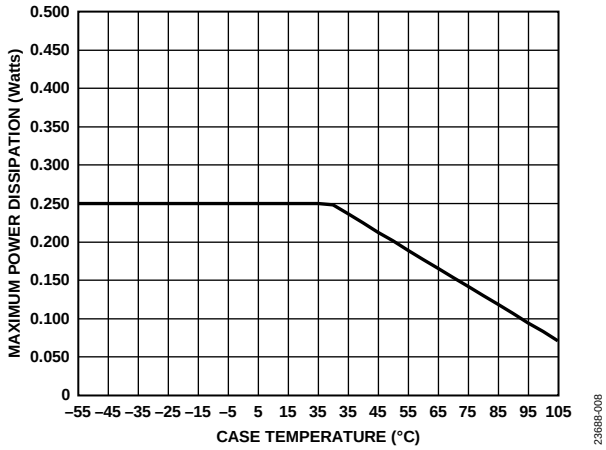

Figure 4. Maximum Power Dissipation vs. Case Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

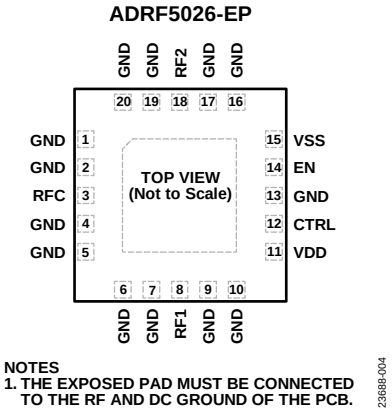

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 6, 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
3	RFC	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic.
8	RF1	RF1 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic.
11	VDD	Positive Supply Voltage.
12	CTRL	Control Input Voltage. See Figure 7 for the interface schematic.
14	EN	Enable Input Voltage. See Figure 7 for the interface schematic.
15	VSS	Negative Supply Voltage.
18	RF2	RF2 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB.

INTERFACE SCHEMATICS

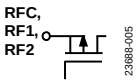

Figure 6. RFC, RF1, RF2 Interface Schematic

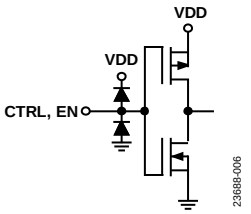

Figure 7. CTRL, EN Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 3.3 V, VSS = −3.3 V, V_{CTRL}/V_{EN} = 0 V or VDD, and T_{CASE} = 25°C in a 50 Ω system, unless otherwise noted.

Insertion loss is measured on the probe matrix board using ground-signal-ground (GSG) probes close to the RFx pins. Signal coupling between the probes limits the isolation performance of the ADRF5026-EP. Isolation is measured on the ADRF5026-EVALZ evaluation board. See the ADRF5026 data sheet for details on the ADRF5026-EVALZ evaluation board and probe matrix board.

See the ADRF5026 data sheet for a full set of Typical Performance Characteristics plots.

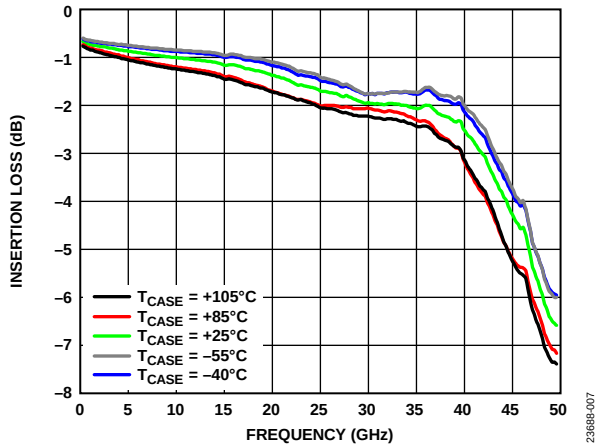

Figure 8. Insertion Loss vs. Frequency over Temperature

OUTLINE DIMENSIONS

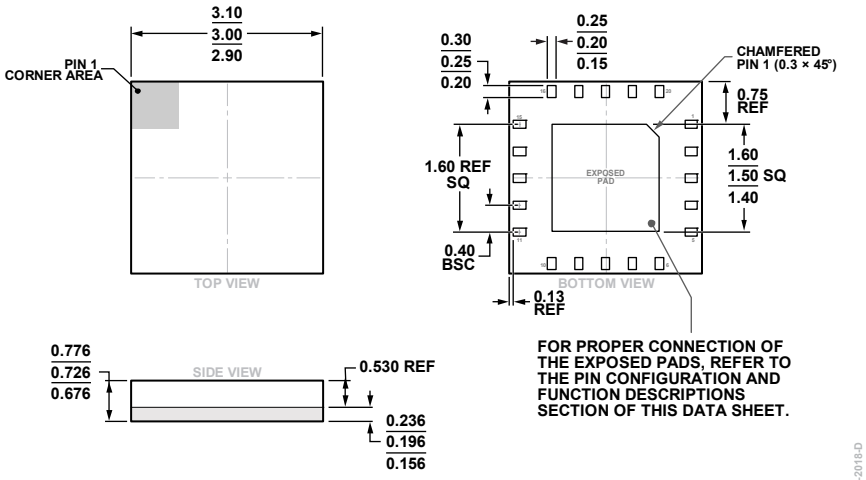

Figure 9. 20-Terminal Land Grid Array [LGA]
3 mm × 3 mm Body and 0.726 mm Package Height
(CC-20-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADRF5026SCCZ-EP	−55°C to +105°C	20-Terminal Land Grid Array [LGA]	CC-20-4	6EP
ADRF5026SCCZ-EPR7	−55°C to +105°C	20-Terminal Land Grid Array [LGA]	CC-20-4	6EP

[1] Z = RoHS Compliant Part.

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ADRF5026BCCZN ADRF5026BCCZN-R7 ADRF5026SCCZ-EP ADRF5026SCCZ-EPR7 ADRF5026-EVALZ-240 ADRF5026-EVALZ-292