2 GHz to 6 GHz, 46 dBm (40 W), GaN Power Amplifier

FEATURES

- Internally matched and AC-coupled, 40 W, GaN power amplifier
- Integrated drain bias inductor
- P_{OUT}: 46.5 dBm typical from 2.0 GHz to 5.7 GHz (P_{IN} = 21 dBm)
- Small signal gain: 40.5 dB typical from 2.3 GHz to 5.7 GHz
- Power gain: 25.5 dB typical from 2.0 GHz to 5.7 GHz (P_{IN} = 21 dBm)
- PAE: 39% typical from 2.3 GHz to 5.7 GHz
- V_{DD} = 28 V at I_{DQ} = 750 mA
- 14-lead ceramic leaded chip carrier [LDCC] with a copper-molybdenum base

APPLICATIONS

- Military jammers
- Commercial and military radars
- Test and measurement equipment

GENERAL DESCRIPTION

The ADPA1113 is a gallium nitride (GaN), broadband power amplifier delivering 46.5 dBm (44.7 W) with 39.0% power added efficiency (PAE) from 2.3 GHz to 5.7 GHz. No external matching or AC-coupling are required to achieve full-band operation. Additionally, no external inductor is required to bias the amplifier.

The ADPA1113 is ideal for continuous wave applications, such as military jammers and radars.

FUNCTIONAL BLOCK DIAGRAM

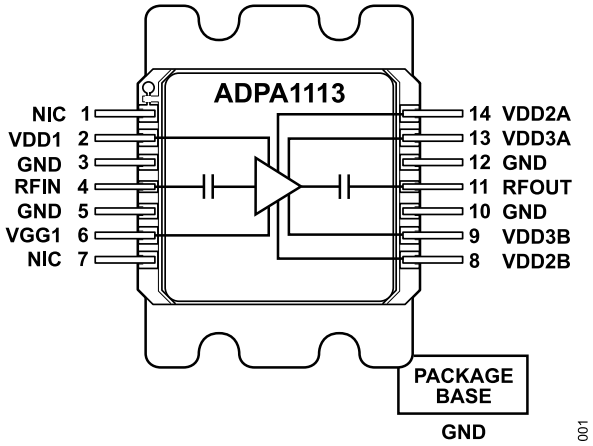

Figure 1. Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

1/2024—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

2.0 GHz to 2.3 GHz Frequency Range

T_{CASE} = 25°C, supply voltage (V_{DD}) = 28 V, target quiescent current (I_{DQ}) = 750 mA, and frequency range = 2.0 GHz to 2.3 GHz, unless otherwise noted.

Table 1. 2.0 GHz to 2.3 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2.0		2.3	GHz	
GAIN					
Small Signal Gain	36.5	39.0		dB	
Gain Variation over Temperature		0.44		dB/°C	
Gain Flatness		±1.2		dB	
RETURN LOSS					
Input (S11)		18		dB	
Output (S12)		7		dB	
POWER					Input power (P_{IN}) = 21 dBm
Output (P_{OUT})	44.5	46.5		dBm	
Gain (S21)	23.5	25.5		dB	
PAE		47.0		%	
I_{DQ}		750		mA	Adjust the gate control voltage (V_{GG1}) between −4 V and −1.9 V to achieve an I_{DQ} = 750 mA typical

2.3 GHz to 5.7 GHz Frequency Range

T_{CASE} = 25°C, V_{DD} = 28 V, I_{DQ} = 750 mA, and frequency range = 2.3 GHz to 5.7 GHz, unless otherwise noted.

Table 2. 2.3 GHz to 5.7 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2.3		5.7	GHz	
GAIN					
Small Signal Gain	38.0	40.5		dB	
Gain Variation over Temperature		0.05		dB/°C	
Gain Flatness		±0.8		dB	
RETURN LOSS					
Input		14		dB	
Output		10		dB	
POWER					P_{IN} = 21 dBm
P_{OUT}	44.5	46.5		dBm	
Gain	23.5	25.5		dB	
PAE		39		%	
I_{DQ}		750		mA	Adjust V_{GG1} between −4 V and −1.9 V to achieve an I_{DQ} = 750 mA typical

SPECIFICATIONS

5.7 GHz to 6.0 GHz Frequency Range

T_{CASE} = 25°C, V_{DD} = 28 V, I_{DQ} = 750 mA, and frequency range = 5.7 GHz to 6.0 GHz, unless otherwise noted.

Table 3. 5.7 GHz to 6.0 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	5.7		6.0	GHz	
GAIN					
Small Signal Gain	36.5	39.0		dB	
Gain Variation over Temperature		0.05		dB/°C	
Gain Flatness		±0.4		dB	
RETURN LOSS					
Input		20.0		dB	
Output		8.0		dB	
POWER					P_{IN} = 21 dBm
P_{OUT}	44.0	46.0		dBm	
Gain	23.0	25.0		dB	
PAE		32		%	
I_{DQ}		750		mA	Adjust V_{GG1} between −4 V and −1.9 V to achieve an I_{DQ} = 750 mA typical

ABSOLUTE MAXIMUM RATINGS

This device is not surface mountable and is not intended nor suitable to be used in a solder reflow process. This device must not be exposed to ambient temperatures above 150°C.

Table 4. Absolute Maximum Ratings

Parameter	Rating
Bias Voltage	
Drain (VDD1, VDD2A, VDD2B, VDD3A, and VDD3B)	35 V DC
Gate (VGG1)	−8 V DC to 0 V DC
RFIN	26 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C, Derate 725 mW/°C Above 85°C	101 W
Temperature	
Maximum Channel	225°C
Nominal Peak Channel, T_{CASE} = 85°C, P_{IN} = 21 dBm, P_{DISS} = 75 W at 6 GHz	188.5°C
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type[1, 2]	θ_{JC}	Unit
EJ-14-1	1.38	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the package flange to the heat sink. The package flange is held constant at the operating temperature of 85°C.

[2] θ_{JC} is the channel to case thermal resistance where the case is the bottom of the package flange.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1113

Table 6. ADPA1113, 14-Lead LDCC

ESD Model	Withstand Threshold (V)	Class
HBM	500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

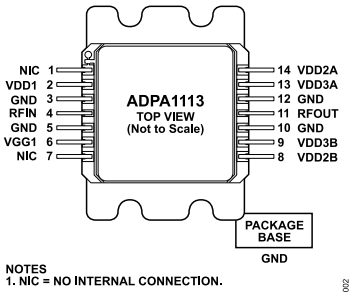

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	NIC	No Internal Connection. The NIC pins are not connected internally. For normal operation, connect to ground.
2	VDD1	Drain Bias for First Stage of Amplifier. See Figure 3 for the VDD1 pin interface schematic.
3, 5, 10, 12	GND	Ground. The ground pins must be connected to the RF and the DC ground. See Figure 4 for the GND interface schematic.
4	RFIN	RF Input. The RFIN pin is AC-coupled and internally matched to 50 Ω. See Figure 3 for the RFIN interface schematic.
6	VGG1	Gate Control for All Three Stages of the Amplifier. See Figure 3 for the VGG1 interface schematic.
8	VDD2B	Drain Bias for the Second Stage of the South Side of the Amplifier. See Figure 5 for the VDD2B interface schematic.
9	VDD3B	Drain Bias for the Third Stage of the South Side of the Amplifier. See Figure 6 for the VDD3B interface schematic.
11	RFOUT	RF Output. The RFOUT pin is AC-coupled and internally matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.
13	VDD3A	Drain Bias for the Third Stage of the North Side of the Amplifier. See Figure 6 for the VDD3A interface schematic.
14	VDD2A	Drain Bias for the Second Stage of the North Side of the Amplifier. See Figure 5 for the VDD2A interface schematic.
Package Base	GND	The package base must be connected to the RF and the DC ground. See Figure 4 for the GND Interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

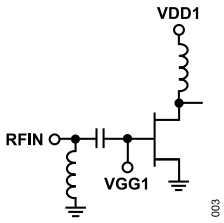

Figure 3. VDD1, RFIN, and VGG1 Interface Schematic

Figure 4. GND Interface Schematic

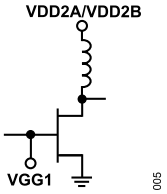

Figure 5. VDD2A and VDD2B Interface Schematic

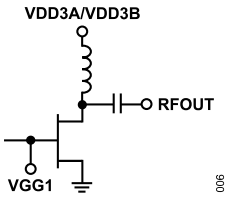

Figure 6. VDD3A, VDD3B, and RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

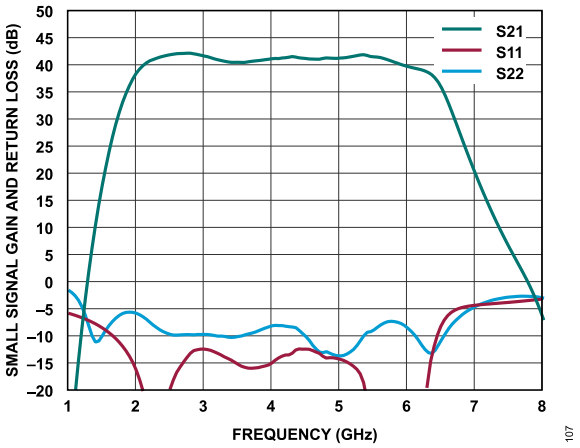

Figure 7. Small Signal Gain and Return Loss vs. Frequency

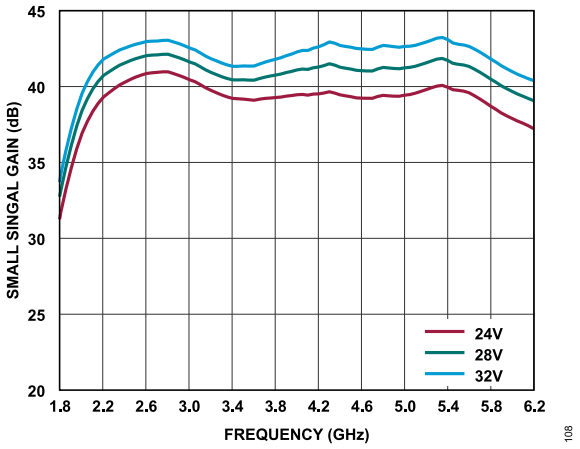

Figure 8. Small Signal Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

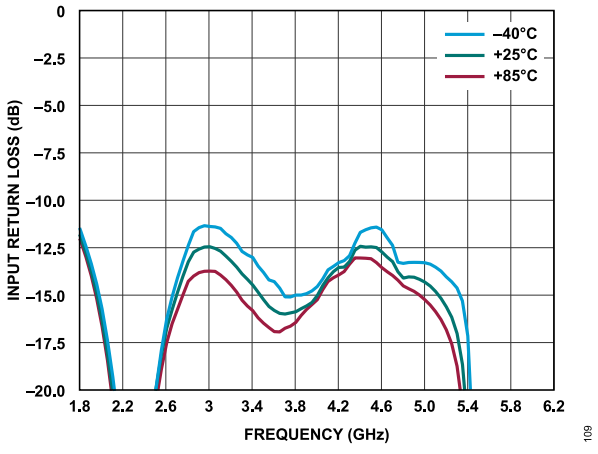

Figure 9. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 750 mA

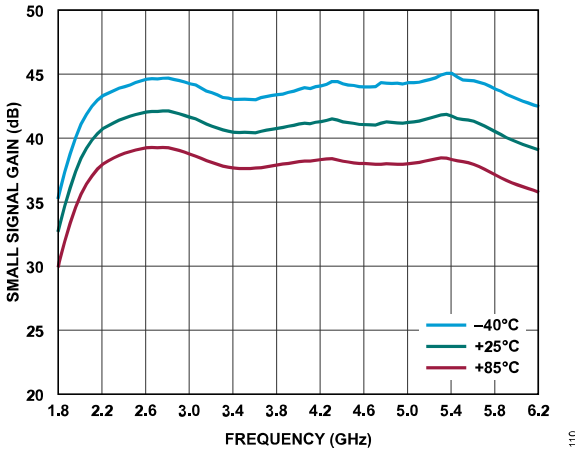

Figure 10. Small Signal Gain vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 750 mA

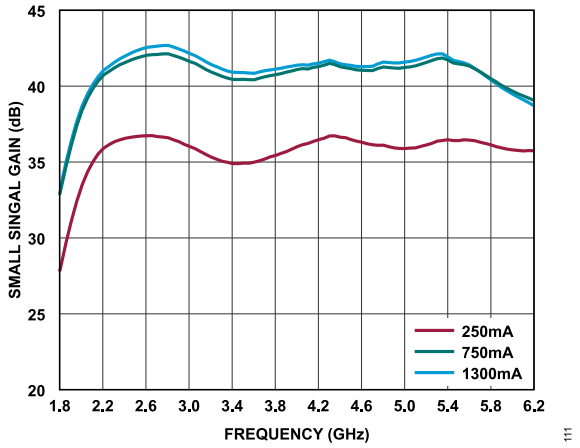

Figure 11. Small Signal Gain vs. Frequency for Various I_{DQ} Supply Currents, V_{DD} = 28 V

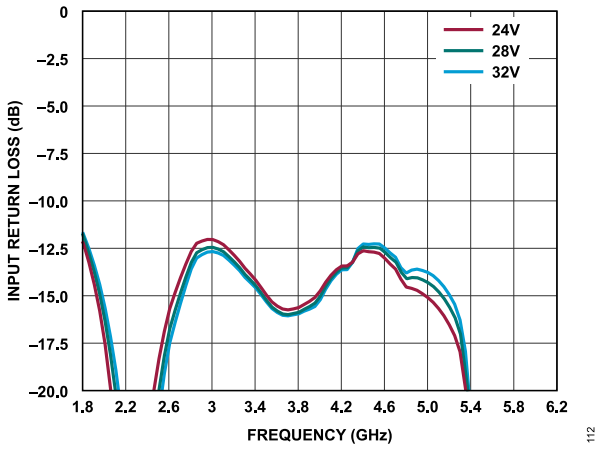

Figure 12. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

TYPICAL PERFORMANCE CHARACTERISTICS

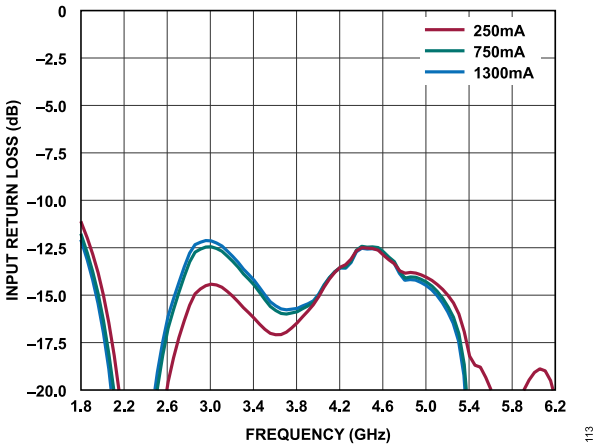

Figure 13. Input Return Loss vs. Frequency for Various I_{DQ} Supply Currents, V_{DD} = 28 V

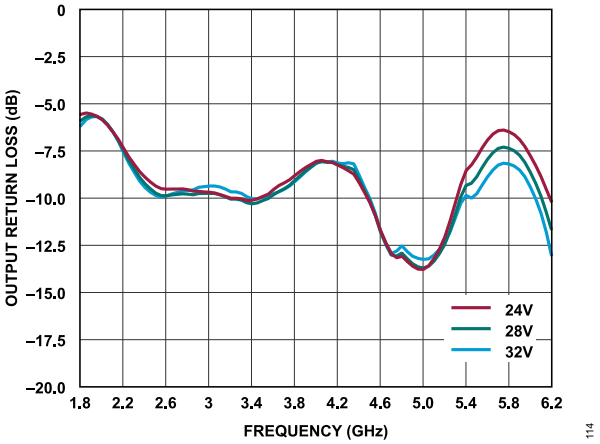

Figure 14. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

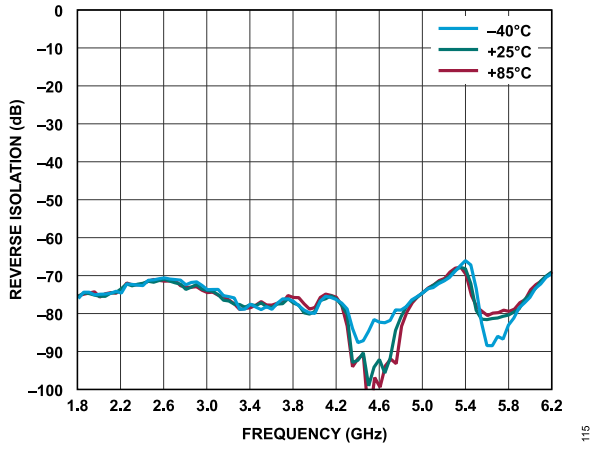

Figure 15. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 750 mA

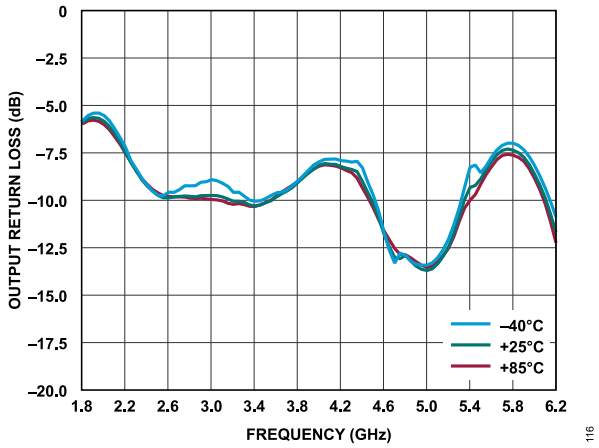

Figure 16. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 750 mA

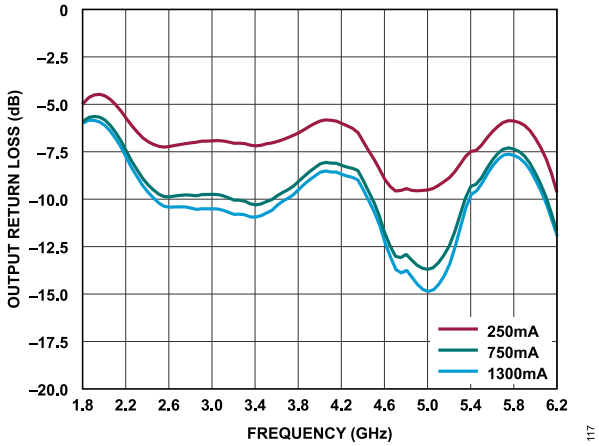

Figure 17. Output Return Loss vs. Frequency for Various I_{DQ} Supply Currents, V_{DD} = 28 V

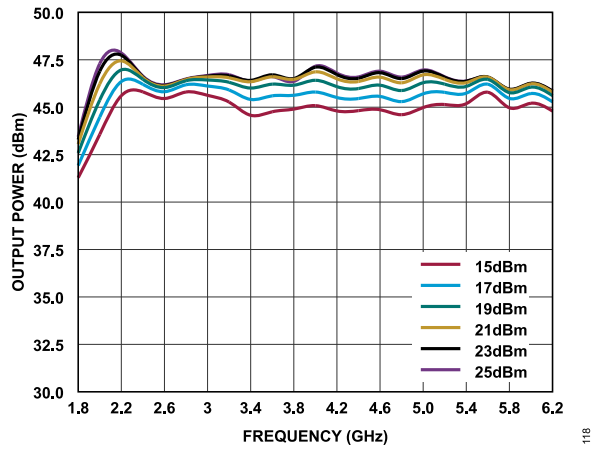

Figure 18. Output Power vs. Frequency for Various P_{IN} Levels, V_{DD} = 28 V, I_{DQ} = 750 mA

TYPICAL PERFORMANCE CHARACTERISTICS

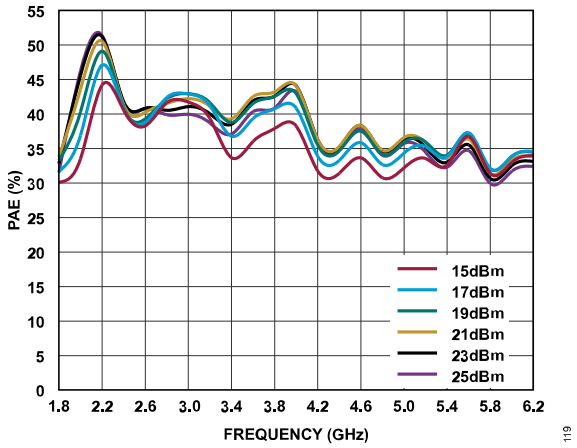

Figure 19. PAE vs. Frequency for Various P_{IN} Levels, V_{DD} = 28 V, I_{DQ} = 750 mA

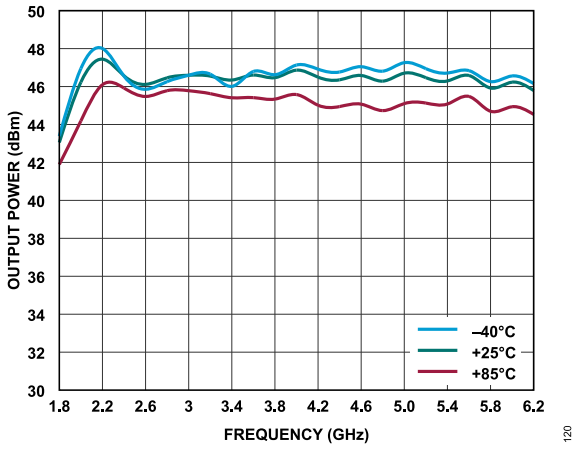

Figure 20. Output Power vs. Frequency at Various Temperatures for P_{IN} = 21 dBm, V_{DD} = 28 V, I_{DQ} = 750 mA

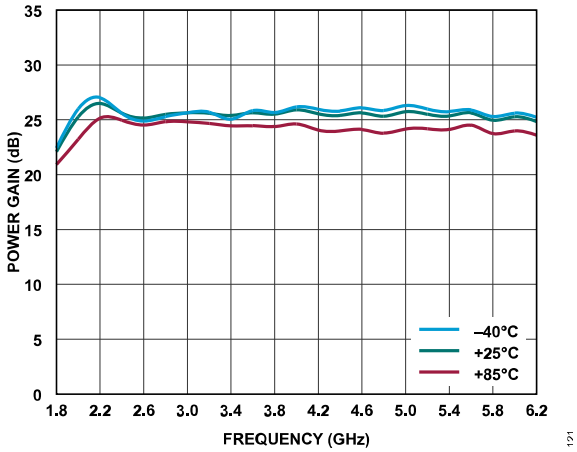

Figure 21. Power Gain vs. Frequency at Various Temperatures for P_{IN} = 21 dBm, V_{DD} = 28 V, I_{DQ} = 750 mA

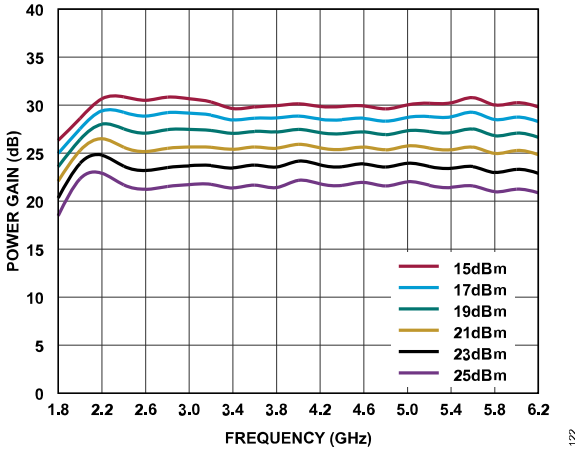

Figure 22. Power Gain vs. Frequency for Various P_{IN} Levels, V_{DD} = 28 V, I_{DQ} = 750 mA

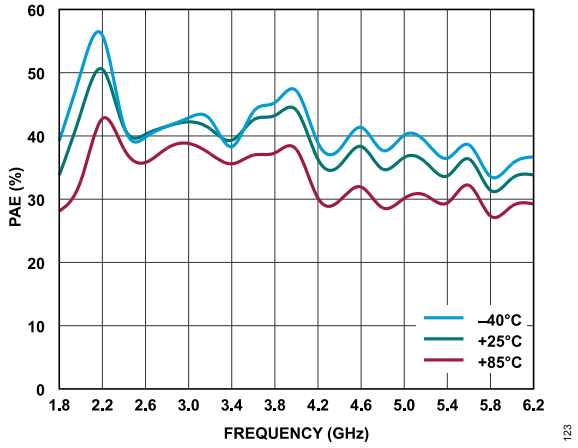

Figure 23. PAE vs. Frequency at Various Temperatures for P_{IN} = 21 dBm, V_{DD} = 28 V, I_{DQ} = 750 mA

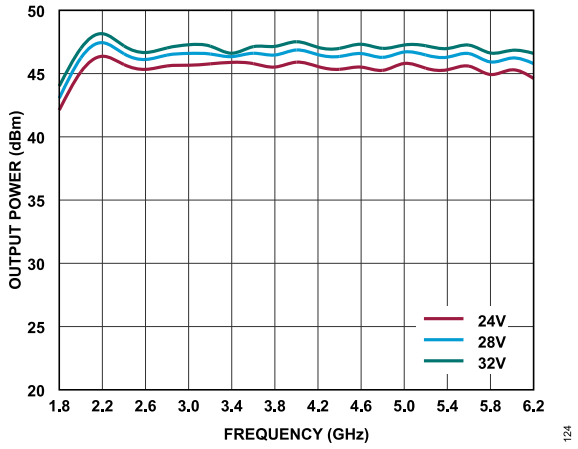

Figure 24. Output Power at P_{IN} = 21 dBm vs. Frequency for Various Supply Voltages at I_{DQ} = 750 mA

TYPICAL PERFORMANCE CHARACTERISTICS

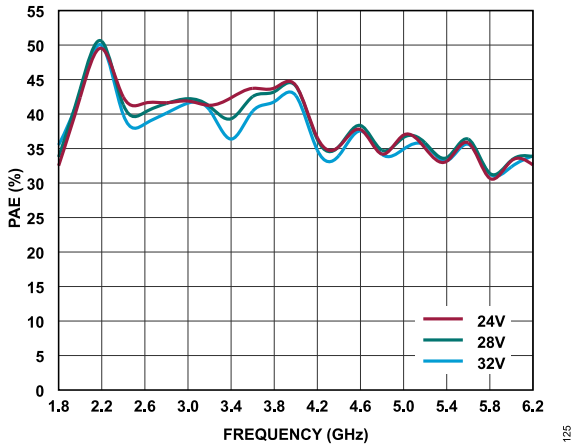

Figure 25. PAE at P_{IN} = 21 dBm vs. Frequency for Various Supply Voltages at I_{DQ} = 750 mA

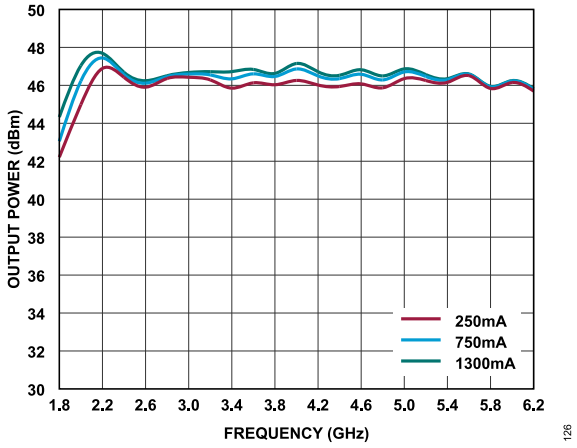

Figure 26. Output Power at P_{IN} = 21 dBm vs. Frequency for Various I_{DQ} Supply Currents at V_{DD} = 28 V

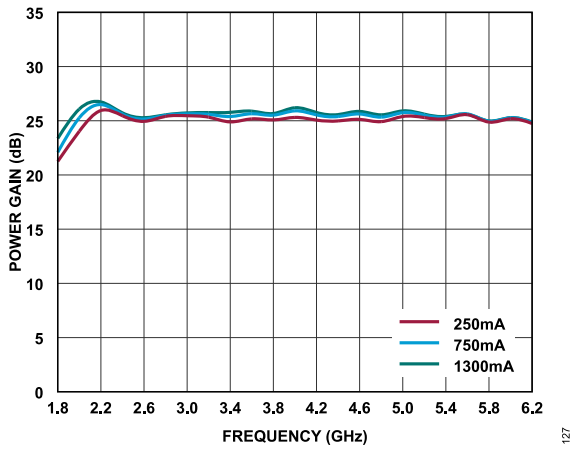

Figure 27. Power Gain at P_{IN} = 21 dBm vs. Frequency for Various I_{DQ} Supply Currents at V_{DD} = 28 V

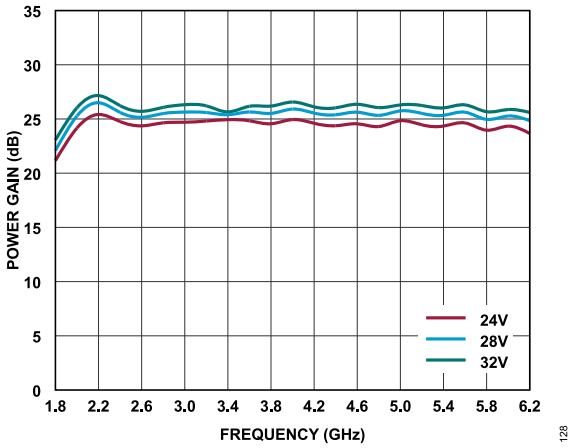

Figure 28. Power Gain at P_{IN} = 21 dBm vs. Frequency for Various Supply Voltages at I_{DQ} = 750 mA

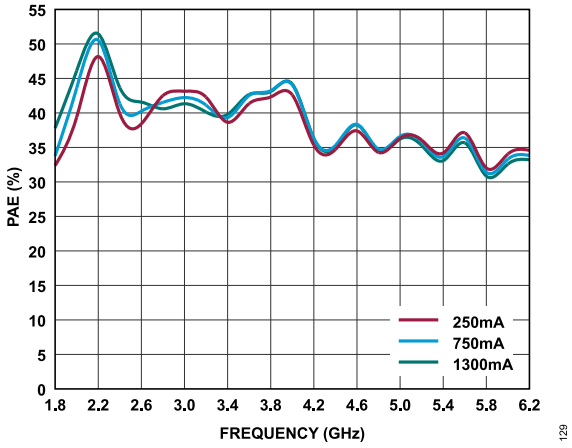

Figure 29. PAE at P_{IN} = 21 dBm vs. Frequency for Various I_{DQ} Supply Currents at V_{DD} = 28 V

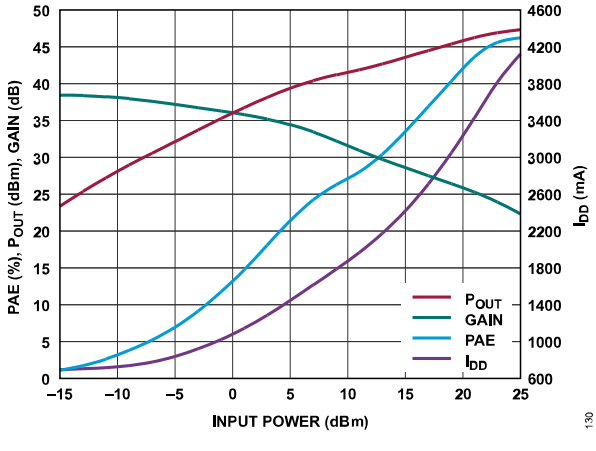

Figure 30. PAE, P_{OUT}, Gain, and Supply Current (I_{DD}) vs. Input Power at 2.0 GHz, V_{DD} = 28 V, I_{DQ} = 750 mA

TYPICAL PERFORMANCE CHARACTERISTICS

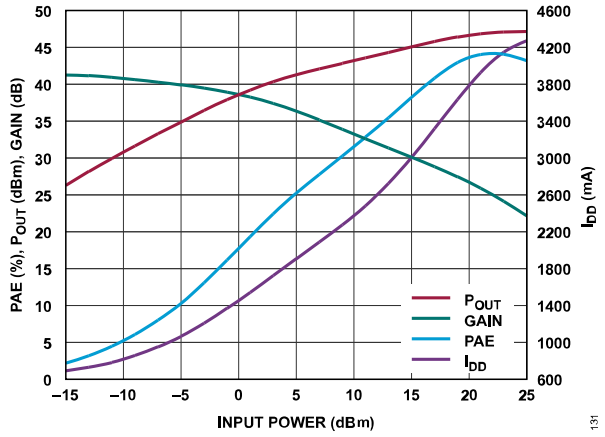

Figure 31. PAE, P_{OUT}, Gain, and I_{DD} vs. Input Power at 4.0 GHz, V_{DD} = 28 V, I_{DQ} = 750 mA

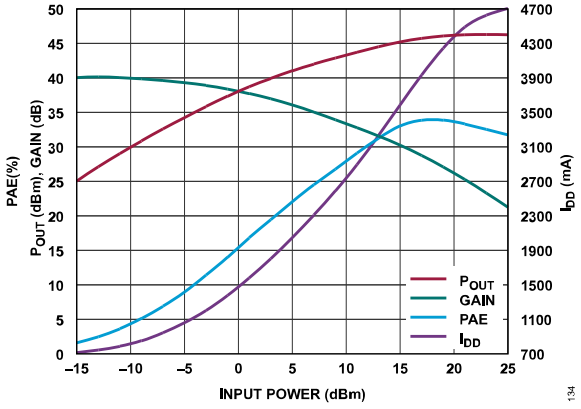

Figure 34. PAE, P_{OUT}, Gain, and I_{DD} vs. Input Power at 6.0 GHz, V_{DD} = 28 V, I_{DQ} = 750 mA

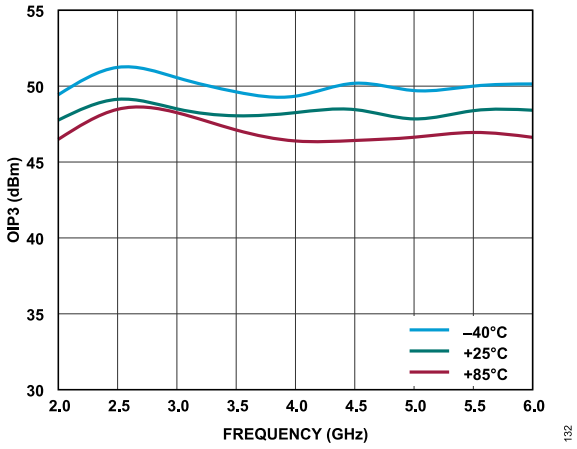

Figure 32. Output Third-Order Intercept (OIP3) vs. Frequency with P_{OUT} per Tone = 36 dBm for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 750 mA

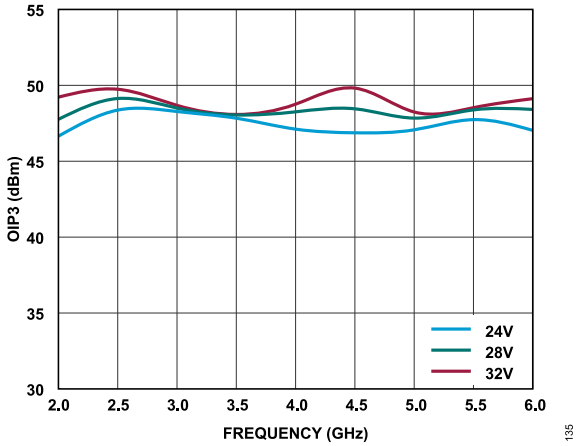

Figure 35. OIP3 vs. Frequency with P_{OUT} per Tone = 36 dBm for Various V_{DD}, I_{DQ} = 750 mA

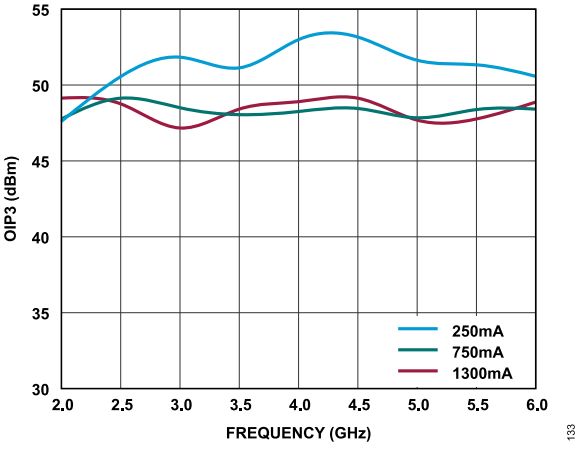

Figure 33. OIP3 vs. Frequency with P_{OUT} per Tone = 36 dBm for Various I_{DQ}, V_{DD} = 28 V

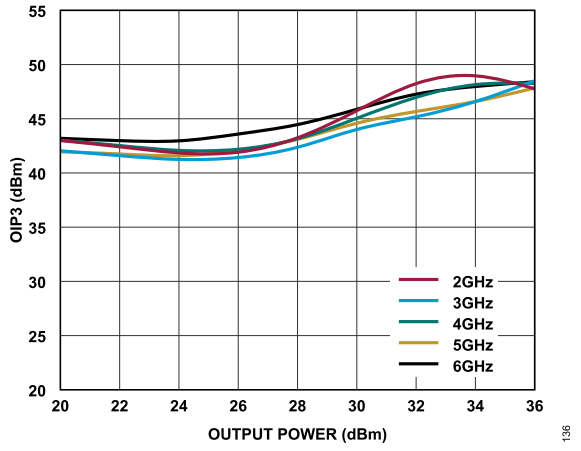

Figure 36. OIP3 vs. Output Power per Tone for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 750 mA

TYPICAL PERFORMANCE CHARACTERISTICS

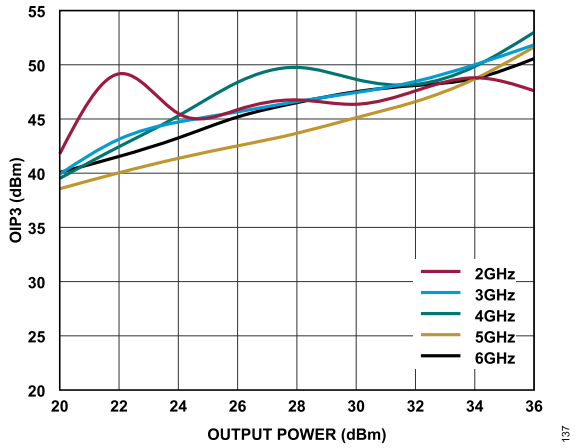

Figure 37. OIP3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 250 mA

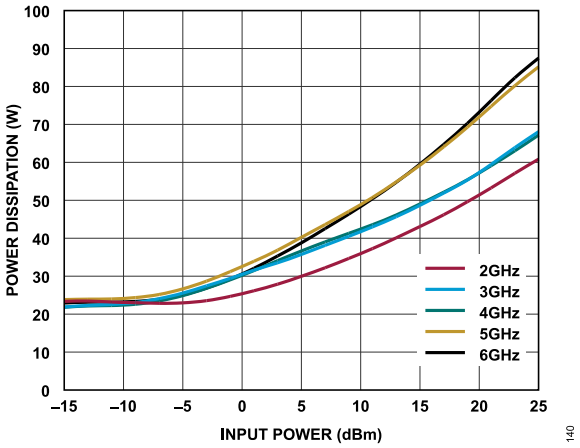

Figure 40. Power Dissipation vs. Input Power for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 750 mA, T_{CASE} = 85°C

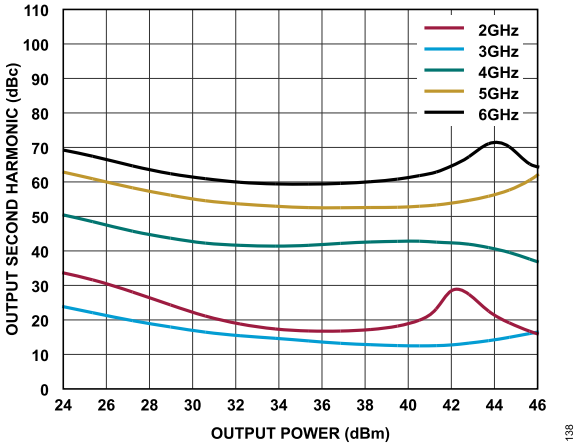

Figure 38. Output Second Harmonic vs. Output Power for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 750 mA

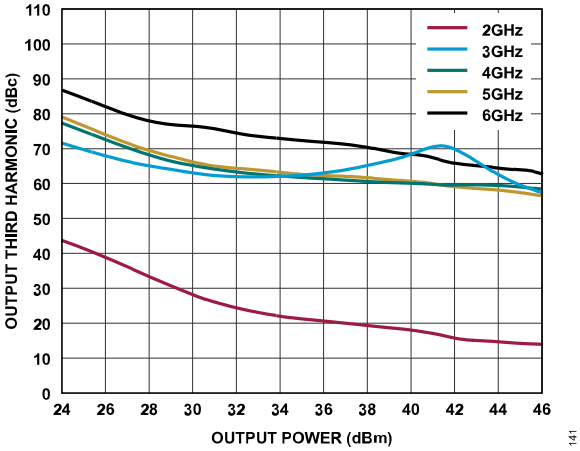

Figure 41. Output Third Harmonic vs. Output Power for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 750 mA

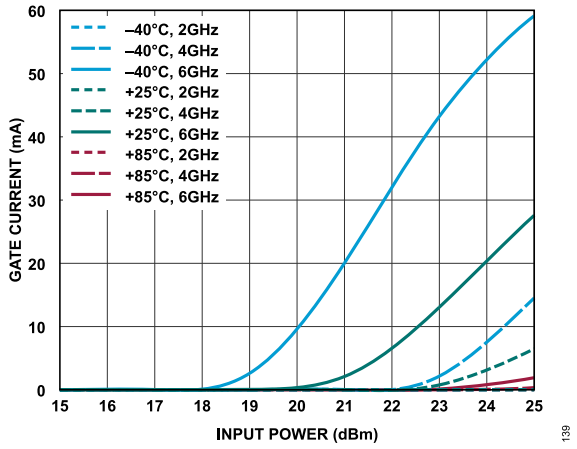

Figure 39. Gate Current vs. Input Power for Various Temperatures and Frequencies, V_{DD} = 28 V, I_{DQ} = 750 mA

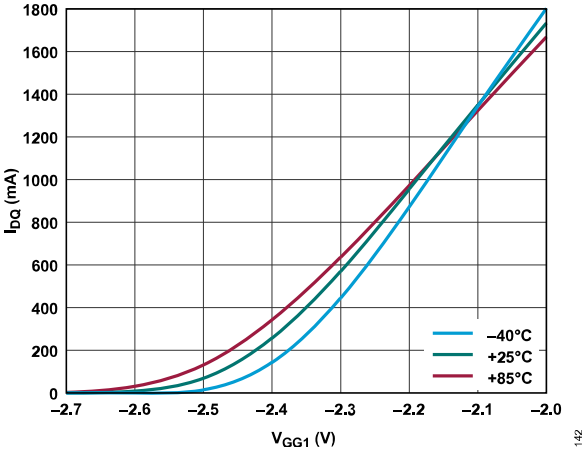

Figure 42. I_{DQ} vs. V_{GG1}, V_{DD} = 28 V

TYPICAL PERFORMANCE CHARACTERISTICS

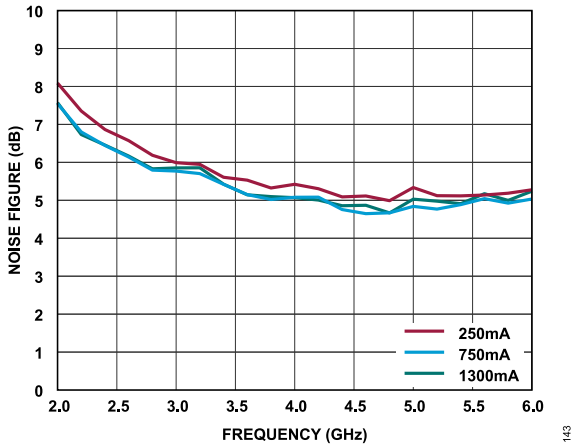

Figure 43. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 28 V

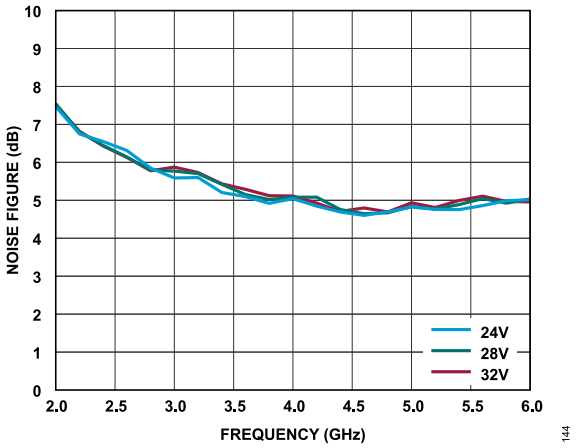

Figure 44. Noise Figure vs. Frequency for Various V_{DD} Values, I_{DQ} = 750 mA

THEORY OF OPERATION

The ADPA1113 is a GaN power amplifier with cascaded gain stages that is biased by a positive drain supply and an externally applied negative gate voltage applied to the VGG1 pin. A nominal 28 V is applied to the first, second, and third stages, and a negative voltage is applied to VGG1 to set the total I_{DQ} to 750 mA nominal.

When biased as described, the device operates in Class AB, resulting in the maximum PAE at saturation. The ADPA1113 features integrated RF chokes for each drain plus on-chip DC blocking of the RFIN and RFOUT ports. While the RFIN and RFOUT ports are internally DC blocked, there is a DC path to ground on the RFIN pin. As a result, if the DC bias level of the signal driving RFIN is not equal to zero, then the DC bias level must be externally AC-coupled.

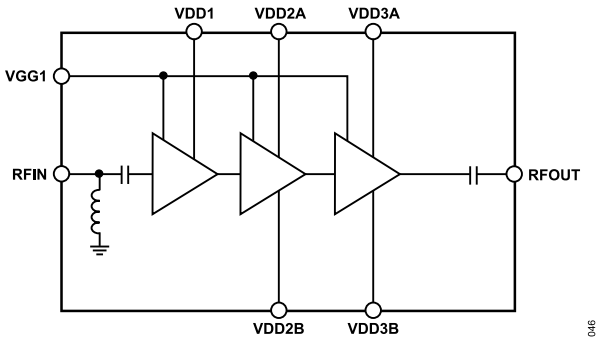

Figure 45. Basic Block Diagram

APPLICATIONS INFORMATION

APPLICATIONS CIRCUIT

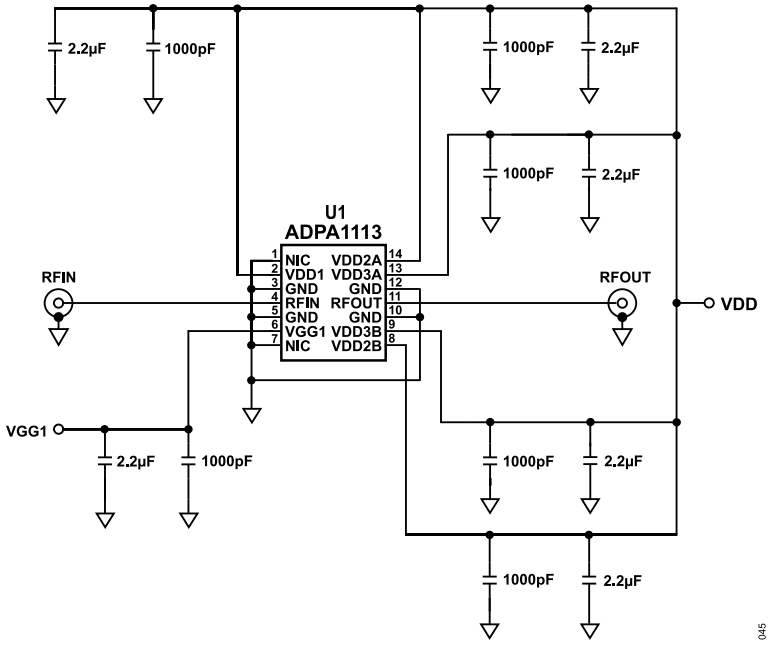

Figure 46. Typical Application Circuit

BASIC CONNECTIONS

The basic connections to operate the ADPA1113 are shown in Figure 46.The same drain supply voltage, 28 V nominal, must be applied to all of the five VDD pins (VDD1, VDD2A, VDD2B, VDD3A, and VDD3B). The VDD pins are capactively decoupled as shown in Figure 46. The gate voltage for all three stages (−1.9 V to −4.0 V for biased operation and −8 V for pinch-off voltage) is applied to the VGG1 pin that is decoupled as shown in Figure 46. Pin 1 and Pin 7 are designated as no internal connection (NIC) pins. Although these NIC pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

To turn on the device, apply −4 V to VGG1 which places it in pinch-off voltage. Then, apply 28 V to VDD1, VDD2A, VDD2B, VDD3A, and VDD3B. Increase the gate voltage (more positive) until the drain current is 750 mA, VGG1 is approximately −2 V, and apply the RF signal. If the desired gate voltage is known in advance, V_{GG1} can be set to that voltage directly without going through the pinch-off step.

To turn off the device, turn off the RF signal and set the VDD voltages to 0 V before increasing VGG1 to 0 V.

The configuration shown in Figure 46, which is also the default configuration of the customer evaluation board, was used to characterize the ADPA1113. It can be possible to reduce the number of power supply decoupling capacitors shown, but this reduction varies by system. When reducing capacitors, the recommendation is to first remove or combine the largest capacitors that are farthest from the device.

Soldering and Assembly Considerations

The ADPA1113 is a nonhermetic air cavity device. The body of the package normally sits within a cutout in the PCB that allows direct access to a heatsink beneath the PCB. To facilitate good thermal and electrical conduction to the heatsink, a shim of electrically and thermally conductive material such as Heat-Spring indium from Indium Corporation can be used. (Alternatively, electrically and thermally conductive paste or grease can be used). The shim is placed between the heatsink and the bottom of the package flange. Then, the package can be attached to the heatsink using 0-80 thread size, 3/16 inches long stainless steel socket head screws (typically). Once attached with the screw hardware, the pins are flush with the PCB which allows the leads to be soldered to the PCB pads.

OUTLINE DIMENSIONS

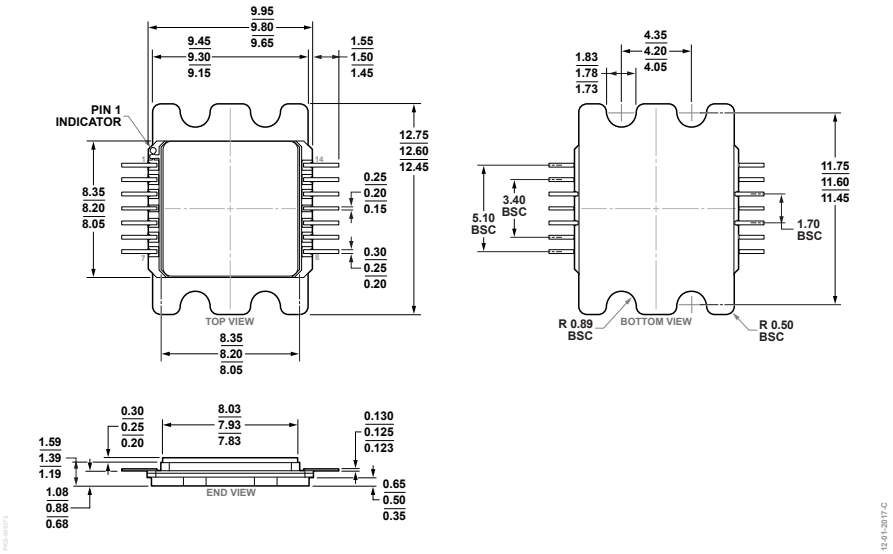

Figure 47. 14-Lead Ceramic Leaded Chip Carrier [LDCC]
(EJ-14-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADPA1113AEJZ	−40°C to +85°C	14-Lead LDCC (9.80 mm × 8.20 mm)	EJ-14-1

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Models[1]	Description
ADPA1113-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

Mouser Electronics

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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADPA1113AEJZ