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Evaluating the ADPA1107 45 dBm (35 W), GaN Power Amplifier, 4.8 GHz to 6.0 GHz

FEATURES

2-layer Rogers 4350B evaluation board with heat spreader
End launch 2.92 mm (K) jack RF connectors
Through calibration path
Drain or gate pulsing capability

EVALUATION KIT CONTENTS

ADPA1107-EVALZ evaluation board
30 V drain pulser board

EQUIPMENT NEEDED

Pulse generator
Oscilloscope
28 V, 3 A power supply
−4 V power supply
Tektronix TCPA312A current probe
Tektronix TCPA300 current probe amplifier
RF signal generator
Directional coupler
RF power sensor
RF power meter
RF attenuator

DOCUMENTS NEEDED

ADPA1107 data sheet

GENERAL DESCRIPTION

The ADPA1107-EVALZ consists of a 2-layer printed circuit board (PCB) fabricated from a 10 mil thick, Rogers 4350B copper clad mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow the spreader to be attached to a heat sink. Alternatively, the spreader can be clamped to a hot and cold plate. The RFIN and RFOUT ports on the ADPA1107-EVALZ are populated by 2.92 mm (K) female coaxial connectors, and the respective RF traces have a 50 Ω characteristic impedance. The ADPA1107-EVALZ is populated with components suitable for use over the entire operating temperature range of the device. To calibrate board trace losses, a through calibration path is provided between the J6 and J5 connectors. J6 and J5 must be populated with 2.92 mm (K) female coaxial connectors to use the through calibration path.

The ground, power, gate control, and detector output voltage are provided through two test points (TP1 and TP2) and two 24-pin headers (J3 and J4) on the ADPA1107-EVALZ. The pinouts for these four headers are detailed in Table 1.

RF traces on the ADPA1107-EVALZ are 50 Ω, grounded, coplanar waveguide. The package ground leads and the exposed pad connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground pad to provide adequate electrical conduction and thermal conduction to the heat spreader.

The ADPA1107-EVALZ ships with a drain pulsing board (pulser board) that can be plugged into the ADPA1107-EVALZ headers and configured to control the biasing of the ADPA1107 by providing a negative gate voltage and a control signal that connects and disconnects the drain voltage to the ADPA1107-EVALZ. The ADPA1107-EVALZ can also operate alone in gate pulsed mode where a negative pulse is applied to the VGG1 pin of the ADPA1107.

For full details on the ADPA1107, see the ADPA1107 data sheet, which must be consulted in conjunction with this user guide when using the ADPA1107-EVALZ.

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REVISION HISTORY

6/2021—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

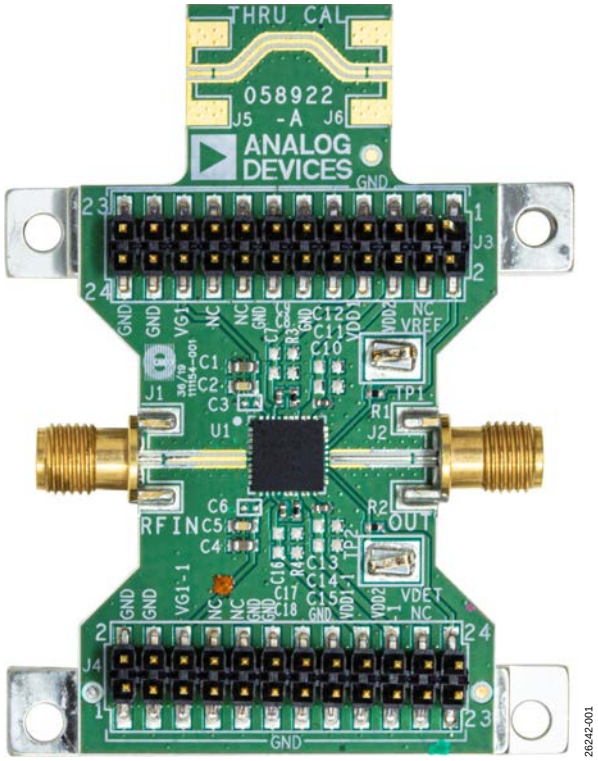

Figure 1. ADPA1107-EVALZ Evaluation Board, Primary Side

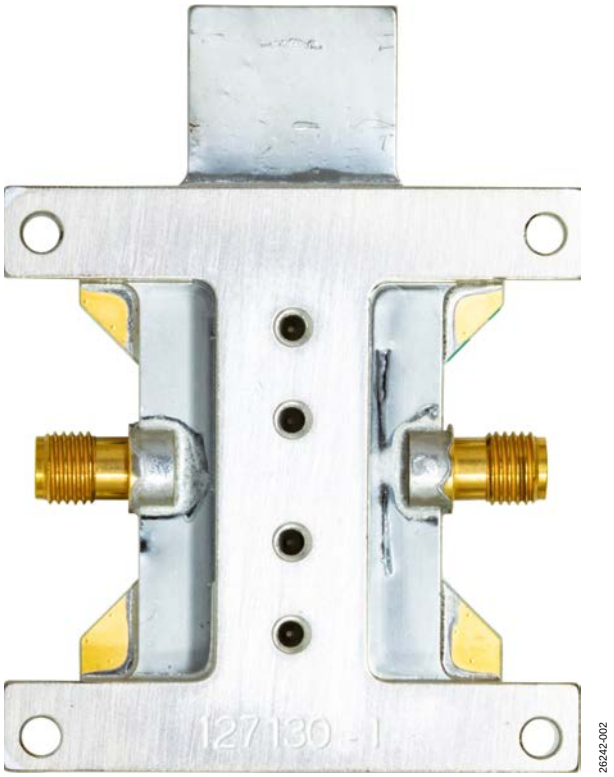

Figure 2. ADPA1107-EVALZ Evaluation Board, Secondary Side

HEADER PINOUT

The schematic for the ADPA1107-EVALZ is shown in Figure 6. The ADPA1107-EVALZ contains four headers, TP1, TP2, J3, and J4. Table 1 describes the pinout of these headers.

Table 1. TP1, TP2 J3, and J4 Header Connections on the ADPA1107-EVALZ

Header	Header Pin Number	Header Pin Name
TP1	Not applicable	VREF
TP2	Not applicable	VDET
J3	1, 3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	4, 16, 18	Not connected
	8	VDD1
	6	VDD2
	2	VREF_BIAS
	20	VG1
J4	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15, 16, 17, 19, 21, 23	GND
	8, 10, 22	Not connected
	6	VG1-1
	18	VDD1-1
	20	VDD2-1
	24	VDET_BIAS

INSERTION LOSS OF THE THROUGH CALIBRATION PATH

To calibrate board trace losses, a through calibration path is provided between the J6 and J5 connectors. J6 and J5 must be populated with 2.92 mm (K) connectors to use the through calibration path. Figure 3 shows the insertion loss, input return loss, and output return loss of the through calibration path. Table 2 lists the insertion loss of the through calibration path vs. frequency.

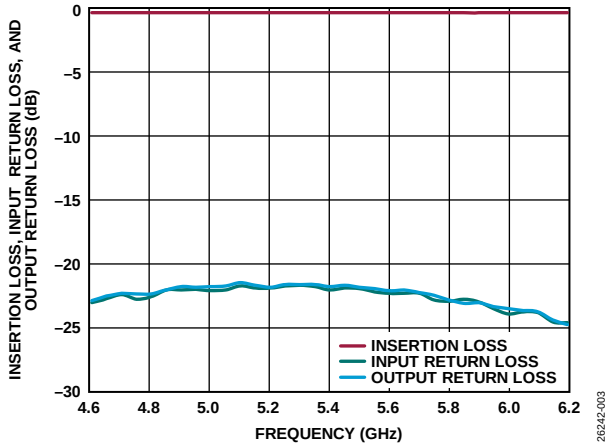

Figure 3. Insertion Loss, Input Return Loss, and Output Return Loss of Through Calibration Path vs. Frequency

Table 2. Insertion Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
4.6	–0.35
4.8	–0.37
5.0	–0.37
5.2	–0.38
5.4	–0.39
5.6	–0.38
5.8	–0.38
6.0	–0.39
6.2	–0.38

OPERATING THE ADPA1107-EVALZ WITH A PULSED GATE VOLTAGE

Remove C4, the 1 µF capacitor, to enable fast gate pulsing and apply a negative voltage pulse to the VGG1 input of the ADPA1107, while the voltage on the VDDxA/VDDxB pins of the ADPA1107 is held constant.

SETUP

All power supply, ground, and control signals are applied to the J3 and J4 headers of the ADPA1107-EVALZ. For this mode of operation, pulse the gate voltage between −4 V (off) and approximately −2.6 V (on) to set the quiescent current (I_{DQ}) to approximately 350 mA. The pulse width and duty cycle must be approximately 100 µs and 10%, respectively.

OPERATION

Take the following steps to power-up:

1. Set VDDx/VDDx-1 (Pin 6 and Pin 8 of J3, and Pin 18 and Pin 20 of J4) to 0 V.
2. Set VG1 (Pin 20 of J3) to off (VGG1 = −4 V).
3. Set supply voltage (V_{DD}) to 28 V.
4. Turn on the gate voltage pulse (VGG1 pulsing between −4 V and approximately −2.6 V).
5. Fine tune the pulse high voltage to achieve the desired I_{DQ} (nominally 350 mA) while maintaining the pulse off voltage level at −4 V.
6. Apply the RF input signal.

Take the following steps to power-down:

1. Turn off the RF signal.
2. Turn off the pulse to VGG1 (VGG1 = −4 V).
3. Set V_{DD} to 0 V.
4. Increase the pulse to VGG1 to 0 V.

OPERATING THE ADPA1107-EVALZ WITH THE DRAIN BIAS PULSER BOARD

The ADPA1107-EVALZ ships with a drain bias pulser board. A block diagram of the pulser board is shown in Figure 4. The pulser board has two primary components. The IRFZ48NSTRLPBF is an 55 V/64 A, metal-oxide semiconductor field effect transistor (MOSFET) that switches the drain voltage to the ADPA1107 on and off, and the MIC5021YN is a high-side, MOSFET, static switch driver that controls the IRFZ48NSTRLPBF MOSFET.

The pulser board plugs into the J3 and J4 headers of ADPA1107-EVALZ and can be configured to provide a pulsed drain voltage and a negative gate control voltage to control the biasing of the ADPA1107.

Table 3. J1 to J5, TP1 to TP4, P1, and P2 Pulser Board Connections to the ADPA1107

Header	Header Pin Number	Header Pin Name
J1	Not applicable	VDD
J2	Not applicable	SENSE
J3	Not applicable	VG1
J4	Not applicable	Pulse
J5	Not applicable	PULSED_VDD
VREFBIAS	Not applicable	VREFBIAS
VREF	Not applicable	VREF
VDET	Not applicable	VDET
VDETBIAS	Not applicable	VDETBIAS
P1	1	VDET
	2	VDET_BIAS
	3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	4, 6, 8	PULSED_VDD
	16, 18, 20	VG1
P2	1, 2, 3, 4, 5, 7, 9 ,11, 12, 13, 14, 15, 16, 17, 19, 21	GND
	6, 8, 10	VG1
	18, 20, 22	PULSED_VDD
	23	VREF
	24	VREF_BIAS

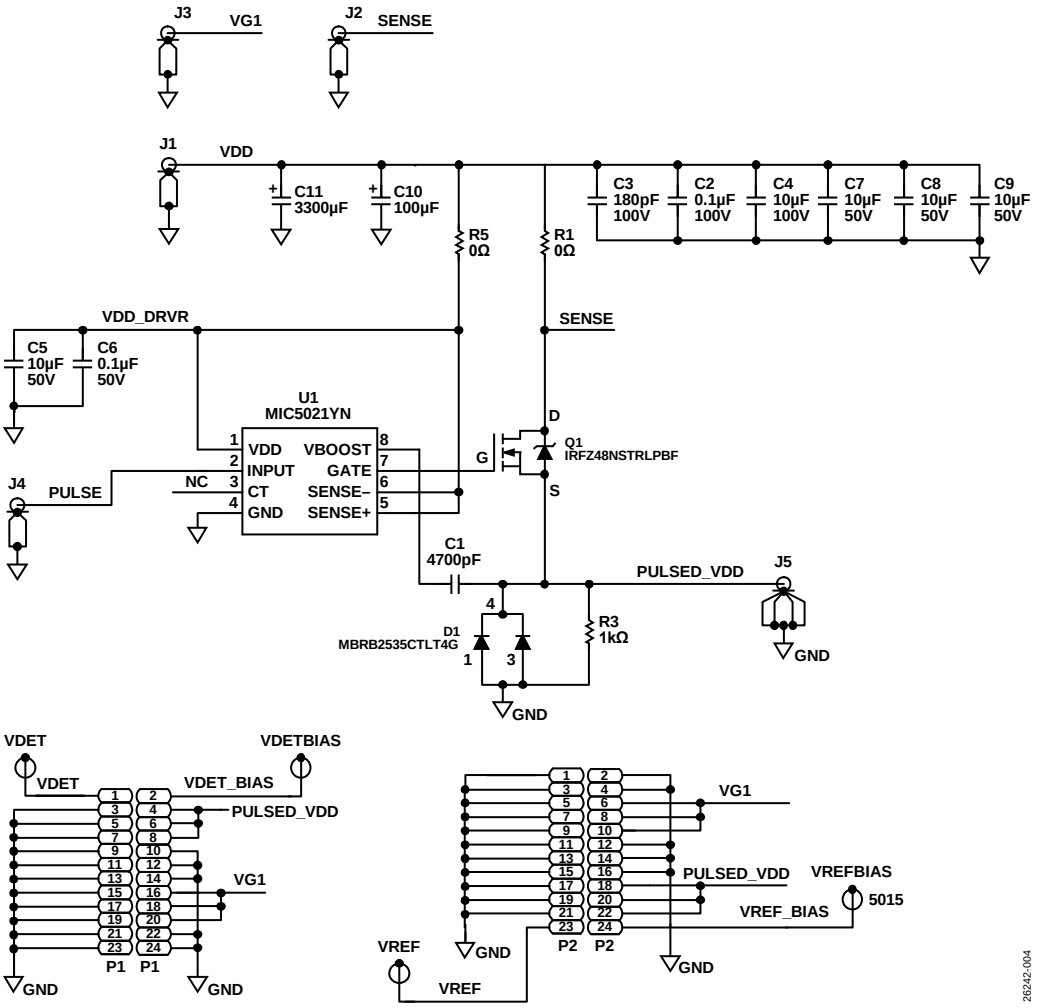

Figure 4. Analog Devices, Inc., Pulser Board Schematic

SETUP

The connections required to use the ADPA1107-EVALZ with the drain bias pulser board are shown in Figure 5. Before applying any bias or signals, plug the pulser board into the ADPA1107-EVALZ so that the P1 header connector of the pulser board connects to the J3 header of the ADPA1107-EVALZ, and the pulser board P2 header connects to the J4 header of the ADPA1107-EVALZ. All external supply voltages and control signals are applied to the pulser board through the J1 through J4 connectors, which are listed in Table 3.

The gate control voltage applied to the J4 connector, passes directly through the pulser board and drives the VGG1 pin of the ADPA1107. Because the VDD and GND lines carry currents up to 2 A, the use of heavy gauge twisted pair wires is recommended to minimize voltage drops. To observe the pulsed drain voltage (PULSED_VDD) that drives the VDDxA/VDDxB pins of the ADPA1107, connect an oscilloscope to the J5 coaxial connector on the pulser board.

Connect a digital pulse generator that can generate 0 V to 5 V pulses with a pulse width of 100 µs and a duty cycle of 10% to the J4 connector.

To observe and measure the drain current and the RF output power of the ADPA1107, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as described in the Making Average to Pulsed Approximations section.

OPERATION

Take the following steps to power-up (unless otherwise stated, all signals are applied to the pulser board):

1. Set the voltage on the J4 connector, PULSE, to 0 V.
2. Set the voltage on the J3 connector, VG1, to −4 V.
3. Set the voltage on the J1 connector, VDD, to 28 V.
4. Turn on the J4 connector, PULSE (0 V/5 V, 100 µs, 10% duty cycle).
5. Increase the voltage on the J3 connector, VG1, (nominally −2.6 V) until the target I_{DQ} is reached (nominally 350 mA).
6. Apply the RF input signal to the RFIN connector of the ADPA1107-EVALZ.

Take the following steps to power-down:

1. Turn off the RF input signal.
2. Set the voltage on the J3 connector, VG1, to −4 V.
3. Turn off the J4 connector, PULSE (set to 0 V).
4. Set the voltage on the J1 connector, VDD, to 0 V.
5. Set the voltage on the J3 connector, VG1, to 0 V.

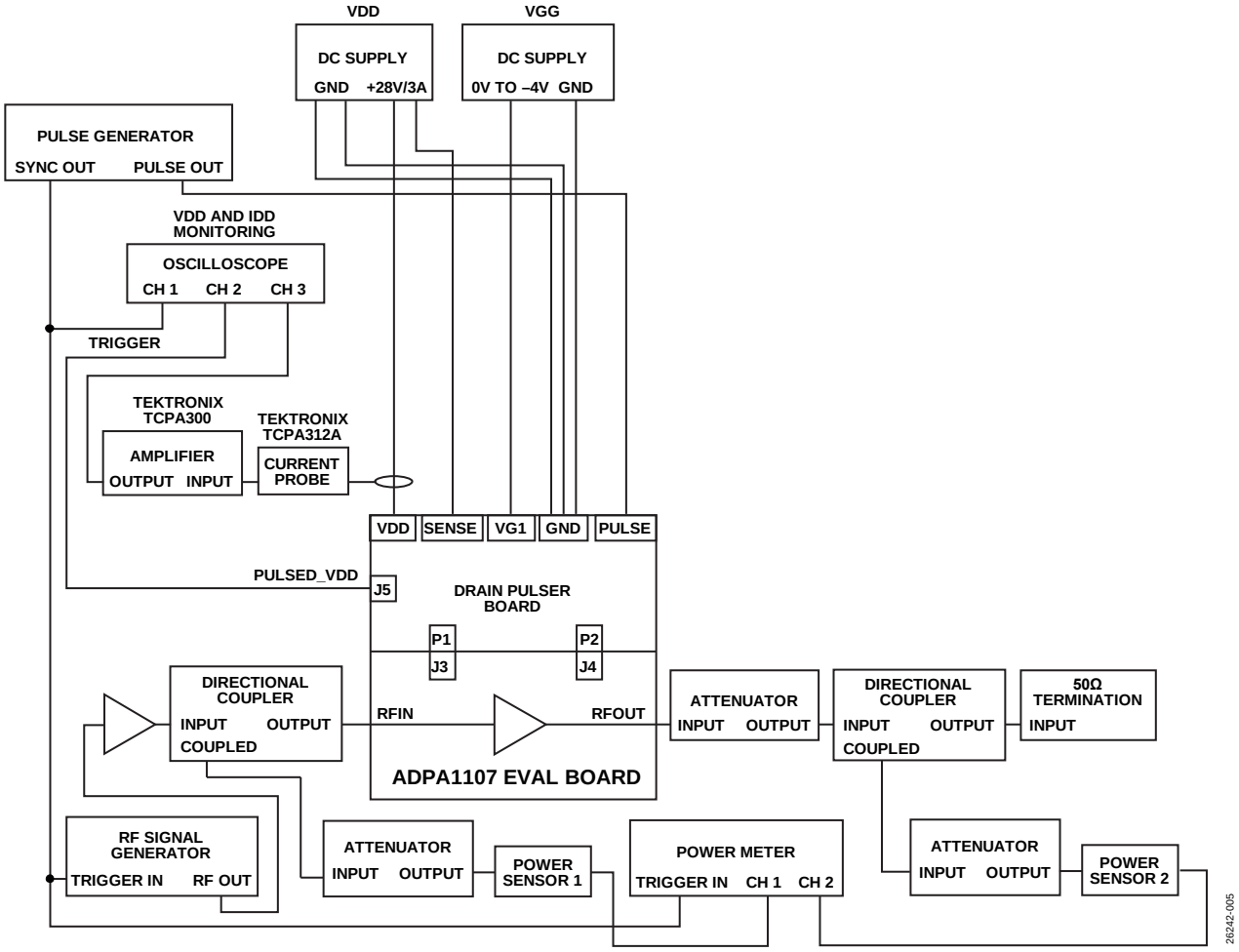

Figure 5. Setup Block Diagram

MAKING AVERAGE TO PULSED APPROXIMATIONS

Instruments that can be triggered are required to measure the RF power, drain current, and power added efficiency (PAE) accurately under pulsed operation. When such instrumentation is not available, use averaging and approximations. The most common approximations involve measuring the average values and then adjusting those values to account for the duty cycle. These approximations can result in errors because of limited measurement bandwidths of instruments and/or the inclusion of on and off transients and/or partial periods in the measurement.

To ensure that partial periods do not contribute significant errors to the measurements, perform averaging over a large number of pulse periods. The results of such approximations can vary with the instruments and settings used. Therefore, experimentation can be necessary to achieve credible and repeatable results. When it is not possible to make pulse triggered measurements, the only pulse connection required is the connection from the pulse generator to the J4 connector of the pulser (see Figure 5).

EVALUATION BOARD SCHEMATIC AND ARTWORK

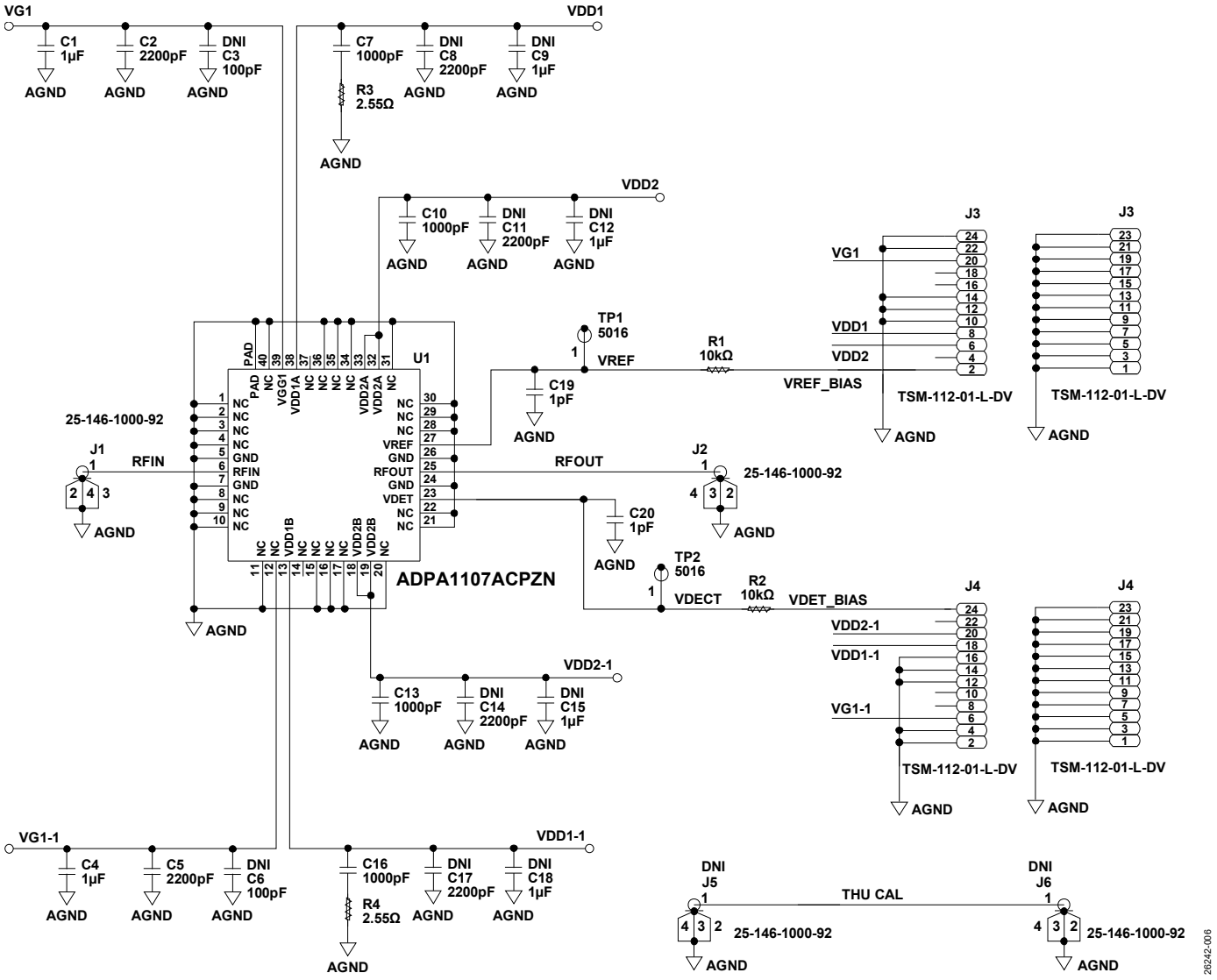

Figure 6. ADPA1107-EVALZ Evaluation Board Schematic

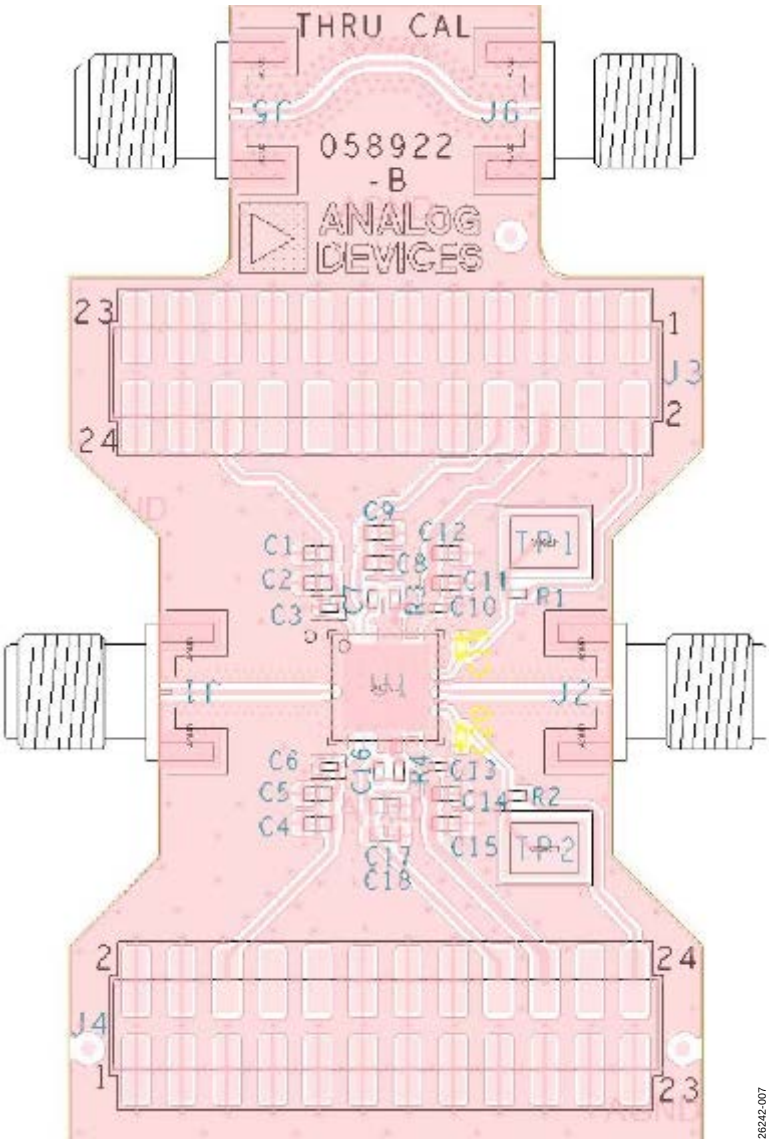

Figure 7. ADPA1107-EVALZ Assembly Drawing (J6 and J5 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description	Manufacturer	Part Number
C1, C4	1 µF capacitors, 50 V, 10%, X7R, 0603	Taiyo Yuden	UMK107AB7105KA-T
C2, C5	2200 pF capacitors, 50 V, 10%, X7R, 0603	Samsung	CL10B222KB8NNNC
C7, C10, C13, C16	1000 pF capacitors, 50 V, 5%, C0G, 0402	Murata	GRM1555C1H102JA01
C19, C20	1 pF capacitors, 25 V, 0.1 pF, C0G, 0402	AVX	04023A1R0BAT2A
J1, J2	Connectors, Type K, jack edge	Winchester Connector.	25-146-1000-92
J3, J4	PCB connector headers, 24-position male headers, unshrouded double row, surface-mount technology (SMT), 2.54 mm pitch	SAMTEC INC.	TSM-112-01-L-DV
R1, R2	10 kΩ resistors, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1002X
R3, R4	2.55 Ω resistors, 1%, 1/16 W, 0402, AEC-Q200	Vishay	CRCW04022R55FNED
TP1, TP2	PCB connectors SMT test points	Keystone Electronics	5016
U1	35 W, 4.8 GHz to 6.0 GHz, GaN power amplifier	Analog Devices	ADPA1107ACPZN
Not Applicable	Aluminum heatsink, 2.51 in × 1.91 in	Not applicable	Not applicable
J5, J6	Connectors, K, jack edge, do not install (DNI)	Winchester Connector.	25-146-1000-92
C3, C6	100 pF capacitors, 50 V, 5%, COG, 0402, DNI	KEMET	C0402C101J5GACTU
C8, C11, C14, C17	2200 pF capacitors, 50 V, 10%, X7R, 0603, DNI	Samsung	CL10B222KB8NNNC
C9, C12, C15, C18	1 µF capacitors, 50 V, 10%, X7R, 0603, DNI	Taiyo Yuden	UMK107AB7105KA-T

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