

FEATURES

- Input voltage range: 2.3 V to 5.5 V**
- One 800 mA buck regulator**
- One 300 mA LDO**
- 20-lead, 4 mm × 4 mm LFCSP package**
- Initial regulator accuracy: ±1%**
- Overcurrent and thermal protection**
- Soft start**
- Undervoltage lockout**
- Open-drain processor reset with threshold monitoring**
- ±1.5% threshold accuracy over the full temperature range**
- Guaranteed reset output valid to $V_{CC} = 1$ V**
- Dual watchdog for secure systems**
 - Watchdog 1 controls reset
 - Watchdog 2 controls reset and regulators power cycle
- Buck regulator key specifications**
 - Current-mode topology for excellent transient response
 - 3 MHz operating frequency
 - Uses tiny multilayer inductors and capacitors
 - Mode pin selects forced PWM or auto PFM/PSM modes
 - 100% duty cycle low dropout mode
- LDO key specifications**
 - Low V_{IN} from 1.7 V to 5.5 V
 - Stable with 1 μ F ceramic output capacitors
 - High PSRR, 60 dB up to 1 kHz/10 kHz
 - Low output noise
 - Low dropout voltage: 150 mV at 300 mA load
 - −40°C to +125°C junction temperature range

GENERAL DESCRIPTION

The ADP5043 combines one high performance buck regulator and one low dropout (LDO) regulator in a small 20-lead LFCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulator enables use of tiny multilayer external components and minimizes board space.

The MODE pin selects the buck's mode of operation. When set to logic high, the buck regulator operates in forced PWM mode. When the MODE pin is set to logic low, the buck regulator operates in PWM mode when the load is around the nominal value. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM) improving the light-load efficiency.

The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5043 LDO extend the battery life of portable devices. The LDO maintains a power supply rejection of greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Each regulator is activated by a high level on the respective enable pin. The ADP5043 is available with factory programmable default output voltages and can be set to a wide range of options.

The ADP5043 contains supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. The ADP5043 also provides power-on reset signals. An on-chip dual watchdog timer can reset the microprocessor or power cycle the system (Watchdog 2) if it fails to strobe within a preset timeout period.

HIGH LEVEL BLOCK DIAGRAM

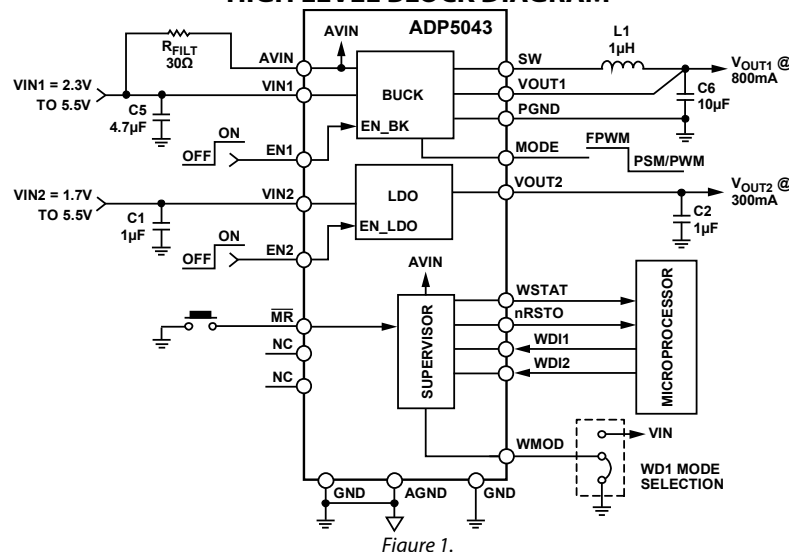


Figure 1.

Rev. C

Document Feedback

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REVISION HISTORY

9/2019—Rev. B to Rev. C

Changes to Output Capacitor Section	22
Updated Outline Dimensions	30

5/2018—Rev. A to Rev. B

Updated Outline Dimensions	30
Changes to Ordering Guide	30

10/2011—Rev. 0 to Rev. A

Updated Outline Dimensions	30
Changes to Ordering Guide	30

4/2011—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

AVIN, VIN1 = ($V_{OUT1} + 0.5\text{ V}$) or 2.3 V, whichever is greater, AVIN, VIN1 $\geq$ VIN2, $T_A = 25^\circ\text{C}$, unless otherwise noted. Regulators are enabled.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AVIN UNDERVOLTAGE LOCKOUT	UVLO _{AVIN}	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$				
Input Voltage Rising	UVLO _{AVINRISE}				2.25	V
Option A					3.9	V
Option B						
Input Voltage Falling	UVLO _{AVINFALL}		1.95			V
Option A			3.1			V
Option B						
SHUTDOWN CURRENT	I _{GND-SD}	ENx = GND ENx = GND, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.1		μA
Thermal Shutdown Threshold	TS _{SD}	T_J rising		150	2	$^\circ\text{C}$
Thermal Shutdown Hysteresis	TS _{SD-HYS}			20		$^\circ\text{C}$
ENx, WDIx, MODE, WMOD, $\overline{\text{MR}}$ INPUTS						
Input Logic High	V _{IH}	$2.5\text{ V} \leq \text{AVIN} \leq 5.5\text{ V}$	1.2			V
Input Logic Low	V _{IL}	$2.5\text{ V} \leq \text{AVIN} \leq 5.5\text{ V}$			0.4	V
Input Leakage Current (WMOD Excluded)	V _{I-LEAKAGE}	ENx = AVIN or GND		0.05		μA
		ENx = AVIN or GND, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$			1	μA
WMOD Input Leakage Current	V _{I-LKG-WMOD}	V _{WMOD} = 3.6 V, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$			50	μA
OPEN-DRAIN OUTPUTS						
nRSTO, WSTAT Output Voltage	V _{OL}	AVIN = 2.3 V to 5.5 V, I _{nRSTO/WSTAT} = 3 mA		30		mV
Open-Drain Reset Output Leakage Current					1	μA

SUPERVISORY SPECIFICATIONS

AVIN, VIN1 = full operating range, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
Supply Current (Supervisory Circuit Only)		45	55	μA	AVIN = 5.5 V, EN1 = EN2 = VIN1
		43	52	μA	AVIN = 3.6 V, EN1 = EN2 = VIN1
RESET THRESHOLD ACCURACY	V _{TH} – 0.8% V _{TH} – 1.5%	V _{TH}	V _{TH} + 0.8% V _{TH} + 1.5%	V	$T_A = 25^\circ\text{C}$, sensed on V _{OUTx}
				V	$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, sensed on V _{OUTx}
RESET THRESHOLD TO OUTPUT DELAY GLITCH IMMUNITY (t _{UOD})	50	125	400	μs	V _{TH} = V _{OUT} – 50 mV
RESET TIMEOUT PERIOD WATCHDOG1 (t _{RP1})					
Option A	24	30	36	ms	
Option B	160	200	240	ms	
RESET TIMEOUT PERIOD WATCHDOG2 (t _{RP2})	3.5	5	7	ms	
V _{CC} TO RESET DELAY (t _{RD})		150		μs	VIN1 falling at 1 mV/ μs
REGULATORS SEQUENCING DELAY (t _{D1} , t _{D2})		2		ms	
WATCHDOG INPUTS					
Watchdog 1 Timeout Period (t _{WD1})					
Option A	81.6	102	122.4	ms	
Option B	1.28	1.6	1.92	sec	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Watchdog 2 Timeout Period (t_{WD2})					
Option A	6	7.5	9	sec	
Option B		Watchdog 2 disabled			
Option C	3.2	4	4.8	min	
Option D	6.4	8	9.6	min	
Option E	11.2	16	19.2	min	
Option F	25.6	32	38.4	min	
Option G	51.2	64	76.8	min	
Option H	102.4	128	153.8	min	
Watchdog 2 Power Off Period (t_{POFF})					
Option A		210		ms	
Option B		400		ms	
WDI1 Pulse Width	80			ns	$V_{IL} = 0.4\text{ V}$, $V_{IH} = 1.2\text{ V}$
WDI2 Pulse Width	8			μs	$V_{IL} = 0.4\text{ V}$, $V_{IH} = 1.2\text{ V}$
Watchdog Status Timeout Period ($t_{WDCLEAR}$)		11.2		sec	
WDI1 Input Current (Source)	8	15	20	μA	$V_{WDI1} = V_{CC}$, time average
WDI1 Input Current (Sink)	-30	-25	-14	μA	$V_{WDI1} = 0$, time average
WDI2 Internal Pull-Down		45		$\text{k}\Omega$	
MANUAL RESET INPUT					
$\overline{\text{MR}}$ Input Pulse Width	1			μs	
$\overline{\text{MR}}$ Glitch Rejection		220		ns	
$\overline{\text{MR}}$ Pull-Up Resistance	25	52	80	$\text{k}\Omega$	
$\overline{\text{MR}}$ to Reset Delay		280		ns	$V_{CC} = 5\text{ V}$

BUCK SPECIFICATIONS

AVIN, VIN1 = 3.6 V, V_{OUT1} = 1.8 V, T_J = -40°C to +125°C for minimum/maximum specifications, L = 1 μH, C_{OUT} = 10 μF, and T_A = 25°C for typical specifications, unless otherwise noted.¹

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range (VIN1)		2.3		5.5	V
OUTPUT CHARACTERISTICS					
Output Voltage Accuracy	PWM mode, I _{LOAD} = 100 mA	-1		+1	%
	PSM mode	-2		+2	%
	VIN1 = 2.3 V to 5.5 V, PWM mode, I _{LOAD} = 1 mA to 800 mA	-3		+3	%
PWM TO POWER SAVE MODE CURRENT THRESHOLD			100		mA
INPUT CURRENT CHARACTERISTICS					
DC Operating Current	I _{LOAD} = 0 mA, device not switching		21	35	μA
Shutdown Current	ENx = 0 V, T _A = T _J = -40°C to +125°C		0.2	1.0	μA
SW CHARACTERISTICS					
SW On Resistance	PFET		180	240	mΩ
	PFET, AVIN = VIN1 = 5 V		140	190	mΩ
	NFET		170	235	mΩ
	NFET, AVIN = VIN1 = 5 V		150	210	mΩ
Current Limit	PFET switch peak current limit	1100	1360	1600	mA
ACTIVE PULL-DOWN	EN1 = 0 V		75		Ω
OSCILLATOR FREQUENCY		2.5	3.0	3.5	MHz
START-UP TIME			250		μs

¹ All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

LDO SPECIFICATIONS

AVIN = 3.6 V, VIN2 = (V_{OUT2} + 0.2 V) or 2.3 V, whichever is greater; AVIN, VIN1 ≥ VIN2; I_{OUT} = 10 mA; C_{IN} = C_{OUT} = 1 μF; T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V _{IN2}	T _J = -40°C to +125°C	1.7		5.5	V
OPERATING SUPPLY CURRENT (per LDO)	I _{GND}	I _{OUT} = 0 μA, V _{OUT} = 3.3 V		15		μA
		I _{OUT} = 0 μA, V _{OUT} = 3.3 V, T _J = -40°C to +125°C			50	μA
		I _{OUT} = 10 mA		67		μA
		I _{OUT} = 10 mA, T _J = -40°C to +125°C			105	μA
		I _{OUT} = 200 mA		100		μA
		I _{OUT} = 200 mA, T _J = -40°C to +125°C			245	μA
FIXED OUTPUT VOLTAGE ACCURACY	V _{OUT2}	I _{OUT} = 10 mA	-1		+1	%
		100 μA < I _{OUT} < 300 mA	-2		+2	%
		VIN2 = (V _{OUT2} + 0.5 V) to 5.5 V				
		100 μA < I _{OUT} < 300 mA	-3		+3	%
		VIN2 = (V _{OUT2} + 0.5 V) to 5.5 V				
		T _J = -40°C to +125°C				

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
REGULATION						
Line Regulation	$\Delta V_{OUT2}/\Delta V_{IN2}$	VIN2 = (VOUT2 + 0.5 V) to 5.5 V I _{OUT2} = 1 mA T _J = -40°C to +125°C	-0.03		+0.03	%/V
Load Regulation ¹	$\Delta V_{OUT2}/\Delta I_{OUT2}$	I _{OUT2} = 1 mA to 200 mA I _{OUT2} = 1 mA to 200 mA T _J = -40°C to +125°C		0.002	0.0075	%/mA %/mA
DROPOUT VOLTAGE ²	V _{DROPOUT}	VOUT2 = 3.3 V I _{OUT2} = 10 mA I _{OUT2} = 10 mA, T _J = -40°C to +125°C I _{OUT2} = 200 mA I _{OUT2} = 200 mA, T _J = -40°C to +125°C		4 60	5 100	mV mV mV mV
ACTIVE PULL-DOWN	R _{PDLDO}	EN2 = 0 V		600		Ω
START-UP TIME	T _{START-UP}	VOUT2 = 3.3 V		85		μs
CURRENT-LIMIT THRESHOLD ³	I _{LIMIT}	T _J = -40°C to +125°C	335	470		mA
OUTPUT NOISE	OUT _{LDO} NOISE	10 Hz to 100 kHz, VIN2 = 5 V, VOUT2 = 3.3 V 10 Hz to 100 kHz, VIN2 = 5 V, VOUT2 = 2.8 V 10 Hz to 100 kHz, VIN2 = 5 V, VOUT2 = 1.5 V		123 110 59		μV rms μV rms μV rms
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, VIN2 = 3.3 V, VOUT2 = 2.8 V, I _{OUT} = 100 mA 100 kHz, VIN2 = 3.3 V, VOUT2 = 2.8 V, I _{OUT} = 100 mA 1 MHz, VIN2 = 3.3 V, VOUT2 = 2.8 V, I _{OUT} = 100 mA		66 57 60		dB dB dB

¹ Based on an end-point calculation using 1 mA and 100 mA loads.

² Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.3 V.

³ Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CAPACITANCE (BUCK) ¹	C _{MIN1}	T _J = -40°C to +125°C	7		40	μF
MINIMUM INPUT AND OUTPUT CAPACITANCE ² (LDO)	C _{MIN2}	T _J = -40°C to +125°C	0.70			μF
CAPACITOR ESR	R _{ESR}	T _J = -40°C to +125°C	0.001		1	Ω

¹ The minimum output capacitance should be greater than 4.7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met.

² The minimum input and output capacitance should be greater than 0.70 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, Y5V and Z5U capacitors are not recommended for use with LDOs or the buck.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVIN, VINx, VOUTx, ENx, MODE, MR, WDIx, WMOD, WSTAT, nRSTO to GND	–0.3 V to +6 V
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Soldering Conditions	JEDEC J-STD-020
ESD Human Body Model	3000 V
ESD Charged Device Model	1500 V
ESD Machine Model	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP5043 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package. Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified value of θ_{JA} is based on a four-layer, 4 inch × 3 inch, 2.5 oz copper board, as per JEDEC standard. For additional information, see the [AN-772](#) Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale (LFCSP)*.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

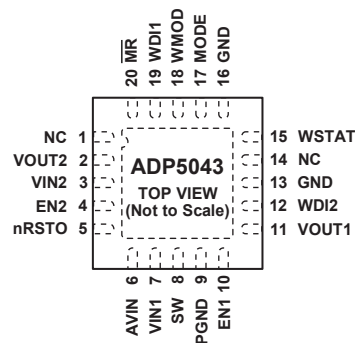
Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead, 0.5 mm pitch LFCSP	38	4.2	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. EXPOSED PAD SHOULD BE CONNECTED TO AGND.
2. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN. THE PIN SHOULD BE LEFT FLOATING.

09682-002

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 14	NC	No Connect. Do not connect to this pin. The pin should be left floating.
2	VOUT2	LDO Output Voltage and Sensing Input.
3	VIN2	LDO Input Supply (1.7 V to 5.5 V).
4	EN2	Enable LDO. EN2 = high: turn on the LDO; EN2 = low: turn off the LDO.
5	nRSTO	Open-Drain Reset Output, Active Low.
6	AVIN	Regulators Housekeeping and Supervisory Input Supply (2.3 V to 5.5 V).
7	VIN1	Buck Input Supply (2.3 V to 5.5 V).
8	SW	Buck Switching Node.
9	PGND	Dedicated Power Ground for Buck Regulator.
10	EN1	Enable Buck. EN1 = high: turn on buck; EN1 = low: turn off buck.
11	VOUT1	Buck Sensing Node.
12	WDI2	Watchdog 2 (Long Timeout) Refresh Input from Processor. This pin can be disabled only by a factory option.
13, 16	GND	Connect to the ground plane.
15	WSTAT	Open-Drain Watchdog Timeout Status. WSTAT = high: Watchdog 1 timeout or power-on reset; WSTAT = low: Watchdog 2 timeout. Auto cleared after one second.
17	MODE	Buck Mode. MODE = high: buck regulator operates in fixed PWM mode; MODE = low: (auto mode) buck regulator operates in power save mode (PSM) at light load and in constant PWM at higher load.
18	WMOD	Watchdog Mode. WMOD = low: Watchdog 1 normal mode; WMOD = high: Watchdog 1 cannot be disabled by a three-state condition applied on WDI1. WMOD has an internal 200 kΩ pull-down resistor connected to AGND.
19	WDI1	Watchdog 1 Refresh Input from Processor. If WDI1 is in high-Z and WMOD is low, Watchdog 1 is disabled.
20	MR	Manual Reset Input, Active Low.
	EPAD	Exposed Pad. The exposed pad should be connected to analog ground (AGND).

TYPICAL PERFORMANCE CHARACTERISTICS

VIN1 = VIN2 = AVIN = 5.0 V, T_A = 25°C, unless otherwise noted.

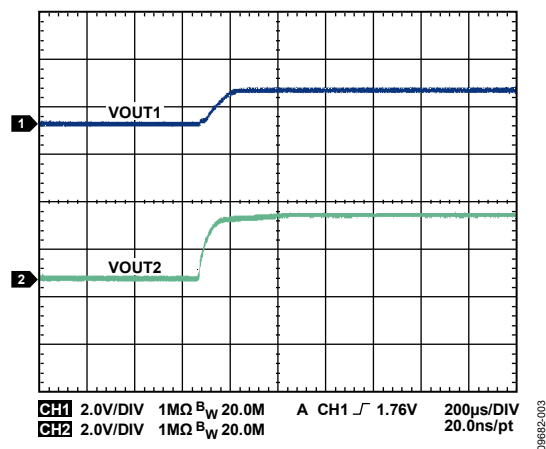


Figure 3. 3-Channel Start-Up Waveforms

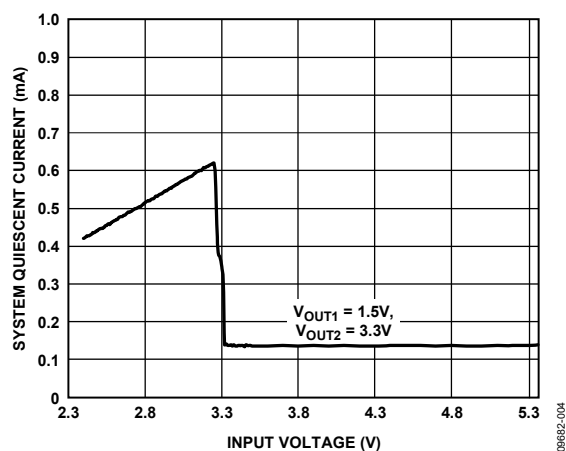


Figure 4. System Quiescent Current (Sum of All the Input Currents) vs. Input Voltage, V_{OUT1} = 1.5 V, V_{OUT2} = 3.3 V

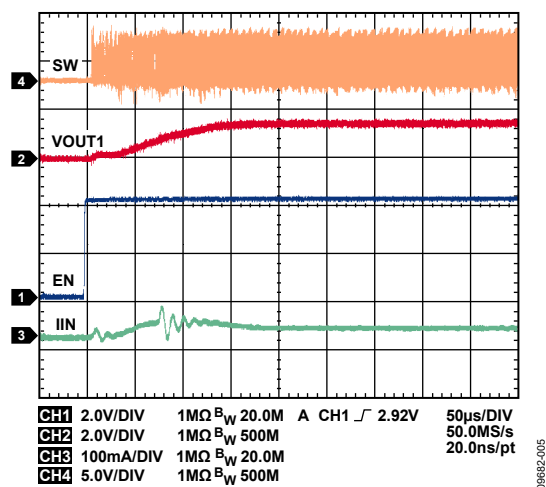


Figure 5. Buck Startup, V_{OUT1} = 1.8 V, I_{OUT1} = 20 mA

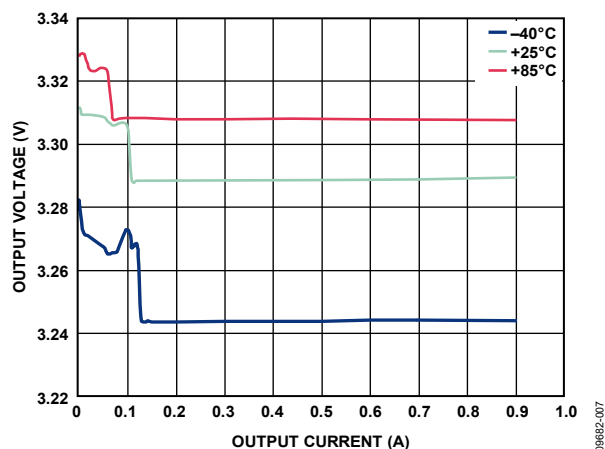


Figure 6. Buck Load Regulation Across Temperature, V_{OUT1} = 3.3 V, Auto Mode

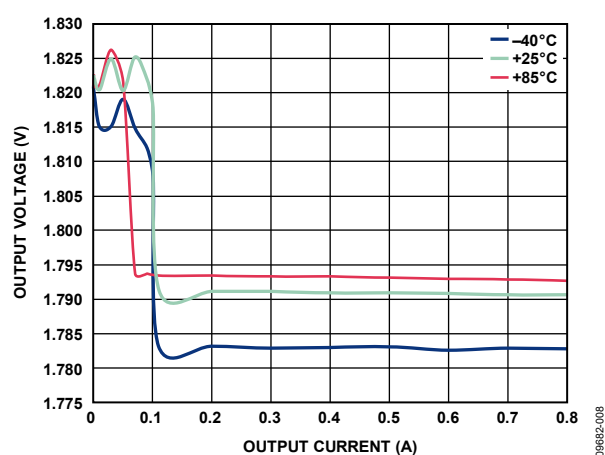


Figure 7. Buck Load Regulation Across Temperature, V_{OUT1} = 1.8 V, Auto Mode

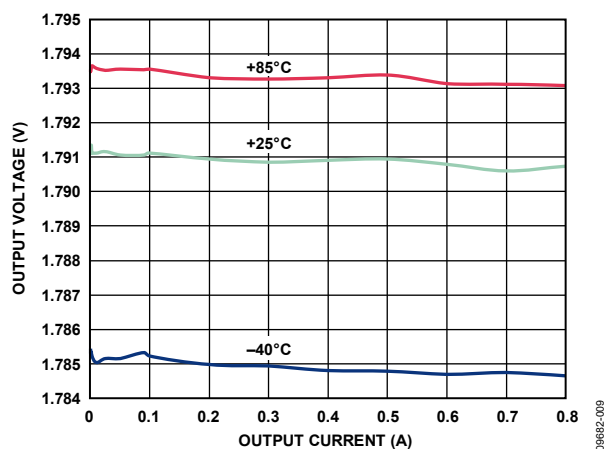


Figure 8. Buck Load Regulation Across Temperature, V_{OUT1} = 1.8 V, PWM Mode

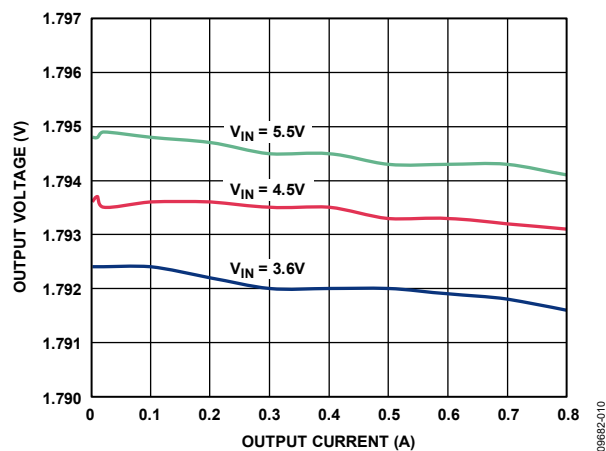


Figure 9. Buck Load Regulation Across Input Voltage,
 $V_{OUT1} = 1.8\text{ V}$, PWM Mode

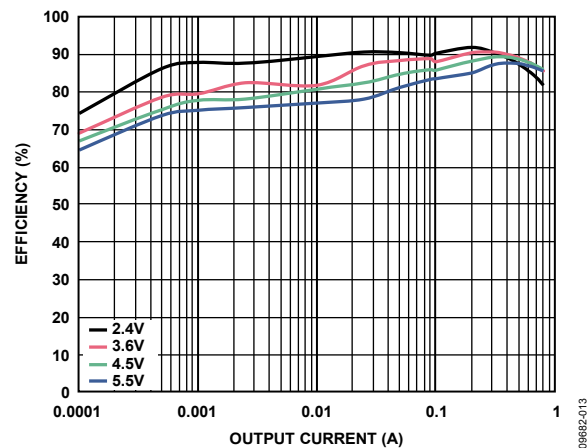


Figure 12. Buck Efficiency vs. Load Current, Across Input Voltage,
 $V_{OUT1} = 1.8\text{ V}$, Auto Mode

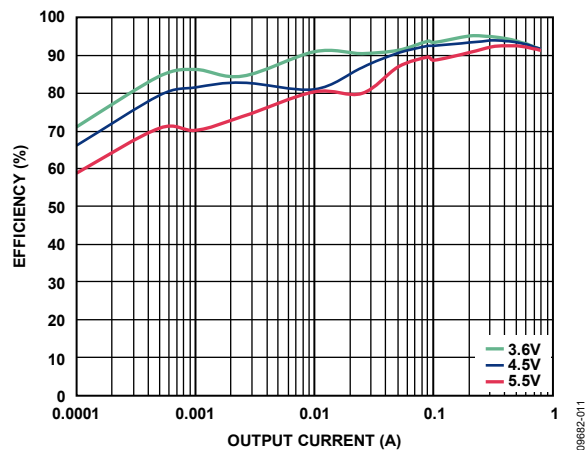


Figure 10. Buck Efficiency vs. Load Current, Across Input Voltage,
 $V_{OUT1} = 3.3\text{ V}$, Auto Mode

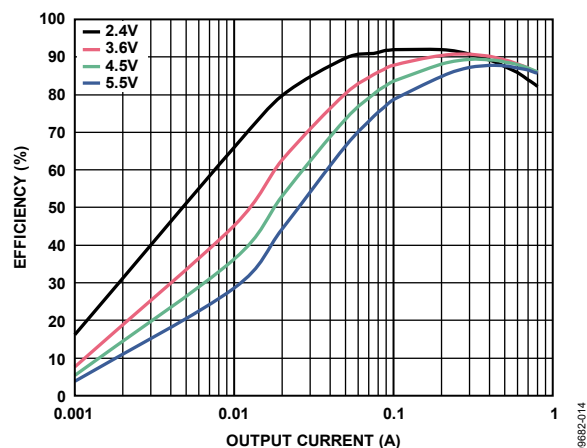


Figure 13. Buck Efficiency vs. Load Current, Across Input Voltage,
 $V_{OUT1} = 1.8\text{ V}$, PWM Mode

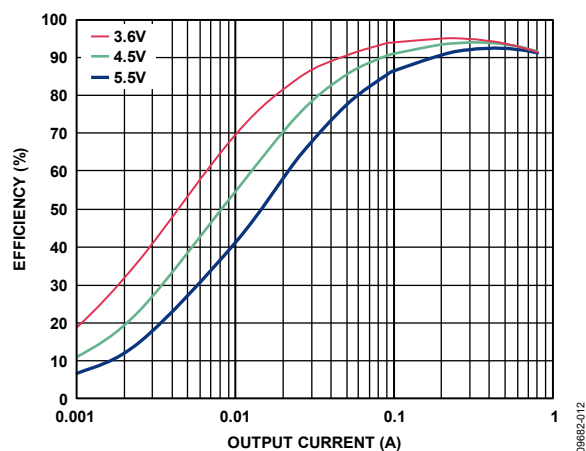


Figure 11. Buck Efficiency vs. Load Current, Across Input Voltage,
 $V_{OUT1} = 3.3\text{ V}$, PWM Mode

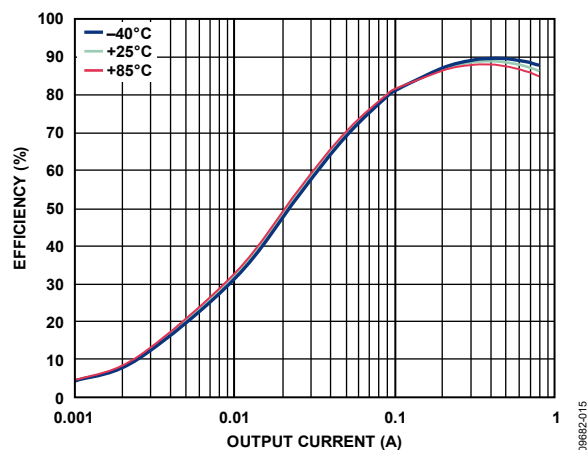


Figure 14. Buck Efficiency vs. Load Current, Across Temperature,
 $V_{OUT1} = 1.8\text{ V}$, PWM Mode

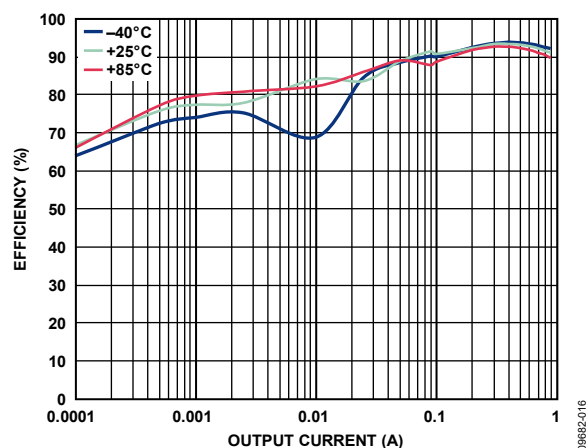


Figure 15. Buck Efficiency vs. Load Current, Across Temperature, $V_{OUT1} = 3.3\text{ V}$, Auto Mode

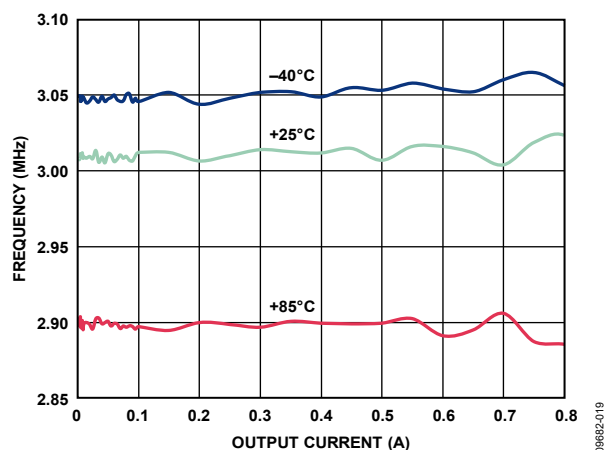


Figure 18. Buck Switching Frequency vs. Output Current, Across Temperature, $V_{OUT1} = 1.8\text{ V}$, PWM Mode

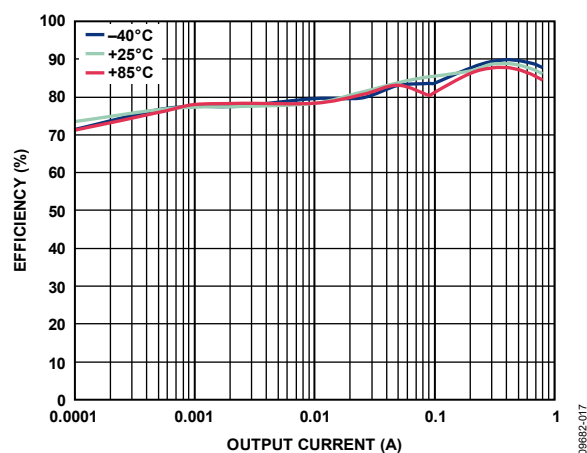


Figure 16. Buck Efficiency vs. Load Current, Across Temperature, $V_{OUT1} = 1.8\text{ V}$, Auto Mode

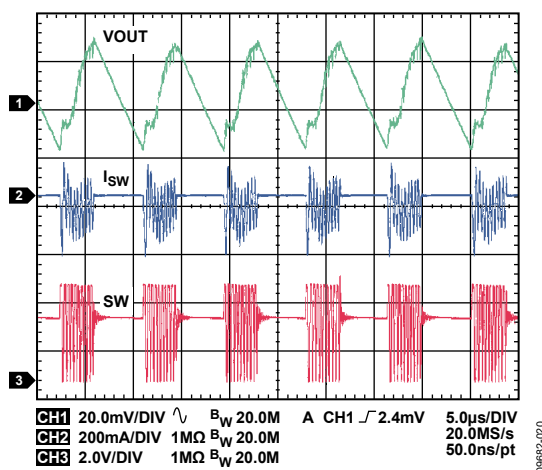


Figure 19. Typical Waveforms, $V_{OUT1} = 3.3\text{ V}$, $I_{OUT1} = 30\text{ mA}$, Auto Mode

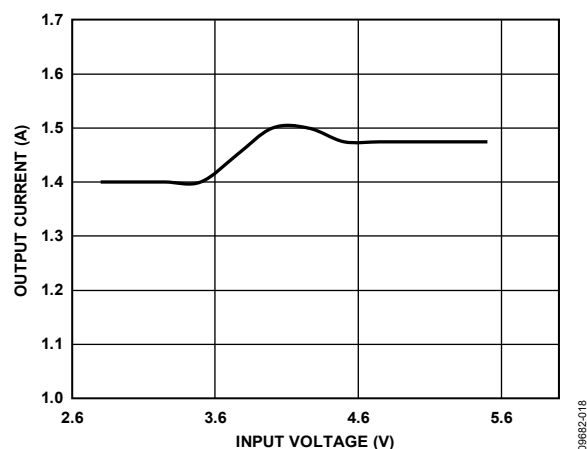


Figure 17. Buck DC Current Capability vs. Input Voltage, $V_{OUT1} = 1.8\text{ V}$

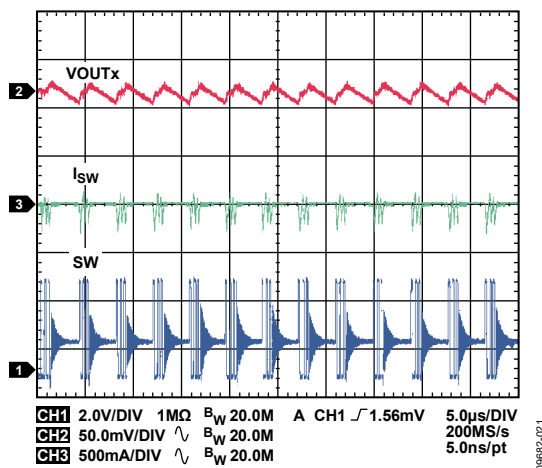


Figure 20. Typical Waveforms, $V_{OUT1} = 1.8\text{ V}$, $I_{OUT1} = 30\text{ mA}$, Auto Mode

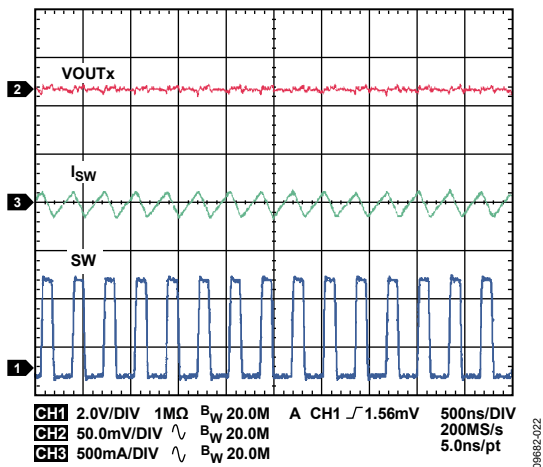


Figure 21. Typical Waveforms, $V_{OUT1} = 1.8\text{ V}$, $I_{OUT1} = 30\text{ mA}$, PWM Mode

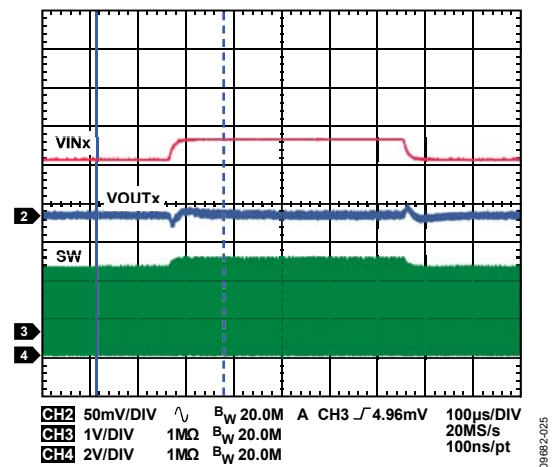


Figure 24. Buck Response to Line Transient, $V_{IN} = 4.5\text{ V}$ to 5.0 V , $V_{OUT1} = 1.8\text{ V}$, PWM Mode

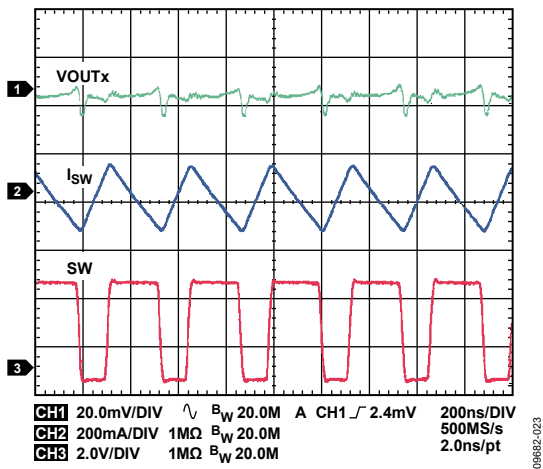


Figure 22. Typical Waveforms, $V_{OUT1} = 3.3\text{ V}$, $I_{OUT1} = 30\text{ mA}$, PWM Mode

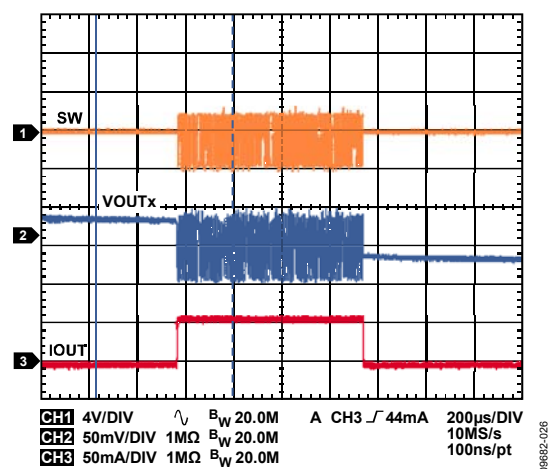


Figure 25. Buck Response to Load Transient, I_{OUT1} from 1 mA to 50 mA , $V_{OUT1} = 3.3\text{ V}$, Auto Mode

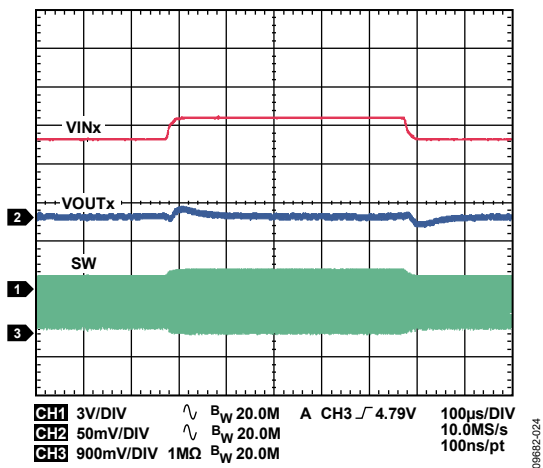


Figure 23. Buck Response to Line Transient, Input Voltage from 4.5 V to 5.0 V , $V_{OUT1} = 3.3\text{ V}$, PWM Mode

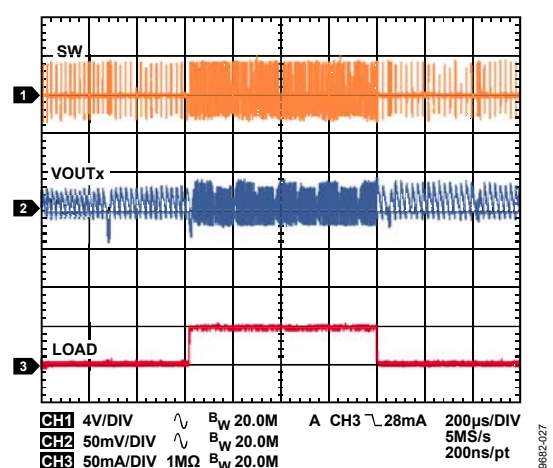


Figure 26. Buck Response to Load Transient, I_{OUT2} from 1 mA to 50 mA , $V_{OUT1} = 1.8\text{ V}$, Auto Mode

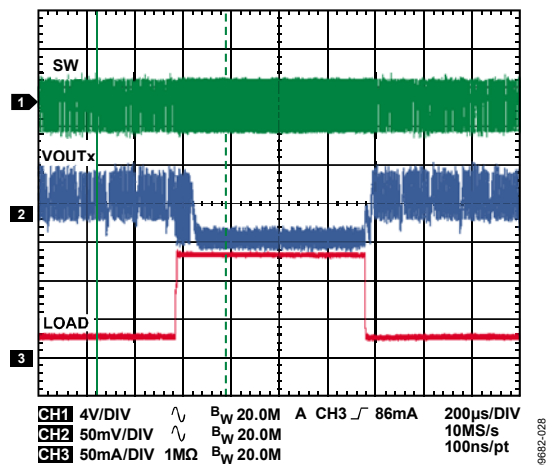


Figure 27. Buck Response to Load Transient, I_{OUT1} from 20 mA to 140 mA, $V_{OUT1} = 3.3$ V, Auto Mode

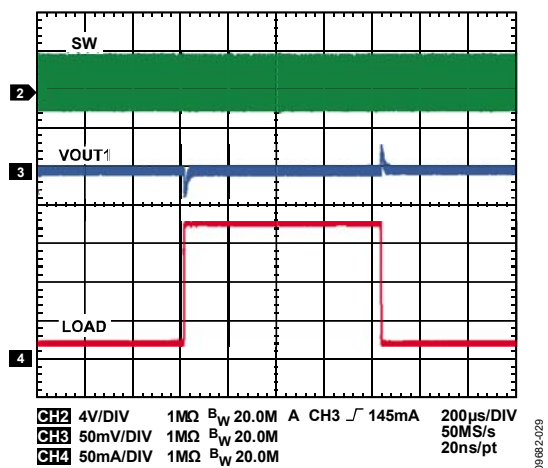


Figure 28. Buck Response to Load Transient, $I_{OUT1} = 20$ mA to 180 mA, $V_{OUT1} = 1.8$ V, PWM Mode

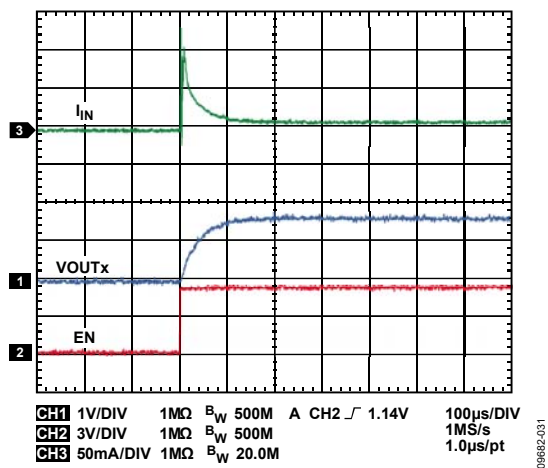


Figure 29. LDO Startup, $V_{OUT2} = 3.3$ V, $I_{OUT2} = 5$ mA

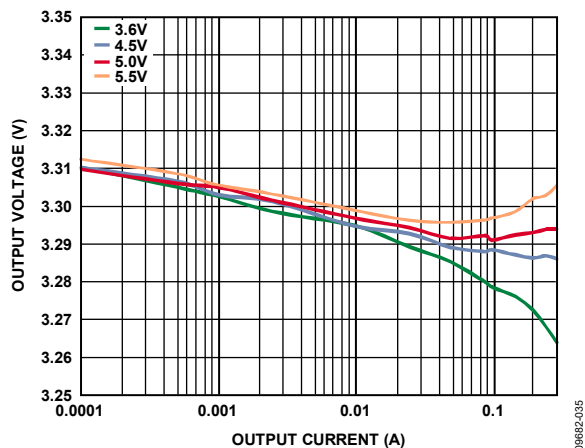


Figure 30. LDO Load Regulation Across Input Voltage, $V_{OUT2} = 3.3$ V

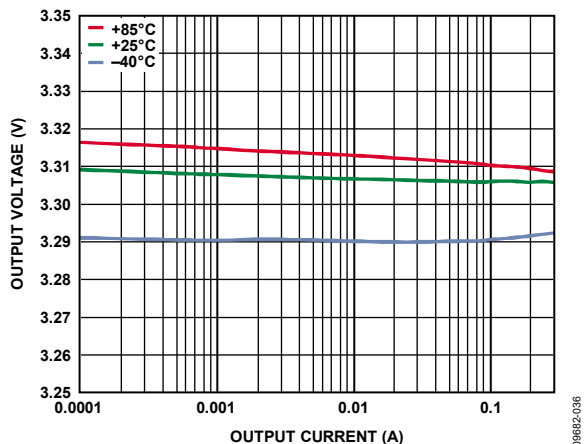


Figure 31. LDO Load Regulation Across Temperature, $V_{IN2} = 3.6$ V, $V_{OUT2} = 3.3$ V

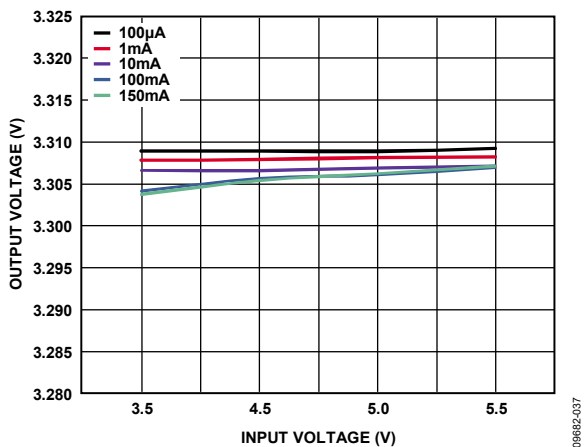


Figure 32. LDO Line Regulation Across Output Load, $V_{OUT2} = 3.3$ V

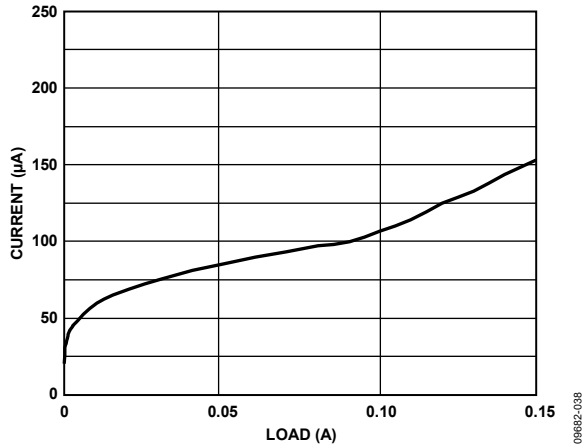


Figure 33. LDO Ground Current vs. Output Load, $V_{OUT2} = 2.8\text{ V}$

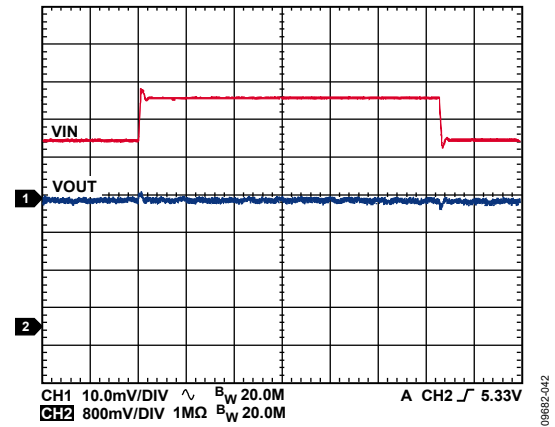


Figure 36. LDO Response to Line Transient, $V_{IN2} = 4.5\text{ V}$ to 5.5 V , $V_{OUT2} = 3.3\text{ V}$

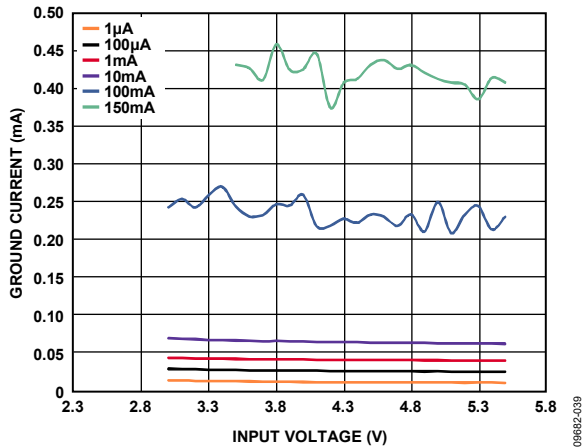


Figure 34. LDO Ground Current vs. Input Voltage, Across Output Load, $V_{OUT2} = 2.8\text{ V}$

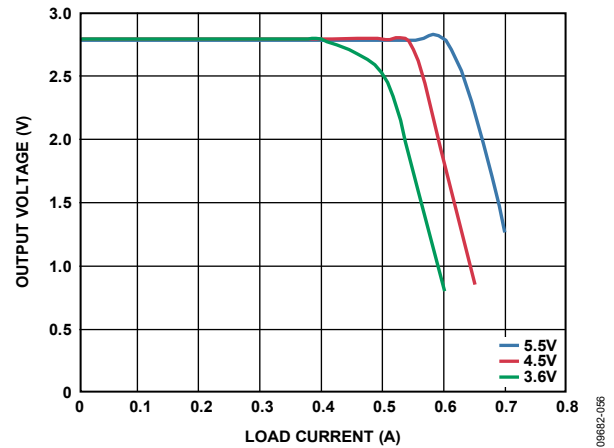


Figure 37. LDO Output Current Capability vs. Output Voltage

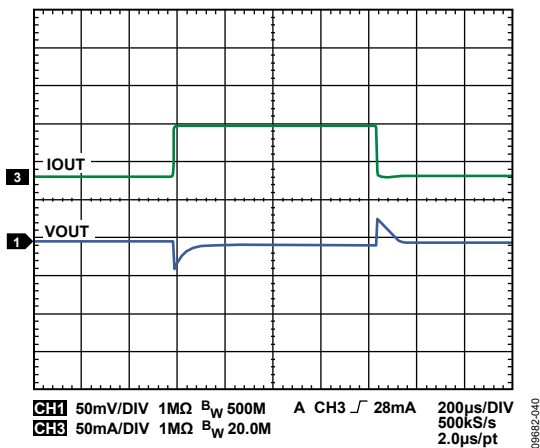


Figure 35. LDO Response to Load Transient, I_{OUT2} from 1 mA to 80 mA , $V_{OUT2} = 3.3\text{ V}$

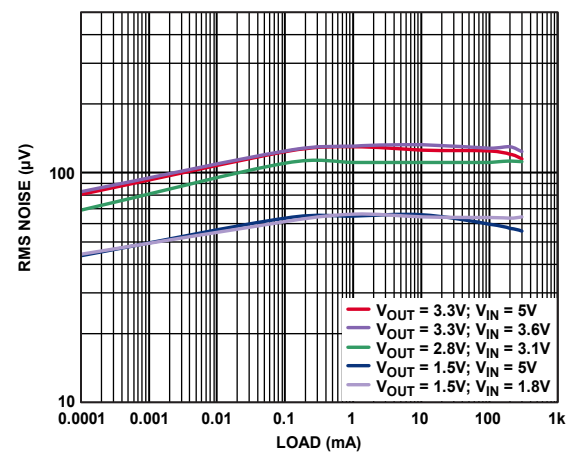


Figure 38. LDO Output Noise vs. Load Current, Across Input and Output Voltage

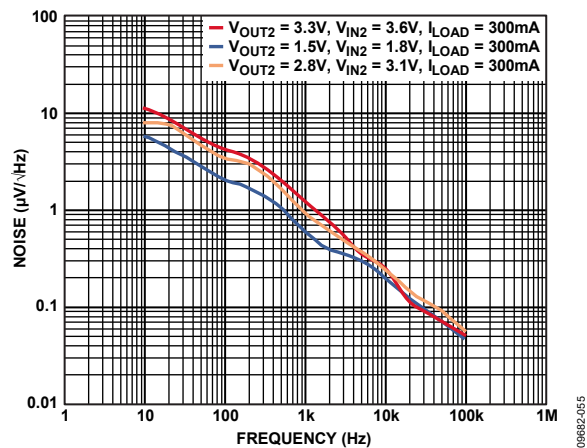
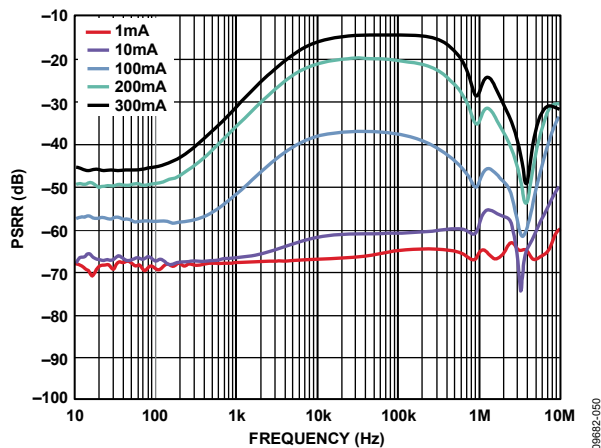
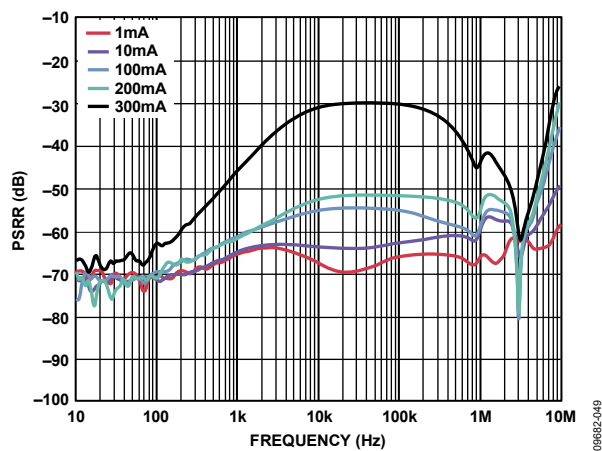
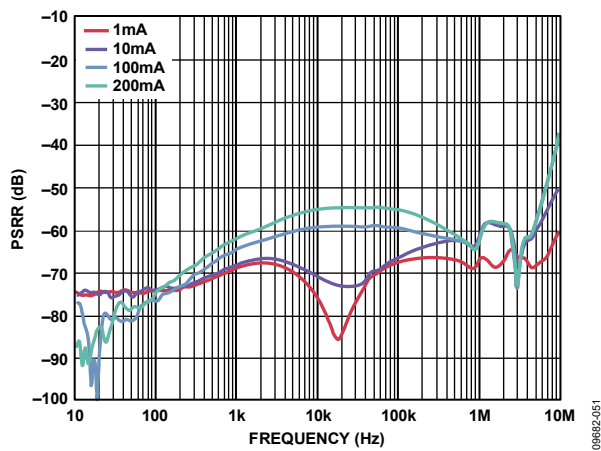


Figure 39. LDO Output Noise Spectrum, Across Input and Output Voltage

Figure 41. LDO PSRR vs. Frequency, $V_{\text{IN2}} = 3.1\text{V}$, $V_{\text{OUT2}} = 2.8\text{V}$ Figure 40. LDO PSRR Across Output Load, $V_{\text{IN2}} = 3.3\text{V}$, $V_{\text{OUT2}} = 2.8\text{V}$ Figure 42. LDO PSRR vs. Frequency, $V_{\text{IN2}} = 5\text{V}$, $V_{\text{OUT2}} = 3.3\text{V}$

THEORY OF OPERATION

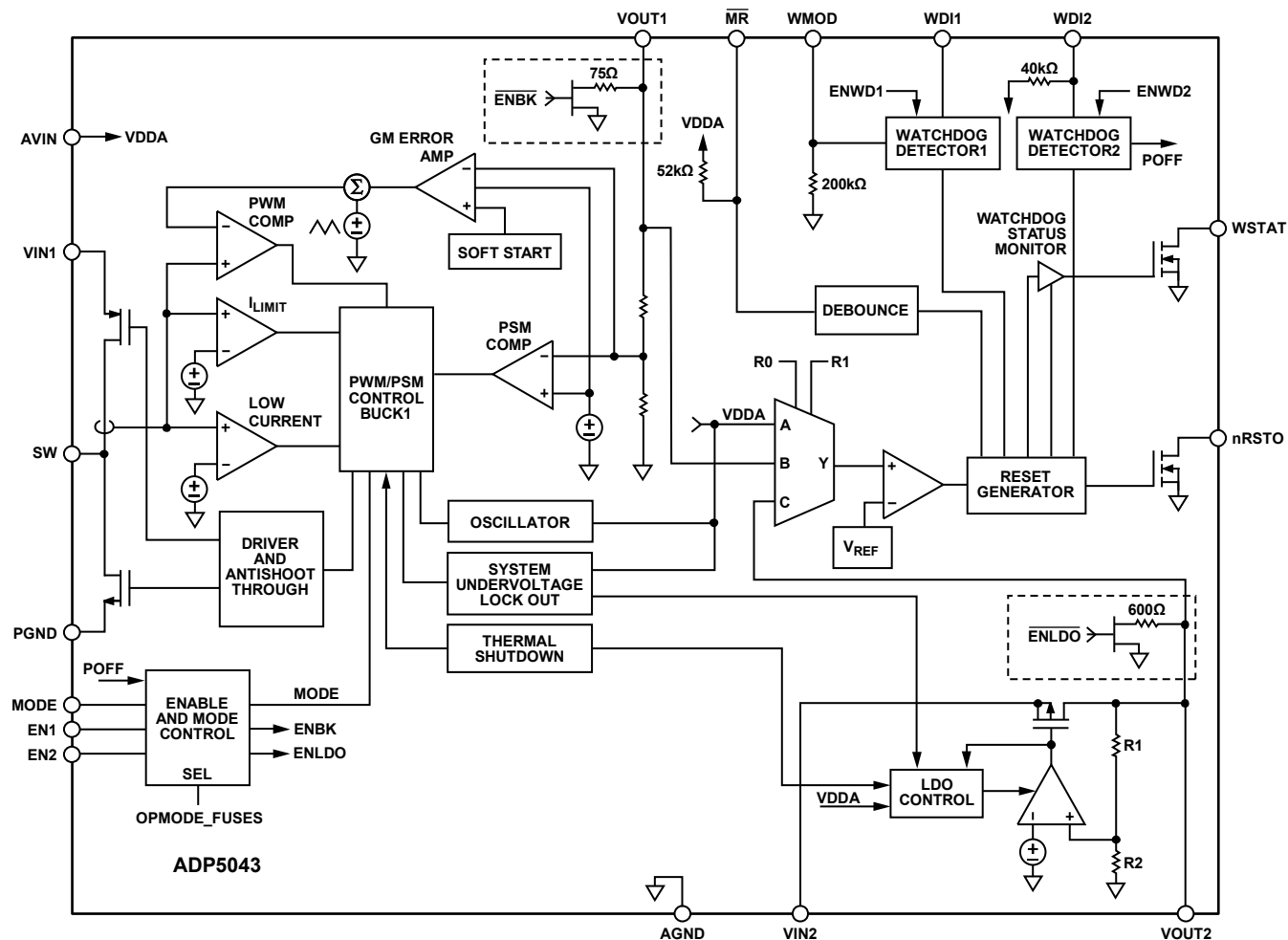


Figure 43. Functional Block Diagram

POWER MANAGEMENT UNIT

The ADP5043 is a micro power management unit (micro PMU) combining one step-down (buck) dc-to-dc regulator, one low dropout linear regulator (LDO), and a supervisory circuit with dual watchdog, for processor control. The regulators are activated by a logic level high applied to the respective EN pins. EN1 controls the buck regulator while EN2 controls the LDO. The ADP5043 has factory programmed output voltages and reset voltage threshold. Other features available in this device are the MODE pin to control the buck switching operation, a status pin (WSTAT) informing the external processor of which watchdog caused a reset, and a push-button reset input (nRSTO).

When a regulator is turned on, the output voltage is controlled through a soft start circuit, which prevents a large inrush current due to the discharged output capacitors.

The buck regulator can operate in forced PWM mode if the MODE pin is at a logic high level. In forced PWM mode, the switching frequency of the buck is always constant and does not change with the load current. If the MODE pin is at a logic low level, the switching regulator operates in auto PWM/PSM mode. In this mode, the regulator operates at fixed PWM frequency when the load current is above the power saving current threshold. When the load current falls below the power saving current threshold, the regulator enters power saving mode where the switching occurs in bursts. The burst repetition rate is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses.

Thermal Protection

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off the buck and LDO. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included in the thermal shutdown circuit so that if thermal shutdown occurs, the buck and LDO do not return to normal operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, a soft start is initiated.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated in the ADP5043. If the input voltage on AVIN drops below a typical 2.15 V UVLO threshold, all channels shut down. In the buck channel, both the power switch and the synchronous rectifier turn off. When the voltage on AVIN rises above the UVLO threshold, the part is enabled once more.

Alternatively, the user can select device models with a UVLO set at a higher level, suitable for 5 V applications. For these models, the device hits the turn-off threshold when the input supply drops to 3.65 V typical.

Enable/Shutdown

The ADP5043 has individual control pins for each regulator. A logic level high applied to the ENx pin activates a regulator; a logic level low turns off a regulator.

When regulators are turned off after a Watchdog 2 event (see the Watchdog 2 Input section), the reactivation of the regulator occurs with a factory programmed order (see Table 9). The delay between the regulator activation (t_{D1} , t_{D2}) is 2 ms.

Table 9. ADP5043 Regulators Sequencing

REGSEQ[1:0]		Regulators Sequence (First to Last)
0	0	LDO to buck
0	1	Buck to LDO
1	0	Buck to LDO
1	1	No sequence, all regulators start at same time

BUCK SECTION

The buck uses a fixed frequency and high speed current-mode architecture. The buck operates with an input voltage of 2.3 V to 5.5 V.

Control Scheme

The buck operates with a fixed frequency current-mode PWM control at medium to high loads for high efficiency; operation shifts to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switch is adjusted to regulate the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner that produces a higher output voltage ripple. During

part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM Mode

In PWM mode, the buck operates at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the high-side PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the low-side NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

The buck smoothly transitions to PSM operation when the load current decreases below the PSM current threshold. When the buck enters power save mode, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level that is approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck enters an idle state. The output capacitor discharges until the output voltage falls to the PWM regulation voltage, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current stays below the PSM current threshold.

PSM Current Threshold

The PSM current threshold is set to 100 mA. The buck employs a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to, and exit from, the PSM mode. The PSM current threshold is optimized for high efficiency over all load currents.

Short-Circuit Protection

The buck includes frequency foldback to prevent current runaway with a hard short on the output. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Soft Start

The buck has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

The buck has protection circuitry to limit the amount of positive current flowing through the PFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Operation

With a dropping input voltage or with an increase in load current, the buck may reach a limit where, even with the PFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

LDO SECTION

The ADP5043 contains one LDO with a low quiescent current that provides an output current up to 300 mA. The low, 15 μ A typical, quiescent current at no load makes the LDO ideal for battery-operated portable equipment.

The LDO operates with an input voltage range of 1.7 V to 5.5 V. The wide operating range makes this LDO suitable for a cascade configuration where the LDO supply voltage is provided from the buck regulator.

The LDO also provides high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with a small 1 μ F ceramic input and output capacitors.

The LDO is optimized to supply analog circuits by offering better noise performance than the buck regulator.

Internally, an LDO consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, reducing the current flowing to the output.

SUPERVISORY SECTION

The ADP5043 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition,

problems with microprocessor code execution can be monitored and corrected with a dual-watchdog timer.

Reset Output

The ADP5043 has an active-low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail that is no higher than 6 V. The resistor should comply with the logic low and logic high voltage level requirements of the microprocessor while supplying input current and leakage paths on the nRSTO pin. A 10 k Ω pull-up resistor is adequate in most situations.

The reset output is asserted when the monitored rail is below the reset threshold (V_{TH}), when WDI1 or WDI2 is not serviced within the watchdog timeout period (t_{WD1} and t_{WD2}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after the monitored rail rises above the reset threshold or after the watchdog timer times out. Figure 44 illustrates the behavior of the reset output, nRSTO, and it assumes that VOUT2 is selected as the rail to be monitored and supplies the external pull-up connected to the nRSTO output.

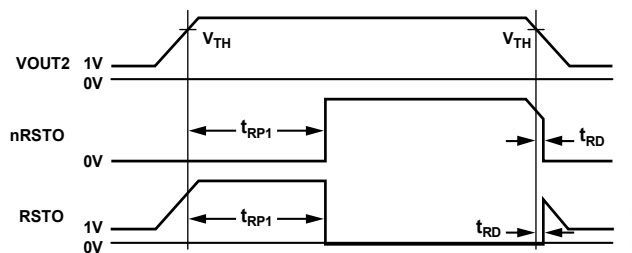


Figure 44. Reset Timing Diagram

The reset threshold voltage and the sensed rail (VOUT1, VOUT2, or AVIN) are factory programmed. Refer to Table 16 for a complete list of the reset thresholds available for the ADP5043.

When monitoring the input supply voltage, AVIN, if the selected reset threshold is below the UVLO level (factory programmable to 2.25 V or 3.6 V) the reset output, nRSTO, is asserted low as soon as the input voltage falls below the UVLO threshold. Below the UVLO threshold, the reset output is maintained low down to ~ 1 V VIN. This is to ensure that the reset output is not released when there is sufficient voltage on the rail supplying a processor to restart the processor operations.

Manual Reset Input

The ADP5043 features a manual reset input ($\overline{MR}$) which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low-to-high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 k Ω , internal pull-up, connected to AVIN, so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative-going transients of up to 100 ns (typical) are ignored. A 0.1 μ F capacitor between $\overline{MR}$ and ground provides additional noise immunity.

Watchdog 1 Input

The ADP5043 features a watchdog timer that monitors microprocessor activity. The watchdog timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI1), which detects pulses as short as 80 ns. If the timer counts through the preset watchdog timeout period (t_{WD1}), an output reset is asserted. The microprocessor is required to toggle the WDI1 pin to avoid being reset. Failure of the microprocessor to toggle WDI1 within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor into a known state.

As well as logic transitions on WDI1, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on the monitored rail. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deasserts. Watchdog 1 timer can be disabled by leaving WDI1 floating or by three-stating the WDI1 driver. The pin WMOD controls the Watchdog 1 operating mode. If WMOD is set to logic level low, Watchdog 1 is enabled as long as WDI1 is not in three-state. If WMOD is set to logic level high, Watchdog 1 is always active and cannot be disabled by a three-state condition. WMOD input has an internal 200 k Ω pull-down resistor.

Watchdog 1 timeout is factory set to two possible values, as indicated in Table 18.

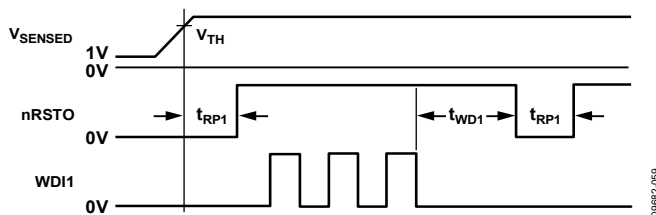


Figure 45. Watchdog 1 Timing Diagram

Watchdog 2 Input

The ADP5043 features an additional watchdog timer that monitors microprocessor activity in parallel with the first watchdog but with a much longer timeout. This provides additional security and safety in case Watchdog 1 is incorrectly strobed. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI2), which detects pulses as short as 8 μ s. If the timer counts through the preset watchdog timeout period (t_{WD2}), reset is asserted, followed by a power cycle of all regulators. The microprocessor is required to toggle the WDI2 pin to avoid being reset and powered down. Failure of the microprocessor to toggle WDI2 within the timeout period, therefore, indicates a code execution error, and the reset output nRSTO is forced low for t_{RP2} . Then, all the regulators are turned off for the t_{POFF} time. After the t_{POFF} period, the regulators are reactivated according to a predefined sequence (see Table 9). Finally, the reset line (nRSTO) is asserted for t_{RP1} . This guarantees a clean power-up of the system and proper reset.

As well as logic transitions on WDI2, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on the V_{TH} monitored rail which can be factory programmable between VOUT1, VOUT2, and AVIN (see Table 21). When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deasserts.

Watchdog 2 timeout is factory set to seven possible values as indicated in Table 19. One additional option allows Watchdog 2 to be factory disabled.

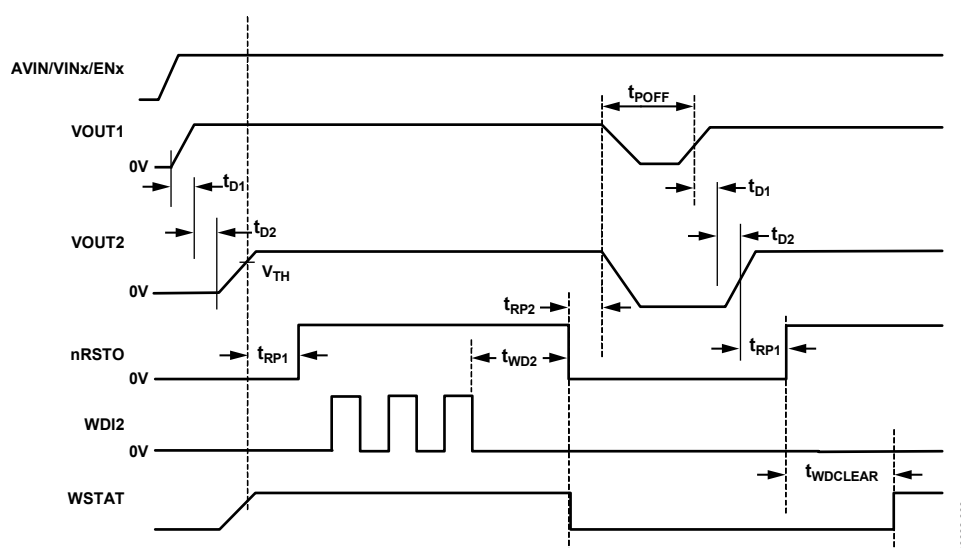


Figure 46. Watchdog 2 Timing Diagram (Assuming that VOUT2 is the Monitored Rail)

Watchdog Status Indicator

In addition to the dual watchdog function, the ADP5043 features a watchdog status monitor available on the WSTAT pin. This pin can be queried by the external processor to determine the origin of a reset. WSTAT is an open-drain output.

WSTAT outputs a logic level depending on the condition that has generated a reset. WSTAT is forced low if the reset was generated because of a Watchdog 2 timeout. WSTAT is pulled high, through external pull-up, for any other reset cause (Watchdog 1 timeout, power failure or monitored voltage be low threshold). The status monitor is automatically cleared (set to logic level high) 10 seconds after the nRSTO low-to-high transition ($t_{WDCLEAR}$). The processor firmware must be designed to read the WSTAT flag before $t_{WDCLEAR}$ expiration after a Watchdog 2 reset.

The WSTAT flag is not updated in the event of a reset due to a low voltage threshold detection or Watchdog 1 event occurring within 10 seconds after an nRSTO low-to-high transition. In this situation, WSTAT maintains the previous state (see the state flow in Figure 47).

The external processor can further distinguish a reset caused by a Watchdog 1 timeout from a power failure, status monitor WSTAT indicating a high level, by implementing a RAM check or signature verification after reset. A RAM check or signature failure indicates that a power failure has occurred, whereas a RAM check or signature validation indicates that a Watchdog 1 timeout has occurred.

Table 10 shows the possible watchdog decoded statuses.

Table 10. Watchdog Status Decoding

WSTAT	RAM Checksum	Reset Origin
High	Failed	Power failure
High	Ok	Watchdog 1
Low	Don't care	Watchdog 2

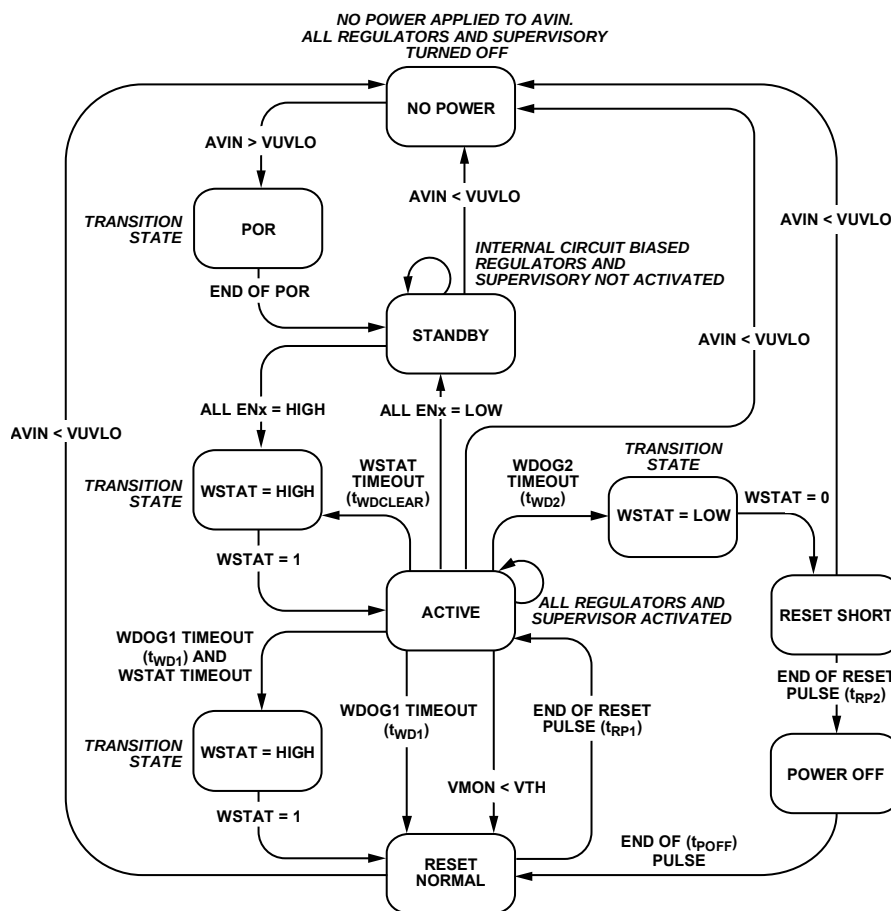


Figure 47. ADP5043 State Flow

APPLICATIONS INFORMATION

BUCK EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response are made by varying the choice of external components in the applications circuit, as shown in Figure 48.

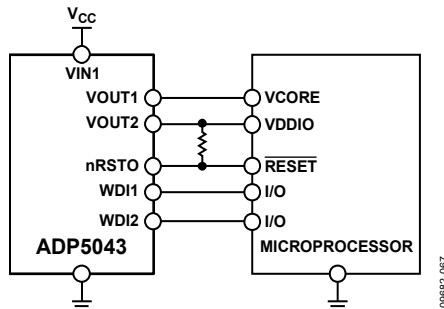


Figure 48. Typical Applications Circuit

Inductor

The high switching frequency of the buck regulator of the ADP5043 allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 μH and 3 μH . Suggested inductors are shown in Table 11.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{\text{RIPPLE}} = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \times f_{\text{SW}} \times L}$$

where:

f_{SW} is the switching frequency.

L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{\text{PEAK}} = I_{\text{LOAD (MAX)}} + \frac{I_{\text{RIPPLE}}}{2}$$

Table 11. Suggested 1.0 μH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (m Ω)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
Murata	LQM18FN1R0M00B	1.6 × 0.8 × 0.8	150	26
Taiyo Yuden	CBMF1608T1R0M	1.6 × 0.8 × 0.8	290	90
Coilcraft	EPL2014-102ML	2.0 × 2.0 × 1.4	900	59
TDK	GLFR1608T1R0M-LR	1.6 × 0.8 × 0.8	230	80
Coilcraft	0603LS-102	1.8 × 1.69 × 1.1	400	81
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1350	85

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material.

Because the buck is a high switching frequency dc-to-dc converter, shielded ferrite core material is recommended for its low core losses and low EMI.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing the capacitor value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are highly recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{\text{EFF}} = C_{\text{OUT}} \times (1 - \text{TEMPCO}) \times (1 - \text{TOL})$$

where:

C_{EFF} is the effective capacitance at the operating voltage.

TEMPCO is the worst-case capacitor temperature coefficient.

TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over -40°C to $+85^\circ\text{C}$ is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 9.2481 μF at 1.8 V, as shown in Figure 49.

Substituting these values in the equation yields

$$C_{\text{EFF}} = 9.2481 \mu\text{F} \times (1 - 0.15) \times (1 - 0.1) = 7.0747 \mu\text{F}$$

To guarantee the performance of the buck regulator, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

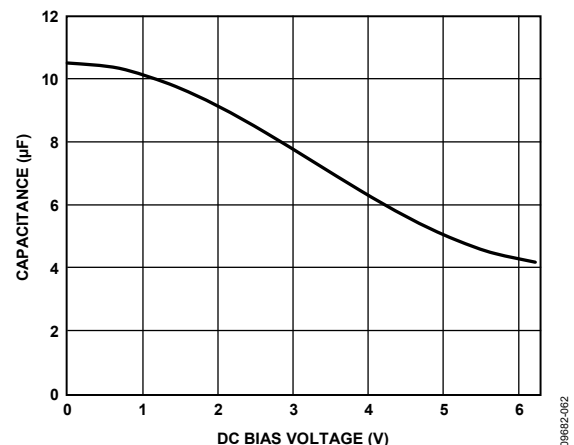


Figure 49. Typical Capacitor Performance

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = I_{RIPPLE} \times (ESR_{COUT} + 1 / (8 \times f_{SW} \times C_{OUT}))$$

where:

V_{RIPPLE} is allowable peak-to-peak output voltage ripple in volts.

I_{RIPPLE} is the inductor ripple current in Amperes.

ESR_{COUT} is the equivalent series resistance of the output capacitor in Ω .

f_{SW} is the converter switching frequency in Hertz.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 7 μF and a maximum of 40 μF .

Table 12. Suggested 10 μF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3
Panasonic	X5R	ECJ1VB0J106M	0603	6.3

The buck regulator requires 10 μF output capacitors to guarantee stability and response to rapid load variations and to transition in and out the PWM/PSM modes. In certain applications, where the buck regulator powers a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 μF to 4.7 μF because the regulator does not expect a large load variation when working in PSM mode (see Figure 50).

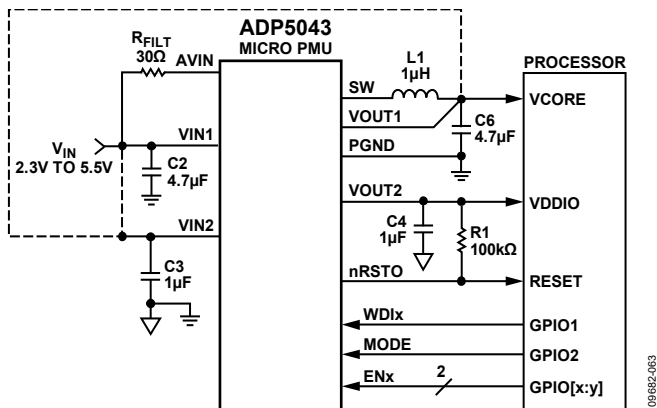


Figure 50. Processor System Power Management with PSM/PWM Control

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the buck as possible. As with the output capacitor, a low ESR input capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 μF and a maximum of 10 μF . Suggested capacitors are shown in Table 13.

Table 13. Suggested 4.7 μF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475ME19D	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
Panasonic	X5R	ECJ-0EB0J475M	0402	6.3

LDO CAPACITOR SELECTION

Output Capacitor

The ADP5043 LDO is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with the ESR value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 μF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the LDO. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the LDO to large changes in load current.

Input Bypass Capacitor

Connecting a 1 μF capacitor from VIN2 to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance is encountered. If greater than 1 μF of output capacitance is required, increase the input capacitor to match it.

Table 14. Suggested 1.0 μF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM155R61A105ME15	0402	10.0
TDK	X5R	C1005JB0J105KT	0402	6.3
Panasonic	X5R	ECJ0EB0J105K	0402	6.3
Taiyo Yuden	X5R	LMK105BJ105MV-F	0402	10.0

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP5043 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are highly recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

Figure 51 depicts the capacitance vs. voltage bias characteristic of a 0402 1 μF , 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about $\pm 15\%$ over the -40°C to $+85^\circ\text{C}$ temperature range and is not a function of package or voltage rating.

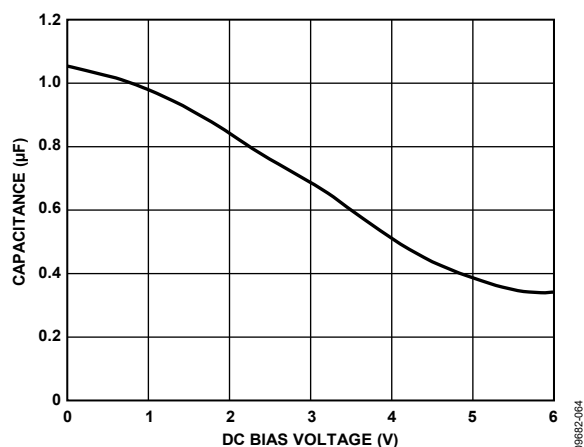


Figure 51. Capacitance vs. Voltage Characteristic

Use the following equation to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.

$TEMPCO$ is the worst-case capacitor temperature coefficient.

TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient ($TEMPCO$) over -40°C to $+85^\circ\text{C}$ is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 μF at 1.8 V as shown in Figure 51.

Substituting these values into the following equation yields:

$$C_{EFF} = 0.94 \mu\text{F} \times (1 - 0.15) \times (1 - 0.1) = 0.719 \mu\text{F}$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5043, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

SUPERVISORY SECTION

Watchdog 1 Input Current

To minimize watchdog input current (and minimize overall power consumption), leave WDI1 low for the majority of the watchdog timeout period. When driven high, WDI1 can draw as much as 25 μA . Pulsing WDI1 low-to-high-to-low at a low duty cycle reduces the effect of the large input current. When WDI1 is unconnected and WMOD is set to logic level low, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

Negative-Going V_{CC} Transients

To avoid unnecessary resets caused by fast power supply transients, the ADP5043 is equipped with glitch rejection circuitry. The typical performance characteristic in Figure 52 plots the monitored rail voltage, V_{TH} , transient duration vs. the transient magnitude. The curve shows combinations of transient magnitude and duration for which a reset is not generated for a 2.93 V reset threshold part. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 μs typically does not cause a reset, but if the transient is any larger in magnitude or duration, a reset is generated.

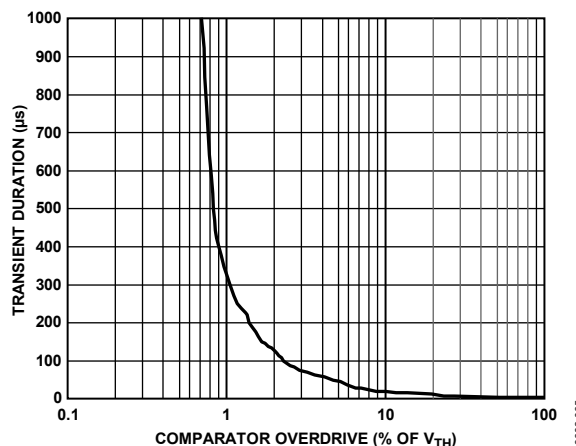


Figure 52. Maximum V_{TH} Transient Duration vs. Reset Threshold Overdrive

Watchdog Software Considerations

In implementing the watchdog strobe code of the microprocessor, quickly switching WDI1 low-to-high and then high-to-low (minimizing WDI1 high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-to-high-to-low WDI1 pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI1. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI1 is set high. The subroutine sets WDI1 low when it is called. If the program executes without error, WDI1 is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI1 is kept low, the watchdog times out, and the microprocessor is reset (see Figure 53).

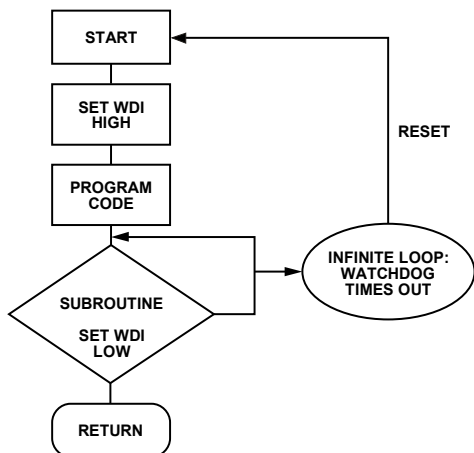


Figure 53. Watchdog Flow Diagram

The second watchdog, refreshed through the WDI2 pin, is useful in applications where safety is a very critical factor and the system must recover from unexpected operations, for example, a processor stuck in a continuous loop where Watchdog 1 is kept refreshed or environmental conditions that may unset or damage the processor port controlling the WDI1 pin. In the event of a Watchdog 2 timeout, the ADP5043 power cycles all the supplied rails to guarantee a clean processor start.

PCB LAYOUT GUIDELINES

Poor layout can affect the ADP5043 performance, causing electro-magnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

POWER DISSIPATION/THERMAL CONSIDERATIONS

The ADP5043 is a highly efficient micro PMU, and in most cases the power dissipated in the device is not a concern. However, if the device operates at high ambient temperatures and with maximum loading conditions, the junction temperature can reach the maximum allowable operating limit (125°C).

When the junction temperature exceeds 150°C, the ADP5043 turns off all the regulators, allowing the device to cool down. Once the die temperature falls below 135°C, the ADP5043 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device and to make sure the ADP5043 operates below the maximum allowable junction temperature.

The efficiency for each regulator on the ADP5043 is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (1)$$

where:

η is efficiency.

P_{IN} is the input power.

P_{OUT} is the output power.

Power loss is given by

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (2a)$$

or

$$P_{LOSS} = P_{OUT} (1 - \eta) / \eta \quad (2b)$$

The power dissipation of the supervisory function is small and can be neglected.

Power dissipation can be calculated in several ways. The most intuitive and practical is to measure the power dissipated at the input and all the outputs. The measurements should be performed at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is dissipated in the device and the inductor. Use Equation 4 to derive the power lost in the inductor, and from this use Equation 3 to calculate the power dissipation in the ADP5043 buck regulator.

A second method to estimate the power dissipation uses the efficiency curves provided for the buck regulator, while the power lost on the LDO is calculated using Equation 12. Once the buck efficiency is known, use Equation 2b to derive the total power lost in the buck regulator and inductor, use Equation 4 to derive the power lost in the inductor, and thus calculate the power dissipation in the buck converter using Equation 3. Add the power dissipated in the buck and in the LDO to find the total dissipated power.

It should be noted that the buck efficiency curves are typical values and may not be provided for all possible combinations of V_{IN} , V_{OUT} , and I_{OUT} . To account for these variations, it is

necessary to include a safety margin when calculating the power dissipated in the buck.

A third way to estimate the power dissipation is analytical and involves modeling the losses in the buck circuit provided by Equation 8 to Equation 11 and the losses in the LDO provided by Equation 12.

Buck Regulator Power Dissipation

The power loss of the buck regulator is approximated by

$$P_{LOSS} = P_{DBUCK} + P_L \quad (3)$$

where:

P_{DBUCK} is the power dissipation on the ADP5043 buck regulator.

P_L is the inductor power losses.

The inductor losses are external to the device and they don't have any effect on the die temperature.

The inductor losses are estimated (without core losses) by

$$P_L \cong I_{OUT1(RMS)}^2 \times DCR_L \quad (4)$$

where $I_{OUT1(RMS)}$ is the RMS load current of the buck regulator.

$$I_{OUT1(RMS)} = I_{OUT1} \times \sqrt{1 + r/12} \quad (5)$$

where r is the inductor ripple current.

$$r \approx V_{OUT1} \times (1 - D) / (I_{OUT1} \times L \times f_{SW}) \quad (6)$$

$$D = V_{OUT1} / V_{IN1} \quad (7)$$

f_{SW} is switching frequency.

L is inductance.

DCR_L is the inductor series resistance.

D is duty cycle.

The ADP5043 buck regulator power dissipation, P_{DBUCK} , includes the power switch conductive losses, the switch losses, and the transition losses of each channel. There are other sources of loss, but these are generally less significant at high output load currents, where the thermal limit of the application will be. Equation 8 shows the calculation made to estimate the power dissipation in the buck regulator.

$$P_{DBUCK} = P_{COND} + P_{SW} + P_{TRAN} \quad (8)$$

The power switch conductive losses are due to the output current, I_{OUT1} , flowing through the PMOSFET and the NMOSFET power switches that have internal resistance, $R_{DS(on)-P}$ and $R_{DS(on)-N}$. The amount of conductive power loss is found by:

$$P_{COND} = [R_{DS(on)-P} \times D + R_{DS(on)-N} \times (1 - D)] \times I_{OUT1}^2 \quad (9)$$

For the ADP5043, at 125°C junction temperature and $V_{IN} = 3.6$ V, $R_{DS(on)-P}$ is approximately 0.2 Ω , and $R_{DS(on)-N}$ is approximately 0.16 Ω . At $V_{IN} = 2.3$ V, these values change to 0.31 Ω and 0.21 Ω respectively, and at $V_{IN} = 5.5$ V, the values are 0.16 Ω and 0.14 Ω .

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. The amount of switching power loss is given by:

$$P_{SW} = (C_{GATE-P} + C_{GATE-N}) \times V_{INI}^2 \times f_{SW} \quad (10)$$

where:

C_{GATE-P} is the PMOSFET gate capacitance.

C_{GATE-N} is the NMOSFET gate capacitance.

For the ADP5043, the total of ($C_{GATE-P} + C_{GATE-N}$) is ~150 pF.

The transition losses occur because the PMOSFET cannot be turned on or off instantaneously, and the SW node takes some time to slew from near ground to near V_{OUT1} (and from V_{OUT1} to ground). The amount of transition loss is calculated by:

$$P_{TRAN} = V_{INI} \times I_{OUT1} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (11)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node, SW. For the ADP5043, the rise and fall times of SW are in the order of 5 ns.

If the equations and parameters previously given are used for estimating the converter efficiency, it must be noted that the equations do not describe all of the converter losses, and the parameter values given are typical numbers. The converter performance also depends on the choice of passive components and board layout, so a sufficient safety margin should be included in the estimate.

LDO Regulator Power Dissipation

The power loss of a LDO regulator is given by:

$$P_{DLDO} = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (12)$$

where:

I_{LOAD} is the load current of the LDO regulator.

V_{IN} and V_{OUT} are input and output voltages of the LDO, respectively.

I_{GND} is the ground current of the LDO regulator.

Power dissipation due to the ground current is small and it can be ignored.

Junction Temperature

The total power dissipation in the ADP5043 simplifies to:

$$P_D = \{[P_{DBUCK} + P_{DLDO1} + P_{DLDO2}]\} \quad (13)$$

In cases where the board temperature (T_A) is known, the thermal resistance parameter, θ_{JA} , can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (14)$$

The typical θ_{JA} value for the 20-lead, 4 mm × 4 mm LFCSP is 38°C/W, see Table 7.

An important factor to consider is that θ_{JA} is based on a four-layer 4 inch × 3 inch, 2.5 oz copper, as per JEDEC standard, and real applications may use different sizes and layers. It is important to maximize the copper used to remove the heat from the device, and copper exposed to air dissipates heat better than copper used in the inner layers. The thermal pad (TP) should be connected to the ground plane with several vias as shown in Figure 55.

If the case temperature can be measured, the junction temperature is calculated by:

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (15)$$

where:

T_C is the case temperature.

θ_{JC} is the junction-to-case thermal resistance provided in Table 7.

When designing an application for a particular ambient temperature range, calculate the expected ADP5043 power dissipation (P_D) due to the losses of all channels by using Equation 8 to Equation 13. From this power calculation, the junction temperature, T_J , can be estimated using Equation 14.

The reliable operation of the buck regulator and the LDO regulator can be achieved only if the estimated die junction temperature of the ADP5043 (Equation 14) is less than 125°C. Reliability and mean time between failures (MTBF) is highly affected by increasing the junction temperature. Additional information about product reliability can be found in the [Analog Devices, Inc., Reliability Handbook](#).

EVALUATION BOARD SCHEMATICS AND ARTWORK

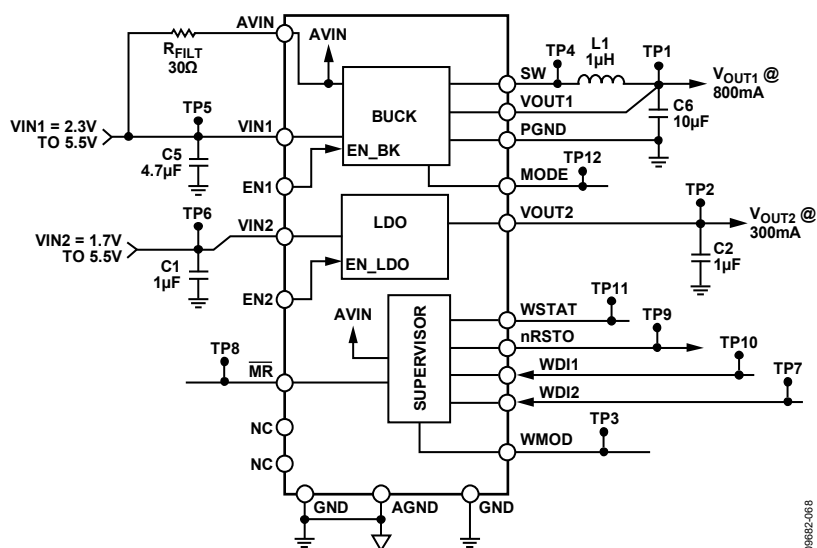


Figure 54. Evaluation Board Schematic

SUGGESTED LAYOUT

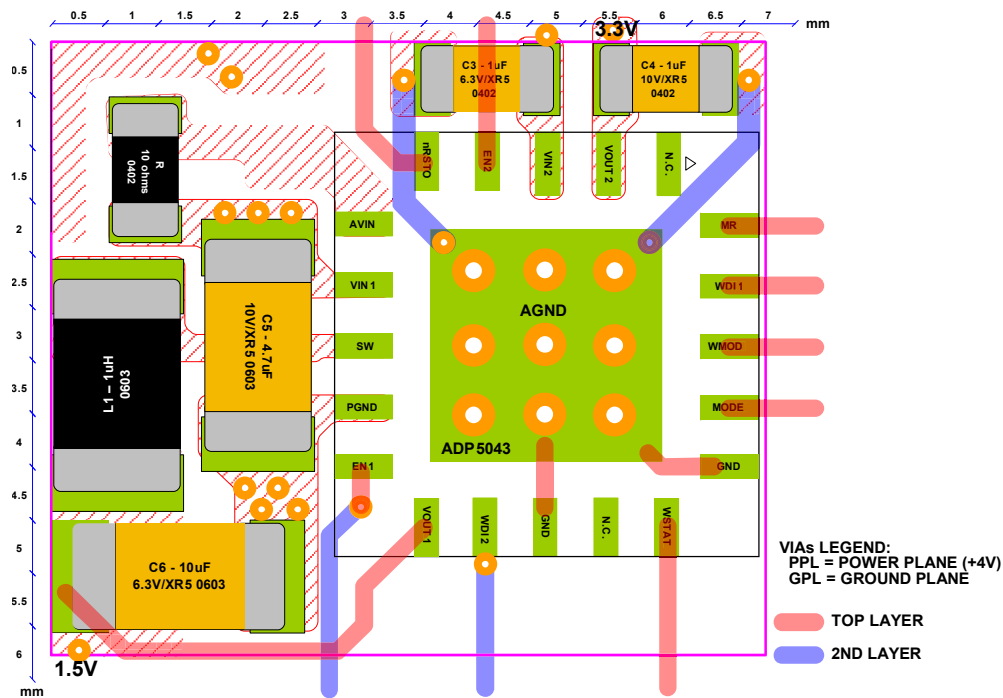


Figure 55. Layout

BILL OF MATERIALS

Table 15.

Reference	Value	Part Number	Vendor	Package
C1, C2	1 μ F, X5R, 6.3 V	LMK105BJ105MV-F	Taiyo Yuden	0402
C5	4.7 μ F, X5R, 10 V	LMK107BJ475MA-T	Taiyo Yuden	0603
C6	10 μ F, X5R, 6.3 V	JMK107BJ106MA-T	Taiyo Yuden	0603
R _{FILT}	30 Ω			0201/0402
L1	1 μ H, 0.09 Ω , 290 mA	BRC1608T1R0M	Taiyo Yuden	0603
	1 μ H, 0.08 Ω , 230 mA	GLFR1608T1R0M-LR	TDK	0603
IC1	Dual regulator micro PMU	ADP5043	Analog Devices	20-Lead LFCSP

APPLICATION DIAGRAM

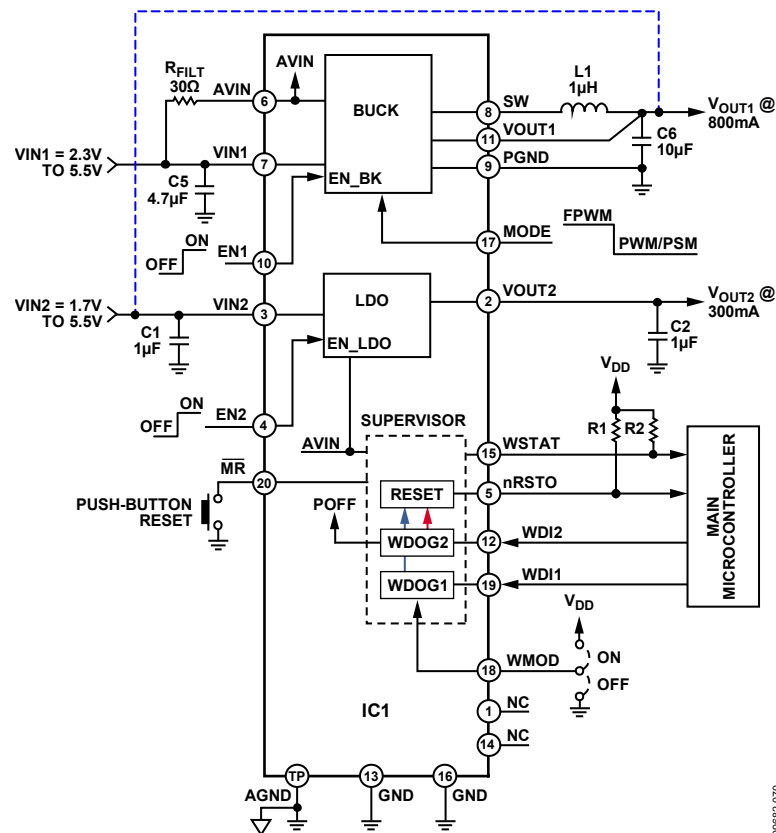


Figure 56. Application Diagram

09682-070

FACTORY PROGRAMMABLE OPTIONS

Table 16. Reset Voltage Threshold Options¹

Selection	T _A = +25°C			T _A = –40°C to +85°C		Unit
	Min	Typ	Max	Min	Max	
111 (For V _{IN} = 5 V – 6%)		4.630			4.700	V
110 (For V _{OUT} = 3.3 V)	3.034	3.080	3.126	3.003	3.157	V
101 (For V _{OUT} = 3.3 V)	2.886	2.930	2.974	2.857	3.000	V
100 (For V _{OUT} = 2.8 V)	2.591	2.630	2.669	2.564	2.696	V
011 (For V _{OUT} = 2.8 V)	2.463	2.500	2.538	2.438	2.563	V
010 (For V _{OUT} = 2.5 V – 6%)		2.350			2.385	V
001 (For V _{OUT} = 2.2 V – 6%)		2.068			2.099	V
000 (For V _{OUT} = 1.8 V – 6%)		1.692			1.717	V

¹ When monitoring AVIN, the reset threshold selected, by fuse option or by the external resistor divided, must be higher than the UVLO threshold (2.25 V or 3.6 V).

Table 17. Reset Timeout Options

Selection	Min	Typ	Max	Unit
0	24	30	36	ms
1	160	200	240	ms

Table 18. Watchdog 1 Timer Options

Selection	Min	Typ	Max	Unit
0	81.6	102	122.4	ms
1	1.12	1.6	1.92	sec

Table 19. Watchdog 2 Timer Options

Selection	Min	Typ	Max	Unit
000	6	7.5	9	sec
001		Watchdog 2 disabled		
010	3.2	4	4.8	min
011	6.4	8	9.6	min
100	12.8	16	19.2	min
101	25.6	32	38.4	min
110	51.2	64	76.8	min
111	102.4	128	153.6	min

Table 20. Power-Off Timing Options

Selection	Min	Typ	Max	Unit
0	140	200	280	ms
1	280	400	560	ms

Table 21. Reset Sensing Options

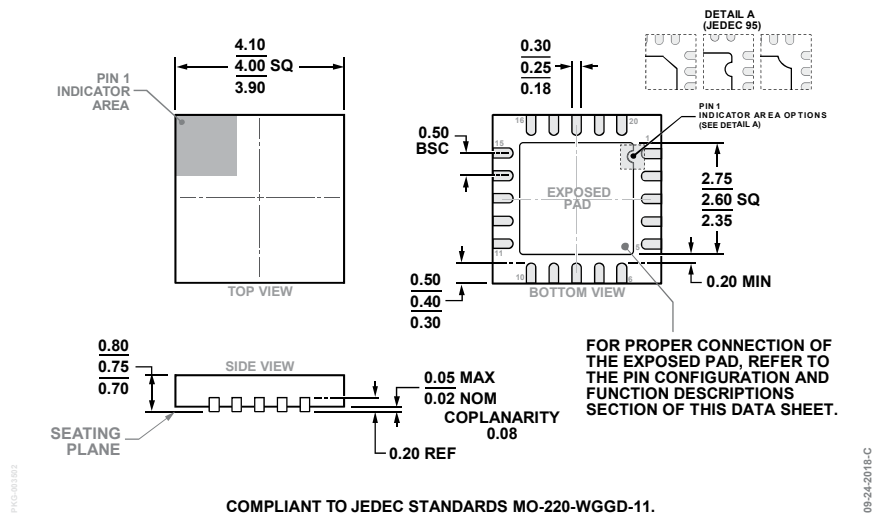
Selection	Monitored Rail
00	VOUT1 pin
01	Reserved
10	VOUT2 pin
11	AVIN ¹ pin

¹ When monitoring AVIN, the reset threshold selected, by fuse option or by the external resistor divided, must be higher than the UVLO threshold (2.25 V or 3.6 V).

Table 22. BUCK and LDO Output Voltage Options

Selection	Output Voltage
Buck	3.3 V, 3.0 V, 2.8 V, 2.5 V, 2.3 V, 2.0 V, 1.82 V, 1.8 V, 1.6 V, 1.5 V, 1.4 V, 1.3 V, 1.2 V, 1.1 V, 1.0 V, 0.9 V
LDO	3.3 V, 3.0 V, 2.8 V, 2.5 V, 2.25 V, 2.0 V, 1.8 V, 1.7 V, 1.6 V, 1.5 V, 1.2 V, 1.1 V, 1 V, 0.9 V, 0.8 V

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.
 Figure 57. 20-Lead, Lead Frame Chip Scale Package [LFCSP]
 4 mm × 4 mm Body and 0.75 mm Package Height
 (CP-20-8)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1,2}	Regulator Settings	Supervisory Settings	Temperature Range	Package Description	Package Option
ADP5043ACPZ-1-R7	V _{OUT1} = 1.5 V V _{OUT2} = 3.3 V UVLO = 2.25 V Sequencing: LDO, buck	WD1 t _{OUT} = 1.6 sec WD2 t _{OUT} = 128 min Reset t _{OUT} = 200 ms P _{OFF} = 200 ms V _{TH} sensing = V _{OUT2} , 2.93 V	T _J = -40°C to +125°C	20-Lead LFCSP	CP-20-8
ADP5043CP-1-EVALZ				Evaluation Board	

¹ Z = RoHS Compliant Part.

² Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits. See the Power Dissipation/Thermal Considerations section for more information.

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