7.5 kV RMS/3.75 kV RMS, Dual-Channel LVDS 2.5 Gigabit Isolator

FEATURES

- 7.5 kV rms/3.75 kV rms LVDS isolators
- Complies with TIA/EIA-644-A LVDS signal levels
- Dual-channel configuration (ADN4620: 2 + 0, ADN4621: 1 + 1)
- Any data rate up to 2.5 Gbps switching with low jitter
  - 5 Gbps total bandwidth across two channels
  - 2.15 ns typical propagation delay
  - Typical jitter: 0.82 ps rms random, 40 ps total peak-to-peak
- Lower power 1.8 V supplies with 3.3 V supplies for I/O
- Up to ±8 kV IEC 61000-4-2 ESD protection across isolation barrier
- High common-mode transient immunity: 70 kV/µs typical
- Safety and regulatory approvals (16-lead SOIC_IC package)
  - UL (pending): 7500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
  - VDE certificate of conformity, reinforced insulation (pending)
    - DIN V VDE V 0884-11 (VDE V 0884-11):2017-01
    - V_{IORM} = 1500 V_{PEAK} (maximum working insulation voltage)
- Enable or disable refresh (20-lead SSOP package)
- Operating temperature range: −40°C to +125°C
- Compact SSOP package with 5.3 mm creepage or wide SOIC_IC package with 15.1 mm creepage

APPLICATIONS

- Analog front-end isolation
- Data plane isolation
- Isolated high speed clock and data links
- Multigigabit serialization/deserialization (SERDES)
- PCB-to-PCB optical replacement (for example, short reach fiber)

FUNCTIONAL BLOCK DIAGRAMS

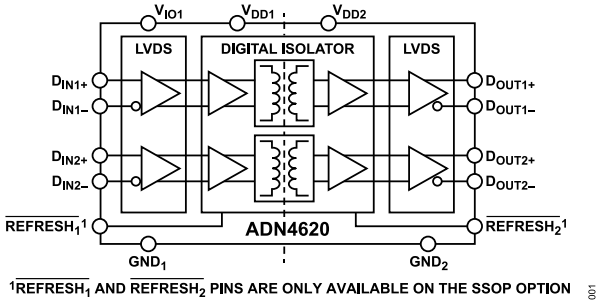

Figure 1. ADN4620 Two Forward Channels

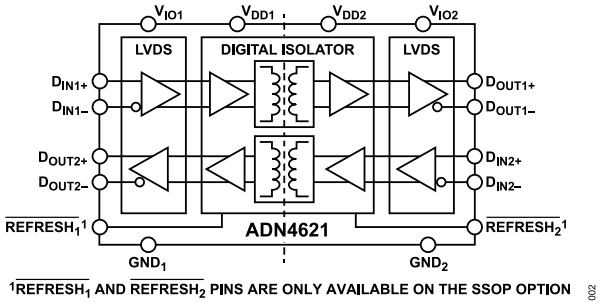

Figure 2. ADN4621 One Forward and One Reverse Channel

GENERAL DESCRIPTION

The ADN4620/ADN4621[1] are dual-channel, signal isolated, low voltage differential signaling (LVDS) buffers that operate at up to 2.5 Gbps with very low jitter. The devices integrate Analog Devices, Inc., *i*Coupler® technology, enhanced for high speed operation to provide drop-in galvanic isolation of LVDS signal chains. AC coupling and/or level shifting to the LVDS receivers and from the LVDS drivers allows isolation of other high speed signals, such as current mode logic (CML).

The ADN4620/ADN4621 include a refresh mechanism to monitor the input and output states and ensure that they remain the same in the absence of data transitions (for example, at power-on). For lower power consumption and high speed operation with low jitter, the isolator circuits rely on 1.8 V supplies, while 3.3 V supplies are used for LVDS receivers to support the full common-mode range with an input voltage range (input common mode plus differential input voltage) of 0 V to 2.4 V per Table 2.

The devices are fully specified over a wide industrial temperature range and are available in a compact SSOP package with 5.3 mm creepage (for reinforced insulation at ac mains voltages) or a wide SOIC_IC package with 15.1 mm creepage (for high working insulation voltages up to 1500 V peak, reinforced).

[1] Protected by U.S. Patents 7,075,329; 9,941,565; and 10,205,442. Other patents are pending.

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6/2022—Revision 0: Initial Version

SPECIFICATIONS

For all minimum and maximum specifications, V_{DD1} = 1.7 V to 1.9 V, V_{DD2} = 1.7 V to 1.9 V, V_{IO1} = 3 V to 3.6 V, V_{IO2} = 3 V to 3.6 V and T_A = −40°C to +125°C, unless otherwise noted. For all typical specifications, V_{DD1} = V_{DD2} = 1.8 V, V_{IO1} = V_{IO2} = 3.3 V, and T_A = 25°C. For all specifications, $\overline{REFRESH_1}$ = GND_1 and $\overline{REFRESH_2}$ = GND_2, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUTS (RECEIVERS)						
Input Threshold						See Figure 36 and Table 2
High	V_{TH}			100	mV	
Low	V_{TL}	−100			mV	
Differential Input Voltage	$\|V_{ID}\|$	100			mV	See Figure 36 and Table 2
Input Common-Mode Voltage	V_{IC}	$0.5\|V_{ID}\|$		$2.4 - 0.5\|V_{ID}\|$	V	See Figure 36 and Table 2
Input Current, High and Low	I_{IH}, I_{IL}	−5		+5	µA	$D_{INx\pm}$ = 2.4 V or 0 V, other input = 1.2 V, V_{DDx} = 1.8 V or 0 V, V_{IOx} = 3.3 V or 0 V
Differential Input Capacitance[1]	$C_{INx\pm}$		1.7		pF	One $D_{INx\pm}$ = 0.4 sin(30 × 10^6πt) V + 0.5 V, other $D_{INx\pm}$ = 1.2 V[2]
LOGIC INPUTS (SSOP)						V_{DDx} = V_{DD1} for $\overline{REFRESH_1}$, V_{DDx} = V_{DD2} for $\overline{REFRESH_2}$
Input High Voltage	V_{INH}	0.65 V_{DDx}			V	
Input Low Voltage	V_{INL}			0.35 V_{DDx}	V	
Input Current High	$\|I_{INH}\|$			1	µA	$\overline{REFRESH_x}$ = V_{DDx}
				25	µA	$\overline{REFRESH_x}$ = 1.9 V, V_{DDx} = 0 V
Input Current Low	$\|I_{INL}\|$			16	µA	$\overline{REFRESH_x}$ = 0 V
OUTPUTS (DRIVERS)						
Differential Output Voltage	$\|V_{OD}\|$	250	310	450	mV	See Figure 34 and Figure 35, load resistance (R_L) = 100 Ω
V_{OD} Magnitude Change	$\Delta\|V_{OD}\|$			50	mV	See Figure 34 and Figure 35, R_L = 100 Ω
Offset Voltage	V_{OS}	1.125	1.17	1.375	V	See Figure 34, R_L = 100 Ω
V_{OS} Magnitude Change	ΔV_{OS}			50	mV	See Figure 34, R_L = 100 Ω
V_{OS}, Peak-to-Peak[1]	$V_{OS(p-p)}$			150	mV	See Figure 34, R_L = 100 Ω
Output Short-Circuit Current	I_{OS}			−20	mA	$D_{OUTx\pm}$ = 0 V
				12	mA	$\|V_{OD}\|$ = 0 V
Differential Output Capacitance[1]	$C_{OUTx\pm}$		5		pF	One $D_{OUTx\pm}$ = 0.4 sin(30 × 10^6πt) V + 0.5 V, other $D_{OUTx\pm}$ = 1.2 V, V_{DD1} or V_{DD2} = 0 V
ADN4620 SUPPLY CURRENT						All channels, 100 Ω across inputs $D_{INx\pm}$, $\|V_{ID}\|$ = 200 mV
Supply Current Side 1	I_{DD1}		65	80	mA	Frequency (f) = 1.25 GHz
Supply Current Side 2	I_{DD2}		55	65	mA	f = 1.25 GHz, R_L = 100 Ω
			48	55	mA	f = 1.25 GHz, R_L = 100 Ω, $\overline{REFRESH_2}$ = V_{DD2}
V_{IO1} Supply	I_{IO1}		11	14	mA	f = 1.25 GHz
ADN4621 SUPPLY CURRENT						All channels, 100 Ω across inputs $D_{INx\pm}$, $\|V_{ID}\|$ = 200 mV
Supply Current Side 1 or Side 2	I_{DD1} or I_{DD2}					V_{DDx} = V_{DD1} for $\overline{REFRESH_1}$, V_{DDx} = V_{DD2} for $\overline{REFRESH_2}$
			65	75	mA	f = 1.25 GHz, R_L = 100 Ω
			54	63	mA	f = 1.25 GHz, R_L = 100 Ω, $\overline{REFRESH_x}$ = V_{DDx}
V_{IO1} or V_{IO2} Supply	I_{IO1} or I_{IO2}		5.5	7	mA	f = 1.25 GHz
COMMON-MODE TRANSIENT IMMUNITY[3]	|CM|	35	70		kV/µs	Common-mode voltage (V_{CM}) = 1000 V, transient magnitude = 800 V

[1] These specifications are guaranteed by design and characterization.

[2] t denotes time.

[3] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining any D_{OUTx+} or D_{OUTx-} pin in the same state as the corresponding D_{INx+} or D_{INx-} pin (no change in output) or producing the expected transition on any D_{OUTx+} or D_{OUTx-} pin if the applied common-mode transient edge is coincident with a data transition on the corresponding D_{INx+} or D_{INx-} pin. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

RECEIVER INPUT THRESHOLD TEST VOLTAGES

Table 2. Test Voltages for Receiver Operation

Applied Voltages				
D_{INx+} (V)	D_{INx-} (V)	Input Voltage, Differential, V_{ID} (V)	Input Voltage, Common-Mode, V_{IC} (V)	Driver Output, Differential V_{OD} (mV)
1.25	1.15	0.1	1.2	>250
1.15	1.25	−0.1	+1.2	<−250
2.4	2.3	0.1	2.35	>250
2.3	2.4	−0.1	+2.35	<−250
0.1	0	0.1	0.05	>250
0	0.1	−0.1	+0.05	<−250
1.5	0.9	0.6	1.2	>250
0.9	1.5	−0.6	+1.2	<−250
2.4	1.8	0.6	2.1	>250
1.8	2.4	−0.6	+2.1	<−250
0.6	0	0.6	0.3	>250
0	0.6	−0.6	+0.3	<−250

TIMING SPECIFICATIONS

For all minimum and maximum specifications, V_{DD1} = V_{DD2} = 1.7 V to 1.9 V and T_A = −40°C to +125°C, unless otherwise noted. For all typical specifications, V_{DD1} = V_{DD2} = 1.8 V and T_A = 25°C.

Table 3.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
PROPAGATION DELAY	t_{PLH}, t_{PHL}		2.15	2.8	ns	See Figure 37, from any D_{INx+} and D_{INx-} pin to the D_{OUTx+} and D_{OUTx-} pins
SKEW						See Figure 37, across all D_{OUTx+} and D_{OUTx-} pins
Duty Cycle[2]	$t_{SK(D)}$		2	19	ps	
Channel to Channel[3]	$t_{SK(CH)}$		13	46	ps	
Part to Part[4]	$t_{SK(PP)}$		150	300	ps	
JITTER[5]						See Figure 37, for any D_{OUTx+} and D_{OUTx-} pins
Random Jitter, RMS[6] (1σ)	$t_{RJ(rms)}$		0.82	1.44	ps rms	1.25 GHz clock input
Deterministic Jitter, Peak-to-Peak[6, 7]	$t_{DJ(p-p)}$		28	54	ps	2.5 Gbps, 2^{23} − 1 pseudorandom bit stream (PRBS)
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{TJ(p-p)}$		40	70	ps	1.25 GHz/2.5 Gbps, 2^{23} − 1 PRBS[8]
With Crosstalk			45		ps	1.25 GHz/2.5 Gbps, 2^{23} − 1 PRBS all channels, $\overline{REFRESH_1}$ = V_{DD1} and $\overline{REFRESH_2}$ = V_{DD2} (SSOP package)[8]
With Crosstalk and Refresh			50		ps	1.25 GHz/2.5 Gbps, 2^{23} − 1 PRBS all channels, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2[8]
Additive Phase Jitter	t_{ADDJ}		148		fs rms	100 Hz to 100 kHz, output frequency (f_{OUT}) = 10 MHz, $\overline{REFRESH_1}$ = V_{DD1} and $\overline{REFRESH_2}$ = V_{DD2} (SSOP package)[9]
			233		fs rms	100 Hz to 100 kHz, f_{OUT} = 10 MHz, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2 (SSOP package and ADN4620 SOIC_IC package)[9]
			308		fs rms	100 Hz to 100 kHz, f_{OUT} = 10 MHz (ADN4621 SOIC_IC package)[9]
			111		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz, $\overline{REFRESH_1}$ = V_{DD1} and $\overline{REFRESH_2}$ = V_{DD2} (SSOP package)[10]
			208		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2 (SSOP package and ADN4620 SOIC_IC package)[10]
			328		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz (ADN4621 SOIC_IC package)[10]
RISE AND FALL TIME	t_R, t_F			180	ps	See Figure 37, 1.25 GHz clock input, any D_{OUTx+} and D_{OUTx-} pin, 20% to 80%, R_L = 100 Ω, load capacitance (C_L) = 5 pF

SPECIFICATIONS

Table 3.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
MAXIMUM DATA RATE		2.5			Gbps	

[1] These specifications are guaranteed by design and characterization.

[2] Duty cycle, or pulse skew, is the magnitude of the maximum difference between t_{PLH} and t_{PHL} for any Channel x of a device (where x = 1 or 2), that is, $|t_{PLHx} - t_{PHLx}|$.

[3] Channel to channel, or output skew, is the difference between the largest and smallest values of t_{PLHx} within a device or the difference between the largest and smallest values of t_{PHLx} within a device, whichever of the two is greater.

[4] Part to part output skew is the difference between the largest and smallest values of t_{PLHx} across multiple devices or the difference between the largest and smallest values of t_{PHLx} across multiple devices, whichever of the two is greater.

[5] Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter. V_{ID} = 400 mV p-p, V_{IC} = 1.2 V, and t_R / t_F < 0.05 ns (20% to 80%).

[6] This specification is measured over a population of ~3,000,000 edges.

[7] Peak-to-peak jitter specifications include jitter due to pulse skew ($t_{SK(D)}$).

[8] Using the following formula: $t_{TJ(p-p)} = 14 \times t_{RJ(rms)} + t_{DJ(p-p)}$.

[9] With an input phase jitter of 340 fs rms subtracted.

[10] With an input phase jitter of 155 fs rms subtracted.

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 4. RS-20 Shrink Small Outline Package [SSOP]

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3.75	kV rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	5.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	5.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	5.6	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		34	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material group per IEC 60664-1

Table 5. RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		7.5	kV rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	15.1	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	15.1	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	16	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		34	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material group per IEC 60664-1

PACKAGE CHARACTERISTICS

Table 6. RS-20 Shrink Small Outline Package [SSOP] and RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	Voltage (input to output) (V_{I-O}) = 500 V dc

SPECIFICATIONS

Table 6. RS-20 Shrink Small Outline Package [SSOP] and RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	Frequency = 1 MHz
Input Capacitance[2]	C_I		3.4		pF	

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together (Pin 1 through Pin 8 for SOIC_IC), and Pin 11 through Pin 20 are shorted together (Pin 9 through Pin 16 for SOIC_IC).

[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 14, Table 15 and the Insulation Lifetime section for details regarding the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 7. RS-20 Shrink Small Outline Package [SSOP]

Regulatory Agency	Standard Certification/Approval	File
UL (Pending)	To be recognized under UL 1577 Component Recognition Program[1]	E214100
	Single protection, 3750 V rms isolation voltage	
CSA (Pending)[2]	To be approved under CSA Component Acceptance Notice 5A	205078
	CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition	
	Basic insulation at 530 V rms	
	Reinforced insulation at 265 V rms	
	CSA 61010-1-12+A1 and IEC 61010-1 third edition	
	Basic insulation at 300 V rms	
	Reinforced insulation at 150 V rms	
	CSA 60601-1:14 and IEC60601-1 third edition+A1	
VDE (Pending)	To be certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01[3]	2471900-4880-0001
	Reinforced insulation, V_{IORM} = 1500 V_{PEAK}, V_{IOSM} = 6000 V_{PEAK}	
CQC (Pending)	To be certified according to GB4943.1-2011 per CQC11-471543-2015	Pending

[1] In accordance with UL 1577, each ADN4620/ADN4621 is proof tested by applying an insulation test voltage ≥4500 V rms for 1 sec.

[2] Working voltages are quoted for Pollution Degree 2, Material Group III. ADN4620/ADN4621 case material has been evaluated by CSA as Material Group I.

[3] In accordance with DIN V VDE V 0884-11, each ADN4620/ADN4621 is proof tested by applying an insulation test voltage ≥2813 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

Table 8. RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Regulatory Agency	Standard Certification/Approval	File
UL (Pending)	To be recognized under UL 1577 Component Recognition Program[1]	E214100
	Single protection, 7500 V rms isolation voltage	
CSA (Pending)[2]	To be approved under CSA Component Acceptance Notice 5A	205078
	CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition	
	CSA 61010-1-12+A1 and IEC 61010-1 third edition	
	CSA 60601-1:14 and IEC60601-1 third edition+A1	
VDE (Pending)	To be certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01[3]	2471900-4880-0001
	Reinforced insulation, V_{IORM} = 1500 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK}	
CQC (Pending)	To be certified according to GB4943.1-2011 per CQC11-471543-2015	Pending

[1] In accordance with UL 1577, each ADN4620/ADN4621 is proof tested by applying an insulation test voltage ≥9000 V rms for 1 sec.

[2] Working voltages are quoted for Pollution Degree 2, Material Group III. ADN4620/ADN4621 case material has been evaluated by CSA as Material Group I.

[3] In accordance with DIN V VDE V 0884-11, each ADN4620/ADN4621 is proof tested by applying an insulation test voltage ≥2813 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

SPECIFICATIONS

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 9. RS-20 Shrink Small Outline Package [SSOP]

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to III	
For Rated Mains Voltage ≤ 1000 V rms			I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	1500	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	2813	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{PD\ (M)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		2250	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		1800	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	6000	V_{PEAK}
Surge Isolation Voltage, Reinforced	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6250	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S		
ADN4620			1.89	W
ADN4621			1.96	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN V VDE V 0884-11.

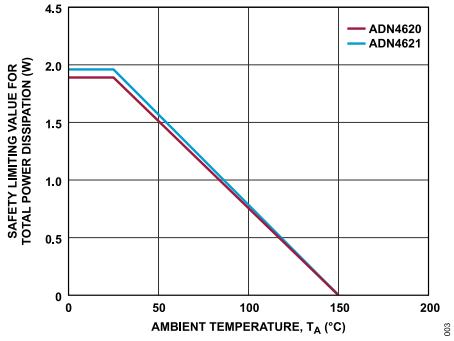

Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11, SSOP

Table 10. RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
For Rated Mains Voltage ≤ 1000 V rms			I to III	

SPECIFICATIONS

Table 10. RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	1500	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (M)}$	2813	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{PD\ (M)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		2250	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		1800	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8000	V_{PEAK}
Surge Isolation Voltage, Reinforced	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S		W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN V VDE V 0884-11.

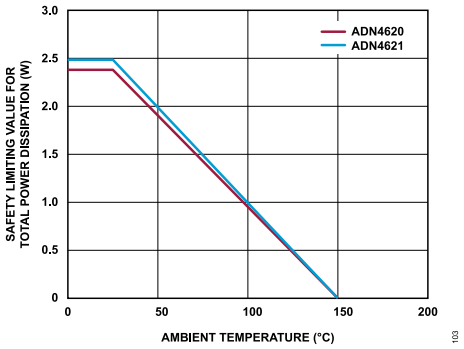

Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11, SOIC_IC

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 11.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltage Side 1 or Side 2	V_{DD1}, V_{DD2}	1.7 V to 1.9 V
Input Output Supply Voltage Side 1 or Side 2	V_{IO1}, V_{IO2}	3 V to 3.6 V

ABSOLUTE MAXIMUM RATINGS

Table 12.

Parameter	Rating
V_{DD1} to GND_1, V_{DD2} to GND_2	−0.3 V to +2 V
V_{IO1} to GND_1, V_{IO2} to GND_2	−0.3 V to +4 V
Input Voltage $\overline{REFRESH_1}$ to GND_1, $\overline{REFRESH_2}$ to GND_2	−0.3 V to +2 V
Input Voltage (D_{INx+} pin, D_{INx-} pin) to GND_x on the Same Side	−0.3 V to +4 V
Output Voltage (D_{OUTx+} pin, D_{OUTx-} pin) to GND_x on the Same Side	−0.3 V to +2 V
Short-Circuit Duration (D_{OUTx+} pin, D_{OUTx-} pin) to GND_x on the Same Side	Continuous
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. Ψ_{JT} is the junction to top thermal characterization parameter.

Table 13. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Unit
RS-20 (ADN4620)	66.1	5.2	°C/W
RS-20 (ADN4621)	63.8	3	°C/W
RI-16-3 (ADN4620)	52.5	3.1	°C/W
RI-16-3 (ADN4621)	50.3	2.4	°C/W

[1] Test Condition 1: thermal impedance simulated with 4-layer standard JEDEC PCB.

Table 14. Maximum Continuous Working Voltage, RS-20 Shrink Small Outline Package [SSOP]

Parameter[1]	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	1182 V rms	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
	1057 V rms	Rating limited by package creepage per IEC 60664-1.
Reinforced Insulation	1060 V rms	Reinforced insulation rating per IEC60747-17. Accumulative FROL ≤ 1 ppm at 26 years.
	527 V rms	Rating limited by package creepage per IEC 60664-1.
Unipolar Waveform		
Basic Insulation	1726 V_{PEAK}	Rating limited by package creepage per IEC 60664-1.
Reinforced Insulation	860 V_{PEAK}	Rating limited by package creepage per IEC 60664-1.
DC Voltage		
Basic Insulation	1057 V dc	Rating limited by package creepage per IEC 60664-1.
Reinforced Insulation	527 V dc	Rating limited by package creepage per IEC 60664-1.

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. See the Insulation Lifetime section for more details.

Table 15. Maximum Continuous Working Voltage, RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Parameter[1]	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	1182 V rms	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	1060 V rms	Reinforced insulation rating per IEC60747-17. Accumulative FROL ≤ 1 ppm at 26 years.
Unipolar Waveform		
Basic Insulation	3343 V_{PEAK}	Limited by accumulative FROL ≤ 1000 ppm at 20 years.
Reinforced Insulation	2460 V_{PEAK}	Rating limited by package creepage per IEC 60664-1.

ABSOLUTE MAXIMUM RATINGS

Table 15. Maximum Continuous Working Voltage, RI-16-3 Wide Body, with 15.1 mm Creepage [SOIC_IC] Package

Parameter[1]	Rating	Constraint
DC Voltage		
Basic Insulation	3020 V dc	Rating limited by package creepage per IEC 60664-1.
Reinforced Insulation	1507 V dc	Rating limited by package creepage per IEC 60664-1.

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. See the Insulation Lifetime section for more details.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADN4620/ADN4621

Table 16. ADN4620/ADN4621, 20-Lead SSOP

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±3000	2
IEC[2]	±7000 (contact discharge)	Level 3

[1] All pins to respective GND_x pins, 1.5 kΩ, 100 pF.

[2] LVDS pins to isolated GND_x pins across isolation barrier.

Table 17. ADN4620/ADN4621, 16-Lead SOIC_IC

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±3000	2
IEC[2]	±8000 (contact discharge)	Level 4

[1] All pins to respective GND_x pins, 1.5 kΩ, 100 pF.

[2] LVDS pins to isolated GND_x pins across isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

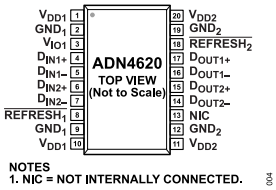

Figure 5. ADN4620 Pin Configuration, SSOP

Table 18. ADN4620 SSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10	V_{DD1}	1.8 V Power Supply for Side 1. Connect both pins externally and bypass to the adjacent GND_1 pins with 0.1 µF capacitors.
2, 9	GND_1	Ground, Side 1.
3	V_{IO1}	3.3 V Input/Output Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
4	D_{IN1+}	Noninverted Differential Input 1.
5	D_{IN1-}	Inverted Differential Input 1.
6	D_{IN2+}	Noninverted Differential Input 2.
7	D_{IN2-}	Inverted Differential Input 2.
8	$\overline{REFRESH_1}$	Active Low Enable for Side 1 Refresh Function. Short to the same PCB ground as GND_1 for normal operation with refresh enabled, or short to the power supply for V_{DD1} for lower power, lower jitter, and quieter operation with refresh disabled.
11, 20	V_{DD2}	1.8 V Power Supply for Side 2. Connect both pins externally and bypass to the adjacent GND_2 pins with 0.1 µF capacitors.
12, 19	GND_2	Ground, Side 2.
13	NIC	Not internally connected.
14	D_{OUT2-}	Inverted Differential Output 2.
15	D_{OUT2+}	Noninverted Differential Output 2.
16	D_{OUT1-}	Inverted Differential Output 1.
17	D_{OUT1+}	Noninverted Differential Output 1.
18	$\overline{REFRESH_2}$	Active Low Enable for Side 1 Refresh Function. Short to the same PCB ground as GND_2 for normal operation with refresh enabled, or short to the power supply for V_{DD2} for lower power, lower jitter, and quieter operation with refresh disabled.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

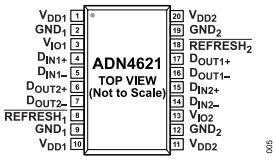

Figure 6. ADN4621 Pin Configuration, SSOP

Table 19. ADN4621 SSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10	V_{DD1}	1.8 V Power Supply for Side 1. Connect both pins externally and bypass to the adjacent GND_1 pins with 0.1 µF capacitors.
2, 9	GND_1	Ground, Side 1.
3	V_{IO1}	3.3 V Input/Output Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
4	D_{IN1+}	Noninverted Differential Input 1.
5	D_{IN1-}	Inverted Differential Input 1.
6	D_{OUT2+}	Noninverted Differential Output 2.
7	D_{OUT2-}	Inverted Differential Output 2.
8	$\overline{REFRESH_1}$	Active Low Enable for Side 1 Refresh Function. Short to the same PCB ground as GND_1 for normal operation with refresh enabled, or short to the power supply for V_{DD1} for lower power, lower jitter, and quieter operation with refresh disabled.
11, 20	V_{DD2}	1.8 V Power Supply for Side 2. Connect both pins externally and bypass to the adjacent GND_2 pins with 0.1 µF capacitors.
12, 19	GND_2	Ground, Side 2.
13	V_{IO2}	3.3 V Input/Output Power Supply for Side 2. Bypass to the adjacent GND_2 pin with a 0.1 µF capacitor.
14	D_{IN2-}	Inverted Differential Input 2.
15	D_{IN2+}	Noninverted Differential Input 2.
16	D_{OUT1-}	Inverted Differential Output 1.
17	D_{OUT1+}	Noninverted Differential Output 1.
18	$\overline{REFRESH_2}$	Active Low Enable for Side 2 Refresh Function. Short to the same PCB ground as GND_2 for normal operation with refresh enabled, or short to the power supply for V_{DD2} for lower power, lower jitter, and quieter operation with refresh disabled.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

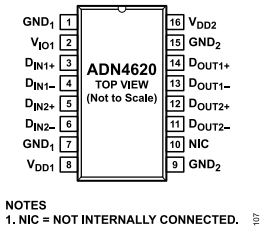

Figure 7. ADN4620 Pin Configuration, SOIC_IC

Table 20. ADN4620 SOIC_IC Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GND_1	Ground, Side 1.
2	V_{IO1}	3.3 V Input/Output Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
3	D_{IN1+}	Noninverted Differential Input 1.
4	D_{IN1-}	Inverted Differential Input 1.
5	D_{IN2+}	Noninverted Differential Input 2.
6	D_{IN2-}	Inverted Differential Input 2.
8	V_{DD1}	1.8 V Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
9, 15	GND_2	Ground, Side 2.
10	NIC	Not internally connected.
11	D_{OUT2-}	Inverted Differential Output 2.
12	D_{OUT2+}	Noninverted Differential Output 2.
13	D_{OUT1-}	Inverted Differential Output 1.
14	D_{OUT1+}	Noninverted Differential Output 1.
16	V_{DD2}	1.8 V Power Supply for Side 2. Bypass to the adjacent GND_2 pin with a 0.1 µF capacitor.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

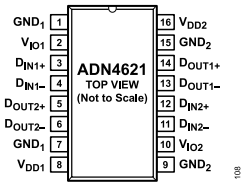

Figure 8. ADN4621 Pin Configuration, SOIC_IC

Table 21. ADN4621 SOIC_IC Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GND_1	Ground, Side 1.
2	V_{IO1}	3.3 V Input/Output Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
3	D_{IN1+}	Noninverted Differential Input 1.
4	D_{IN1-}	Inverted Differential Input 1.
5	D_{OUT2+}	Noninverted Differential Output 2.
6	D_{OUT2-}	Inverted Differential Output 2.
8	V_{DD1}	1.8 V Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
9, 15	GND_2	Ground, Side 2.
10	V_{IO2}	3.3 V Input/Output Power Supply for Side 2. Bypass to the adjacent GND_2 pin with a 0.1 µF capacitor.
11	D_{IN2-}	Inverted Differential Input 2.
12	D_{IN2+}	Noninverted Differential Input 2.
13	D_{OUT1-}	Inverted Differential Output 1.
14	D_{OUT1+}	Noninverted Differential Output 1.
16	V_{DD2}	1.8 V Power Supply for Side 2. Bypass to the adjacent GND_2 pin with a 0.1 µF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD1} = V_{DD2} = 1.8 V, T_A = 25°C, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2, R_L = 100 Ω, 1.25 GHz clock input with $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, and t_R and t_F < 0.05 ns, unless otherwise noted.

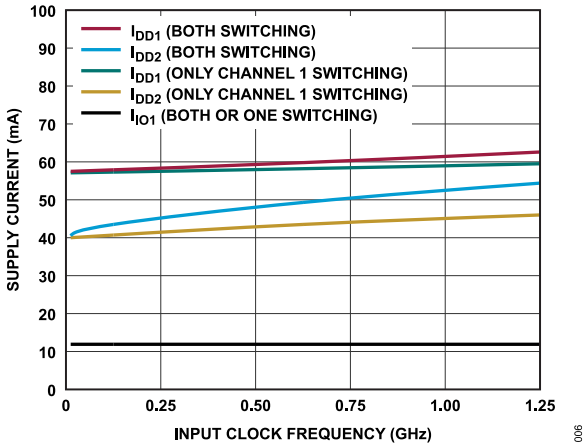

Figure 9. Supply Current vs. Input Clock Frequency, ADN4620

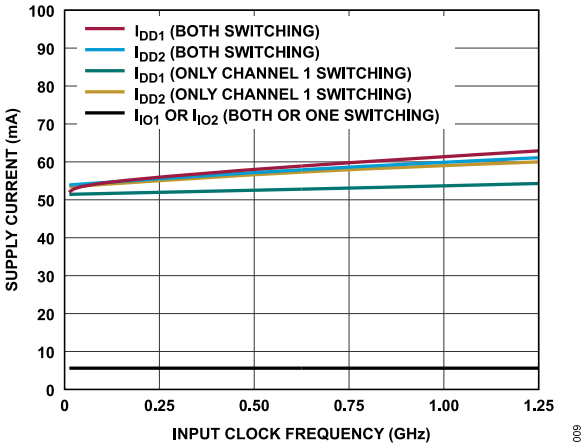

Figure 12. Supply Current vs. Input Clock Frequency, ADN4621

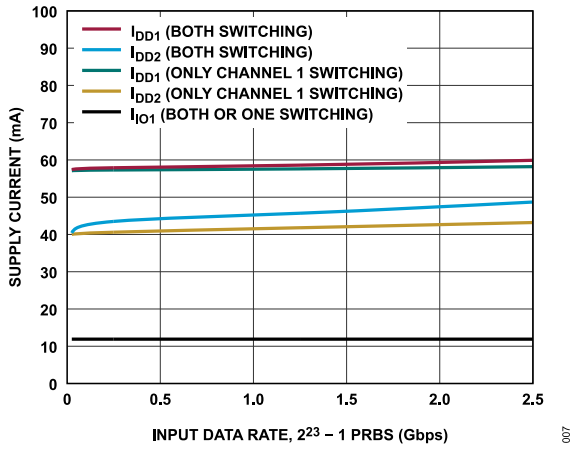

Figure 10. Supply Current vs. Input Data Rate, 2^{23} − 1 PRBS, ADN4620

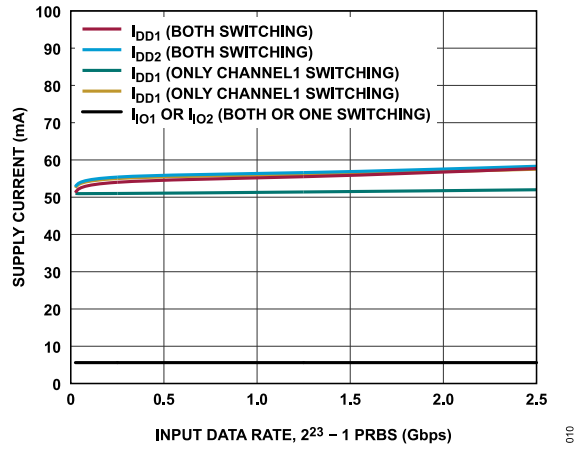

Figure 13. Supply Current vs. Input Data Rate, 2^{23} − 1 PRBS, ADN4621

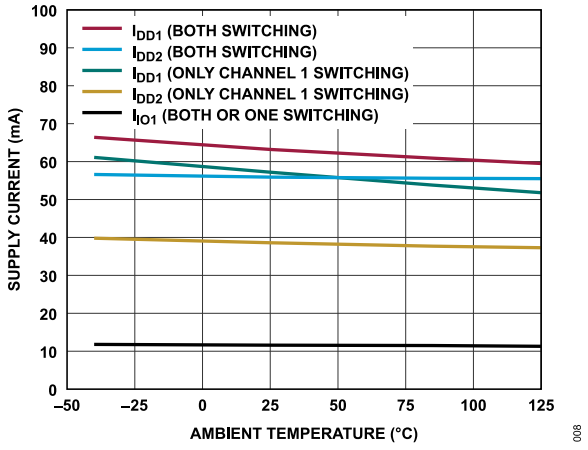

Figure 11. Supply Current vs. Ambient Temperature, ADN4620

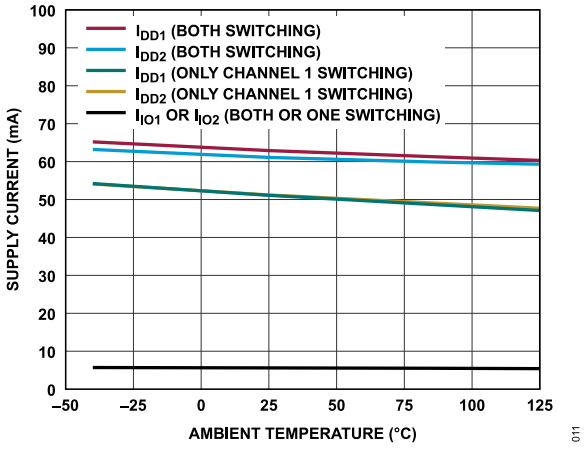

Figure 14. Supply Current vs. Ambient Temperature, ADN4621

TYPICAL PERFORMANCE CHARACTERISTICS

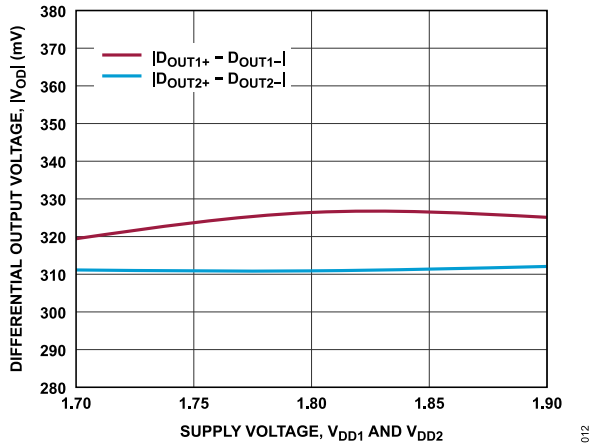

Figure 15. Differential Output Voltage, $|V_{OD}|$ vs. Supply Voltage, V_{DD1} and V_{DD2}

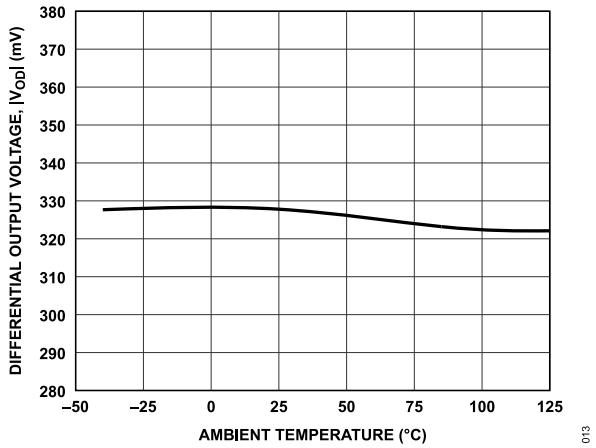

Figure 16. Differential Output Voltage, $|V_{OD}|$ vs. Ambient Temperature

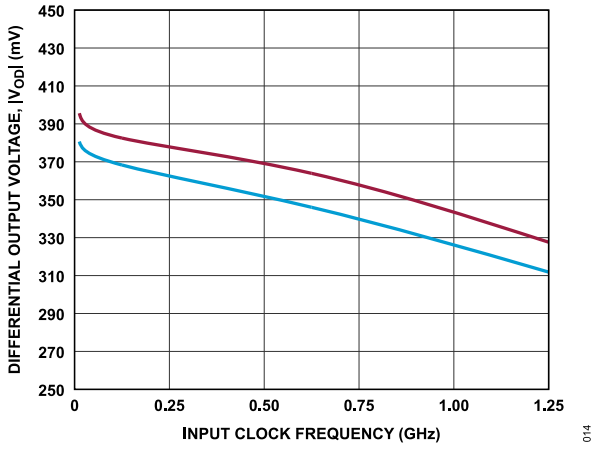

Figure 17. Differential Output Voltage, $|V_{OD}|$ vs. Input Clock Frequency

Figure 18. Differential Output Voltage, $|V_{OD}|$ vs. Output Load, R_L (DC Input)

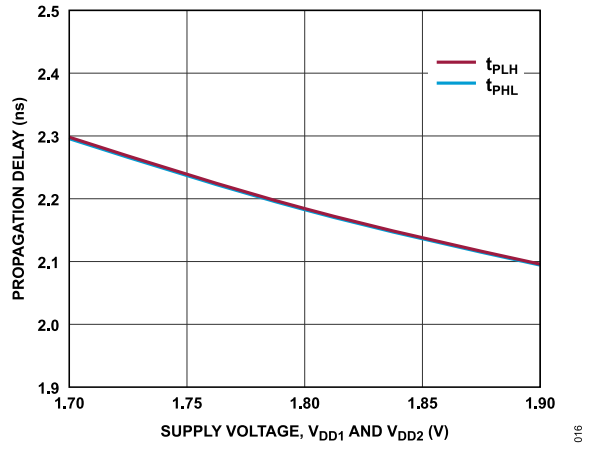

Figure 19. Propagation Delay vs. Supply Voltage, V_{DD1} and V_{DD2}

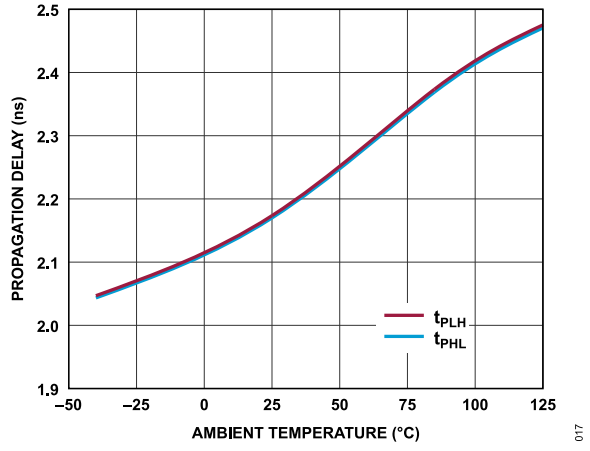

Figure 20. Propagation Delay vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

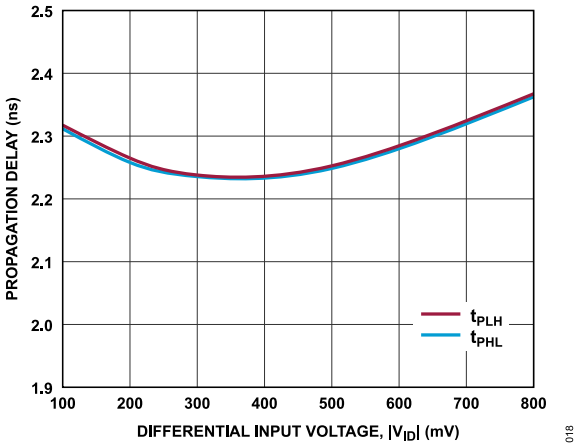

Figure 21. Propagation Delay vs. Differential Input Voltage, $|V_{ID}|$

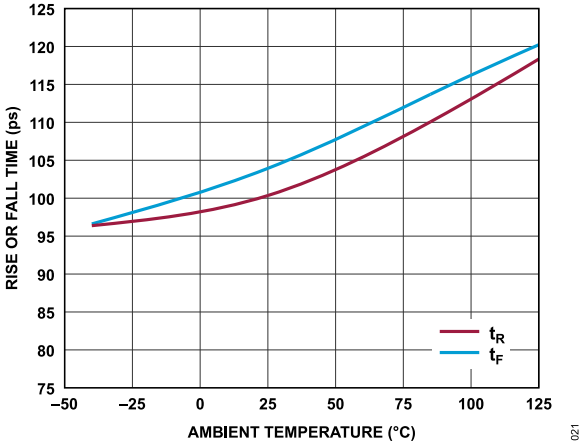

Figure 24. Rise or Fall Time vs. Ambient Temperature

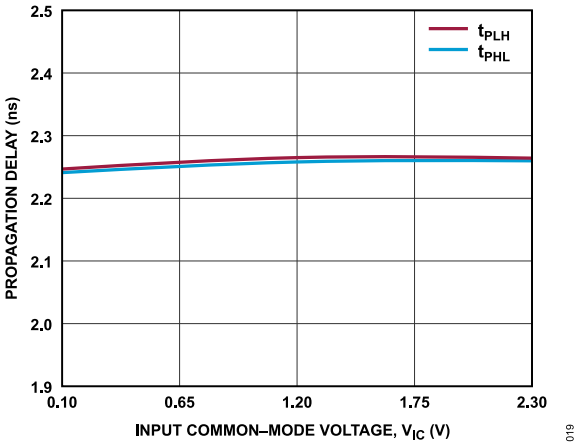

Figure 22. Propagation Delay vs. Input Common-Mode Voltage, V_{IC}

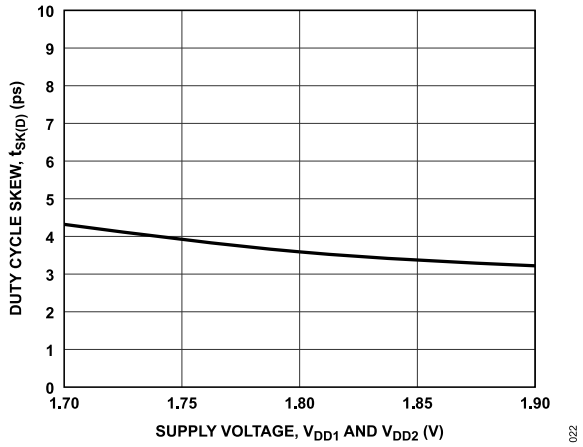

Figure 25. Duty Cycle Skew, $t_{SK(D)}$ vs. Supply Voltage, V_{DD1} and V_{DD2}

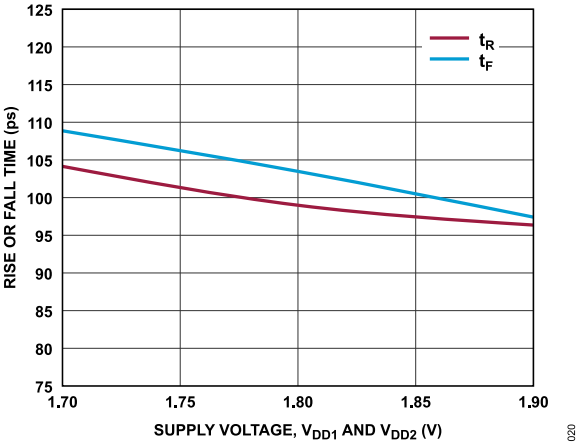

Figure 23. Rise or Fall Time vs. Supply Voltage, V_{DD1} and V_{DD2}

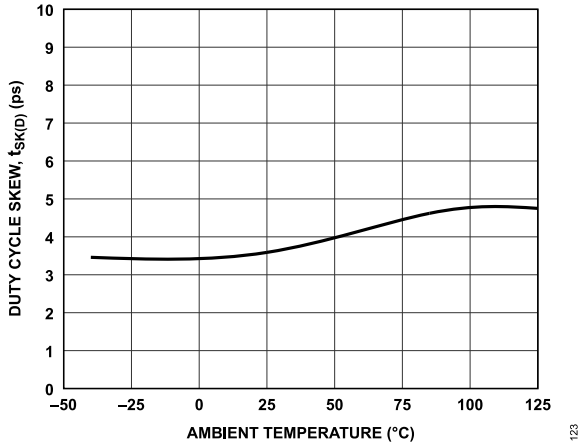

Figure 26. Duty Cycle Skew, $t_{SK(D)}$ vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

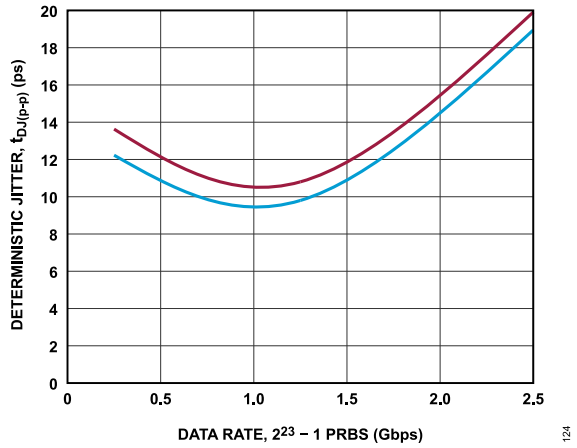

Figure 27. Deterministic Jitter, $t_{DJ(p-p)}$ vs. Data Rate, 2^{23} – 1 PRBS

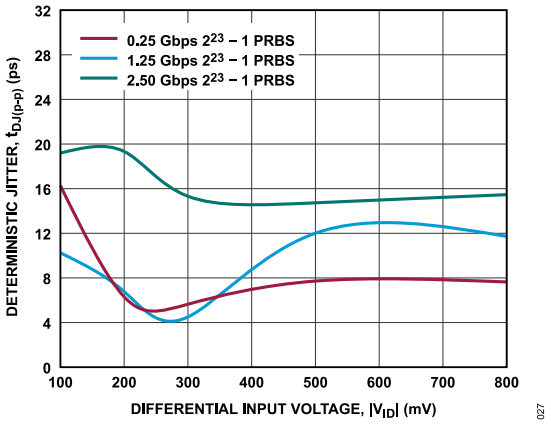

Figure 30. Deterministic Jitter, $t_{DJ(p-p)}$ vs. Differential Input Voltage, $|V_{ID}|$

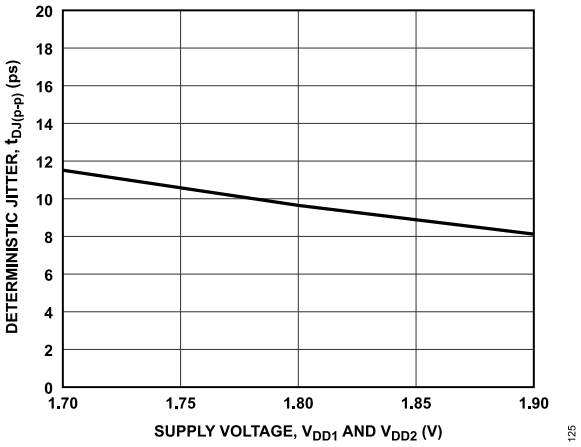

Figure 28. Deterministic Jitter, $t_{DJ(p-p)}$ vs. Supply Voltage, V_{DD1} and V_{DD2}

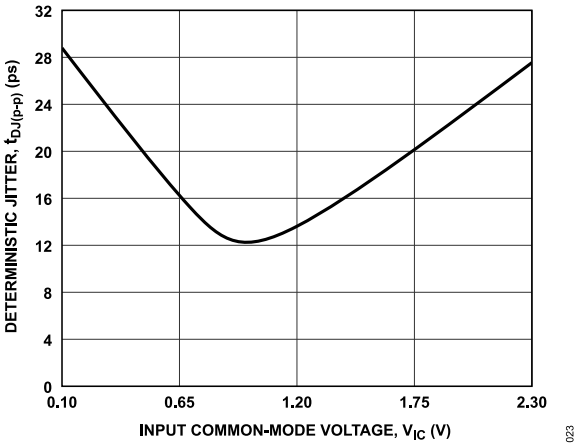

Figure 31. Deterministic Jitter, $t_{DJ(p-p)}$ vs. Input Common-Mode Voltage, V_{IC}

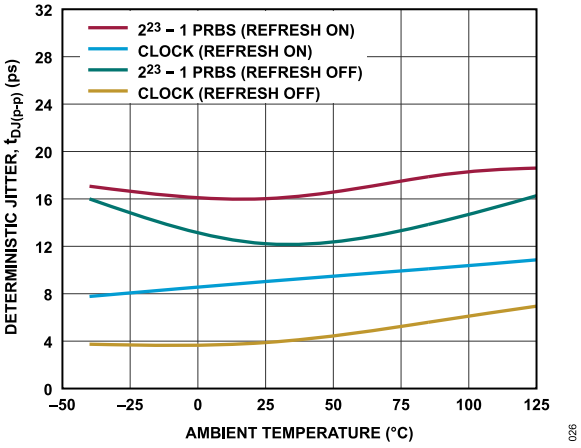

Figure 29. Deterministic Jitter, $t_{DJ(p-p)}$ vs. Ambient Temperature

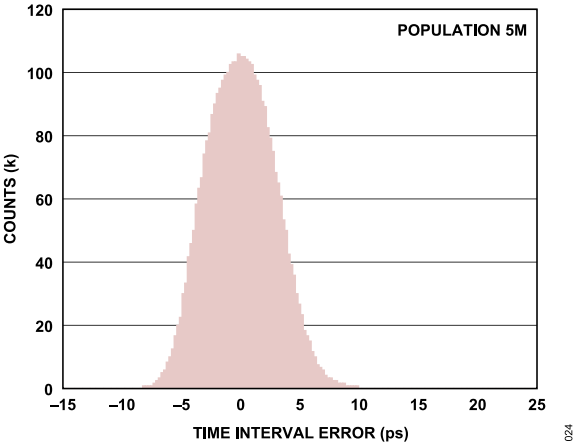

Figure 32. Time Interval Error (TIE) Histogram for $D_{OUT1\pm}$ at 1.25 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

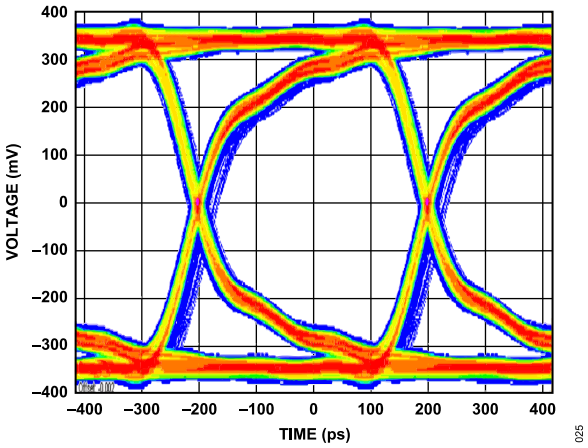

Figure 33. Eye Diagram for $D_{OUT1\pm}$ at 1.25 GHz

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

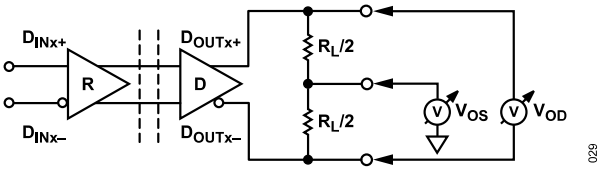

Figure 34. Driver Test Circuit

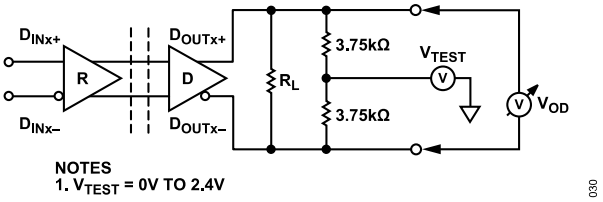

Figure 35. Driver Test Circuit (Full Load Across Common-Mode Range)

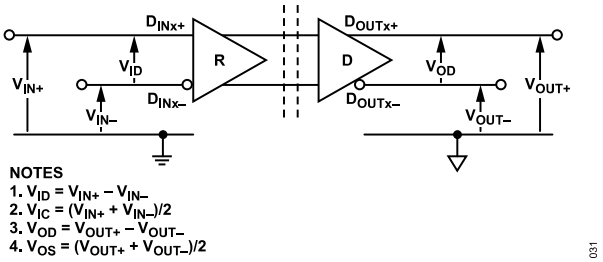

Figure 36. Voltage Definitions

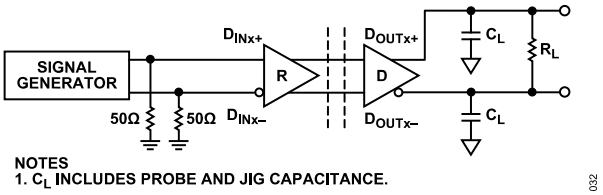

Figure 37. Timing Test Circuit

THEORY OF OPERATION

The ADN4620/ADN4621 are high speed, differential signal isolators capable of switching up to 2.5 Gbps with signal levels compliant to TIA/EIA-644-A. The devices couple differential signals applied to the LVDS receiver inputs across the isolation barrier to the outputs on the other side and retransmit the bit stream or clock as LVDS. This integration allows drop-in isolation of LVDS signal chains and isolation of other signals, such as CML.

The LVDS receiver detects the differential voltage present across a termination resistor on an LVDS input. An integrated digital isolator transmits the input state across the isolation barrier, and an LVDS driver outputs the same state as the input.

When there is a positive differential voltage of ≥100 mV across a termination resistor between any D_{INx+} pin and a corresponding D_{INx-} pin, the corresponding D_{OUTx+} pin sources current. This current flows across the connected transmission line and termination at the receiver at the far end of the bus, while the D_{OUTx-} pin sinks the return current. When there is a negative differential voltage of ≤−100 mV across any $D_{INx\pm}$ pin, the corresponding D_{OUTx+} pin sinks current while the D_{OUTx-} pin sources the current. Table 22 shows these input and output combinations.

The output drive current is between ±2.5 mA and ±4.5 mA (typically ±3.1 mA), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor (R_T). The received voltage is centered around 1.2 V. Because the differential voltage (V_{ID}) reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage magnitude ($|V_{ID}|$).

ISOLATION AND REFRESH

In response to any change in the input state detected by the integrated LVDS receiver, an encoder circuit sends narrow (~1 ns) pulses to a decoder circuit using integrated transformer coils. The decoder is bistable and is, therefore, either set or reset by the pulses that indicate input transitions. The decoder state determines the LVDS driver output state in normal operation, which reflects the isolated LVDS buffer input state.

For normal operation of the ADN4620/ADN4621, the active low enable pins on the SSOP models, $\overline{REFRESH_1}$ and $\overline{REFRESH_2}$, are shorted to the same respective PCB grounds as the GND_1 and GND_2 pins to enable a refresh function. When enabled, this function means that in the absence of input transitions for more than approximately 1 µs, a periodic set of refresh pulses, indicative of the correct input state, ensures dc correctness at the output (including the fail-safe output state, if applicable). This function is permanently enabled for the SOIC_IC models.

On power-up, the output state may initially be in the incorrect dc state if there are no input transitions. The output state is corrected within 1 µs by the refresh pulses.

If the decoder receives no internal pulses for more than approximately 1 µs, the device assumes that the input side is unpowered or nonfunctional, in which case the output is set to a positive differential voltage (logic high).

For clocks, constant bit streams, or protocols with error correction, the refresh functionality may not be required. If the $\overline{REFRESH_1}$ and $\overline{REFRESH_2}$ pins on the SSOP models are shorted to the same respective power supplies as the V_{DD1} and V_{DD2} pins, the refresh functionality is disabled, allowing for lower power operation with no internal clock-like signals (potentially reducing conducted or radiated emissions). In this mode of operation, a new data transition at the input may be required to correct the output state, either after power-up or after a common-mode transient event beyond the guaranteed common-mode transient immunity specification.

TRUTH TABLE

The LVDS standard, TIA/EIA-644-A, defines normal receiver operation under two conditions: an input differential voltage of ≥+100 mV corresponding to one logic state, and a voltage of ≤−100 mV for the other logic state. Between these thresholds, the standard LVDS receiver operation is undefined (the LVDS receiver can detect either state), as shown in Table 22.

Table 22. Input and Output Operation

Input ($D_{INx\pm}$)			Output ($D_{OUTx\pm}$)		
Powered On	**V_{ID} (mV)**	**Logic**	**Powered On**	**V_{OD} (mV)**	**Logic**
Yes	≥100	High	Yes	≥250	High
Yes	≤−100	Low	Yes	≤−250	Low
Yes	$-100 < V_{ID} < +100$	Indeterminate	Yes	Indeterminate	Indeterminate
No	Don't care	Don't care	Yes	≥250	High

APPLICATIONS INFORMATION

PCB LAYOUT

The ADN4620/ADN4621 can operate with high speed LVDS signals up to a 1.25 GHz clock, or a 2.5 Gbps nonreturn to zero (NRZ) data. When operating with such high frequencies, apply best practices for the LVDS trace layout and termination. Place 100 Ω termination resistors as close as possible to the receivers, across the D_{INx+} pins and D_{INx-} pins.

Controlled impedance traces (100 Ω differential) are needed on LVDS signal lines for full signal integrity, reduced system jitter, and for minimizing electromagnetic interference (EMI) from the PCB. Trace widths, lateral distance within each pair of traces, and distance to the ground plane underneath all trace pairs must be chosen appropriately. Via fencing to the PCB ground between pairs is also a best practice to minimize crosstalk between adjacent pairs.

The ADN4620/ADN4621 in SSOP package have passed EN 55032 Class B emissions limits when operating with up to 2.5 Gbps PRBS data, using a high speed PCB design with an embedded PCB stitching capacitor (constructed by overlapping internal PCB Layer 2 and Layer 3 under the area of the isolator). Similarly the ADN4620 in SOIC_IC package has passed EN 55032 Class B emissions limits up to 2.1 Gbps, and ADN4621 in SOIC_IC up to 0.9 Gbps. Depending on the system design, or when isolating for high speed clocks, other EMC mitigation measures may be required to provide a sufficient margin below Class B emissions limits.

The best practice for high speed PCB design can minimize emissions from traces with high speed LVDS signals. However, trace lengths can be modified to avoid resonances at specific frequencies when the traces act as an antenna for switching noise. Special care is recommended for off-board connections, where switching transients from high speed LVDS signals (and clocks in particular) may conduct onto cabling, resulting in radiated emissions. Use common-mode chokes, ferrites, or other filters as appropriate at LVDS connectors and power supplies, as well as cable shield or PCB ground connections to earth or chassis.

The ADN4620/ADN4621 require appropriate decoupling of the V_{DDx} pins with 100 nF capacitors. Power supplies must also have appropriate filtering to avoid possible radiated emissions due to high frequency switching noise.

APPLICATION EXAMPLES

High speed LVDS interfaces for the analog front-end (AFE), processor to processor serial communication, or video and imaging data can be isolated using the ADN4620/ADN4621 between components, between PCBs, or at a cable interface.

The ADN4620/ADN4621 provide the galvanic isolation required for robust external ports, and the low jitter and high drive strength of the devices allow communication along short cable runs of a few meters. High common-mode immunity ensures communication integrity even in harsh, noisy environments, and isolation can protect against electromagnetic compatibility (EMC) transients up to ±7 kV_{PEAK} for ESD, and ±6.25 kV_{PEAK} for surge.

Standard LVDS inputs and outputs allow simple integration into high speed signal chains using field-programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs), redrivers, or coupling networks to interface to CML and other physical layers.

Isolated AFE applications provide an example of the ADN4620/ADN4621 isolating an LVDS interface between components. As shown in Figure 38, two ADN4621 components isolate the LVDS interface of the ADAQ23876 µmodule data acquisition solution, including 800 Mbps data, 400 MHz echoed clock, and a 15 MHz sample clock. The ADN4621 additive phase jitter is sufficiently low that it does not affect the analog-to-digital converter (ADC) performance even when isolating the sample clock. In addition, implementing the galvanic isolation improves ADC performance by removing digital and power supply noise from the FPGA/ASIC circuit.

PCB to PCB connections and even cable interfaces can leverage LVDS signaling for high bandwidth links with low latency synchronous data transfer. Serialized gigabit Ethernet connections can be isolated to robustly cascade Ethernet or multiprotocol switches for industrial controller communication modules, as shown in Figure 39. The ADN4621 isolates the 1.25 Gbps transmit and receive signal for two ports at each node to create a daisy chain topology. The propagation delay of just over a couple of nanoseconds provides the low latency needed for industrial automation and process control.

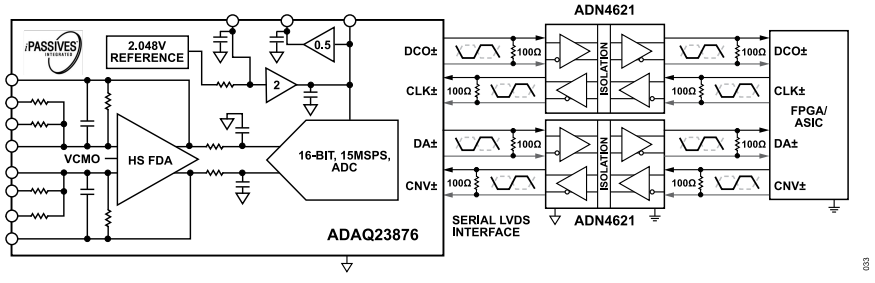

Figure 38. Isolated Analog Front-End Implementation Example (Isolated ADAQ23876 Using the ADN4621)

APPLICATIONS INFORMATION

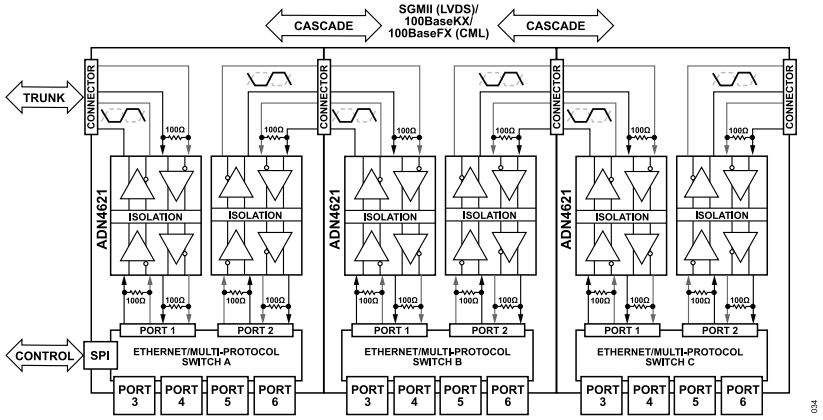

Figure 39. Isolated Serial Communication Example (Isolated Serial Gigabit Ethernet Switch Cascaded Using ADN4621)

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the device is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large, either to falsely set or reset the decoder. The following analysis defines such conditions. The ADN4620/ADN4621 is examined in a 1.7 V operating condition because this operating condition represents the most susceptible mode of operation for these products.

The pulses at the transformer output have an amplitude greater than 0.35 V. The decoder has a sensing threshold of about 0.11 V, therefore establishing a 0.24 V margin in which induced voltages are tolerated.

The voltage (V) induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N \quad (1)$$

where:

$d\beta$ is the change in magnetic flux density.

dt is the change in time.

r_n is the radius of the n^{th} turn in the receiving coil.

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADN4620/ADN4621 and an imposed requirement that the induced voltage be, at most, 50% of the 0.11 V threshold at the decoder, a maximum allowable external magnetic flux density is calculated as shown in Figure 40.

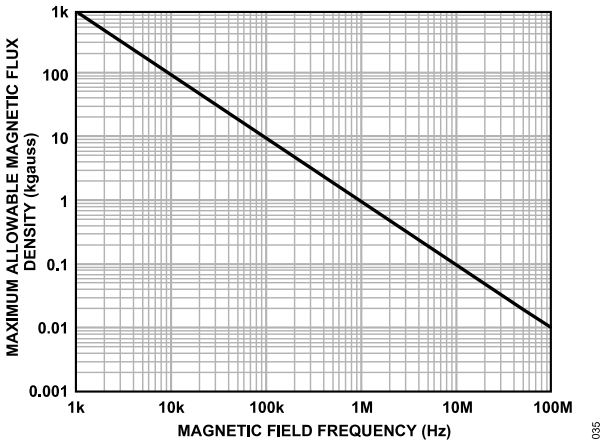

Figure 40. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 1.06 kgauss induces a voltage of 0.055 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs with the worst case polarity during a transmitted pulse, the applied magnetic field reduces the received pulse from >0.35 V

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to 0.295 V. This voltage is still higher than the 0.11 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADN4620/ADN4621 transformers. Figure 41 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADN4620/ADN4621 is insensitive to external fields. Only extremely large, high frequency currents that are close to the component can potentially be a concern. For the 1 MHz example noted, a 2.64 kA current must be placed 5 mm from the ADN4620/ADN4621 to affect component operation.

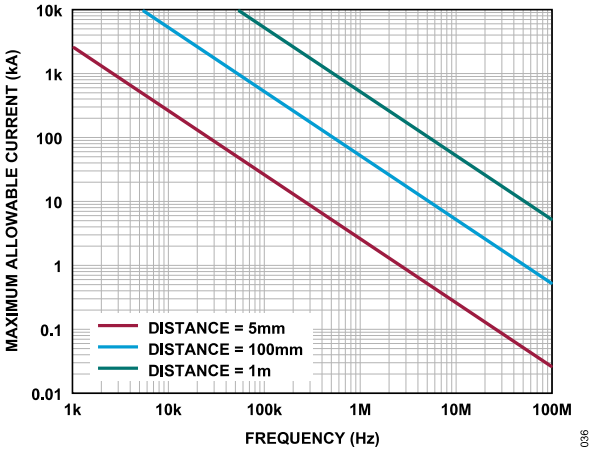

Figure 41. Maximum Allowable Current for Various Current to ADN4620/ ADN4621 Spacings

In combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Avoid PCB structures that form loops.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, which allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation barrier, pollution degree, and material group. The material group and creepage for ADN4620/ADN4621 are detailed in Table 4.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the thickness of the insulation, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this type of waveform reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the isolation barrier, as shown in Equation 2. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 3. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (2)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (3)$$

where:

V_{RMS} is the total rms working voltage.

$V_{AC\ RMS}$ is the time varying portion of the working voltage.

V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clear-

APPLICATIONS INFORMATION

ance, and lifetime of a device, see Figure 42 and the following equations.

The working voltage across the barrier from Equation 2 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (4)$$

$$V_{RMS} = \sqrt{240^2 + 400^2} \quad (5)$$

V_{RMS} = 466 V

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 3.

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (6)$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2} \quad (7)$$

$V_{AC\ RMS}$ = 240 V rms

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. Table 14 compares the value to the limits for the working voltage for the expected lifetime. Note that the dc working voltage limit in Table 14 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

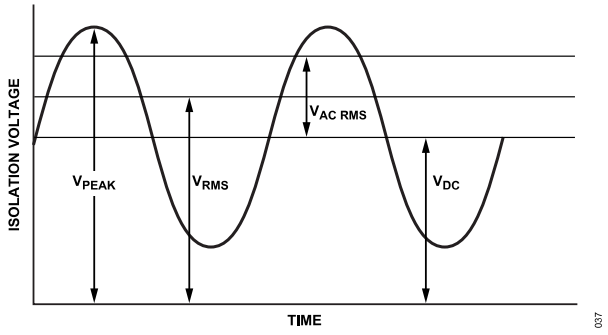

Figure 42. Critical Voltage Example

OUTLINE DIMENSIONS

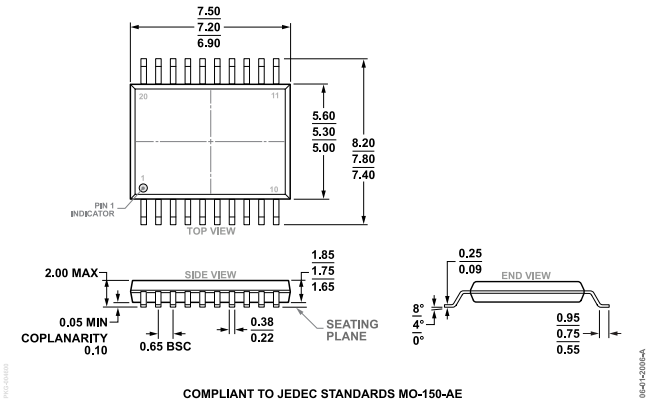

Figure 43. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

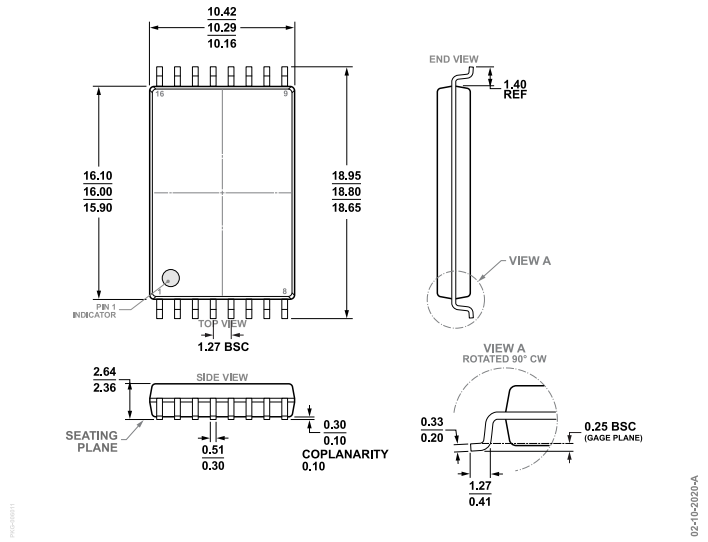

Figure 44. 16-Lead Standard Small Outline Package, with 15.1 mm Creepage [SOIC_IC]
Wide Body
(RI-16-3)
Dimensions shown in millimeters

Updated: September 01, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADN4620BRIZ	-40°C to +125°C	SOIC INCREASED CREEPAGE		RI-16-3
ADN4620BRIZ-RL	-40°C to +125°C	SOIC INCREASED CREEPAGE	Reel, 500	RI-16-3
ADN4620BRSZ	-40°C to +125°C	20-Lead SSOP		RS-20
ADN4620BRSZ-RL	-40°C to +125°C	20-Lead SSOP	Reel, 1500	RS-20
ADN4621BRIZ	-40°C to +125°C	SOIC INCREASED CREEPAGE		RI-16-3
ADN4621BRIZ-RL	-40°C to +125°C	SOIC INCREASED CREEPAGE	Reel, 500	RI-16-3
ADN4621BRSZ	-40°C to +125°C	20-Lead SSOP		RS-20
ADN4621BRSZ-RL	-40°C to +125°C	20-Lead SSOP	Reel, 1500	RS-20

[1] Z = RoHS Compliant Part.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Table 23.

Model[1]	Description
EVAL-ADN4620EBZ	ADN4620 SSOP Evaluation Board
EVAL-ADN4621EBZ	ADN4621 SSOP Evaluation Board

[1] Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADN4620BRSZ ADN4620BRSZ-RL EVAL-ADN4620EBZ ADN4620BRIZ ADN4620BRIZ-RL