

FEATURES

Gain: 24 dB typical
Output power for 1 dB compression: 28 dBm typical
Saturated output power: 29 dBm typical
Output third-order intercept: 34 dBm typical
Input return loss: 18 dB typical
Output return loss: 10 dB typical
DC supply: 4 V at 800 mA
No external matching required
Die size: 2.999 mm × 3.999 mm × 0.05 mm

APPLICATIONS

E-band communication systems
High capacity wireless backhaul radio systems
Test and measurement

GENERAL DESCRIPTION

The ADMV7710 is an integrated, E-band, gallium arsenide (GaAs), pseudomorphic, high electron mobility transfer (pHEMT), mono-lithic microwave integrated circuit (MMIC), medium power amplifier with an on-chip, temperature compensated power detector that operates from 71 GHz to 76 GHz. The ADMV7710 provides 24 dB of gain, 28 dBm of output power at 1 dB compression, and 29 dBm of saturated output power at 20% power added efficiency from a 4 V power supply. The ADMV7710 exhibits excellent linearity and is optimized for E-band communications and high capacity, wireless backhaul radio systems. The amplifier configuration and high gain make the device an excellent candidate for last stage signal amplification before the antenna. All data is taken with the chip in a 50 Ω test fixture connected via a 3 mil wide × 0.5 mil thick × 7 mil long ribbon on each port. The ADMV7710 is available in a 40-pad bare die (CHIP) and operates over the -55°C to $+85^{\circ}\text{C}$ temperature range.

FUNCTIONAL BLOCK DIAGRAM

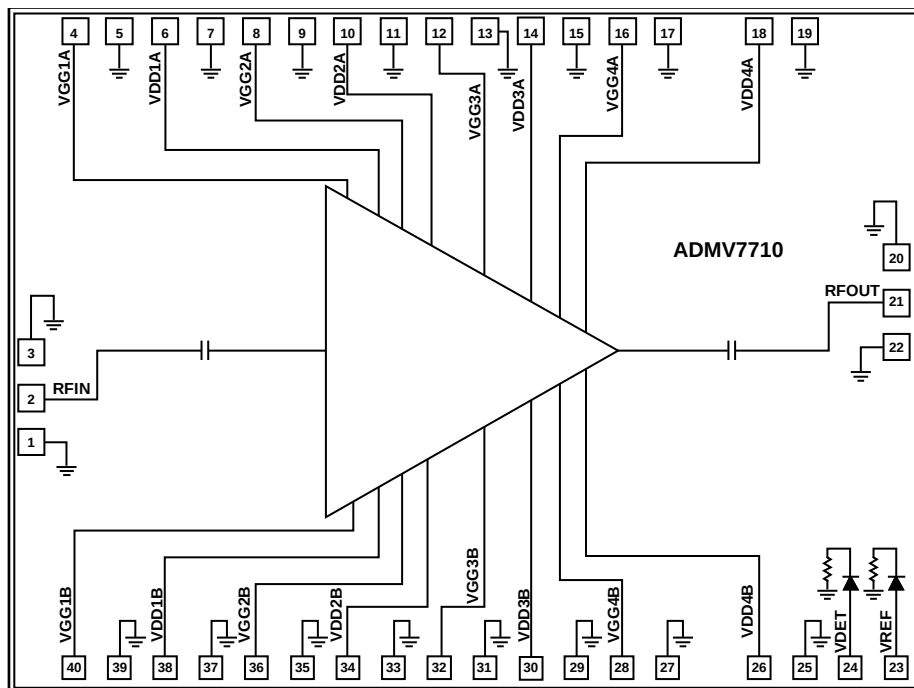


Figure 1.

Rev. A

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REVISION HISTORY

12/2018—Rev. 0 to Rev. A

Changes to Figure 42	12
Changes to Figure 43 and Figure 44	13
Added Figure 45; Renumbered Sequentially	13
Changes to Ordering Guide	18

3/2018—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, V_{DDxA} and $V_{DDxB} = 4\text{ V}$, $I_{DD} = 800\text{ mA}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Frequency Range		71		76	GHz
PERFORMANCE					
Gain		21	24		dB
Gain Variation over Temperature			0.02		dB/ $^\circ\text{C}$
Output Power for 1 dB Compression	OP1dB	26	28		dBm
Saturated Output Power	P_{SAT}		29		dBm
Output Third-Order Intercept at Maximum Gain ¹	OIP3		34		dBm
Power Added Efficiency	PAE		20		%
Input Return Loss			18		dB
Output Return Loss			10		dB
POWER SUPPLY					
Total Drain Current ²	I_{DD}		800		mA

¹ Data taken at output power (P_{OUT}) = 14 dBm per tone, 1 MHz spacing.

² Adjust the VGGxA and VGGxB pads from -2 V to 0 V to achieve the total drain current (I_{DD}) = 800 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (VDD1A to VDD4A, VDD1B to VDD4B)	4.5 V
Gate Bias Voltage (VGG1A to VGG4A, VGG1B to VGG4B)	–3 V to 0 V
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	175°C
Operating Temperature Range	–55°C to +85°C
Storage Temperature Range	–65°C to +150°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	150 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case (or die to package) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}^1	Unit
C-40-2	24.2	°C/W

¹ Based on the ATROX 800HT1V[®] as the die attach epoxy.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADMV7710
TOP VIEW
(Not to Scale)

Pin	Signal
1	GND
2	RFIN
3	GND
4	VGG1A
5	GND
6	VDD1A
7	GND
8	VGG2A
9	GND
10	VDD2A
11	GND
12	VGG3A
13	GND
14	VDD3A
15	GND
16	VGG4A
17	GND
18	VDD4A
19	GND
20	GND
21	RFOUT
22	GND
23	VDD4B
24	GND
25	VDET
26	VREF
27	GND
28	VDD4B
29	GND
30	VDD3B
31	GND
32	VGG3B
33	GND
34	VDD2B
35	GND
36	VGG2B
37	GND
38	VDD1B
39	GND
40	VGG1B

16400

Pad No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 20, 22, 25, 27, 29, 31, 33, 35, 37, 39	GND	Ground Connection (See Figure 3).
2	RFIN	RF Input. AC-couple RFIN and match it to 50 Ω (see Figure 4).
4, 8, 12, 16	VGG1A to VGG4A	First Stage Gate Bias Voltage for the Power Amplifier (See Figure 8). For the required external components, see Figure 47.
6, 10, 14, 18	VDD1A to VDD4A	First Stage Drain Bias Voltage for the Power Amplifier (See Figure 5).
21	RFOUT	RF Output. AC-couple RFOUT and match it to 50 Ω (see Figure 6).
23	VREF	Reference Voltage for the Power Detector (See Figure 7). VREF is the dc bias of the diode biased through an external resistor used for temperature compensation of VDET. Refer to the typical application circuit (see Figure 47) for the required external components.
24	VDET	Detector Voltage for the Power Detector (See Figure 7). VDET is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit (see Figure 47) for the required external components.
26, 30, 34, 38	VDD4B to VDD1B	Second Stage Drain Bias Voltage for the Power Amplifier (See Figure 5).
28, 32, 36, 40	VGG4B to VGG1B	Second Stage Gate Bias Voltage for the Power Amplifier (See Figure 8). For the required external components, see Figure 47.
Die Bottom	GND	Ground. The die bottom must be connected to the RF/dc ground (see Figure 3).

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

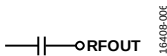


Figure 6. RFOUT Interface Schematic

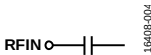


Figure 4. RFIN Interface Schematic



Figure 7. VREF, VDET Interface Schematic

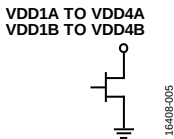


Figure 5. VDD1A to VDD4A and VDD1B to VDD4B Interface Schematic

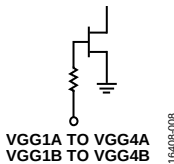
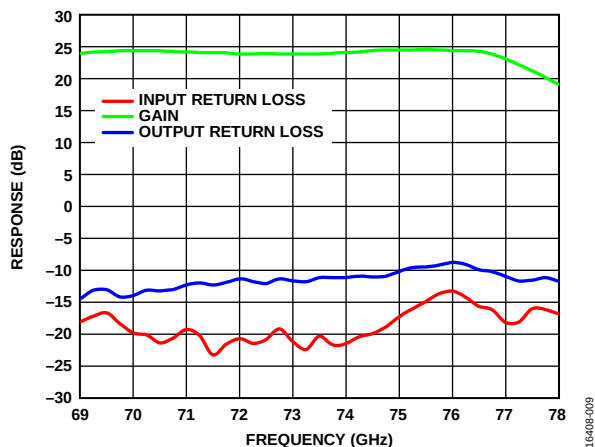
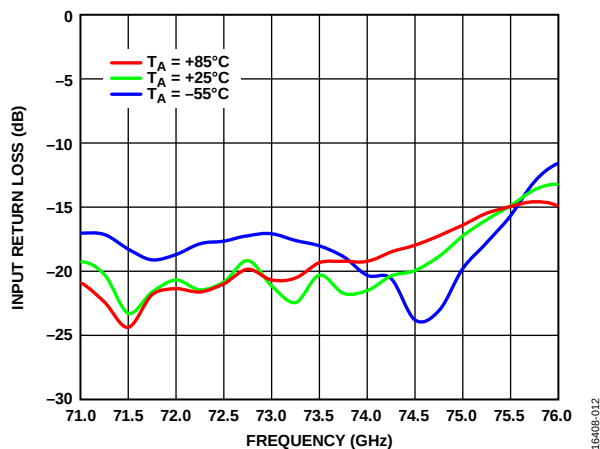
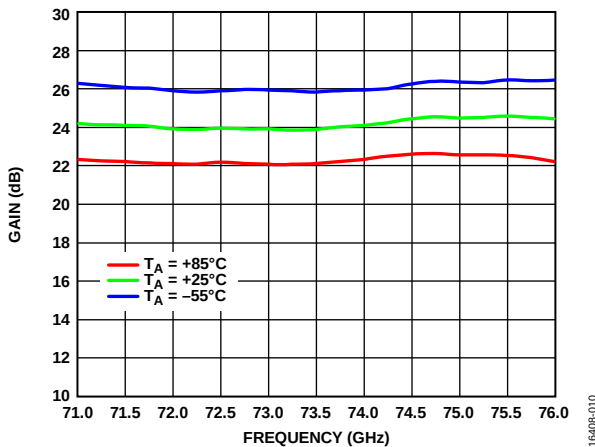
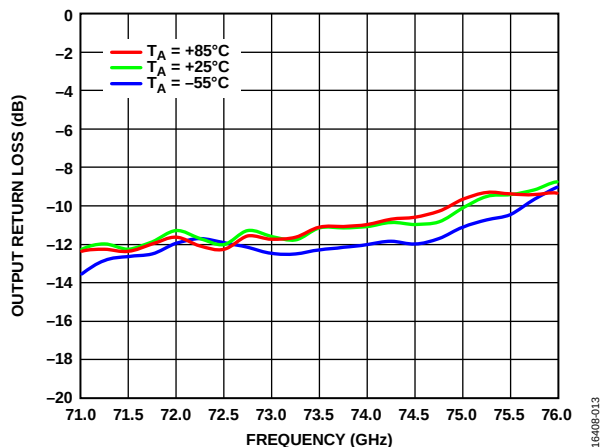
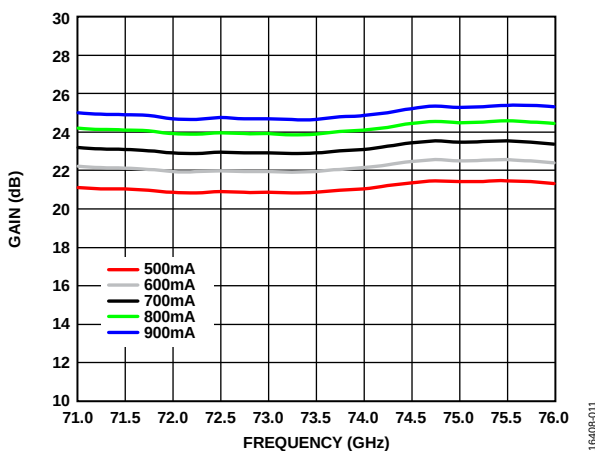
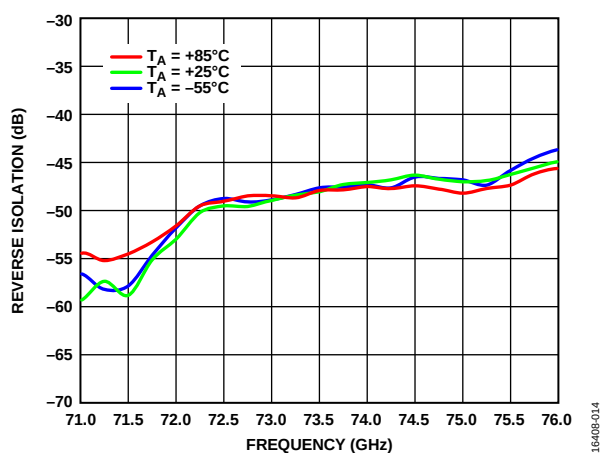


Figure 8. VGG1A to VGG4A and VGG1B to VGG4B Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 9. Broadband Gain and Return Loss Response vs. Frequency, $I_{DD} = 800$ mAFigure 12. Input Return Loss vs. Frequency over Various Temperatures, $I_{DD} = 800$ mAFigure 10. Gain vs. Frequency over Various Temperatures, $I_{DD} = 800$ mAFigure 13. Output Return Loss vs. Frequency over Various Temperatures, $I_{DD} = 800$ mAFigure 11. Gain vs. Frequency over I_{DD} Figure 14. Reverse Isolation vs. Frequency over Various Temperatures, $I_{DD} = 800$ mA

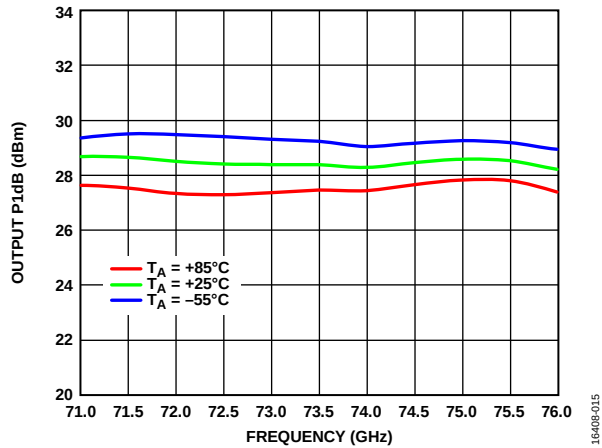


Figure 15. Output P1dB vs. Frequency over Various Temperatures, $I_{DD} = 800$ mA

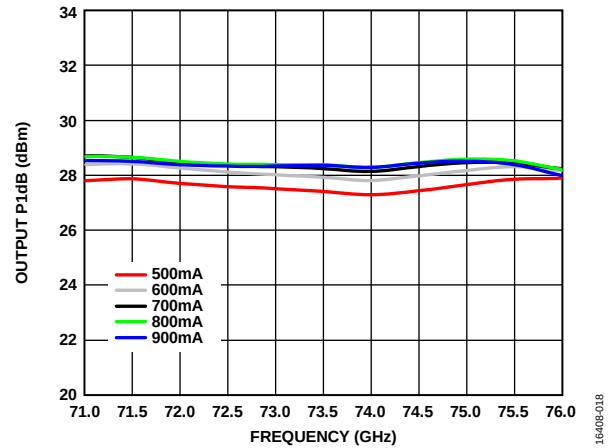


Figure 18. Output P1dB vs. Frequency over I_{DD}

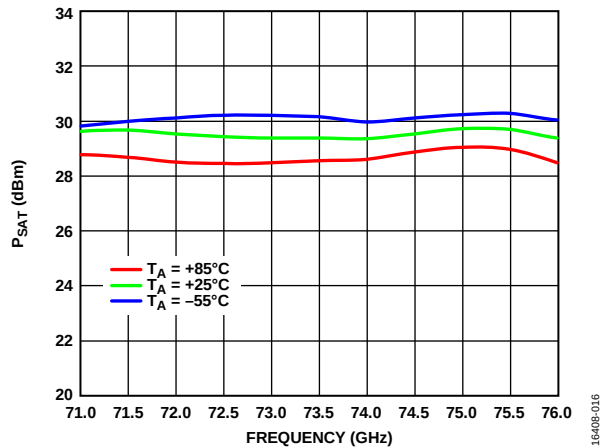


Figure 16. P_{SAT} vs. Frequency over Various Temperatures, $I_{DD} = 800$ mA

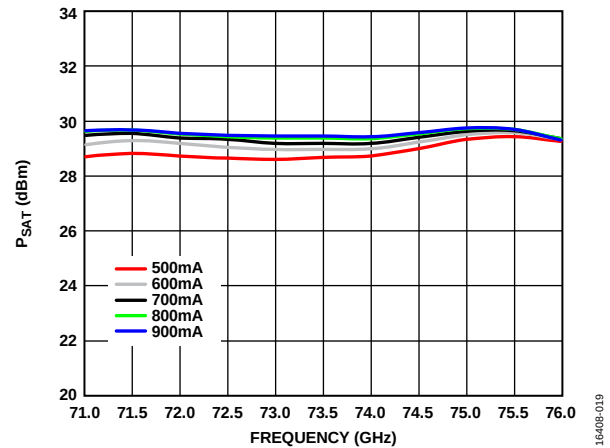


Figure 19. P_{SAT} vs. Frequency over I_{DD}

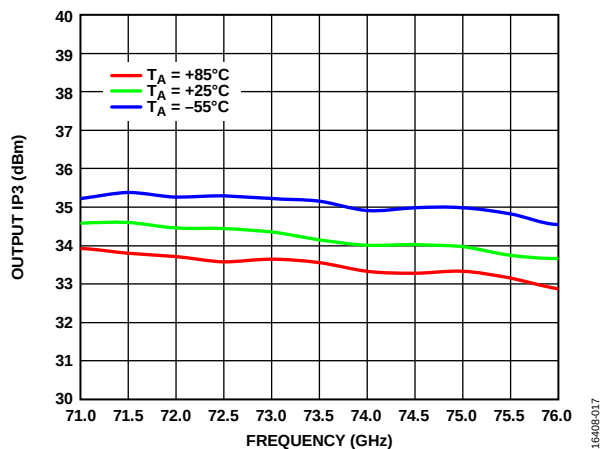


Figure 17. Output IP3 vs. Frequency over Various Temperatures, $I_{DD} = 800$ mA, P_{OUT} per Tone = 14 dBm

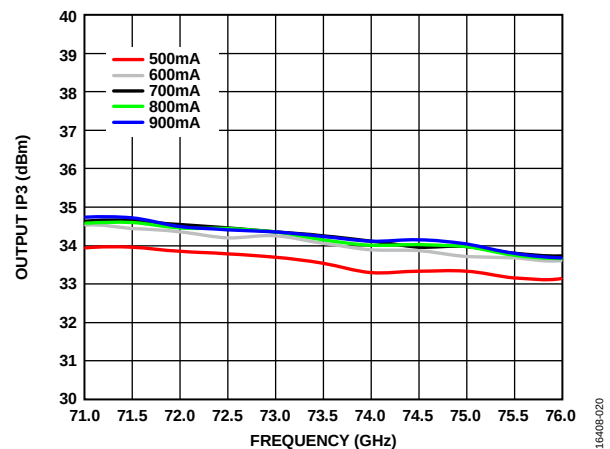
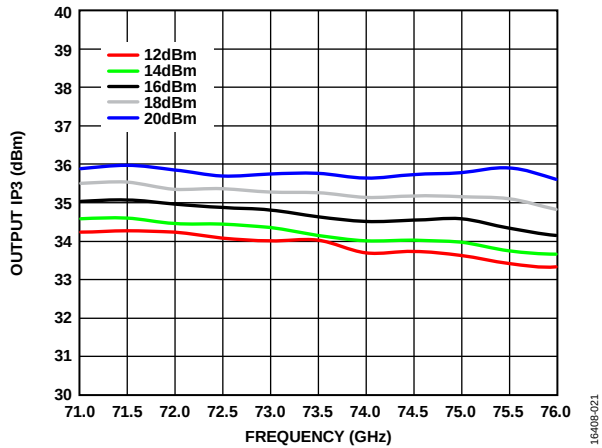
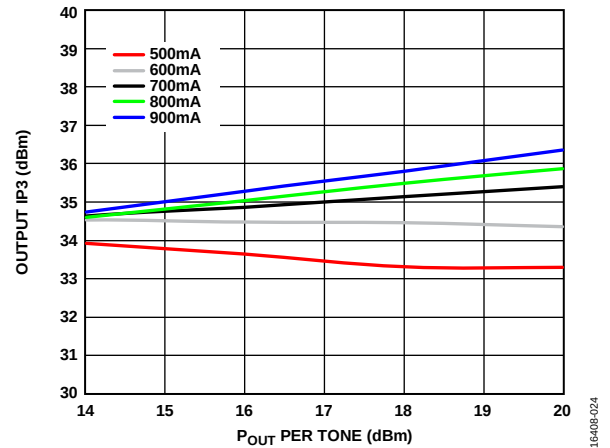
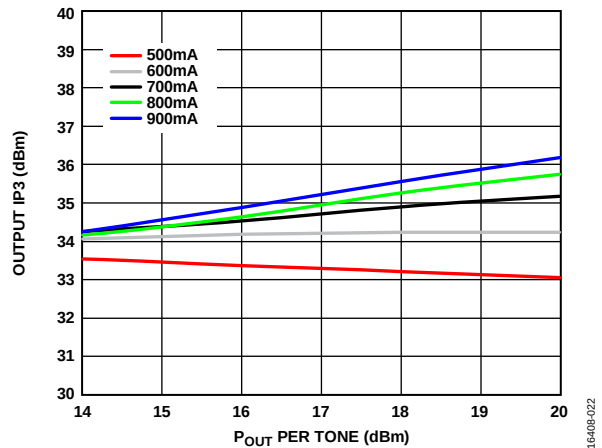
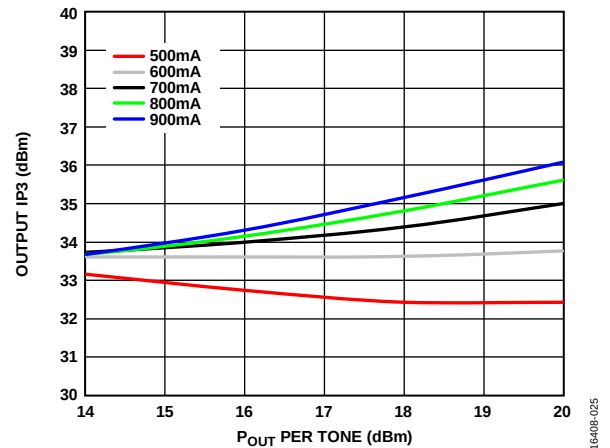
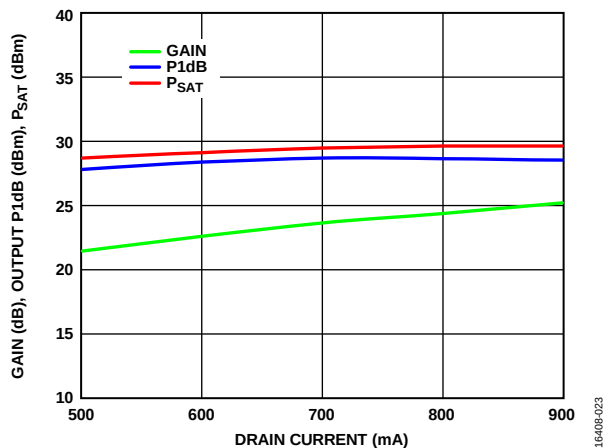
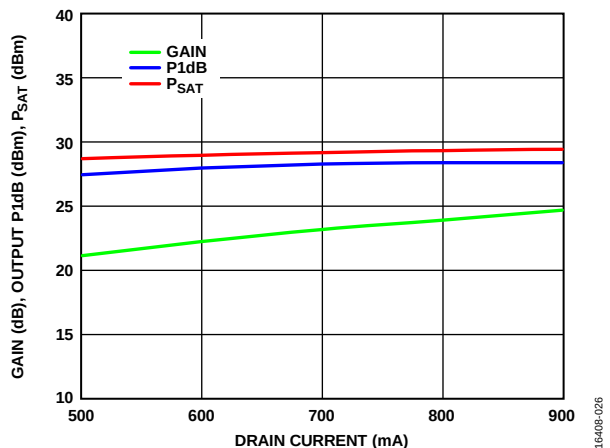


Figure 20. Output IP3 vs. Frequency over I_{DD} , P_{OUT} per Tone = 14 dBm

Figure 21. Output IP3 vs. Frequency over P_{OUT} per Tone, $I_{DD} = 800$ mAFigure 24. Output IP3 vs. P_{OUT} per Tone over I_{DD} , RF = 71 GHzFigure 22. Output IP3 vs. P_{OUT} per Tone over I_{DD} , RF = 73.5 GHzFigure 25. Output IP3 vs. P_{OUT} per Tone over I_{DD} , RF = 76 GHzFigure 23. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}), RF = 71 GHzFigure 26. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}), RF = 73.5 GHz

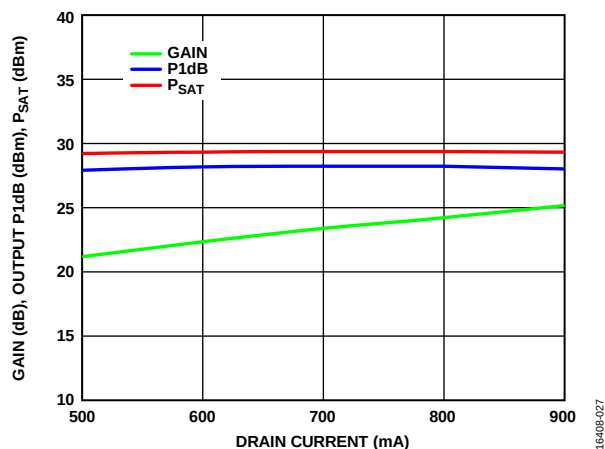


Figure 27. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}), RF = 76 GHz

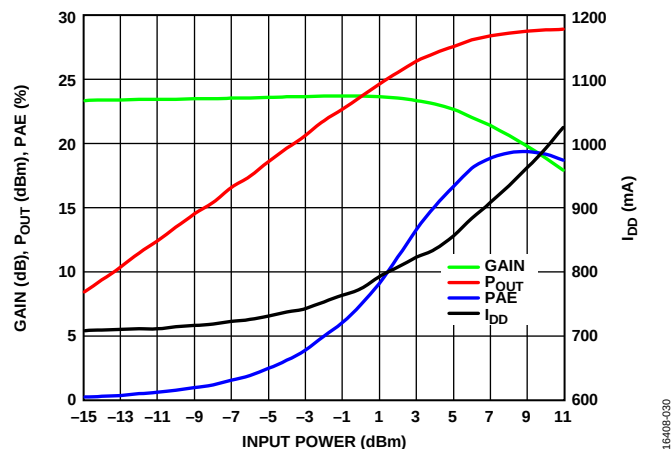


Figure 30. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 76 GHz, I_{DD} = 700 mA

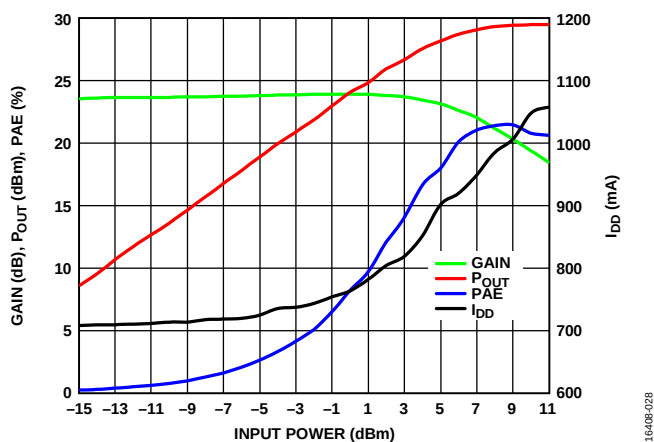


Figure 28. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 71 GHz, I_{DD} = 700 mA

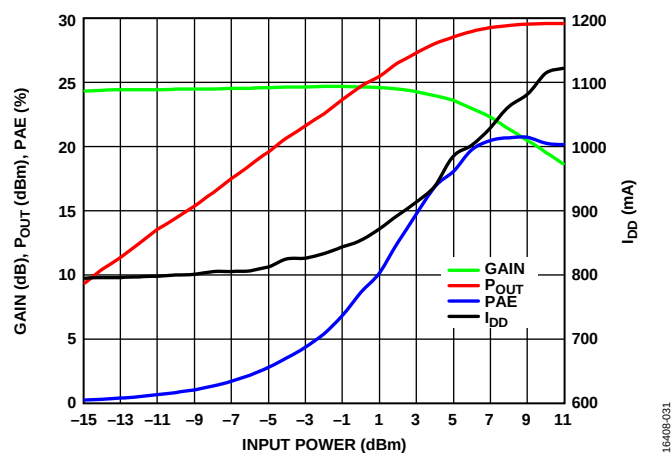


Figure 31. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 71 GHz, I_{DD} = 800 mA

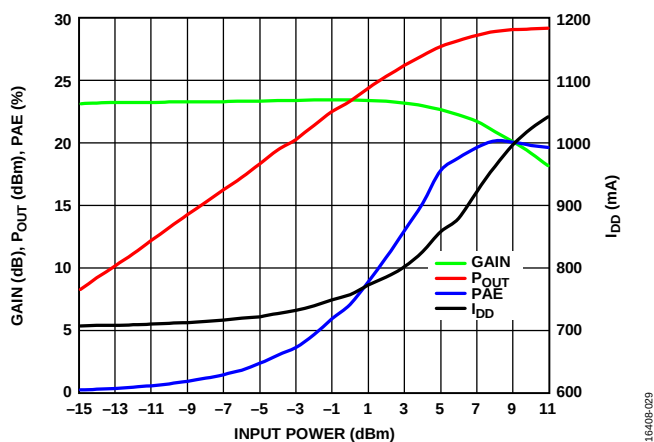


Figure 29. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 73.5 GHz, I_{DD} = 700 mA

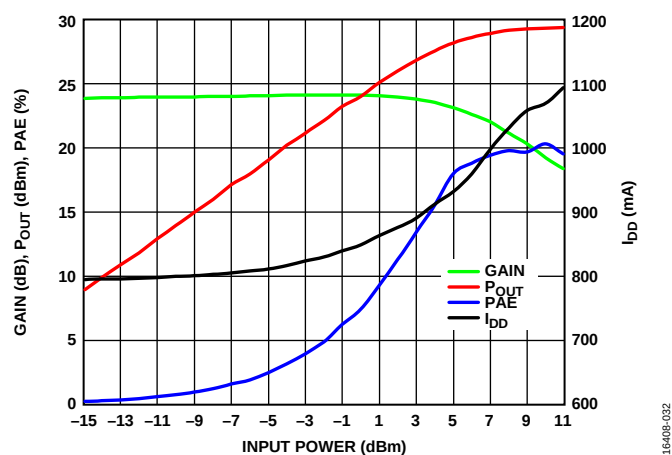


Figure 32. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 73.5 GHz, I_{DD} = 800 mA

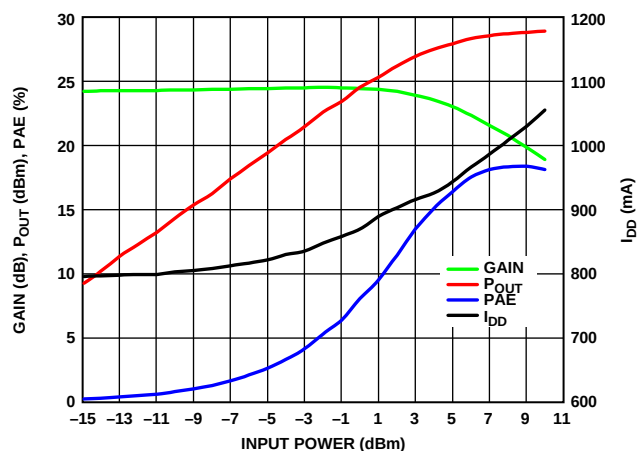


Figure 33. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 76 GHz, $I_{DD} = 800$ mA

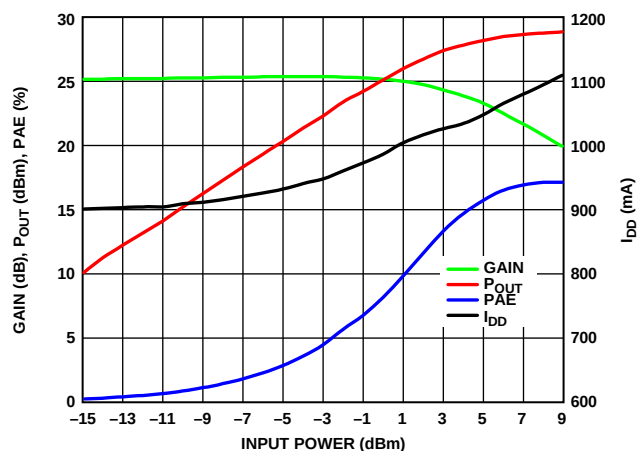


Figure 36. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 76 GHz, $I_{DD} = 900$ mA

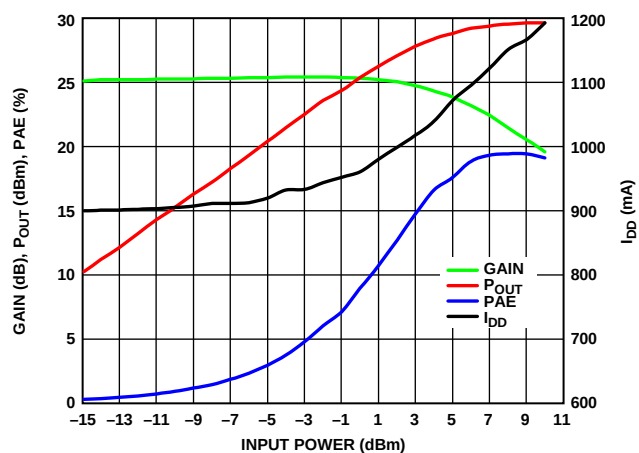


Figure 34. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 71 GHz, $I_{DD} = 900$ mA

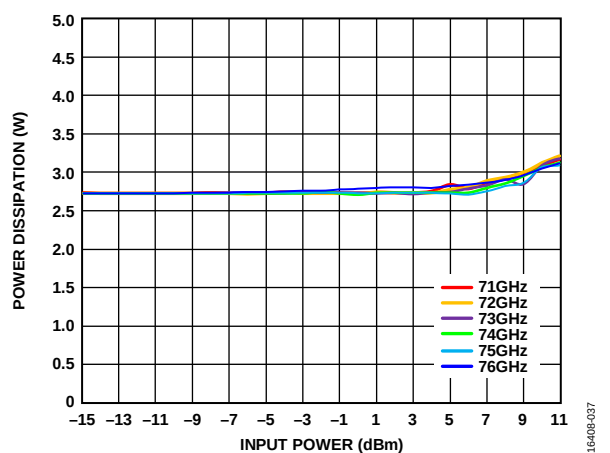


Figure 37. Power Dissipation vs. Input Power over Various Frequencies, $I_{DD} = 700$ mA, $T_A = 85^\circ\text{C}$

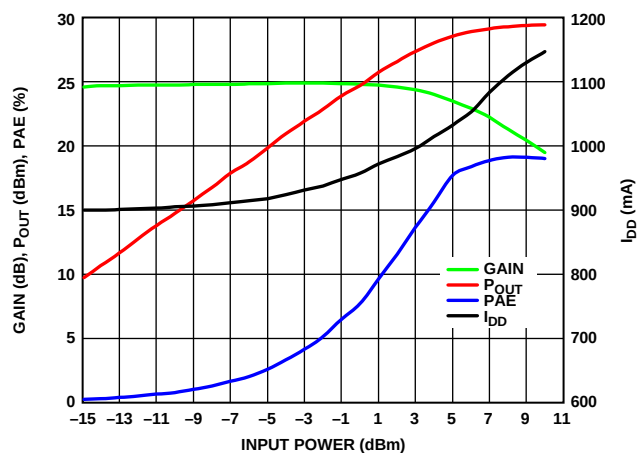


Figure 35. Gain, P_{OUT} , PAE, and I_{DD} vs. Input Power, RF = 73.5 GHz, $I_{DD} = 900$ mA

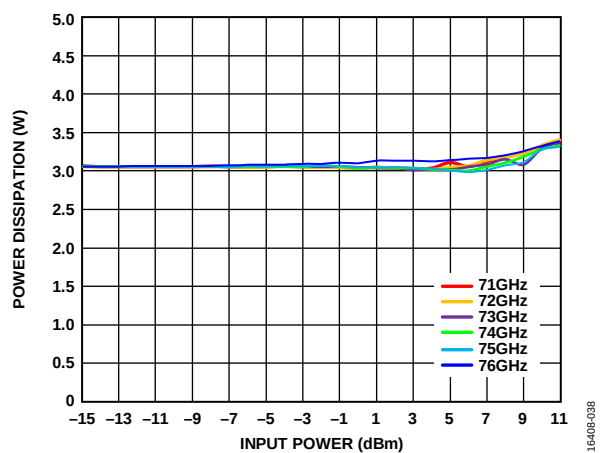


Figure 38. Power Dissipation vs. Input Power over Various Frequencies, $I_{DD} = 800$ mA, $T_A = 85^\circ\text{C}$

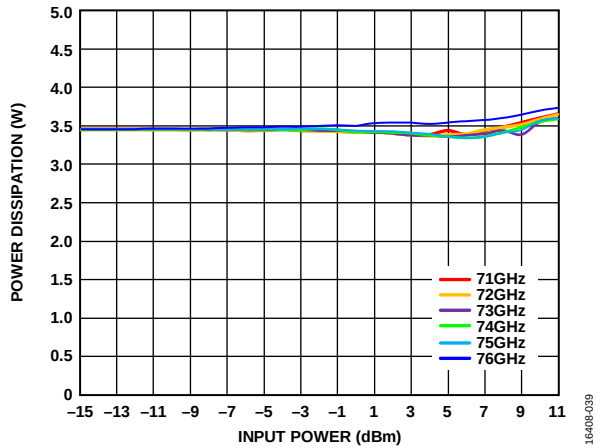


Figure 39. Power Dissipation vs. Input Power over Various Frequencies, $I_{DD} = 900 \text{ mA}$, $T_A = 85^\circ\text{C}$

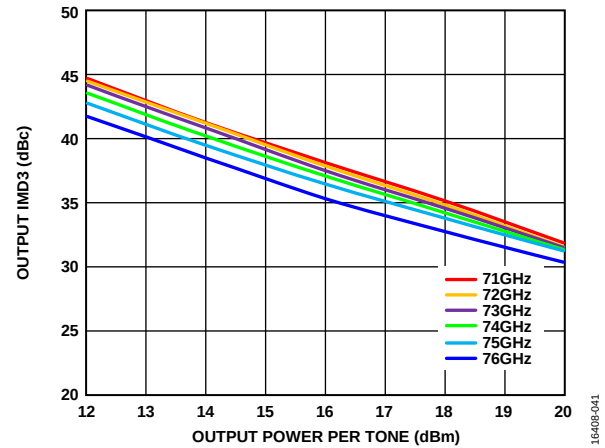


Figure 41. Upper Output Third-Order Intermodulation Distortion (IMD3) vs. Output Power (P_{OUT}) per Tone over Various Frequencies, $I_{DD} = 800 \text{ mA}$

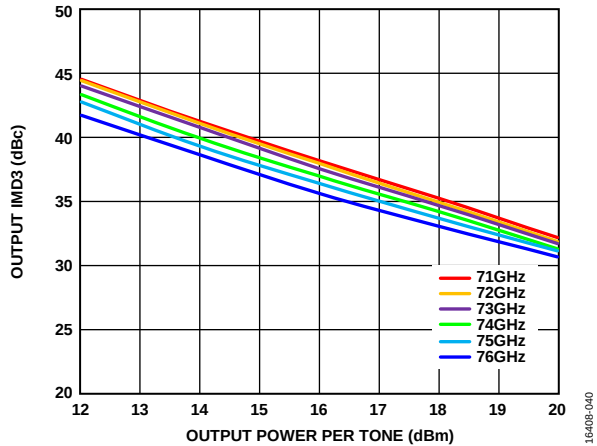


Figure 40. Lower Output Third-Order Intermodulation Distortion (IMD3) vs. Output Power (P_{OUT}) per Tone over Various Frequencies, $I_{DD} = 800 \text{ mA}$

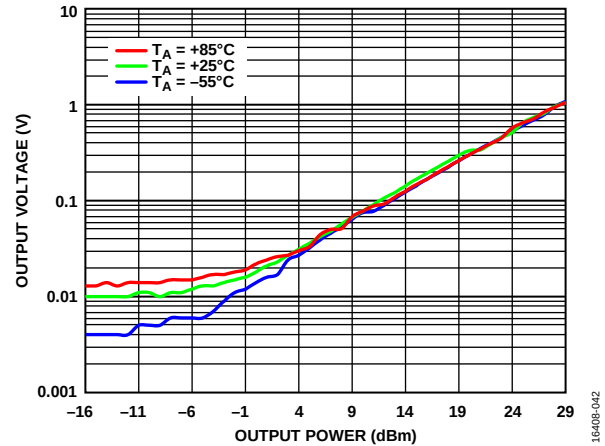


Figure 42. Detector Output Voltage (V_{OUT}) vs. Output Power over Various Temperatures, $I_{DD} = 800 \text{ mA}$, $R_F = 71 \text{ GHz}$

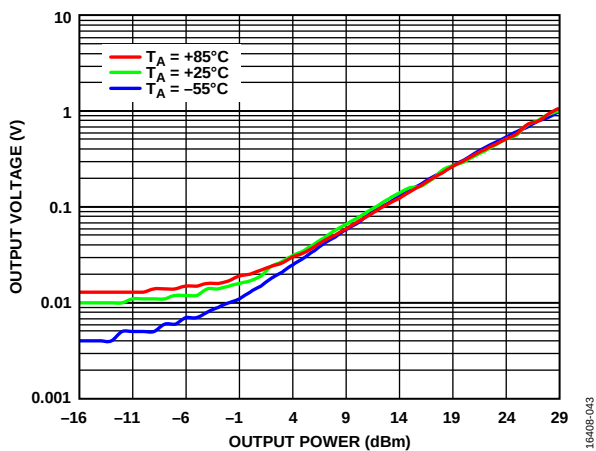


Figure 43. Detector Output Voltage (V_{OUT}) vs. Output Power over Various Temperatures, $I_{DD} = 800$ mA, $RF = 73.5$ GHz

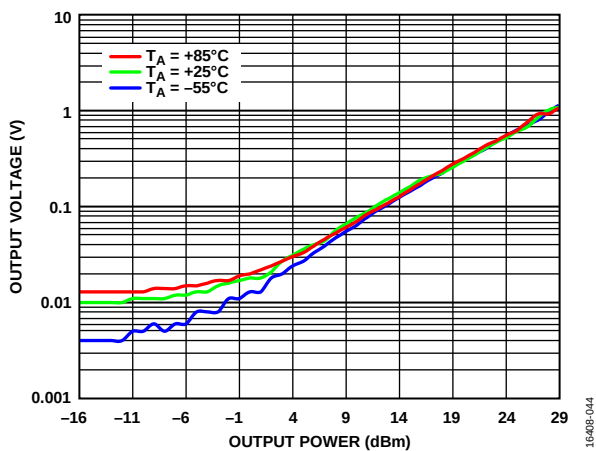


Figure 44. Detector Output Voltage (V_{OUT}) vs. Output Power over Various Temperatures, $I_{DD} = 800$ mA, $RF = 76$ GHz

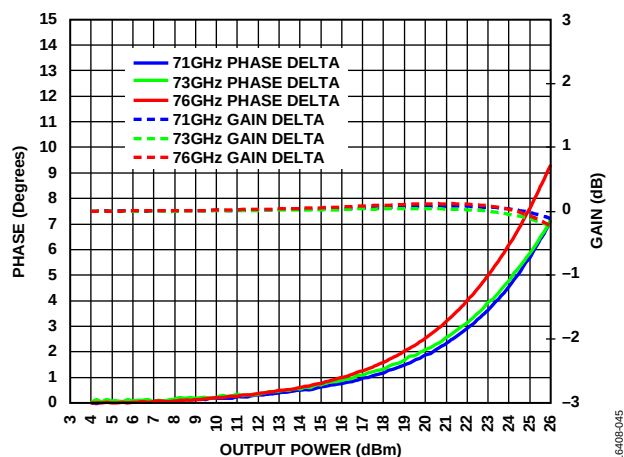


Figure 45. AM to PM Conversion vs. Output Power at Various Frequencies, $T_A = 25^\circ\text{C}$

THEORY OF OPERATION

The circuit architecture of the ADMV7710 power amplifier is shown in Figure 46. The ADMV7710 uses four cascaded gain stages to form an amplifier with a combined gain of 24 dB and a saturated output power (P_{SAT}) of 29 dBm. At the output of the last stage, a coupler taps off a small portion of the output signal.

The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode is included to correct detector temperature dependencies. See the application circuit shown in Figure 47 for further details on biasing the different blocks and using the detector features.

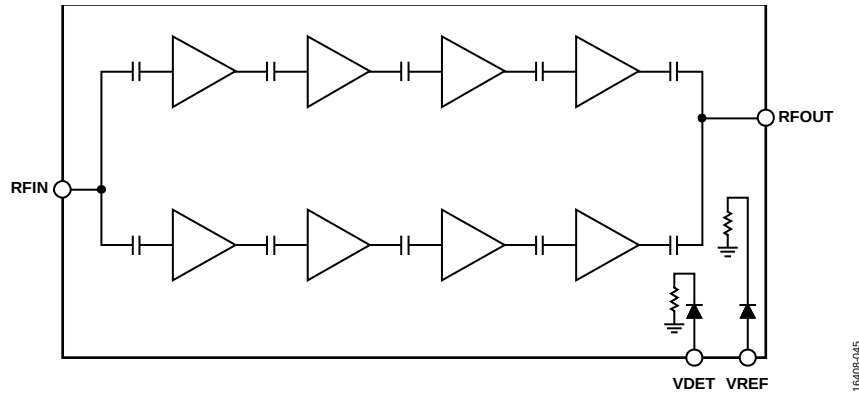


Figure 46. Power Amplifier Circuit Architecture

16408-Q45

APPLICATIONS INFORMATION

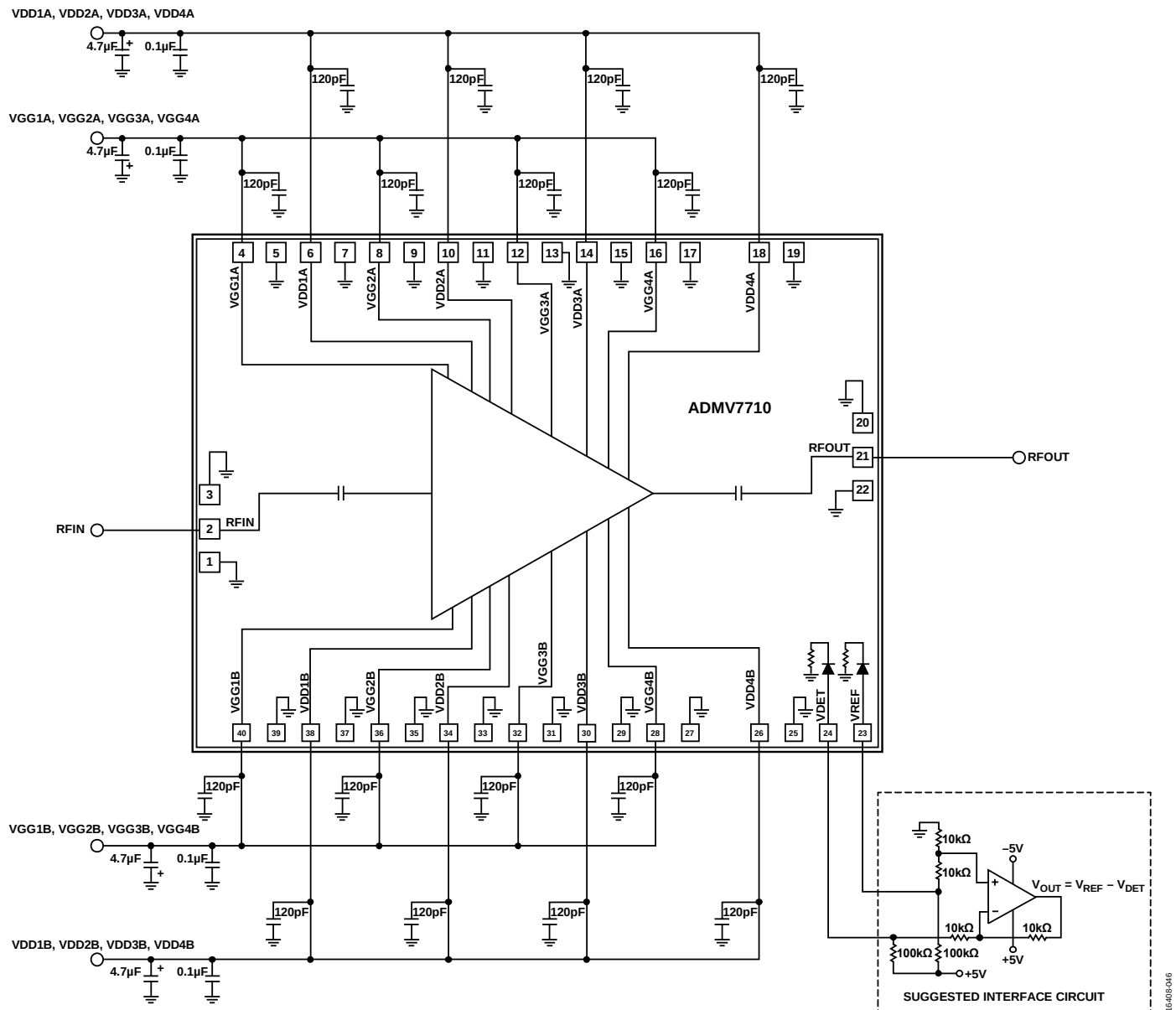
A typical application circuit for the ADMV7710 is shown in Figure 47. Combine the supply lines as shown in the application circuit schematic to minimize the external component count and to simplify power supply routing.

The ADMV7710 uses several amplifier, detector, and attenuator stages. All stages use depletion mode pHEMT transistors. It is important to use the following power-up bias sequence to avoid transistor damage:

1. Apply a -2 V bias to the VGG1A to VGG4A and VGG1B to VGG4B pads.

2. Apply 4 V to the VDD1A to VDD1B and VDD1B to VDD4B pads.
3. Adjust VGG1A to VGG4A and VGG1B to VGG4B between -2 V and 0 V to achieve a total amplifier drain current of 800 mA .

To power down the ADMV7710, follow the reverse procedure. For additional guidance on general bias sequencing, see the [MMIC Amplifier Biasing Procedure](#) application note.



ASSEMBLY DIAGRAM

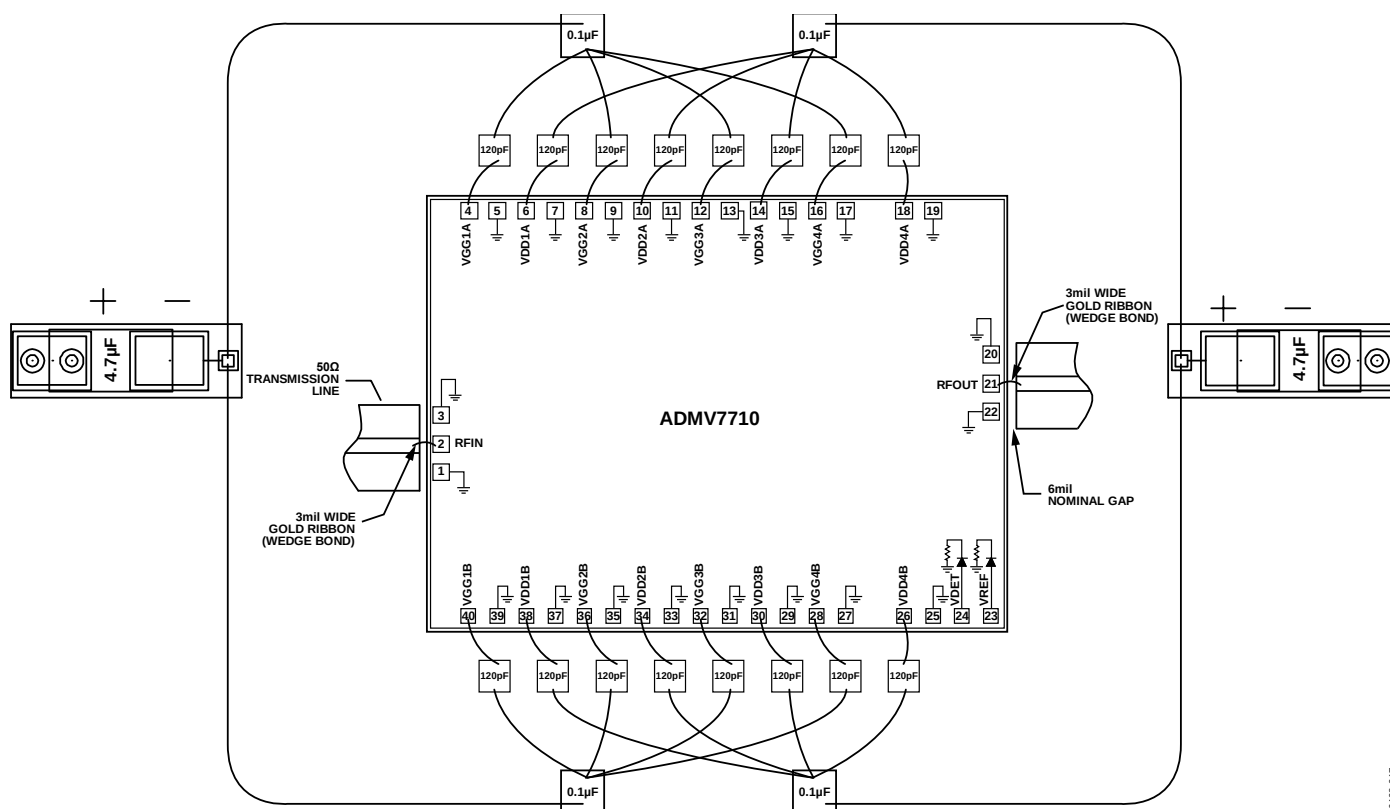


Figure 48. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 49).

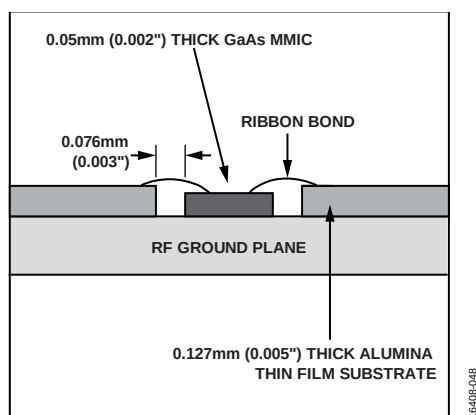


Figure 49. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the following precautions.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% Au/20% Sn preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

ATROX 800HT1V is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 3 mil $\times$ 0.5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

OUTLINE DIMENSIONS

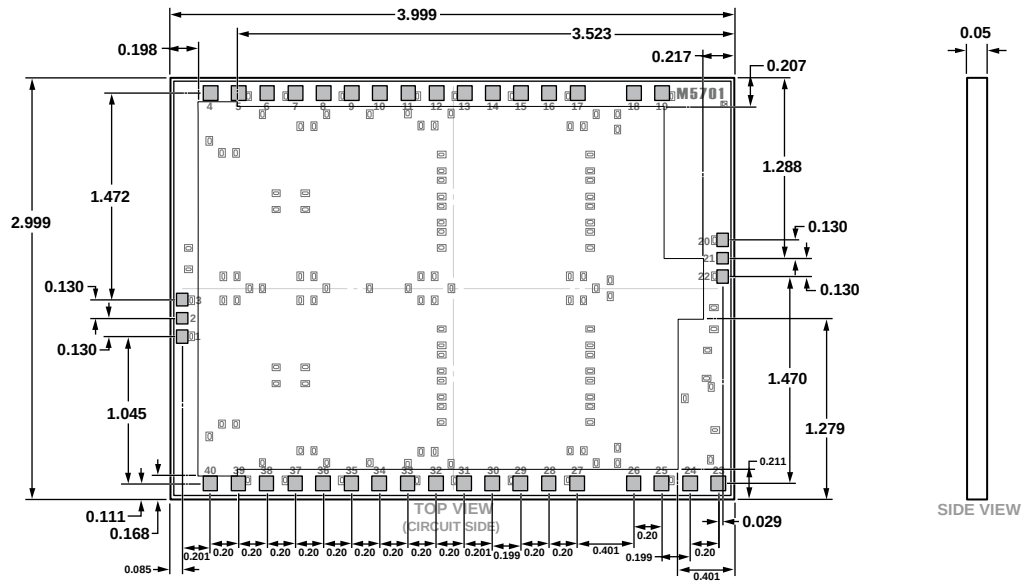


Figure 50. 40-Pad Bare Die [CHIP]
(C-40-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1, 2}	Temperature Range	Package Description	Package Option
ADMV7710CHIPS	–55°C to +85°C	40-Pad Bare Die [CHIP]	C-40-2
ADMV7710-SX	–55°C to +85°C	40-Pad Bare Die [CHIP]	C-40-2

¹ The ADMV7710-SX consists of two pairs of the die in a gel pack for sample orders.

² This is a gel pack option; contact Analog Devices, Inc., sales representatives for additional packaging options.

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