Commercial Space Product

3.3 V, 20 Mbps RS485/RS422 Transceiver

FEATURES

- 3.3 V supply voltage
- 20 Mbps maximum data rate
- No damage or latch-up up to ±15 kV HBM
- Guaranteed fail-safe receiver operation over the entire common-mode range
- Current-limited drivers and thermal shutdown
- Power-up and power-down glitch free driver outputs
- Low operating current: 370 µA typical in receive mode
- Compatible with TIA/EIA-485-A specifications
- Available in 14-lead SOIC_N package

COMMERCIAL SPACE FEATURES

- Supports aerospace applications
- Wafer diffusion lot traceability
- Radiation lot acceptance testing: TID
- Radiation benchmark
  - Total Ionizing Dose (TID)
  - Single Event Effects (SEE)

APPLICATIONS

- Low Earth orbit (LEO) space payloads
- Low power RS485/RS422 transceiver
- Level translator
- Backplane transceiver

FUNCTIONAL BLOCK DIAGRAM

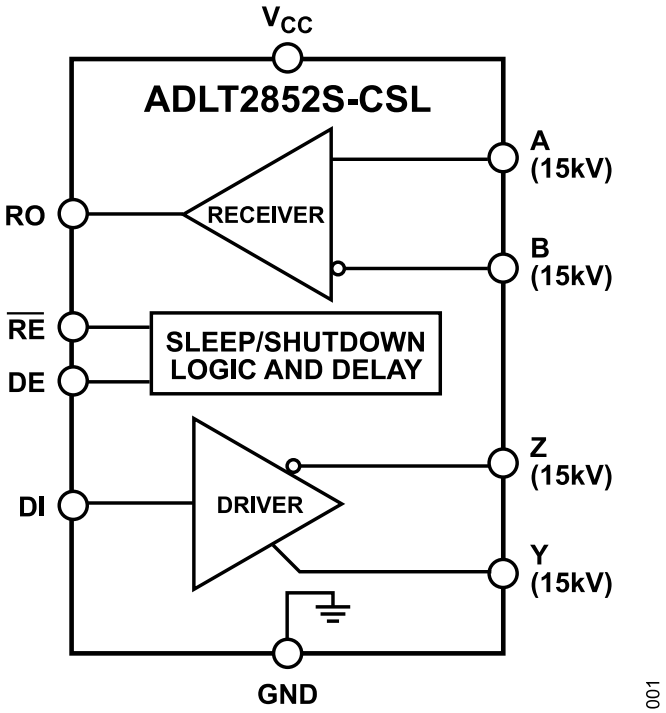

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADLT2852S-CSL is a low power, 20 Mbps RS485/RS422 transceiver operating on a 3.3 V supply. The receiver has a fail-safe feature that guarantees a high output state under conditions of floating or shorted inputs.

The driver maintains a high output impedance over the entire common-mode range when disabled or when the supply is removed. Excessive power dissipation caused by bus contention or a fault is prevented by current limiting all outputs and by thermal shutdown.

Enhanced electrostatic discharge (ESD) protection allows this device to withstand up to ±15 kV human body model (HBM) on the transceiver interface pins without latch-up or damage.

The ADLT2852S-CSL is specified over the −55°C to +125°C temperature range. Additional application and technical information can be found in the Commercial Space Products Program brochure and the LTC2852 data sheet.

TABLE OF CONTENTS

REVISION HISTORY

12/2024—Rev. 0 to Rev. A

Changes to Commercial Space Features Section ... 1
Added Radiation Features Section and Table 7; Renumbered Sequentially ... 6

5/2022—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3 V. All currents into the device pins are positive, and all currents out of the device pins are negative. All voltages are referenced to device ground, unless otherwise specified. Specifications represent performance at −55°C ≤ T_A ≤ +125°C, unless otherwise specified.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DRIVER						
Differential Driver Output Voltage	$\|V_{OD}\|$	Resistance (R) = ∞, V_{CC} = 3 V (see Figure 12)			V_{CC}	V
		R = 27 Ω, V_{CC} = 3 V (see Figure 12)	1.5		V_{CC}	V
		R = 50 Ω, V_{CC} = 3.13 V (see Figure 12)	2		V_{CC}	V
Difference in Magnitude of Driver Differential Output Voltage for Complementary Output States	$\Delta\|V_{OD}\|$	R = 27 Ω or 50 Ω (see Figure 12)			0.2	V
Common Mode Output Voltage	V_{OC}	R = 27 Ω or 50 Ω (see Figure 12)			3	V
Difference in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	$\Delta\|V_{OC}\|$	R = 27 Ω or 50 Ω (see Figure 12)			0.2	V
Three-State (High Impedance) Output Current on Y and Z	I_{OZD}	DE = 0 V, (Y or Z) = –7 V, 12 V			±50	µA
Maximum Driver Short-Circuit Current	I_{OSD}	–7 V ≤ (Y or Z) ≤ +12 V (see Figure 13), applicable only at T_A = 25°C		±180	±250	mA
			–250		+300	mA
RECEIVER						
Input Current (A, B)	I_{IN}	DE = TE = 0 V, V_{CC} = 0 V or 3.3 V, input voltage (V_{IN}) = 12 V (see Figure 14)			250	µA
		DE = TE = 0 V, V_{CC} = 0 V or 3.3 V, V_{IN} = –7 V, (see Figure 14)	–145			µA
Input Resistance	R_{IN}	$\overline{RE}$ = V_{CC} or 0 V, DE = TE = 0 V, V_{IN} = –7 V, –3 V, 3 V, 7 V, 12 V (see Figure 14)	48	125		kΩ
Differential Input Threshold Voltage	V_{TH}	–7 V ≤ B ≤ +12 V			±0.2	V
Input Hysteresis	ΔV_{TH}	B = 0 V, applicable only at T_A = 25°C		25		mV
Output High Voltage	V_{OH}	Receive output current (I(RO)) = –4 mA, A and B = 200 mV, V_{CC} = 3 V	2.4			V
Output Low Voltage	V_{OL}	I(RO) = 4 mA, A and B = –200 mV, V_{CC} = 3 V			0.4	V
Three-State (High Impedance) Output Current on RO	I_{OZR}	$\overline{RE}$ = V_{CC}, 0 V ≤ RO ≤ V_{CC}			±1	µA
Short-Circuit Current	I_{OSR}	0 V ≤ RO ≤ V_{CC}			±85	mA
LOGIC						
Input High Voltage	V_{IH}	V_{CC} = 3.6 V	2			V
Input Low Voltage	V_{IL}	V_{CC} = 3 V			0.8	V
Input Current	I_{INL}			0	±10	µA
SUPPLIES						
Current in Shutdown Mode	I_{CCS}	DE = 0 V, $\overline{RE}$ = V_{CC}		0	15	µA
Current in Receive Mode	I_{CCR}	DE = 0 V, $\overline{RE}$ = 0 V		370	900	µA
Current in Transmit Mode	I_{CCT}	No load, DE = V_{CC}, $\overline{RE}$ = V_{CC}		450	1000	µA
Current with Both Driver and Receiver Enabled	I_{CCTR}	No load, DE = V_{CC}, $\overline{RE}$ = 0 V		450	1000	µA

SPECIFICATIONS

SWITCHING CHARACTERISTICS

V_{CC} = 3.3 V. All currents into the device pins are positive, and all currents out of the device pins are negative. All voltages are referenced to device ground, unless otherwise specified. Specifications represent performance at −55°C ≤ T_A ≤ +125°C, unless otherwise specified.

Table 2. Switching Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DRIVER						
Maximum Data Rate[1]	f_{MAX}		20			Mbps
Input to Output	t_{PLHD}, t_{PHLD}	Differential resistance (R_{DIFF}) = 54 Ω, load capacitance (C_L) = 100 pF (see Figure 15)		10	50	ns
Input to Output Difference, $\lvert t_{PLHD} - t_{PHLD} \rvert$	Δt_{PD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)		1	6	ns
Output Y to Output Z	t_{SKEWD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)		1	±6	ns
Rise or Fall Time	t_{RD}, t_{FD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)		4	12.5	ns
Enable or Disable Time	t_{ZLD}, t_{ZHD}, t_{LZD}, t_{HZD}	Load resistance (R_L) = 500 Ω, C_L = 50 pF, $\overline{RE}$ = 0 V (see Figure 16)			70	ns
Enable from Shutdown	t_{ZHSD}, t_{ZLSD}	R_L = 500 Ω, C_L = 50 pF, $\overline{RE}$ = V_{CC} (see Figure 16)			8	µs
Time to Shutdown	t_{SHDN}	R_L = 500 Ω, C_L = 50 pF, (DE is low, $\overline{RE}$ = V_{CC}) or (DE = 0 V, $\overline{RE}$ is high) (see Figure 16)			100	ns
RECEIVER						
Input to Output	t_{PLHR}, t_{PHLR}	C_L = 15 pF, common-mode voltage (V_{CM}) = 1.5 V, absolute value of A and B voltage ($\lvert V_{AB} \rvert$) = 1.5 V, rise time (t_R) and fall time (t_F) < 4 ns (see Figure 17)		50	70	ns
Differential Receiver Skew, $\lvert t_{PLHR} - t_{PHLR} \rvert$	t_{SKEWR}	C_L = 15 pF (see Figure 17)		1	6	ns
Output Rise or Fall Time	t_{RR}, t_{FR}	C_L = 15 pF (see Figure 17)		3	12.5	ns
Enable and Disable	t_{ZLR}, t_{ZHR}, t_{LZR}, t_{HZR}	R_L = 1 kΩ, C_L = 15 pF, DE = V_{CC} (see Figure 18)			50	ns
Enable from Shutdown	t_{ZHSR}, t_{ZLSR}	R_L = 1 kΩ, C_L = 15 pF, DE = 0 V (see Figure 18)			8	µs

[1] The maximum data rate is guaranteed by other measured parameters and is not tested directly.

RADIATION TEST AND LIMIT SPECIFICATIONS

Total ionizing dose (TID) testing characterized to 30 krads (20 krads + 50% overstress) with biased annealing at 100°C for 168 hours.

Table 3. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DRIVER						
Difference in Magnitude of Driver Differential Output Voltage for Complementary Output States	$\Delta\lvert V_{OD} \rvert$	R = 27 Ω or 50 Ω (see Figure 12)			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 27 Ω or 50 Ω (see Figure 12)			3	V
Difference in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	$\Delta\lvert V_{OC} \rvert$	R = 27 Ω or 50 Ω (see Figure 12)			0.2	V
Three-State (High Impedance) Output Current on Y and Z	I_{OZD}	DE = 0 V, (Y or Z) = –7 V, 12 V	–10		+200	µA
Maximum Driver Short-Circuit Current	I_{OSD}	–7 V ≤ (Y or Z) ≤ +12 V (see Figure 13)	–260		+300	mA
RECEIVER						
Input Current (A, B)	I_{IN}					
		DE = TE = 0 V, V_{CC} = 0 V or 3.3 V, V_{IN} = 12 V (see Figure 14)			135	µA
		DE = TE = 0 V, V_{CC} = 0 V or 3.3 V, V_{IN} = –7 V, (see Figure 14)	–105			µA
Input Resistance	R_{IN}	$\overline{RE}$ = V_{CC} or 0 V, DE = TE = 0 V, V_{IN} = –7 V, –3 V, 3 V, 7 V, 12 V (see Figure 14)	94			kΩ
Differential Input Threshold Voltage	V_{TH}	–7 V ≤ B ≤ +12 V	–220		+220	mV

SPECIFICATIONS

Table 3. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Hysteresis	ΔV_{TH}	B = 0 V	20		40	mV
Output High Voltage	V_{OH}	I(RO) = –4 mA, A and B = 200 mV, V_{CC} = 3 V	2.4			V
Output Low Voltage	V_{OL}	I(RO) = 4 mA, A and B = –200 mV, V_{CC} = 3 V			0.4	V
Three-State (High Impedance) Output Current on RO	I_{OZR}	$\overline{RE}$ = V_{CC}, 0 V ≤ RO ≤ V_{CC}	–1		+1	µA
Short-Circuit Current	I_{OSR}	0 V ≤ RO ≤ V_{CC}	–85		+85	mA
LOGIC						
Input High Voltage	V_{IH}	V_{CC} = 3.6 V	2			V
Input Low Voltage	V_{IL}	V_{CC} = 3 V			0.8	V
Input Current	I_{INL}		–10		+10	µA
SUPPLIES						
Current in Shutdown Mode	I_{CCS}	DE = 0 V, $\overline{RE}$ = V_{CC}			65	µA
Current in Receive Mode	I_{CCR}	DE = 0 V, $\overline{RE}$ = 0 V			850	µA
Current in Transmit Mode	I_{CCT}	No load, DE = V_{CC}, $\overline{RE}$ = V_{CC}			1100	µA
Current with Both Driver and Receiver Enabled	I_{CCTR}	No load, DE = V_{CC}, $\overline{RE}$ = 0 V			1200	µA

Table 4. Switching Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DRIVER						
Input to Output	t_{PLHD}, t_{PHLD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)			55	ns
Input to Output Difference, $\lvert t_{PLHD} - t_{PHLD} \rvert$	Δt_{PD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)			9	ns
Output Y to Output Z	t_{SKEWD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)			6	ns
Rise or Fall Time	t_{RD}, t_{FD}	R_{DIFF} = 54 Ω, C_L = 100 pF (see Figure 15)			13	ns
Enable or Disable Time	t_{ZLD}, t_{ZHD}, t_{LZD}, t_{HZD}	R_L = 500 Ω, C_L = 50 pF, $\overline{RE}$ = 0 V (see Figure 16)			50	ns
Enable from Shutdown	t_{ZHSD}, t_{ZLSD}	R_L = 500 Ω, C_L = 50 pF, $\overline{RE}$ = V_{CC} (see Figure 16)			6	µs
Time to Shutdown	t_{SHDN}	R_L = 500 Ω, C_L = 50 pF, (DE is low, $\overline{RE}$ = V_{CC}) or (DE = 0 V, $\overline{RE}$ is high) (see Figure 16)			100	ns
RECEIVER						
Receiver Input to Output	t_{PLHR}, t_{PHLR}	C_L = 15 pF, V_{CM} = 1.5 V, $\lvert V_{AB} \rvert$ = 1.5 V, t_R and t_F < 4 ns (see Figure 17)			80	ns
Differential Receiver Skew, $\lvert t_{PLHR} - t_{PHLR} \rvert$	t_{SKEWR}	C_L = 15 pF (see Figure 17)			9	ns
Output Rise or Fall Time	t_{RR}, t_{FR}	C_L = 15 pF (see Figure 17)			9.5	ns
Enable and Disable	t_{ZLR}, t_{ZHR}, t_{LZR}, t_{HZR}	R_L = 1 kΩ, C_L = 15 pF, DE = V_{CC} (see Figure 18)			50	ns
Enable from Shutdown	t_{ZHSR}, t_{ZLSR}	R_L = 1 kΩ, C_L = 15 pF, DE = 0 V (see Figure 18)			6	µs

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{CC})	–0.3 V to +7 V
Logic Input Voltages ($\overline{RE}$, DE, and DI)	–0.3 V to +7 V
Interface Input and Output	
A, B, Y, and Z	(V_{CC} – 15 V) to +15 V
RO Voltage	–0.3 V to (V_{CC} + 0.3 V)
Operating Temperature Range[1]	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C

[1] This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection activates at a junction temperature exceeding 150°C. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

θ_{JA} is the natural convection junction to ambient thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	θ_{JA}	Unit
05-08-1610	37	88	°C/W

RADIATION FEATURES

Table 7. Radiation Features

Specification	Value	Unit
Maximum Total Dose Available (Dose Rate = 50 rad(Si)/sec to 300 rad(Si)/sec)[1]	20	Krad (Si)
No Single Event Latch-Up (SEL) Occurs at Effective Linear Energy Transfer (LET)[2]	57.5	MeV-cm^2/mg

[1] Guaranteed by device and process characterization. Email space@analog.com for data available up to 30 Krad (Si)

[2] Limits are characterized at the initial qualification and after any design or process changes that may affect the SEL characteristics but are not production lot tested, unless specified by the customer through the purchase order or contract. For more information on SEE test results, email space@analog.com for further data beyond the published report on ADLT2852S product page.

OUTGAS TESTING

The criteria used for the acceptance and rejection of materials must be determined by the user and based upon specific component and system requirements. Historically, a total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% have been used as screening levels for rejection of spacecraft materials.

Table 8. Outgas Testing

Specification (Tested per ASTM E595-15)	Value	Unit
TML	0.07	%
CVCM	<0.01	%
Water Vapor Recovered	0.03	%

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADLT2852S-CSL

Table 9. ADLT2852S-CSL, 14-Lead SOIC_N

ESD Model	Withstand Threshold (V)	Class
HBM	±15,000	3B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

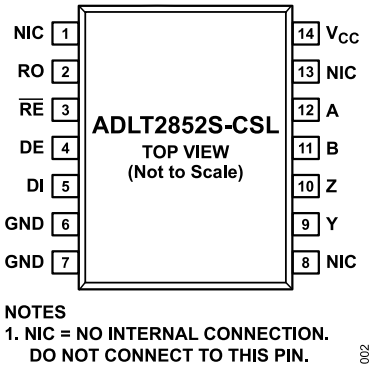

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 13	NIC	Not internal connection. Do not connect to this pin.
2	RO	Receiver Output. If the receiver output is enabled ($\overline{RE}$ low) and A > B by 200 mV, RO is high. If A < B by 200 mV, RO is low. If the receiver inputs are open, shorted, or terminated without a valid signal, RO is high.
3	$\overline{RE}$	Receiver Enable. A low input enables the receiver. A high input forces the receiver output into a high impedance state.
4	DE	Driver Enable. A high input on DE enables the driver. A low input forces the driver outputs into a high impedance state. If $\overline{RE}$ is high with DE low, the device enters a low power shutdown state.
5	DI	Driver Input. If the driver outputs are enabled (DE high), a low input on DI forces the driver positive output low and negative output high. A high input on DI, with the driver outputs enabled, forces the driver positive output high and negative output low.
6, 7	GND	Ground.
9	Y	Noninverting Driver Output. High impedance when the driver is disabled or unpowered.
10	Z	Inverting Driver Output. High impedance when the driver is disabled or unpowered.
11	B	Inverting Receiver Input. Impedance is >96 kΩ when in receive mode or unpowered.
12	A	Noninverting Receiver Input. Impedance is >96 kΩ when in receive mode or unpowered.
14	V_{CC}	Positive Supply. 3 V ≤ V_{CC} ≤ 3.6 V. Bypass with 0.1 µF ceramic capacitor.

TRUTH TABLE

Table 11. Truth Table

Logic Inputs					
DE	$\overline{RE}$	Mode	A, B	Y, Z	RO
0	0	Receive	R_{IN}	Hi-Z	Driven
0	1	Shutdown	R_{IN}	Hi-Z	Hi-Z
1	0	Transceive	R_{IN}	Driven	Driven
1	1	Transmit	R_{IN}	Driven	Hi-Z

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = 3.3 V, unless otherwise noted.

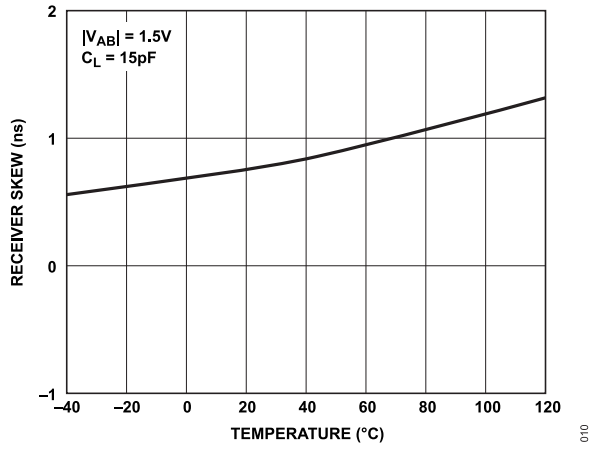

Figure 3. Receiver Skew vs. Temperature

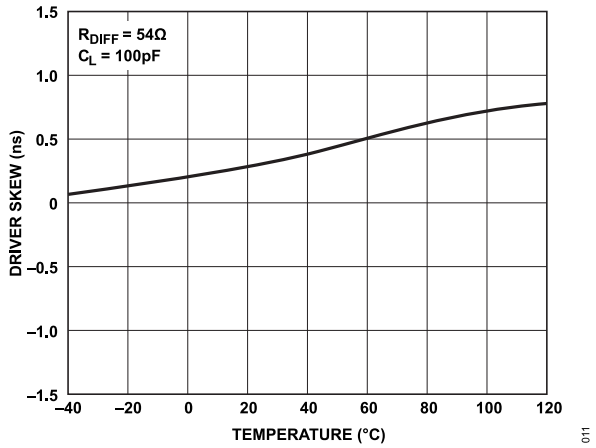

Figure 4. Driver Skew vs. Temperature

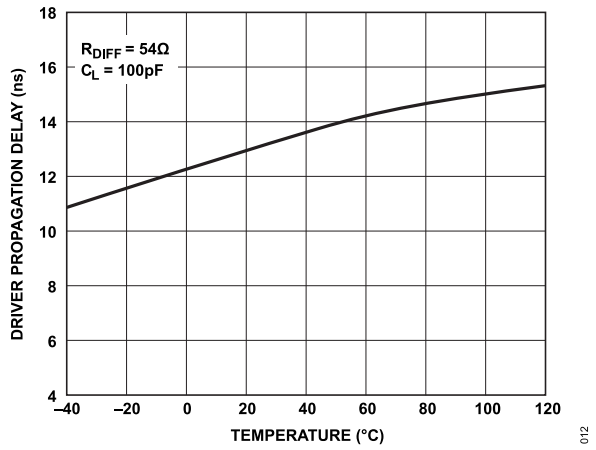

Figure 5. Driver Propagation Delay vs. Temperature

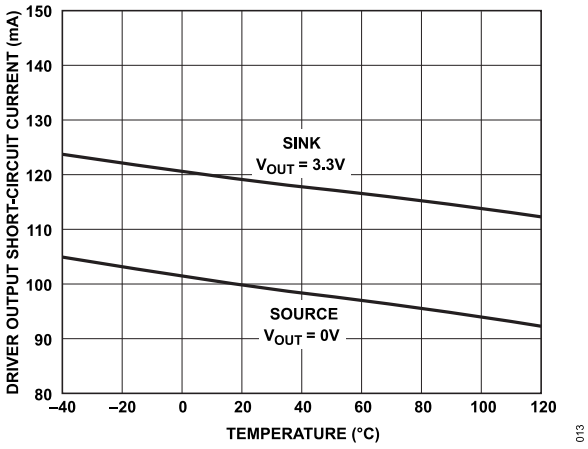

Figure 6. Driver Output Short-Circuit Current vs. Temperature (V_{OUT} Is Output Voltage)

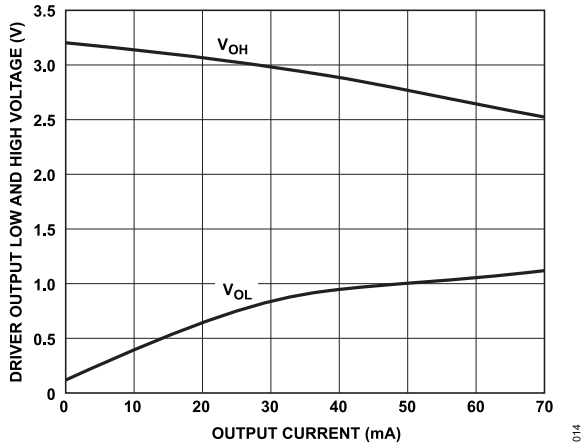

Figure 7. Driver Output Low and High Voltage vs. Output Current

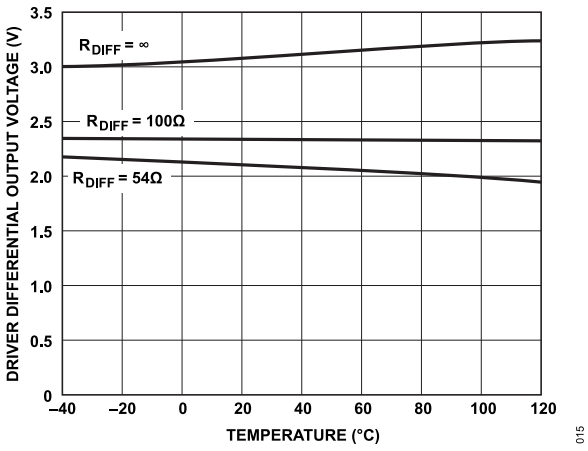

Figure 8. Driver Differential Output Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

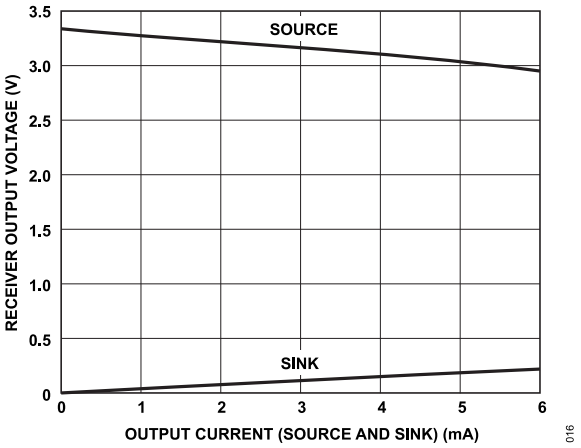

Figure 9. Receiver Output Voltage vs. Output Current (Source and Sink)

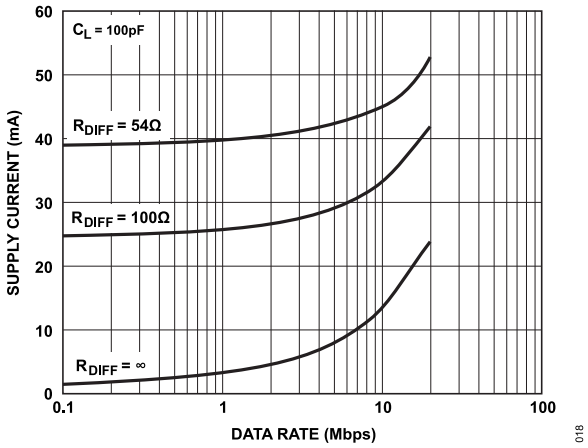

Figure 11. Supply Current vs. Data Rate

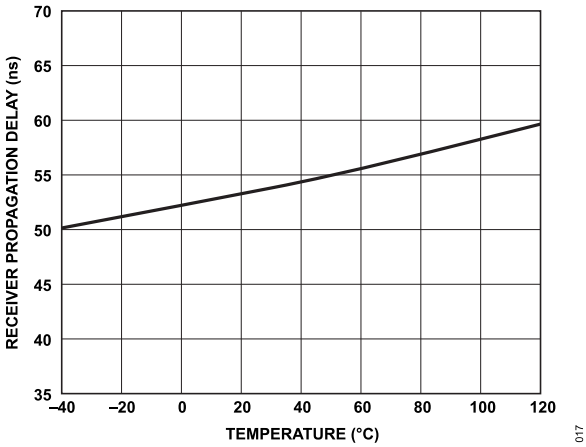

Figure 10. Receiver Propagation Delay vs. Temperature

TEST CIRCUITS

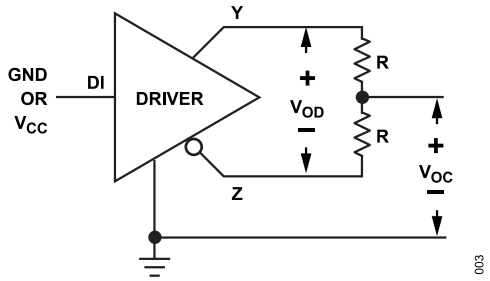

Figure 12. Driver DC Characteristics

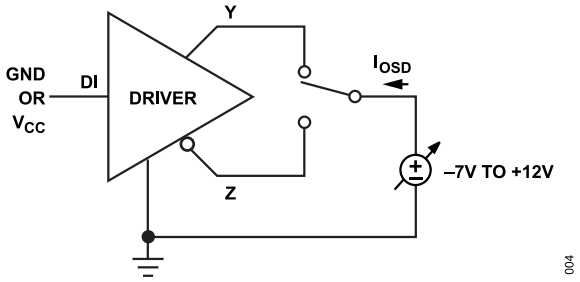

Figure 13. Driver Output Short-Circuit Current

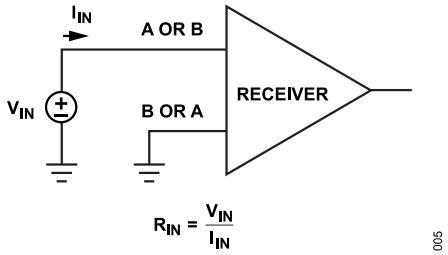

Figure 14. Receiver Input Current and Input Resistance

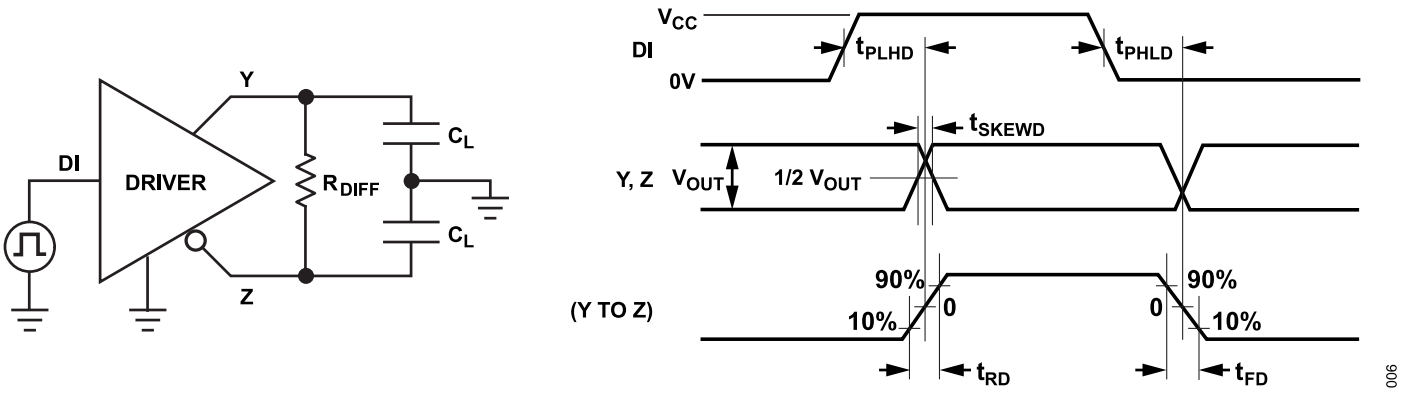

Figure 15. Driver Timing Measurement

TEST CIRCUITS

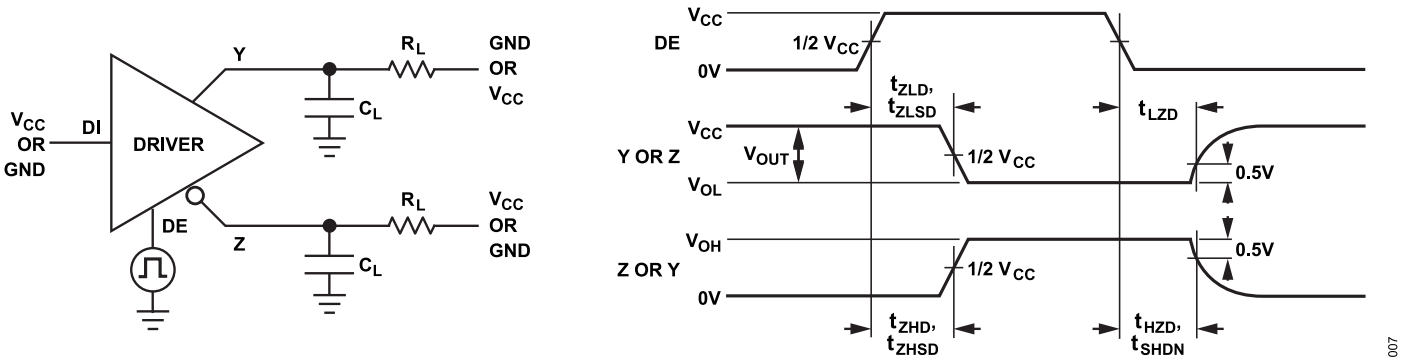

Figure 16. Driver Enable and Disable Timing Measurements

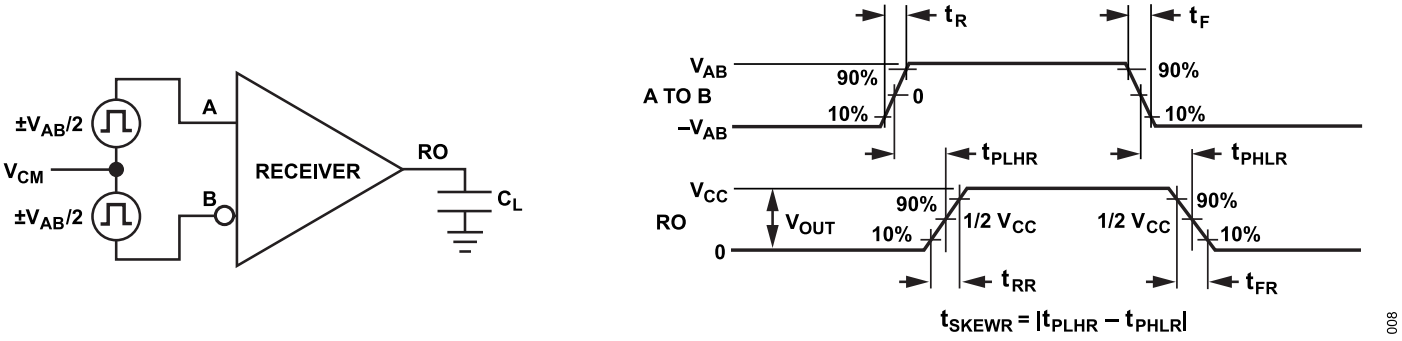

Figure 17. Receiver Propagation Delay Measurements

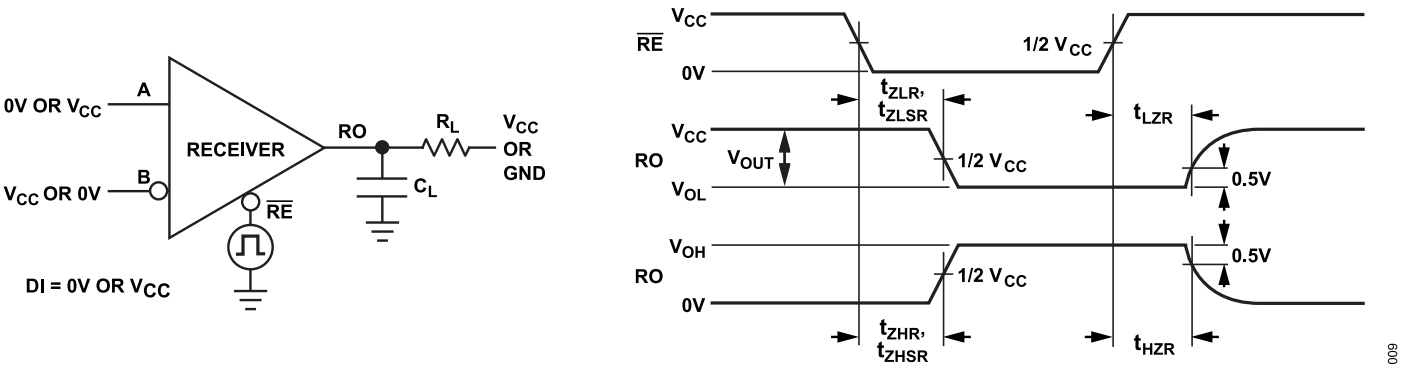

Figure 18. Receiver Enable and Disable Timing Measurements

OUTLINE DIMENSIONS

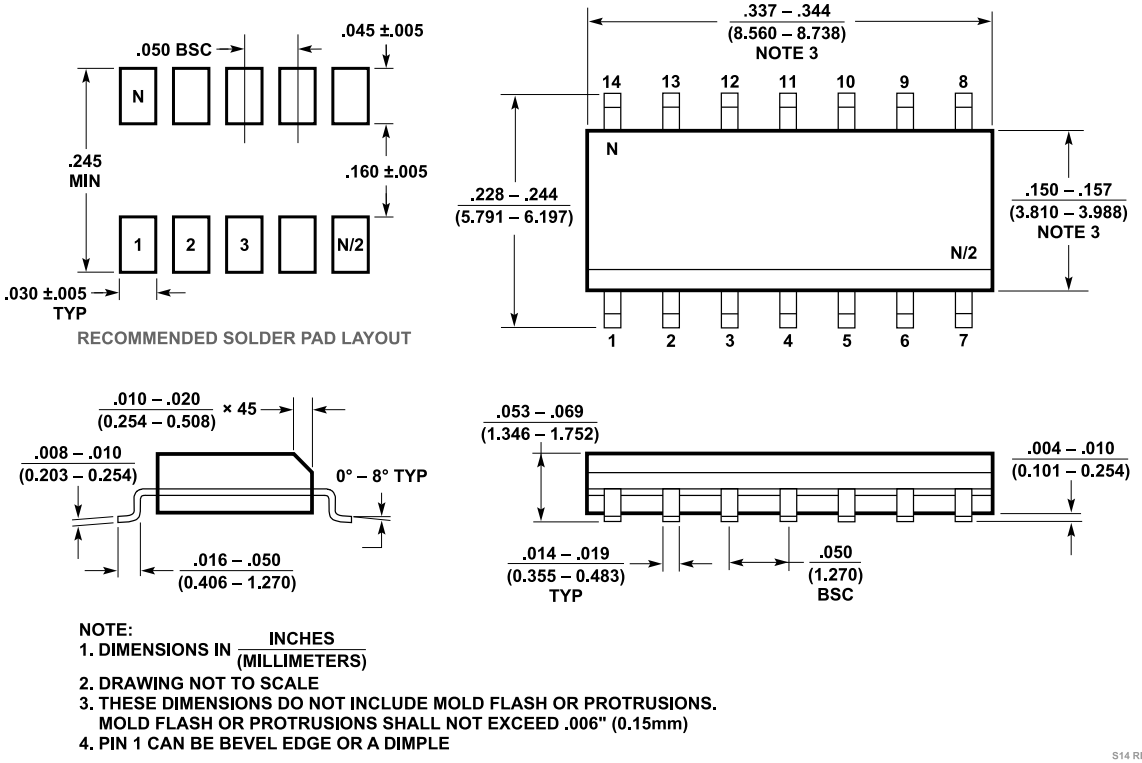

Figure 19. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(05-08-1610)
Dimensions shown in inches and (millimeters)

Updated: May 06, 2022

ORDERING GUIDE

Model	Temperature Range	Package Description	Packing Quantity	Package Option
ADLT2852MPS-CSL	−55°C to +125°C	14-Lead SOIC_N, 150 Mil	Tube, 55	05-08-1610

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