

## FEATURES

- 3 dB bandwidth: 10.0 GHz
- Preset 10 dB gain, can be reduced by adding external resistors
- Differential or single-ended input to differential output
- Internally dc-coupled inputs and outputs
- Input voltage noise (NSD, RTI): 2.25 nV/ $\sqrt{\text{Hz}}$  at 100 MHz
- Low noise input stage: 11.3 dB noise figure at 1 GHz
- Low distortion with +5.0 V and –1.8 V supplies and 1.4 V p-p output differential with a 50  $\Omega$  || 1 pF load differential
- 2 GHz: –59.4 dBc (HD2), –54.3 dBc (HD3), –68.2 dBc (IMD3)
- 6 GHz: –66 dBc (HD2), –88.1 dBc (HD3), –48.3 dBc (IMD3)
- 276 mA positive supply current at 5.0 V typical
- 224 mA negative supply current at –1.8 V typical
- Power disable

## APPLICATIONS

Instrumentation and defense applications

## GENERAL DESCRIPTION

The ADL5580 is a high performance, single-ended or differential amplifier with 10 dB of voltage gain, optimized for applications spanning from dc to 10.0 GHz. The amplifier offers a low referred to input (RTI) noise spectral density (NSD) of 2.24 nV/ $\sqrt{\text{Hz}}$  (at 1000 MHz) and is optimized for distortion performance over a wide frequency range, making the device an ideal driver for high speed 12-bit to 16-bit analog-to-digital converters (ADCs). The ADL5580 is suited for use in high performance, zero intermediate frequency (IF), and complex IF receiver designs. In addition, this device has low distortion for single-ended input driver applications.

By using two external series resistors, the gain selection from 10 dB for a differential input can be modified to a lower gain. The device maintains low distortion through its output common-mode voltage ( $V_{\text{CM}}$ ) of 0.5 V, providing a flexible capability for driving ADCs with full-scale levels up to 1.4 V p-p.

## FUNCTIONAL BLOCK DIAGRAM

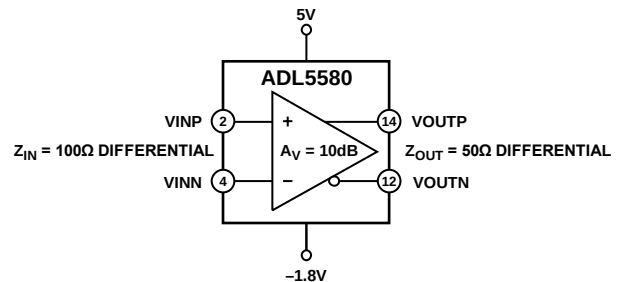


Figure 1.

17004-001

Operating from a +5 V and –1.8 V supply, the positive and negative supply current of the ADL5580 is typically +276 mA and –224 mA, respectively. The device has a power disable feature, and when disabled, the amplifier consumes 2 mA.

The ADL5580 is optimized for wideband, low distortion, and low noise operation at the dc to 10.0 GHz frequency range. These attributes, together with its adjustable gain capability, make this device an optimal choice for driving a wide variety of ADCs, mixers, pin diode attenuators, surface acoustic wave (SAW) filters, and a multiplicity of discrete RF devices.

Fabricated on an Analog Devices, Inc., high speed silicon germanium (SiGe) process, the ADL5580 is supplied in a compact 4 mm × 4 mm, 20-terminal land grid array (LGA) package and operates over the –40°C to +85°C temperature range.

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## REVISION HISTORY

12/2020—Revision 0: Initial Version

## SPECIFICATIONS

Positive supply voltage ( $V_S$ ) = +5.0 V, negative  $V_S$  = -1.8 V, input  $V_{CM}$  = 1.7 V, output  $V_{CM}$  = 0.5 V, source impedance ( $R_S$ ) = 100  $\Omega$  differential, load impedance ( $R_L$ ) = 50  $\Omega$  differential, output voltage ( $V_{OUT}$ ) = 1.4 V p-p composite, peak capacitance ( $C_{PEAK}$ ) = 3,  $T_A$  = 25°C, and signal spacing = 2 MHz for two-tone measurements, unless otherwise noted.

Table 1.

| Parameter                                             | Test Conditions/Comments                          | Min | Typ   | Max | Unit                         |
|-------------------------------------------------------|---------------------------------------------------|-----|-------|-----|------------------------------|
| <b>DYNAMIC PERFORMANCE</b>                            |                                                   |     |       |     |                              |
| -3 dB Bandwidth <sup>1</sup>                          | $V_{OUT} \leq 1.4$ V p-p                          |     | 10.0  |     | GHz                          |
| Bandwidth, 1.0 dB Flatness                            | $V_{OUT} \leq 1.4$ V p-p                          |     | 6     |     | GHz                          |
| Voltage Gain ( $A_V$ )                                |                                                   |     |       |     |                              |
| Differential Input                                    | $R_L = 50 \Omega    1$ pF differential            |     | 10    |     | dB                           |
| Single-Ended Input                                    | $R_L = 50 \Omega    1$ pF differential            |     | 10    |     | dB                           |
| Gain Supply Sensitivity                               | Positive $V_S \pm 5\%$ and negative $V_S \pm 5\%$ |     | 128   |     | mdB/V                        |
| Gain Temperature Sensitivity                          | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$  |     | 10.7  |     | mdB/ $^\circ\text{C}$        |
| Slew Rate                                             | Rising, $V_{OUT} = 1.4$ V p-p step                |     | 24    |     | V/ns                         |
|                                                       | Falling, $V_{OUT} = 1.4$ V p-p step               |     | 24    |     | V/ns                         |
| Settling Time                                         | 1.4 V step to 1%                                  |     | 2.4   |     | ns                           |
| Overdrive Settling Time                               | Differential output voltage 2.8 V p-p             |     | 640   |     | ps                           |
| EN Response Time                                      | From shutdown mode                                |     | 20    |     | ns                           |
|                                                       | To shutdown mode                                  |     | 6     |     | ns                           |
| Reverse Isolation (SDD12)                             | Frequency = 1000 MHz                              |     | -70   |     | dB                           |
| Input to Output Isolation when Disabled               | Frequency = 1000 MHz, EN pin set to low           |     | -87   |     | dBc                          |
| <b>INPUT AND OUTPUT CHARACTERISTICS</b>               |                                                   |     |       |     |                              |
| Input $V_{CM}$                                        | V <sub>CM1</sub>                                  |     | 1.7   |     | V                            |
| Input Resistance                                      |                                                   |     |       |     |                              |
| Differential                                          |                                                   |     | 100   |     | $\Omega$                     |
| Single-Ended                                          |                                                   |     | 100   |     | $\Omega$                     |
| Common-Mode Rejection Ratio (CMRR)                    | Frequency = 1000 MHz                              |     | 32.9  |     | dB                           |
| Output $V_{CM}$                                       | V <sub>CMO</sub>                                  |     | 0.5   |     | V                            |
| Output Resistance (Differential)                      |                                                   |     | 50    |     | $\Omega$                     |
| V <sub>CM1</sub> and V <sub>CMO</sub> Input Impedance |                                                   |     | 10    |     | k $\Omega$                   |
| Input Common-Mode                                     |                                                   |     |       |     |                              |
| Offset                                                |                                                   |     | 97.7  |     | mV                           |
| Drift                                                 | $T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$    |     | 0.188 |     | mV/ $^\circ\text{C}$         |
| Input Differential Offset                             |                                                   |     |       |     |                              |
| Voltage                                               |                                                   |     | 0.4   |     | mV                           |
| Drift                                                 | $T_A = -40^\circ\text{C}$ to $+25^\circ\text{C}$  |     | 3.076 |     | $\mu\text{V}/^\circ\text{C}$ |
| Output Common-Mode                                    |                                                   |     |       |     |                              |
| Offset                                                |                                                   |     | 6.6   |     | mV                           |
| Drift                                                 | $T_A = -40^\circ\text{C}$ to $+25^\circ\text{C}$  |     | 0.119 |     | mV/ $^\circ\text{C}$         |
| Output Differential Offset                            |                                                   |     |       |     |                              |
| Voltage                                               |                                                   |     | 0.4   |     | mV                           |
| Drift                                                 | $T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$    |     | 6.666 |     | $\mu\text{V}/^\circ\text{C}$ |
| Maximum Output Voltage Swing                          | Frequency = 1000 MHz, 1 dB compression point      |     | 5     |     | V p-p                        |

| Parameter                                      | Test Conditions/Comments | Min | Typ   | Max | Unit   |
|------------------------------------------------|--------------------------|-----|-------|-----|--------|
| NOISE AND HARMONIC PERFORMANCE                 |                          |     |       |     |        |
| Input Signal Frequency, 100 MHz                |                          |     |       |     |        |
| Second Harmonic Distortion (HD2)               |                          |     | -77.2 |     | dBc    |
| Third Harmonic Distortion (HD3)                |                          |     | -74.2 |     | dBc    |
| Output Third-Order Intercept (OIP3)            |                          |     | 43.6  |     | dBm    |
| Third-Order Intermodulation Distortion (IMD3)  |                          |     | -84.7 |     | dBc    |
| Output Second-Order Intercept (OIP2)           |                          |     | 77.7  |     | dBm    |
| Second-Order Intermodulation Distortion (IMD2) |                          |     | -76.4 |     | dBc    |
| Output 1 dB Compression Point (OP1dB)          |                          |     | 17.5  |     | dBm    |
| Noise Figure                                   |                          |     | 11.3  |     | dB     |
| NSD, RTI <sup>2</sup>                          |                          |     | 2.25  |     | nV/√Hz |
| Input Signal Frequency, 500 MHz                |                          |     |       |     |        |
| HD2                                            |                          |     | -66.4 |     | dBc    |
| HD3                                            |                          |     | -66.1 |     | dBc    |
| OIP3                                           |                          |     | 40.3  |     | dBm    |
| IMD3                                           |                          |     | -78.2 |     | dBc    |
| OIP2                                           |                          |     | 66.8  |     | dBm    |
| IMD2                                           |                          |     | -65.6 |     | dBc    |
| OP1dB                                          |                          |     | 17.5  |     | dBm    |
| Noise Figure                                   |                          |     | 11.2  |     | dB     |
| NSD, RTI <sup>2</sup>                          |                          |     | 2.23  |     | nV/√Hz |
| Input Signal Frequency, 1000 MHz               |                          |     |       |     |        |
| HD2                                            |                          |     | -66.3 |     | dBc    |
| HD3                                            |                          |     | -61.1 |     | dBc    |
| OIP3                                           |                          |     | 38.1  |     | dBm    |
| IMD3                                           |                          |     | -73.5 |     | dBc    |
| OIP2                                           |                          |     | 65.9  |     | dBm    |
| IMD2                                           |                          |     | -64.7 |     | dBc    |
| OP1dB                                          |                          |     | 17.5  |     | dBm    |
| Noise Figure                                   |                          |     | 11.3  |     | dB     |
| NSD, RTI <sup>2</sup>                          |                          |     | 2.24  |     | nV/√Hz |
| Input Signal Frequency, 2000 MHz               |                          |     |       |     |        |
| HD2                                            |                          |     | -59.4 |     | dBc    |
| HD3                                            |                          |     | -54.3 |     | dBc    |
| OIP3                                           |                          |     | 35.3  |     | dBm    |
| IMD3                                           |                          |     | -68.2 |     | dBc    |
| OIP2                                           |                          |     | 60.2  |     | dBm    |
| IMD2                                           |                          |     | -59.1 |     | dBc    |
| OP1dB                                          |                          |     | 17.5  |     | dBm    |
| Noise Figure                                   |                          |     | 11.4  |     | dB     |
| NSD, RTI <sup>2</sup>                          |                          |     | 2.26  |     | nV/√Hz |

| Parameter                        | Test Conditions/Comments                    | Min  | Typ   | Max  | Unit   |
|----------------------------------|---------------------------------------------|------|-------|------|--------|
| Input Signal Frequency, 3000 MHz |                                             |      |       |      |        |
| HD2                              |                                             |      | −60.6 |      | dBc    |
| HD3                              |                                             |      | −47.1 |      | dBc    |
| OIP3                             |                                             |      | 32.8  |      | dBm    |
| IMD3                             |                                             |      | −63.2 |      | dBc    |
| OIP2                             |                                             |      | 69.8  |      | dBm    |
| IMD2                             |                                             |      | −68.6 |      | dBc    |
| OP1dB                            |                                             |      | 17.5  |      | dBm    |
| Noise Figure                     |                                             |      | 10.9  |      | dB     |
| NSD, RTI <sup>2</sup>            |                                             |      | 2.13  |      | nV/√Hz |
| Input Signal Frequency, 4000 MHz |                                             |      |       |      |        |
| HD2                              |                                             |      | −58   |      | dBc    |
| HD3                              |                                             |      | −54.8 |      | dBc    |
| OIP3                             |                                             |      | 30.7  |      | dBm    |
| IMD3                             |                                             |      | −53.9 |      | dBc    |
| OIP2                             |                                             |      | 58.6  |      | dBm    |
| IMD2                             |                                             |      | −57.3 |      | dBc    |
| OP1dB                            |                                             |      | 18.0  |      | dBm    |
| Noise Figure                     |                                             |      | 10.3  |      | dB     |
| NSD, RTI <sup>2</sup>            |                                             |      | 1.96  |      | nV/√Hz |
| Input Signal Frequency, 5000 MHz |                                             |      |       |      |        |
| HD2                              |                                             |      | −60   |      | dBc    |
| HD3                              |                                             |      | −72.1 |      | dBc    |
| OIP3                             |                                             |      | 28.1  |      | dBm    |
| IMD3                             |                                             |      | −53.9 |      | dBc    |
| OIP2                             |                                             |      | 60.9  |      | dBm    |
| IMD2                             |                                             |      | −59.7 |      | dBc    |
| OP1dB                            |                                             |      | 17.5  |      | dBm    |
| Noise Figure                     |                                             |      | 10.0  |      | dB     |
| NSD, RTI <sup>2</sup>            |                                             |      | 1.90  |      | nV/√Hz |
| Input Signal Frequency, 6000 MHz |                                             |      |       |      |        |
| HD2                              |                                             |      | −66   |      | dBc    |
| HD3                              |                                             |      | −88.1 |      | dBc    |
| OIP3                             |                                             |      | 25.4  |      | dBm    |
| IMD3                             |                                             |      | −48.3 |      | dBc    |
| OIP2                             |                                             |      | 67.3  |      | dBm    |
| IMD2                             |                                             |      | −66.1 |      | dBc    |
| OP1dB                            |                                             |      | 17.0  |      | dBm    |
| NF                               |                                             |      | 9.5   |      | dB     |
| NSD, RTI <sup>2</sup>            |                                             |      | 1.78  |      | nV/√Hz |
| DIGITAL LOGIC                    |                                             |      |       |      |        |
| Input Voltage                    | SCLK, SDIO, $\overline{\text{CS}}$ , and EN |      |       |      |        |
| High (V <sub>IH</sub> )          |                                             | 1.07 |       |      | V      |
| Low (V <sub>IL</sub> )           |                                             |      |       | 0.68 | V      |
| Input Current                    |                                             |      |       |      |        |
| High (I <sub>IH</sub> )          |                                             |      |       | −100 | μA     |
| Low (I <sub>IL</sub> )           |                                             |      |       | 100  | μA     |

| Parameter                       | Test Conditions/Comments                                              | Min  | Typ  | Max   | Unit |
|---------------------------------|-----------------------------------------------------------------------|------|------|-------|------|
| Output Voltage                  | SDIO                                                                  |      |      |       |      |
| At 1.8 V                        | Register 0x200, Bit 0 = 0x0                                           |      |      |       |      |
| High (V <sub>OH</sub> )         | Output high current (I <sub>OH</sub> ) = –100 µA or –1 mA static load | 1.5  |      |       | V    |
| Low (V <sub>OL</sub> )          | Output low current (I <sub>OL</sub> ) = 100 µA or 1 mA static load    |      |      | 0.2   | V    |
| At 3.3 V                        | Register 0x200, Bit 0 = 0x1                                           |      |      |       |      |
| V <sub>OH</sub>                 | I <sub>OH</sub> = –100 µA or –1 mA static load                        | 2.7  |      |       | V    |
| V <sub>OL</sub>                 | I <sub>OL</sub> = 100 µA or 1 mA static load                          |      |      | 0.2   | V    |
| SUPPLY AND POWER SPECIFICATIONS |                                                                       |      |      |       |      |
| Power                           |                                                                       |      | 1.76 |       | W    |
| Shutdown Power                  | At room temperature                                                   |      | 11   |       | mW   |
| Shutdown Current                | At room temperature                                                   |      | 2    |       | mA   |
| Positive Supply                 |                                                                       |      |      |       |      |
| Voltage (V <sub>PAVCC</sub> )   | 5%                                                                    | 4.75 | 5.0  | 5.25  | V    |
| Current (I <sub>PAVCC</sub> )   |                                                                       |      | 276  |       | mA   |
| Negative Supply                 |                                                                       |      |      |       |      |
| Voltage (V <sub>MAVEE</sub> )   | 5%                                                                    | –1.7 | –1.8 | –1.89 | V    |
| Current (I <sub>MAVEE</sub> )   |                                                                       |      | –224 |       | mA   |

<sup>1</sup> S parameters are taken with the device under test (DUT) itself. The printed circuit board (PCB) is not used in the measurement.

<sup>2</sup> NSD RTI is calculated from noise figure as follows, assuming that R<sub>s</sub> = R<sub>i</sub>:

$$NSD(RTI) = \frac{1}{2} \times \sqrt{4kT \times (10^{NF/10} - 1) \times R_{IN}}$$

where:

*k* is Boltzmann's constant, which equals 1.381 × 10<sup>–23</sup> J/K.

*T* is the standard absolute temperature for evaluating noise figure, which equals 290 K.

*R<sub>IN</sub>* is the differential input impedance of the amplifier, which equals 100 Ω.

## DIGITAL LOGIC TIMING

Table 2.

| Parameter         | Description                                                                                   | Min | Typ | Max | Unit |
|-------------------|-----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| f <sub>SCLK</sub> | Maximum serial clock rate, 1/t <sub>SCLK</sub> (t <sub>SCLK</sub> is the SCLK time)           |     | 25  |     | MHz  |
| t <sub>PWH</sub>  | Minimum period that SCLK is in logic high state                                               |     | 10  |     | ns   |
| t <sub>PWL</sub>  | Minimum period that SCLK is in logic low state                                                |     | 10  |     | ns   |
| t <sub>DS</sub>   | Setup time between data and rising edge of SCLK                                               |     | 5   |     | ns   |
| t <sub>DH</sub>   | Hold time between data and rising edge of SCLK                                                |     | 5   |     | ns   |
| t <sub>DCS</sub>  | Setup time between falling edge of $\overline{CS}$ and rising edge of SCLK                    |     | 10  |     | ns   |
| t <sub>H</sub>    | Hold time between rising edge of $\overline{CS}$ and the last falling edge of SCLK            |     | 10  |     | ns   |
| t <sub>DV</sub>   | Maximum time delay between falling edge of SCLK and output data valid for a read operation    |     | 5   | 14  | ns   |
| t <sub>z</sub>    | Maximum time delay between $\overline{CS}$ deactivation and SDIO bus return to high impedance |     |     | 12  | ns   |

### Timing Diagrams

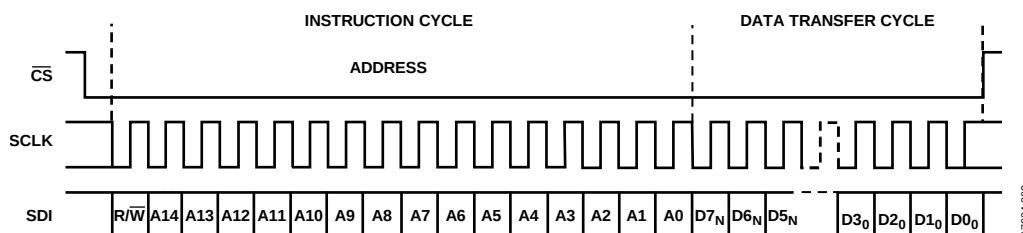


Figure 2. Serial Port Interface Register Timing, MSB First

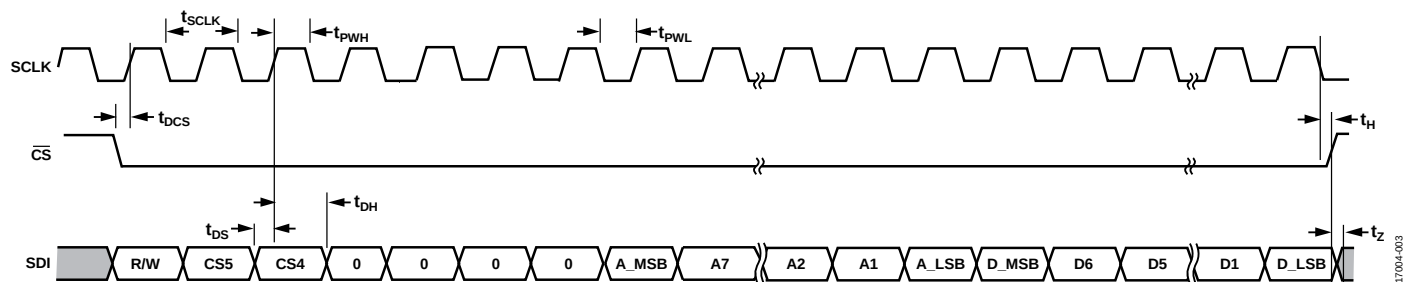


Figure 3. Timing Diagram for the Serial Port Interface Register Write

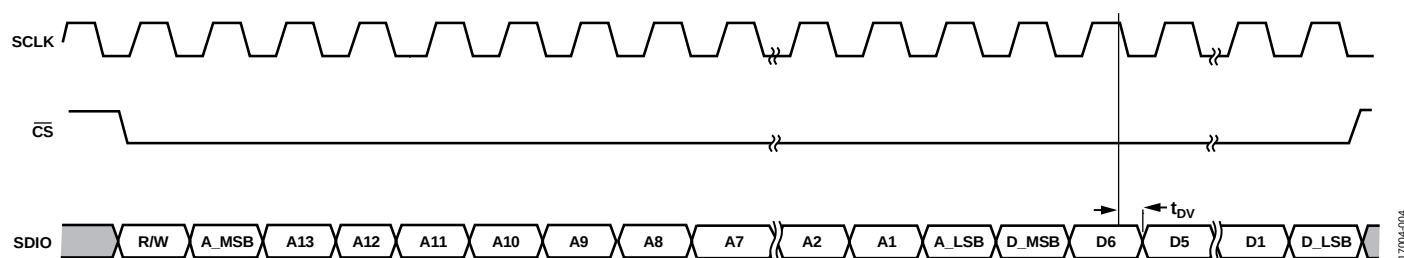


Figure 4. Timing Diagram for Serial Port Interface Register Read

## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter                                      | Rating           |
|------------------------------------------------|------------------|
| Supply Voltage                                 |                  |
| At PAVCC                                       | 5.5 V            |
| At MAVEE                                       | –1.98 V          |
| RF Input Power (VINP and VINN) at 100 $\Omega$ | $\pm 350$ mV     |
| $\overline{\text{CS}}$ , SCLK, SDIO, and EN    | –0.3 V to +3.6 V |
| Temperature                                    |                  |
| Operating Range                                | –40°C to +85°C   |
| Maximum Junction                               | 125°C            |
| Storage                                        | 150°C            |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

| Package Type <sup>1</sup> | $\theta_{JA}$ | $\theta_{JCTOP}$ | $\theta_{JCBOTTOM}$ | $\theta_{JB}$ | $\psi_{JT}$ | $\psi_{JB}$ | Unit |
|---------------------------|---------------|------------------|---------------------|---------------|-------------|-------------|------|
| CC-20-7                   | 53.5          | 24.3             | 20.9                | 24.2          | 6.0         | 25.5        | °C/W |

<sup>1</sup> Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD-51.

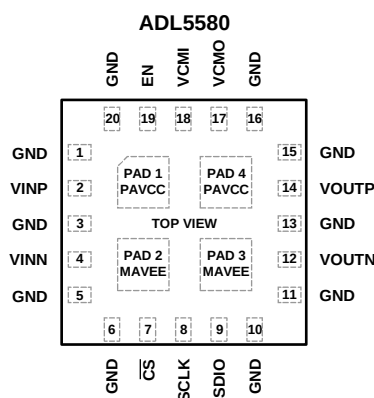
## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



### NOTES

1. PAD 1 AND PAD 4 ARE THE POSITIVE VOLTAGE SUPPLY, 5.0V.
2. PAD 2 AND PAD 3 ARE THE NEGATIVE VOLTAGE SUPPLY, -1.8V.

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Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No                             | Mnemonic        | Description                                                                                                   |
|------------------------------------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 1, 3, 5, 6, 10, 11, 13, 15, 16, 20 | GND             | Ground. Connect the GND pins to ground.                                                                       |
| 2                                  | VINP            | Positive RF Input (RFIN) Signal. VINP is the positive side of the amplifier balanced differential inputs.     |
| 4                                  | VINN            | Negative RFIN Signal. VINN is the negative side of the amplifier balanced differential inputs.                |
| 7                                  | $\overline{CS}$ | Serial Peripheral Interface (SPI) Chip Select. $\overline{CS}$ is a digital input.                            |
| 8                                  | SCLK            | SPI Serial Clock. SCLK is a digital input.                                                                    |
| 9                                  | SDIO            | SPI Serial Data Input and Output. SDIO is a digital input and output.                                         |
| 12                                 | VOUTN           | Negative RF Output (RFOUT) Signal. VOUTN is the negative side of the amplifier balanced differential outputs. |
| 14                                 | VOUTP           | Positive RFOUT Signal. VOUTP is the positive side of the amplifier balanced differential outputs.             |
| 17                                 | VCMO            | $V_{CM}$ for the RF Output Signal.                                                                            |
| 18                                 | VCM             | $V_{CM}$ for the RF Input Signal.                                                                             |
| 19                                 | EN              | Digital Input Power Enable.                                                                                   |
| PAD1, PAD4                         | PAVCC           | Positive Voltage Supply, 5.0 V.                                                                               |
| PAD2, PAD3                         | MAVEE           | Negative Voltage Supply, -1.8 V.                                                                              |

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 5.0$  V, negative  $V_S = -1.8$  V, input  $V_{CM} = 1.7$  V, output  $V_{CM} = 0.5$  V,  $R_S = 100\ \Omega$  differential,  $R_L = 50\ \Omega$  differential  $V_{OUT} = 1.4$  V p-p composite,  $C_{PEAK} = 3$ ,  $T_A = 25^\circ\text{C}$ , and signal spacing = 2 MHz for two-tone measurements, unless otherwise noted.

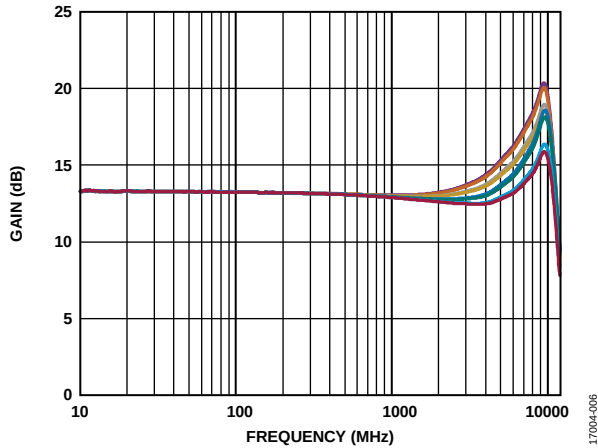


Figure 6. Gain vs. Frequency for  $C_{PEAK} = 0$  Through  $C_{PEAK} = 7$ , Supply = Nominal, Temperature =  $25^\circ\text{C}$

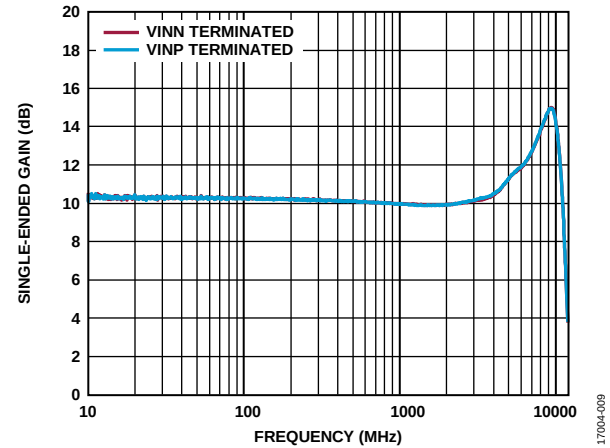


Figure 9. Single-Ended Gain vs. Frequency, Temperature =  $25^\circ\text{C}$ ,  $C_{PEAK} = 3$ , Supply = Nominal

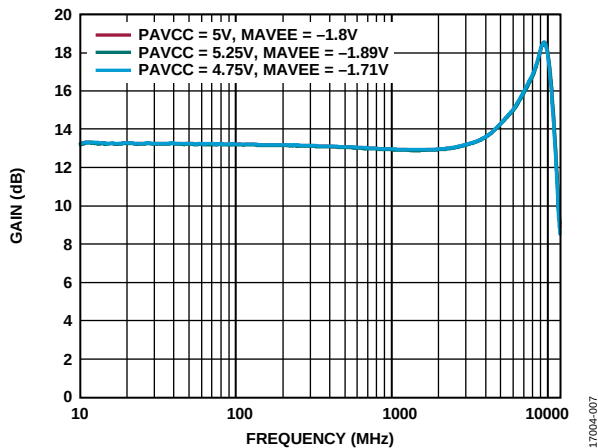


Figure 7. Gain vs. Frequency over Supply,  $C_{PEAK} = 3$ , Temperature =  $25^\circ\text{C}$

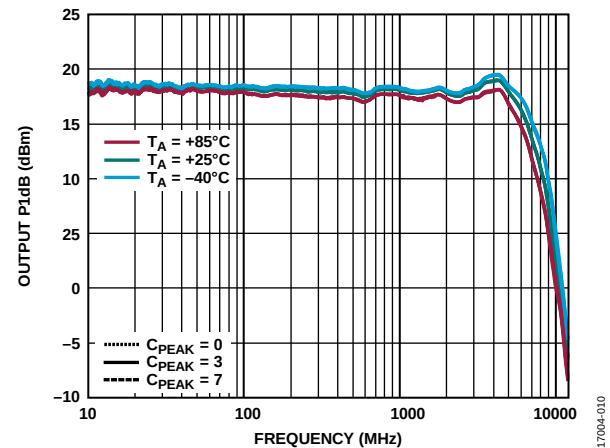


Figure 10. Output P1dB vs. Frequency over Temperature, Supply = Nominal,  $C_{PEAK} = 0$ ,  $C_{PEAK} = 3$ , and  $C_{PEAK} = 7$

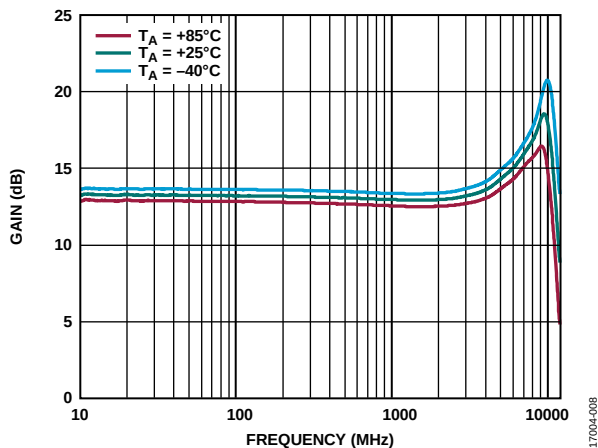


Figure 8. Gain vs. Frequency over Temperature,  $C_{PEAK} = 3$ , Supply = Nominal

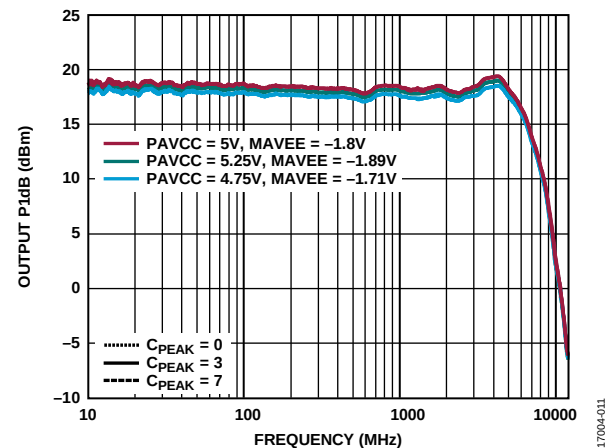


Figure 11. Output P1dB vs. Frequency over Supply, Temperature =  $25^\circ\text{C}$ ,  $C_{PEAK} = 0$ ,  $C_{PEAK} = 3$ , and  $C_{PEAK} = 7$

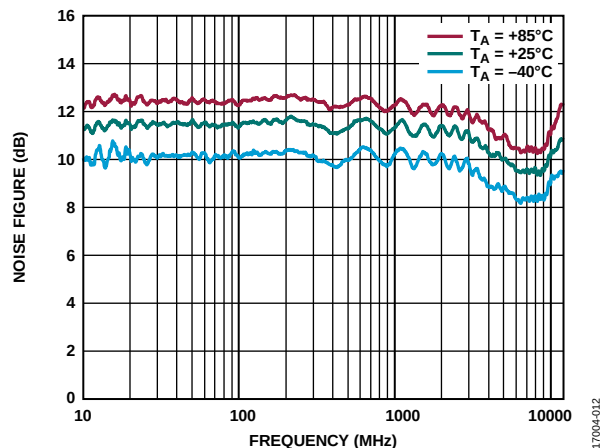


Figure 12. Noise Figure vs. Frequency over Temperature,  $C_{PEAK} = 3$ , Supply = Nominal

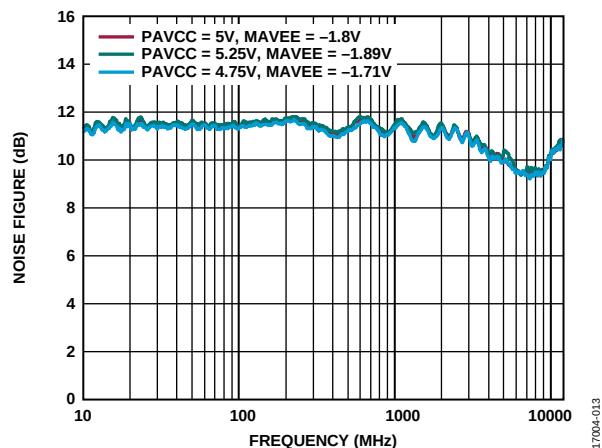


Figure 13. Noise Figure vs. Frequency over Supply,  $C_{PEAK} = 3$ , Temperature = 25°C

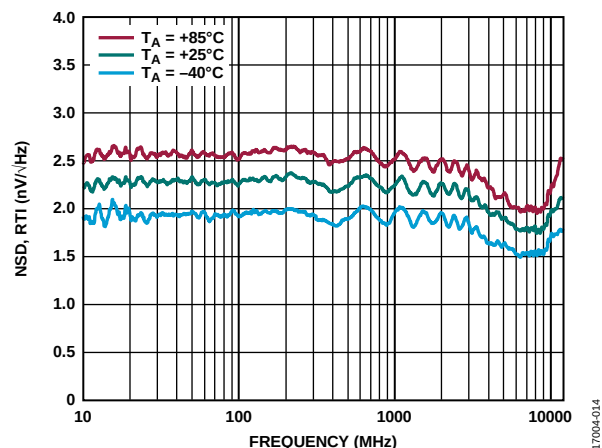


Figure 14. NSD, RTI vs. Frequency over Temperature, Supply = Nominal,  $C_{PEAK} = 3$

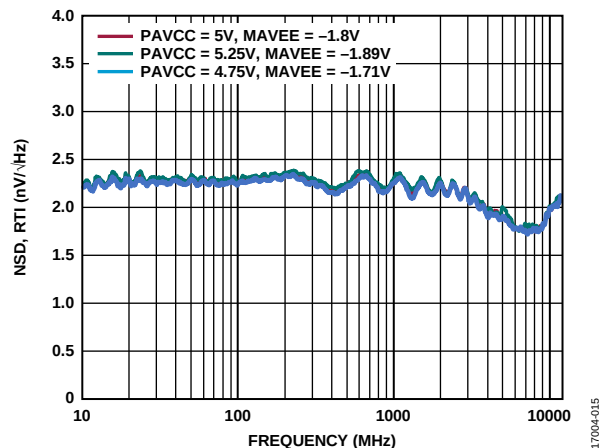


Figure 15. NSD, RTI vs. Frequency over Supply, Temperature = 25°C,  $C_{PEAK} = 3$

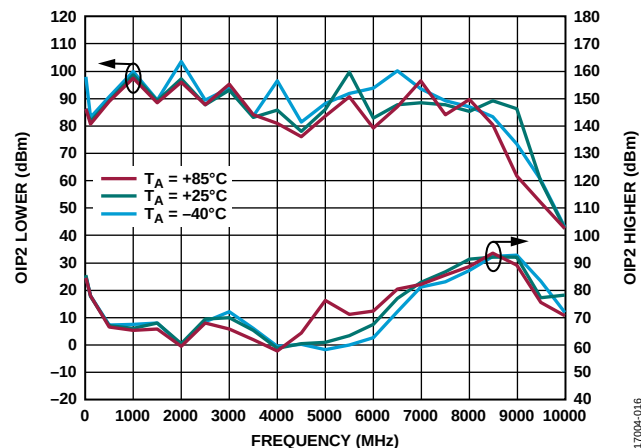


Figure 16. OIP2 Lower and OIP2 Higher vs. Frequency over Temperature, Supply = Nominal,  $C_{PEAK} = 7$

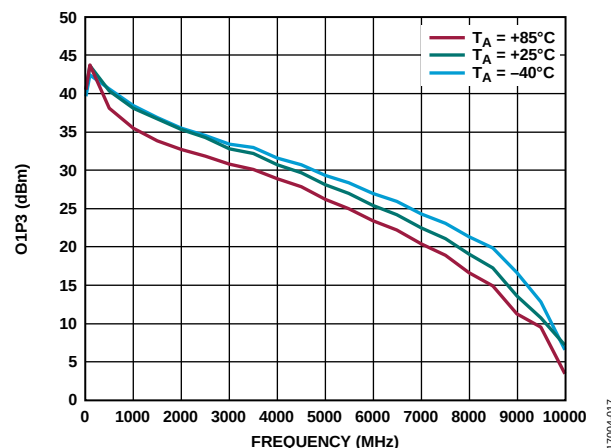


Figure 17. OIP3 vs. Frequency over Temperature, Supply = Nominal,  $C_{PEAK} = 7$

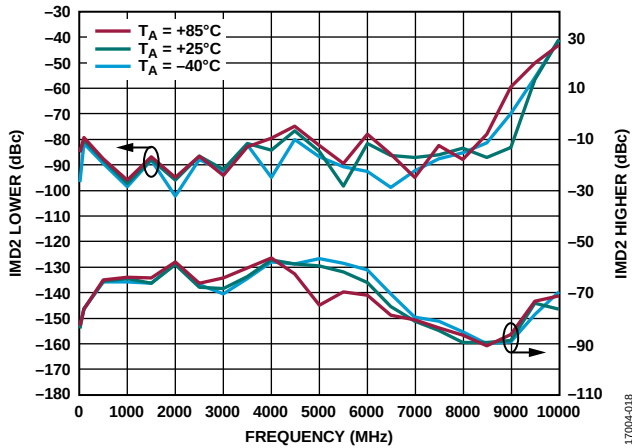


Figure 18. IMD2 Lower and IMD2 Higher vs. Frequency over Temperature, Supply = Nominal,  $C_{PEAK} = 7$

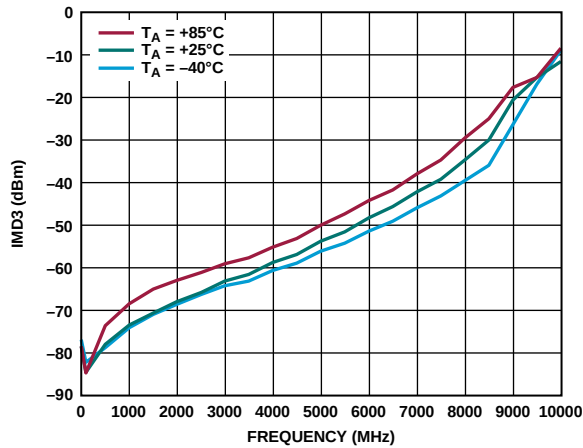


Figure 19. IMD3 vs. Frequency over Temperature, Supply = Nominal and  $C_{PEAK} = 7$

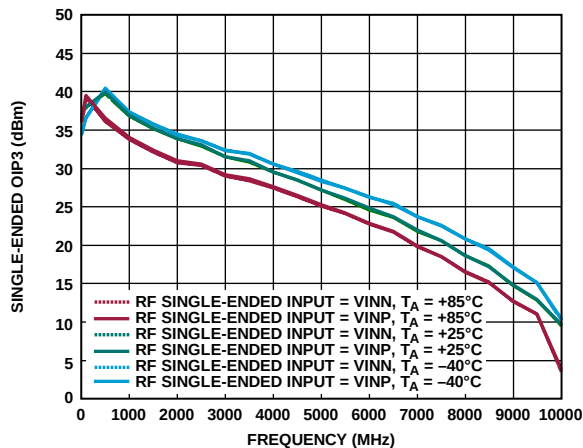


Figure 20. Single-Ended OIP3 vs. Frequency over Temperature

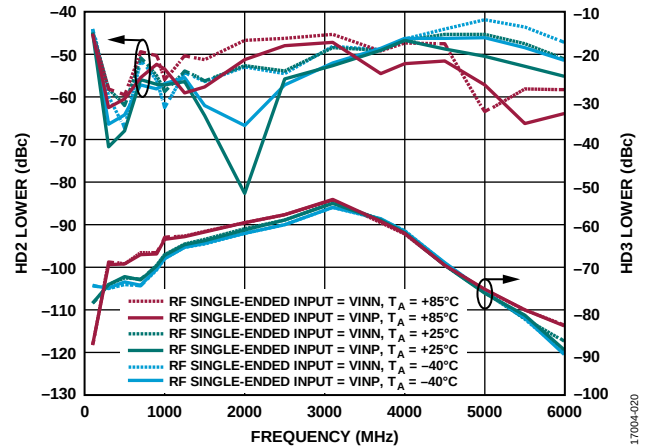


Figure 21. HD2 Lower and HD3 Lower vs. Frequency over Temperature,  $C_{PEAK} = 7$

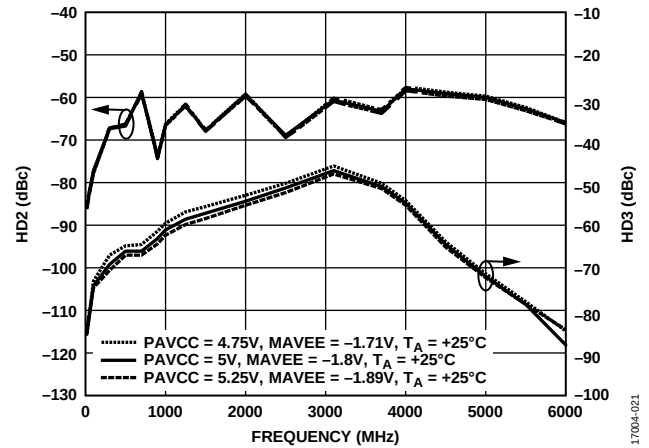


Figure 22. HD2 and HD3 vs. Frequency, Temperature = Nominal, Supply = Nominal, and  $C_{PEAK} = 7$

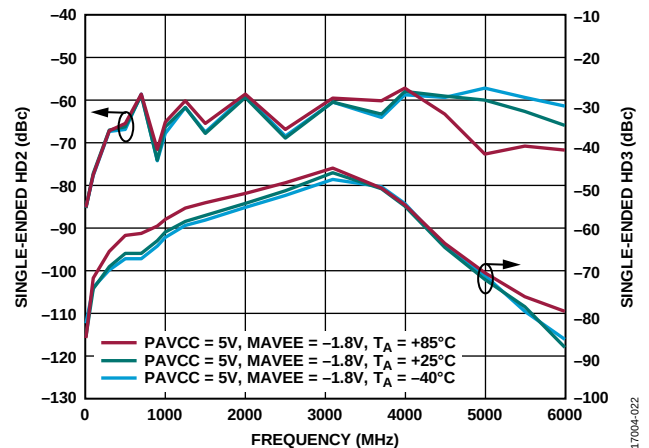


Figure 23. Single-Ended HD2 and HD3 vs. Frequency over Temperature

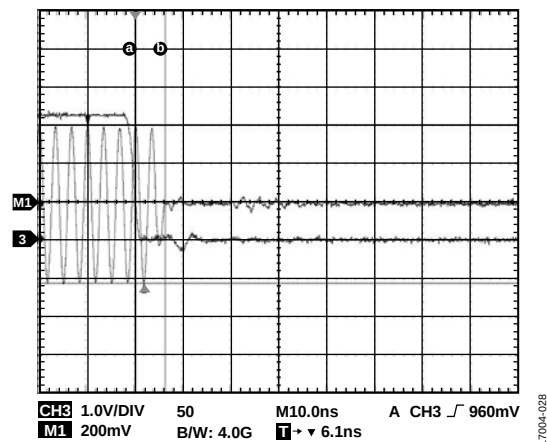


Figure 24. Enable Time Domain Response (Channel 3 (3) Is the Enable Voltage, and Marker 1 (M1) Is the Output Voltage)

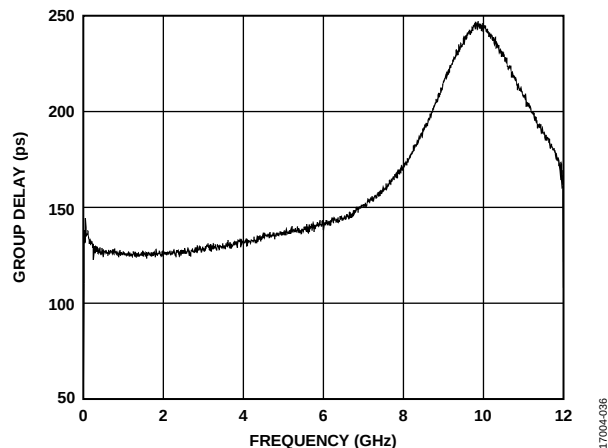


Figure 27. Group Delay vs. Frequency

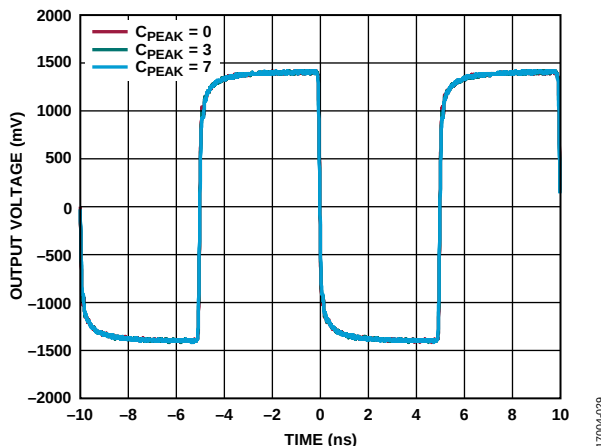


Figure 25. Large Signal Pulse Response

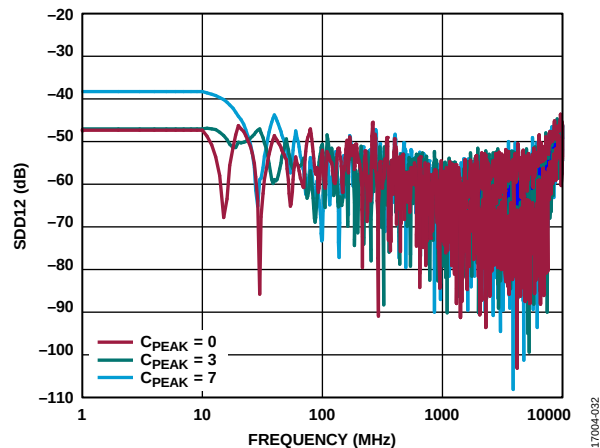


Figure 28. SDD12 vs. Frequency (Red:  $C_{PEAK} = 0$ , Green:  $C_{PEAK} = 3$ , and Blue:  $C_{PEAK} = 7$ )

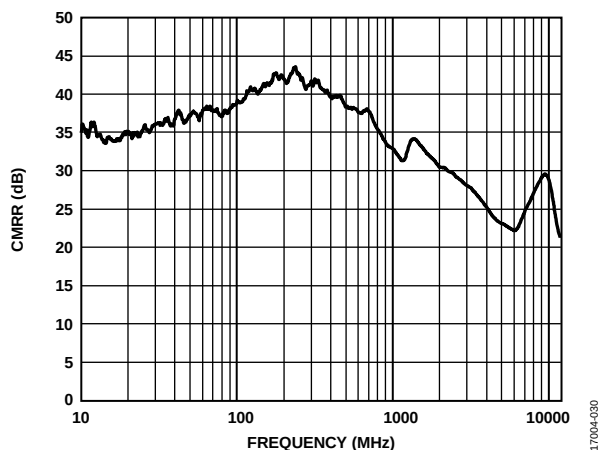


Figure 26. CMRR vs. Frequency

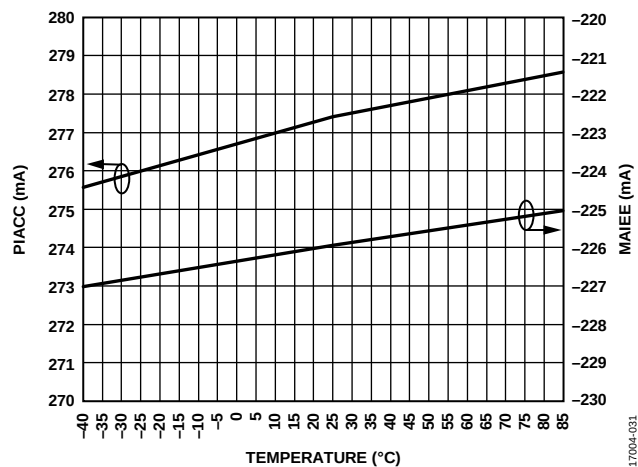


Figure 29. PAVCC Current (PIACC) and MAVEE Current (MAIEE) vs. Temperature

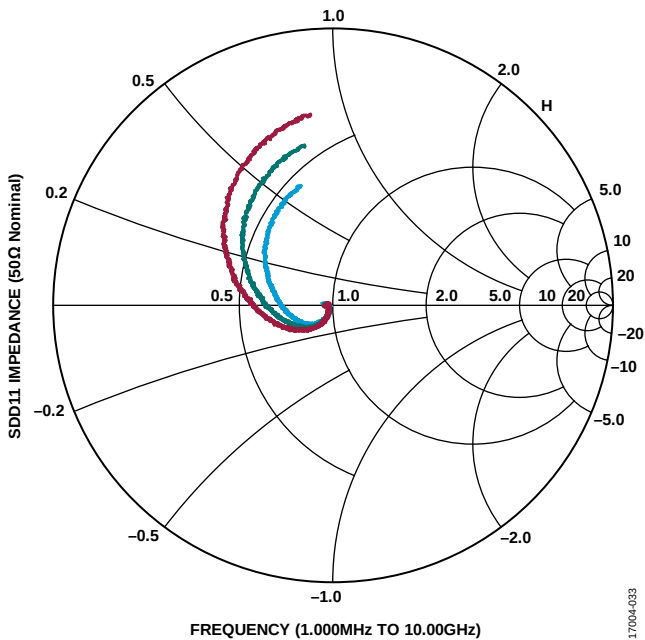


Figure 30. SDD11 Impedance vs. Frequency (Red:  $C_{PEAK} = 0$ , Green:  $C_{PEAK} = 3$ , and Blue:  $C_{PEAK} = 7$ ) (SDD11 Is the Differential S11)

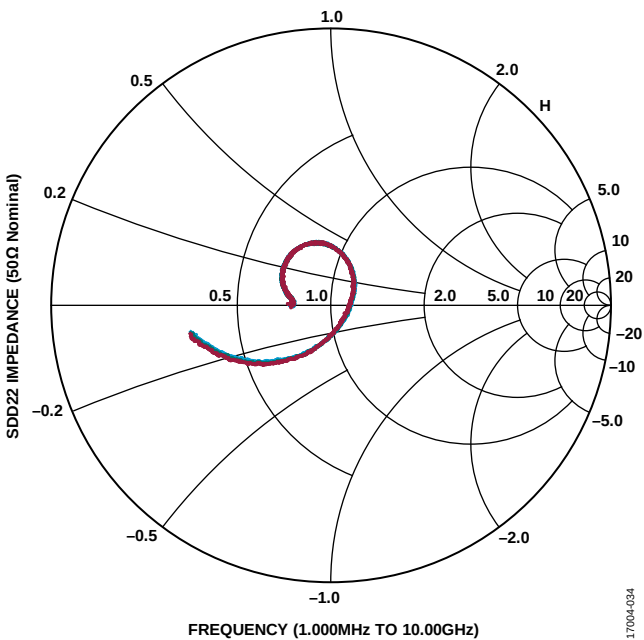


Figure 31. SDD22 Impedance vs. Frequency (Red:  $C_{PEAK} = 0$ , Green:  $C_{PEAK} = 3$ , and Blue:  $C_{PEAK} = 7$ )

## THEORY OF OPERATION

The ADL5580 is a fixed voltage gain (10 dB), fully differential, high linearity amplifier, and ADC driver that operates on a dual power supply voltage, +5 V and -1.8 V.

The small signal -3 dB bandwidth is 10.0 GHz, and all of the integrated building blocks of the ADL5580 are programmable via the SPI.

### RF INPUT AND OUTPUT WITH COMMON-MODE NETWORK

The input impedance is 100  $\Omega$  differential, and the output impedance is 50  $\Omega$  differential, which allows users to drive ADCs like the [AD9213](#) directly without any matching networks, that is at a 50  $\Omega$  differential input. For load conditions other than 50  $\Omega$  differential, external termination networks are required.

The input and output termination blocks have four operation modes that allow users to set the input and output common-mode operation through Register 0x100, Bits[7:0], see Table 7.

In Mode 00, the  $V_{CM}$  terminal must be provided externally on the input termination and the output termination blocks.

For Mode 01, the internal voltage generator (the voltage controlled by two bits) is activated, and the  $V_{CM}$  terminal input and output termination blocks are driven to the internal reference voltage. If the internal reference voltage and the connecting termination blocks have a different  $V_{CM}$ , the behavior of the system is undefined and must be avoided.

Mode 10 is identical to Mode 01 except that the VCMO and VCMi pins are driven to the internal reference voltage to convey the internal  $V_{CM}$  to the connecting termination blocks.

Use Mode 11 to set the internal  $V_{CM}$  termination to externally provide the voltage for the VCMx pins.

### RF SIGNAL CHAIN

The ADL5580 provides another level of control to optimize flatness or wider bandwidth. In applications where flatness is critical, the ADL5580 offers flatness optimization at the expense of the operating bandwidth. However, if the operating

bandwidth is critical, the ADL5580 offers tuning options through the peaking control bits, PRG\_CPEAK\_1P8V (Register 0x101, Bits[6:4]).

#### Enable

The enable bits (EN\_AMP\_1P8V and EN\_REF\_1P8V) are located in Register 0x101, Bit 1 and Bit 0, respectively. These particular enable bits control enabling the amplifier (EN\_AMP\_1P8V) and the reference (EN\_REF\_1P8V). The ADL5580 can be enabled or disabled by using the EN pin (Pin 19), a real-time external pin with no SPI latency

### PROGRAMMABILITY GUIDE

Viewing the register map at the highest level, the registers are subdivided into three memory map functional blocks (see Table 6). See Table 9 for a complete list of all the registers on the ADL5580.

**Table 6. Memory Map Functional Blocks**

| Register Address      | Functional Blocks                 |
|-----------------------|-----------------------------------|
| 0x000 to 0x011        | Analog Devices SPI configuration  |
| 0x100 to 0x101, 0x200 | Signal path configuration, enable |
| 0x300                 | Optional linearity optimization   |

#### SPI

The SPI of the ADL5580 allows the user to configure the device for specific functions or operations via a 3-wire SPI port. It includes enable blocks, the bias current level, transfer function peaking, change input and output termination block operation modes, and change input and output  $V_{CM}$  termination for certain operation modes. This SPI provides users with added flexibility and customization and consists of three control lines: SCLK, SDIO, and CS. The timing requirements for the SPI port are shown in Table 2.

The ADL5580 input logic level for the write cycle is with a 1.8 V logic level.

On a read cycle, the SDIO is configurable for 1.8 V (default) or 3.3 V output levels by setting the SPI\_1P8\_3P3\_CTRL bit (Register 0x200, Bit 0).

**Table 7. Common-Mode Setup Modes**

| Mode | Register 0x100, Bits[7:6] | Register 0x100, Bits[5:4] |            | Register 0x100, Bits[3:2] | Register 0x100, Bits[1:0] |            |
|------|---------------------------|---------------------------|------------|---------------------------|---------------------------|------------|
|      | Output $V_{CM}$ (V)       | Output Internal $V_{CM}$  | VCMO Pin   | Input $V_{CM}$ (V)        | Input Internal $V_{CM}$   | VCMi Pin   |
| 00   | 0.41                      | Disabled                  | Disconnect | 1.39                      | Disabled                  | Disconnect |
| 01   | 0.51                      | Enabled                   | Disconnect | 1.53                      | Enabled                   | Disconnect |
| 10   | 0.60                      | Enabled                   | Export     | 1.67                      | Enabled                   | Export     |
| 11   | 0.70                      | Disabled                  | Import     | 1.80                      | Disabled                  | Import     |

## APPLICATIONS INFORMATION

Figure 32 shows the basic connection diagram, and Table 8 describes the operation of the ADL5580.

The ADL5580 is sensitive to power supplies. Power rail voltages must be brought up and applied in a monotonically increasing

manner without any glitches to avoid issues with the internal digital logic.

The ADL5580 can be ac-coupled, as shown in Figure 32, or the device can be dc-coupled if within the specified input and output  $V_{CM}$  ranges.

## BASIC CONNECTIONS

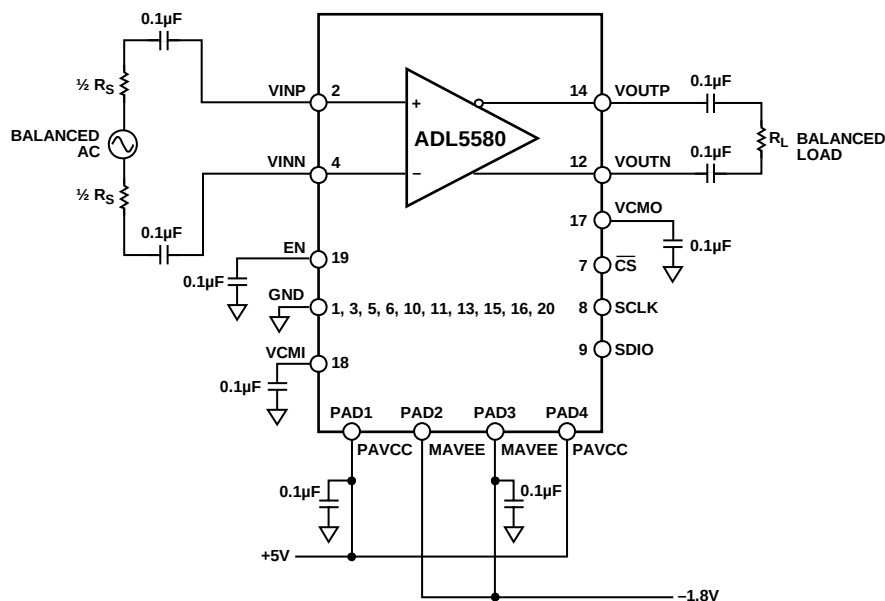


Figure 32. Basic Connection Diagram

Table 8. Basic Connections of the ADL5580

| Functional Blocks | Pin No.                               | Mnemonic               | Description                                                                                              | Basic Connection                                                                                                                    |
|-------------------|---------------------------------------|------------------------|----------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 5 V               | PAD1, PAD4                            | PAVCC                  | Amplifier analog supply voltage, 5 V                                                                     | Decouple each PAVCC pad via 100 pF, 1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pads. |
| –1.8 V            | PAD2, PAD3                            | MAVEE                  | Amplifier analog supply voltage, –1.8 V                                                                  | Decouple each MAVEE pad via 100 pF, 1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pads. |
| RF Input          | 2<br>4<br>18                          | VINP<br>VINN<br>VCM    | Differential RF inputs<br>Positive RF Input<br>Negative RF Input<br>$V_{CM}$ for the RF input signal     | Connect these pins to a differential configuration.                                                                                 |
| RF Output         | 12<br>14<br>17                        | VOUTN<br>VOUTP<br>VCMO | Differential RF outputs<br>Negative RF output<br>Positive RF output<br>$V_{CM}$ for the RF output signal | Connect the RF outputs to a power meter, network analyzer, noise figure meter, or spectrum analyzer.                                |
| Serial Port       | 7<br>8<br>9                           | CS<br>SCLK<br>SDIO     | Chip select active low<br>SPI clock<br>SPI data input output                                             | 1.8 V to 3.3 V tolerant logic levels.<br>1.8 V to 3.3 V tolerant logic levels.<br>1.8 V to 3.3 V tolerant logic levels.             |
| AMP Control       | 19                                    | EN                     | Amplifier enable                                                                                         | 1.8 V to 3.3 V tolerant logic levels.                                                                                               |
| Ground            | 1, 3, 5, 6, 10, 11,<br>13, 15, 16, 20 | GND                    | Ground                                                                                                   | Connect the GND pins to the ground of the PCB.                                                                                      |



## INPUT AND OUTPUT INTERFACING

### Differential Input to Differential Output

The ADL5580 can be configured as a differential input to differential output driver (see Figure 33). The  $50\ \Omega$  resistors, R1 and R2, combined with the  $100\ \Omega$  input impedance provide a  $50\ \Omega$  input match with the 1:1 balun. The input and output  $0.1\ \mu\text{F}$  capacitors isolate the common-mode bias voltage ( $V_{\text{BIAS}}$ ) on input and output pins from the source and balanced load. The load is  $50\ \Omega$  to provide the expected ac performance.

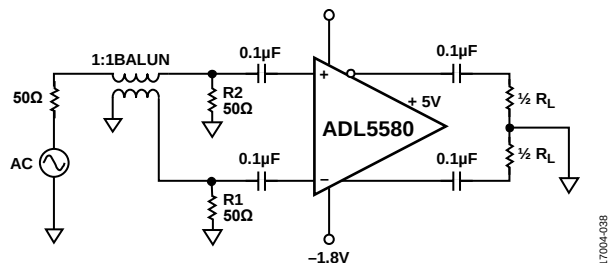


Figure 33. Differential Input to Differential Output Configuration

The differential gain of the ADL5580 is dependent on the source impedance and load, as shown in Figure 34.

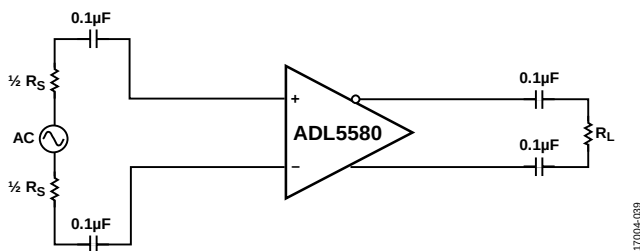


Figure 34. Differential Input Loading Circuit

### Single-Ended Input to Differential Output

The ADL5580 can also be configured in a single-ended input to differential output configuration. In this configuration, the gain of the device is reduced due to the application of the signal to only one side of the amplifier. The input and output  $0.1\ \mu\text{F}$  capacitors isolate the  $V_{\text{CM}}$  on input and output pins from the source and balanced load.

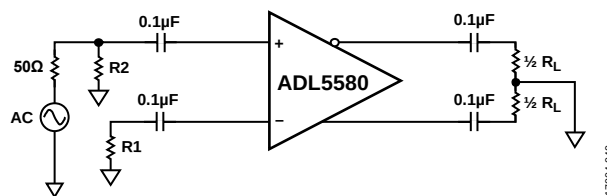


Figure 35. Single-Ended Input to Differential Output Configuration

The ADL5580 is a high output linearity, fixed gain dc-coupled amplifier for multigigasample ADC interfacing. The open-loop architecture anticipates a  $50\ \Omega$  differential dc output load. The maximum linear output swing is optimized for 1.4 V p-p differential.

## LAYOUT

Solder the four exposed power supply pads on the underside of the ADL5580 to a low thermal and electrical impedance power plane. These pads are typically soldered to exposed opens in the solder mask on the evaluation board. Notice the use of 4 via holes on each exposed power pad of the [ADL5580-EVALZ](#). Connect these power vias to power layers on the evaluation board to maximize heat dissipation from the device package. For more information on the evaluation board, see the [ADL5580-EVALZ](#) product page.

Ensure that the decoupling capacitors are located close to the supply voltage pins.

## REGISTER SUMMARY

Table 9.

| Reg   | Name           | Bits  | Bit 7                | Bit 6          | Bit 5             | Bit 4      | Bit 3         | Bit 2      | Bit 1        | Bit 0                   | Reset            | R/W  |     |
|-------|----------------|-------|----------------------|----------------|-------------------|------------|---------------|------------|--------------|-------------------------|------------------|------|-----|
| 0x000 | ADI_SPI_CONFIG | [7:0] | SOFTRESET_           | LSB_FIRST_     | ENDIAN_           | SDOACTIVE_ | SDOACTIVE     | ENDIAN     | LSB_FIRST    | SOFTRESET               | 0x00             | R/W  |     |
| 0x001 | REG_0X0001     | [7:0] | SINGLE_ INTSTRUCTION | CSB_STALL      | MASTER_ SLAVE_ RB | RESERVED   |               | SOFT_RESET |              | MASTER_ SLAVE_ TRANSFER | 0x00             | R/W  |     |
| 0x003 | CHIPTYPE       | [7:0] | CHIPTYPE             |                |                   |            |               |            |              |                         |                  | 0x01 | R   |
| 0x004 | PRODUCT_ID_L   | [7:0] | PRODUCT_ID_L         |                |                   |            |               |            |              |                         |                  | 0x03 | R   |
| 0x005 | PRODUCT_ID_H   | [7:0] | PRODUCT_ID_H         |                |                   |            |               |            |              |                         |                  | 0x00 | R   |
| 0x00A | SCRATCHPAD     | [7:0] | SCRATCHPAD           |                |                   |            |               |            |              |                         |                  | 0x00 | R/W |
| 0x00B | SPI_REV        | [7:0] | SPI_REV              |                |                   |            |               |            |              |                         |                  | 0x00 | R   |
| 0x010 | VARIANT_FEOL   | [7:0] | FEOL                 |                |                   |            | VARIANT       |            |              |                         | 0x00             | R    |     |
| 0x011 | BEOL_SIF       | [7:0] | SIF                  |                |                   |            | BEOL          |            |              |                         | 0x00             | R    |     |
| 0x100 | GEN_CTL0       | [7:0] | PRG_OTRM_1P8V        |                | MS_OTRM_1P8V      |            | PRG_ITRM_1P8V |            | MS_ITRM_1P8V |                         | 0x78             | R/W  |     |
| 0x101 | GEN_CTL1       | [7:0] | RESERVED             | PRG_CPEAK_1P8V |                   |            | RESERVED      |            | EN_AMP_1P8V  | EN_REF_1P8V             | 0x33             | R/W  |     |
| 0x200 | SPI_CTL        | [7:0] | RESERVED             |                |                   |            |               |            |              |                         | SPI_1P8_3P3_CTRL | 0x01 | R/W |

## REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: ADI\_SPI\_CONFIG

Table 10. Bit Descriptions for ADI\_SPI\_CONFIG

| Bit(s) | Bit Name   | Description                                              | Reset | Access |
|--------|------------|----------------------------------------------------------|-------|--------|
| 7      | SOFTRESET_ | Soft Reset<br>0: reset asserted<br>1: reset not asserted | 0x00  | R/W    |
| 6      | LSB_FIRST_ | LSB First<br>0: LSB first<br>1: MSB first                | 0x00  | R/W    |
| 5      | ENDIAN_    | Endian<br>0: little endian<br>1: big endian              | 0x00  | R/W    |
| 4      | SDOACTIVE_ | SDO Active<br>0: SDO inactive<br>1: SDO active           | 0x00  | R/W    |
| 3      | SDOACTIVE  | SDO Active<br>0: SDO inactive<br>1: SDO active           | 0x00  | R/W    |
| 2      | ENDIAN     | Endian<br>0: little endian<br>1: big endian              | 0x00  | R/W    |
| 1      | LSB_FIRST  | LSB First<br>0: LSB first<br>1: MSB first                | 0x00  | R/W    |
| 0      | SOFTRESET  | Soft Reset<br>0: reset asserted<br>1: reset not asserted | 0x00  | R/W    |

Address: 0x001, Reset: 0x00, Name: REG\_0X0001

Table 11. Bit Descriptions for REG\_0X0001

| Bit(s) | Bit Name              | Description                           | Reset | Access |
|--------|-----------------------|---------------------------------------|-------|--------|
| 7      | SINGLE_INTSTRUCTION   | Single Instruction                    | 0x00  | R/W    |
| 6      | CSB_STALL             | Chip Select ( $\overline{CS}$ ) Stall | 0x00  | R/W    |
| 5      | MASTER_SLAVE_RB       | Master Slave Read Back (RB)           | 0x00  | R/W    |
| [4:3]  | RESERVED              | Reserved                              | 0x00  | R      |
| [2:1]  | SOFT_RESET            | Soft Reset                            | 0x00  | R/W    |
| 0      | MASTER_SLAVE_TRANSFER | Master Slave Transfer                 | 0x00  | R/W    |

Address: 0x003, Reset: 0x01, Name: CHIPTYPE

Table 12. Bit Descriptions for CHIPTYPE

| Bit(s) | Bit Name | Description          | Reset | Access |
|--------|----------|----------------------|-------|--------|
| [7:0]  | CHIPTYPE | Chip Type, Read Only | 0x01  | R      |

Address: 0x004, Reset: 0x03, Name: PRODUCT\_ID\_L

Table 13. Bit Descriptions for PRODUCT\_ID\_L

| Bit(s) | Bit Name     | Description                | Reset | Access |
|--------|--------------|----------------------------|-------|--------|
| [7:0]  | PRODUCT_ID_L | Product_ID_L, Lower 8 Bits | 0x03  | R      |

Address: 0x005, Reset: 0x00, Name: PRODUCT\_ID\_H

Table 14. Bit Descriptions for PRODUCT\_ID\_H

| Bit(s) | Bit Name     | Description                 | Reset | Access |
|--------|--------------|-----------------------------|-------|--------|
| [7:0]  | PRODUCT_ID_H | Product_ID_H, Higher 8 Bits | 0x00  | R      |

Address: 0x00A, Reset: 0x00, Name: SCRATCHPAD

Table 15. Bit Descriptions for SCRATCHPAD

| Bit(s) | Bit Name   | Description | Reset | Access |
|--------|------------|-------------|-------|--------|
| [7:0]  | SCRATCHPAD | Scratch Pad | 0x00  | R/W    |

Address: 0x00B, Reset: 0x00, Name: SPI\_REV

Table 16. Bit Descriptions for SPI\_REV

| Bit(s) | Bit Name | Description               | Reset | Access |
|--------|----------|---------------------------|-------|--------|
| [7:0]  | SPI_REV  | SPI Register Map Revision | 0x00  | R      |

Address: 0x010, Reset: 0x00, Name: VARIANT\_FEOL

Table 17. Bit Descriptions for VARIANT\_FEOL

| Bit(s) | Bit Name | Description              | Reset | Access |
|--------|----------|--------------------------|-------|--------|
| [7:4]  | FEOL     | Front End of Line (FEOL) | 0x00  | R      |
| [3:0]  | VARIANT  | Variant                  | 0x00  | R      |

Address: 0x011, Reset: 0x00, Name: BEOL\_SIF

Table 18. Bit Descriptions for BEOL\_SIF

| Bit(s) | Bit Name | Description                           | Reset | Access |
|--------|----------|---------------------------------------|-------|--------|
| [7:4]  | SIF      | Stress Intensity Factor (SIF) Version | 0x00  | R      |
| [3:0]  | BEOL     | Back End of Line (BEOL) Version       | 0x00  | R      |

Address: 0x100, Reset: 0x78, Name: GEN\_CTL0

Table 19. Bit Descriptions for GEN\_CTL0

| Bit(s) | Bit Name      | Description                                                                                  | Reset | Access |
|--------|---------------|----------------------------------------------------------------------------------------------|-------|--------|
| [7:6]  | PRG_OTRM_1P8V | These bits set up the output $V_{CM}$ .                                                      | 0x1   | R/W    |
| [5:4]  | MS_OTRM_1P8V  | These bits set $V_{CM}$ to internal or external and set the VC <sub>MO</sub> pin definition. | 0x3   | R/W    |
| [3:2]  | PRG_ITRM_1P8V | These bits set up the input $V_{CM}$ .                                                       | 0x2   | R/W    |
| [1:0]  | MS_ITRM_1P8V  | These bits set $V_{CM}$ to internal or external and set the VC <sub>MI</sub> pin definition. | 0x0   | R/W    |

Address: 0x101, Reset: 0x33, Name: GEN\_CTL1

Table 20. Bit Descriptions for GEN\_CTL1

| Bit(s) | Bit Name       | Description                    | Reset | Access |
|--------|----------------|--------------------------------|-------|--------|
| 7      | RESERVED       | Reserved.                      | 0x0   | R      |
| [6:4]  | PRG_CPEAK_1P8V | These bits set up $C_{PEAK}$ . | 0x3   | R/W    |
| [3:2]  | RESERVED       | Reserved.                      | 0x0   | R      |
| 1      | EN_AMP_1P8V    | Enable Amplifier Block.        | 0x1   | R/W    |
| 0      | EN_REF_1P8V    | Enable Reference Block.        | 0x1   | R/W    |

Address: 0x200, Reset: 0x01, Name: SPI\_CTL

Table 21. Bit Descriptions for SPI\_CTL

| Bit(s) | Bit Name         | Description                                                  | Reset | Access |
|--------|------------------|--------------------------------------------------------------|-------|--------|
| [7:1]  | RESERVED         | Reserved                                                     | 0x0   | R      |
| 0      | SPI_1P8_3P3_CTRL | SPI Supply Control<br>0: 1.8 V readback<br>1: 3.3 V readback | 0x1   | R/W    |

## OUTLINE DIMENSIONS

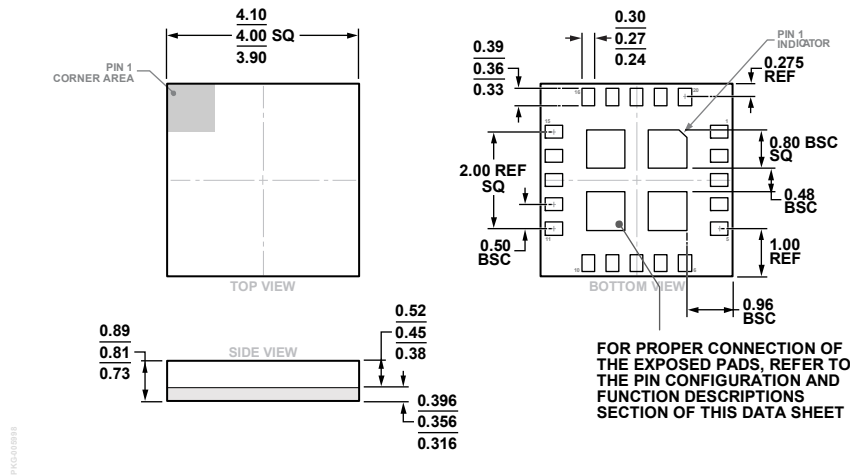


Figure 36. 20-Terminal Land Grid Array [LGA]  
(CC-20-7)

Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                                                        | Package Option |
|--------------------|-------------------|----------------------------------------------------------------------------|----------------|
| ADL5580BCCZ        | −40°C to +85°C    | 20-Terminal Land Grid Array [LGA]                                          | CC-20-7        |
| ADL5580BCCZ-R7     | −40°C to +85°C    | 20-Terminal Land Grid Array [LGA]                                          | CC-20-7        |
| ADL5580-EVALZ      |                   | Evaluation Board                                                           |                |
| AD-FMCADC20-DC-EBZ |                   | DC-Coupled Combination <a href="#">AD9213</a> and ADL5580 Reference Design |                |
| AD-FMCADC20-EBZ    |                   | AC-Coupled Combination <a href="#">AD9213</a> and ADL5580 Reference Design |                |

<sup>1</sup> Z = RoHS-Compliant Part.

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