

## 0.56 $\Omega$ On Resistance High Density Octal SPST Switch

### FEATURES

- ▶ 0.56  $\Omega$  typical on resistance
- ▶ High continuous current of up to 768 mA
- ▶ Flat  $R_{ON}$  across signal range, 0.004  $\Omega$
- ▶ THD of -122 dB at 1 kHz
- ▶ Route through pins for digital signals and supplies
- ▶ Integrated passive components
- ▶ SPI interface with error detection
- ▶ Guaranteed break-before-make switching, allowing external wiring of switches to deliver multiplexer configurations
- ▶ Fully specified at  $\pm 15$  V and  $+12$  V
- ▶ 1.8 V logic compatibility with  $2.7 \text{ V} \leq V_L \leq 3.3 \text{ V}$  (excludes SPI read-back to a 1.8 V device)
- ▶ 4 mm  $\times$  5 mm, 30-terminal LGA

### APPLICATIONS

- ▶ Automatic test equipment
- ▶ Instrumentation
- ▶ Data acquisition
- ▶ Relay replacement
- ▶ Avionics
- ▶ Audio and video switching
- ▶ Communication systems

### FUNCTIONAL BLOCK DIAGRAM

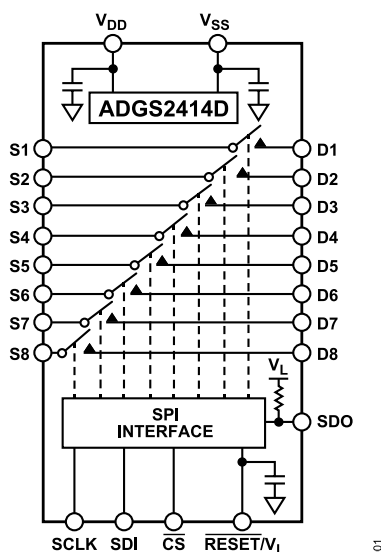


Figure 1. Functional Block Diagram

### GENERAL DESCRIPTION

The ADGS2414D contains eight independent, low on-resistance, single-pole/single-throw (SPST) switches in a 4 mm  $\times$  5 mm, 30 pin LGA package.

The ADGS2414D enables higher channel density in systems where printed circuit board space is constrained or existing system form factors restrict expansion.

When using SPI daisy-chain mode, the unique route through pins, provide considerable space savings when multiple ADGS2414D instances are combined to design very high channel count systems, such as large switching matrices and fanout applications. The integrated supply decoupling capacitors and SDO pullup resistor further increase the space savings and reduce printed circuit board complexity.

The low on-resistance (0.56  $\Omega$  typical) of each switch channel allows for higher current density in systems where heat dissipation is an issue, and the on-resistance profile of the switch channels is exceptionally flat over the full-analog input range, which ensures good linearity and low distortion when switching precision analog signals.

Each switch has an input signal range from  $V_{SS}$  to  $V_{DD} - 2 \text{ V}$ . When on, each switch conducts equally well in both directions, and in the off condition, signal levels up to the supplies are blocked.

The SPI has robust error detection features, such as cyclic redundancy check (CRC) error detection, invalid read and write address detection, and SCLK count error detection.

### PRODUCT HIGHLIGHTS

1. The SPI removes the need for parallel conversion, logic traces, and reduces the general-purpose input/output (GPIO) channel count.
2. Daisy-chain mode removes additional logic traces when multiple devices are used.
3. Route through of digital signals and supplies eases routing and allows for an increase in channel density.
4. Integrated passive components eliminate the need for external passive components.
5. CRC error detection, invalid read and write address detection, and SCLK count error detection ensure a robust digital interface.
6. CRC, invalid read and write address, and SCLK error detection capabilities allow for the use of the ADGS2414D in safety-critical systems.
7. Pin for pin replacement for the ADGS1414D.

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**REVISION HISTORY****12/2023—Revision 0: Initial Version**

## SPECIFICATIONS

## OPERATING SUPPLY VOLTAGES

Table 1. Operating Supply Voltages

Supply Voltage	Min	Max	Unit
Dual Supply	±4.5	±16.5	V
Single Supply	+5	+20	V

## ±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = 2.7\text{ V to } 5.5\text{ V}$ , and  $\text{GND} = 0\text{ V}$ , unless otherwise noted.

Table 2. ±15 V Dual Supply

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD} - 2\text{ V to } V_{SS}$	V	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On Resistance, $R_{ON}$	0.56			$\Omega$ typ	Source voltage, ( $V_S$ ) = -13.5 V to +10 V, source current, ( $I_S$ ) = -100 mA, see <a href="#">Figure 29</a>
	0.7	0.85	1.0	$\Omega$ max	
	0.6			$\Omega$ typ	$V_S = -13.5\text{ V to } +11\text{ V}$ , $I_S = -100\text{ mA}$
	0.75	0.9	1.05	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.045			$\Omega$ typ	$V_S = -13.5\text{ V to } +11\text{ V}$ , $I_S = -100\text{ mA}$
	0.12	0.14	0.16	$\Omega$ max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.004			$\Omega$ typ	$V_S = -13.5\text{ V to } +10\text{ V}$ , $I_S = -100\text{ mA}$
	0.035	0.035	0.035	$\Omega$ max	
	0.04			$\Omega$ typ	$V_S = -13.5\text{ V to } +11\text{ V}$ , $I_S = -100\text{ mA}$
	0.08	0.1	0.1	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	±1.7			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$ , drain voltage, $V_D = \mp 10\text{ V}$ , see <a href="#">Figure 30</a>
	±4.0	+40/-5.5	+120/-5.5	nA max	
Drain Off Leakage, $I_D$ (Off)	±1.7			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ , see <a href="#">Figure 30</a>
	±4.0	+40/-5.5	+120/-5.5	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	±0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$ , see <a href="#">Figure 31</a>
	±1.3	±3.0	+12.5/-3.0	nA max	
<b>DIGITAL OUTPUT</b>					
Output Voltage					
Low, $V_{OL}$			0.4	V max	Sink current, $I_{SINK} = 1\text{ mA}$
			0.3	V max	$I_{SINK} = 100\text{ }\mu\text{A}$
High, $V_{OH}$			$V_L - 1.25\text{ V}$	V min	Source current, $I_{SOURCE} = 1\text{ mA}$
			$V_L - 0.125\text{ V}$	V min	$I_{SOURCE} = 100\text{ }\mu\text{A}$
Digital Output Capacitance, $C_{OUT}$	4			pF typ	
<b>DIGITAL INPUTS</b>					
Input Voltage					
High, $V_{INH}$			2	V min	$3.3\text{ V} < V_L \leq 5.5\text{ V}$
			1.35	V min	$2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Low, $V_{INL}$			0.8	V max	$3.3\text{ V} < V_L \leq 5.5\text{ V}$
			0.8	V max	$2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Input Current					
Low, $I_{INL}$ or High, $I_{INH}$	0.001			$\mu\text{A}$ typ	Input voltage, $V_{IN} = \text{ground voltage, } V_{GND} \text{ or } V_L$
			±0.1	$\mu\text{A}$ max	

## SPECIFICATIONS

Table 2.  $\pm 15$  V Dual Supply (Continued)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Digital Input Capacitance, $C_{IN}$	4			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, $t_{ON}$	600			ns typ	Load resistance, $R_L = 300\ \Omega$ , load capacitance, $C_L = 35\ \text{pF}$ , $V_S = 10\ \text{V}$ , see Figure 38
Off Time, $t_{OFF}$	701	723	749	ns max	
	196			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\ \text{pF}$ , $V_S = 10\ \text{V}$ , see Figure 38
	250	252	254	ns max	
Break-Before-Make Time Delay, $t_D$	429			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\ \text{pF}$ , Source 1 voltage, $V_{S1} =$ Source 2 voltage, $V_{S2} = 10\ \text{V}$ , see Figure 37
Charge Injection, $Q_{INJ}$	349	358	385	ns min	
	-1.8			nC typ	$V_S = 0\ \text{V}$ , source resistance $R_S = 0\ \Omega$ , $C_L = 1\ \text{nF}$ , see Figure 39
Off Isolation	-76			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , frequency, $f = 100\ \text{kHz}$ , see Figure 33
Channel to Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $f = 100\ \text{kHz}$ , see Figure 32
Total Harmonic Distortion + Noise, THD + N	0.002			% typ	$R_L = 1\ \text{k}\Omega$ , 20 V p-p, $f = 20\ \text{Hz}$ to 20 kHz, see Figure 34
Total Harmonic Distortion, THD	-122			dB typ	$R_L = 1\ \text{k}\Omega$ , 20 V p-p, $f = 1\ \text{kHz}$
	-96			dB typ	$R_L = 1\ \text{k}\Omega$ , 20 V p-p, $f = 20\ \text{kHz}$
	-80			dB typ	$R_L = 1\ \text{k}\Omega$ , 20 V p-p, $f = 100\ \text{kHz}$
-3 dB Bandwidth	171			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , see Figure 35
Insertion Loss	-0.06			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $f = 1\ \text{MHz}$ , see Figure 35
Source Capacitance, $C_S$ (Off)	76			pF typ	$V_S = 0\ \text{V}$ , $f = 1\ \text{MHz}$
Drain Capacitance, $C_D$ (Off)	76			pF typ	$V_S = 0\ \text{V}$ , $f = 1\ \text{MHz}$
$C_D$ (On), $C_S$ (On)	28			pF typ	$V_S = 0\ \text{V}$ , $f = 1\ \text{MHz}$
POWER REQUIREMENTS					
Positive Supply Current, $I_{DD}$	330			$\mu\text{A}$ typ	$V_{DD} = +16.5\ \text{V}$ , $V_{SS} = -16.5\ \text{V}$ All switches open
			440	$\mu\text{A}$ max	
	350			$\mu\text{A}$ typ	All switches closed, $V_L = 5.5\ \text{V}$
			460	$\mu\text{A}$ max	
	350			$\mu\text{A}$ typ	All switches closed, $V_L = 2.7\ \text{V}$
			460	$\mu\text{A}$ max	
Load Current, $I_L$					
	Inactive			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_L$
			8.5	$\mu\text{A}$ max	
				$\mu\text{A}$ typ	Digital inputs = 0 V or 3 V
			4.0	$\mu\text{A}$ max	
Inactive, SCLK = 1 MHz	14			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	7			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\ \text{V}$
				$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	390			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\ \text{V}$
	210			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\ \text{V}$
				$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\ \text{V}$
Inactive, SDI = 1 MHz	15			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\ \text{V}$
	7.5			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\ \text{V}$
				$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\ \text{V}$
	230			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	120			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\ \text{V}$
				$\mu\text{A}$ typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\ \text{V}$
Active at 50 MHz	7.0			mA typ	
			9.0	mA max	

## SPECIFICATIONS

Table 2.  $\pm 15$  V Dual Supply (Continued)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Negative Supply Current, $I_{SS}$	3.3			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7$ V
			5.0	mA max	
	180			$\mu$ A typ	Digital inputs = 0 V or $V_L$
			250	$\mu$ A max	

## 12 V SINGLE SUPPLY

$V_{DD} = 12$  V  $\pm 10\%$ ,  $V_{SS} = 0$  V,  $V_L = 2.7$  V to 5.5 V, and GND = 0 V, unless otherwise noted.

Table 3. 12 V Single Supply

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V <sub>DD</sub> - 2 V	V	V <sub>DD</sub> = 10.8 V, V <sub>SS</sub> = 0 V
R <sub>ON</sub>	0.56			Ω typ	V <sub>S</sub> = 0 V to 7.3 V, I <sub>S</sub> = −100 mA
	0.7	0.85	1.0	Ω max	
	0.6			Ω typ	V <sub>S</sub> = 0 V to 8.3 V, I <sub>S</sub> = −100 mA
	0.75	0.9	1.05	Ω max	
ΔR <sub>ON</sub>	0.45			Ω typ	V <sub>S</sub> = 0 V to 8.3 V, I <sub>S</sub> = −100 mA
	0.12	0.14	0.16	Ω max	
R <sub>FLAT</sub> (ON)	0.004			Ω typ	V <sub>S</sub> = 0 V to 7.3 V, I <sub>S</sub> = −100 mA
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V <sub>S</sub> = 0 V to 8.3 V, I <sub>S</sub> = −100 mA
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					
I <sub>S</sub> (Off)	±1.7			nA typ	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V
	±4.0	+40/-5.5	+120/-5.5	nA max	V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V
I <sub>D</sub> (Off)	±1.7			nA typ	V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V
	±4.0	+40/-5.5	+120/-5.5	nA max	
I <sub>D</sub> (On), I <sub>S</sub> (On)	±0.1			nA typ	V <sub>S</sub> = V <sub>D</sub> = 1 V/10 V
	±1.3	±3	+12.5/-3.0	nA max	
DIGITAL OUTPUT					
Output Voltage					
Low, V <sub>OL</sub>			0.4	V max	I <sub>SINK</sub> = 1 mA
			0.3	V max	I <sub>SINK</sub> = 100 μA
High, V <sub>OH</sub>			V <sub>L</sub> − 1.25 V	V min	I <sub>SOURCE</sub> = 1 mA
			V <sub>L</sub> − 0.125 V	V min	I <sub>SOURCE</sub> = 100 μA
C <sub>OUT</sub>	4			pF typ	
DIGITAL INPUTS					
Input Voltage					
High, V <sub>INH</sub>			2	V min	3.3 V < V <sub>L</sub> ≤ 5.5 V
			1.35	V min	2.7 V ≤ V <sub>L</sub> ≤ 3.3 V
Low, V <sub>INL</sub>			0.8	V max	3.3 V < V <sub>L</sub> ≤ 5.5 V
			0.8	V max	2.7 V ≤ V <sub>L</sub> ≤ 3.3 V
Input Current					
Low, I <sub>INL</sub> or High, I <sub>INH</sub>	0.001			μA typ	V <sub>IN</sub> = V <sub>GND</sub> or V <sub>L</sub>
			±0.1	μA max	
C <sub>IN</sub>	4			pF typ	
DYNAMIC CHARACTERISTICS					

## SPECIFICATIONS

Table 3. 12 V Single Supply (Continued)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
$t_{ON}$	473			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\ \text{pF}$ , $V_S = 8\ \text{V}$
	550	551	556	ns max	
$t_{OFF}$	297			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\ \text{pF}$ , $V_S = 8\ \text{V}$
	348	352	356	ns max	
$t_D$	245			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\ \text{pF}$ , $V_{S1} = V_{S2} = 8\ \text{V}$
	195	200	207	ns min	
$Q_{INJ}$	-1.1			nC typ	$V_S = 6\ \text{V}$ , $R_S = 0\ \Omega$ , $C_L = 1\ \text{nF}$
Off Isolation	-61			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $f = 100\ \text{kHz}$
Channel to Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $f = 100\ \text{kHz}$
THD + N	0.005			% typ	$R_L = 1\ \text{k}\Omega$ , 6 V p-p, $f = 20\ \text{Hz}$ to $20\ \text{kHz}$
THD	-111			dB typ	$R_L = 1\ \text{k}\Omega$ , 6 V p-p, $f = 1\ \text{kHz}$
	-85			dB typ	$R_L = 1\ \text{k}\Omega$ , 6 V p-p, $f = 20\ \text{kHz}$
	-71			dB typ	$R_L = 1\ \text{k}\Omega$ , 6 V p-p, $f = 100\ \text{kHz}$
-3 dB Bandwidth	114			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$
Insertion Loss	-0.06			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $f = 1\ \text{MHz}$
$C_S$ (Off)	100			pF typ	$V_S = 6\ \text{V}$ , $f = 1\ \text{MHz}$
$C_D$ (Off)	100			pF typ	$V_S = 6\ \text{V}$ , $f = 1\ \text{MHz}$
$C_D$ (On), $C_S$ (On)	37			pF typ	$V_S = 6\ \text{V}$ , $f = 1\ \text{MHz}$
POWER REQUIREMENTS					$V_{DD} = 13.2\ \text{V}$
$I_{DD}$	330			$\mu\text{A}$ typ	All switches open
			440	$\mu\text{A}$ max	
	350			$\mu\text{A}$ typ	All switches closed, $V_L = 5.5\ \text{V}$
			460	$\mu\text{A}$ max	
	350			$\mu\text{A}$ typ	All switches closed, $V_L = 2.7\ \text{V}$
			460	$\mu\text{A}$ max	
$I_L$					
Inactive	6.3			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_L$
			8.5	$\mu\text{A}$ max	
	2.5			$\mu\text{A}$ typ	Digital inputs = 0 V or 3 V
			4.0	$\mu\text{A}$ max	
Inactive, SCLK = 1 MHz	14			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	7			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\ \text{V}$
SCLK = 50 MHz	390			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	210			$\mu\text{A}$ typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\ \text{V}$
Inactive, SDI = 1 MHz	15			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	7.5			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\ \text{V}$
SDI = 25 MHz	230			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\ \text{V}$
	120			$\mu\text{A}$ typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\ \text{V}$
Active at 50 MHz	7.0			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\ \text{V}$
			9.0	mA max	
	3.3			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7\ \text{V}$
			5.0	mA max	

## SPECIFICATIONS

## CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 4. Eight Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx <sup>1</sup>				
$V_{DD} = +15\text{ V}$ , $V_{SS} = -15\text{ V}$ ( $\theta_{JA} = 56.74^\circ\text{C/W}$ )	439	232	112	mA maximum
$V_{DD} = +12\text{ V}$ , $V_{SS} = 0\text{ V}$ ( $\theta_{JA} = 56.74^\circ\text{C/W}$ )	439	232	112	mA maximum

<sup>1</sup> Sx refers to the S1 to S8 pins, and Dx refers to the D1 to D8 pins.

Table 5. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx <sup>1</sup>				
$V_{DD} = +15\text{ V}$ , $V_{SS} = -15\text{ V}$ ( $\theta_{JA} = 56.74^\circ\text{C/W}$ )	768	313	122	mA maximum
$V_{DD} = +12\text{ V}$ , $V_{SS} = 0\text{ V}$ ( $\theta_{JA} = 56.74^\circ\text{C/W}$ )	768	313	122	mA maximum

<sup>1</sup> Sx refers to the S1 to S8 pins, and Dx refers to the D1 to D8 pins.

## SPECIFICATIONS

## TIMING CHARACTERISTICS

$V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , and all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. See [Figure 2](#) to [Figure 4](#) for the timing diagrams.

Table 6. Timing Characteristics

Parameter	Limit	Unit	Test Conditions/Comments
TIMING CHARACTERISTICS			
$t_1$	20	ns min	SCLK period
$t_2$	8	ns min	SCLK high pulse width
$t_3$	8	ns min	SCLK low pulse width
$t_4$	10	ns min	$\overline{CS}$ falling edge to SCLK active edge
$t_5$	6	ns min	Data setup time
$t_6$	8	ns min	Data hold time
$t_7$	10	ns min	SCLK active edge to rising edge
$t_8$	20	ns max	$\overline{CS}$ falling edge to SDO data available
$t_9^1$	30	ns max	SCLK falling edge to SDO data available
$t_{10}$	30	ns max	$\overline{CS}$ rising edge to SDO returns to high
$t_{11}$	20	ns min	$\overline{CS}$ high time between SPI commands
$t_{12}$	8	ns min	$\overline{CS}$ falling edge to SCLK becomes stable
$t_{13}$	8	ns min	$\overline{CS}$ rising edge to SCLK becomes stable

<sup>1</sup> Measured with a 20 pF load.  $t_9$  determines the maximum SCLK frequency when SDO is used.



SPECIFICATIONS

TIMING DIAGRAMS

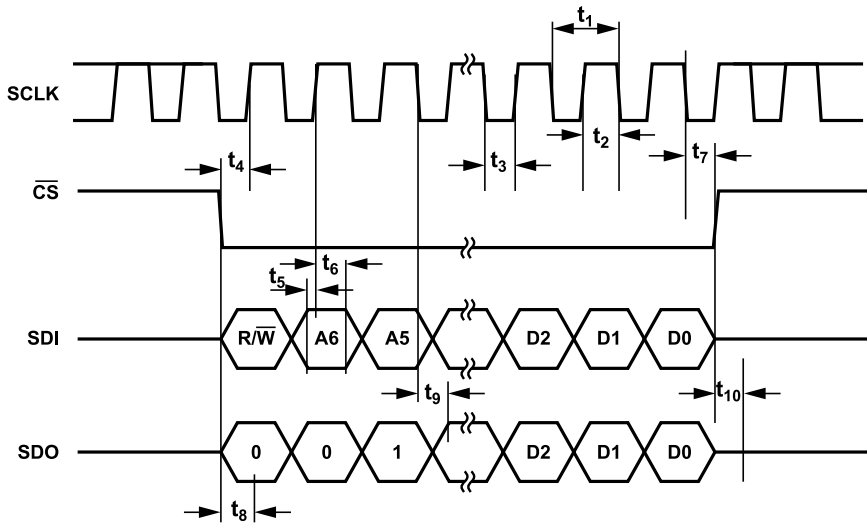


Figure 2. Address Mode Timing Diagram

002

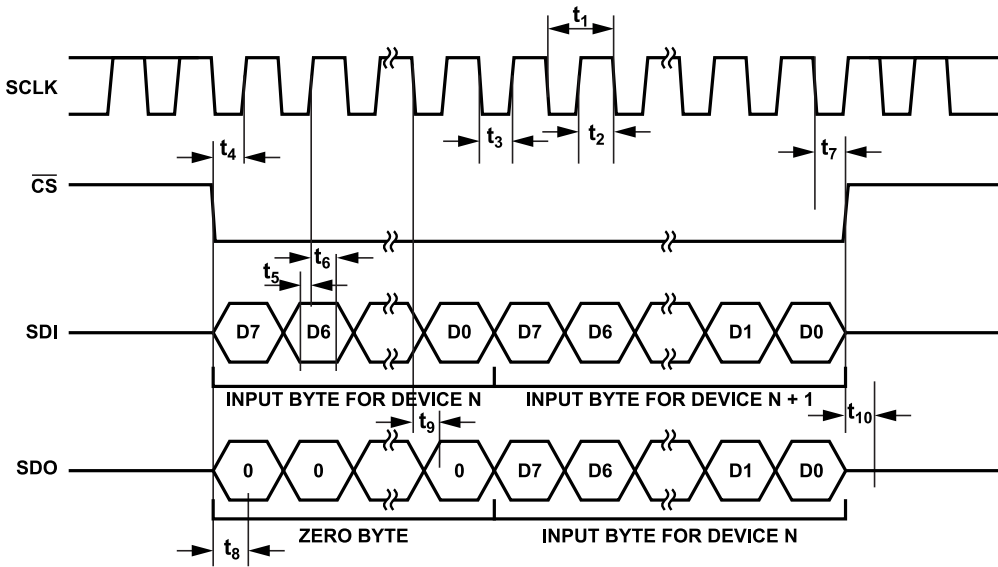


Figure 3. Daisy-Chain Timing Diagram

003

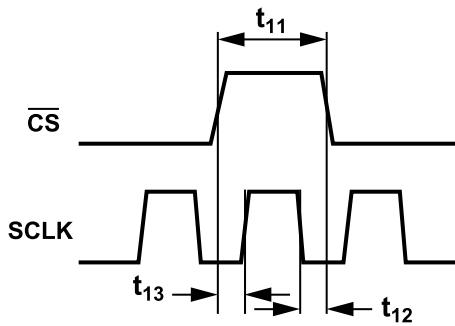


Figure 4. SCLK and CS Timing Relationship

004

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 7. Absolute Maximum Ratings

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
$V_L$ to GND	
For $V_{DD} \leq 5.5$ V	-0.3 V to $V_{DD} + 0.3$ V
For $V_{DD} > 5.5$ V	-0.3 V to +6 V
SDO	-0.3 V to $V_L + 0.3$ V or 6 mA, whichever occurs first
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	-0.3 V to +6 V
Peak Current, Sx or Dx <sup>2</sup>	1180 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx <sup>2</sup>	Data <sup>3</sup> + 15%
Temperature	
Operating Range	-40°C to +125°C
Storage Range	-65°C to +150°C
Junction	150°C
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020

<sup>1</sup> Overvoltages at the digital Sx and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> Sx refers to the S1 to S8 pins, and Dx refers to the D1 to D8 pins.

<sup>3</sup> See Table 4 and Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.  $\theta_{JCB}$  is the junction to the bottom of the case value.

Table 8. Thermal Resistance

Package Type <sup>1</sup>	$\theta_{JA}$	$\theta_{JCB}$	Unit
CC-30-3	56.81	29.82	°C/W

<sup>1</sup> Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD-51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for ADGS2414D

Table 9. ADGS2414D, 30-Terminal LGA

Package Type	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

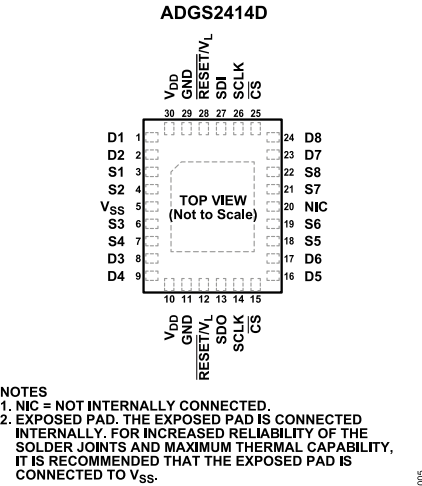
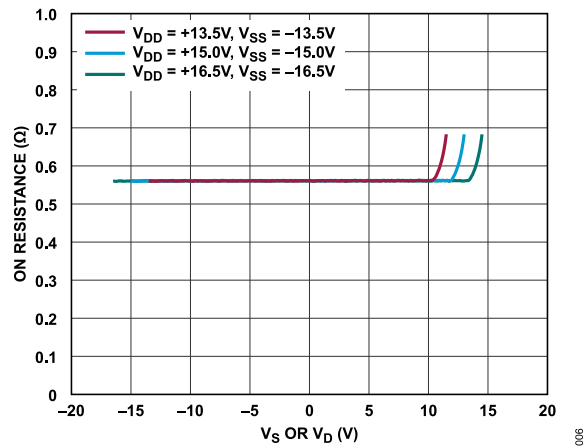
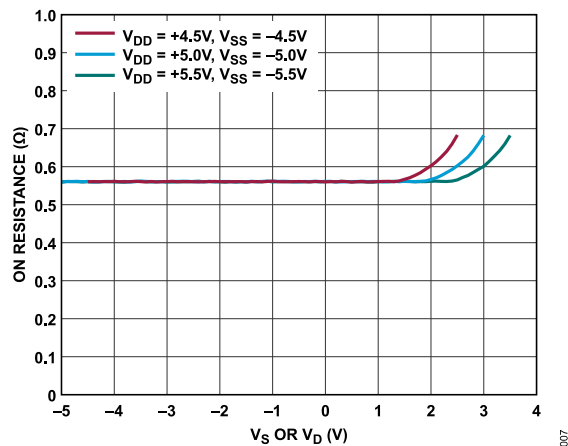
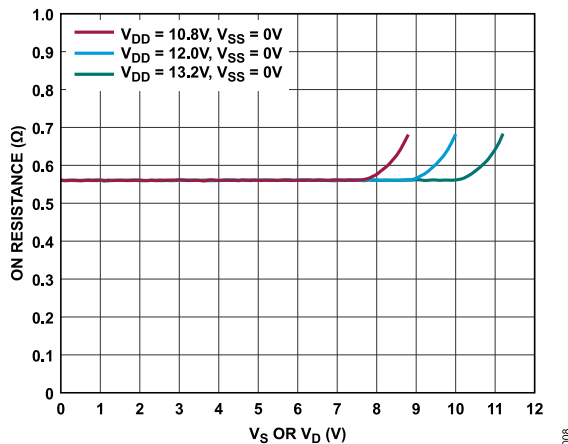
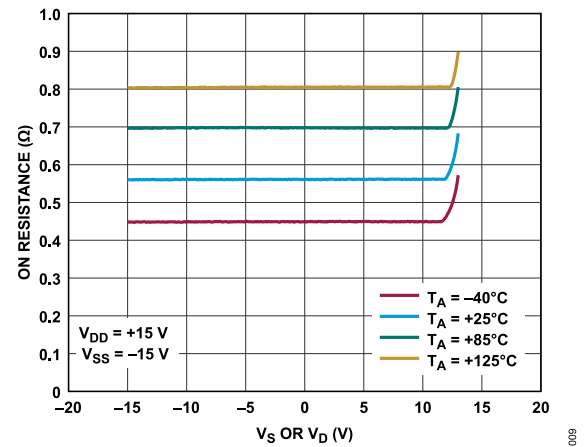
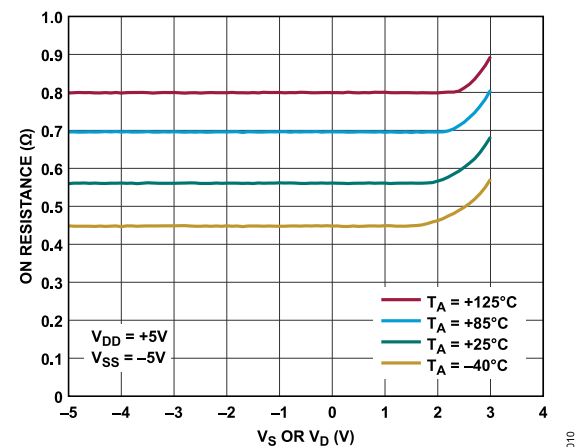
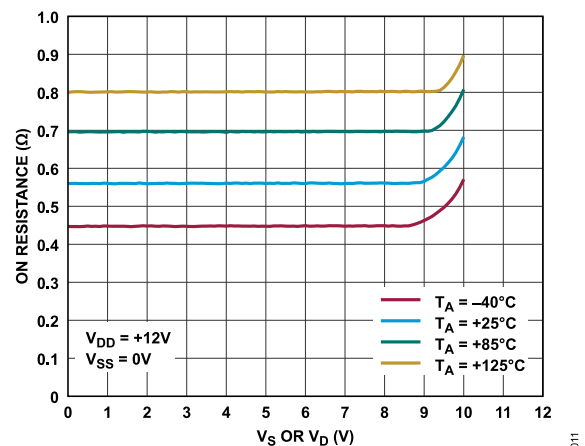


Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal 1. The D1 pin can be an input or an output.
2	D2	Drain Terminal 2. The D2 pin can be an input or an output.
3	S1	Source Terminal 1. The S1 pin can be an input or an output.
4	S2	Source Terminal 2. The S2 pin can be an input or an output.
5	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, tie the V <sub>SS</sub> pin to ground.
6	S3	Source Terminal 3. The S3 pin can be an input or an output.
7	S4	Source Terminal 4. The S4 pin can be an input or an output.
8	D3	Drain Terminal 3. The D3 pin can be an input or an output.
9	D4	Drain Terminal 4. The D4 pin can be an input or an output.
10, 30	V <sub>DD</sub>	Most Positive Power Supply Potential. Both V <sub>DD</sub> pins are connected internally.
11, 29	GND	Ground (0 V) Reference. Both GND pins are connected internally.
12, 28	RESET/V <sub>L</sub>	RESET/Logic Power Supply Input (V <sub>L</sub> ). Under normal operation, drive RESET/V <sub>L</sub> with a 2.7 V to 5.5 V supply. Pull RESET/V <sub>L</sub> low to complete a hardware reset. After a reset, all switches open, and the appropriate registers are set to their default. Both RESET and V <sub>L</sub> are connected internally.
13	SDO	Serial Data Output. Use the SDO pin for daisy-chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK.
14, 26	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data can be transferred at rates up to 50 MHz. Both SCLK pins are connected internally.
15, 25	CS	Active Low Control Input. CS is the frame synchronization signal for the input data. Both CS pins are connected internally.
16	D5	Drain Terminal 5. The D5 pin can be an input or an output.
17	D6	Drain Terminal 6. The D6 pin can be an input or an output.
18	S5	Source Terminal 5. The S5 pin can be an input or an output.
19	S6	Source Terminal 6. The S6 pin can be an input or an output.
20	NIC	Not Internally Connected.
21	S7	Source Terminal 7. The S7 pin can be an input or an output.
22	S8	Source Terminal 8. The S8 pin can be an input or an output.
23	D7	Drain Terminal 7. The D7 pin can be an input or an output.
24	D8	Drain Terminal 8. The D8 pin can be an input or an output.
27	SDI	Serial Data Input. Data is captured on the positive edge of SCLK.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad is connected to V <sub>SS</sub> .

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 6. On Resistance vs.  $V_S$  or  $V_D$  for  $\pm 15$  V Dual SupplyFigure 7. On Resistance vs.  $V_S$  or  $V_D$  for  $\pm 5$  V Dual SupplyFigure 8. On Resistance vs.  $V_S$  or  $V_D$  for +12 V Single SupplyFigure 9. On Resistance vs.  $V_S$  or  $V_D$  for Various Temperatures,  $\pm 15$  V Dual SupplyFigure 10. On Resistance vs.  $V_S$  or  $V_D$  for Various Temperatures,  $\pm 5$  V Dual SupplyFigure 11. On Resistance vs.  $V_S$  or  $V_D$  for Various Temperatures, +12 V Single Supply

## TYPICAL PERFORMANCE CHARACTERISTICS

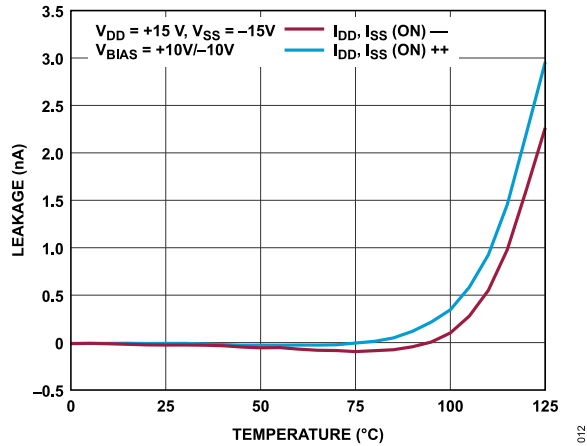


Figure 12. On Leakage Currents vs. Temperature, ±15 V Dual Supply

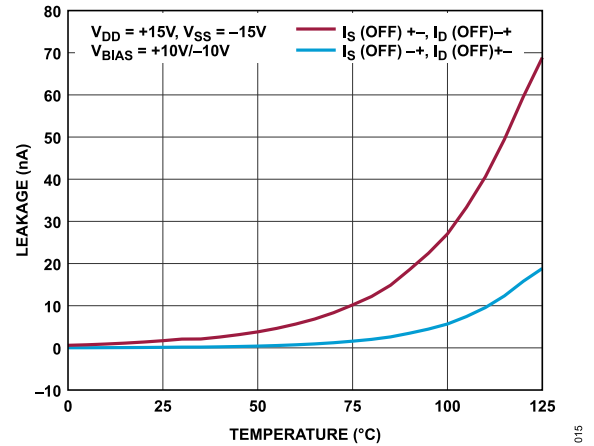


Figure 15. Off Leakage Currents vs. Temperature, ±15 V Dual Supply

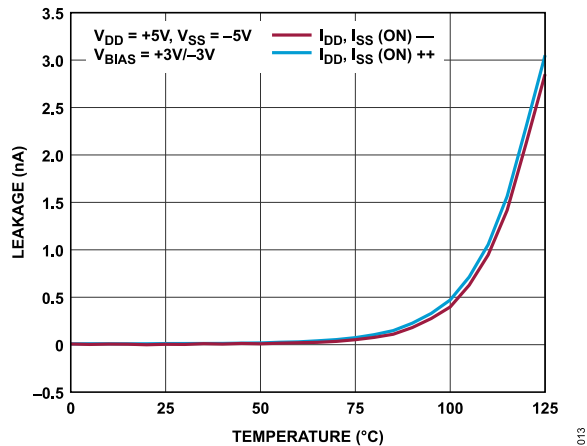


Figure 13. On Leakage Currents vs. Temperature, ±15 V Dual Supply

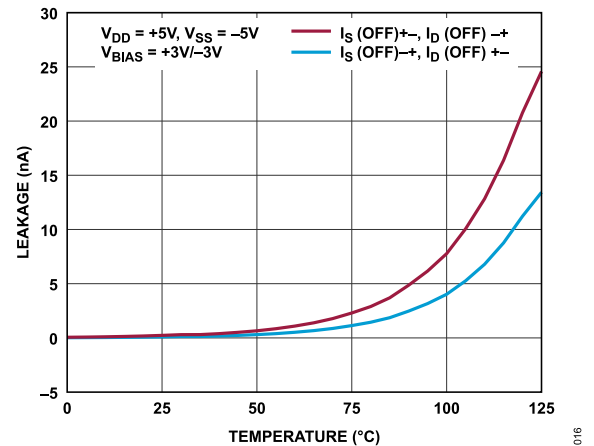


Figure 16. On Leakage Currents vs. Temperature, ±15 V Dual Supply

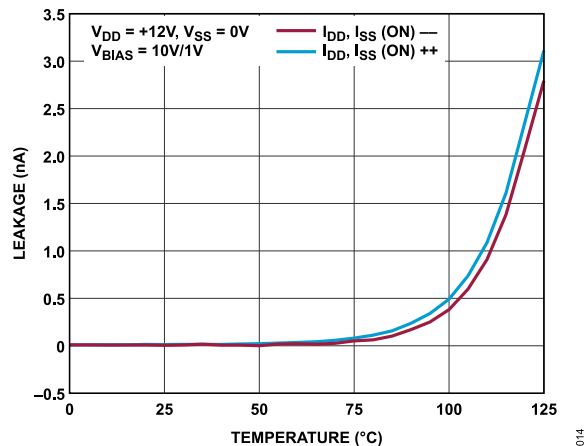


Figure 14. On Leakage Currents vs. Temperature, +12 V Single Supply

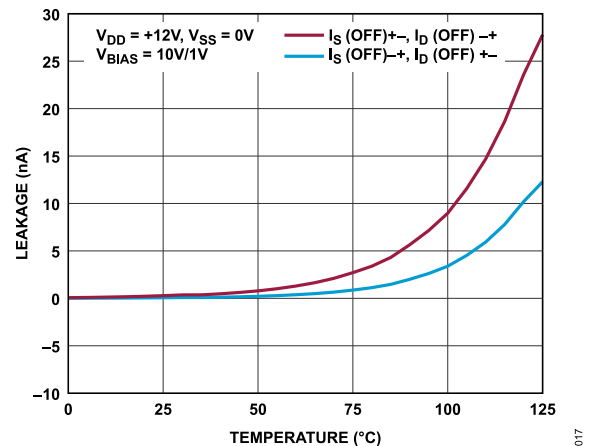
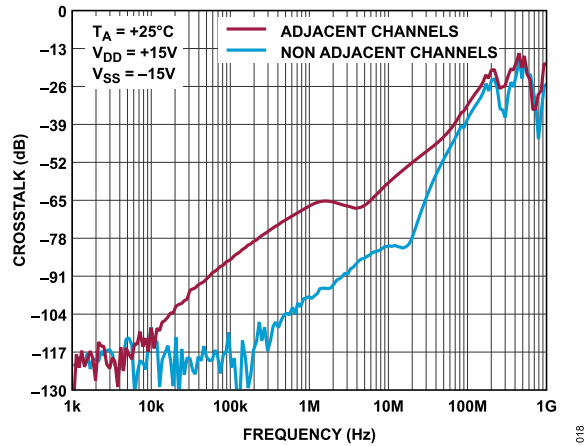
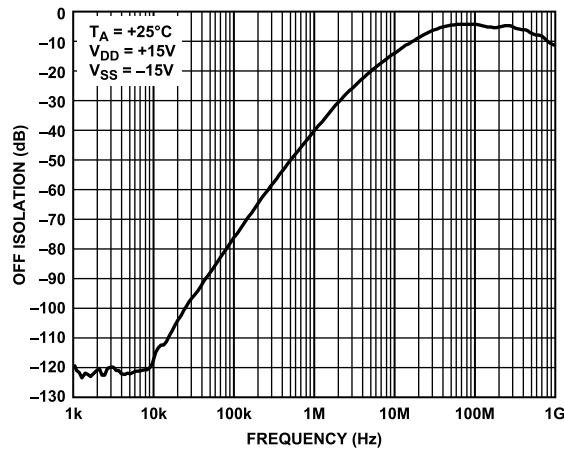
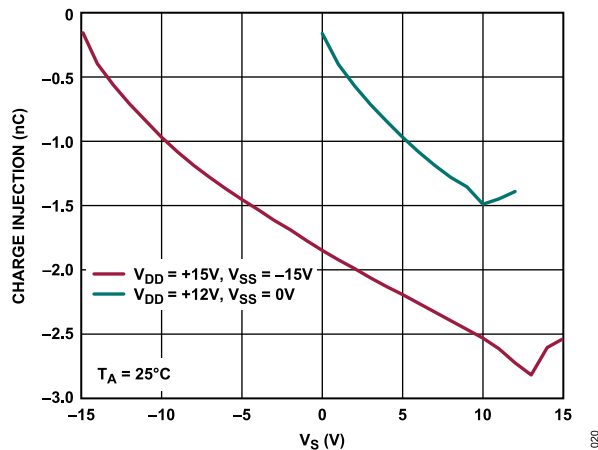
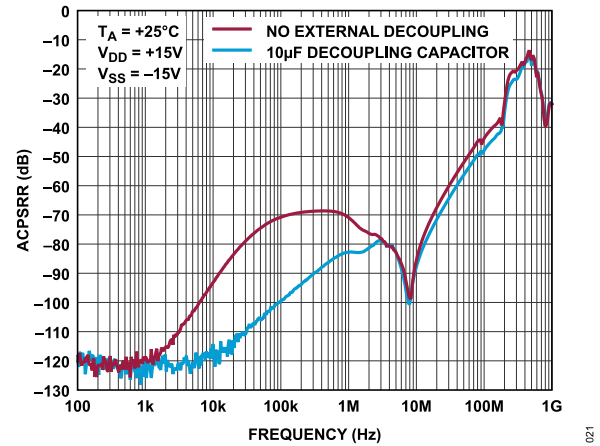
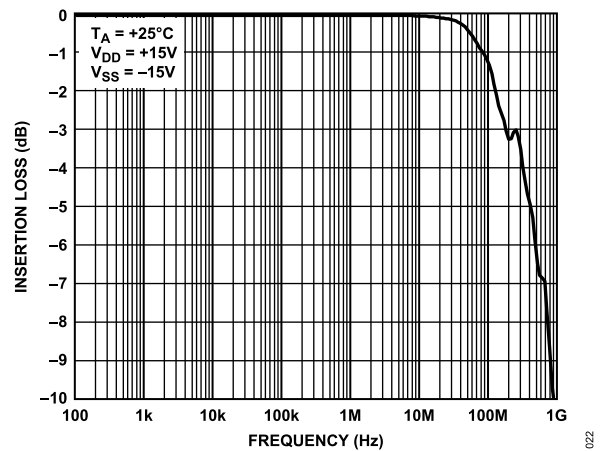
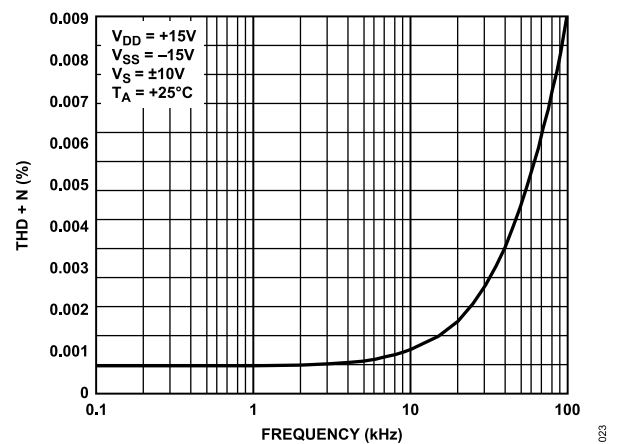


Figure 17. On Leakage Currents vs. Temperature, +12 V Single Supply

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 18. Crosstalk vs. Frequency,  $\pm 15$  V Dual SupplyFigure 19. Off Isolation vs. Frequency,  $\pm 15$  V Dual SupplyFigure 20. Charge Injection vs.  $V_S$ Figure 21. AC Power Supply Rejection Ratio (AC PSRR) vs. Frequency,  $\pm 15$  V Dual SupplyFigure 22. Insertion Loss vs. Frequency,  $\pm 15$  V Dual SupplyFigure 23. THD + N vs. Frequency,  $\pm 15$  V Dual Supply

## TYPICAL PERFORMANCE CHARACTERISTICS

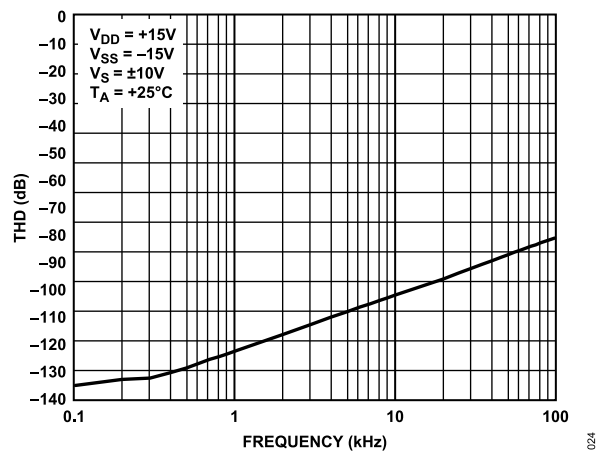


Figure 24. THD vs. Frequency, ±15 V Dual Supply

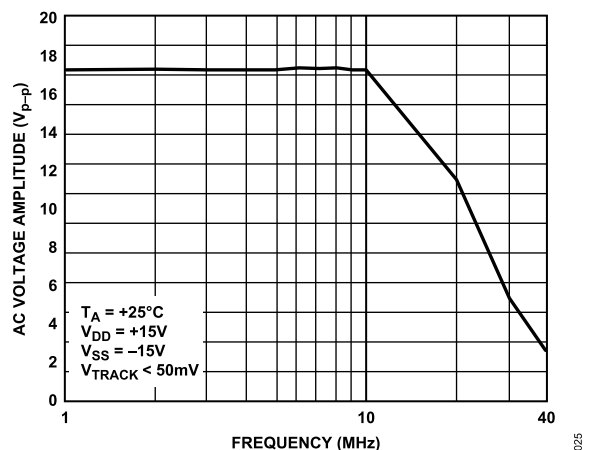
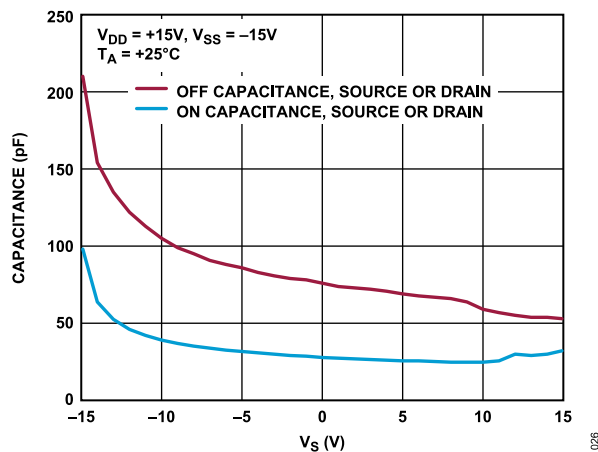
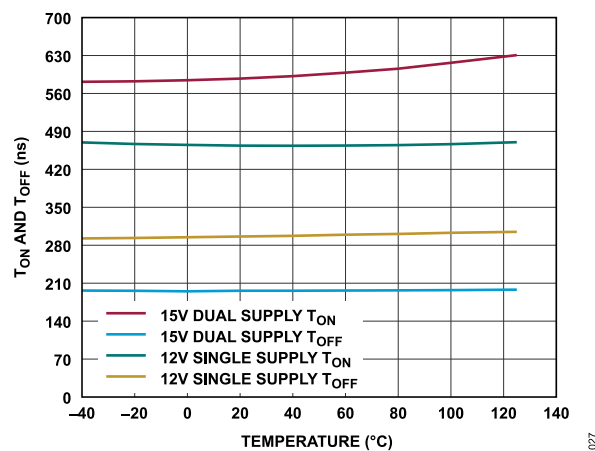
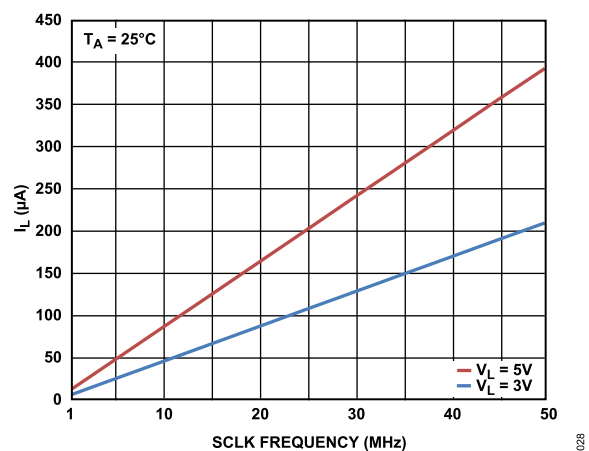


Figure 25. Large AC Signal Voltage vs. Frequency

Figure 26. Capacitance vs.  $V_S$ , ±15 V Dual SupplyFigure 27.  $T_{ON}/T_{OFF}$  Time vs. Temperature for Single Supply (SS) and Dual Supply (DS)Figure 28.  $I_L$  vs. SCLK Frequency When  $\overline{CS}$  Is High

TEST CIRCUITS

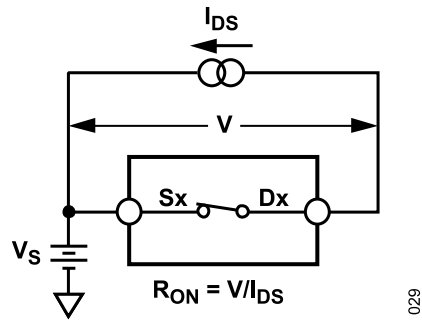


Figure 29. On Resistance ( $I_{DS}$  = Drain and Source Current)

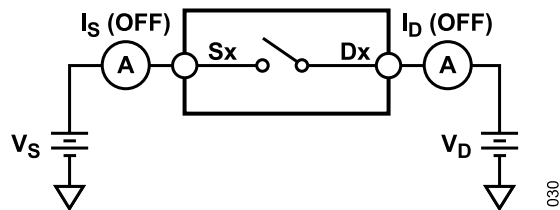


Figure 30. Off Leakage

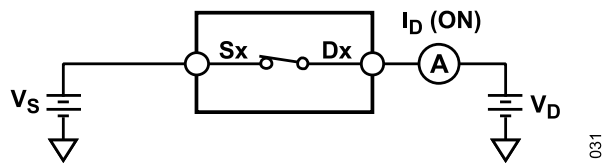


Figure 31. On Leakage

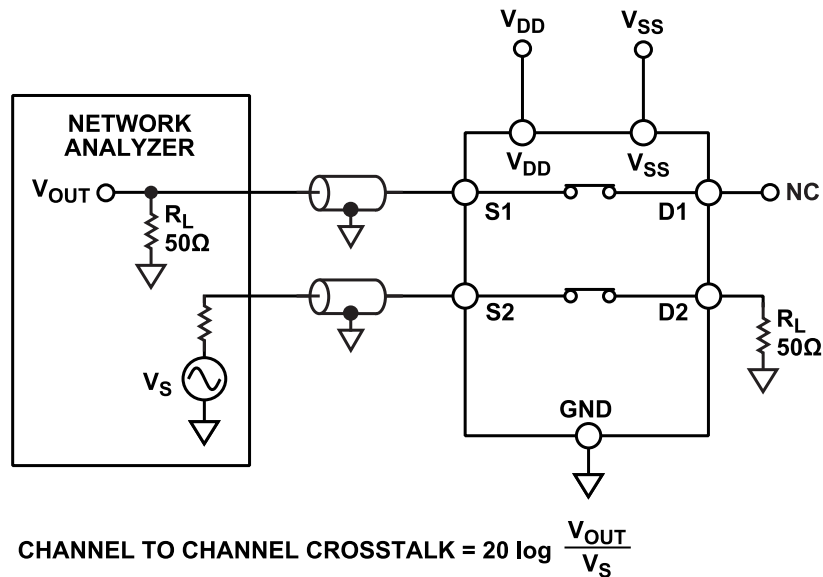
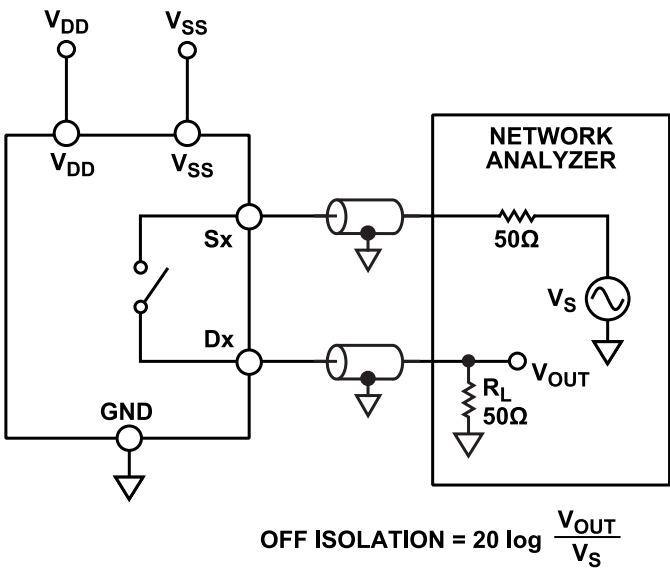


Figure 32. Channel to Channel Crosstalk

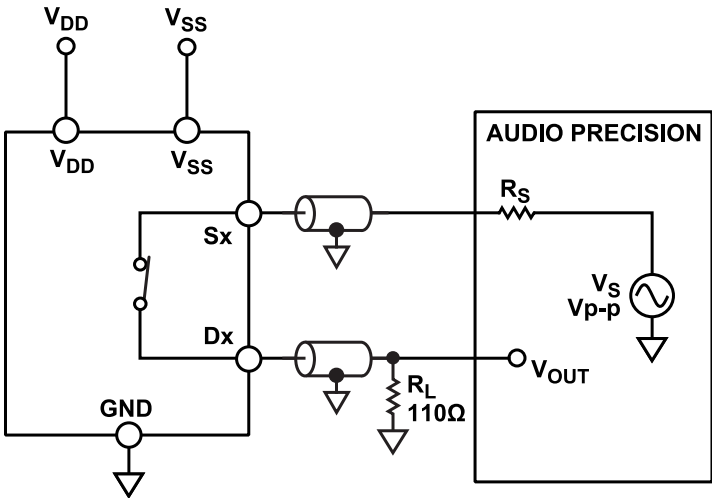


TEST CIRCUITS



033

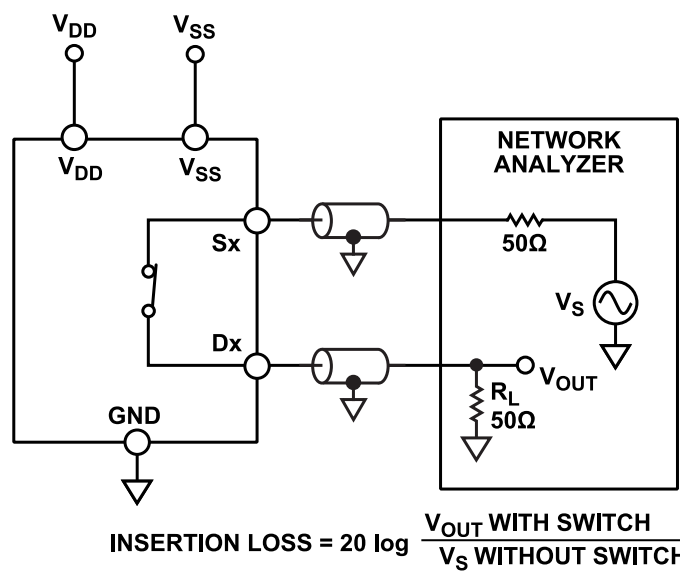
Figure 33. Off Isolation



034

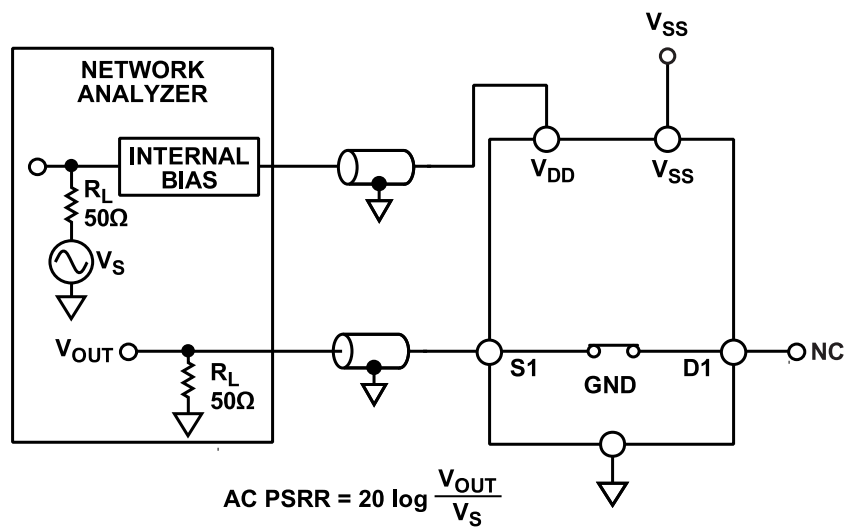
Figure 34. THD + N

## TEST CIRCUITS



035

Figure 35. -3 dB Bandwidth



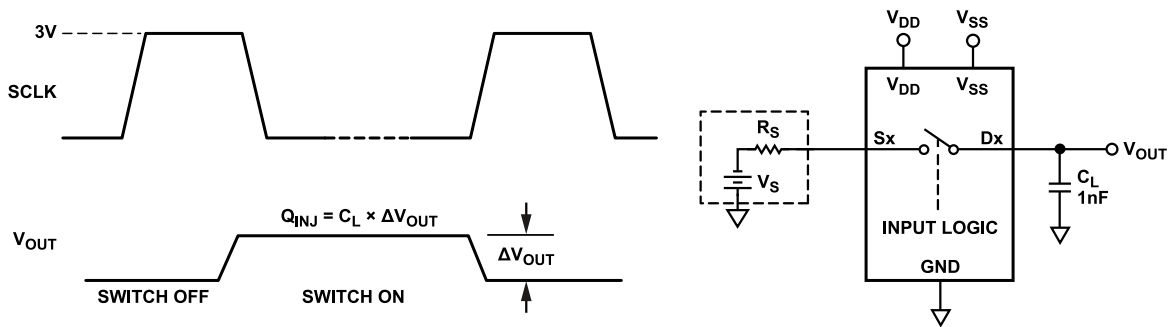
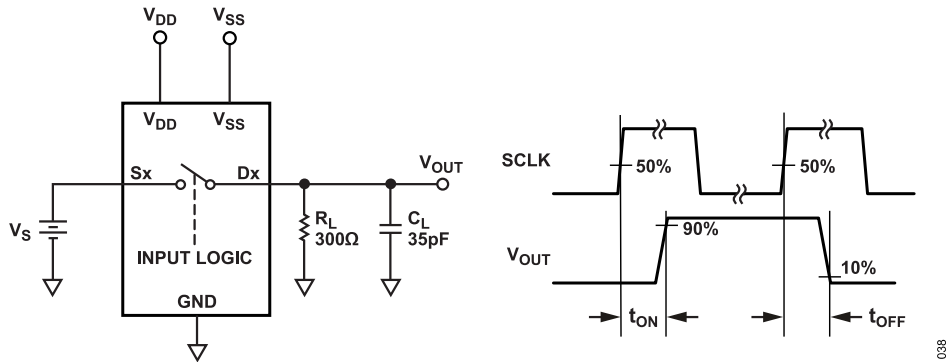
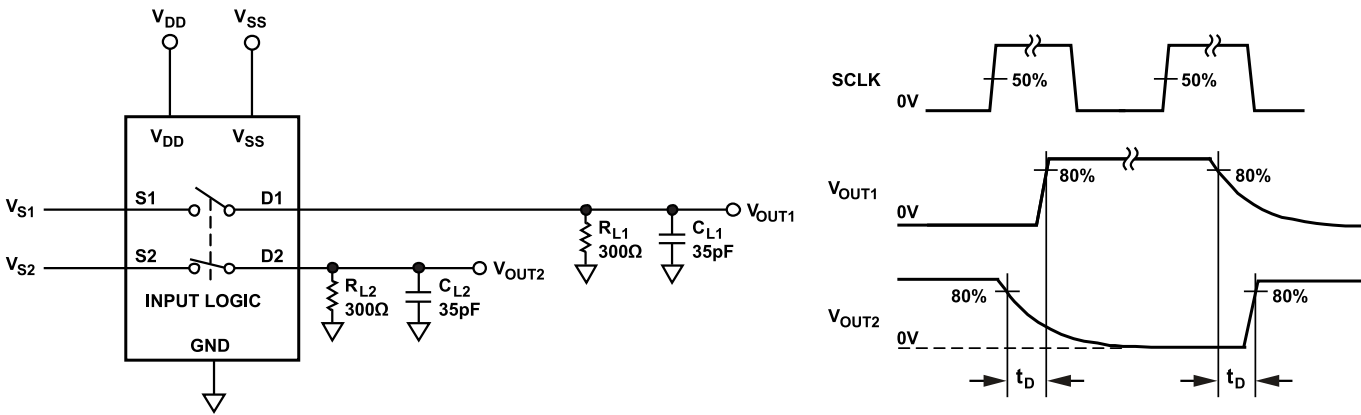
## NOTES

1. BOARD AND COMPONENT EFFECTS ARE NOT DE-EMBEDDED FROM THE AC PSRR MEASUREMENT.

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Figure 36. AC PSRR

TEST CIRCUITS



## TERMINOLOGY

**I<sub>DD</sub>**

I<sub>DD</sub> represents the positive supply current.

**I<sub>SS</sub>**

I<sub>SS</sub> represents the negative supply current.

**V<sub>D</sub>, V<sub>S</sub>**

V<sub>D</sub> and V<sub>S</sub> represent the analog voltage on Terminal Dx and Terminal Sx, respectively.

**R<sub>ON</sub>**

R<sub>ON</sub> represents the ohmic resistance between Terminal Dx and Terminal Sx.

**ΔR<sub>ON</sub>**

ΔR<sub>ON</sub> represents the difference between the R<sub>ON</sub> of any two channels.

**R<sub>FLAT (ON)</sub>**

R<sub>FLAT (ON)</sub> is flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

**I<sub>S</sub> (Off)**

I<sub>S</sub> (Off) is the source leakage current with the switch off.

**I<sub>D</sub> (Off)**

I<sub>D</sub> (Off) is the drain leakage current with the switch off.

**I<sub>D</sub> (On), I<sub>S</sub> (On)**

I<sub>D</sub> (On) and I<sub>S</sub> (On) represent the channel leakage currents with the switch on.

**V<sub>INL</sub>**

V<sub>INL</sub> is the maximum input voltage for Logic 0.

**V<sub>INH</sub>**

V<sub>INH</sub> is the minimum input voltage for Logic 1.

**I<sub>INL</sub>, I<sub>INH</sub>**

I<sub>INL</sub> and I<sub>INH</sub> represent the low and high input currents of the digital inputs.

**C<sub>D</sub> (Off)**

C<sub>D</sub> (Off) represents the off switch drain capacitance, which is measured with reference to ground.

**C<sub>S</sub> (Off)**

C<sub>S</sub> (Off) represents the off switch source capacitance, which is measured with reference to ground.

**C<sub>D</sub> (On), C<sub>S</sub> (On)**

C<sub>D</sub> (On) and C<sub>S</sub> (On) represent on switch capacitances, which are measured with reference to ground.

**C<sub>IN</sub>**

C<sub>IN</sub> is the digital input capacitance.

**C<sub>OUT</sub>**

C<sub>OUT</sub> is the digital output capacitance.

**t<sub>ON</sub>**

t<sub>ON</sub> represents the delay between applying the digital control input and the output switching on.

**t<sub>OFF</sub>**

t<sub>OFF</sub> represents the delay between applying the digital control input and the output switching off.

**Off Isolation**

Off isolation is a measure of unwanted signal coupling through an off switch.

**Charge Injection**

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Crosstalk**

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**–3 dB Bandwidth**

Bandwidth is the frequency at which the output is attenuated by 3 dB.

**On Response**

On response is the frequency response of the on switch.

**Insertion Loss**

Insertion loss is the loss due to the on resistance of the switch.

**Total Harmonic Distortion + Noise (THD + N)**

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

**AC Power Supply Rejection Ratio (AC PSRR)**

AC PSRR is the ratio of the amplitude of the signal on the output to the amplitude of the modulation. AC PSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADGS2414D is a set of serially controlled, octal SPST switches with error detection features. SPI Mode 0 and Mode 3 can be used with the ADGS2414D, and the device operates with SCLK frequencies up to 50 MHz. The default mode for the ADGS2414D is address mode in which the registers of the device are accessed by a 16-bit SPI command that is bounded by  $\overline{CS}$ . The SPI command is a 24-bit command if the user enables CRC error detection. Other error detection features include SCLK count error and invalid read and write error. Read the error flags register to detect if any of these SPI errors occur. The ADGS2414D can also operate in two other modes: burst mode and daisy-chain mode.

The interface pins of the ADGS2414D are  $\overline{CS}$ , SCLK, SDI, and SDO. Hold  $\overline{CS}$  low when using the SPI. Data is captured on the SDI on the rising edge of SCLK, and data is propagated out on the SDO on the falling edge of SCLK.

ADDRESS MODE

Address mode is the default mode for the ADGS2414D upon power-up. A single SPI frame in address mode is bounded by a  $\overline{CS}$  falling edge and the succeeding  $\overline{CS}$  rising edge. The SPI frame is comprised of 16 SCLK cycles. The timing diagram for address mode is shown in Figure 40. The first SDI bit indicates if the SPI command is a read or write command. When the first bit is set to 0, a write command is issued, and if the first bit is set to 1, a read command is issued. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command because, during these clock cycles, SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the eighth to the 15<sup>th</sup> SCLK falling edge during SPI reads. A register write occurs on the 16<sup>th</sup> SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits as the first eight bits. The alignment bits observed at SDO are 0x25.

ERROR DETECTION FEATURES

Protocol and communication errors on the SPI are detectable. There are three error detection features: incorrect SCLK count error detection, invalid read and write address error detection, and CRC error detection. Each of these error detection features has a corresponding enable bit in the error configuration register. In addition, there is an error flag bit for each of these error detection features in the error flags register.

CYCLIC REDUNDANCY CHECK (CRC) ERROR DETECTION

The CRC error detection feature extends a valid SPI frame by eight SCLK cycles. These eight extra cycles are needed to send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: the R/W bit, the register address, Bits[6:0], and the register data, Bits[7:0]. The CRC polynomial used in the SPI block is  $x^8 + x^2 + x^1 + 1$  with a seed value of 0. For a timing diagram with CRC enabled, see Figure 41. Register writes occur at the 24<sup>th</sup> SCLK rising edge with CRC error checking enabled.

During an SPI write, the microcontroller or central processing unit (CPU) provides the CRC byte through SDI. The SPI block checks the CRC byte just before the 24th SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI. The CRC error flag asserts in the error flags register in the case of the incorrect CRC byte being detected.

During an SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC error detection feature is disabled by default and can be configured by the user through the error configuration register.

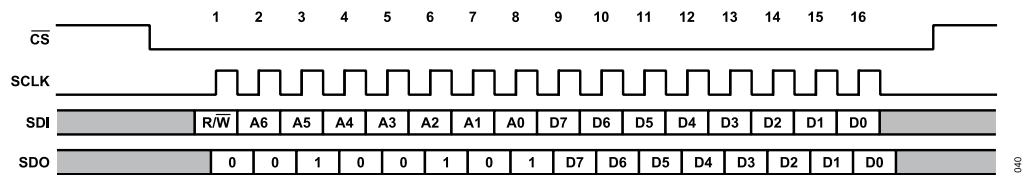


Figure 40. Address Mode Timing Diagram

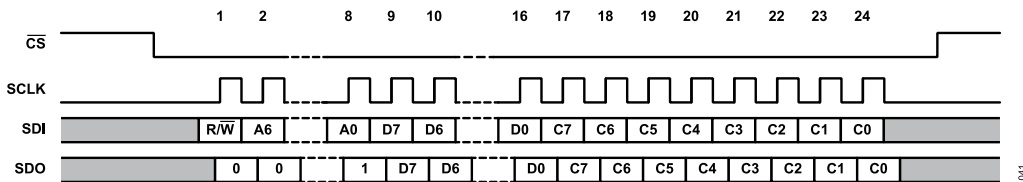


Figure 41. Timing Diagram with CRC Enabled

## THEORY OF OPERATION

### SCLK COUNT ERROR DETECTION

SCLK count error detection allows the user to detect if an incorrect number of SCLK cycles are sent by the microcontroller or CPU. When in address mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected, the SCLK count error flag asserts in the error flags register. When less than 16 SCLK cycles are received by the device, a write to the register map does not occur. When the ADGS2414D receives more than 16 SCLK cycles, a write to the memory map still occurs at the 16<sup>th</sup> SCLK rising edge, and the flag asserts in the error flags register. With CRC enabled, the expected number of SCLK cycles is 24. SCLK count error detection is enabled by default and can be configured by the user through the error configuration register.

### INVALID READ AND WRITE ADDRESS ERROR

An invalid read and write address error detects when a nonexistent register address is a target for a read or write. In addition, this error asserts when a write to a read only register is attempted. The invalid read and write address error flag asserts in the error flags register when an invalid read and write address error occurs. The invalid read and write address error is detected on the ninth SCLK rising edge, which means a write to the register does not occur when an invalid address is targeted. Invalid read and write address error detection is enabled by default and can be disabled by the user through the error configuration register.

### CLEARING THE ERROR FLAGS REGISTER

To clear the error flags register, write the special 16-bit SPI frame, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must also send the correct CRC byte for a successful error clear command. At the 16<sup>th</sup> or 24<sup>th</sup> SCLK rising edge, the error flags register resets to zero.

### BURST MODE

The SPI can accept consecutive SPI commands without the need to deassert the  $\overline{CS}$  line, which is called burst mode. Burst mode is enabled through the burst enable register. This mode uses the same 16-bit command to communicate with the device. In addition, the response of the device at SDO is still aligned with the corresponding SPI command. Figure 42 shows an example of SDI and SDO during burst mode.

The invalid read and write address and CRC error checking functions operate similarly during burst mode as these error checking functions do during address mode. However, SCLK count error

detection operates in a slightly different manner. The total number of SCLK cycles within a given  $\overline{CS}$  frame are counted, and if the total is not a multiple of 16, or a multiple of 24 when CRC is enabled, the SCLK count error flag asserts.

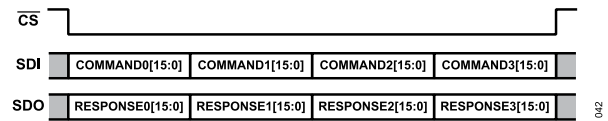


Figure 42. Burst Mode Frame

### SOFTWARE RESET

When in address mode, the user can initiate a software reset by writing two consecutive SPI commands, 0xA3 followed by 0x05, targeting Register 0x0B. After a software reset, all register values are set to default.

### DAISY-CHAIN MODE

The connection of several ADGS2414D devices in a daisy-chain configuration is possible, and Figure 43 illustrates this setup. All devices share the same  $\overline{CS}$ , SCLK, and  $V_L$  line, whereas the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In daisy-chain mode, SDO is an eight-cycle delayed version of SDI. When in daisy-chain mode, all commands target the switch data register. Therefore, it is not possible to make configuration changes while in daisy-chain mode.

When in address mode, the ADGS2414D can only enter daisy-chain mode by sending the 16-bit SPI command, 0x2500 (see Figure 44). When the ADGS2414D receives this command, the SDO of the device sends out the same command because the alignment bits at the SDO are 0x25, which allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 45. When  $\overline{CS}$  goes high, Device 1 writes Command 0, Bits[7:0] to its switch data register, Device 2 writes Command 1, Bits[7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering daisy-chain mode, the first eight bits sent out by SDO on each device in the chain are 0x00. When  $\overline{CS}$  goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads data on SDI while data is propagated out of SDO on an SCLK falling edge.

THEORY OF OPERATION

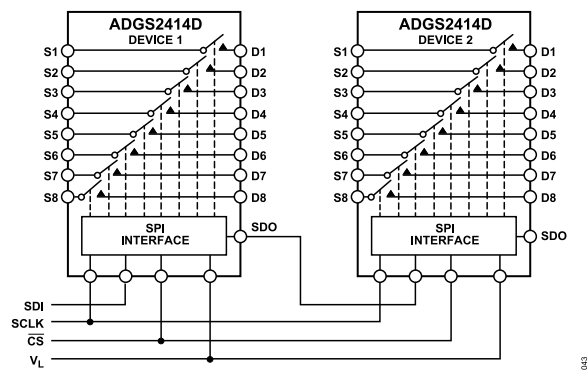


Figure 43. Two ADGS2414D Devices Connected in a Daisy-Chain Configuration

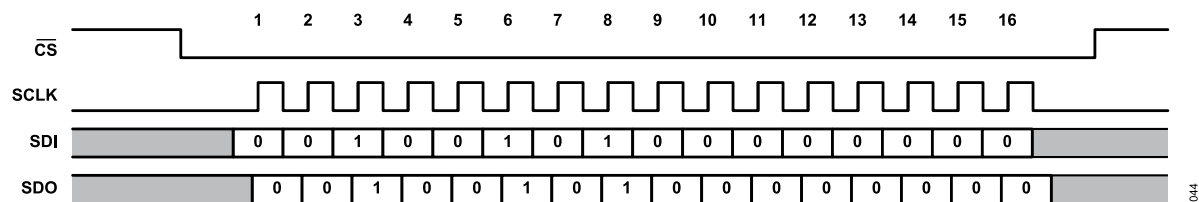
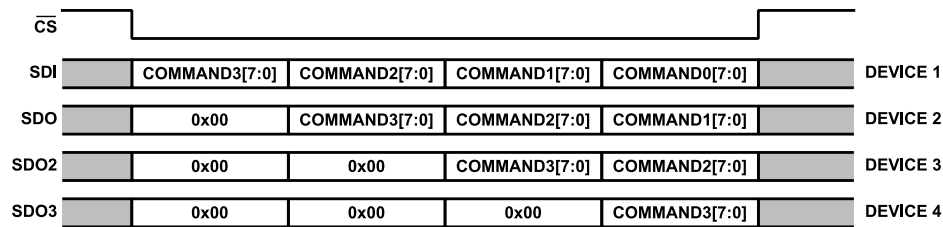


Figure 44. SPI Command to Enter Daisy-Chain Mode



NOTES  
1. SDO2 AND SDO3 ARE THE OUTPUT COMMANDS FROM DEVICE 2 AND DEVICE 3, RESPECTIVELY.

Figure 45. Example of an SPI Frame Where Four ADGS2414D Devices Connect in Daisy-Chain Mode

## THEORY OF OPERATION

### POWER-ON RESET

The digital section of the ADGS2414D goes through an initialization phase during  $V_L$  power-up. This initialization also occurs after a hardware or software reset. After  $V_L$  power-up or a reset, ensure that a minimum of 120  $\mu$ s passes from the time of power-up or reset before any SPI command is issued. Ensure that  $V_L$  does not drop out during the 120  $\mu$ s initialization phase because it may result in the incorrect operation of the ADGS2414D.



## APPLICATIONS INFORMATION

### LARGE VOLTAGE, HIGH FREQUENCY SIGNAL TRACKING

Figure 25 shows the voltage range and corresponding frequencies that the ADGS2414D can reliably convey. The tracking voltage ( $V_{\text{TRACK}}$ ) in the figure shows the source voltage and the drain voltage difference, which is less than 50 mV for a given amplitude and frequency. For large voltage, high frequency signals, the frequency must be kept below 10 MHz. If the required frequency is greater than 10 MHz, decrease the signal range appropriately to ensure signal integrity.

### SYSTEM CHANNEL DENSITY

The ADGS2414D feature set allows for large system channel density. These features include route through pins for the digital signals and power supplies, as well as integrated passive components.

### ROUTE THROUGH PINS

When multiple ADGS2414D devices are used in a system, the route through pins allow for a greater channel density layout. The

route through pins enable the passing of power supplies and digital lines between devices with ease. The  $V_{\text{DD}}$ ,  $\overline{\text{RESET}}/V_{\text{L}}$ , and GND power lines, as well as the SCLK,  $\overline{\text{CS}}$ , SDI, and SDO digital lines, are available on both the top and bottom pins of the package.

These route through pins simplify PCB routing and reduce the need for vias when connecting many ADGS2414D devices together.

Figure 46 shows an example layout where the route through pins on four ADGS2414D devices configured in daisy-chain mode are used to reduce the overall size of the layout.

### INTEGRATED PASSIVE COMPONENTS

Note the lack of external passive components in the layout in Figure 46. The ADGS2414D has integrated decoupling capacitors for the  $V_{\text{DD}}$ ,  $V_{\text{SS}}$ , and  $\overline{\text{RESET}}/V_{\text{L}}$  power supplies. Therefore, the need for external decoupling capacitors is eliminated, reducing the total system footprint of the ADGS2414D. If additional decoupling is required for extremely noise-sensitive applications, add an external decoupling capacitor. Figure 21 shows the AC PSRR performance with and without external decoupling capacitors. The ADGS2414D also contains an integrated pullup resistor to  $V_{\text{L}}$  for the SDO pin.

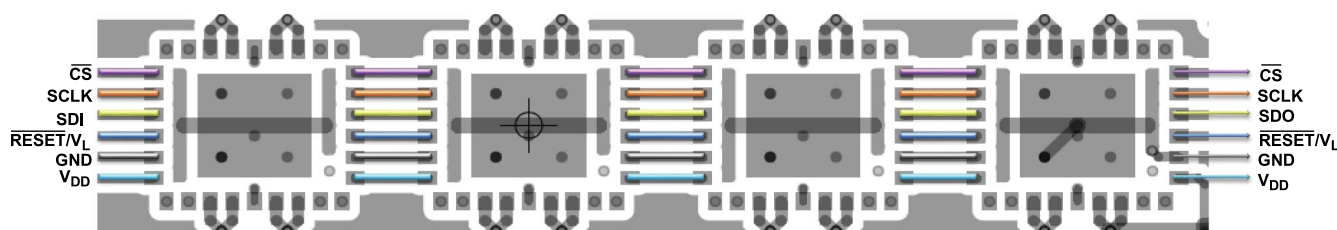


Figure 46. Layout Example Showing the Use of the Route Pins and the Elimination of External Passive Components

## APPLICATIONS INFORMATION

## BREAK-BEFORE-MAKE SWITCHING

The ADGS2414D exhibits break-before-make switching action. This feature allows for the use of the device in multiplexer applications. To use the device as a multiplexer, externally hardware a device into the desired mux configuration, as shown in Figure 47.

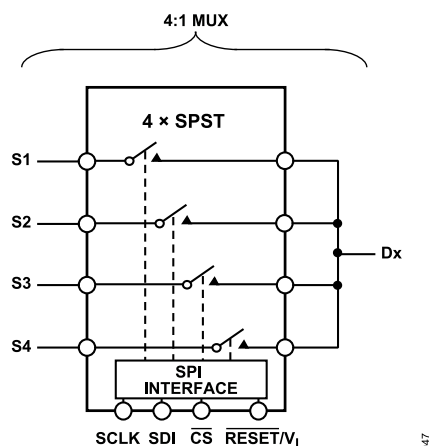


Figure 47. An SPI Controlled Switch Configured into a 4:1 Mux

## DIGITAL INPUT BUFFERS

There are input buffers present on the digital input pins ( $\overline{CS}$ , SCLK, and SDI). These buffers are active at all times. Therefore, there is a current draw from the  $V_L$  supply if SCLK or SDI is toggled, regardless of whether  $\overline{CS}$  is active. For typical values of this current draw, refer to the Specifications section and Figure 28.

## POWER SUPPLY RAILS

The ADGS2414D can operate with bipolar supplies between  $\pm 4.5$  V and  $\pm 16.5$  V. The supplies on  $V_{DD}$  and  $V_{SS}$  do not have to be symmetrical. However, the  $V_{DD}$  to  $V_{SS}$  range must not exceed 33 V. The ADGS2414D can also operate with single supplies between 5 V and 20 V with  $V_{SS}$  connected to GND. The voltage range that can be supplied to  $V_L$  is from 2.7 V to 5.5 V. The device is fully specified at  $\pm 15$  V and +12 V analog supply voltage ranges.

## POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of high-performance signal chains.

An example of a bipolar power solution is shown in Figure 48. The LT3463 (a dual switching regulator) generates a positive and negative supply rail for the ADGS2414D, an amplifier, and/or a precision converter in a typical signal chain. Also shown in Figure 48 are two optional low dropout regulators (LDOs), the ADP7142 and ADP7182 (positive and negative LDOs, respectively), which can reduce the output ripple of the LT3463 in ultralow noise-sensitive applications.

The ADP7142 can generate the  $V_L$  voltage that is required to power the digital circuitry within the ADGS2414D.

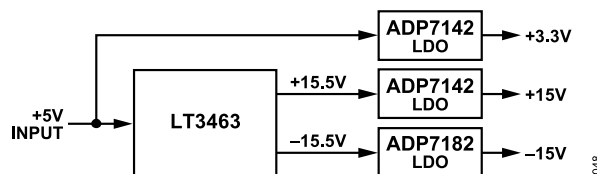


Figure 48. Bipolar Power Solution

Table 11. Recommended Power Management Devices

Product	Description
LT3463	Dual micropower, DC to DC converter with Schottky diodes
ADP7142	40 V, 200 mA, low noise, CMOS, LDO linear regulator
ADP7182	-28 V, -200 mA, low noise, LDO linear regulator

## 1.8 V LOGIC COMPATIBILITY

The SDI,  $\overline{CS}$ , and SCLK digital inputs of the ADGS2414D are compatible with 1.8 V logic when  $V_L$  is between or equal to 2.7 V and 3.3 V.

The SDO digital output levels are proportional to the  $V_L$  voltage. For example, if  $V_L = 3$  V, a logic high on the SDO is approximately 3 V. When performing an SPI readback from the ADGS2414D with a controller device using 1.8 V logic, there may be an issue if the digital pins on the controller cannot tolerate digital input signals that exceed 1.8 V.

Figure 49 describes how to use the ADG3231 level translator to perform a 1.8 V SPI readback with a device that has 1.8 V logic ports, such as a microcontroller or field programmable gate array (FPGA). Place the ADG3231 between the SDO of the ADGS2414D and the microcontroller or FPGA. Supply  $V_{CC1}$  of the ADG3231 with the  $V_L$  voltage of the ADGS2414D and connect  $V_{CC2}$  to the 1.8 V supply from the microcontroller or FPGA. The ADG3231 then translates the logic level of the SDO from  $V_L$  to 1.8 V.

This solution is only required if the 1.8 V microcontroller or FPGA cannot tolerate digital input signals that exceed 1.8 V.

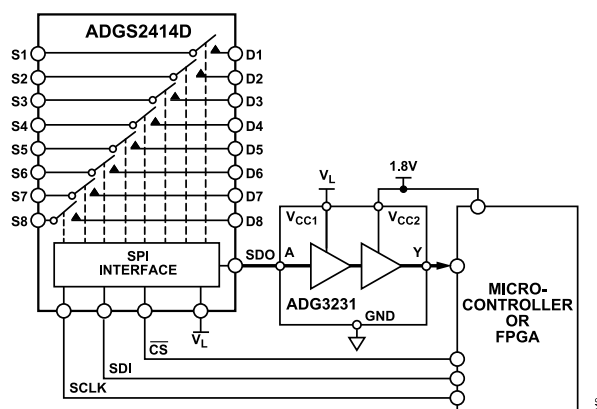


Figure 49. Using the ADG3231 to Perform a 1.8 V SPI Readback

## REGISTER SUMMARY

Table 12. Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/ $\bar{W}$
0x01	SW_DATA	SW8_EN	SW7_EN	SW6_EN	SW5_EN	SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/ $\bar{W}$
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/ $\bar{W}$
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/ $\bar{W}$
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	$\bar{W}$

## REGISTER DETAILS

## SWITCH DATA REGISTER

Address: 0x01, Reset: 0x00, Name: SW\_DATA

Use the switch data register to control the status of the eight switches of the ADGS2414D.

Table 13. Bit Descriptions for SW\_DATA

Bit	Bit Name	Setting	Description	Default	Access
7	SW8_EN		Enable the SW8_EN bit for Switch 8. 0 Switch 8 open. 1 Switch 8 closed.	0x0	R/W
6	SW7_EN		Enable the SW7_EN bit for Switch 7. 0 Switch 7 open. 1 Switch 7 closed.	0x0	R/W
5	SW6_EN		Enable the SW6_EN bit for Switch 6. 0 Switch 6 open. 1 Switch 6 closed.	0x0	R/W
4	SW5_EN		Enable the SW5_EN bit for Switch 5. 0 Switch 5 open. 1 Switch 5 closed.	0x0	R/W
3	SW4_EN		Enable the SW4_EN bit for Switch 4. 0 Switch 4 open. 1 Switch 4 closed.	0x0	R/W
2	SW3_EN		Enable the SW3_EN bit for Switch 3. 0 Switch 3 open. 1 Switch 3 closed.	0x0	R/W
1	SW2_EN		Enable the SW2_EN bit for Switch 2. 0 Switch 2 open. 1 Switch 2 closed.	0x0	R/W
0	SW1_EN		Enable the SW1_EN bit for Switch 1. 0 Switch 1 open. 1 Switch 1 closed.	0x0	R/W

## ERROR CONFIGURATION REGISTER

Address: 0x02, Reset: 0x06, Name: ERR\_CONFIG

Use the error configuration register to enable and disable the relevant error features as required.

Table 14. Bit Descriptions for ERR\_CONFIG

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		Bits[7:3] are reserved. Set Bits[7:3] to 0.	0x0	R
2	RW_ERR_EN	0 1	Enable the RW_ERR_EN bit to detect an invalid read and write address. Disabled. Enabled.	0x1	R/W
1	SCLK_ERR_EN	0 1	Enable the SCLK_ERR_EN bit to detect the correct number of SCLK cycles in an SPI frame. 16 SCLK cycles are expected when CRC is disabled and burst mode is disabled. 24 SCLK cycles are expected when CRC is enabled and burst mode is disabled. A multiple of 16 SCLK cycles is expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles is expected when CRC is enabled and burst mode is enabled. Disabled. Enabled.	0x1	R/W

## REGISTER DETAILS

Table 14. Bit Descriptions for ERR\_CONFIG (Continued)

Bits	Bit Name	Settings	Description	Default	Access
0	CRC_ERR_EN	0 1	Enable the CRC_ERR_EN bit for CRC error detection. SPI frames are 24 bits wide when enabled. Disabled. Enabled.	0x0	R/W

## ERROR FLAGS REGISTER

Address: 0x03, Reset: 0x00, Name: ERR\_FLAGS

Use the error flags register to determine if an error has occurred. To clear the error flags register, write the special 16-bit SPI command, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, include the correct CRC byte during the SPI write for the clear error flags register command to succeed.

Table 15. Bit Descriptions for ERR\_FLAGS

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		Bits[7:3] are reserved and are set to 0.	0x0	R
2	RW_ERR_FLAG	0 1	Error flag for invalid read and write address. The error flag asserts during an SPI read if the target address does not exist. The error flag also asserts when the target address of an SPI write does not exist or is read only. No error. Error.	0x0	R
1	SCLK_ERR_FLAG	0 1	Error flag for the detection of the correct number of SCLK cycles in an SPI frame. No error. Error.	0x0	R
0	CRC_ERR_FLAG	0 1	Error flag that determines if a CRC error has occurred during a register write. No error. Error.	0x0	R

## BURST ENABLE REGISTER

Address: 0x05, Reset: 0x00, Name: BURST\_EN

Use the burst enable register to enable or disable burst mode. When burst mode is enabled, the user can send multiple consecutive SPI commands without deasserting  $\overline{CS}$ .

Table 16. Bit Descriptions for BURST\_EN

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		Bits[7:1] are reserved. Set Bits[7:1] to 0.	0x0	R
0	BURST_MODE_EN	0 1	Burst mode enable bit. Disabled. Enabled.	0x0	R/W

## REGISTER DETAILS

## SOFTWARE RESET REGISTER

**Address: 0x0B, Reset: 0x00, Name: SOFT\_RESETB**

Use the software reset register to perform a software reset. Consecutively write 0xA3 followed by 0x05 to this register, and the registers of the device reset to their default state.

*Table 17. Bit Descriptions for SOFT\_RESETB*

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To perform a software reset, consecutively write 0xA3 followed by 0x05 to the SOFT_RESETB register.	0x0	W

OUTLINE DIMENSIONS

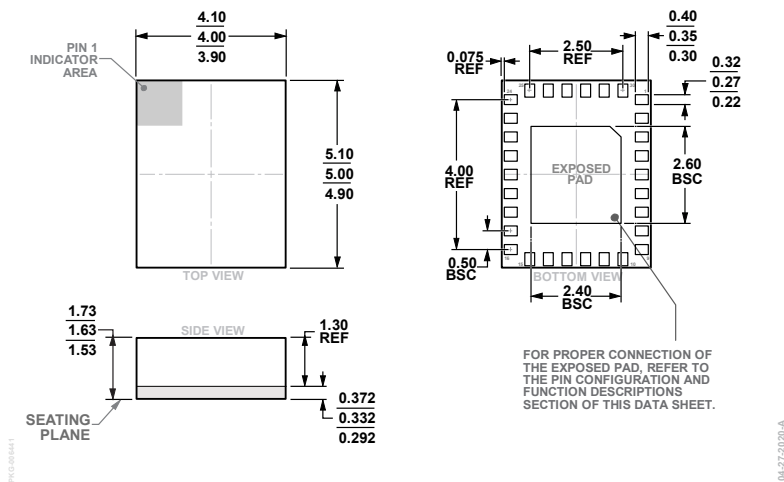


Figure 50. 30-Terminal Land Grid Array [LGA]  
(CC-30-3)  
4 mm × 5 mm Body and 1.63 mm Package Height  
Dimensions shown in millimeters

Updated: August 19, 2023

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADGS2414DBCCZ	-40°C to +125°C	30-lead LGA (4 mm x 5 mm x 1.63mm)	Tray, 490	CC-30-3
ADGS2414DBCCZ-RL7	-40°C to +125°C	30-lead LGA (4 mm x 5 mm x 1.63mm)	Reel, 1000	CC-30-3

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 18. Evaluation Boards

Model <sup>1</sup>	Description
EV-ADGS2414DSDZ	Evaluation Board

<sup>1</sup> Z = RoHS-Compliant Part.

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