Data Sheet

ADGM1121

0 Hz/DC to 18 GHz, DPDT, MEMS Switch

FEATURES

- DC to 18 GHz frequency range
- High bit rate capability up to 64 Gbps
- Low insertion loss:
  - 0.5 dB (typical) at 8 GHz
  - 1.0 dB (typical) at 16 GHz
- High Input IIP3: 73 dBm (typical)
- High RF power handling: 33 dBm (maximum)
- On-resistance: 1.9 Ω (typical)
- High DC current handling: 200 mA
- High switch cycle count: 100 million cycles (minimum)
- Fast switching time: 200 µs T_{ON} (typical)
- Integrated 3.3 V driver for simple control with parallel interface and SPI
- Space-saving integrated passive including decoupling and shunt resistors
- Small 5 mm × 4 mm × 1 mm, 24-lead plastic package
- Temperature range: −40°C to +85°C

APPLICATIONS

- ATE load and probe boards
- DC with high speed loopback testing
- High speed SerDes, PICe Gen4/5, USB4, PAM4
- Relay replacements
- Reconfigurable filters/attenuators
- Military and microwave radios
- Cellular infrastructure: 5G mm wave

FUNCTIONAL BLOCK DIAGRAM

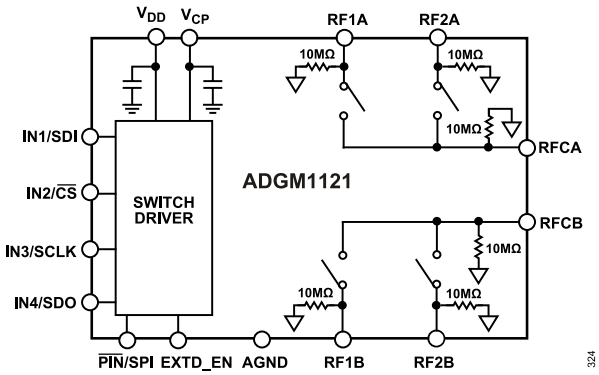

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADGM1121 is a wideband, double-pole, double-throw (DPDT) switch, fabricated using Analog Devices' microelectromechanical system (MEMS) switch technology. This technology enables a small form factor, wide RF bandwidth, highly linear and low insertion loss switch that is operational down to 0 Hz/DC, making it an ideal solution for a wide range of RF and precision equipment switching needs.

An integrated driver chip generates a high voltage to electrostatically actuate switch that can be controlled by a parallel interface and a serial peripheral interface (SPI). All switches are independently controllable.

The device is packaged in a 24-lead, 5 mm × 4 mm × 1 mm land grid array (LGA) package. To ensure optimum operation of the ADGM1121, see the Critical Operational Requirements section.

The on-resistance (R_{ON}) performance of the ADGM1121 is affected by part-to-part variation, channel-to-channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

COMPANION PRODUCTS

- Quad PMU : AD5522
- SP4T MEMS Switch: ADGM1144, ADGM1304, ADGM1004
- Low Noise, LDO : ADP7142, LT1962, LT3045-1

Rev. 0

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SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, AGND, RFGND = 0 V all specifications at 25°C, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
ON-RESISTANCE PROPERTIES						
Initial On-Resistance Properties						
On-Resistance	R_{ON}		1.9	3	Ω	Drain source current (I_{DS}) = 50 mA, 0 V input bias, at 1 ms after first actuation, maximum specification from −40°C to 85°C.
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			0.8	Ω	Maximum value tested from −40°C to 85°C.
On-Resistance Drift						
Over Time	$\Delta R_{ON\ TIME}$			−0.32	Ω	R_{ON} changed from 1 ms to 100 ms after first actuation, maximum value tested from −40°C to 85°C.
Over Actuations	ΔR_{ON}		0.2	0.32	Ω	Absolute change after 10^6 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C.
			+/−0.7		Ω	Absolute change after 100 x 10^6 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C.
				2	Ω	Absolute change after 100 x 10^6 actuations, switch is actuated at 85°C and R_{ON} is measured at 25°C, actuation frequency = 289 Hz.
RELIABILITY PROPERTIES						
Continuously On Lifetime			10		Years	Time before failure[3] at 85°C.
Actuation Lifetime						
Cold Switched		100 x 10^6	500 x 10^6		Actuations	Load between toggling is 150 mA, tested at 85°C.
RF Hot Switched						RF power = continuous wave (CW), terminated into 50 Ω, 50% of test population failure point (T50).
7 dBm			500 x 10^9		Actuations	
10 dBm			150 x 10^6		Actuations	
13 dBm			30 x 10^6		Actuations	
20 dBm			20 x 10^3		Actuations	
DC Hot Switched						Terminated into 50 Ω, RFxx load capacitance = 10 µF, 50% of test population failure point (T50).
0.5 V or 9 mA			500 x 10^6		Actuations	
1 V or 18 mA			500 x 10^6		Actuations	
2.5 V or 46 mA			35 x 10^6		Actuations	
3.5 V or 65 mA			6.5 x 10^3		Actuations	
5 V or 93 mA			2 x 10^3			
DYNAMIC CHARACTERISTICS						
Operational Frequency Range			18		GHz	−3 dB
Insertion Loss	IL					RFCA to RF1A/2A, RFCB to RF1B/2B
			−0.34		dB	DC to 2.5 GHz
			−0.5		dB	2.5 GHz to 6 GHz
			−0.55		dB	6 GHz to 10 GHz
			−1		dB	10 GHz to 16 GHz
Isolation	ISO					RF1A/2A to RFCA, RF1B/2B to RFCB, with at least one switch on.
			−27		dB	DC to 2.5 GHz

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
			−21		dB	2.5 GHz to 6 GHz
			−17		dB	6 GHz to 10 GHz
			−16		dB	10 GHz to 16 GHz
Crosstalk	CTK					RF1A to RF1B, RF2A to RF2B, RFCA to RFCB
			−31		dB	DC to 2.5 GHz
			−26		dB	2.5 GHz to 6 GHz
			−24		dB	6 GHz to 10 GHz
			−20		dB	10 GHz to 16 GHz
Return Loss	RL					Measured at RF1A/RF2A and RF1B/RF2B
			−25		dB	DC to 2.5 GHz
			−21		dB	2.5 GHz to 6 GHz
			−19		dB	6 GHz to 10 GHz
			−15		dB	10 GHz to 16 GHz
Third-Order Intermodulation Intercept	IIP3		73		dBm	Input: 2110 MHz and 2170 MHz, 3510 MHz and 3570 MHz; input power = 30 dBm
Second Harmonic	HD2		−99		dBc	Input: 5 MHz; input power = 0 dBm
	HD2		−93		dBc	Input: 150 MHz, 800 MHz; input power = 33 dBm
Third Harmonic	HD3		−88		dBc	Input: 150 MHz, 800 MHz; input power = 33 dBm
Total Harmonic Distortion	THD		−105		dBc	R_L = 300 Ω, f = 1 kHz, RFxx = 2.5 Vp-p
Total Harmonic Distortion Plus Noise	THD + N		−104		dBc	R_L = 300 Ω, f = 1 kHz, RFxx = 2.5 Vp-p
Maximum RF Power				33	dBm	RF power = CW, terminated into 50 Ω termination; −40°C to +85°C
DC Signal Range		−6		+6	V	On switch DC input bias voltage signal range; −40°C to +85°C
Stand Off voltage		−6		+6	V	−40°C to +85°C, this specification is applied when the switch is in the off position with no RF signal applied
Max. DC Current				200	mA	−40°C to +85°C
On Switching Time[4]	t_{ON}			200	µs	50% INx to 90% (0.05 dB of final IL value) RFxx, 50 Ω termination, −40°C to 85°C. See Figure 5 for details.
Off Switching Time[4,5]	t_{OFF}			200	µs	50% INx to 10% (0.05 dB of final IL value) RFxx, 50 Ω termination, −40°C to 85°C. See Figure 5 for details.
Power-Up Time			4	5	ms	V_{CP} cap = 100 pF, −40°C to +85°C
Video Feedthrough			10		mV peak	1 MΩ termination at RFxx and 50ohm termination at RFC.
Actuation Frequency				2	kHz	Both switches toggled simultaneously.
Internal Oscillator Frequency		8.6	10	11	MHz	
Internal Oscillator Feedthrough[6]			−123		dBm	See note [7] for measurement setup details
			−146		dBm/Hz	This value comes from calculations.
Phase Delta Between Channels			1.8		degree	
Propagation Delay			41		ps	
Channel-to-Channel Skew			4		ps	
CAPACITANCE PROPERTIES						At 1 MHz, includes LGA package capacitance.
On Switch Channel Capacitance	C_{ON}		2.3		pF	
Off Switch Channel Capacitance	C_{OFF}		1.4		pF	

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
LEAKAGE PROPERTIES						
On Leakage[8]		0.7	1.1	1.39	µA	RFxx(off channels) = +6 V; RFCx/RFxx (on channel) = −6 V; Max. value tested from −40°C to +85°C.
Off Leakage[8]		0.34	0.6	0.77	µA	RFxx = +6V; RFCx = −6 V; Max. value tested from −40°C to +85°C.
Internal Shunt Resistor		8.7	11.5	15.2	MΩ	Typical temperature coefficient = 27.5 kΩ/°C, maximum and minimum value tested at 25°C.
DIGITAL INPUTS						Minimum and maximum over −40°C to 85°C.
Input High Voltage	V_{INH}	2			V	
Input Low Voltage	V_{INL}			0.8	V	
Input Current	I_{INL}/I_{INH}		0.025	1	µA	V_{IN} = V_{INL} or V_{INH}
Capacitance			5		pF	
DIGITAL OUTPUTS						Minimum and maximum over −40°C to 85°C.
Output Low Voltage	V_{OL}			0.4	V_{MAX}	I_{SINK} = 1 mA
Output High Voltage	V_{OH}	V_{DD} − 0.4 V			V_{MIN}	I_{SOURCE} = 1 mA
Capacitance			5		pF	
POWER REQUIREMENTS						Minimum and maximum over −40°C to 85°C.
Supply Voltage	V_{DD}	3.0		3.6	V	
Supply Current	I_{DD}			2.5	mA	Digital inputs = 0 V or V_{DD}, SDO floating in SPI mode.
Low Power Mode Current[9]	$I_{DD\ EXT\ VCP}$			50	µA	This value is I_{DD} in low power mode.
External Drive Voltage[10]	VCP_{EXT}	79.2	80	80.8		
External Drive Current	$I_{CP\ EXT\ VCP}$			5	µA	

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.

[2] RFxx is RF1A, RF1B, RF2A, and RF2B. RFCx is RFCA or RFCB. INx is IN1, IN2, IN3, and IN4.

[3] This value shows the time it takes for 1% of a sample lot to fail.

[4] Switch is settled after 200 µs. Do not apply RF power between 0 µs to 200 µs.

[5] RF power should be removed or less than 5 dBm, 50 µs before turning the switch off.

[6] Disable the internal oscillator to eliminate feedthrough.

[7] Spectrum analyzer setup: resolution bandwidth (RBW) = 200 Hz, video bandwidth (VBW) = 2 Hz, span = 100 kHz, input attenuator = 0 dB, detector type = peak, max hold = off. Measurements taken with one switch on and off switch port terminated into 50 Ω. The fundamental feedthrough noise or harmonic thereof is tested (whichever is the highest).

[8] The on leakage and off leakage specifications depend on the DC voltage level applied to the switch node. For example, if 1 V is applied at RF1x to RFCx, the on leakage specification is 0.2 µA and off leakage specification is 0.1 µA. The leakage specification of the switch is mainly driven by the internal 10 MΩ resistors to ground connected on all the RF nodes to avoid floating nodes.

[9] For more details, see the Low Power Mode section.

[10] For more details, see the Internal Oscillator Feedthrough Mitigation section.

SPECIFICATIONS

TIMING CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V, AGND, RFGND = 0 V and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Limit at T_{MIN}	Limit at T_{MAX}	Unit	Conditions
t_1	100		ns	SCLK period
t_2	45		ns	SCLK high pulse width
t_3	45		ns	SCLK low pulse width
t_4	25		ns	$\overline{CS}$ falling edge to SCLK active edge
t_5	20		ns	Data setup time
t_6	20		ns	Data hold time
t_7	25		ns	SCLK active edge to $\overline{CS}$ rising edge
t_8		20	ns	$\overline{CS}$ falling edge to SDO data available
t_9[1]		40	ns	SCLK falling edge to SDO data available
t_{10}		25	ns	$\overline{CS}$ rising edge to SDO data available
t_{11}	100		ns	$\overline{CS}$ high time between SPI commands
t_{12}	25		ns	SCLK edge rejection to $\overline{CS}$ falling edge
t_{13}	25		ns	$\overline{CS}$ rising edge to SCLK edge rejection

[1] Measured with a 20 pF load. t_9 determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

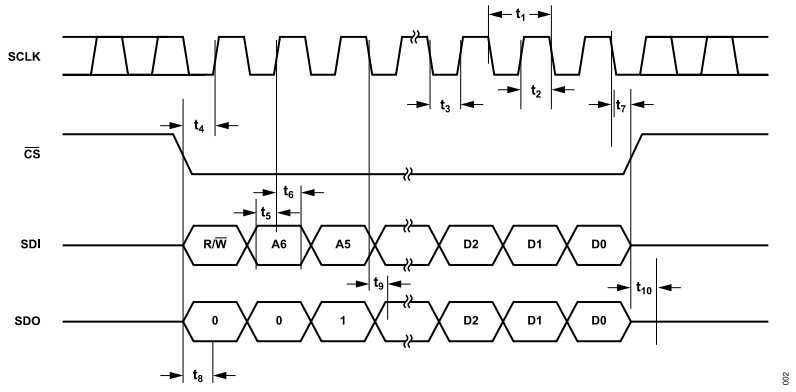

Figure 2. Addressable Mode Timing

SPECIFICATIONS

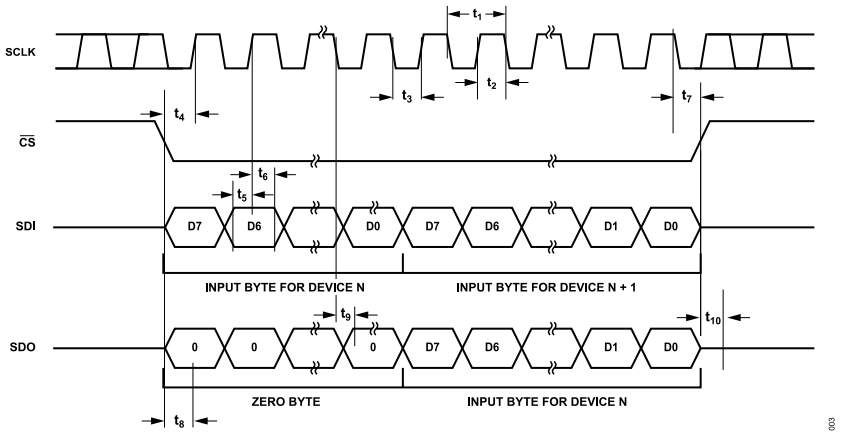

Figure 3. Daisy Chain Timing

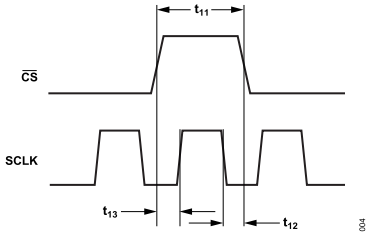

Figure 4. SCLK and $\overline{CS}$ Timing Relationship

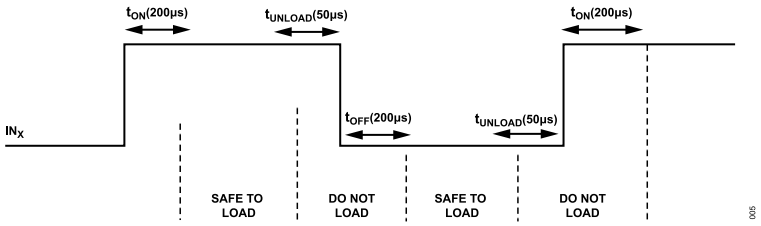

Figure 5. Switch Loading Profile

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first).
Switch DC Rating[2]	
Voltage	±7 V
Current	220 mA
VCP_{EXT}	82 V
Stand Off Voltage[3]	±10 V
RF Power Rating[4]	34 dBm
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 30 sec
Group D	
Mechanical Shock[5]	1500 *g* with 0.5 ms pulse
Vibration	20 Hz to 2000 Hz acceleration at 50 *g*
Constant Acceleration	30,000 *g*

1 Limit the current to the maximum ratings shown.

2 This rating is with respect to the switch in the on position with no RF signal applied.

3 This rating is with respect to the switch in the off position with no RF signal applied.

4 This rating is with respect to the switch in the on position and terminated into 50 Ω.

5 If a device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JCT}	θ_{JCB}	Unit
CC-24-11	104.3	134	66.2	°C/W

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JCT} is the junction to the top of the case thermal resistance.

θ_{JCB} is the junction to the bottom of the case thermal resistance.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for the handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) as per ANSI/ESDA/JEDEC JS-001. Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 5. ESD Ratings

ESD Model	Withstand Threshold	Class
HBM[1]	200 V for the RF1A, RF2A, RFCA, RF1B, RF2B, and RFCB pins 2.5 kV for all other pins	0B
FICDM[2]	1 kV	C3

1 Take proper precautions during handling, as outlined in the Handling Precautions section.

2 A safe automated handling and assembly process is achieved at this rating level by implementing industry standard ESD controls.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

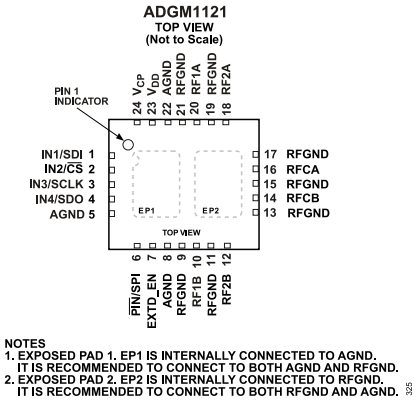

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1/SDI	Parallel Logic Digital Control Input 1. The voltage applied to this pin controls the gate of the RF1A to RFCA MEMS switch. In SPI mode, this pin is the serial data input (SDI) pin.
2	IN2/$\overline{CS}$	Parallel Logic Digital Control Input 2. The voltage applied to this pin controls the gate of the RF2A to RFCA MEMS switch. In SPI mode, this pin is the chip select ($\overline{CS}$) pin. $\overline{CS}$ is an active low signal that selects the target device with which the controller device intends to communicate.
3	IN3/SCLK	Parallel Logic Digital Control Input 3. The voltage applied to this pin controls the gate of the RF2B to RFCB MEMS switch. In SPI mode, this pin is the serial clock (SCLK) pin that synchronizes the target device(s) to the controller device.
4	IN4/SDO	Parallel Logic Digital Control Input 4. The voltage applied to this pin controls the gate of the RF1B to RFCB MEMS switch. In SPI mode, this pin is the serial data output (SDO) pin.
6	$\overline{PIN}$/SPI	Parallel Mode Enable/SPI Mode Enable. The SPI is enabled when this pin is high, and the parallel interface (IN1, IN2, IN3, IN4) is enabled when this pin is low.
7	EXTD_EN	External Voltage Drive Enable. In normal operation, set EXTD_EN low to enable the built-in 10 MHz oscillator, which enables the internal driver IC voltage boost circuitry. Setting EXTD_EN high disables the internal 10 MHz oscillator and driver boost circuitry. With the oscillator disabled, the switch can still be controlled through the logic interface pins (IN1 to IN4) or SPI, but the V_{CP} pin must be driven with 80 V DC from an external voltage supply. In this mode, the ADGM1121 only consumes 50 µA maximum supply current. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough from the switch.
5, 8, 22	AGND	Analog Ground Connection (recommend connecting AGND and RFGND together).
9, 11, 13, 15, 17, 19, 21	RFGND	RF Ground Connection (recommend connecting AGND and RFGND together).
10	RF1B	RF1B Port. This pin can be an input or an output. If unused, the pin must be connected to GND or terminated with a 50 Ω resistor to RFGND
12	RF2B	RF2B Port. This pin can be an input or an output. If unused, the pin must be connected to GND or terminated with a 50 Ω resistor to RFGND
14	RFCB	Common RFCB Port. This pin can be an input or an output.
16	RFCA	Common RFCA Port. This pin can be an input or an output.
18	RF2A	RF2A Port. This pin can be an input or an output. If unused, the pin must be connected to GND or terminated with a 50 Ω resistor to RFGND
20	RF1A	RF1A Port. This pin can be an input or an output. If unused, the pin must be connected to GND or terminated with a 50 Ω resistor to RFGND
23	V_{DD}	Positive Power Supply Input. For the recommended input voltage, see Table 1. No external AC decoupling capacitors are needed as they are integrated into the package.
24	V_{CP}	Driver IC input/output. In normal operating mode, this pin outputs 80 V DC and should not be loaded externally as there is an internal decoupling capacitor connected to ground in the package. If pin 7, the external driver enable pin is high, the internal voltage boost circuity is disabled, and an 80 V DC voltage must be input into V_{CP} to drive the switches through the logic interface.
	EP1	Exposed Pad 1. EP1 is internally connected to AGND. Connect this pad to AGND or to both AGND and RFGND.
	EP2	Exposed Pad 2. EP2 is internally connected to RFGND. Connect this pad to RFGND or to both RFGND and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

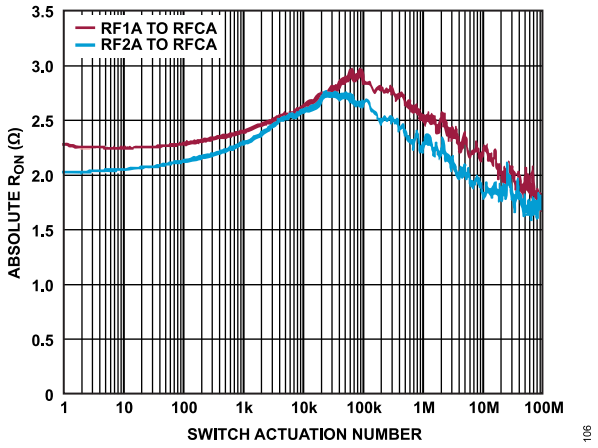

Figure 7. Absolute R_{ON} vs. Switch Actuation Number (T_A = 25°C, Load Current Applied During Actuations = 50 mA)

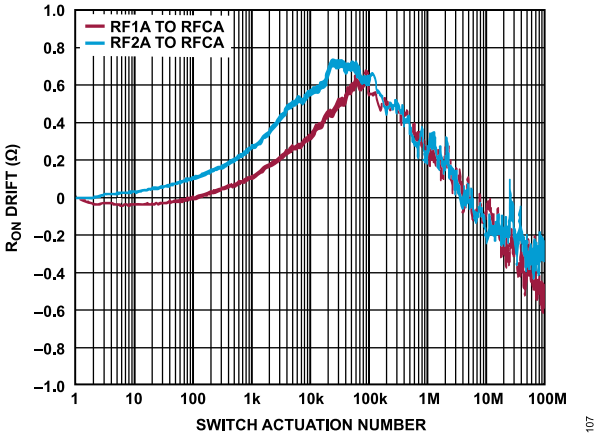

Figure 8. R_{ON} Drift vs. Switch Actuation Number, Normalized at Zero (T_A = 25°C, and Load Current Applied During Actuations = 50 mA)

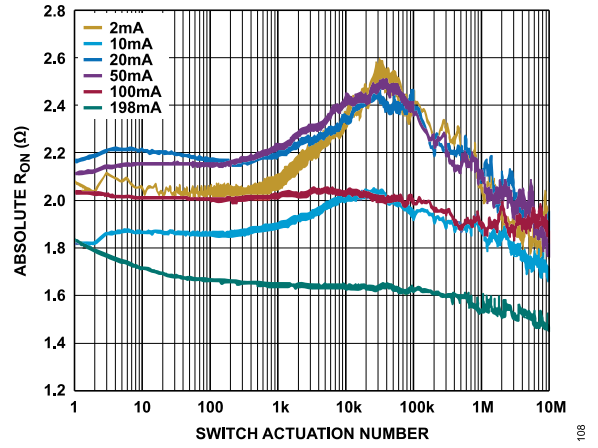

Figure 9. Absolute R_{ON} vs. Switch Actuation Number Over Different Currents Applied During Actuations (T_A = 25°C, V_{DD} = 3.3 V)

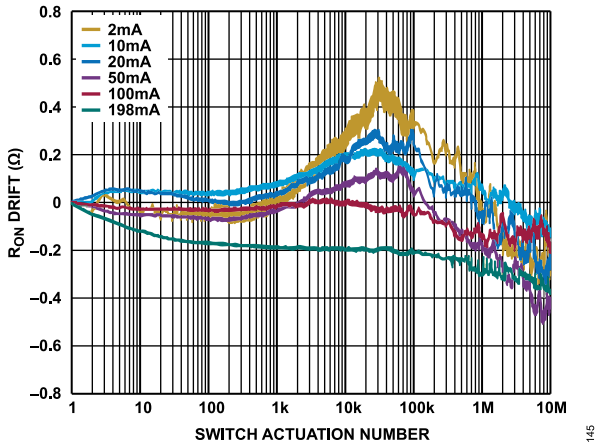

Figure 10. R_{ON} Drift vs. Switch Actuation Number Over Different Currents Applied During Actuations, Normalized at Zero (T_A = 25°C, V_{DD} = 3.3 V)

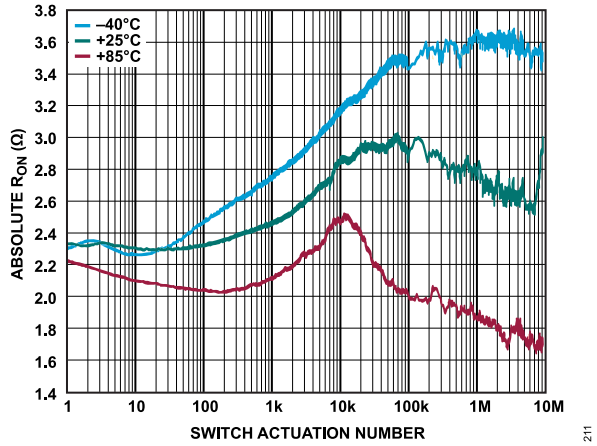

Figure 11. Absolute R_{ON} vs. Switch Actuation Number Over Temperature (Load Current Applied During Actuations = 50 mA, V_{DD} = 3.3 V)

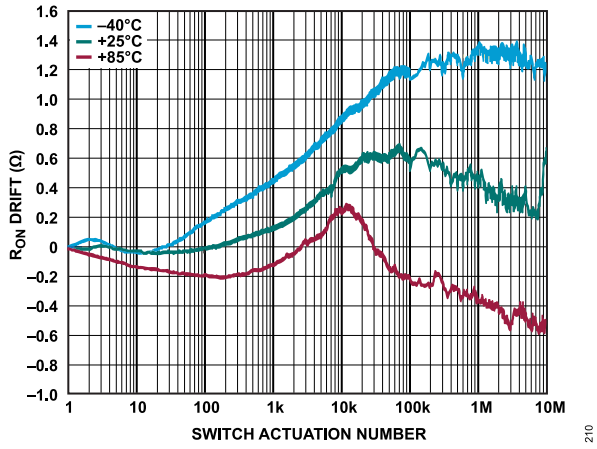

Figure 12. R_{ON} Drift vs. Switch Actuation Number Over Temperature, Normalized at Zero (Load Current Applied During Actuations = 50 mA, V_{DD} = 3.3 V)

TYPICAL PERFORMANCE CHARACTERISTICS

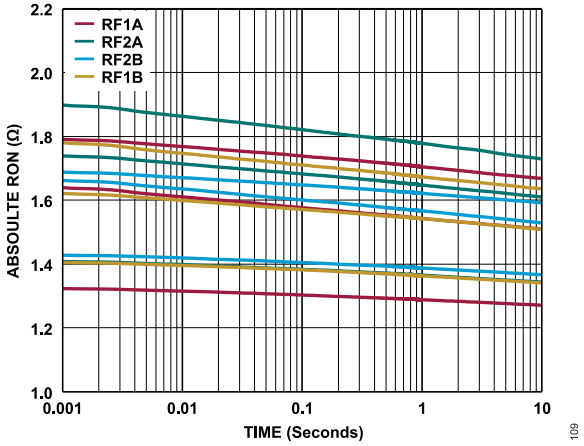

Figure 13. Absolute R_{ON} vs. Time (1 ms to 10 sec) Over Different Channels, Multiple Devices (T_A = 25°C, V_{DD} = 3.3 V, Load Current = 50 mA)

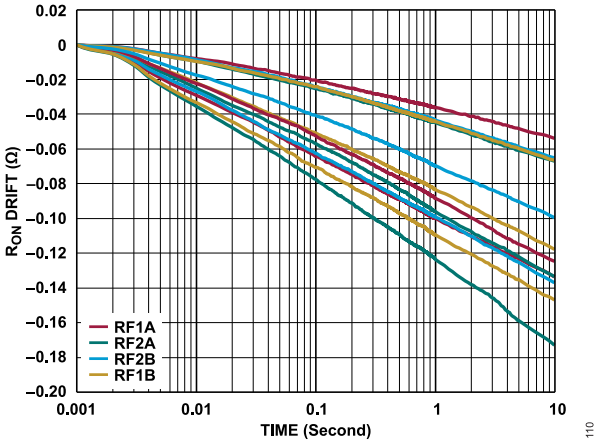

Figure 14. R_{ON} Drift vs. Time (1 ms to 10 sec) Over Different Channels, Multiple Devices, Normalized at Zero (T_A = 25°C, V_{DD} = 3.3 V, Load Current = 50 mA)

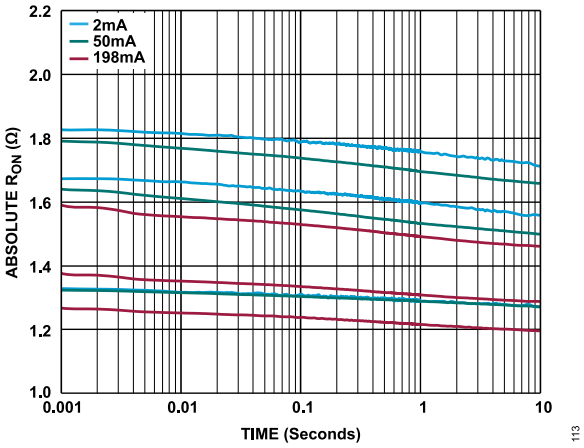

Figure 15. Absolute R_{ON} vs. Time (1 ms to 10 sec) Over Different Current Levels, Multiple Devices (T_A = 25°C, V_{DD} = 3.3 V, RF1A to RFCA)

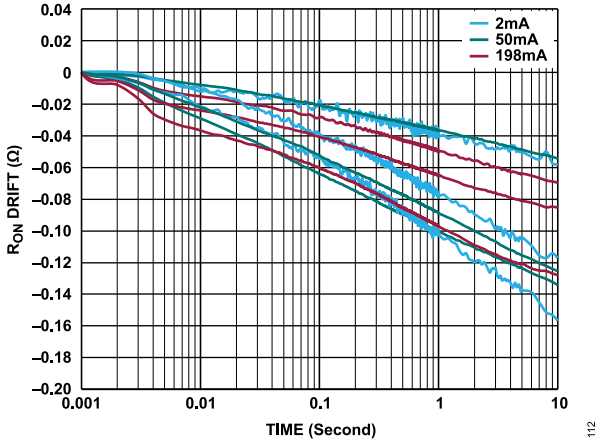

Figure 16. R_{ON} Drift vs. Time (1 ms to 10 sec) Over Different Current Levels, Multiple Devices, Normalized at Zero (T_A = 25°C, V_{DD} = 3.3 V, RF1A to RFCA)

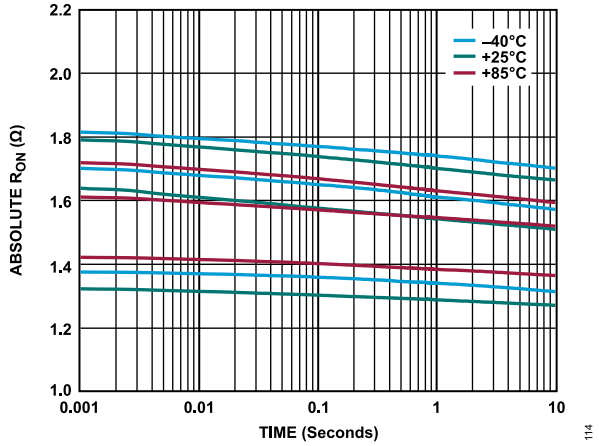

Figure 17. Absolute R_{ON} vs. Time (1 ms to 10 sec) Over Temperature, Multiple Devices (Load Current = 50 mA, V_{DD} = 3.3 V, RF1A to RFCA)

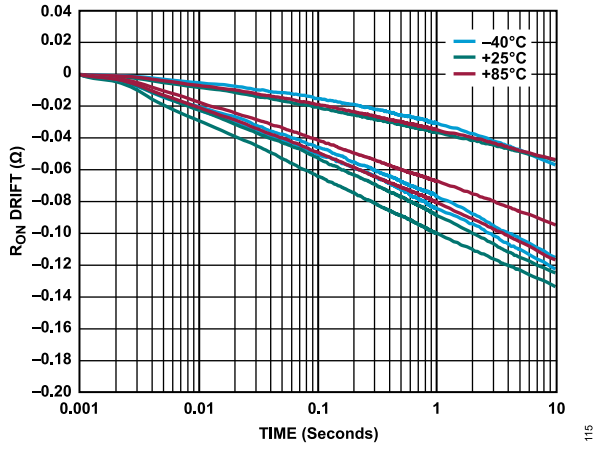

Figure 18. R_{ON} Drift vs. Time (1 ms to 10 sec) Over Temperature, Multiple Devices, Normalized at Zero (Load Current = 50 mA, V_{DD} = 3.3 V, RF1A to RFCA)

TYPICAL PERFORMANCE CHARACTERISTICS

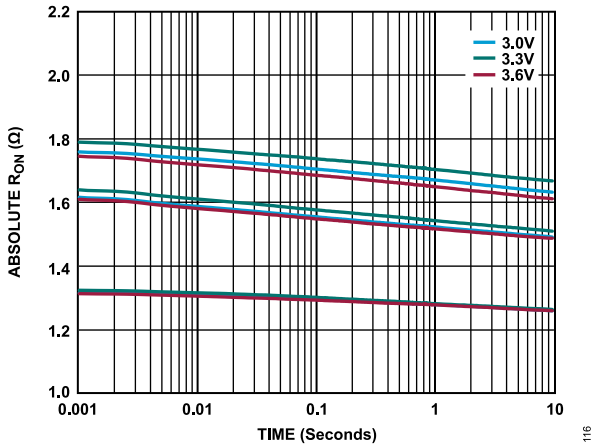

Figure 19. Absolute R_{ON} vs. Time (1 ms to 10 sec) Over Supplies, Multiple Devices (Load Current = 50 mA, V_{DD} = 3.3 V, RF1A to RFCA)

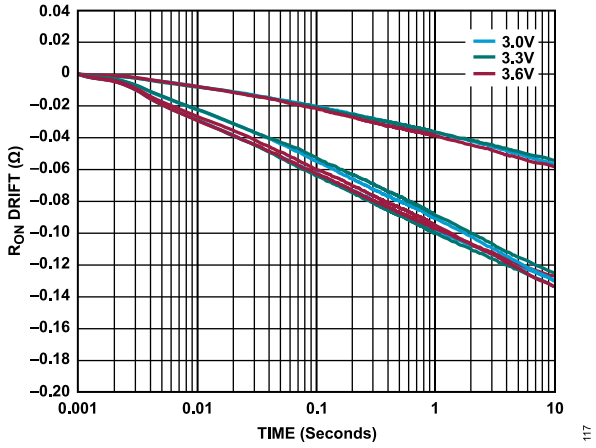

Figure 20. R_{ON} Drift vs. Time (1 ms to 10 sec) Over Supplies, Multiple Devices, Normalized at Zero (Load Current = 50 mA, V_{DD} = 3.3 V, RF1A to RFCA)

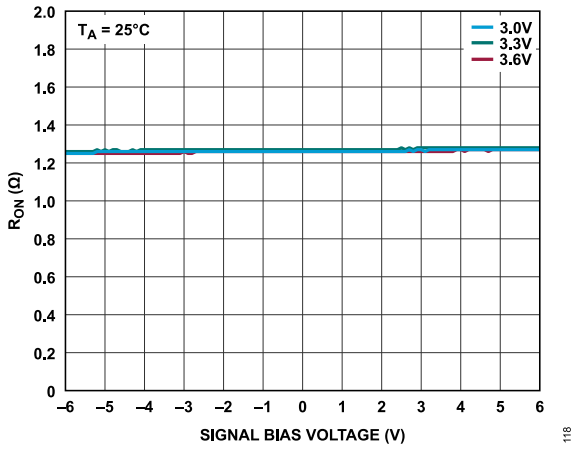

Figure 21. R_{ON} vs. Signal Bias Voltage Over Supply Voltages (RF1A to RFCA On, 50 mA)

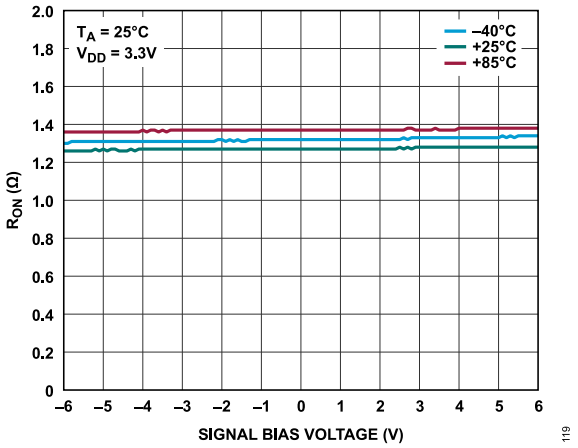

Figure 22. R_{ON} vs. Signal Bias Voltage Over Temperature (RF1A to RFCA On, 50 mA)

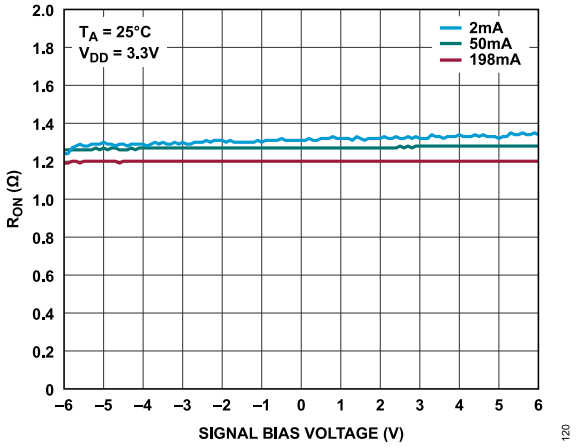

Figure 23. R_{ON} vs. Signal Bias Voltage Over Different Current Levels (RF1A to RFCA On)

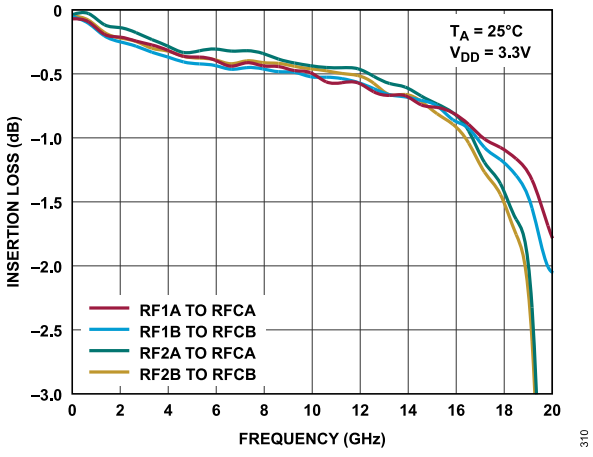

Figure 24. Insertion Loss vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

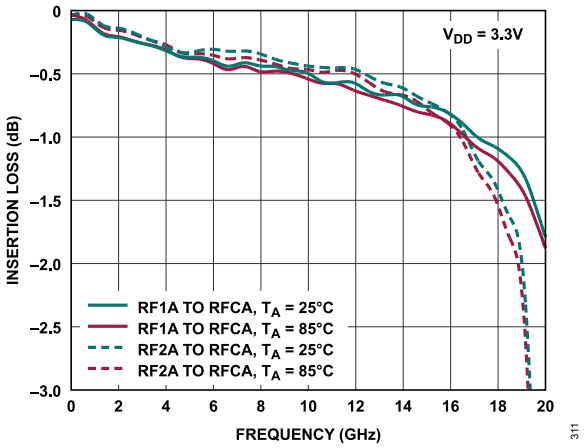

Figure 25. Insertion Loss vs. Frequency Over Temperature (RF1A to RFCA, RF2A to RFCA)

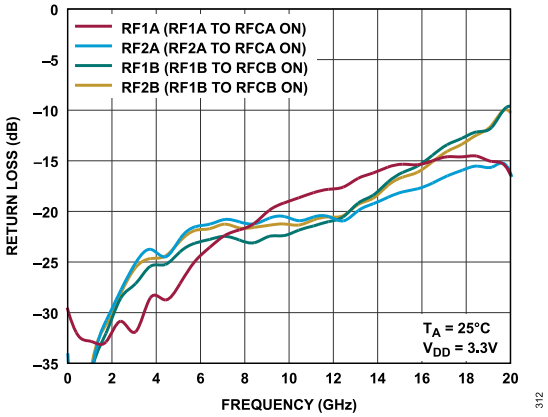

Figure 26. Return Loss vs. Frequency (Measuring from RF1A, RF2A, RF1B, and RF2B)

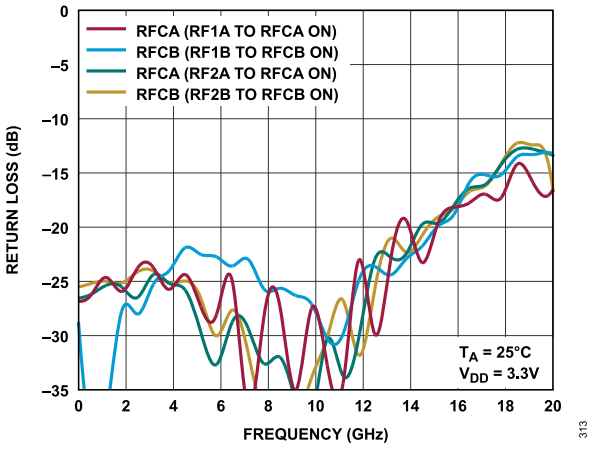

Figure 27. Return Loss vs. Frequency (Measuring from RFCA and RFCB)

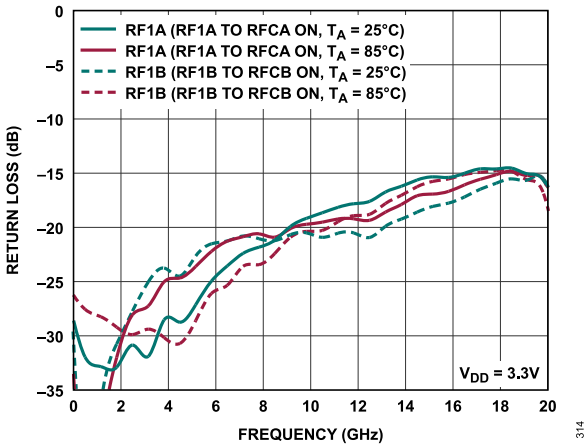

Figure 28. Return Loss vs. Frequency Over Temperature (Measuring from RF1A, RF2A, RF1B, and RF2B)

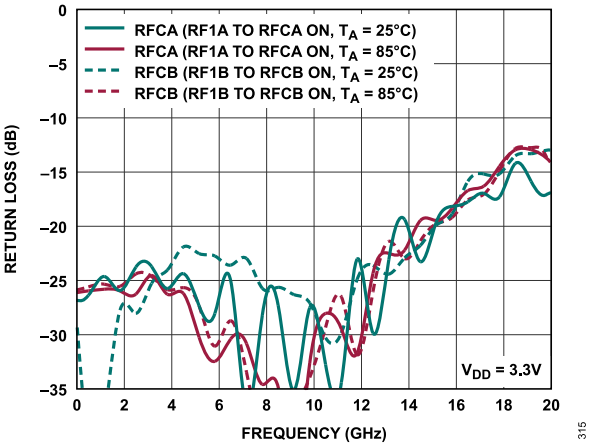

Figure 29. Return Loss vs. Frequency Over Temperature (Measuring from RFCA and RFCB)

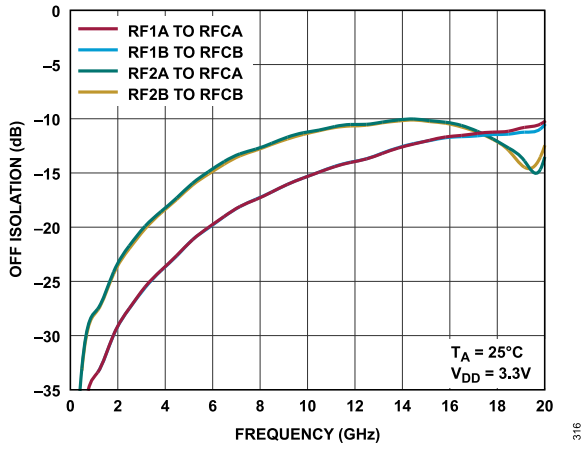

Figure 30. Off Isolation vs. Frequency (All Channels Off)

TYPICAL PERFORMANCE CHARACTERISTICS

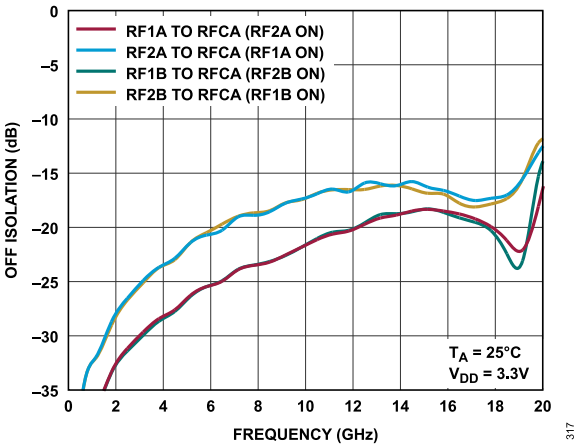

Figure 31. Off Isolation vs. Frequency (One Channel On)

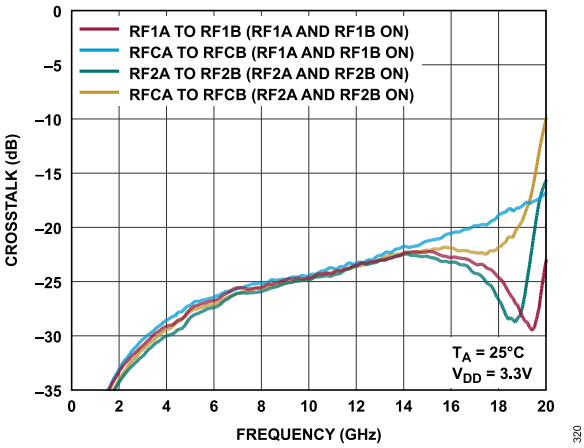

Figure 34. Crosstalk vs. Frequency (Two Channels On)

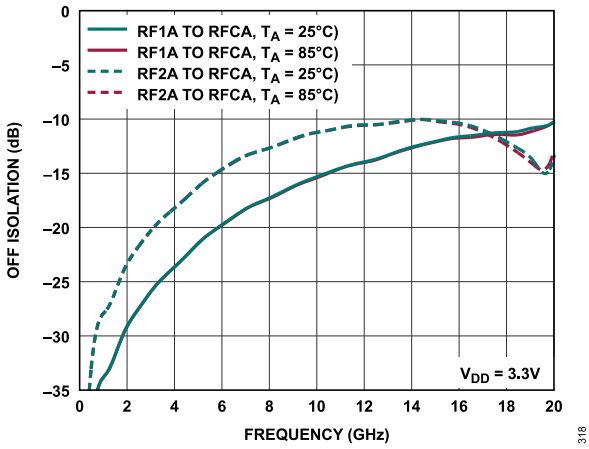

Figure 32. Off Isolation vs. Frequency Over Temperature (All Channels Off)

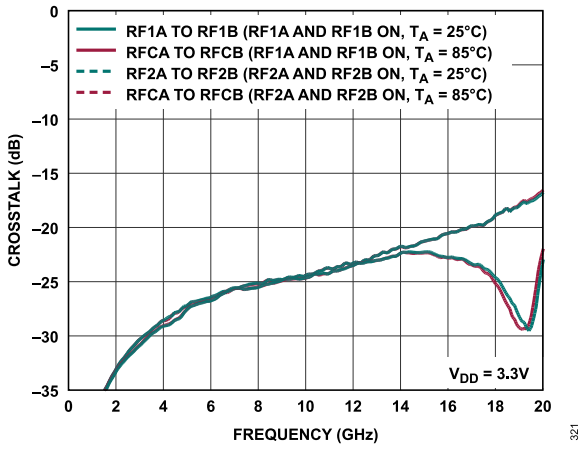

Figure 35. Crosstalk vs. Frequency Over Temperature (Two Channels On)

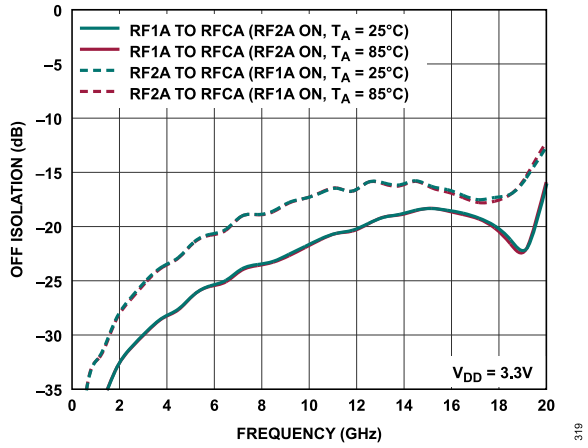

Figure 33. Off Isolation vs. Frequency Over Temperature (One Channel On)

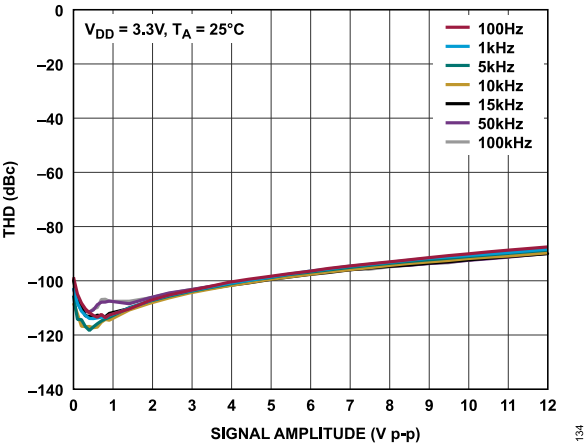

Figure 36. THD vs. Signal Amplitude (R_L = 300 Ω, Signal Source Impedance = 20 Ω)

TYPICAL PERFORMANCE CHARACTERISTICS

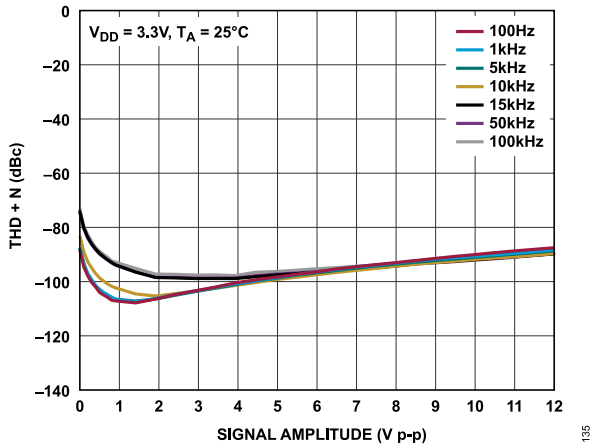

Figure 37. THD + N vs. Signal Amplitude (R_L = 300 Ω, Signal Source Impedance = 20 Ω)

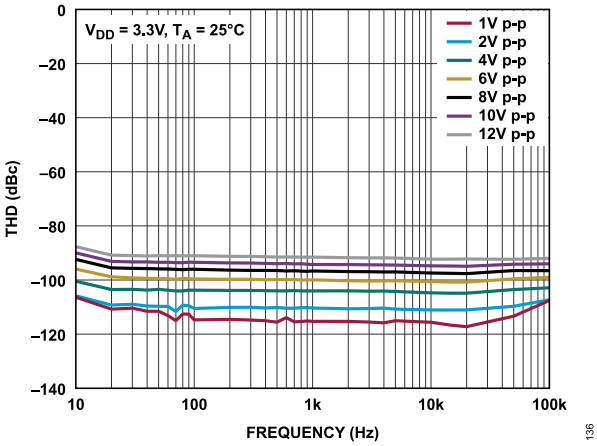

Figure 38. THD vs. Frequency (R_L = 300 Ω, Signal Source Impedance = 20 Ω)

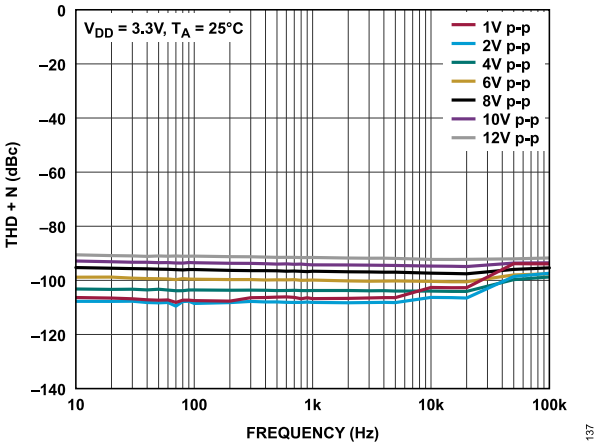

Figure 39. THD + N vs. Frequency (R_L = 300 Ω, Signal Source Impedance = 20 Ω)

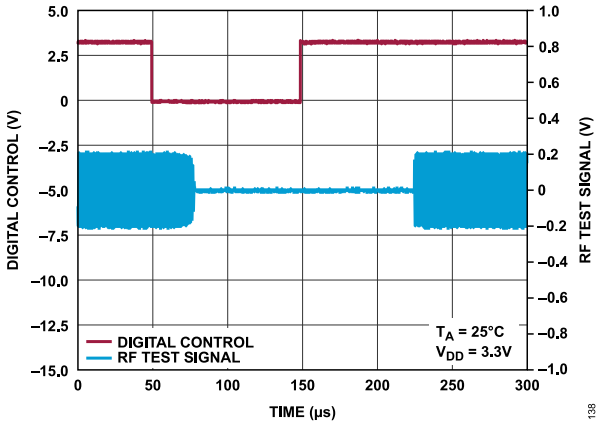

Figure 40. Digital Control and RF Test Signal vs. Time (V_{DD} = 3.3 V)

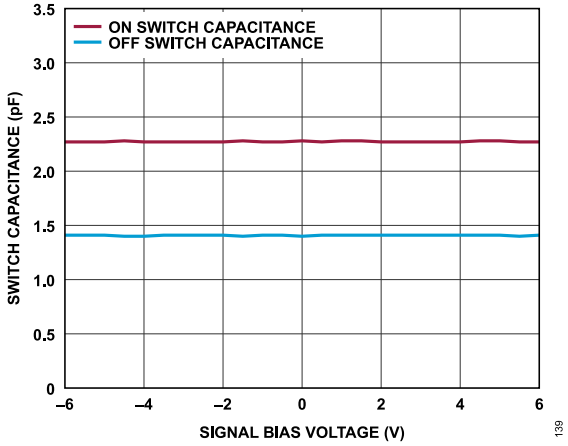

Figure 41. Switch Capacitance vs. Signal Bias Voltage (V_{DD} = 3.3 V, T_A = 25°C)

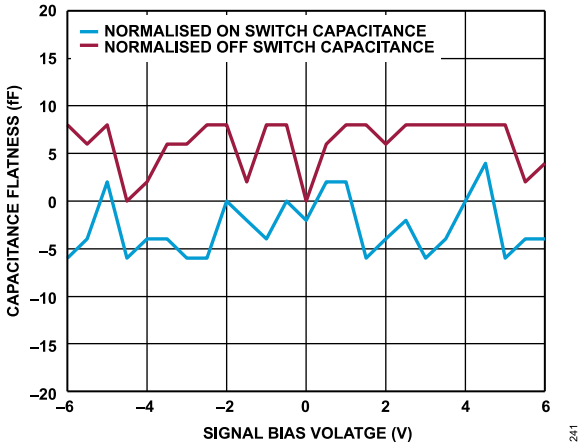

Figure 42. Capacitance Flatness vs. Signal Bias Voltage (V_{DD} = 3.3 V, T_A = 25°C)

TYPICAL PERFORMANCE CHARACTERISTICS

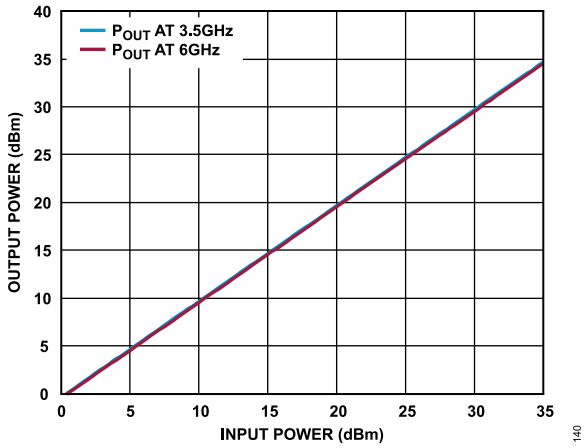

Figure 43. Output Power (P_{OUT}) vs. Input Power (P_{IN}) (V_{DD} = 3.3 V)

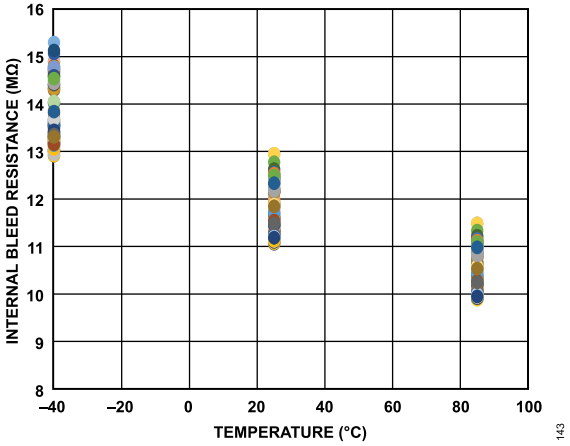

Figure 46. Internal Bleed Resistor Distribution Over Temperature

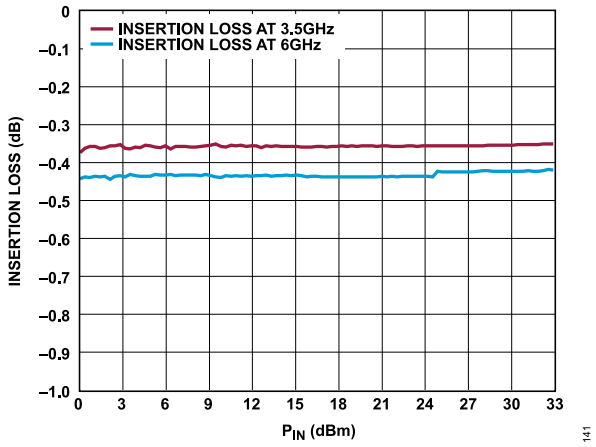

Figure 44. Insertion Loss vs. P_{IN}

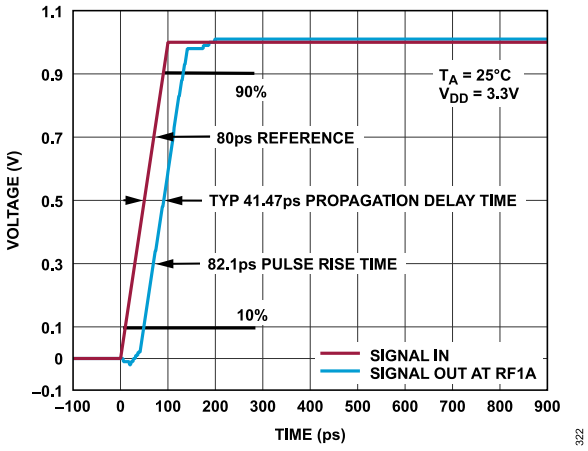

Figure 47. Time Domain Response (RF1A to RFCA)

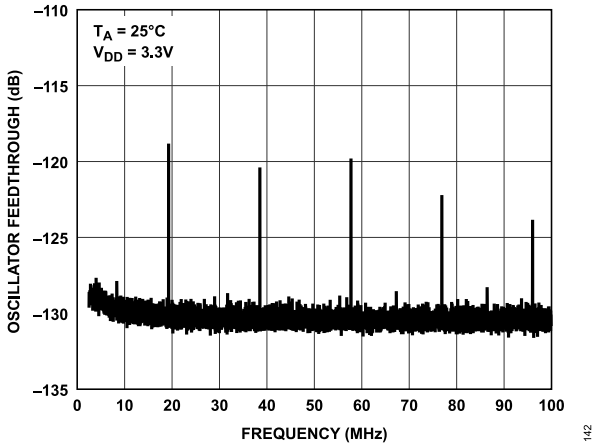

Figure 45. Oscillator Feedthrough vs. Frequency, Wide Bandwidth (V_{DD} = 3.3 V)

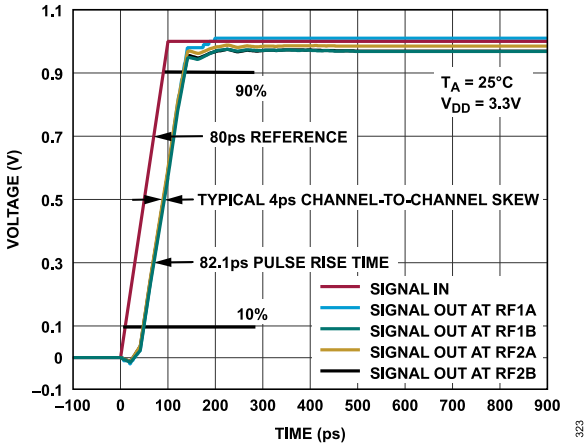

Figure 48. Channel-to-Channel Skew, Time Domain Response

TYPICAL PERFORMANCE CHARACTERISTICS

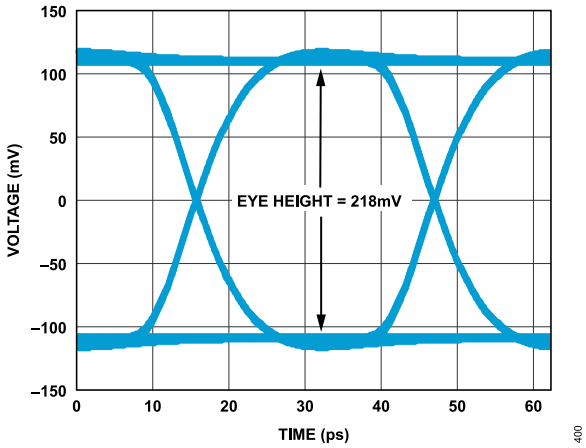

Figure 49. Reference Eye Diagram at 32 Gbps (Non-Return-to-Zero (NRZ), T_{RISE}/T_{FALL} = 16 ps)

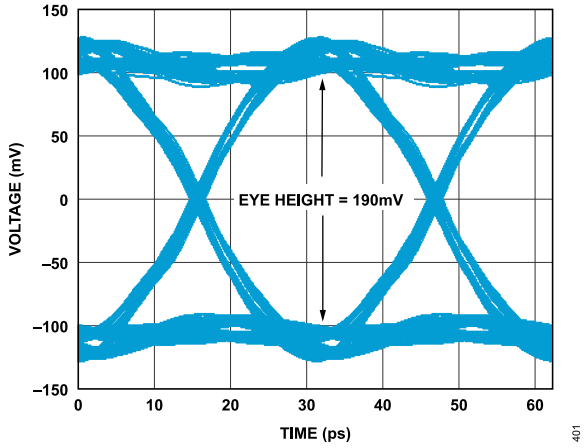

Figure 50. Eye Diagram at 32 Gbps (NRZ, T_{RISE}/T_{FALL} = 16 ps, Signal Thru 1 x ADGM1121)

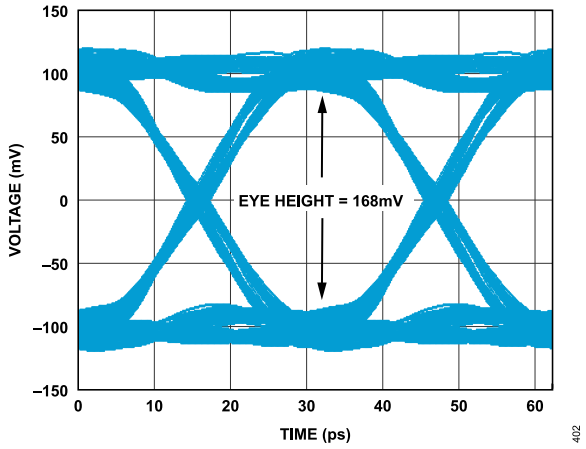

Figure 51. Eye Diagram at 32 Gbps (NRZ, T_{RISE}/T_{FALL} = 16 ps, Signal Thru 2 x ADGM1121 in Loopback Configuration)

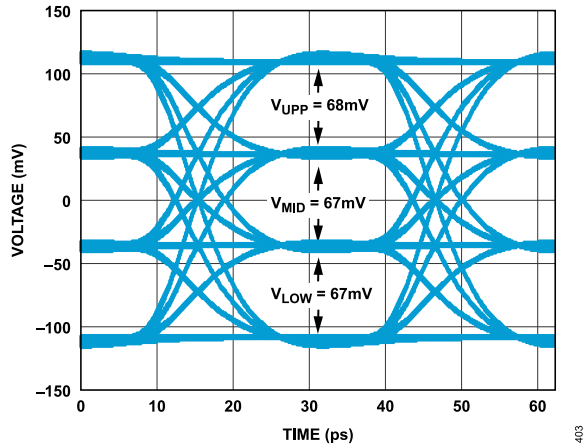

Figure 52. Reference Eye Diagram at 64 Gbps (Pattern Used Pulse Amplitude Modulation 4-Level (PAM4), T_{RISE}/T_{FALL} = 16 ps)

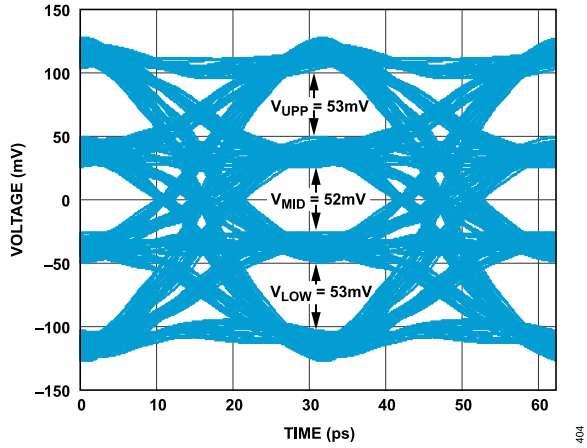

Figure 53. Eye Diagram at 64 Gbps (PAM4, T_{RISE}/T_{FALL} = 16 ps, Signal Thru 1 x ADGM1121)

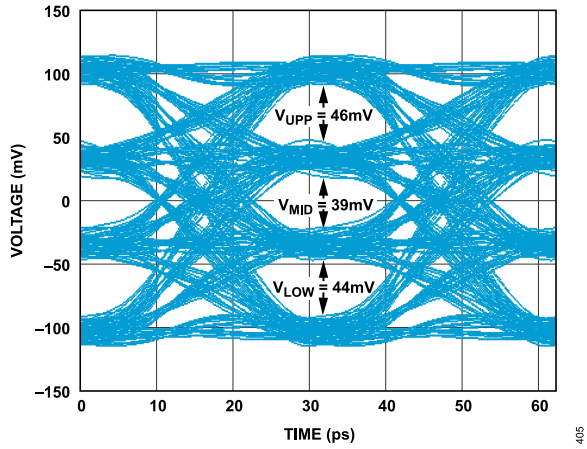

Figure 54. Eye Diagram at 64 Gbps (PAM4, T_{RISE}/T_{FALL} = 16 ps, Signal Thru 2 x ADGM1121 in Loopback Configuration)

THEORY OF OPERATION

SWITCH DESIGN

The ADGM1121 is a wideband DPDT switch fabricated using Analog Devices' microelectromechanical systems (MEMS) switch technology. This technology enables high power, low loss, low distortion gigahertz switches to be realized for demanding RF applications.

A key strength of the MEMS switch is that it simultaneously brings together best-in-class high frequency RF performance and 0 Hz/DC precision performance. This combination coupled with superior reliability and a tiny surface mountable form factor make the MEMS switch the ideal switching solution for all RF and precision signal instrumentation needs.

PARALLEL DIGITAL INTERFACE

The ADGM1121 can be controlled through a parallel interface. Standard complementary metal–oxide–semiconductor (CMOS)/low voltage transistor-transistor logic (LVTTL) signals applied through this interface control the independent actuation/release of all the switch channels of the ADGM1121.

Setting pin 6 ($\overline{\text{PIN}}$/SPI) low enables the parallel control interface. Pins 1, 2, 3, and 4 (IN1, IN2, IN3, and IN4) control the switching functions of the ADGM1121. When a Logic 1 is applied to one of these pins, the corresponding switch turns on. Conversely, when a Logic 0 is applied, the switch turns off. See Table 7 for the truth table.

When no supply voltage is applied to pin 23 (V_{DD}), all switches are in an indeterminate state.

Table 7. Truth Table in Parallel Digital Interface Mode

IN1	IN2	IN3	IN4	RF1A to RFCA	RF2A to RFCA	RF2B to RFCB	RF1B to RFCB
0	0	0	0	Off	Off	Off	Off
0	0	0	1	Off	Off	Off	On
0	0	1	0	Off	Off	On	Off
0	0	1	1	Off	Off	On	On
0	1	0	0	Off	On	Off	Off
0	1	0	1	Off	On	Off	On
0	1	1	0	Off	On	On	Off
0	1	1	1	Off	On	On	On
1	0	0	0	On	Off	Off	Off
1	0	0	1	On	Off	Off	On
1	0	1	0	On	Off	On	Off
1	0	1	1	On	Off	On	On
1	1	0	0	On	On	Off	Off
1	1	0	1	On	On	Off	On
1	1	1	0	On	On	On	Off
1	1	1	1	On	On	On	On

THEORY OF OPERATION

SPI DIGITAL INTERFACE

The ADGM1121 can be controlled through an SPI digital interface when pin 6 ($\overline{PIN}$/SPI) is high. SPI Mode 0 or Mode 3 can be used with the device, and it operates with SCLK frequencies up to 10 MHz. The default mode when the SPI is active is the "Addressable Mode", in which the devices registers are accessed by a 16-bit SPI command bounded by the state of $\overline{CS}$. The ADGM1121 can also operate in the daisy-chain mode.

The SPI pins of the ADGM1121 are $\overline{CS}$, SCLK, SDI, and SDO. Hold $\overline{CS}$ low when using the SPI. Data is captured on SDI on the rising edge of SCLK and data is propagated out on SDO on the falling edge of SCLK. SDO has a push-pull output driver architecture. So, it does not require pull-up resistors. When not pulled low by the ADGM1121, SDO is in a high-impedance state.

Addressable Mode

The addressable mode is the default mode for the ADGM1121 upon power up. A single SPI frame in the addressable mode is bound by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. It comprises 16 SCLK cycles. Figure 55 shows the timing diagram for addressable mode for SPI Mode 0.

The first SDI bit indicates if the SPI command is a read or write command. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command as during these clock cycles SDO propagates out the data contained in the addressed register.

In Mode 0, during any SPI command, SDO sends out eight alignment bits on the $\overline{CS}$ falling edge and the first seven SCLK falling edges (in Mode 3, the first SCLK falling edge is ignored, as shown in Figure 56). The alignment bits observed at SDO are 0x25.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the eighth to the fifteenth SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

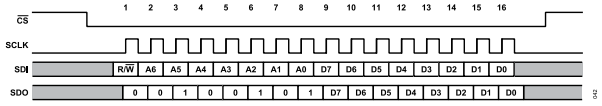

Figure 55. Addressable Mode Timing Diagram (Mode 0)

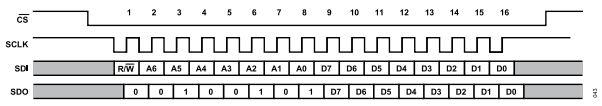

Figure 56. Addressable Mode Timing Diagram (Mode 3)

Daisy-Chain Mode

The connection of several ADGM1121 devices in a daisy-chain configuration is possible. All devices share the same $\overline{CS}$ and SCLK line while the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In the daisy-chain mode, SDO is an 8-cycle delayed version of SDI.

The ADGM1121 may only enter the daisy-chain mode from the addressable mode by sending the 16-bit SPI command, 0x2500. See Figure 57 for an example of this. When the ADGM1121 receives this command, the SDO of devices sends out the same command. This is because the alignment bits at SDO are 0x25. This allows multiple daisy-connected devices to enter the daisy-chain mode in a single SPI frame. A hardware reset is required to exit the daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 58. When $\overline{CS}$ goes high, Device1 writes Command0 [7:0] to its switch data register, Device 2 writes Command1 [7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering the daisy-chain mode, the first eight bits sent out by SDO are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset to zero.

An SCLK rising edge reads in data on SDI while data is propagated out SDO on an SCLK falling edge. The expected number of SCLK cycles should be a multiple of eight before $\overline{CS}$ goes high. When this is not the case, the SPI sends the last eight bits received to the switch data register.

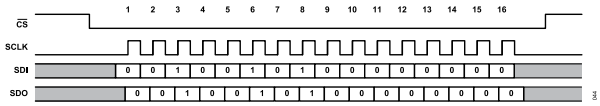

Figure 57. SPI Command to Enter the Daisy-Chain Mode

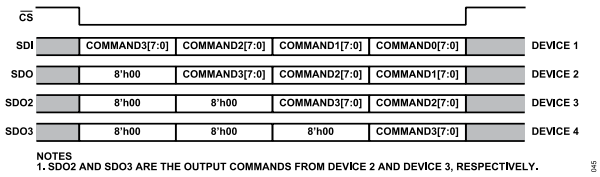

Figure 58. Example of an SPI Frame When Three ADGM1121 are Connected in the Daisy-Chain Mode

Hardware Reset

The digital section of the ADGM1121 goes through an initialization phase during V_{DD} power up. To hardware reset the part, power cycle the V_{DD} input. After power-up or a hardware reset, ensure there is a minimum of 10 µs from the time of power-up or reset before any SPI command is issued. Ensure that V_{DD} does not drop out during the 10 µs initialization phase because it may result in incorrect operation of the ADGM1121.

THEORY OF OPERATION

Internal Error Status

Where an internal error is detected in the part, it is flagged in the internal error status bits [7:6] of the SWITCH_DATA register. An internal error results from an error in the configuration of the part at power-up.

INTERNAL OSCILLATOR FEEDTHROUGH

The ADGM1121 has an internal oscillator running at a nominal 10 MHz. This oscillator drives the charge pump circuitry that provides the actuation voltage for each of the switch gate electrodes. Although this oscillator is very low power, the 10 MHz signal is coupled to the switch and can be considered a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −123 dBm when one switch is on. The V_{DD} level and temperature changes affect the frequency of the noise spur. For the maximum and minimum frequency ranges over temperature and voltage supply range, see Table 1.

INTERNAL OSCILLATOR FEEDTHROUGH MITIGATION

In normal operation, the 80 V actuation voltage is supplied by the driver IC. Setting the EXTD_EN pin (pin 7) low enables the built-in 10 MHz oscillator. This setting enables the charge pump circuitry to generate the 80 V required for the MEMS switch actuation. The internal oscillator is a source of noise that couples through to the RF ports. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −123 dBm when one switch is on. The internal oscillator feedthrough can be eliminated by setting the EXTD_EN pin high, which disables the internal oscillator and charge pump circuitry. When the internal oscillator and charge pump circuitry are disabled, the V_{CP} pin (pin 24) must be driven with 80 V DC (VCP_{EXT}) from an external voltage supply, as outlined in Table 6, required for the MEMS switch actuation. The switch can still be controlled through the digital logic interface pins.

LOW POWER MODE

Setting the EXTD_EN pin high shuts down the internal oscillator. The ADGM1121 enters the low power quiescent state, drawing only 50 µA maximum supply current. When the internal oscillator and charge pump circuitry are disabled, the V_{CP} pin (pin 24) must be driven with 80 V DC (VCP_{EXT}) from an external voltage supply, as outlined in Table 6, required for the MEMS switch actuation. The switch can still be controlled through the digital logic interface pins or SPI.

TYPICAL OPERATING CIRCUIT

Figure 59 shows the typical operating circuit for the ADGM1121. V_{DD} is connected to 3.3 V. EP1 connects to EP2 internally. It is recommended to connect RFGND to AGND using one large pad on the PCB to short together EP1 and EP2. EP1 and EP2 are not connected internally. Figure 59 shows the ADGM1121 configured to use the internal oscillator as the reference clock to the driver IC control circuit. Alternatively, set pin 7 (EXTD_EN) high and apply 80 V DC directly to pin 24 to disable the internal oscillator and eliminate all oscillator feedthrough. The switches can then be controlled as normal through the logic control interface, pin 1 to pin 4.

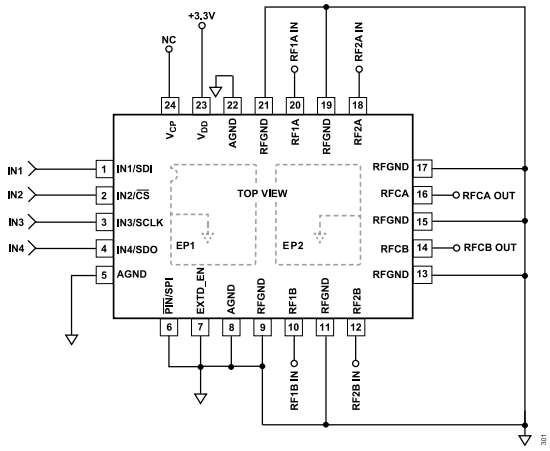

Figure 59. Typical Operating Circuit in the Parallel Digital Interface Mode

APPLICATIONS INFORMATION

POWER SUPPLY RAILS

The ADGM1121 can operate with unipolar supplies between 3.0 V and 3.6 V. The device is fully specified at a 3.3 V analog supply voltage.

POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of most high performance signal chains.

Figure 60 shows an example of a unipolar solution for the ADGM1121. The ADP7142 is a low dropout linear regulator that operates from 2.7 V to 40 V and is ideal for the regulation of high performance analog and mixed-signal circuits operating from 39 V down to 1.2 V rails. The ADP7142 has 11 µV rms output noise independent of the output voltage. The ADP7142 can be used to power the supply rail for the ADGM1121, a microcontroller, and/or other devices in the signal chain.

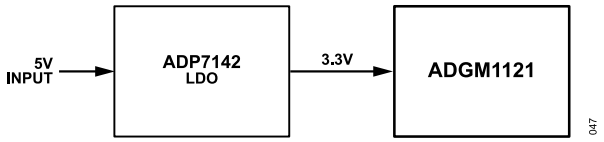

Figure 60. Unipolar Power Solution

If low noise performance at the power supply is required, the ADP7142 can be replaced by the LT1962 or LT3045-1.

Table 8. Recommended Power Management Devices

Product	Description
ADP7142	40 V, 200 mA, low noise, CMOS LDO linear regulator
LT1962	300 mA, low noise, micropower, low dropout (LDO) regulator
LT3045-1	20 V, 500 mA, ultra-low noise, ultra-high power supply rejection ratio (PSRR) linear regulator with voltage for input to output control (VIOC)

HIGH-SPEED DIGITAL LOOPBACK

Testing high-speed input and output (HSIO) interfaces, such as peripheral component interconnect express 4 (PCIe) Gen 4.0 and PCIe Gen 5.0, in a high volume manufacturing environment is a challenge. A common approach to validate an HSIO interface is the implementation of a high-speed loopback test method. This incorporates both high-speed and DC test paths in one configuration.

To perform high-speed loopback testing, generally a pseudorandom bit sequence (PRBS) is transmitted at high speed from the transmitter and received at the receiver end after being looped back on the load board or test board. At the receiver end, the sequence is analyzed to calculate the bit error rate (BER).

DC parametric tests are performed on the input and output pins, such as a continuity test and a leakage test, to ensure device functionality. To perform these tests, the input/output pins of the DUT must be connected directly to a DC instrument where the DC measurement of the input/output pin is executed.

The ADGM1121 offers both high speed digital and DC testing capability with superior density in a small 5.00 mm × 4.00 mm × 1.0 mm LGA package, as shown in Figure 61. The MEMS switch also enables communication from the tester to the device under test (DUT). The ADGM1121 provides excellent performance from DC to 16 GHz, which allows the switch to handle both high-speed signals up to 64 Gbps and precision DC signals.

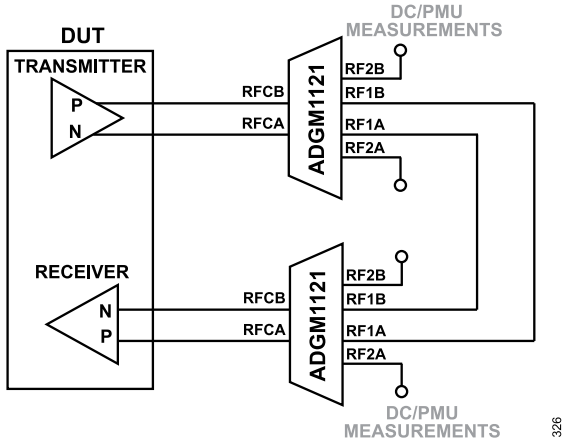

Figure 61. ADGM1121 Enabling Both High-Speed Digital and DC Testing

CRITICAL OPERATIONAL REQUIREMENTS

SYSTEM ERROR CONSIDERATIONS DUE TO ON-RESISTANCE DRIFT

The on-resistance (R_{ON}) performance of the ADGM1121 is affected by part-to-part variation, channel-to-channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes

In a 50 Ω system, the on-resistance drift over switch actuations (ΔR_{ON}) can introduce system inaccuracy. Figure 62 shows the ADGM1121 connected with the load in a 50 Ω system, where R_S is the source impedance. To calculate the system error caused by the ADGM1121 ΔR_{ON}, use the following equation:

System Error (%) = $\Delta R/R_{LOAD}$

where:

ΔR is the ADGM1121 ΔR_{ON}.

R_{LOAD} is the load impedance.

The ADGM1121 ΔR_{ON} also affects insertion loss, which must be considered when using the device. To calculate the on-resistance impact on insertion loss, use the following equation:

Insertion Loss = 10log (*1* + ($\Delta R/R_{LOAD}$))

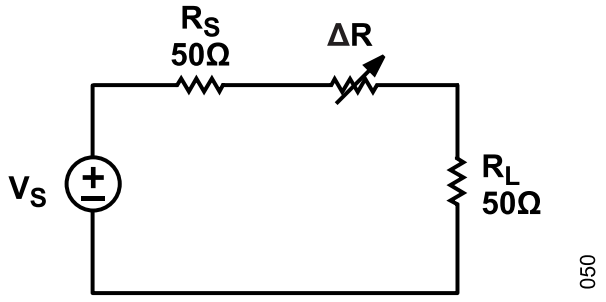

Figure 62. 50 Ω System Representation Where the ADGM1121 is Connected with the Load

Table 9. System Error and Insertion Loss Error Due to ADGM1121 R_{ON} Drift

On-Resistance Drift	System Error (%)	Insertion Loss Error (dB)
0.7	1.4	0.06
2	4	0.17

The ΔR_{ON} over time specification is -0.32 Ω (maximum) measured after 100 ms, as shown in Figure 13 to Figure 20. According to the plots, the R_{ON} drifts over time is −0.06 Ω (typical) after 100 ms. The R_{ON} of the ADGM1121 typically drifts by −0.04 Ω per decade. For example, after 100 ms, the R_{ON} drifts −0.06 Ω. After 1 s, the R_{ON} drifts −0.1 Ω. And after 10 s, it drifts −0.14 Ω. Therefore, after 1000 s, the R_{ON} is expected to drift by −0.22 Ω.

ON-RESISTANCE SHIFT DUE TO TEMPERATURE SHOCK POST ACTUATIONS

When the switch is actuated multiple times at one temperature, and if there is a sudden shift from this temperature, a large shift is shown in the switch R_{ON}. Figure 63 shows the absolute R_{ON} performance of the population of devices over different number of actuations. During this measurement, the switch is actuated at 85°C and the switch R_{ON} is measured at 25°C. Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for the ADGM1121 ΔR_{ON} over actuations.

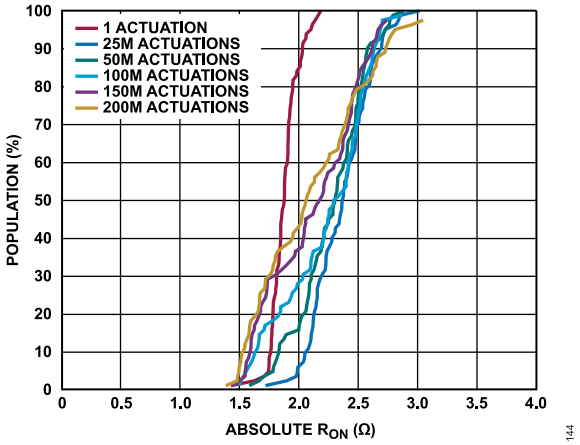

Figure 63. Population vs. Absolute R_{ON}, Switch Actuated at 85°C and R_{ON} Measured at 25°C, Actuation Frequency = 289 Hz, V_{DD} = 3.3 V

HOT SWITCHING

Hot switching occurs by cycling the switch on or off with an excessive voltage or current applied to the switch. The presence of the applied signal during the switching cycle damages the switch contacts. Hot switching damage is dependent on the current or the voltage levels. Hot switching causes a significant reduction in the cycle lifetime of the switch, as shown in Figure 67 and Figure 69. Figure 64 shows the hot switching condition when the switch is turned on with 1 V present at the switch terminal during switching. With a voltage across an off switch, damage can occur as the contact or switch closes.

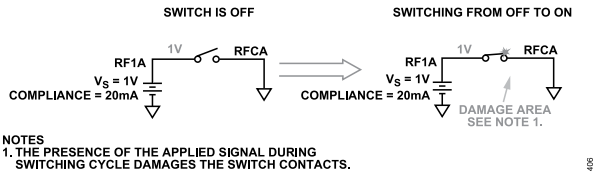

Figure 64. Hot Switching Condition When Turning the Switch from Off to On

Figure 65 shows the hot switching condition when the switch is turned off with 10 mA passing through the switch during switching. With current passing through an on switch, damage can occur as the contact or switch opens.

CRITICAL OPERATIONAL REQUIREMENTS

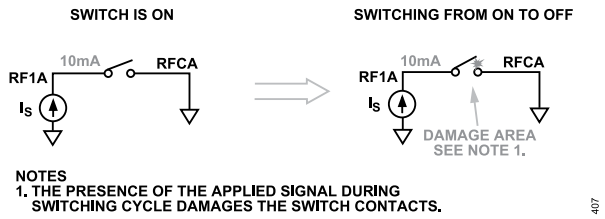

Figure 65. Hot Switching Condition When Turning the Switch from On to Off

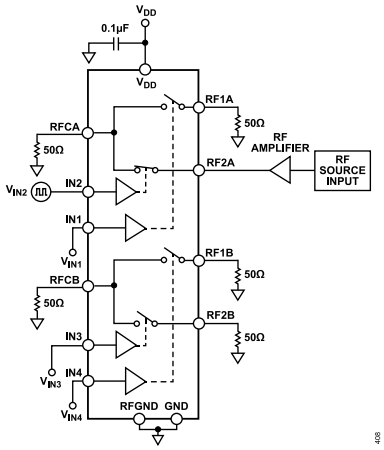

Figure 66. RF Hot Switching Setup

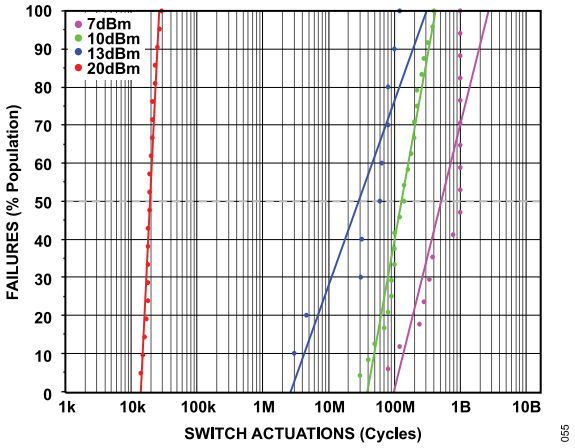

Figure 67. RF Hot Switching Probability Distribution on Log Normal (RF Power = Continuous Wave, Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V)

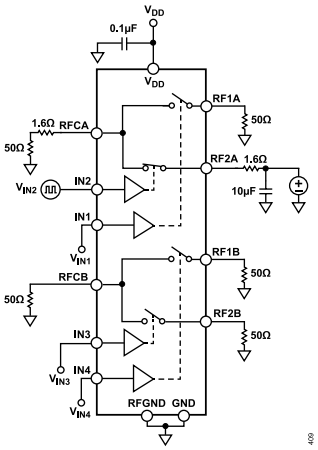

Figure 68. DC Hot Switching Setup

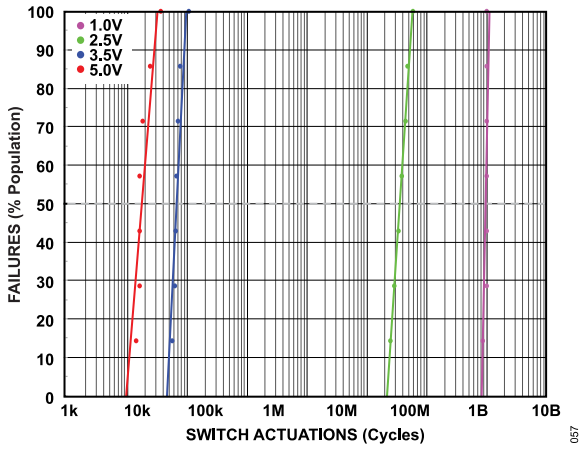

Figure 69. DC Hot Switching Probablity Distribution on Log Normal (Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V)

HANDLING PRECAUTIONS

ESD Precautions

All RF pins of the ADGM1121 pass the following ESD limits:

- 200 V, Class 0B HBM, ANSI/ESDA/JEDEC JS-001-2014
- 1 kV Class C3 FICDM ANSI/ESDA/JEDEC JS-002

All the RFx pins are rated to 1 kV FICDM, making the device safe for automated handling and assembly process. Standard ESD precautions should be taken during manufacturing.

200 V HBM rating of ADGM1121 is susceptible to ESD surge due to human body contact. ESD protection should be added if human body contact is expected.

CRITICAL OPERATIONAL REQUIREMENTS

Electrical Overstress (EOS) Precautions

ADGM1121 is susceptible to EOS. Therefore, observe the following precautions:

- The ADGM1121 is a ESD sensitive device. Observe all normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- Avoid running measurement instruments, such as digital multimeters (DMMs), in autorange modes. Some instruments can generate large transient compliance voltages when switching between ranges.
- Use the highest practical DMM range setting (the lowest resolution) for resistance measurements to minimize compliance voltages, particularly during switching.
- Coaxial cables can store charge and lead to EOS when directly connected to the switch. Discharge cables before connecting directly to the switch.
- Avoid connecting capacitive terminations directly to the switch, as shown in Figure 70. A shunt capacitor can store a charge that can potentially lead to hot switching events when the switch opens or closes, affecting the lifetime of the switch.

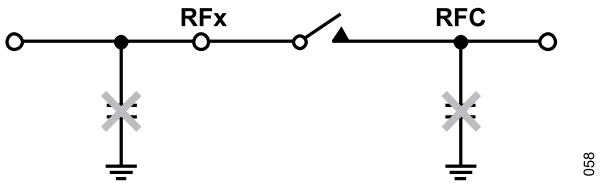

Figure 70. Avoid Large Capacitor Directly Connected to the Switch

Mechanical Shock Precautions

The ADGM1121 passes Group D mechanical shocks tests, as detailed in Absolute Maximum Ratings . These tests validate the robustness of the device to normal mechanical shocks.

The device should not be used if dropped. To reduce excessive mechanical shock and ESD events, avoid handling of loose devices, as outlined in Figure 71 .

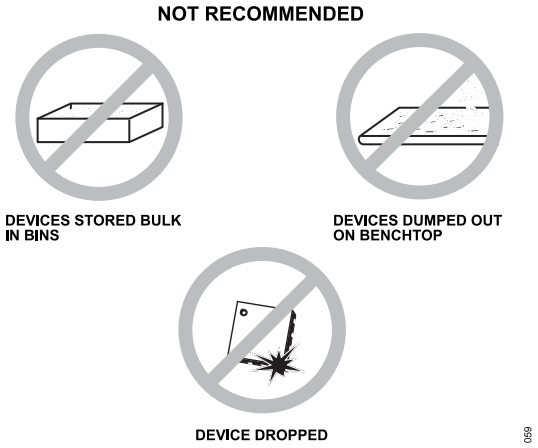

Figure 71. Situations to Avoid During Handling

REGISTER SUMMARY

Table 10. Register Summary

Register (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
0x20	SWITCH_DATA	INTERNAL_ERROR		RESERVED		SWITCH_DATA				0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x20, Reset: 0x00, Name: SWITCH_DATA

The switch data register controls the status of the two switches of the ADGM1121.

Table 11. Bit Descriptions for SWITCH_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	INTERNAL_ERROR		These bits determine if an internal error has occurred.	0x0	R
		00	No error detected		
		01	Error detected		
		10	Error detected		
		11	Error detected		
[5:4]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
3	SW4_EN		Enable bit for Switch 4.	0x0	R/W
		0	Switch RF1B open		
		1	Switch RF1B closed		
2	SW3_EN		Enable bit for Switch 3.	0x0	R/W
		0	Switch RF2B open		
		1	Switch RF2B closed		
1	SW2_EN		Enable bit for Switch 2.	0x0	R/W
		0	Switch RF2A open		
		1	Switch RF2A closed		
0	SW1_EN		Enable bit for Switch 1	0x0	R/W
		0	Switch RF1A open		
		1	Switch RF1A closed		

OUTLINE DIMENSIONS

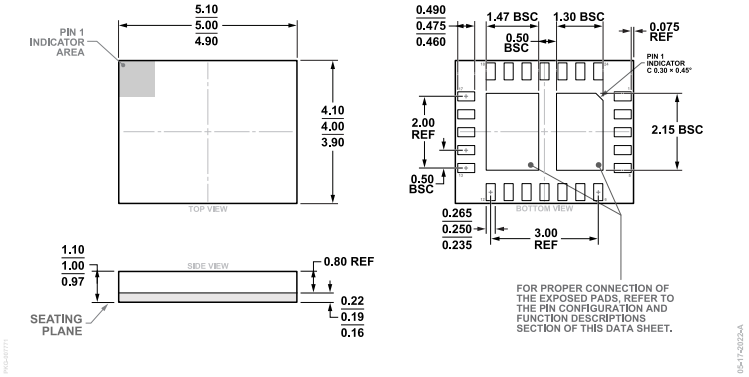

Figure 72. 24-Lead Land Grid Array [LGA] 5 mm × 4 mm Body and 1 mm Package Height (CC-24-11) Dimensions shown in millimeters

Updated: June 22, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADGM1121BCCZ-RL7	-40°C to +85°C	24-Terminal Land Grid Array [LGA]	Reel, 1000	CC-24-9

[1] Z = RoHS Compliant Part.

EVALUATION BOARD

Model[1]	Package Description
EVAL-ADGM1121SDZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

ADGM1121BCCZ ADGM1121BCCZ-RL7 EVAL-ADGM1121SDZ