

## 1.5 $\Omega$ $R_{ON}$ , Quad SPST Switch with 1.2 V and 1.8 V JEDEC Logic Compliance

### FEATURES

- ▶ 1.5  $\Omega$  on resistance for  $\pm 15$  V dual supply at 25°C
- ▶ 0.3  $\Omega$  on-resistance flatness for  $\pm 15$  V dual supply at 25°C
- ▶ 0.1  $\Omega$  on-resistance match between channels for  $\pm 15$  V dual supply at 25°C
- ▶ Fully specified at  $\pm 15$  V, +12 V,  $\pm 5$  V
  - ▶  $\pm 4.5$  V to  $\pm 16.5$  V dual-supply operation
  - ▶ 5 V to 16.5 V single-supply operation
- ▶  $V_L$  supply for low logic-level compatibility
  - ▶ 1.8 V JEDEC standard compliant (JESD8-7A)
  - ▶ 1.2 V JEDEC standard compliant (JESD8-12A.01)
- ▶ Rail-to-rail operation
- ▶ 24-lead, 4 mm  $\times$  4 mm LFCSP

### APPLICATIONS

- ▶ Automated test equipment
- ▶ Data-acquisition systems
- ▶ Battery-powered systems
- ▶ Sample-and-hold systems
- ▶ FPGA and microcontroller systems
- ▶ Audio signal routing
- ▶ Video signal routing
- ▶ Communications systems
- ▶ Relay replacement

### GENERAL DESCRIPTION

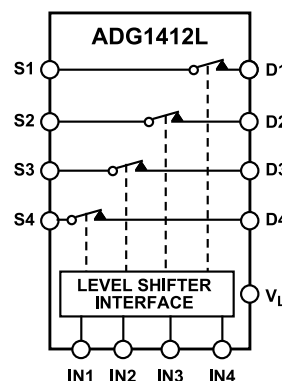
The ADG1412L is a monolithic complementary metal-oxide semiconductor (CMOS) device containing four independently selectable switches designed on an iCMOS<sup>®</sup> process. Industrial CMOS (iCMOS) is a modular manufacturing process combining high voltage CMOS and bipolar technologies.

The on-resistance profile is flat over the full analog input range, ensuring excellent linearity and low distortion (1.5  $\Omega$  typical) when switching signals.

The ADG1412L contains four independent SPST switches, and these switches are turned on with Logic 1. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

An external  $V_L$  supply provides flexibility for lower logic control. The ADG1412L is both 1.2 V and 1.8 V JEDEC standard compliant.

### FUNCTIONAL BLOCK DIAGRAM



NOTES  
 1. SWITCHES SHOWN FOR A 1 INPUT LOGIC. 001

Figure 1. Functional Block Diagram

### PRODUCT HIGHLIGHTS

1. 2.6  $\Omega$  maximum on resistance over temperature.
2. Minimum distortion.
3.  $V_L$  supply for low logic-level compatibility.
4. JEDEC standard compliant for both 1.2 V and 1.8 V logic levels.
5. Guaranteed switch off when digital inputs are floating.
6. 24-lead, 4 mm  $\times$  4 mm LFCSP.

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**REVISION HISTORY****8/2022—Revision 0: Initial Version**

## SPECIFICATIONS

## OPERATING SUPPLY VOLTAGES

Table 1. Operating Supply Voltages

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
Dual	±4.5		±16.5	V	$V_{DD}$ to $V_{SS}$
Single	5		16.5	V	$V_{DD}$ to GND, $V_{SS} = \text{GND} = 0 \text{ V}$
DIGITAL VOLTAGE					
Single	1.1		1.3	V	$V_L$ to GND, $I_{NX}$ voltage ( $V_{INX}$ ) = 1.2 V logic
	1.65		1.95	V	$V_L$ to GND, $V_{INX} = 1.8 \text{ V logic}$

## ±15 V DUAL SUPPLY

$V_{DD} = 15 \text{ V} \pm 10\%$ ,  $V_{SS} = -15 \text{ V} \pm 10\%$ ,  $\text{GND} = 0 \text{ V}$ , and  $V_L = 1.1 \text{ V}$  to  $1.95 \text{ V}$ , unless otherwise noted.

Table 2. ±15 V Dual Supply

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	1.5			$\Omega$ typ	Source voltage ( $V_S$ ) = $\pm 10 \text{ V}$ , source current ( $I_S$ ) = -10 mA, see <a href="#">Figure 26</a>
	1.8	2.3	2.6	$\Omega$ max	$V_{DD} = +13.5 \text{ V}$ , $V_{SS} = -13.5 \text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.1			$\Omega$ typ	$V_S = \pm 10 \text{ V}$ , $I_S = -10 \text{ mA}$
	0.18	0.19	0.21	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.3			$\Omega$ typ	$V_S = \pm 10 \text{ V}$ , $I_S = -10 \text{ mA}$
	0.36	0.4	0.45	$\Omega$ max	
LEAKAGE CURRENTS					$V_{DD} = +16.5 \text{ V}$ , $V_{SS} = -16.5 \text{ V}$
Source Off Leakage, $I_S$ (Off)	±0.03			nA typ	$V_S = \pm 10 \text{ V}$ , drain voltage ( $V_D$ ) = $\mp 10 \text{ V}$ , see <a href="#">Figure 27</a>
	±0.55	±2	±12.5	nA max	
Drain Off Leakage, $I_D$ (Off)	±0.03			nA typ	$V_S = \pm 10 \text{ V}$ , $V_D = \mp 10 \text{ V}$ , see <a href="#">Figure 27</a>
	±0.55	±2	±12.5	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	±0.15			nA typ	$V_S = V_D = \pm 10 \text{ V}$ , see <a href="#">Figure 28</a>
	±2	±4	±30	nA max	
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			$0.65 \times V_L$	V min	
Input Low Voltage, $V_{INL}$			$0.35 \times V_L$	V max	
Input High Current, $I_{INH}$	55			$\mu\text{A typ}$	$V_{INX} = V_L = 1.8 \text{ V}$ , see the <a href="#">Theory of Operation</a> section
			90	$\mu\text{A max}$	
	40			$\mu\text{A typ}$	$V_{INX} = V_L = 1.2 \text{ V}$ , see the <a href="#">Theory of Operation</a> section
			65	$\mu\text{A max}$	
Input Low Current, $I_{INL}$	0.2			$\mu\text{A typ}$	$V_{INX} = 0 \text{ V}$
			0.8	$\mu\text{A max}$	
Digital-Input Capacitance, $C_{IN}$	5			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, $t_{ON}$ <sup>1</sup>	110			ns typ	Load resistance ( $R_L$ ) = 300 $\Omega$ , load capacitance ( $C_L$ ) = 35 pF
	133	152	167	ns max	$V_S = 10 \text{ V}$ , see <a href="#">Figure 33</a>
Off Time, $t_{OFF}$ <sup>1</sup>	161			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	200	225	245	ns max	$V_S = 10 \text{ V}$ , see <a href="#">Figure 33</a>
Charge Injection, $Q_{INJ}$	-20			pC typ	$V_S = 0 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see <a href="#">Figure 34</a>

## SPECIFICATIONS

Table 2.  $\pm 15$  V Dual Supply

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	-76			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , frequency = 100 kHz, see Figure 29
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , frequency = 1 MHz, see Figure 30
Total Harmonic Distortion, THD	-101			dB typ	$R_L = 10\ \text{k}\Omega$ , 20 V p-p, frequency = 20 kHz, see Figure 32
	-89			dB typ	$R_L = 10\ \text{k}\Omega$ , 20 V p-p, frequency = 100 kHz, see Figure 32
Total Harmonic Distortion + Noise, THD + N	0.004			% typ	$R_L = 10\ \text{k}\Omega$ , 20 V p-p, frequency = 100 kHz, see Figure 32
-3 dB Bandwidth	170			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , see Figure 31
Insertion Loss	-0.2			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , frequency = 1 MHz, see Figure 31
Source Off Capacitance, $C_S$ (Off)	22			pF typ	$V_S = 0\ \text{V}$ , frequency = 1 MHz
Drain Off Capacitance, $C_D$ (Off)	23			pF typ	$V_S = 0\ \text{V}$ , frequency = 1 MHz
Drain On Capacitance, $C_D$ (On), Source On Capacitance, $C_S$ (On)	113			pF typ	$V_S = 0\ \text{V}$ , frequency = 1 MHz
POWER REQUIREMENTS					
Positive Supply Current, $I_{DD}$	55		95	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +16.5\ \text{V}$ , $V_{SS} = -16.5\ \text{V}$ Digital inputs = 0 V or $V_{VL}$
Negative Supply Current, $I_{SS}$	0.01		1	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 0 V or $V_{VL}$
Digital Supply Current, $I_{VL}$	45		70	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{INx} = V_L = 1.8\ \text{V}$
	30		55	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{INx} = V_L = 1.2\ \text{V}$

<sup>1</sup> A minimum 50  $\mu\text{s}$  initialization time is required before applying an  $INx$  input. See the Theory of Operation section.

**+12 V SINGLE SUPPLY**

$V_{DD} = 12\ \text{V} \pm 10\%$ ,  $V_{SS} = 0\ \text{V}$ ,  $GND = 0\ \text{V}$ , and  $V_L = 1.1\ \text{V}$  to  $1.95\ \text{V}$ , unless otherwise noted.

Table 3. +12 V Single Supply

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	2.8			$\Omega$ typ	$V_S = 0\ \text{V}$ to 10 V, $I_S = -10\ \text{mA}$ , see Figure 26
	3.5	4.3	4.8	$\Omega$ max	$V_{DD} = 10.8\ \text{V}$ , $V_{SS} = 0\ \text{V}$
On-Resistance Match	0.13			$\Omega$ typ	$V_S = 0\ \text{V}$ to 10 V, $I_S = -10\ \text{mA}$
Between Channels, $\Delta R_{ON}$					
	0.21	0.23	0.25	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.6			$\Omega$ typ	$V_S = 0\ \text{V}$ to 10 V, $I_S = -10\ \text{mA}$
	1.1	1.2	1.3	$\Omega$ max	
LEAKAGE CURRENTS					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = 10.8\ \text{V}$ , $V_{SS} = 0\ \text{V}$
	$\pm 0.55$	$\pm 2$	$\pm 12.5$	nA max	$V_S = 1\ \text{V}/10\ \text{V}$ , $V_D = 10\ \text{V}/0\ \text{V}$ , see Figure 27
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = 1\ \text{V}/10\ \text{V}$ , $V_D = 10\ \text{V}/0\ \text{V}$ , see Figure 27
	$\pm 0.55$	$\pm 2$	$\pm 12.5$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.15$			nA typ	$V_S = V_D = 1\ \text{V}/10\ \text{V}$ , see Figure 28
	$\pm 1.5$	$\pm 4$	$\pm 30$	nA max	
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			$0.65 \times V_L$	V min	
Input Low Voltage, $V_{INL}$			$0.35 \times V_L$	V max	
Input High Current, $I_{INH}$	55			$\mu\text{A}$ typ	$V_{INx} = V_L = 1.8\ \text{V}$ , see the Theory of Operation section

## SPECIFICATIONS

Table 3. +12 V Single Supply

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Input Low Current, $I_{INL}$			90	$\mu\text{A max}$	$V_{INx} = V_L = 1.2\text{ V}$ , see the <a href="#">Theory of Operation</a> section
	40			$\mu\text{A typ}$	
			65	$\mu\text{A max}$	$V_{INx} = 0\text{ V}$
	0.2			$\mu\text{A typ}$	
			0.8	$\mu\text{A max}$	
Digital-Input Capacitance, $C_{IN}$	5			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, $t_{ON}$ <sup>1</sup>	182	269	300	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	225			ns max	$V_S = 8\text{ V}$ , see <a href="#">Figure 33</a>
Off Time, $t_{OFF}$ <sup>1</sup>	175	262	295	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	230			ns max	$V_S = 8\text{ V}$ , see <a href="#">Figure 33</a>
Charge Injection, $Q_{INJ}$	10			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see <a href="#">Figure 34</a>
Off Isolation	-76			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , frequency = 100 kHz, see <a href="#">Figure 29</a>
Channel-to-Channel Crosstalk	-100			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , frequency = 1 MHz, see <a href="#">Figure 30</a>
Total Harmonic Distortion, THD	-87			dB typ	$R_L = 10\text{ k}\Omega$ , 9 V p-p, frequency = 20 kHz, see <a href="#">Figure 32</a>
	-83			dB typ	$R_L = 10\text{ k}\Omega$ , 9 V p-p, frequency = 100 kHz, see <a href="#">Figure 32</a>
Total Harmonic Distortion + Noise, THD + N	0.007			% typ	$R_L = 10\text{ k}\Omega$ , 9 V p-p, frequency = 100 kHz, see <a href="#">Figure 32</a>
-3 dB Bandwidth	130			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see <a href="#">Figure 31</a>
Insertion Loss	-0.3			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , frequency = 1 MHz, see <a href="#">Figure 31</a>
Source Off Capacitance, $C_S$ (Off)	29			pF typ	$V_S = 6\text{ V}$ , frequency = 1 MHz
Drain Off Capacitance, $C_D$ (Off)	30			pF typ	$V_S = 6\text{ V}$ , frequency = 1 MHz
Drain On Capacitance, $C_D$ (On), Source On Capacitance, $C_S$ (On)	116			pF typ	$V_S = 6\text{ V}$ , frequency = 1 MHz
POWER REQUIREMENTS					
Positive Supply Current, $I_{DD}$	55			$\mu\text{A typ}$	$V_{DD} = 13.2\text{ V}$
			95	$\mu\text{A max}$	Digital inputs = 0 V or $V_{VL}$
Digital Supply Current, $I_{VL}$	45			$\mu\text{A typ}$	$V_{INx} = V_L = 1.8\text{ V}$
			70	$\mu\text{A max}$	
	30			$\mu\text{A typ}$	$V_{INx} = V_L = 1.2\text{ V}$
			55	$\mu\text{A max}$	

<sup>1</sup> A minimum 50  $\mu\text{s}$  initialization time is required before applying an INx input. See the [Theory of Operation](#) section.

**±5 V DUAL SUPPLY**

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ , GND = 0 V, and  $V_L = 1.1\text{ V}$  to 1.95 V, unless otherwise noted.

Table 4. ±5 V Dual Supply

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V <sub>DD</sub> to V <sub>SS</sub>	V	
On Resistance, R <sub>ON</sub>	3.3	4.9	5.4	Ω typ	V <sub>S</sub> = ±4.5 V, I <sub>S</sub> = -10 mA, see <a href="#">Figure 26</a>
	4			Ω max	V <sub>DD</sub> = +4.5 V, V <sub>SS</sub> = -4.5 V
On-Resistance Match Between Channels, ΔR <sub>ON</sub>	0.13			Ω typ	V <sub>S</sub> = ±4.5 V, I <sub>S</sub> = -10 mA
On-Resistance Flatness, R <sub>FLAT(ON)</sub>	0.22	0.23	0.25	Ω max	V <sub>S</sub> = ±4.5 V, I <sub>S</sub> = -10 mA
	0.9			Ω typ	
		1.1	1.24	1.31	
LEAKAGE CURRENTS					
Source Off Leakage, I <sub>S</sub> (Off)	±0.03			nA typ	V <sub>DD</sub> = +5.5 V, V <sub>SS</sub> = -5.5 V
					V <sub>S</sub> = ±4.5 V, V <sub>D</sub> = ∓4.5 V, see <a href="#">Figure 27</a>

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Table 4.  $\pm 5$  V Dual Supply

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Drain Off Leakage, I <sub>D</sub> (Off)	±0.55	±2	±12.5	nA max	V <sub>S</sub> = ±4.5 V, V <sub>D</sub> = ∓4.5 V, see <a href="#">Figure 27</a>
	±0.03			nA typ	
Channel On Leakage, I <sub>D</sub> , I <sub>S</sub> (On)	±0.55	±2	±12.5	nA max	V <sub>S</sub> = V <sub>D</sub> = ±4.5 V, see <a href="#">Figure 28</a>
	±0.05			nA typ	
	±1.0			±4	
DIGITAL INPUTS					
Input High Voltage, V <sub>INH</sub>	55		0.65 × V <sub>L</sub>	V min	V <sub>INX</sub> = V <sub>L</sub> = 1.8 V, see the <a href="#">Theory of Operation</a> section
Input Low Voltage, V <sub>INL</sub>			0.35 × V <sub>L</sub>	V max	
Input High Current, I <sub>INH</sub>			90	μA typ	
			40	μA max	
			65	μA typ	V <sub>INX</sub> = V <sub>L</sub> = 1.2 V, see the <a href="#">Theory of Operation</a> section
				μA max	
Input Low Current, I <sub>INL</sub>	0.2			μA typ	V <sub>INX</sub> = 0 V
			0.8	μA max	
Digital-Input Capacitance, C <sub>IN</sub>	5			pF typ	
DYNAMIC CHARACTERISTICS					
On Time, t <sub>ON</sub> <sup>1</sup>	252	388	432	ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	333			ns max	V <sub>S</sub> = 3 V, see <a href="#">Figure 33</a>
Off Time, t <sub>OFF</sub> <sup>1</sup>	256	391	422	ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	345			ns max	V <sub>S</sub> = 3 V, see <a href="#">Figure 33</a>
Charge Injection, Q <sub>INJ</sub>	10			pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF, see <a href="#">Figure 34</a>
Off Isolation	-76			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, frequency = 100 kHz, see <a href="#">Figure 29</a>
Channel-to-Channel Crosstalk	-100			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, frequency = 1 MHz, see <a href="#">Figure 30</a>
Total Harmonic Distortion, THD	-90			dB typ	R <sub>L</sub> = 10 kΩ, 10 V p-p, frequency = 20 kHz, see <a href="#">Figure 32</a>
	-78			dB typ	R <sub>L</sub> = 10 kΩ, 10 V p-p, frequency = 100 kHz, see <a href="#">Figure 32</a>
Total Harmonic Distortion + Noise, THD + N	0.02			% typ	R <sub>L</sub> = 10 kΩ, 10 V p-p, frequency = 100 kHz, see <a href="#">Figure 32</a>
-3 dB Bandwidth	130			MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see <a href="#">Figure 31</a>
Insertion Loss	-0.3			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, frequency = 1 MHz, see <a href="#">Figure 31</a>
Source Off Capacitance, C <sub>S</sub> (Off)	32			pF typ	V <sub>S</sub> = 0 V, frequency = 1 MHz
Source Off Capacitance, C <sub>D</sub> (Off)	33			pF typ	V <sub>S</sub> = 0 V, frequency = 1 MHz
Drain On Capacitance, C <sub>D</sub> (On), Source On Capacitance, C <sub>S</sub> (On)	116			pF typ	V <sub>S</sub> = 0 V, frequency = 1 MHz
POWER REQUIREMENTS					
Positive Supply Current, I <sub>DD</sub>	50		90	μA typ	V <sub>DD</sub> = +5.5 V, V <sub>SS</sub> = -5.5 V
			μA max	Digital inputs = 0 V or V <sub>VL</sub>	
Negative Supply Current, I <sub>SS</sub>	0.01		μA typ	Digital inputs = 0 V or V <sub>VL</sub>	
			μA max		
Digital Supply Current, I <sub>VL</sub>	45		1.0	μA typ	V <sub>INX</sub> = V <sub>L</sub> = 1.8 V
			70	μA max	
	30			μA typ	V <sub>INX</sub> = V <sub>L</sub> = 1.2 V
			55	μA max	

<sup>1</sup> A minimum 50  $\mu$ s initialization time is required before applying an INx input. See the [Theory of Operation](#) section.

## SPECIFICATIONS

## CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 5. Four Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx <sup>1</sup> ( $\theta_{JA} = 45^{\circ}\text{C/W.}$ )				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	321	174	80	mA maximum
$V_{DD} = +5\text{ V}, V_{SS} = -5\text{ V}$	242	143	74	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	260	150	76	mA maximum

<sup>1</sup> Sx refer to S1 to S4 pins, and Dx refers to the D1 to D4 pins.

Table 6. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx <sup>1</sup> ( $\theta_{JA} = 45^{\circ}\text{C/W.}$ )				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	572	244	88	mA maximum
$V_{DD} = +5\text{ V}, V_{SS} = -5\text{ V}$	436	211	85	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	467	220	86	mA maximum

<sup>1</sup> Sx refer to S1 to S4 pins, and Dx refers to the D1 to D4 pins.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 7. Absolute Maximum Ratings**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	−0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to −25 V
$V_I$ to GND	−0.3 V to +2.25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs <sup>2</sup>	GND − 0.3 V to 2.25 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins <sup>3</sup>	650 mA (pulsed at 1 ms, 10% duty-cycle maximum)
Continuous Current, Sx or Dx Pins <sup>3</sup>	Data + 15% <sup>4</sup>
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

<sup>1</sup> Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Current must be limited to the maximum ratings given.

<sup>2</sup> Overvoltages at the INx digital-input pins are clamped by internal diodes.

<sup>3</sup> Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

<sup>4</sup> See Table 5 and Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and  $\theta_{JC}$  is the junction-to-case thermal resistance.

**Table 8. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
CP-24-17 <sup>1</sup>	45	4.62	°C/W

<sup>1</sup> Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for ADG1412L

**Table 9. ADG1412L, 24-Lead LFCSP**

ESD Model	Withstand Threshold (V)	Class
HBM <sup>1</sup>	±2000	2
FICDM	±1250	C3

<sup>1</sup> For the input and output port to the supplies, the input and output port to the input and output port, and all other inputs.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

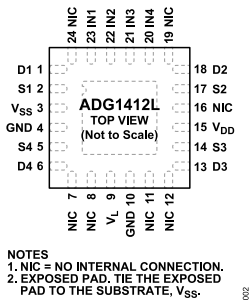


Figure 2. Pin Configuration

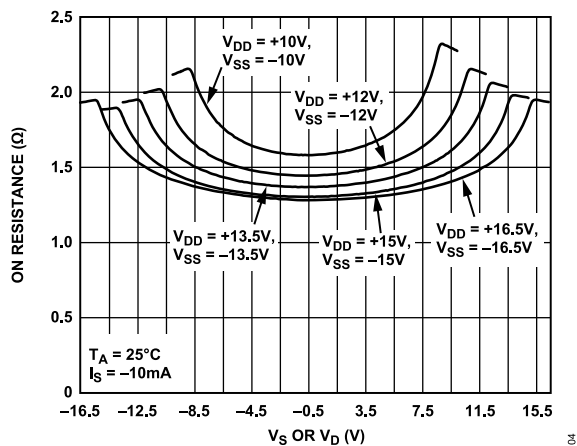
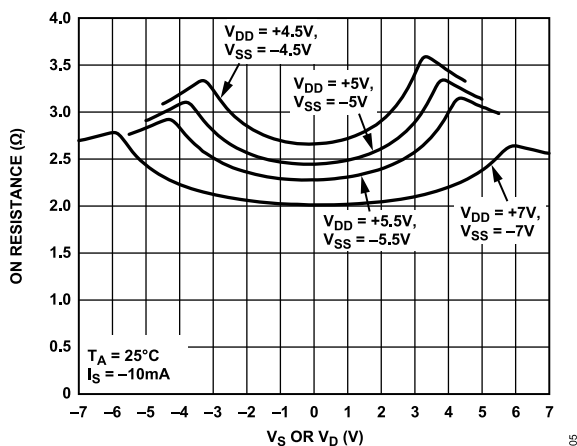
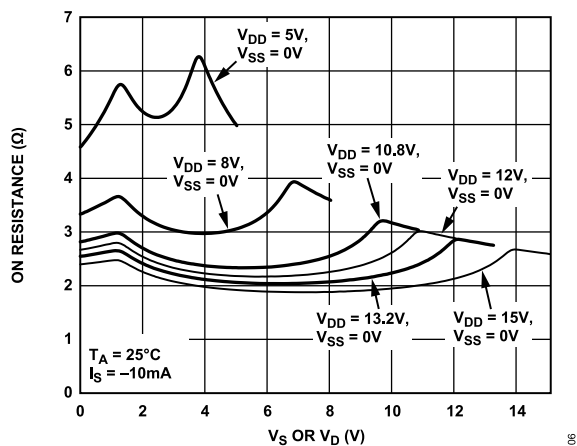
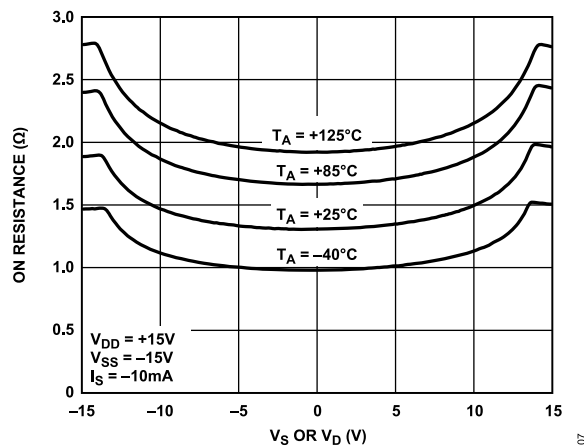
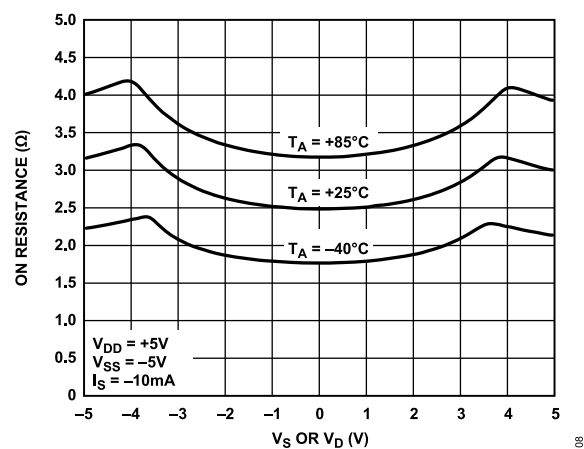
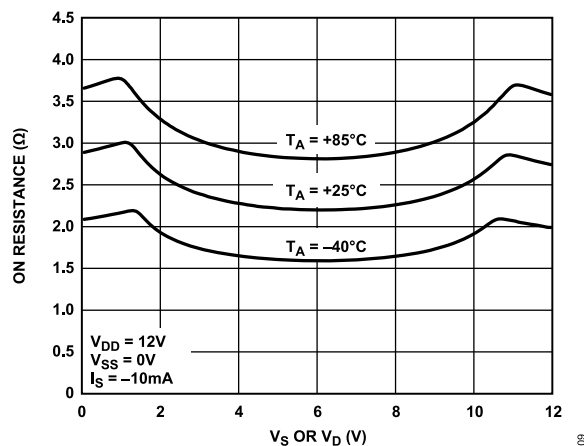
Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal. The D1 pin can be an input or output.
2	S1	Source Terminal. The S1 pin can be an input or output.
3	$V_{SS}$	Most Negative Power-Supply Potential.
4, 10	GND	Ground (0 V) Reference. The GND pins must be tied together.
5	S4	Source Terminal. The S4 pin can be an input or output.
6	D4	Drain Terminal. The D4 pin can be an input or output.
7, 8, 11, 12, 16, 19, 24	NIC	No Internal Connection. This pin is not connected internally.
9	$V_L$	Logic Power-Supply Potential.
13	D3	Drain Terminal. The D3 pin can be an input or output.
14	S3	Source Terminal. The S3 pin can be an input or output.
15	$V_{DD}$	Most Positive Power-Supply Potential.
17	S2	Source Terminal. The S2 pin can be an input or output.
18	D2	Drain Terminal. The D2 pin can be an input or output.
20	IN4	Logic Control Input.
21	IN3	Logic Control Input.
22	IN2	Logic Control Input.
23	IN1	Logic Control Input.
	EPAD	Exposed Pad. Tie the exposed pad to the substrate, $V_{SS}$ .

Table 11. ADG1412L Truth Table

INx	Switch Condition
0	Off
1	On

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. On Resistance vs.  $V_D$  or  $V_S$ , Dual SupplyFigure 4. On Resistance vs.  $V_D$  or  $V_S$ , Dual SupplyFigure 5. On Resistance vs.  $V_D$  or  $V_S$ , Single SupplyFigure 6. On Resistance vs.  $V_D$  or  $V_S$  for Different Temperatures,  $\pm 15$  V Dual SupplyFigure 7. On Resistance vs.  $V_D$  or  $V_S$  for Different Temperatures,  $\pm 5$  V Dual SupplyFigure 8. On Resistance vs.  $V_D$  or  $V_S$  for Different Temperatures, +12 V Single Supply

## TYPICAL PERFORMANCE CHARACTERISTICS

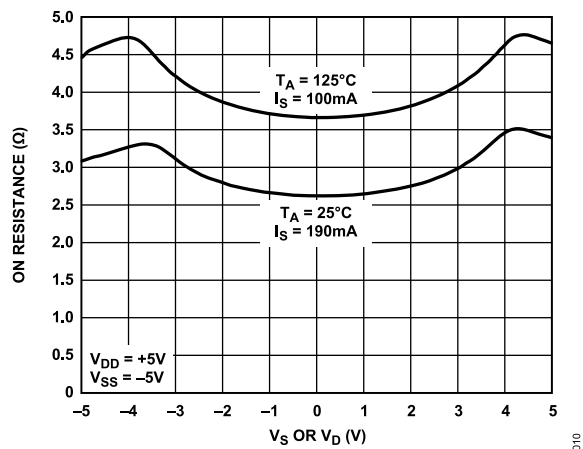
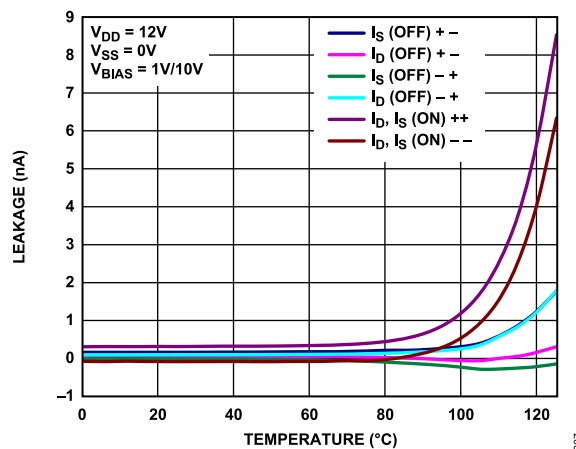
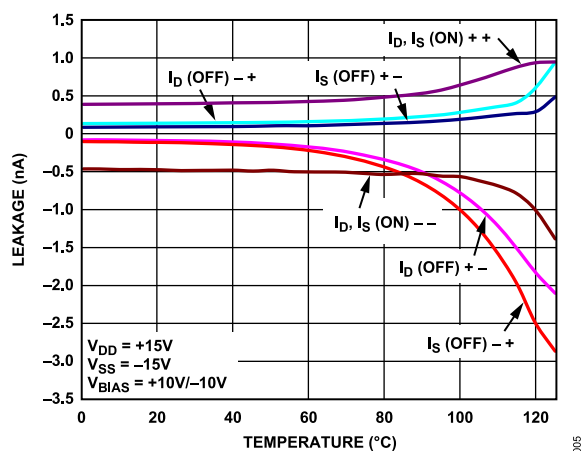
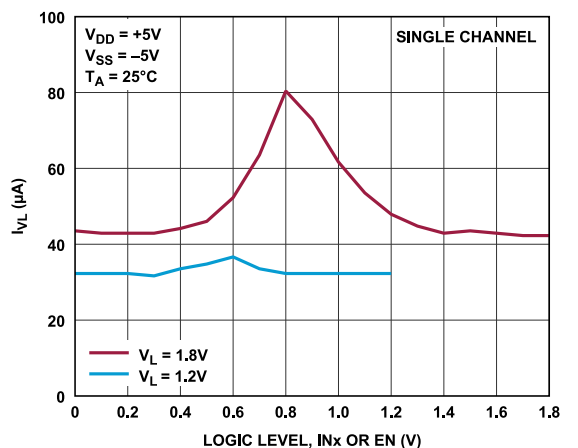
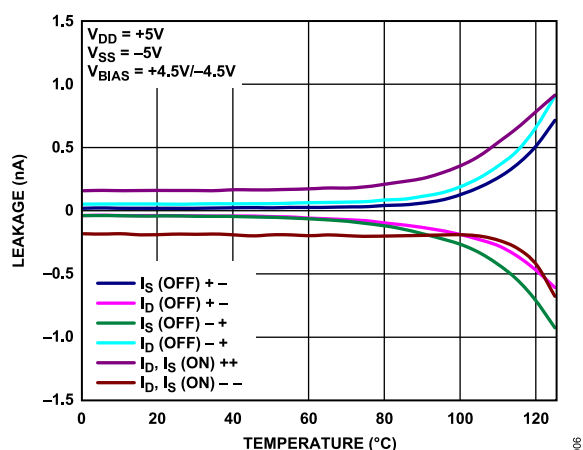
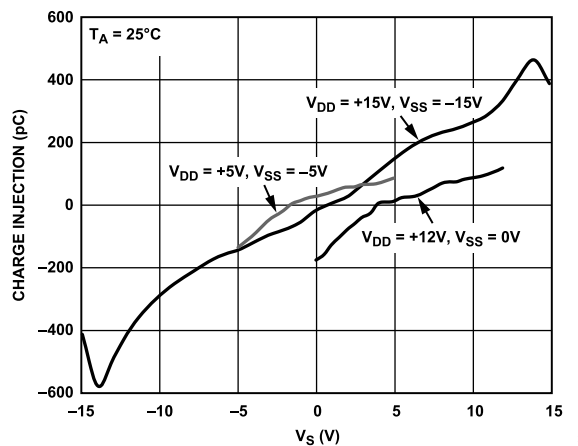
Figure 9. On Resistance vs.  $V_D$  or  $V_S$  for Different Current Levels,  $\pm 5$  V Dual Supply

Figure 12. Leakage Currents vs. Temperature, 12 V Single Supply

Figure 10. Leakage Currents vs. Temperature,  $\pm 15$  V Dual SupplyFigure 13.  $I_{VL}$  vs. Logic LevelFigure 11. Leakage Currents vs. Temperature,  $\pm 5$  V Dual SupplyFigure 14. Charge Injection vs.  $V_S$

## TYPICAL PERFORMANCE CHARACTERISTICS

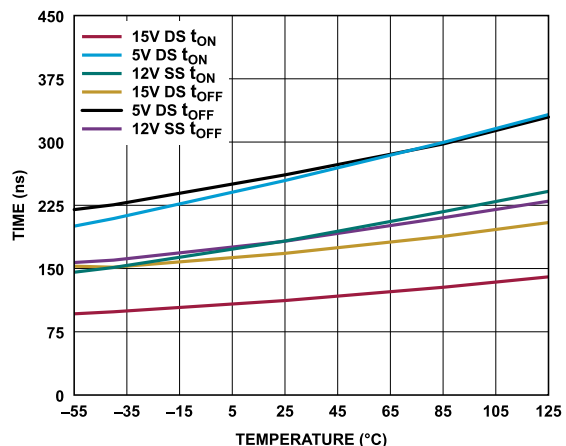


Figure 15.  $t_{ON}/t_{OFF}$  Time vs. Temperature for Single Supply (SS) and Dual Supply (DS)

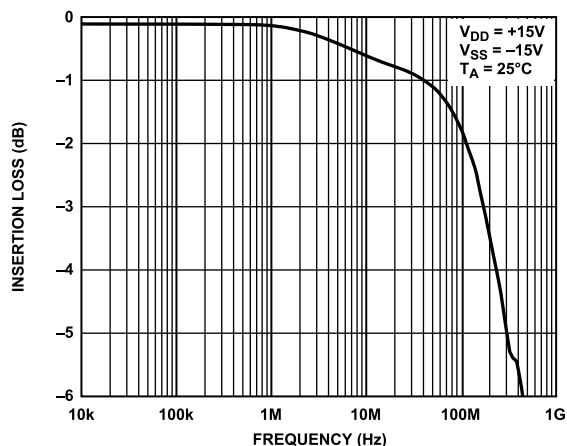


Figure 18. Insertion Loss vs. Frequency,  $\pm 15$  V Dual Supply

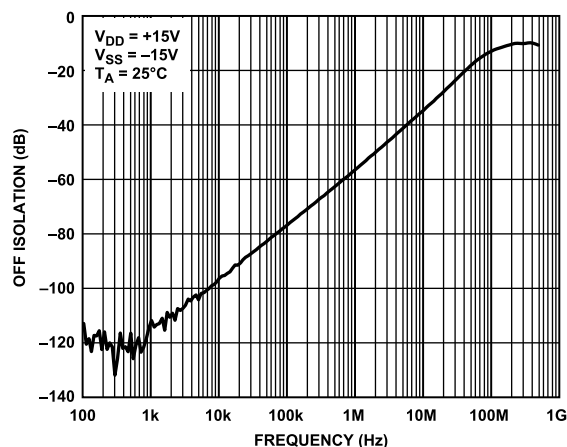


Figure 16. Off Isolation vs. Frequency,  $\pm 15$  V Dual Supply

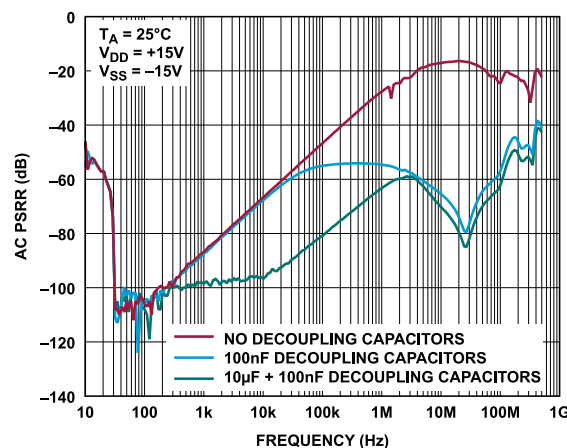


Figure 19. AC PSRR vs. Frequency,  $\pm 15$  V Dual Supply

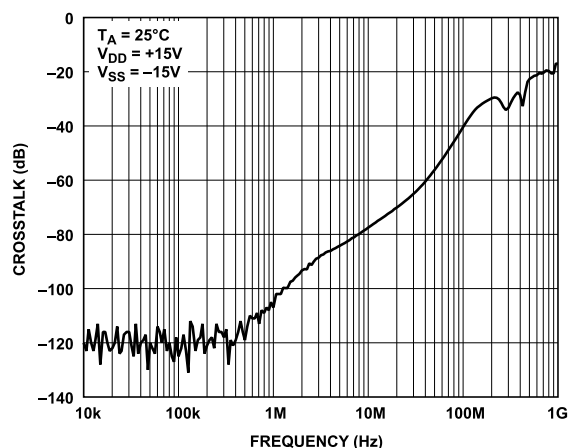


Figure 17. Crosstalk vs. Frequency,  $\pm 15$  V Dual Supply

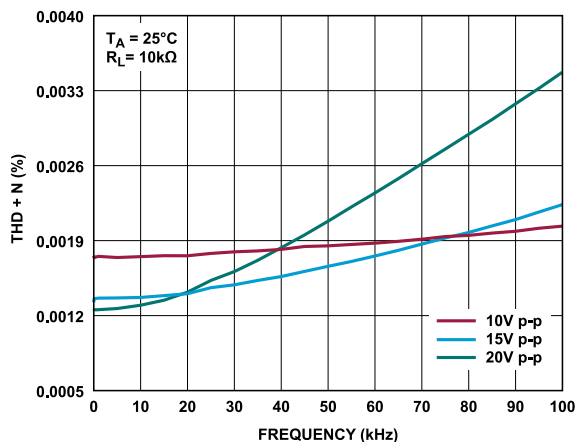


Figure 20. THD + N vs. Frequency,  $\pm 15$  V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

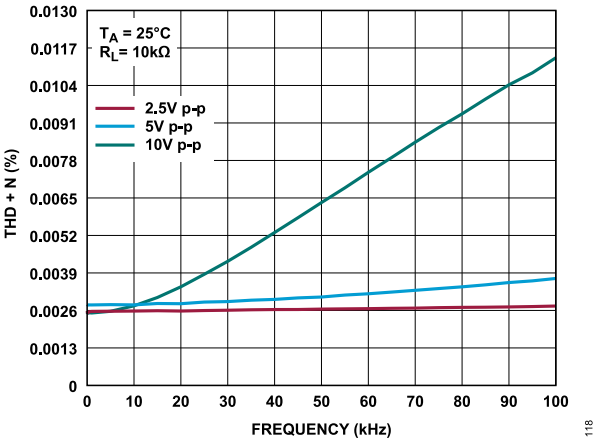


Figure 21. THD + N vs. Frequency,  $\pm 5$  V Dual Supply

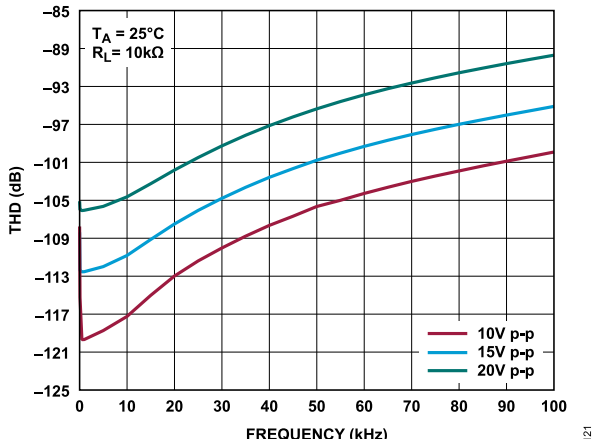


Figure 24. THD vs. Frequency,  $\pm 15$  V Dual Supply

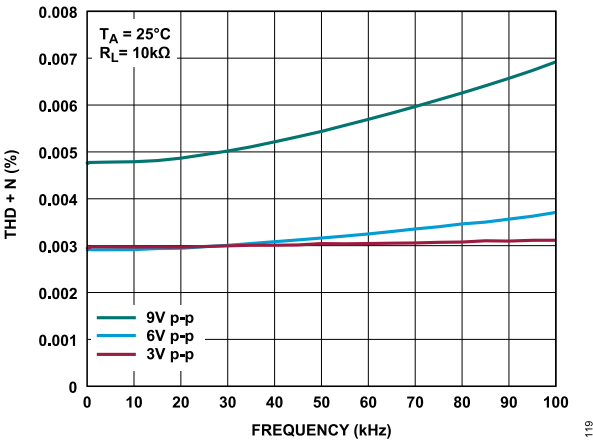


Figure 22. THD + N vs. Frequency, +12 V Single Supply

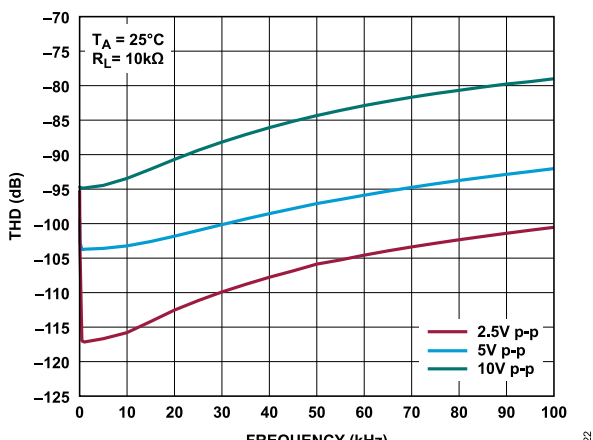


Figure 25. THD vs. Frequency,  $\pm 5$  V Dual Supply

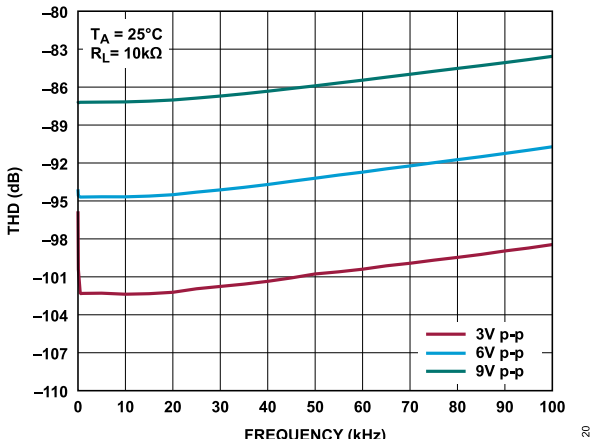


Figure 23. THD vs. Frequency, +12 V Single Supply

## TEST CIRCUITS

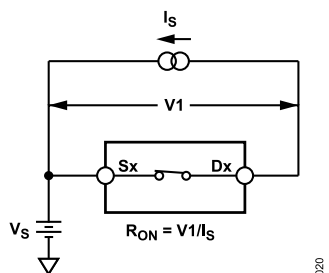


Figure 26. On Resistance

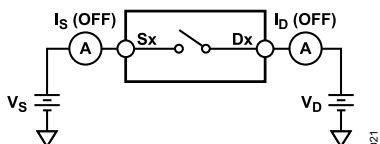


Figure 27. Off Leakage

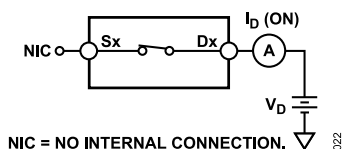


Figure 28. On Leakage

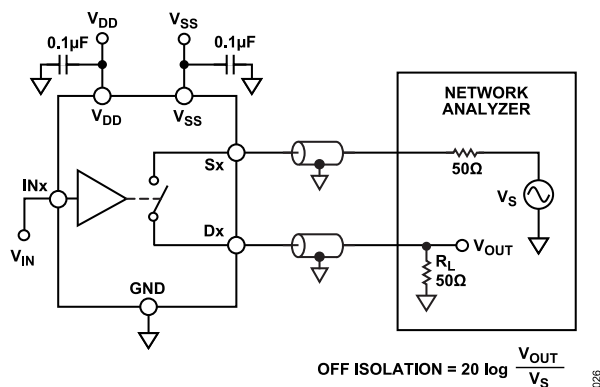


Figure 29. Off Isolation

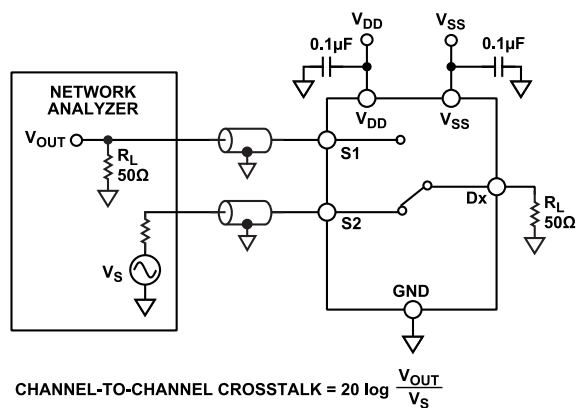


Figure 30. Channel-to-Channel Crosstalk

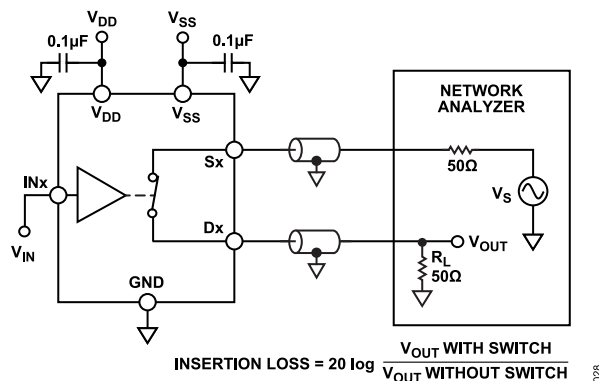


Figure 31. Bandwidth

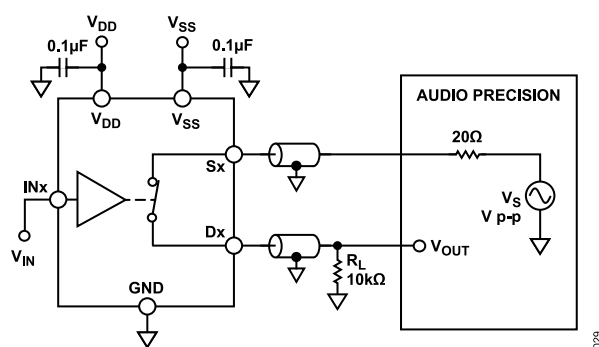


Figure 32. THD + Noise

## TEST CIRCUITS

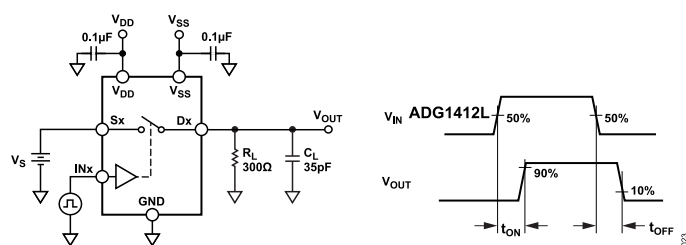


Figure 33. Switching Times

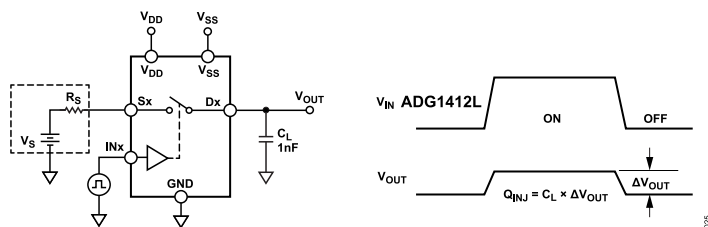


Figure 34. Charge Injection

## TERMINOLOGY

**I<sub>DD</sub>**

The positive supply current.

**I<sub>SS</sub>**

The negative supply current.

**I<sub>VL</sub>**

The digital supply current.

**V<sub>D</sub> and V<sub>S</sub>**

The analog voltage on Terminal D and Terminal S.

**R<sub>ON</sub>**

The ohmic resistance between Terminal D and Terminal S.

**R<sub>FLAT(ON)</sub>**

The difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

**ΔR<sub>ON</sub>**

The difference between the R<sub>ON</sub> of any two channels.

**I<sub>S</sub> Off**

The source leakage current with the switch off.

**I<sub>D</sub> Off**

The drain leakage current with the switch off.

**I<sub>D</sub> I<sub>S</sub> On**

The channel leakage current with the switch on.

**V<sub>D</sub> AND V<sub>S</sub>**

Analog voltages on Terminal D and Terminal S.

**V<sub>INL</sub>**

The maximum input voltage for Logic 0.

**V<sub>INH</sub>**

The minimum input voltage for Logic 1.

**I<sub>INL</sub>, I<sub>INH</sub>**

The input current of the digital input when high or when low.

**C<sub>S</sub> (Off) and C<sub>D</sub> (Off)**

The off switch source and drain capacitance for the off condition, which is measured with reference to ground.

**C<sub>D</sub> (On) and C<sub>S</sub> (On)**

The on switch drain and source capacitance for the on condition, which is measured with reference to ground.

**C<sub>IN</sub>**

The digital input capacitance.

**t<sub>ON</sub>**

The delay between the 50% and 90% points of the digital control input and the output switching on.

**t<sub>OFF</sub>**

The delay between the 50% and 10% points of the digital control input and the output switching off.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Off Isolation**

A measure of unwanted signal coupling through an off switch.

**Channel-to-Channel Crosstalk**

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Bandwidth**

The frequency at which the output is attenuated by 3 dB.

**Insertion Loss**

The loss due to the on resistance of the switch.

**TOTAL HARMONIC DISTORTION (THD)**

THD is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

**Total Harmonic Distortion + Noise (THD + N)**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

**AC Power Supply Rejection Ratio (AC PSRR)**

A measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.115 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the AC PSRR.

## THEORY OF OPERATION

### SWITCH ARCHITECTURE

The ADG1412L is a set of low logic controlled, quad SPST switches that are compatible with 1.2 V or 1.8 V logic depending on the  $V_L$  input.

### $V_L$ FLEXIBILITY

An external  $V_L$  supply provides flexibility for lower logic levels. The following  $V_L$  conditions must be satisfied for the switch to operate in either 1.2 V or 1.8 V logic operation:

- ▶  $V_L = 1.1 \text{ V to } 1.3 \text{ V}$  for 1.2 V logic
- ▶  $V_L = 1.65 \text{ V to } 1.95 \text{ V}$  for 1.8 V logic

### 1.2 V AND 1.8 V JEDEC COMPLIANCE

The ADG1412L is both 1.2 V and 1.8 V JEDEC standard compliant (normal range) to the digital-input threshold. This compliance with the digital-input threshold ensures low voltage CMOS logic compatibility when operating with a valid logic power-supply range.

Note that the switch digital-input requirement for both the 1.2 V and 1.8 V logic levels are the following:

- ▶  $V_{INH} = 0.65 \times V_L$
- ▶  $V_{INL} = 0.35 \times V_L$

### INITIALIZATION TIME

The digital section of the ADG1412L goes through an initialization phase during  $V_{DD}$ ,  $V_{SS}$ , and  $V_L$  power up. After  $V_{DD}$ ,  $V_{SS}$ , and  $V_L$  power up, ensure that a minimum of 50  $\mu\text{s}$  has passed and that  $V_{DD}$ ,  $V_{SS}$ , and  $V_L$  do not drop before issuing an  $INx$  input.

### SWITCHES IN A KNOWN STATE

The switches within the ADG1412L are off when the  $INx$  pins are floating, which prevents unwanted signals from passing through these switches. This built-in feature of the ADG1412L eliminates the need to install an external pull-down resistor. The ADG1412L can pull down the floating  $INx$  inputs against the leakage currents up to half of the  $I_{INH}$ .

## APPLICATIONS INFORMATION

FIELD PROGRAMMABLE GRID ARRAY (FPGA)  
LOW LOGIC COMPLIANCE

Figure 35 shows a typical application where the ADG1412L is used together with an FPGA or microcontroller. The flexible  $V_L$  pin can be tied to the digital-supply voltage ( $V_{CCO}$ ), and the INx input can be tied directly to the digital IO port for ease of use.

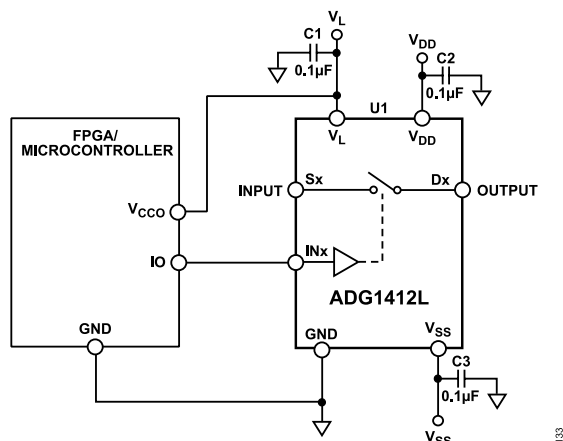


Figure 35. Typical Application

The ADG1412L is 1.2 V and 1.8 V JEDEC standard compliant, which ensures that the logic-input specifications,  $V_{INH}$  and  $V_{INL}$ , meet the digital-output specifications, minimum  $V_{OH}$  and maximum  $V_{OL}$ , of the FPGA or microcontroller. Common implementations do not guarantee logic-level compatibility, which can introduce implementation risks. The ADG1412L eliminates these risks by complying with the widely accepted 1.2 V and 1.8 V logic-level standard.

 **$V_{OH}$  AND  $V_{OL}$  AND  $V_{INH}$  AND  $V_{INL}$  RELATIONSHIP**

It is recommended to confirm that the logic output high,  $V_{OH}$ , of the FPGA or microcontroller is higher than the input logic high,  $V_{INH}$ . In addition, the logic output low,  $V_{OL}$ , of the FPGA or microcontroller must be lower than the input low,  $V_{INL}$ .

Figure 36 shows the 1.2 V logic compatibility relationship between  $V_{OH}$  and  $V_{OL}$  of the FPGA or the microcontroller with the INx inputs of the ADG1412L,  $V_{INH}$  and  $V_{INL}$ .

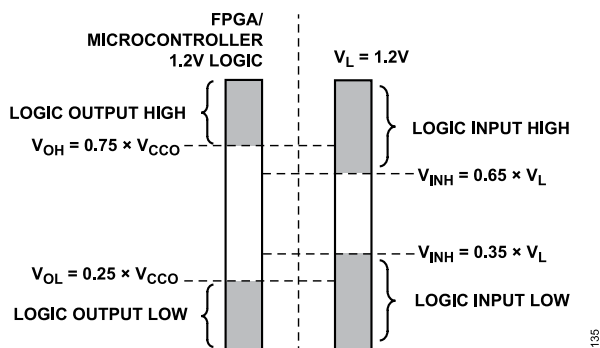


Figure 36. 1.2 V Logic Compatibility Between  $V_{OH}$  and  $V_{OL}$  and  $V_{INH}$  and  $V_{INL}$

Figure 37 shows the 1.8 V logic compatibility relationship between  $V_{OH}$  and  $V_{OL}$  of the FPGA or the microcontroller with the INx inputs of the ADG1412L,  $V_{INH}$  and  $V_{INL}$ .

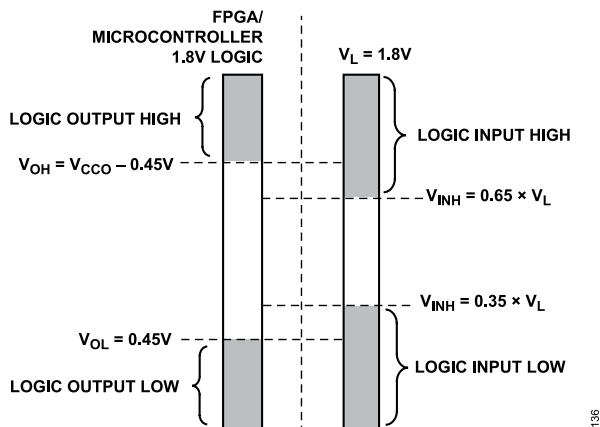


Figure 37. 1.8 V Logic Compatibility Between  $V_{OH}$  and  $V_{OL}$  and  $V_{INH}$  and  $V_{INL}$

**POWER-SUPPLY RAILS**

To guarantee correct operation of the ADG1412L, a minimum of 0.1  $\mu$ F decoupling capacitors are required on the  $V_{DD}$ ,  $V_{SS}$ , and  $V_L$  supply pins.

The ADG1412L can operate with  $V_{DD}$  and  $V_{SS}$  dual supplies between  $\pm 4.5$  V to  $\pm 16.5$  V. This device can also operate with a  $V_{DD}$  single supply between 5 V to 16.5 V and a  $V_L$  of between 1.1 V to 1.95 V. However, the  $V_{DD}$  to  $V_{SS}$  range must not exceed 35 V, and the  $V_L$  range must not exceed 2.25 V, as stated in the [Absolute Maximum Ratings](#) section.

OUTLINE DIMENSIONS

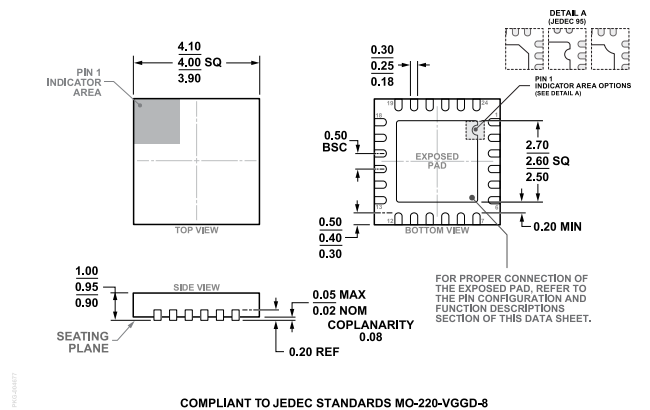


Figure 38. 24-Lead Lead Frame Chip Scale Package [LFCSP]  
4 mm x 4 mm Body and 0.95 mm Package Height  
(CP-24-17)  
Dimensions shown in millimeters

ORDERING GUIDE

Table 12. Ordering Guide

Model <sup>1</sup>	Temperature	Package Description	Package Option	Package Quantity
ADG1412LYCPZ-REEL7	-40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17	Reel, 1500

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 13. Evaluation Boards

Model <sup>1</sup>	Description
EVAL-ADG1412LEBZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[ADG1412LYCPZ-REEL7](#) [EVAL-ADG1412LEBZ](#)