8-Channel DAS with 18-Bit, 1 MSPS Bipolar Input, Simultaneous Sampling ADC

Data Sheet

AD7606C-18

FEATURES

- 18-bit ADC with 1 MSPS on all channels
- Input buffer with 1 MΩ minimum analog input impedance (R_{IN})
- Single 5 V analog supply and 1.71 V to 5.25 V V_{DRIVE}
- Per channel selectable analog input ranges
  - Bipolar single-ended: ±12.5 V, ±10 V, ±6.25 V, ±5 V, ±2.5 V
  - Unipolar single-ended: 0 V to 12.5 V, 0 V to 10 V, 0 V to 5 V
  - Bipolar differential: ±20 V, ±12.5 V, ±10 V, ±5 V
- Two bandwidth options: 25 kHz and 220 kHz, per channel
- Flexible digital filter, oversampling ratio up to 256
- −40°C to +125°C operating range
- ±21 V input clamp protection with 6 kV ESD
- Pin to pin compatible to the AD7606B, AD7608, and AD7609
- Performance
  - 93 dB typical SNR for ±20 V bipolar differential range
  - 102 dB SNR, oversampling by 32
  - −100 dB typical THD for all other ranges
  - TUE = 0.05% of FSR maximum, external reference
  - ±0.5 ppm/°C typical PFS and NFS error drift
  - ±3 ppm/°C typical reference temperature coefficient

CALIBRATION AND DIAGNOSTICS

- Per channel system phase, offset, and gain calibration
- Analog input open circuit detection feature
- Self diagnostics and monitoring features
- CRC error checking on read and write data and registers

APPLICATIONS

- Power line monitoring
- Protective relays
- Multiphase motor control
- Instrumentation and control systems
- Data acquisition systems

COMPANION PRODUCTS

- Voltage References: ADR4525, LT6657, LTC6655
- Digital Isolators: ADuM142E, ADuM6422A, ADuM5020, ADuM5028
- AD7606x Family Software Model
- *Additional companion products on the AD7606C-18 product page*

FUNCTIONAL BLOCK DIAGRAM

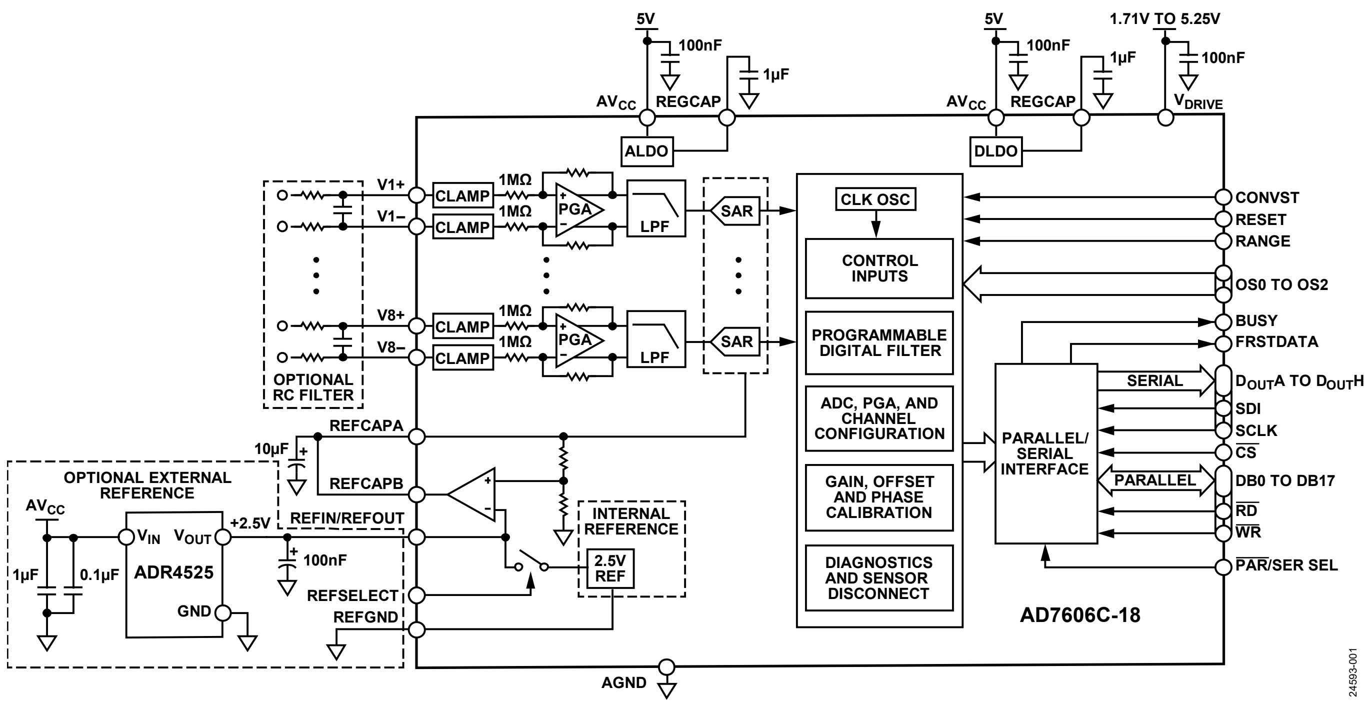

Figure 1.

Rev. A

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

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REVISION HISTORY

4/2021—Rev. 0 to Rev. A

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10/2020—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7606C-18 is an 18-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS) with eight channels. Each channel contains analog input clamp protection, a programmable gain amplifier (PGA), a low-pass filter (LPF), and an 18-bit successive approximation register (SAR) analog-to-digital converter (ADC). The AD7606C-18 also contains a flexible digital filter, a low drift, 2.5 V precision reference, a reference buffer to drive the ADC, and flexible parallel and serial interfaces.

The AD7606C-18 operates from a single 5 V supply and accommodates the following input ranges when sampling at throughput rates of 1 MSPS for all channels:

- Bipolar single-ended: ±12.5 V, ±10 V, ±6.25 V, ±5 V, and ±2.5 V
- Unipolar single-ended: 0 V to 12.5 V, 0 V to 10 V, and 0 V to 5 V
- Bipolar differential: ±20 V, ±12.5 V, ±10 V, and ±5 V

The input clamp protection tolerates voltages up to ±21 V. The single supply operation, on-chip filtering, and high input impedance eliminate the need for external driver op amps, which require bipolar supplies. For applications with lower throughput rates, the AD7606C-18 flexible digital filter can be used to improve noise performance.

In hardware mode, the AD7606C-18 is fully compatible with the AD7608 and AD7609. In software mode, the following advanced features are available:

- Analog input range selectable per channel with added ranges available
- High bandwidth mode (220 kHz) selectable per channel
- Additional oversampling options with an oversampling ratio up to 256
- System gain, system offset, and system phase calibration, per channel
- Analog input open circuit detector
- Diagnostic multiplexer
- Monitoring functions (serial peripheral interface (SPI) invalid read and write, cyclic redundancy check (CRC), busy stuck monitor, and reset detection)

Note that throughout this data sheet, multifunction pins, such as the $\overline{RD}$/SCLK pin, are referred to either by the entire pin name or by a single function of the pin, for example, the SCLK pin, when only that function is relevant.

Table 1. Bipolar Input, Simultaneous Sampling, Pin to Pin Compatible Family of Devices

Input Type	Resolution (Bits)	R_{IN}[1] = 1 MΩ, 200 kSPS	R_{IN} = 5 MΩ, 800 kSPS	R_{IN} = 1 MΩ, 1 MSPS	Number of Channels
Single-Ended	18	AD7608		AD7606C-18[2]	8
	16	AD7606	AD7606B[2]	AD7606C-16	8
		AD7606-6			6
		AD7606-4			4
	14	AD7607			8
True Differential	18	AD7609		AD7606C-18[2]	8

[1] R_{IN} is input impedance.
[2] This state-of-the-art device is recommended for newer designs as an alternative to the AD7606, AD7608, and AD7609.

SPECIFICATIONS

Voltage reference (V_{REF}) = 2.5 V external and internal, analog supply voltage (AV_{CC}) = 4.75 V to 5.25 V, logic supply voltage (V_{DRIVE}) = 1.71 V to 5.25 V, sample frequency (f_{SAMPLE}) = 1 MSPS, T_A = −40°C to +125°C, and all input voltage ranges, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	Input frequency (f_{IN}) = 1 kHz sine wave, unless otherwise noted				
Signal-to-Noise Ratio (SNR)					
Low Bandwidth Mode	±20 V bipolar differential range	91	93		dB
	±20 V bipolar differential range, oversampling by 32, f_{IN} = 50 Hz		102		dB
	±12.5 V bipolar differential range	90	92		dB
	±10 V bipolar differential range	90	91.5		dB
	±5 V bipolar differential range	89	90.5		dB
	±12.5 V bipolar single-ended range	90	92		dB
	±10 V bipolar single-ended range	90.5	92.5		dB
	±6.25 V bipolar single-ended range	89	91.5		dB
	±5 V bipolar single-ended range	89	91		dB
	±2.5 V bipolar single-ended range	86.5	88		dB
	0 V to 12.5 V unipolar single-ended range	88.5	90		dB
	0 V to 10 V unipolar single-ended range	88	90		dB
	0 V to 5 V unipolar single-ended range	84.5	86.5		dB
High Bandwidth Mode	±20 V bipolar differential range		89		dB
	±12.5 V bipolar differential range		87		dB
	±10 V bipolar differential range		86		dB
	±5 V bipolar differential range		83.5		dB
	±12.5 V bipolar single-ended range		87.5		dB
	±10 V bipolar single-ended range		87		dB
	±6.25 V bipolar single-ended range		84.5		dB
	±5 V bipolar single-ended range		83.5		dB
	±2.5 V bipolar single-ended range		82		dB
	0 V to 12.5 V unipolar single-ended range		83		dB
	0 V to 10 V unipolar single-ended range		82		dB
	0 V to 5 V unipolar single-ended range		80		dB
Total Harmonic Distortion (THD)	Low bandwidth mode				
	Unipolar input ranges		−97		dB
	All other ranges		−100	−95	dB
Spurious-Free Dynamic Range (SFDR)			−105		dB
Channel to Channel Isolation	f_{IN} on unselected channels up to 200 kHz		−110		dB
Full-Scale (FS) Step Settling Time	0.01% of FS, low bandwidth mode		80		μs
	0.01% of FS, high bandwidth mode		15		μs
ANALOG INPUT FILTER					
−3 dB Full Power Bandwidth	Low bandwidth mode		25		kHz
	High bandwidth mode		220		kHz
	High bandwidth mode, 2.5 V bipolar, 0 V to 5 V unipolar		150		kHz
−0.1 dB Full Power Bandwidth	Low bandwidth mode		3.9		kHz
	High bandwidth mode		25		kHz
	High bandwidth mode, 2.5 V bipolar, 0 V to 5 V unipolar		20		kHz
Phase Delay	Low bandwidth mode		6.8		μs
	High bandwidth mode		1.1		μs
	High bandwidth mode, ±2.5 V range, 0 V to 5 V unipolar		1.5		

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Phase Delay Matching					
	Low bandwidth mode			200	ns
	High bandwidth mode			30	ns
DC ACCURACY					
Resolution	No missing codes	18			Bits
Differential Nonlinearity (DNL)			±0.5	±0.99	LSB[1]
Integral Nonlinearity (INL)	Bipolar input ranges		±2	±7.5	LSB[1]
	Unipolar input ranges		±4		LSB
Total Unadjusted Error (TUE)[2]					
	External reference		±25	±130	LSB
	External reference, ±2.5 V range		±25	±180	LSB
	Unipolar input ranges		±60	±280	LSB
Bipolar Ranges					
Positive Full-Scale (PFS) and Negative Full-Scale (NFS) Error[3]			±20	±120	LSB
PFS and NFS Error Drift			±0.5	±3	ppm/°C
PFS and NFS Error Matching			15	60	LSB
Bipolar Zero Code Error					
	2.5 V range		±10	±160	LSB[1]
	All other input ranges		±10	±80	LSB[1]
Bipolar Zero Code Error Drift					
	2.5 V range		±2	±5	ppm/°C
	All other input ranges		±0.5	±2.5	ppm/°C
Bipolar Zero Code Error Matching			20	90	LSB[1]
Unipolar Ranges					
FS Error			±40	±240	LSB
FS Error Drift			±1	±7	ppm/°C
FS Error Matching			20	160	LSB
Zero Scale Error			±40	±200	LSB
Zero Scale Error Drift			±2.5	±7	ppm/°C
Zero Scale Error Matching			20	160	LSB
SYSTEM CALIBRATION					
PFS and NFS Calibration Range	Series resistor in front of the Vx+ and Vx− inputs	1		64	kΩ
Offset Calibration Range		1		512	LSB
Phase Calibration Range		1		255	μs
PFS and NFS Error	After gain calibration		±60		LSB
Offset Error	After offset calibration		±2		LSB
Phase Error	After phase calibration		±1		μs
ANALOG INPUT					
Input Voltage (V_{IN}) Ranges	V_{IN} = Vx+ − Vx−				
	±20 V bipolar differential range	−20		+20	V
	±12.5 V bipolar differential range	−12.5		+12.5	V
	±10 V bipolar differential range	−10		+10	V
	±5 V bipolar differential range	−5		+5	V
	±12.5 V bipolar single-ended range	−12.5		+12.5	V
	±10 V bipolar single-ended range	−10		+10	V
	±6.25 V bipolar single-ended range	−6.25		+6.25	V
	±5 V bipolar single-ended range	−5		+5	V
	±2.5 V bipolar single-ended range	−2.5		+2.5	V
	0 V to 12.5 V unipolar single-ended range	0		12.5	V
	0 V to 10 V unipolar single-ended range	0		10	V
	0 V to 5 V unipolar single-ended range	0		5	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Absolute Voltage Negative Input	Vx− − AGND				
	±12.5 V bipolar single-ended range	−1		+1.6	V
	±10 V bipolar single-ended range	−0.6		+1.9	V
	±6.25 V bipolar single-ended range	−0.4		+2.5	V
	±5 V bipolar single-ended range	−0.1		+2.7	V
	±2.5 V bipolar single-ended range	−0.05		+3	V
	0 V to 12.5 V unipolar single-ended range	−6.5		+1.2	V
	0 V to 10 V unipolar single-ended range	−4.9		+1.7	V
	0 V to 5 V unipolar single-ended range	−2.3		+4	V
Common-Mode Input Range	±20 V bipolar differential range	−10		+10	V
	±12.5 V bipolar differential range	−7.8		+7.8	V
	±10 V bipolar differential range	−6		+7	V
	±5 V bipolar differential range	−3		+5	V
Input Impedance (R_{IN})		1	1.2		MΩ
Analog Input Current			$(V_{IN} − 2)/R_{IN}$		µA
Input Capacitance (C_{IN})[4]			5		pF
Input Impedance Drift			±1	±25	ppm/°C
REFERENCE INPUT AND OUTPUT					
Reference Input Voltage	External reference	2.495	2.5	2.505	V
DC Leakage Current				±0.12	µA
Input Capacitance (C_{IN})			7.5		pF
Reference Output Voltage	Internal reference, T_A = 25°C	2.4975	2.5	2.5025	V
Reference Temperature Coefficient			±3	±10	ppm/°C
Reference Voltage to the ADC	REFCAPA (Pin 44) and REFCAPB (Pin 45)	4.39		4.41	V
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.7 × V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.2 × V_{DRIVE}	V
Input Current (I_{IN})				±1	µA
Input Capacitance (C_{IN})			5		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	Source current (I_{SOURCE}) = 100 µA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	Sink current (I_{SINK}) = 100 µA			0.2	V
Floating State Leakage Current				±1	µA
Output Capacitance[4]			5		pF
Output Coding Bipolar Ranges	Twos complement				
Output Coding Unipolar Ranges	Straight binary				
CONVERSION RATE					
Conversion Time	See Table 3		550		ns
Acquisition Time[5]			450		ns
Throughput Rate	Per channel			1000	kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75	5	5.25	V
V_{DRIVE}		1.71		5.25	V
AV_{CC} Current (I_{AVCC})					
Normal Mode (Static)			9	11	mA
Normal Mode (Operational)	f_{SAMPLE} = 1 MSPS		45	50	mA
	f_{SAMPLE} = 10 kSPS		8.5	10	mA
Standby			5	6	mA
Shutdown Mode			0.5	5	µA
V_{DRIVE} Current (I_{VDRIVE})					
Normal Mode (Static)			2.8	5	µA
Normal Mode (Operational)	f_{SAMPLE} = 1 MSPS		1.8	1.9	mA
	f_{SAMPLE} = 10 kSPS		21	24	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Standby			2.5	4	μA
Shutdown Mode			0.5	1.5	μA
Power Dissipation					
Normal Mode (Static)			47	58	mW
Normal Mode (Operational)	f_{SAMPLE} = 1 MSPS		245	272	mW
	f_{SAMPLE} = 10 kSPS		45	52	mW
Standby			26	32	mW
Shutdown Mode			5	24	μW

[1] LSB means least significant bit. With a ±2.5 V input range, 1 LSB = 19μV. With a ±5 V input range, 1 LSB = 38.14 μV. With a ±10 V input range, 1 LSB = 76.293 μV.
[2] TUE (% FSR) = TUE (LSB)/2^{18} × 100. For example, 130 LSBs = 0.05 % of FSR.
[3] These specifications include the full temperature range variation and contribution from the reference buffer.
[4] Not production tested. Sample tested during initial release to ensure compliance.
[5] The ADC input is settled by the internal PGA. Therefore, the acquisition time is the time between the end of the conversion and the start of the next conversion with no impact on external components.

TIMING SPECIFICATIONS

Universal Timing Specifications

AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 1.71 V to 5.25 V, V_{REF} = 2.5 V external reference and internal reference, and T_A = −40°C to +125°C, unless otherwise noted. Interface timing tested using a load capacitance of 20 pF, dependent on V_{DRIVE} and load capacitance for the serial interface.

Table 3.

Parameter	Min	Typ	Max	Unit	Description
t_{CYCLE}	1			μs	Minimum time between consecutive CONVST rising edges (excluding oversampling modes)[1]
t_{LP_CNV}	10			ns	CONVST low pulse width
t_{HP_CNV}	10			ns	CONVST high pulse width
$t_{D\_CNV\_BSY}$			22	ns	CONVST high to BUSY high delay time
t_{S_BSY}	0			ns	Minimum time from BUSY falling edge to $\overline{RD}$ falling edge setup time (in parallel interface) or to MSB being available on the D_{OUT}x line (in serial interface)
t_{D_BSY}	25			ns	Minimum time between last $\overline{RD}$ falling edge (in parallel interface) or last LSB being clocked out (serial interface) and the following BUSY falling edge, read during conversion
t_{ACQ}	0.35			μs	Acquisition time
t_{CONV}	0.5		0.65	μs	Conversion time, no oversampling
	1.7		1.75	μs	Oversampling by 2
	3.6		3.8	μs	Oversampling by 4
	7.6		7.85	μs	Oversampling by 8
	15.5		16	μs	Oversampling by 16
	31.0		32.5	μs	Oversampling by 32
	62.75		65.0	μs	Oversampling by 64
	126		130	μs	Oversampling by 128
	252		256	μs	Oversampling by 256
t_{RESET}					
Partial Reset	55		2000	ns	Partial RESET high pulse width
Full Reset	3200			ns	Full RESET high pulse width
t_{DEVICE_SETUP}				μs	Time between RESET falling edge and first CONVST rising edge
Partial Reset	50			ns	
Full Reset	274			μs	
$t_{WAKE-UP}$					Wake-up time after standby and shutdown mode (see Figure 86)
Standby	1			μs	
Shutdown	10			ms	
$t_{POWER-UP}$	10			ms	Time between stable AV_{CC} and V_{DRIVE} and assert of RESET

[1] Applies to serial mode when all eight D_{OUT}x lines are selected.

Universal Timing Diagram

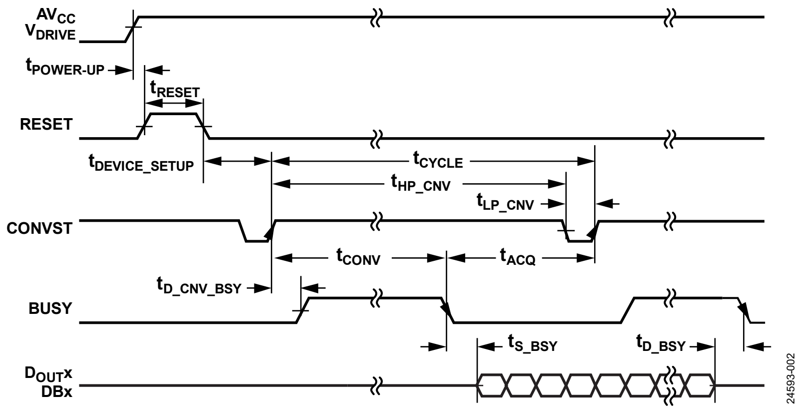


Figure 2. Universal Timing Diagram

Parallel Mode Timing Specifications

Table 4.

Parameter	Min	Typ	Max	Unit	Description
$t_{S\_\overline{CS}\_\overline{RD}}$	0			ns	$\overline{CS}$ falling edge to $\overline{RD}$ falling edge setup time
$t_{H\_\overline{RD}\_\overline{CS}}$	0			ns	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge hold time
$t_{HP\_\overline{RD}}$	10			ns	$\overline{RD}$ high pulse width
$t_{LP\_\overline{RD}}$	10			ns	$\overline{RD}$ low pulse width
$t_{HP\_\overline{CS}}$	10			ns	$\overline{CS}$ high pulse width
$t_{D\_\overline{CS}\_DB}$			35	ns	Delay from $\overline{CS}$ until DBx three-state disabled
$t_{D\_\overline{RD}\_DB}$					Data access time after falling edge of $\overline{RD}$
			30	ns	$V_{DRIVE} > 2.7$ V
			25	ns	$V_{DRIVE} < 2.7$ V
$t_{H\_\overline{RD}\_DB}$	12			ns	Data hold time after falling edge of $\overline{RD}$
$t_{DHZ\_\overline{CS}\_DB}$			40	ns	$\overline{CS}$ rising edge to DBx high impedance
$t_{CYC\_\overline{RD}}$	30			ns	$\overline{RD}$ falling edge to next $\overline{RD}$ falling edge
$t_{D\_\overline{CS}\_FD}$			20	ns	Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled
$t_{D\_\overline{RD}\_FDH}$			30	ns	Delay from $\overline{RD}$ falling edge until FRSTDATA high
$t_{D\_\overline{RD}\_FDL}$			30	ns	Delay from $\overline{RD}$ falling edge until FRSTDATA low
$t_{DHZ\_\overline{CS}\_FD}$			25	ns	Delay from $\overline{CS}$ rising edge until FRSTDATA three-state enabled
$t_{S\_\overline{CS}\_\overline{WR}}$	0			ns	$\overline{CS}$ to $\overline{WR}$ setup time
$t_{HP\_\overline{WR}}$	2			ns	$\overline{WR}$ high pulse width
$t_{LP\_\overline{WR}}$	35			ns	$\overline{WR}$ low pulse width
$t_{H\_\overline{WR}\_\overline{CS}}$	0			ns	$\overline{WR}$ hold time
$t_{S\_DB\_\overline{WR}}$	5			ns	Configuration data to $\overline{WR}$ setup time
$t_{H\_\overline{WR}\_DB}$	5			ns	Configuration data to $\overline{WR}$ hold time
$t_{CYC\_\overline{WR}}$	180			ns	Configuration data settle time, $\overline{WR}$ rising edge to next $\overline{WR}$ rising edge

Parallel Mode Timing Diagrams

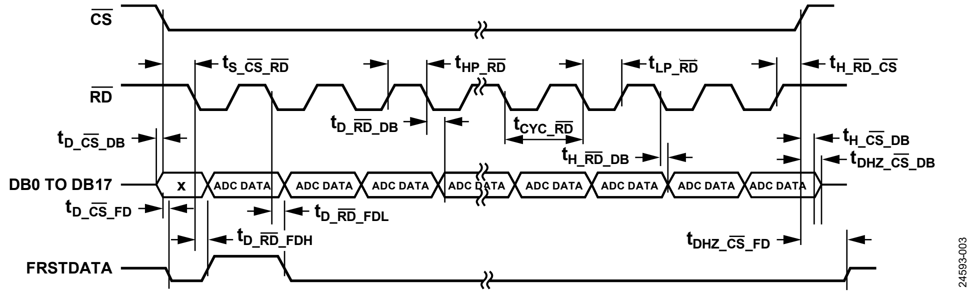


Figure 3. Parallel Mode Read, Separate $\overline{CS}$ and $\overline{RD}$ Pulses

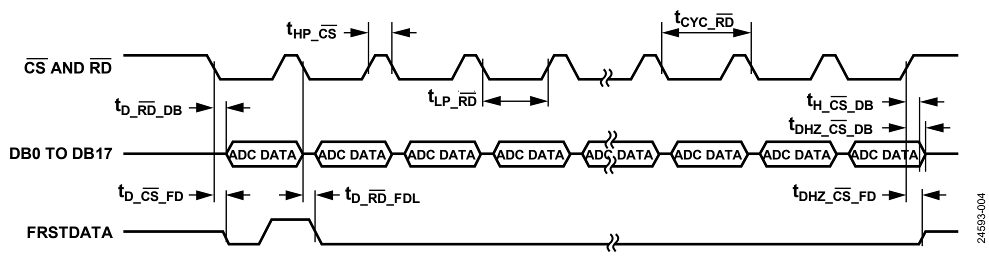


Figure 4. Parallel Mode Read, Linked $\overline{CS}$ and $\overline{RD}$ Pulses

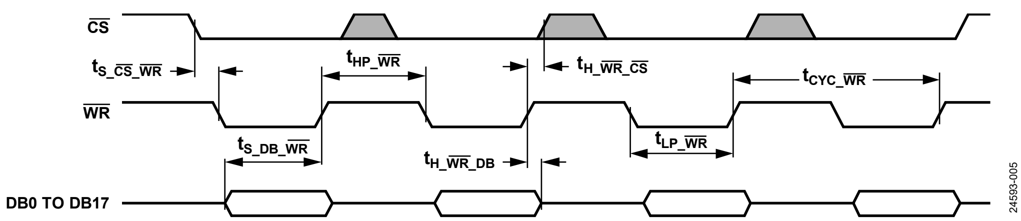


Figure 5. Parallel Mode Write Operation

Serial Mode Timing Specifications

Table 5.

Parameter	Min	Typ	Max	Unit	Description
f_{SCLK}					SCLK frequency, $f_{SCLK} = 1/t_{SCLK}$
			60	MHz	$V_{DRIVE} > 2.7$ V
			40	MHz	$V_{DRIVE} < 2.7$ V
t_{SCLK}	$1/f_{SCLK}$			µs	Minimum SCLK period
$t_{S\_\overline{CS}\_SCK}$	2			ns	$\overline{CS}$ to SCLK falling edge setup time
$t_{H\_SCK\_\overline{CS}}$	2			ns	SCLK to $\overline{CS}$ rising edge hold time
t_{LP_SCK}	$0.4 \times t_{SCLK}$			ns	SCLK low pulse width
t_{HP_SCK}	$0.4 \times t_{SCLK}$			ns	SCLK high pulse width
$t_{D\_\overline{CS}\_DO}$			18	ns	Delay from $\overline{CS}$ until $D_{OUT}x$ three-state disabled
$t_{D\_SCK\_DO}$					Data out access time after SCLK rising edge
			17	ns	$V_{DRIVE} > 2.7$ V
			25	ns	$V_{DRIVE} < 2.7$ V
$t_{H\_SCK\_DO}$					Data out hold time after SCLK rising edge
	5			ns	$V_{DRIVE} > 2.7$ V
	10			ns	$V_{DRIVE} < 2.7$ V
$t_{S\_SDI\_SCK}$	9			ns	Data in setup time before SCLK falling edge
$t_{H\_SCK\_SDI}$	0			ns	Data in hold time after SCLK falling edge

Parameter	Min	Typ	Max	Unit	Description
$t_{DHZ\_\overline{CS}\_DO}$			25	ns	$\overline{CS}$ rising edge to $D_{OUT}x$ high impedance
$t_{\overline{WR}}$	25			ns	Time between writing and reading the same register or between two writes, if f_{SCLK} >50 MHz
$t_{D\_\overline{CS}\_FD}$			16	ns	Delay from $\overline{CS}$ until $D_{OUT}x$ three-state disabled or delayed from $\overline{CS}$ until MSB valid
$t_{D\_SCK\_FDL}$			18	ns	18th SCLK falling edge to FRSTDATA low
t_{DHZ_FD}			20	ns	$\overline{CS}$ rising edge until FRSTDATA three-state enabled

Serial Mode Timing Diagrams

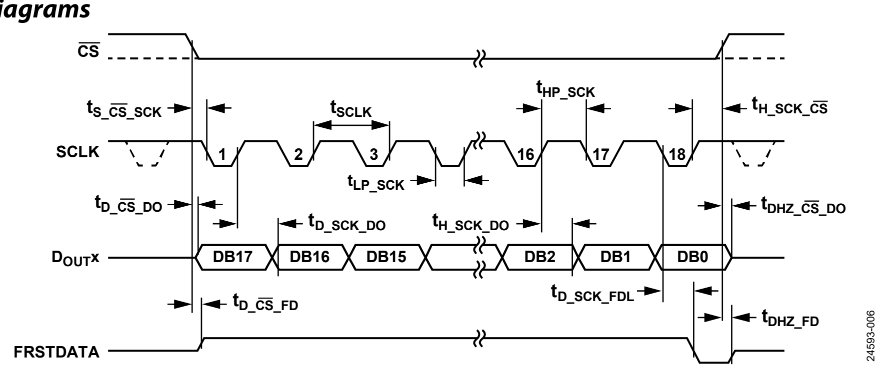


Figure 6. Serial Timing Diagram, ADC Mode (Channel 1)

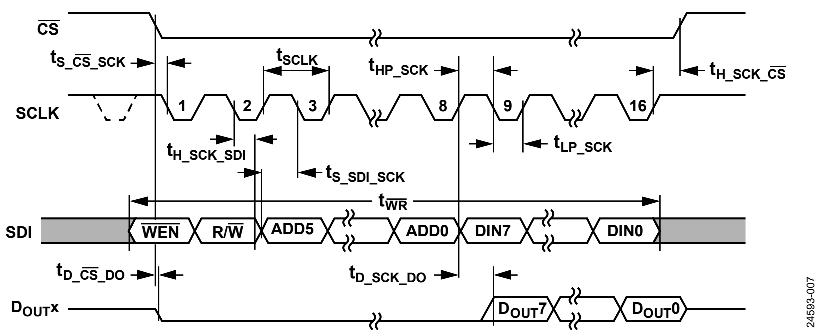


Figure 7. Serial Timing Interface, Register Map Read and Write Operations

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +6.5 V
V_{DRIVE} to AGND	−0.3 V to AV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±21 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Pb/Sn, Soldering Reflow (10 sec to 30 sec)	240 (+0)°C
Pb-Free, Soldering Reflow	260 (+0)°C

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
ST-64-2	40	7	°C/W

[1] Simulated data based on JEDEC 2s2p thermal test PCB in a JEDEC natural convention environment.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

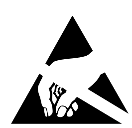
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD7606C-18

Table 8. AD7606C-18, 64-Lead LQFP

ESD Model	Withstand Threshold (V)	Class
HBM		3A
Analog Inputs Only	6000	
All Other Pins	4000	
FICDM	750	C4

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

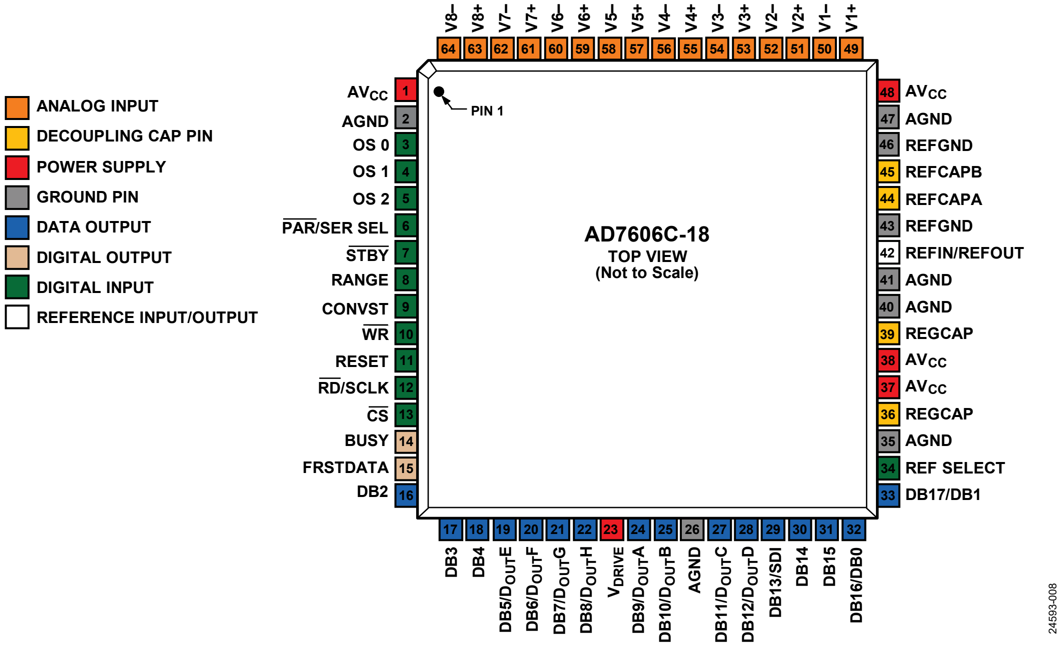


Figure 8. Pin Configuration

Table 9. Pin Function Description

Pin No.	Type[1]	Mnemonic	Description
1, 37, 38, 48	P	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these supply pins to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. The AGND pins are the ground reference points for all analog circuitry on the AD7606C-18. All analog input signals and external reference signals must be referred to the AGND pins. All six of the AGND pins must connect to the AGND plane of a system.
3 to 5	DI	OS0 to OS2	Oversampling Mode Pins. OS0 to OS2 select the oversampling ratio or enable software mode (see Table 14 for oversampling bit decoding). See the Digital Filter section for more details about the oversampling mode of operation.
6	DI	$\overline{\text{PAR}}$/SER SEL	Parallel/Serial Interface Selection Input. If the $\overline{\text{PAR}}$/SER SEL pin is tied to a logic low, the parallel interface is selected. If the $\overline{\text{PAR}}$/SER SEL pin is tied to a logic high, the serial interface is selected. See the Digital Interface section for more information on each interface available.
7	DI	$\overline{\text{STBY}}$	Standby Mode Input. In hardware mode, the $\overline{\text{STBY}}$ pin, in combination with the RANGE pin, places the AD7606C-18 into one of two power-down modes: standby mode or shutdown mode. In software mode, the $\overline{\text{STBY}}$ pin is ignored. Therefore, it is recommended to connect the $\overline{\text{STBY}}$ pin to logic high. See the Power-Down Modes section for more information on both hardware mode and software mode.
8	DI	RANGE	Analog Input Range Selection Input. In hardware mode, the RANGE pin determines the input range of the analog input channels (see Table 10). If the $\overline{\text{STBY}}$ pin is at logic low, the RANGE pin determines the power-down mode (see Table 16). In software mode, the RANGE pin is ignored. However, the RANGE pin must be tied high or low.
9	DI	CONVST	Conversion Start Input. When the CONVST pin transitions from low to high, the analog input is sampled on all eight SAR ADCs. In software mode, the CONVST pin can be configured as an external oversampling clock. Providing a low jitter external clock helps improve the SNR performance for large oversampling ratios. See the External Oversampling Clock section for further details.
10	DI	$\overline{\text{WR}}$	Parallel Write Control Input. In hardware mode, the $\overline{\text{WR}}$ pin has no function. Therefore, the $\overline{\text{WR}}$ pin can be tied high, tied low, or shorted to CONVST. In software mode, the $\overline{\text{WR}}$ pin is the active low write pin for writing registers using the parallel interface. See the Parallel Interface section for more information.

Pin No.	Type[1]	Mnemonic	Description
11	DI	RESET	Reset Input, Active High. Full and partial reset options are available. The type of reset is determined by the length of the reset pulse. It is recommended that the device receives a full reset pulse after power-up. See the Reset Functionality section for further details.
12	DI	$\overline{RD}$/SCLK	Parallel Data Read Control Input when the Parallel Interface is Selected ($\overline{RD}$). Serial Clock Input when the Serial Interface is Selected (SCLK). See the Digital Interface section for more details.
13	DI	$\overline{CS}$	Chip Select. The $\overline{CS}$ pin is the active low chip select input for ADC data reads or register data reads and writes, in both the serial and parallel interfaces. See the Digital Interface section for more details.
14	DO	BUSY	Busy Output. The BUSY pin transitions to a logic high along with the CONVST rising edge. The BUSY output remains high until the conversion process for all channels is complete.
15	DO	FRSTDATA	First Data Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel interface (see Figure 3) or the serial interface (see Figure 6). See the Digital Interface section for more details.
16 to 18	DO/DI	DB2 to DB4	Parallel Output/Input Data Bits. When using the parallel interface, the DB2 to DB4 pins act as three-state parallel digital input and output pins (see the Parallel Interface section). When $\overline{CS}$ and $\overline{RD}$ are low, the DB2 to DB4 pins are used to output DB2 to DB4 of the conversion result during the first $\overline{RD}$ pulse and zeros during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, tie the DB2 to DB4 pins to AGND.
19	DO/DI	DB5/D_{OUT}E	Parallel Output/Input Data Bit 5/Serial Interface Data Output Pin. When using the parallel interface, the DB5/D_{OUT}E pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB5/D_{OUT}E pin is used to output DB5 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB5/D_{OUT}E pin functions as D_{OUT}E. See Table 23 for more details on each data interface and operation mode.
20	DO/DI	DB6/D_{OUT}F	Parallel Output/Input Data Bit 6/Serial Interface Data Output Pin. When using the parallel interface, the DB6/D_{OUT}F pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB6/D_{OUT}F pin is used to output DB6 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB6/D_{OUT}F pin functions as D_{OUT}F. See Table 23 for more details on each data interface and operation mode.
21	DO/DI	DB7/D_{OUT}G	Parallel Output/Input Data Bit 7/Serial Interface Data Output Pin. When using the parallel interface, the DB7/D_{OUT}G pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB7/D_{OUT}G pin is used to output DB7 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB7/D_{OUT}G pin functions as D_{OUT}G. See Table 23 for more details on each data interface and operation mode.
22	DO/DI	DB8/D_{OUT}H	Parallel Output/Input Data Bit 8/Serial Interface Data Output Pin. When using the parallel interface, the DB8/D_{OUT}H pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB8/D_{OUT}H pin is used to output DB8 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB8/D_{OUT}H pin functions as D_{OUT}H. See Table 23 for more details on each data interface and operation mode.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (1.71 V to 5.25 V) supplied at the V_{DRIVE} pin determines the operating voltage of the interface. The V_{DRIVE} pin is nominally at the same supply as the supply of the host interface, that is, the data signal processor (DSP) and field programmable gate array (FPGA).
24	DO/DI	DB9/D_{OUT}A	Parallel Output/Input Data Bit 9/Serial Interface Data Output Pin. When using the parallel interface, the DB9/D_{OUT}A pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB9/D_{OUT}A pin is used to output DB9 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB9/D_{OUT}A pin functions as D_{OUT}A. See Table 23 for more details on each data interface and operation mode.
25	DO/DI	DB10/D_{OUT}B	Parallel Output/Input Data Bit 10/Serial Interface Data Output Pin. When using the parallel interface, the DB10/D_{OUT}B pin acts as a three-state parallel digital input and output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB10/D_{OUT}B pin is used to output DB10 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB10/D_{OUT}B pin functions as D_{OUT}B. See Table 23 for more details on each data interface and operation mode.

Pin No.	Type[1]	Mnemonic	Description
27	DO/DI	DB11/$D_{OUT}C$	Parallel Output/Input Data Bit 11/Serial Interface Data Output Pin. When using the parallel interface, the DB11/$D_{OUT}C$ pin acts as a three-state parallel digital input and output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB11/$D_{OUT}C$ pin is used to output DB11 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, the DB11/$D_{OUT}C$ pin functions as $D_{OUT}C$ if in software mode and using the 4 $D_{OUT}x$ line option or 8 $D_{OUT}x$ line option. See Table 23 for more details on each data interface and operation mode.
28	DO/DI	DB12/$D_{OUT}D$	Parallel Output/Input Data Bit 12/Serial Interface Data Output Pin. When using the parallel interface, the DB12/$D_{OUT}D$ pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB12/$D_{OUT}D$ pin is used to output DB12 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using serial interface, the DB12/$D_{OUT}D$ pin functions as $D_{OUT}D$ if in software mode and using the 4 $D_{OUT}x$ line option or 8 $D_{OUT}x$ line option. See Table 23 for more details on each data interface and operation mode.
29	DO/DI	DB13/SDI	Parallel Output/Input Data Bit 13/Serial Data Input. When using parallel interface, the DB13/SDI pin acts as a three-state parallel digital input and output pin. When $\overline{CS}$ and $\overline{RD}$ are low, the DB13/SDI pin is used to output DB13 of the conversion result during the first $\overline{RD}$ pulse and zero during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface in software mode, the DB13/SDI pin functions as SDI. See Table 23 for more details on each data interface and operation mode.
30, 31	DO/DI	DB14, DB15	Parallel Output/Input Data Bits. When using the parallel interface, the DB14 and DB15 pins act as three-state parallel digital input and output pins (see the Parallel Interface section). When $\overline{CS}$ and $\overline{RD}$ are low, the DB14 and DB15 pins are used to output DB14 and DB15 of the conversion result during the first $\overline{RD}$ pulse and zeros during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, tie the DB14 and DB15 pins to AGND.
32	DO/DI	DB16/DB0	Parallel Output/Input Data Bits. When using the parallel interface, the DB16/DB0 pin acts as a three-state parallel digital input and output pin (see the Parallel Interface section). When $\overline{CS}$ and $\overline{RD}$ are low, the DB16/DB0 pin is used to output DB16 of the conversion result during the first $\overline{RD}$ pulse and DB0 of the same conversion result during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, tie the DB16/DB0 pin to AGND.
33	DO/DI	DB17/DB1	Parallel Output/Input Data Bits. When using the parallel interface, the DB17/DB1 pin acts as a three-state parallel digital input and output pin (see the Parallel Interface section). When $\overline{CS}$ and $\overline{RD}$ are low, the DB17/DB1 pin is used to output DB17 of the conversion result during the first $\overline{RD}$ pulse and DB1 of the same conversion result during the second $\overline{RD}$ pulse (see Figure 99). When using the serial interface, tie the DB17/DB1 pin to AGND.
34	DI	REF SELECT	Internal/External Reference Selection Logic Input. If the REF SELECT pin is set to logic high, the internal reference is selected and enabled. If the REF SELECT pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36, 39	P	REGCAP	Decoupling Capacitor Pin for Voltage Output from 1.9 V Internal Regulator, Analog Low Dropout (ALDO) and Digital Low Dropout (DLDO). The REGCAP output pins must be decoupled separately to AGND using a 1 µF capacitor. The voltage on the REGCAP pins is in the range of 1.875 V to 1.93 V.
42	REF	REFIN/REFOUT	Reference Input/Reference Output. The internal 2.5 V reference is available on the REFOUT pin for external use while the REF SELECT pin is set to logic high. Alternatively, by setting the REF SELECT pin to logic low, the internal reference is disabled and an external reference of 2.5 V must be applied to this input (REFIN). A 100 nF capacitor must be applied from the REFIN pin to ground, close to the REFGND pins, for both internal and external reference options. See the Reference section for more details.
43, 46	REF	REFGND	Reference Ground Pins. The REFGND pins must be connected to AGND.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force and Sense Pins. The REFCAPA and REFCAPB pins must be connected together and decoupled to AGND using a low effective series resistance (ESR), 10 µF ceramic capacitor. The voltage on the REFCAPA and REFCAPB pins is typically 4.4 V.
49	AI	V1+	Channel 1 Positive Analog Input Pin.
50	AI	V1−	Channel 1 Negative Analog Input Pin.
51	AI	V2+	Channel 2 Positive Analog Input Pin.
52	AI	V2−	Channel 2 Negative Analog Input Pin.
53	AI	V3+	Channel 3 Positive Analog Input Pin.
54	AI	V3−	Channel 3 Negative Analog Input Pin.
55	AI	V4+	Channel 4 Positive Analog Input Pin.
56	AI	V4−	Channel 4 Negative Analog Input Pin.
57	AI	V5+	Channel 5 Positive Analog Input Pin.

Pin No.	Type[1]	Mnemonic	Description
58	AI	V5−	Channel 5 Negative Analog Input Pin.
59	AI	V6+	Channel 6 Positive Analog Input Pin.
60	AI	V6−	Channel 6 Negative Analog Input Pin.
61	AI	V7+	Channel 7 Positive Analog Input Pin.
62	AI	V7−	Channel 7 Negative Analog Input Pin.
63	AI	V8+	Channel 8 Positive Analog Input Pin.
64	AI	V8−	Channel 8 Negative Analog Input Pin.

[1] P is power supply, DI is digital input, DO is digital output, REF is reference input/output, AI is analog input, and GND is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

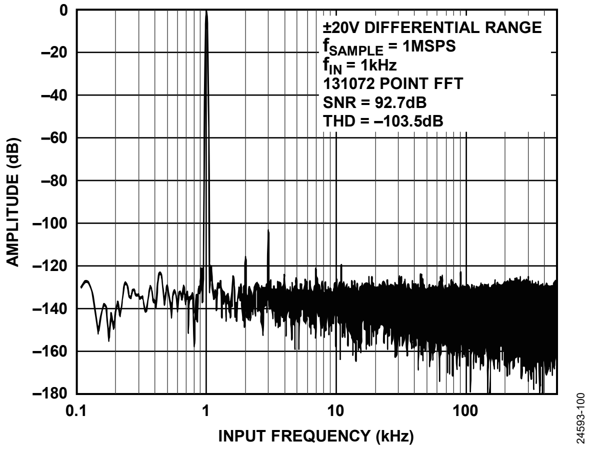


Figure 9. Fast Fourier Transform (FFT), ±20 V Differential Range, Low Bandwidth Mode

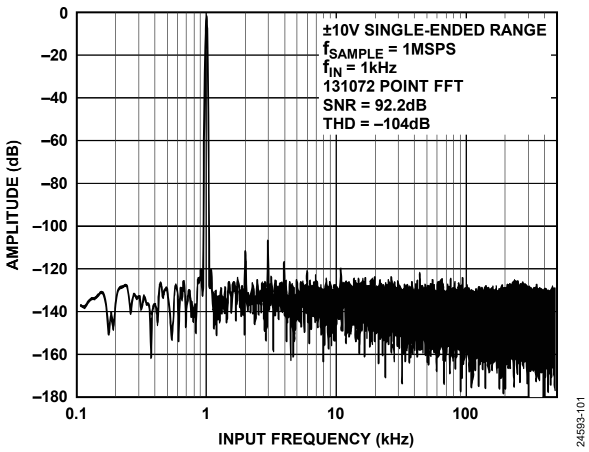


Figure 10. FFT, ±10 V Single-Ended Range, Low Bandwidth Mode

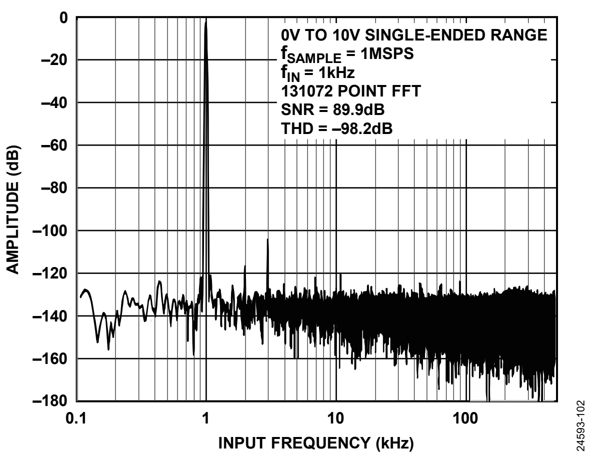


Figure 11. FFT, 0 V to 10 V Single-Ended Range, Low Bandwidth Mode

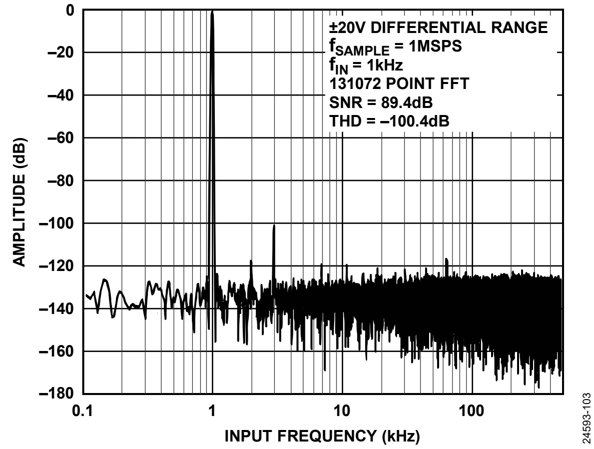


Figure 12. FFT, ±20 V Differential Range, High Bandwidth Mode

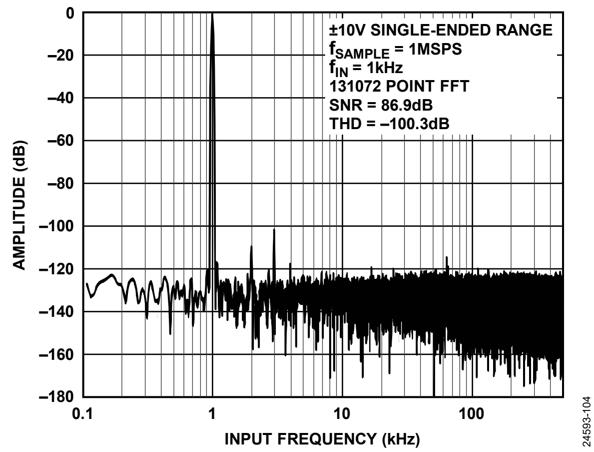


Figure 13. FFT, ±10 V Single-Ended Range, High Bandwidth Mode

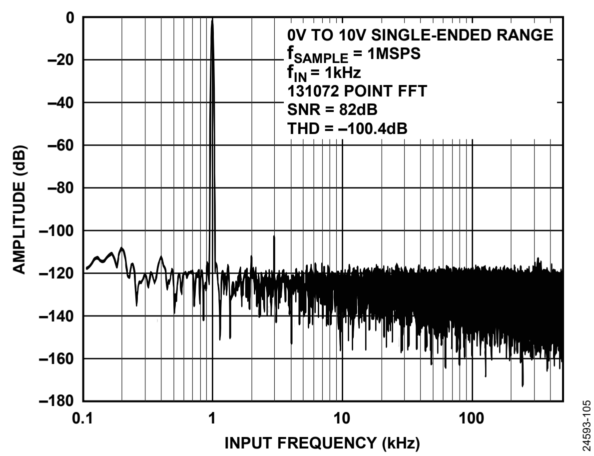


Figure 14. FFT, 0 V to 10 V Single-Ended Range, High Bandwidth Mode

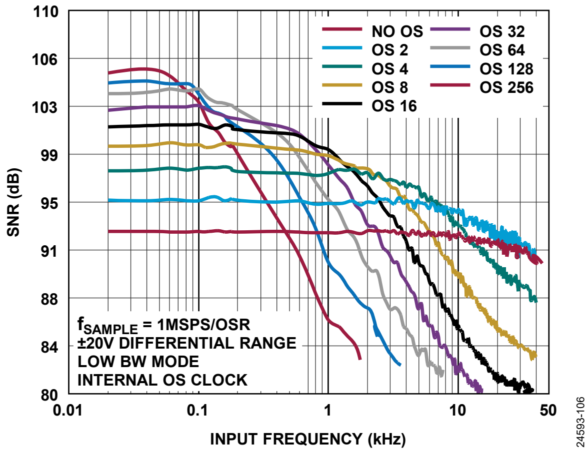


Figure 15. SNR vs. Input Frequency for Different Oversampling Ratio (OSR) Values, ±20 V Differential Range, Low Bandwidth Mode, Internal Oversampling Clock (OS = Oversampling)

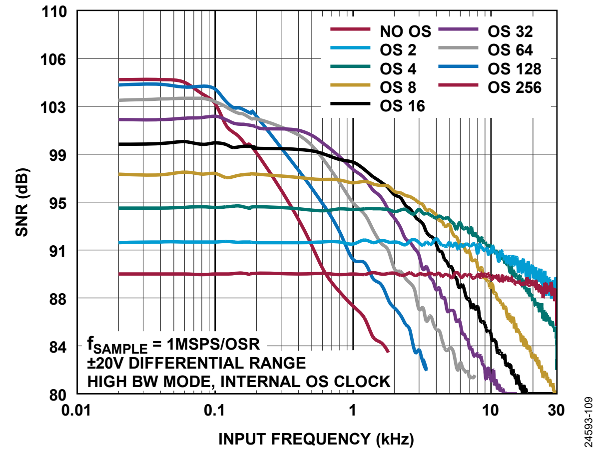


Figure 18. SNR vs. Input Frequency for Different OSR Values, ±20 V Differential Range, High Bandwidth Mode, Internal Oversampling Clock

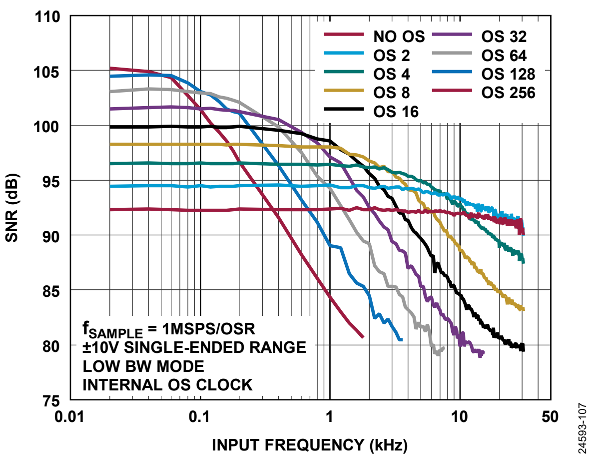


Figure 16. SNR vs. Input Frequency for Different OSR Values, ±10 V Single-Ended Range, Low Bandwidth Mode, Internal Oversampling Clock

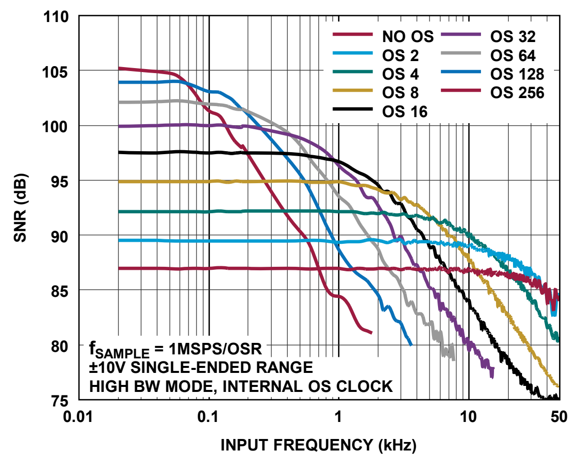


Figure 19. SNR vs. Input Frequency for Different OSR Values, ±10 V Single-Ended Range, High Bandwidth Mode, Internal Oversampling Clock

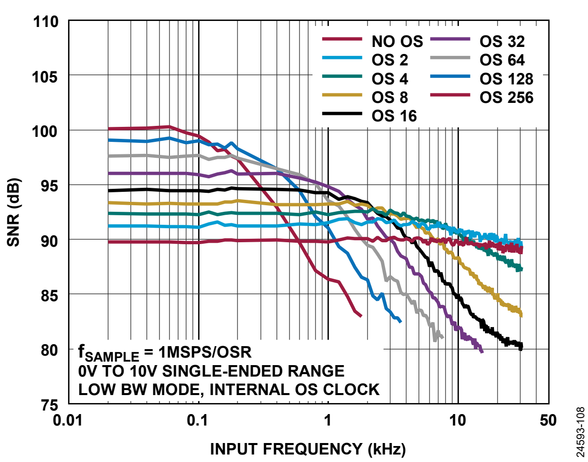


Figure 17. SNR vs. Input Frequency for Different OSR Values, 0 V to 10 V Single-Ended Range, Low Bandwidth Mode, Internal Oversampling Clock

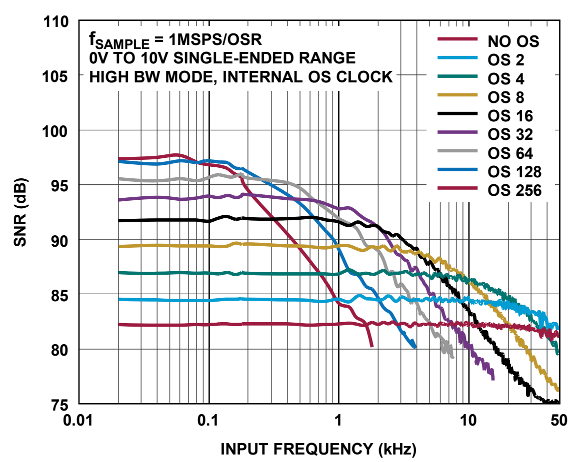


Figure 20. SNR vs. Input Frequency for Different OSR Values, 0 V to 10 V Single-Ended Range, High Bandwidth Mode, Internal Oversampling Clock

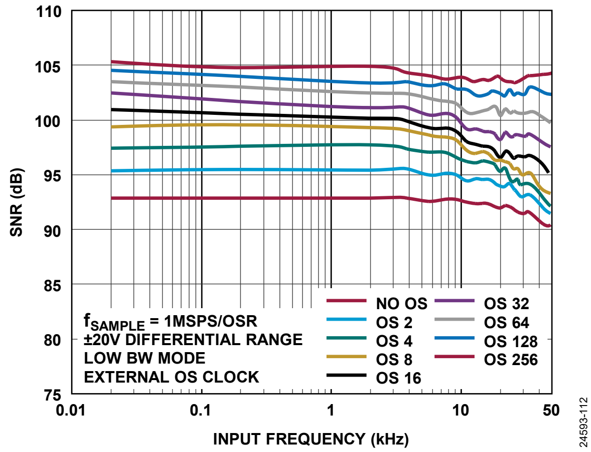


Figure 21. SNR vs. Input Frequency for Different OSR Values, ±20 V Differential Range, Low Bandwidth Mode, External Oversampling Clock

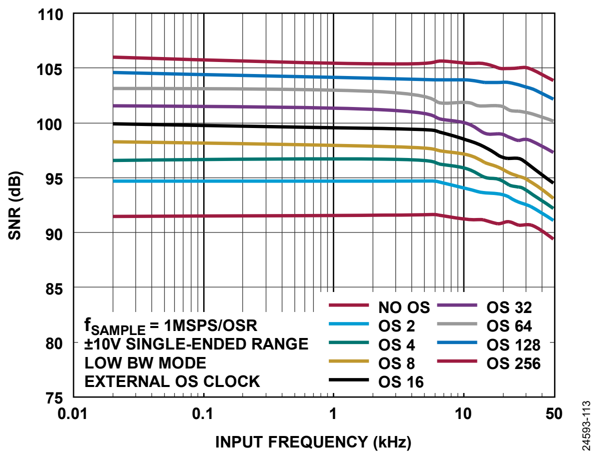


Figure 22. SNR vs. Input Frequency for Different OSR Values, ±10 V Single-Ended Range, Low Bandwidth Mode, External Oversampling Clock

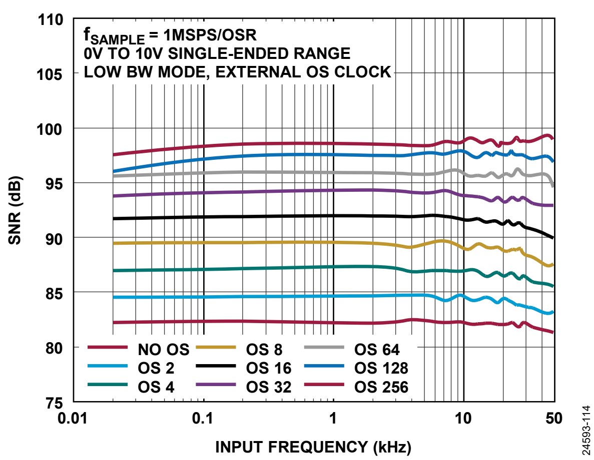


Figure 23. SNR vs. Input Frequency for Different OSR Values, 0 V to 10 V Single-Ended Range, Low Bandwidth Mode, External Oversampling Clock

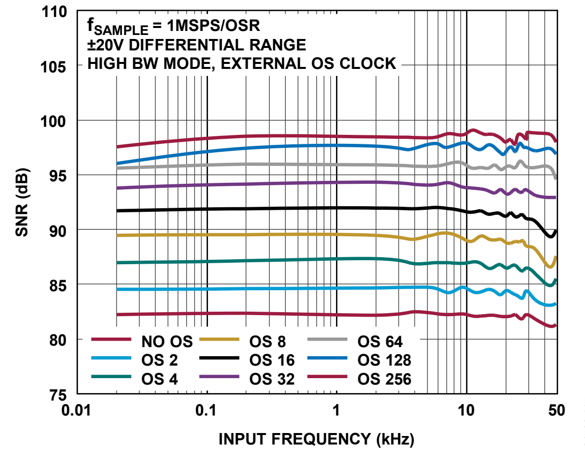


Figure 24. SNR vs. Input Frequency for Different OSR Values, ±20 V Differential Range, High Bandwidth Mode, External Oversampling Clock

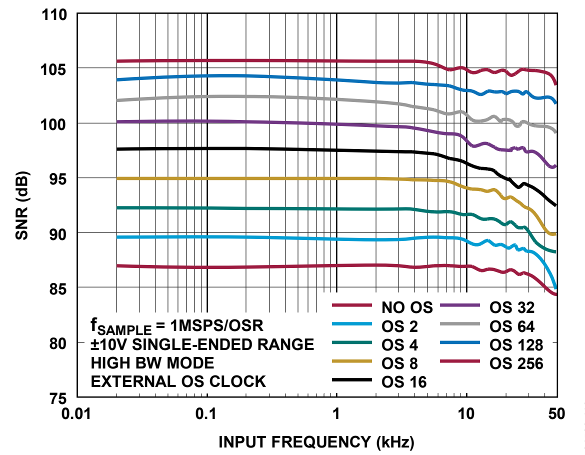


Figure 25. SNR vs. Input Frequency for Different OSR Values, ±10 V Single-Ended Range, High Bandwidth Mode, External Oversampling Clock

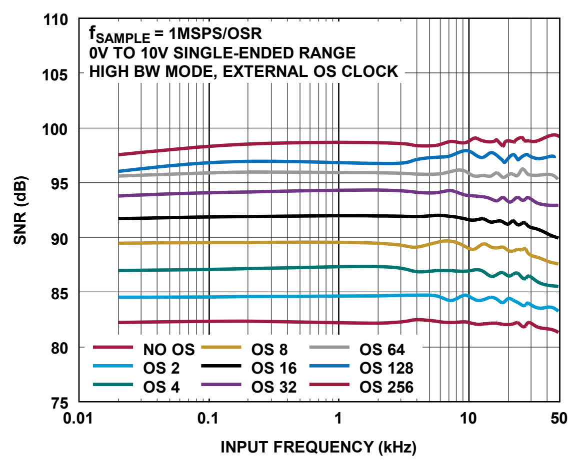


Figure 26. SNR vs. Input Frequency for Different OSR Values, 0 V to 10 V Single-Ended Range, High Bandwidth Mode, External Oversampling Clock

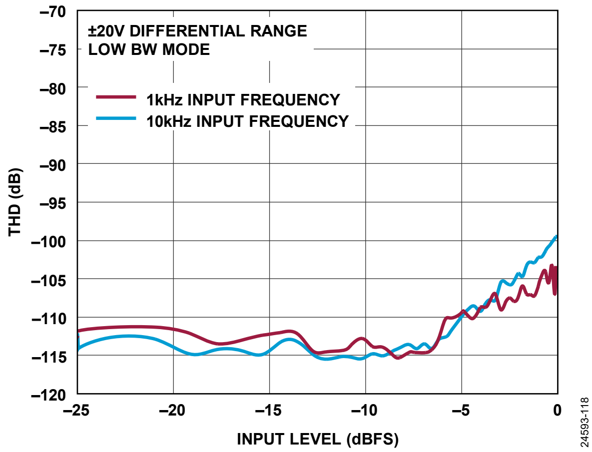


Figure 27. THD vs. Input Level, ±20 V Differential Range, Low Bandwidth Mode

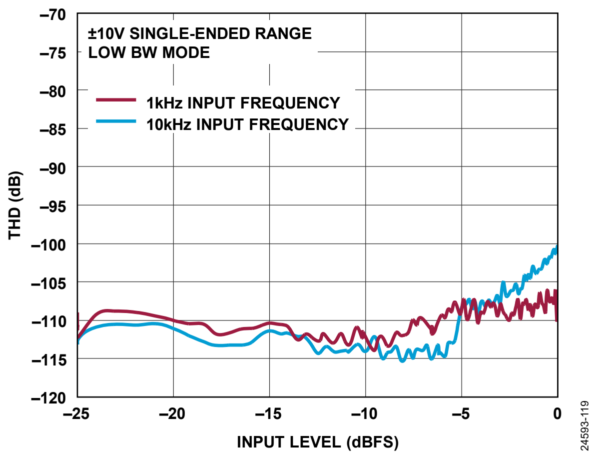


Figure 28. THD vs. Input Level, ±10 V Single-Ended Range, Low Bandwidth Mode

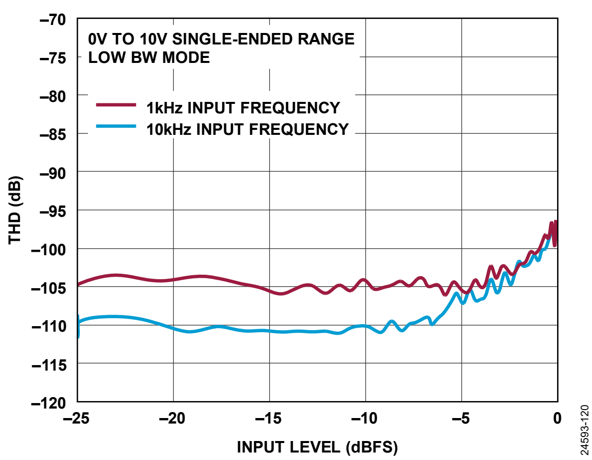


Figure 29. THD vs. Input Level, 0 V to 10 V Single-Ended Range, Low Bandwidth Mode

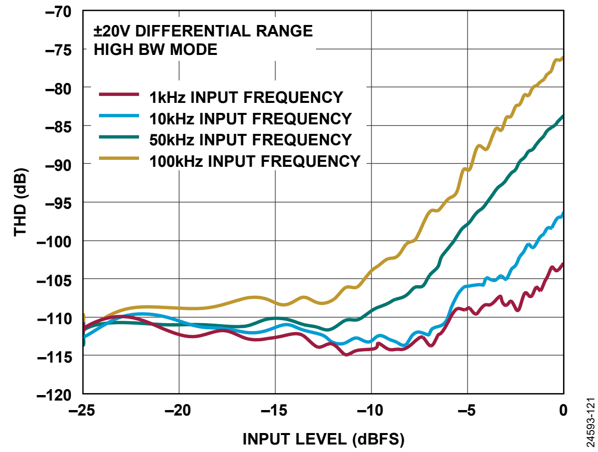


Figure 30. THD vs. Input Level, ±20 V Differential Range, High Bandwidth Mode

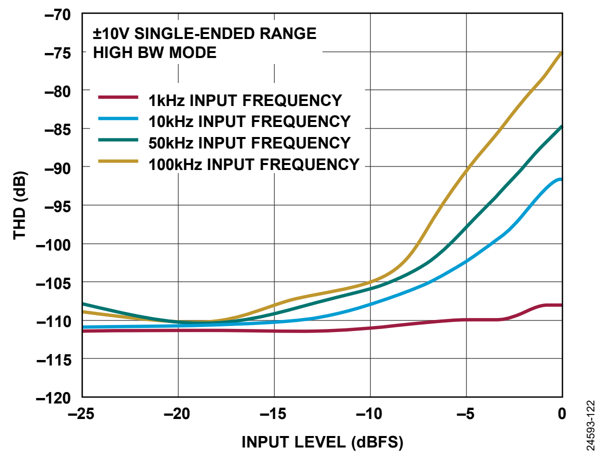


Figure 31. THD vs. Input Level, ±10 V Single-Ended Range, High Bandwidth Mode

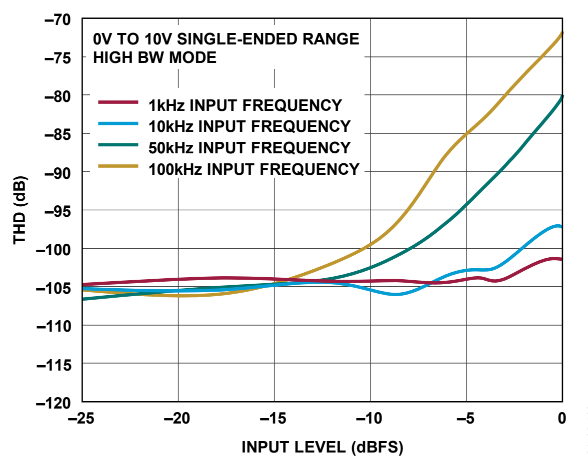


Figure 32. THD vs. Input Level, 0 V to 10 V Single-Ended Range, High Bandwidth Mode

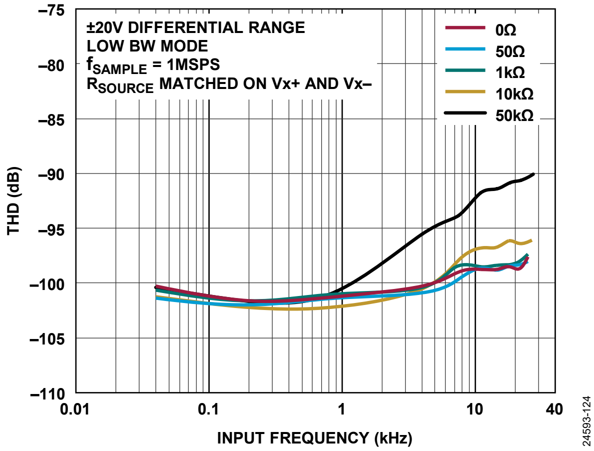


Figure 33. THD vs. Input Frequency for Various Source Impedances (R_{SOURCE}), ±20 V Differential Range, Low Bandwidth Mode

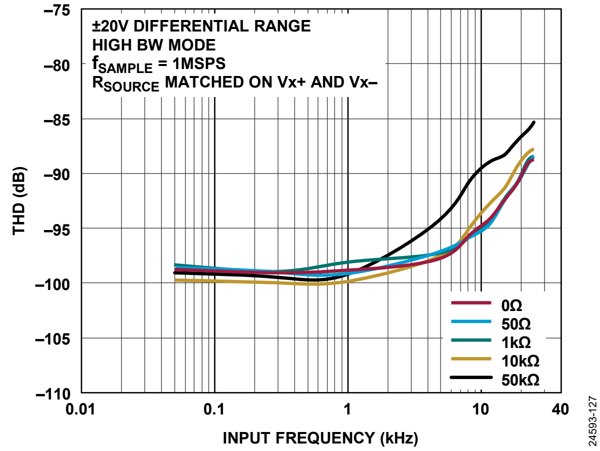


Figure 36. THD vs. Input Frequency for Various Source Impedances, ±20 V Differential Range, High Bandwidth Mode

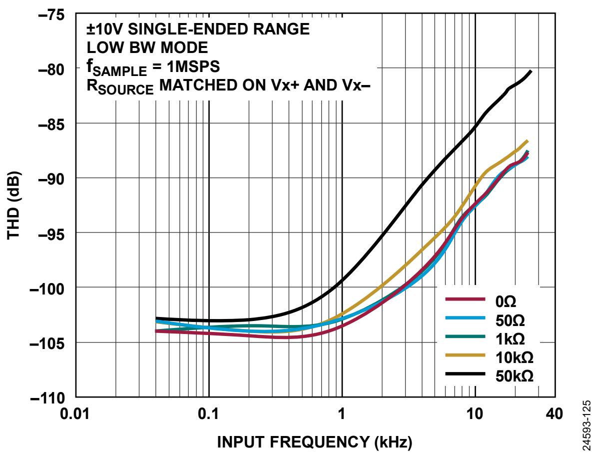


Figure 34. THD vs. Input Frequency for Various Source Impedances, ±10 V Single-Ended Range, Low Bandwidth Mode

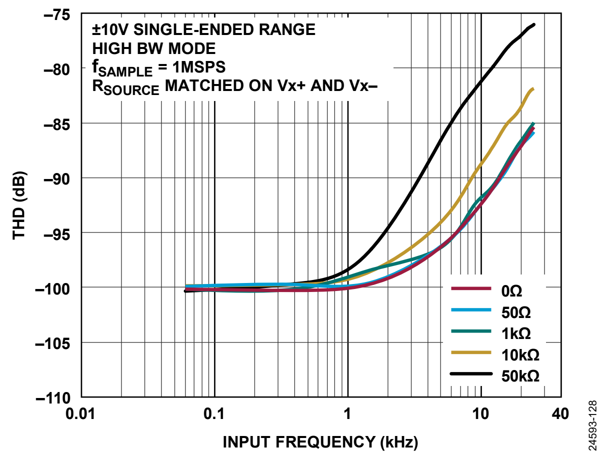


Figure 37. THD vs. Input Frequency for Various Source Impedances, ±10 V Single-Ended Range, High Bandwidth Mode

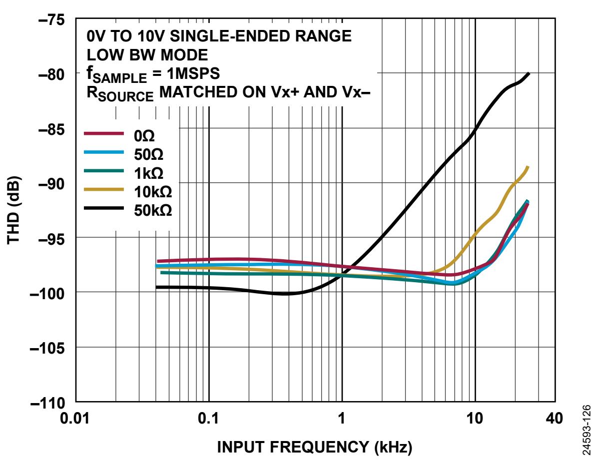


Figure 35. THD vs. Input Frequency for Various Source Impedances, 0 V to 10 V Single-Ended Range, Low Bandwidth Mode

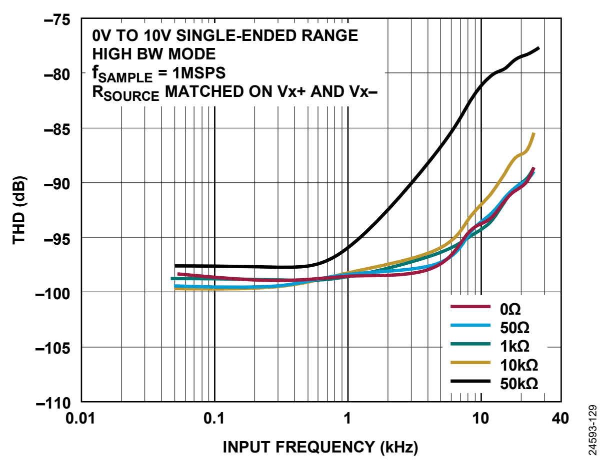


Figure 38. THD vs. Input Frequency for Various Source Impedances, 0 V to 10 V Single-Ended Range, High Bandwidth Mode

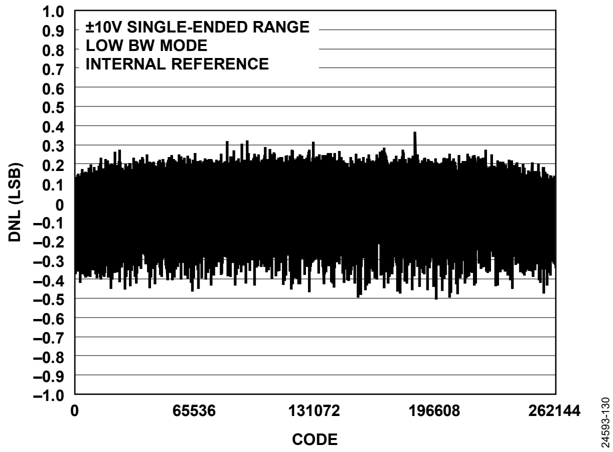


Figure 39. Typical DNL, Low Bandwidth Mode

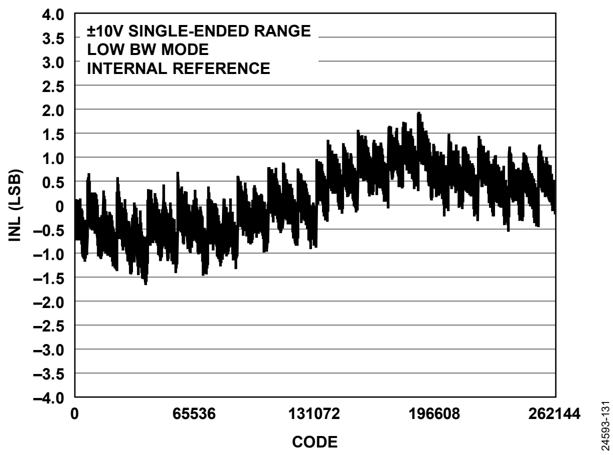


Figure 40. Typical INL, Low Bandwidth Mode

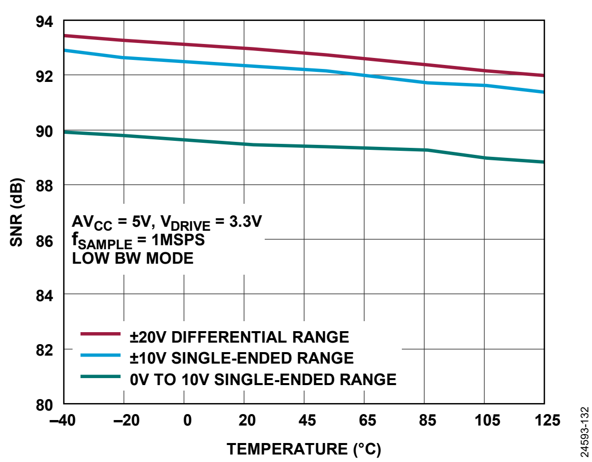


Figure 41. SNR vs. Temperature, Low Bandwidth Mode

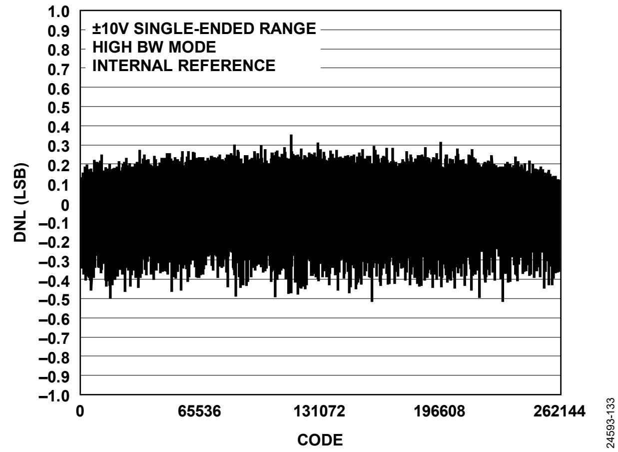


Figure 42. Typical DNL, High Bandwidth Mode

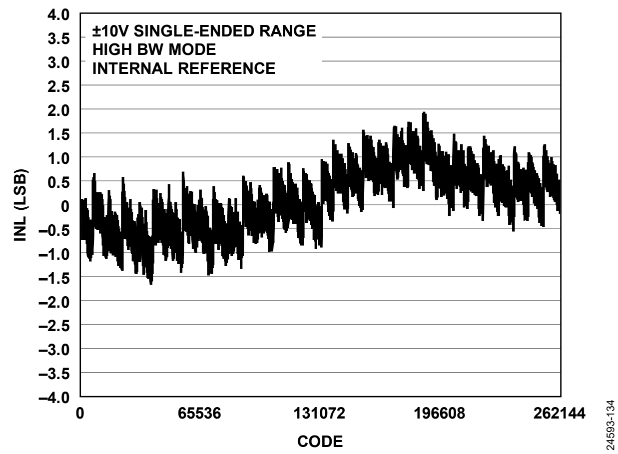


Figure 43. Typical INL, High Bandwidth Mode

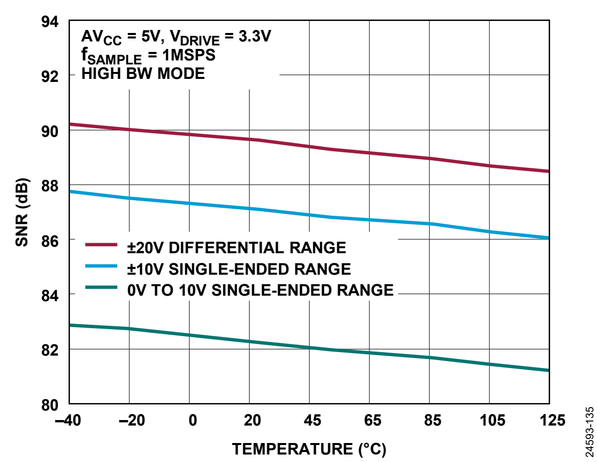


Figure 44. SNR vs. Temperature, High Bandwidth Mode

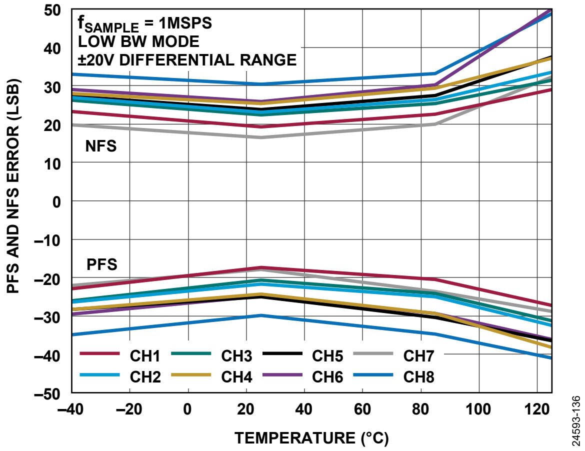


Figure 45. Positive Full-Scale (PFS) and Negative Full-Scale (NFS) Error vs. Temperature, ±20 V Differential Range

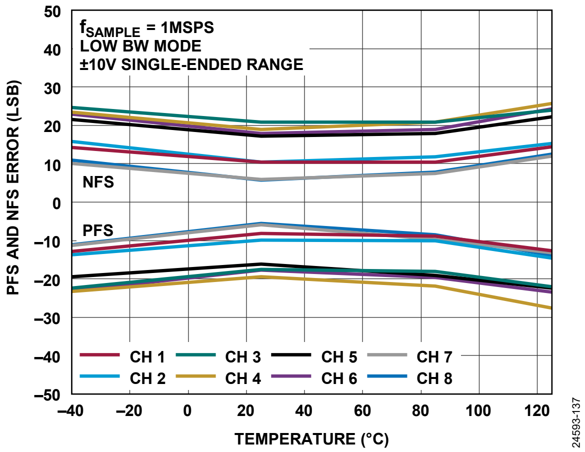


Figure 46. PFS and NFS Error vs. Temperature, ±10 V Single-Ended Range

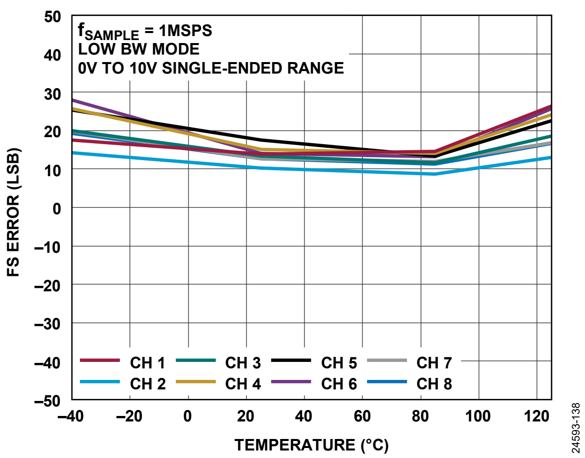


Figure 47. FS Error vs. Temperature, 0 V to 10 V Single-Ended Range

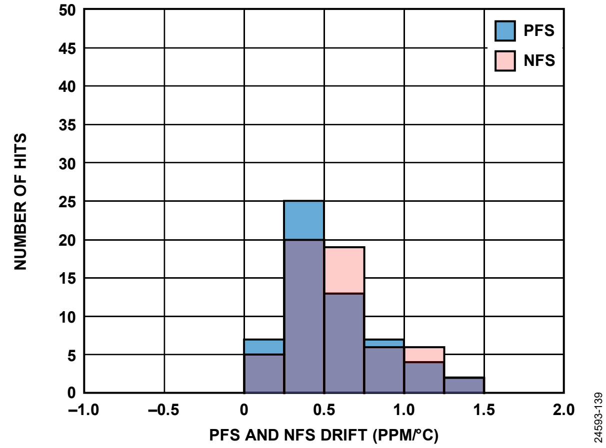


Figure 48. PFS and NFS Drift Histogram, ±10 V Single-Ended Range

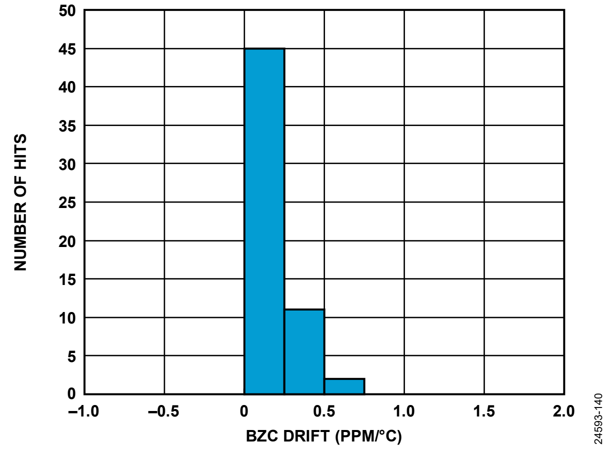


Figure 49. Bipolar Zero Code (BZC) Drift Histogram, ±10 V Single-Ended Range

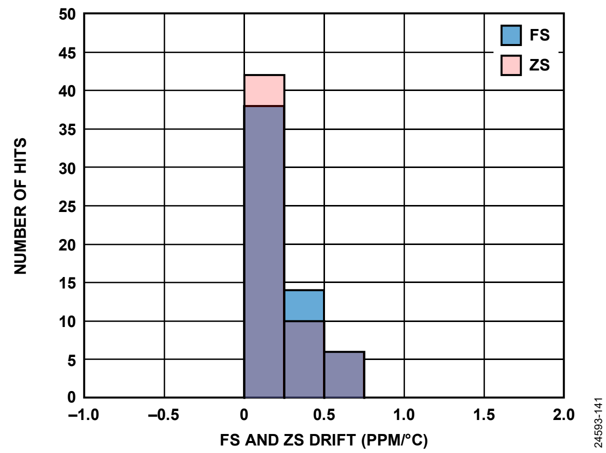


Figure 50. FS and Zero-Scale (ZS) Drift Histogram, 0 V to 10 V Single-Ended Range

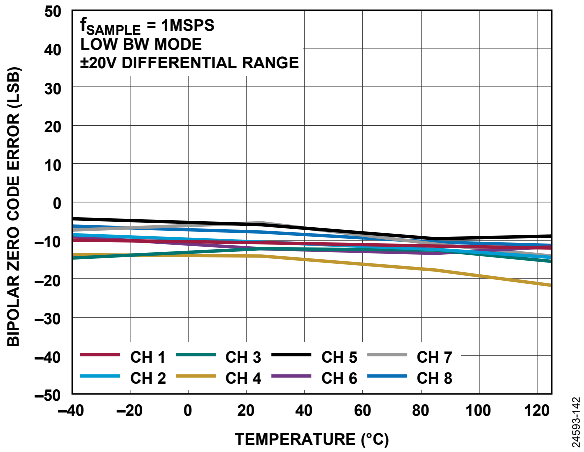


Figure 51. Bipolar Zero Code Error vs. Temperature, ±20 V Differential Range

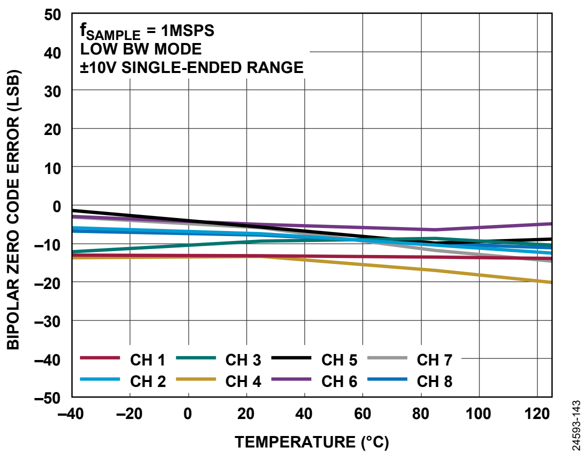


Figure 52. Bipolar Zero Code Error vs. Temperature, ±10 V Single-Ended Range

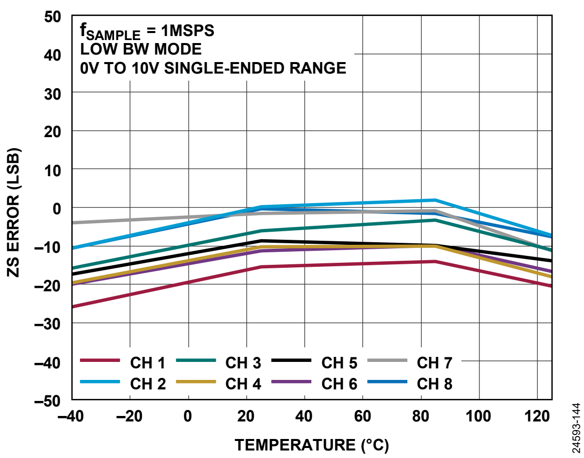


Figure 53. ZS Error vs. Temperature, 0 V to 10 V Single-Ended Range

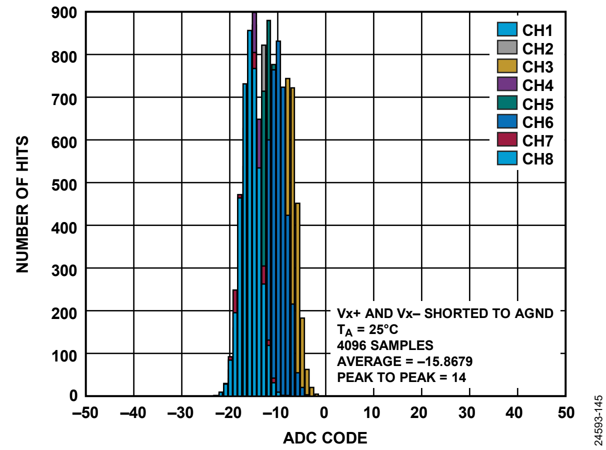


Figure 54. Histogram of Codes, ±20 V Differential Range

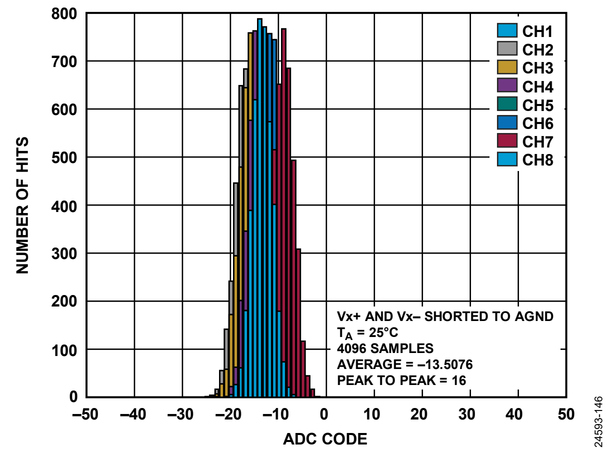


Figure 55. Histogram of Codes, ±10 V Single-Ended Range

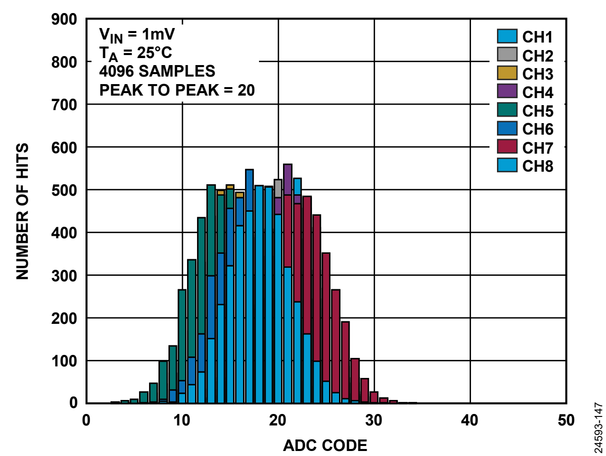


Figure 56. Histogram of Codes, 0 V to 10 V Single-Ended Range

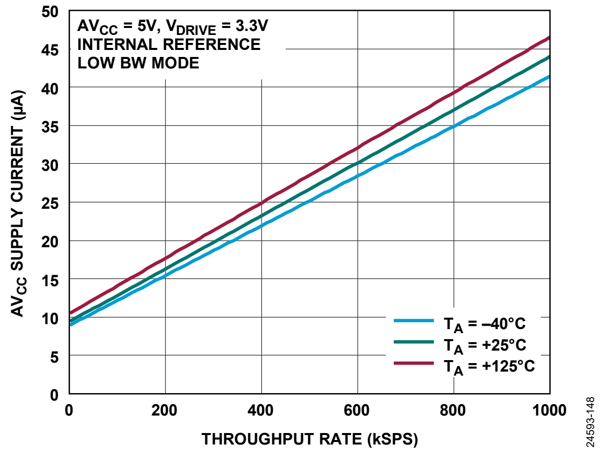


Figure 57. AV_{CC} Supply Current vs. Throughput Rate for Various Temperatures

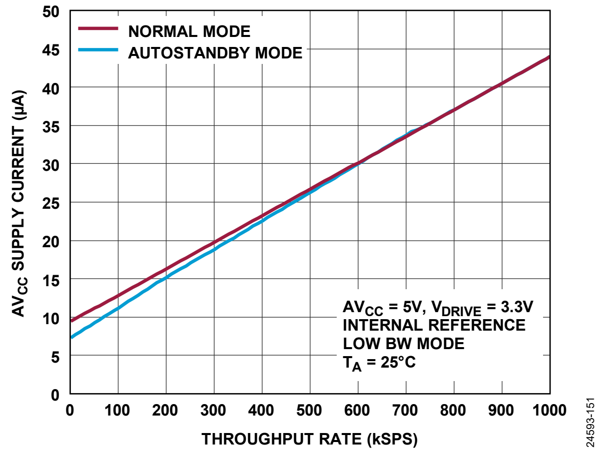


Figure 60. AV_{CC} Supply Current vs. Throughput Rate, Normal Mode and Autostandby Mode

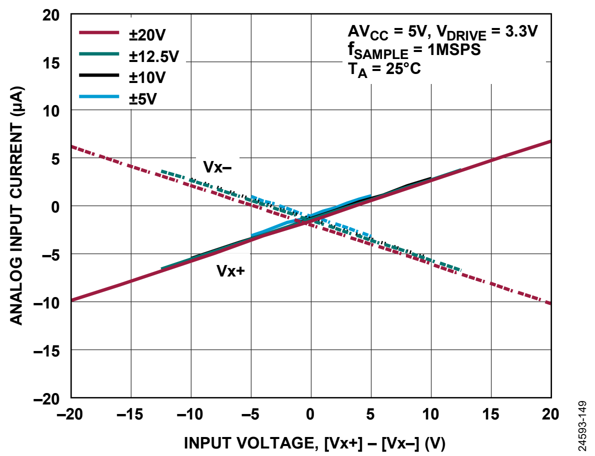


Figure 58. Analog Input Current vs. Input Voltage for Various Differential Ranges

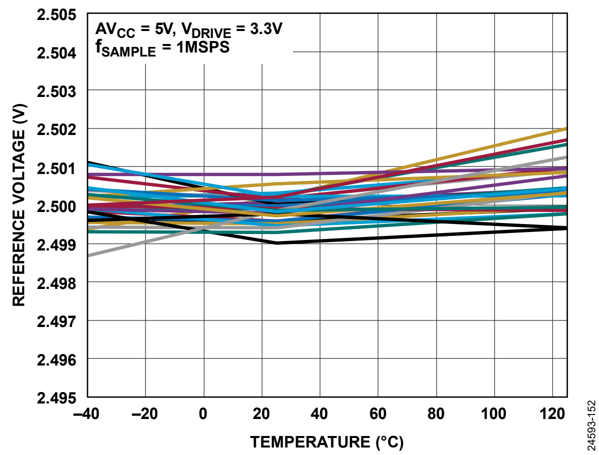


Figure 61. Reference Drift

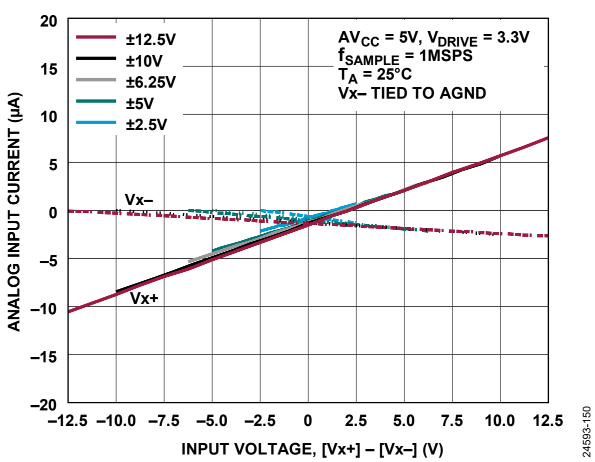


Figure 59. Analog Input Current vs. Input Voltage for Various Bipolar Single-Ended Ranges

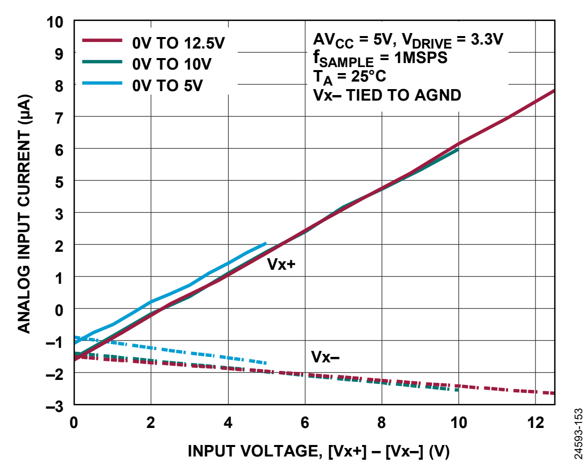


Figure 62. Analog Input Current vs. Input Voltage for Various Unipolar Single-Ended Ranges

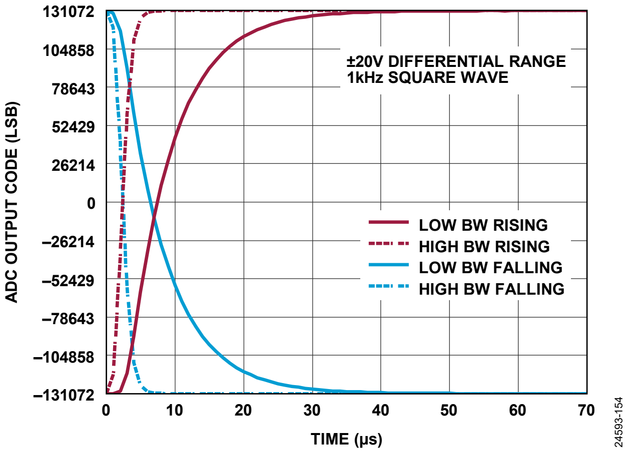


Figure 63. Step Response, ±20 V Differential Range

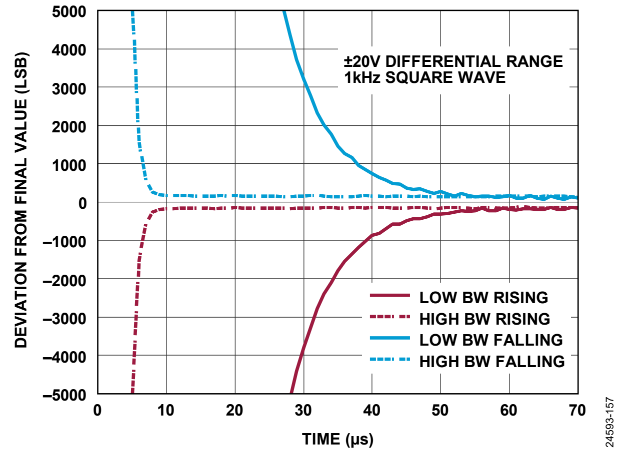


Figure 66. Step Response, ±20 V Differential Range, Fine Settling

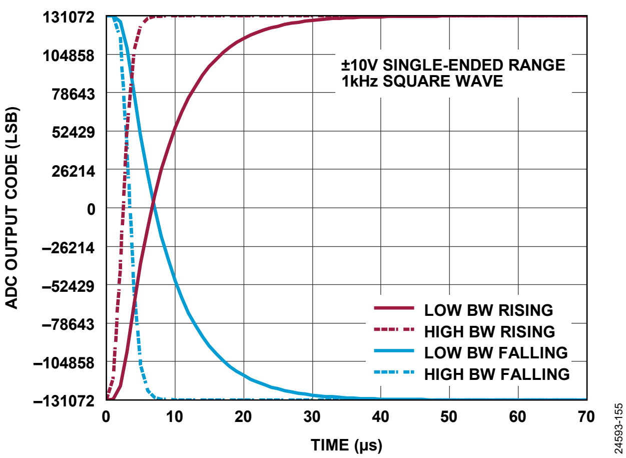


Figure 64 Step Response, ±10 V Single-Ended Range

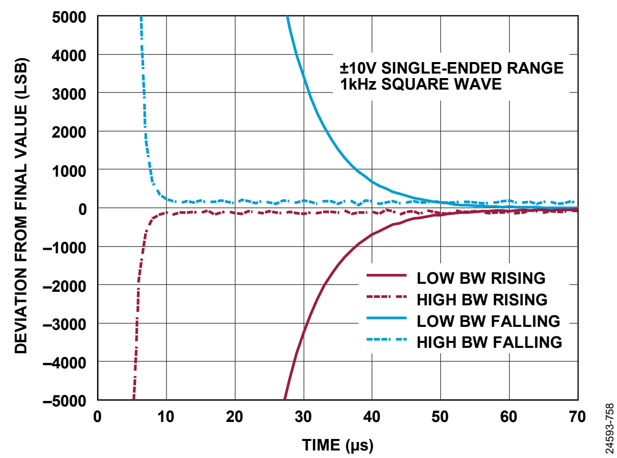


Figure 67. Step Response, ±10 V Single-Ended Range, Fine Settling

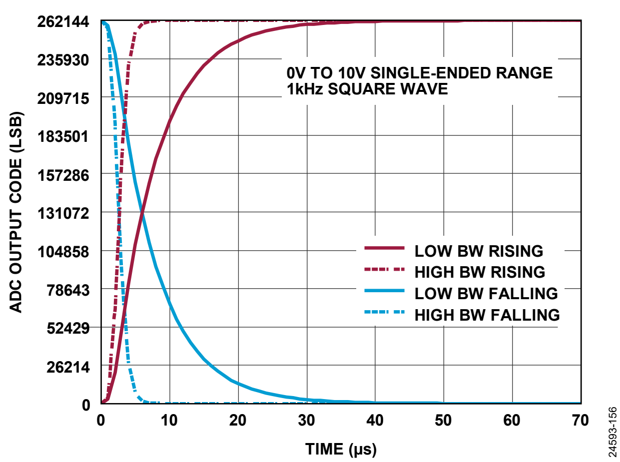


Figure 65. Step Response, 0 V to 10 V Single-Ended Range

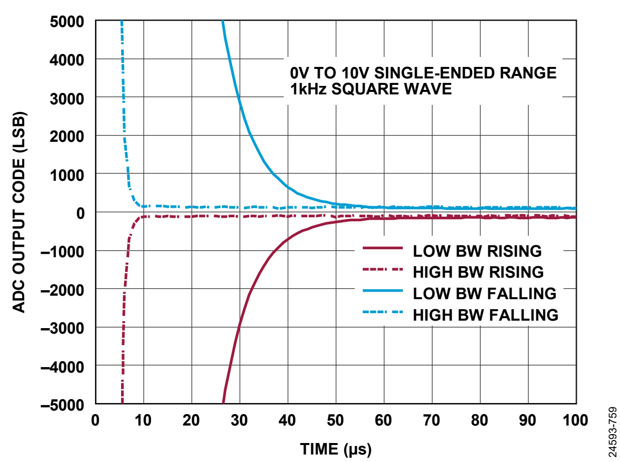


Figure 68. Step Response, 0 V to 10 V Single-Ended Range, Fine Settling

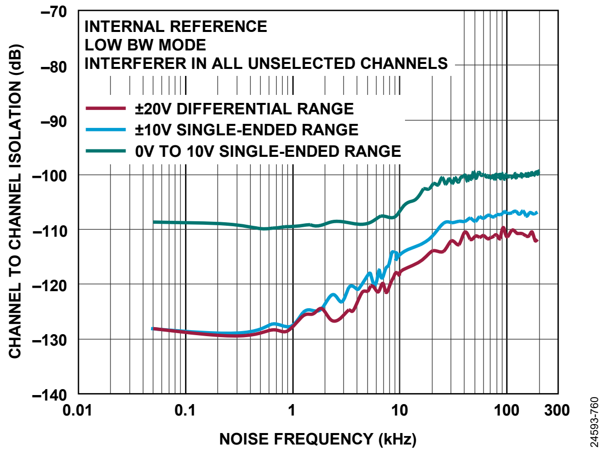


Figure 69. Channel to Channel Isolation vs. Noise Frequency, Low Bandwidth Mode

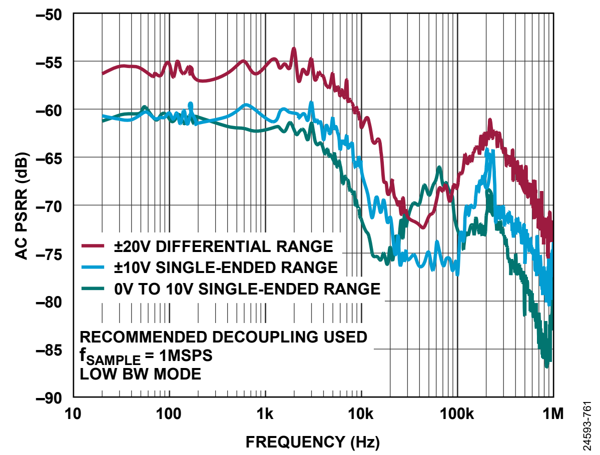


Figure 70. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, Low Bandwidth Mode

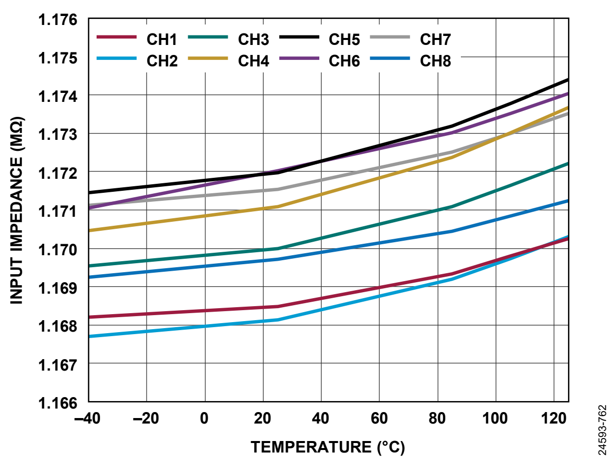


Figure 71. Input Impedance vs. Temperature

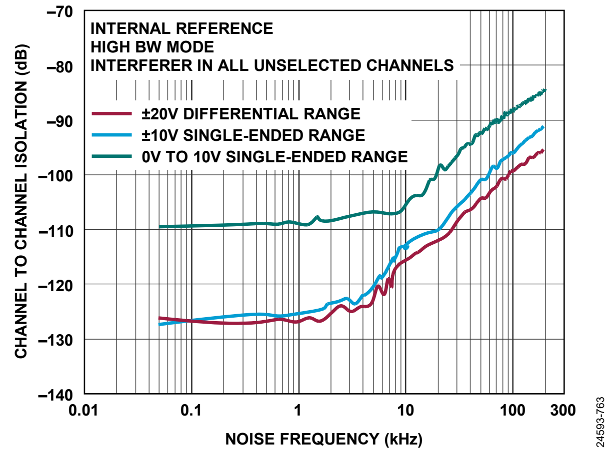


Figure 72. Channel to Channel Isolation vs. Noise Frequency, High Bandwidth Mode

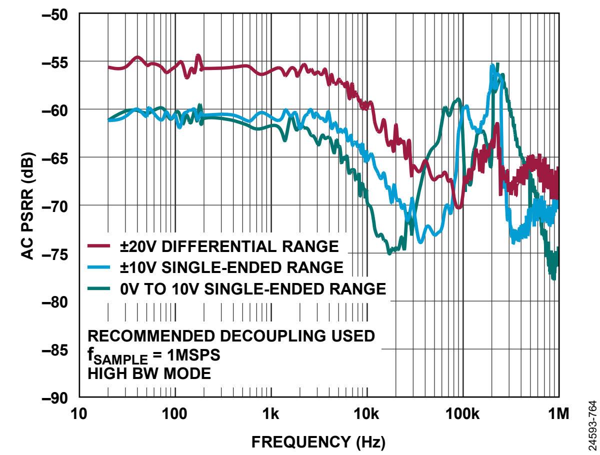


Figure 73. AC PSRR vs. Frequency, High Bandwidth Mode

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at ½ LSB below the first code transition and full scale at ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
Bipolar zero code error is the deviation of the midscale transition (all 1s to all 0s) from the ideal, which is 0 V − ½ LSB.

Bipolar Zero Code Error Matching
Bipolar zero code error matching is the absolute difference in bipolar zero code error between any two input channels.

Open Circuit Code Error
Open circuit code error is the ADC output code when there is an open circuit on the analog input and a pull-down resistor (R_{PD}) connected between the analog input pair of pins. See Figure 95 for more details.

Positive Full-Scale (PFS) Error
In bipolar ranges, PFS error is the deviation of the actual last code transition from the ideal last code transition (for example, 10 V – 1½ LSB (9.99988), 5 V – 1½ LSB (4.99994), or 2.5 V – 1½ LSB (2.49997)) after the bipolar zero code error is adjusted out. The PFS error includes the contribution from the reference buffer.

Positive Full-Scale (PFS) Error Matching
PFS error matching is the absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale (NFS) Error
In bipolar ranges, NFS error is the deviation of the first code transition from the ideal first code transition (for example, −10 V + ½ LSB (−9.99996), −5 V + ½ LSB (−4.99998), or −2.5 V + ½ LSB (−2.49999)) after the bipolar zero code error is adjusted out. The NFS error includes the contribution from the reference buffer.

Negative Full-Scale (NFS) Error Matching
NFS error matching is the absolute difference in negative full-scale error between any two input channels.

Full-Scale (FS) Error
In unipolar ranges, FS error is the deviation of the actual last code transition from the ideal last code transition (for example, 10 V – 1½ LSB (9.99954), or 5 V – 1½ LSB (4.99977)) after the zero scale error is adjusted out. The FS error includes the contribution from the reference buffer

Zero Scale (ZS) Error
In unipolar ranges, ZS error is the deviation of the first code transition from the ideal first code transition, which is 0 V − ½ LSB.

Total Unadjusted Error (TUE)
TUE is the maximum deviation of the output code from the ideal. TUE includes INL errors, bipolar zero code and positive and negative full-scale errors, and reference errors.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD ratio is the measured ratio of signal-to-noise-and-distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half of the sampling frequency ($f_S/2$, excluding dc).

The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise.

The theoretical SINAD for an ideal N-bit converter with a sine wave input is given by

$$SINAD = (6.02N + 1.76) \text{ dB}$$

Thus, for a 16-bit converter, the SINAD is 98 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the harmonics to the fundamental. For the AD7606C-18, it is defined as

$$THD \text{ (dB)} = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1}$$

where:
V_2 to V_9 are the rms amplitudes of the second through ninth harmonics.
V_1 is the rms amplitude of the fundamental.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the value is determined by a noise peak.

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. The power supply rejection (PSR) is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSRR is defined as the ratio of the 100 mV p-p sine wave applied to the AV_{CC} supplies of the ADC frequency, f_S, to the power of the ADC output at that frequency, f_S.

$$PSRR \text{ (dB)} = 20 \log (0.1/Pf_S)$$

where:
Pf_S is equal to the power at frequency, f_S, coupled onto the AV_{CC} supply.

Channel to Channel Isolation

Channel to channel isolation is a measure of the level of crosstalk between all input channels. It is measured by applying a full-scale sine wave signal, up to 200 kHz, to all unselected input channels and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied (see Figure 58).

Phase Delay

Phase delay is a measure of the absolute time delay between when an input is sampled by the converter and when the result associated with that sample is available to be read back from the ADC, including delay induced by the analog front end of the device.

Phase Delay Drift

Phase delay drift is the change in phase delay per unit temperature across the entire operating temperature of the device.

Phase Delay Matching

Phase delay matching is the maximum phase delay seen between any simultaneously sampled pair.

Box Method

The box method is represented by the following equation:

$$TCV_{OUT} = \left| \frac{max\{V_{OUT}(T_1, T_2, T_3)\} - min\{V_{OUT}(T_1, T_2, T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_1)} \right| \times 10^6$$

where:
TCV_{OUT} is expressed in ppm/°C.
$V_{OUT}(T_X)$ is the output voltage at temperature T_X.
T_1 = −40°C.
T_2 = +25°C.
T_3 = +125°C.

This box method ensures that TCV_{OUT} accurately portrays the maximum difference between any of the three temperatures at which the output voltage of the device is measured.

THEORY OF OPERATION

ANALOG FRONT-END

The AD7606C-18 is an 18-bit, simultaneous sampling, analog-to-digital DAS with eight channels. Each channel contains analog input clamp protection, a PGA, an LPF, and an 18-bit SAR ADC.

Analog Input Ranges

The AD7606C-18 can handle true bipolar differential, bipolar single-ended, and unipolar single-ended input voltages. In software mode, it is possible to configure an individual analog input range per channel, from Address 0x03 through Address 0x06. The logic level on the RANGE pin is ignored in software mode.

In hardware mode, the logic level on the RANGE pin determines either ±10 V or ±5 V single-ended as the analog input range of all analog input channels, as shown in Table 10.

A logic change on the RANGE pin has an immediate effect on the analog input range. However, there is typically a settling time of approximately 80 µs in addition to the normal acquisition time requirement. Changing the RANGE pin during a conversion is not recommended for fast throughput rate applications.

Table 10. Analog Input Range Selection

Range (V)	Hardware Mode[1]	Software Mode[2]
±10 Single-Ended	RANGE pin high	Address 0x03 through Address 0x06
±5 Single-Ended	RANGE pin low	Address 0x03 through Address 0x06
Any Other Range	Not applicable	Address 0x03 through Address 0x06

[1] The same analog input range, ±10 V or ±5 V, applies to all eight channels.
[2] The analog input range is selected on a per channel basis using the memory map.

Analog Input Impedance

The analog input impedance of the AD7606C-18 is 1 MΩ minimum. This is a fixed input impedance that does not vary with the AD7606C-18 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7606C-18, allowing direct connection to the source or sensor. Therefore, bipolar supplies can be removed from the signal chain.

Analog Input Clamp Protection

Figure 74 shows the analog input circuitry of the AD7606C-18. Each analog input of the AD7606C-18 contains clamp protection circuitry. Despite single, 5 V supply operation, the analog input clamp protection allows an input overvoltage of up to ±21 V.

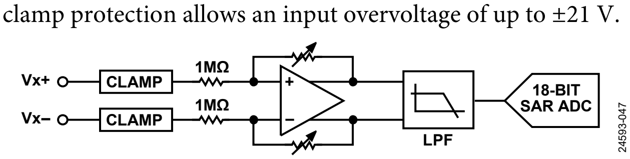


Figure 74. Analog Input Circuitry for Each Channel

Figure 75 shows the input clamp current vs. the source voltage characteristic of the clamp circuit. For input voltages of up to ±21 V, no current flows in the clamp circuit. For input voltages that are above ±21 V, the AD7606C-18 clamp circuitry turns on.

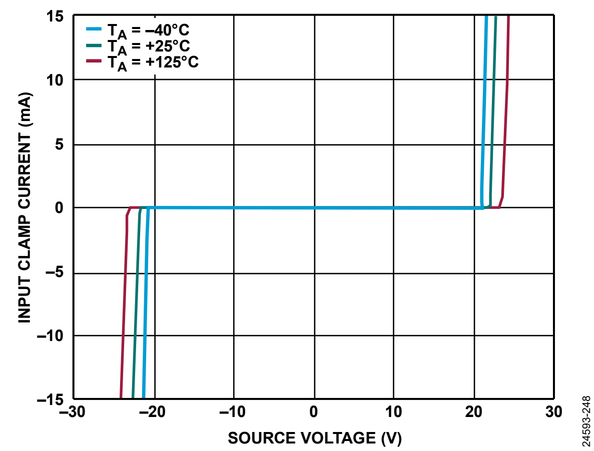


Figure 75. Input Protection Clamp Profile

It is recommended to place a series resistor on the analog input channels to limit the current to ±10 mA for input voltages greater than ±21 V. In an application where there is a series resistance (R) on an analog input channel, Vx+, it is recommended to match the resistance (R) with the resistance on Vx– to eliminate any offset introduced into the system, as shown in Figure 76. However, in software mode, there is a per channel system offset calibration that removes the offset of the full system (see the System Offset Calibration section).

During normal operation, it is not recommended to leave the AD7606C-18 in a condition where the analog input is greater than the input range for extended periods of time because this can degrade the bipolar zero code error performance. In shutdown or standby mode, there is no such concern.

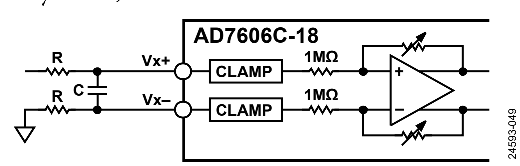


Figure 76. Input Resistance Matching on the Analog Input of the AD7606C-18 for Single-Ended Ranges (Vx– Tied to Ground)

PGA

A PGA is provided at each input channel. The gain is configured depending on the analog input range selected (see Table 10) to scale the analog input signal, either bipolar differential or bipolar or unipolar single-ended, to the ADC fully differential input range.

Input impedance on each input of the PGA is accurately trimmed to keep overall gain error. This trimmed value is then used when the gain calibration is enabled to compensate for the gain error introduced by an external series resistor. See the System Gain Calibration section for more information on the PGA feature.

Analog Input Antialiasing Filter

An analog antialiasing filter is provided on the AD7606C-18. Figure 77 and Figure 78 show the frequency response and phase response, respectively, of the analog antialiasing filter. The −3 dB frequency is typically 25 kHz.

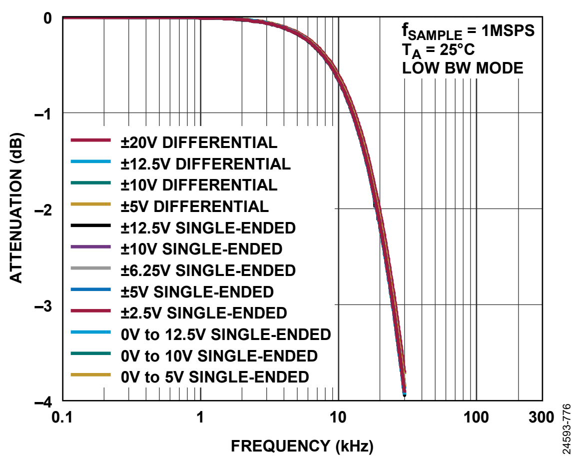


Figure 77. Analog Antialiasing Filter Frequency Response, Low Bandwidth Mode

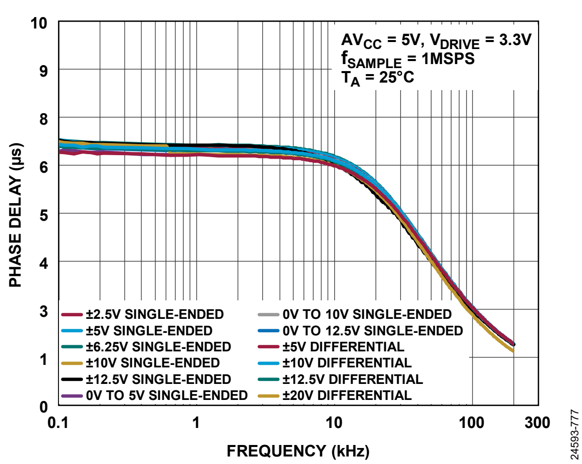


Figure 78. Analog Antialiasing Filter Phase Response, Low Bandwidth Mode

In addition, the AD7606C-18 allows the ADC to enable the high bandwidth mode, on a per channel basis, that moves the −3 dB frequency up to 220 kHz, as shown in Figure 79 and Figure 80. This mode is dedicated for fast analog input settling applications, as shown in Figure 63 to Figure 68.

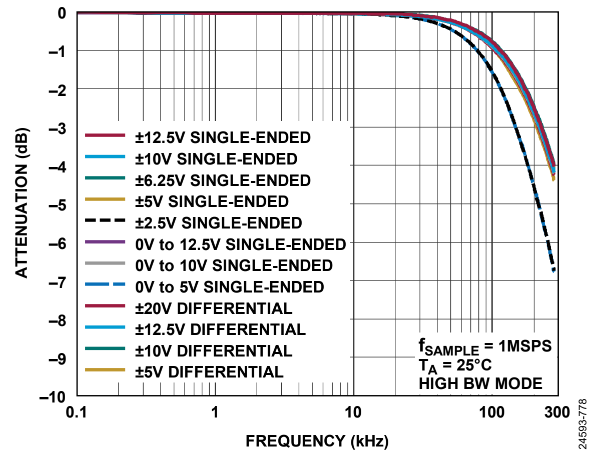


Figure 79. Analog Antialiasing Filter Frequency Response, High Bandwidth Mode

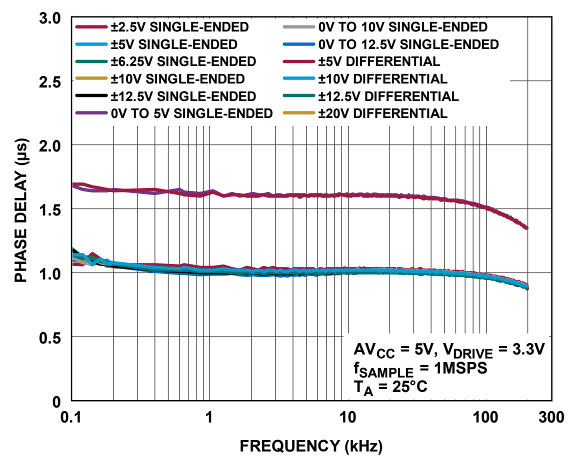


Figure 80. Analog Antialiasing Filter Phase Response, High Bandwidth Mode

SAR ADC

The AD7606C-18 allows the ADC to accurately acquire an input signal of full-scale amplitude to 18-bit resolution. All eight SAR ADCs sample their respective inputs simultaneously on the rising edge of the CONVST signal.

The BUSY signal indicates when conversions are in progress. Therefore, when the rising edge of the CONVST signal is applied, the BUSY pin goes logic high and transitions low at the end of the entire conversion process. The end of the conversion process across all eight channels is indicated by the falling edge of the BUSY signal. When the BUSY signal edge falls, the acquisition time for the next set of conversions begins. The rising edge of the CONVST signal has no effect while the BUSY signal is high.

New data can be read from the output register via the parallel or serial interface after the BUSY output goes low. Alternatively, data from the previous conversion can be read while the BUSY pin is high, as explained in the Reading During Conversion section.

The AD7606C-18 contains an on-chip oscillator that performs the conversions. The conversion time for all ADC channels is t_{CONV} (see Table 3). In software mode, there is an option to apply an external clock through the CONVST pin. Providing a low jitter external clock improves SNR performance for large oversampling ratios. See the Digital Filter section and Figure 15 to Figure 18 for further information.

Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

ADC Transfer Function

The output coding of the AD7606C-18 is twos complement for the bipolar analog input ranges, either single-ended or differential. In unipolar ranges, the output coding is straight binary.

The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is FSR/262,144 for the AD7606C-18. Figure 81 shows the ideal transfer characteristics for the AD7606C-18. The LSB size is dependent on the analog input range selected, as shown in Table 11 and Table 12.

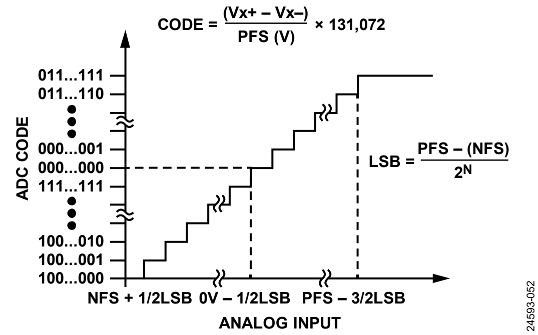


Figure 81. AD7606C-18 Ideal Transfer Characteristics, Bipolar Analog Input Ranges (Twos Complement Output Coding)

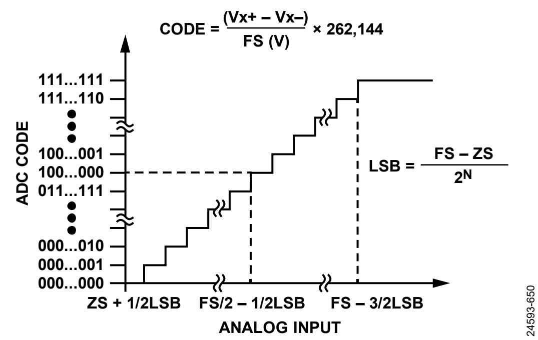


Figure 82. AD7606C-18 Ideal Transfer Characteristics, Unipolar Analog Input Ranges (Straight Binary Output Coding)

Table 11. Bipolar Input Voltage Ranges

Range	PFS (V)	Midscale (V)	NFS (V)	LSB (µV)
Differential, Bipolar				
±20 V	+20	0	−20	152.58
±12.5 V	+12.5	0	−12.5	95.36
±10 V	+10	0	−10	76.3
±5 V	+5	0	−5	38.1
Single-Ended, Bipolar				
±12.5 V	+12.5	0	−12.5	95.36
±10 V	+10	0	−10	76.3
±6.25 V	+6.25	0	−6.25	47.7
±5 V	+5	0	−5	38.1
±2.5 V	+2.5	0	−2.5	19

Table 12. Unipolar Input Voltage Ranges

Range	FS (V)	Midscale (V)	ZS (V)	LSB (µV)
Single-Ended, Unipolar				
0 V to 12.5 V	12.5	6.25	0	47.7
0 V to 10 V	10	5	0	38.1
0 V to 5 V	5	2.5	0	19

REFERENCE

The AD7606C-18 contains an on-chip, 2.5 V, band gap reference. The REFIN/REFOUT pin allows either of the following:

- Access to the internal 2.5 V reference if the REF SELECT pin is tied to logic high
- Application of an external reference of 2.5 V if the REF SELECT pin is tied to logic low

Table 13. Reference Configuration

REF SELECT Pin	Reference Selected
Logic High	Internal reference enabled
Logic Low	Internal reference disabled, an external 2.5 V reference voltage must be applied to the REFIN/REFOUT pin

The AD7606C-18 contains a reference buffer configured to gain the reference voltage up to approximately 4.4 V, as shown in Figure 83. The 4.4 V buffered reference is the reference used by the SAR ADC, as shown in Figure 83. After a reset, the AD7606C-18 operates in the reference mode selected by the REF SELECT pin. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 µF must be applied to the REFGND pin to ensure that the reference buffer is in closed-loop operation. A 0.1 µF ceramic capacitor is required on the REFIN/REFOUT pin.

When the AD7606C-18 is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin.

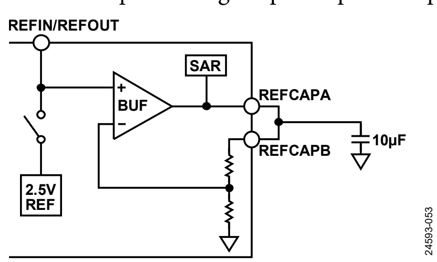


Figure 83. Reference Circuitry

Using Multiple AD7606C-18 Devices

For applications using multiple AD7606C-18 devices, the configurations in the External Reference Mode section and the Internal Reference Mode section are recommended, depending on the application requirements.

External Reference Mode

One external reference can drive the REFIN/REFOUT pins of all AD7606C-18 devices (see Figure 84). In this configuration, decouple each REFIN/REFOUT pin of the AD7606C-18 with at least a 100 nF decoupling capacitor.

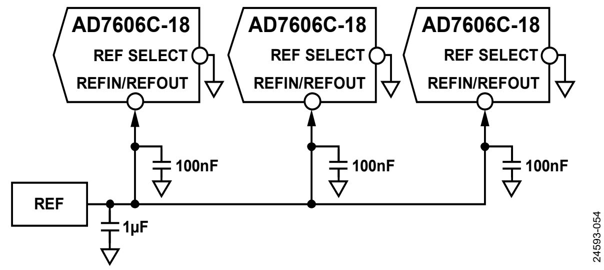


Figure 84. Single External Reference Driving Multiple AD7606C-18 REFIN/REFOUT Pins

Internal Reference Mode

One AD7606C-18 device, configured to operate in the internal reference mode, can drive the remaining AD7606C-18 devices, which are configured to operate in external reference mode (see Figure 85). Decouple the REFIN/REFOUT pin of the AD7606C-18, configured in internal reference mode, using a 10 µF ceramic decoupling capacitor. The other AD7606C-18 devices, configured in external reference mode, must use at least a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

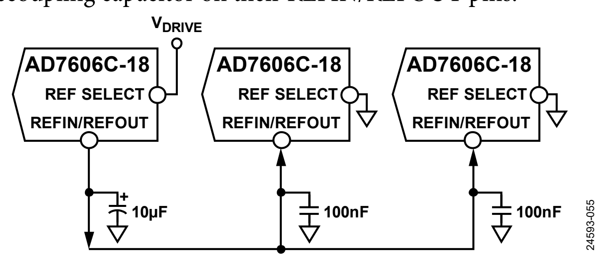


Figure 85. Internal Reference Driving Multiple AD7606C-18 REFIN/REFOUT Pins

OPERATION MODES

The AD7606C-18 can be operated in hardware or software mode by controlling the OSx pins, as described in Table 14.

In hardware mode, the AD7606C-18 is configured depending on the logic level on the RANGE, OSx, or $\overline{\text{STBY}}$ pins. The AD7606C-18 is backwards compatible to the AD7606, AD7606B, AD7608, and AD7609.

In software mode, when all three OSx pins are connected to logic high level, the AD7606C-18 is configured by the corresponding registers accessed via the serial or parallel interface. Additional features are available, as described in Table 15. The reference and the data interface is selected through the REFSELECT and $\overline{\text{PAR}}$/SER SEL pins in both hardware and software modes.

Table 14. Oversample Pin Decoding

OS2	OS1	OS0	AD7606C-18
0	0	0	No oversampling
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	Enters software mode

Table 15. Functionality Matrix

Parameter	Hardware Mode	Software Mode
Analog Input Range[1]	±10 V or ±5 V[2]	Single-ended, bipolar: ±12.5 V, ±10 V, ±6.25 V, ±5 V, and ±2.5 V[3] Single-ended, unipolar: 0 V to 12.5 V, 0 V to 10 V, 0 V to 5 V[3] Differential, bipolar: ±20 V, ±12.5 V, ±10 V, and ±5 V[3]
System Gain, Phase, and Offset Calibration	Not accessible	Available[3]
OSR	From no oversampling to OSR = 64	From no oversampling to OSR = 256
Analog Input Open Circuit Detection	Not accessible	Available[3]
Serial Data Output Lines	2	Selectable: 1, 2, 4, or 8
Diagnostics	Not accessible	Available
Power-Down Modes	Standby and shutdown	Standby, shutdown, and autostandby

[1] See Table 10 for the analog input range selection.
[2] Same input range configured in all input channels.
[3] On a per channel basis

Reset Functionality

The AD7606C-18 has two reset modes: full or partial. The reset mode selected is dependent on the length of the reset high pulse. A partial reset requires the RESET pin to be held high between 55 ns and 2 µs. After 50 ns from the release of the RESET pin (t_{DEVICE_SETUP}, partial reset), the device is fully functional and a conversion can be initiated. A full reset requires the RESET pin to be held high for a minimum of 3.2 µs. After 274 µs (t_{DEVICE_SETUP}, full reset) from the release of the RESET pin, the device is completely reconfigured and a conversion can be initiated.

A partial reset reinitializes the following modules:

- Digital filter
- SPI and parallel, resetting to ADC mode
- SAR ADCs
- CRC logic

After the partial reset, the RESET_DETECT bit on the status register asserts (Address 0x01, Bit 7). The current conversion result is discarded after the completion of a partial reset. The partial reset does not affect the register values programmed in software mode or the latches that store the user configuration in both hardware and software modes.

A full reset returns the device to its default power-on state, the RESET_DETECT bit on the status register asserts (Address 0x01, Bit 7), and the current conversion result is discarded. The following features, in addition to those listed above, are configured when the AD7606C-18 is released from full reset:

- Hardware mode or software mode
- Interface type, serial or parallel

Power-Down Modes

In hardware mode, two power-down modes are available on the AD7606C-18: standby mode and shutdown mode. The $\overline{\text{STBY}}$ pin controls whether the AD7606C-18 is in normal mode or in one of the two power-down modes, as shown in Table 16. If the $\overline{\text{STBY}}$ pin is low, the power-down mode is selected by the state of the RANGE pin.

Table 16. Power-Down Mode Selection, Hardware Mode

Power Mode	$\overline{\text{STBY}}$ Pin	RANGE Pin
Normal	1	X[1]
Standby	0	1
Shutdown	0	0

[1] X = don't care.

In software mode, the power-down mode is selected through the OPERATION_MODE bits on the CONFIG register (Address 0x02, Bits[1:0]), within the memory map. There is an extra power-down mode available in software mode called autostandby mode.

Table 17. Power-Down Mode Selection, Software Mode, Through CONFIG Register (Address 0x02)

Operation Mode	Address 0x02, Bit 1	Address 0x02, Bit 0
Normal	0	0
Standby	0	1
Autostandby	1	0
Shutdown	1	1

When the AD7606C-18 is placed in shutdown mode, all circuitry is powered down and the current consumption reduces to 4.5 µA maximum. The power-up time is approximately 10 ms. When the AD7606C-18 is powered up from shutdown mode, a full reset must be applied to the AD7606C-18 after the required power-up time elapses.

When the AD7606C-18 is placed in standby mode, all of the PGAs and all of the SAR ADCs enter a low power mode, such that the overall current consumption reduces to 6.5 mA maximum. No reset is required after exiting standby mode.

When the AD7606C-18 is placed in autostandby mode, which is available only in software mode, the device automatically enters standby mode on the BUSY signal falling edge. The AD7606C-18 exits standby mode automatically on the CONVST signal rising edge. Therefore, the CONVST signal low pulse time is longer than t_{WAKE_UP} (standby mode) = 1 µs (see Figure 86).

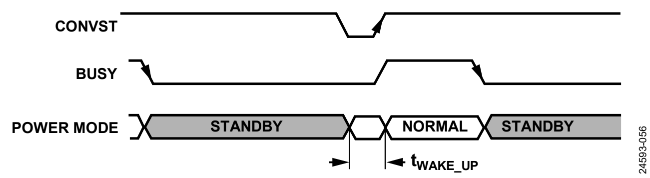


Figure 86. Autostandby Mode Operation

DIGITAL FILTER

The AD7606C-18 contains an optional digital averaging filter that can be enabled in slower throughput rate applications that require higher SNR or dynamic range.

In hardware mode, the oversampling ratio of the digital filter is controlled using the oversampling pins, OSx, as shown in Table 14. The OSx pins are latched on either the falling edge of the BUSY signal or upon a full reset.

In software mode, if all OSx pins are tied to logic high, the oversampling ratio is selected through the oversampling register (Address 0x08). Two additional oversampling ratios (oversampling by 128 and oversampling by 256) are available in software mode.

In oversampling mode, the ADC takes the first sample for each channel on the rising edge of the CONVST signal. After converting the first sample, the subsequent samples are taken by the internally generated sampling signal, as shown in Figure 87. Alternatively, this sampling signal can be applied externally as described in the External Oversampling Clock section.

For example, if oversampling by eight is configured, eight samples are taken, averaged, and the result is provided on the output. A CONVST signal rising edge triggers the first sample, and the remaining seven samples are taken with an internally generated sampling signal (OS_CLOCK). Consequently, turning on the averaging of multiple samples leads to an improvement in SNR performance at the expense of reducing the maximum throughput rate. When the oversampling function is turned on, the BUSY signal high time (t_{CONV}) extends, as shown in Table 3.

Table 18 and Table 19 show the trade off in SNR vs. bandwidth and throughput for the ±10 V single-ended range, ±20 V differential range, and 0 V to 10 V single-ended range.

Figure 87 shows that the conversion time (t_{CONV}) extends when oversampling is turned on. The throughput rate ($1/t_{CYCLE}$) must be reduced to accommodate the longer conversion time and to allow the read operation to occur. To achieve the fastest throughput rate possible when oversampling is turned on, the read can be performed during the BUSY signal high time, as explained in the Reading During Conversion section.

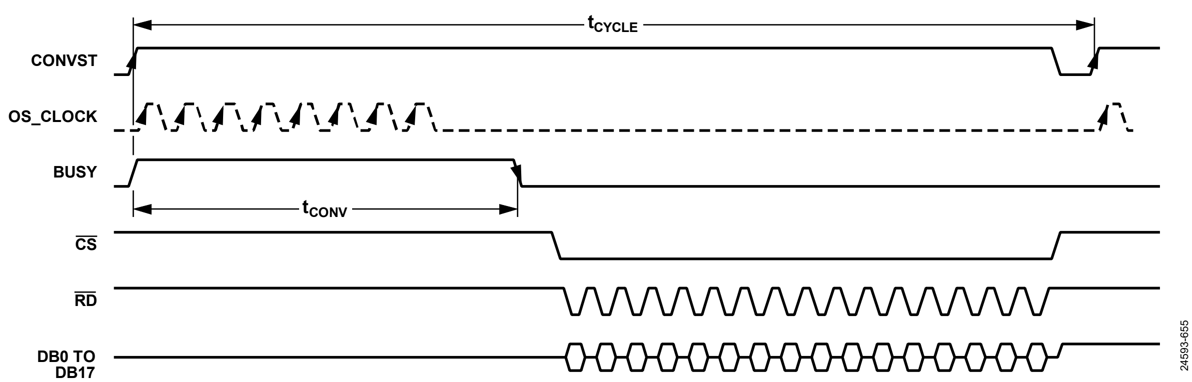


Figure 87. AD7606C-18 Oversampling by 8 Example, Read After Conversion, Parallel Interface, OS_CLOCK Is the Internally Generated Sampling Signal

Table 18. Oversampling Performance, Low Bandwidth Mode

		±10 V Single-Ended Range		±20 V Differential Range		0 V to 10 V Single-Ended Range		
Oversampling Ratio	Input Frequency (Hz)	SNR (dB)	−3 dB Bandwidth (kHz)	SNR (dB)	−3 dB Bandwidth (kHz)	SNR (dB)	−3 dB Bandwidth (kHz)	Maximum Throughput (kSPS)
No oversampling	1000	92.5	25	93	25	90	25	1000
2	1000	94.5	24.6	95	24.4	91.5	24.6	500
4	1000	96.5	24	97.5	23.7	92.3	24	250
8	1000	98	22.3	99.5	22.2	93.3	22.3	125
16	1000	100	17.8	101	17.6	94.3	17.8	62.5
32	160	101.5	11.6	103	11.5	96	11.6	31.25
64	160	103.3	6.5	104	6.4	97.5	6.4	15.6
128	50	104.5	3.3	104.4	3.4	99	3.3	7.8
256	50	105	1.7	105	1.7	100	1.7	3.9

Table 19. Oversampling Performance, High Bandwidth Mode

Oversampling Ratio	Input Frequency (Hz)	±10 V Single-Ended Range		±20 V Differential Range		0 V to 10 V Single-Ended Range		Maximum Throughput (kSPS)
		SNR (dB)	−3 dB Bandwidth (kHz)	SNR (dB)	−3 dB Bandwidth (kHz)	SNR (dB)	−3 dB Bandwidth (kHz)	
No oversampling	1000	87	220	89	220	82	220	1000
2	1000	89	154	91.5	154	84.5	155	500
4	1000	92	97.5	94.5	97.5	87	97.5	250
8	1000	95	53	97	53	89.5	53.5	125
16	1000	97.5	27.5	99.5	27.5	91.5	27.5	62.5
32	160	99.8	13.8	101.5	13.7	94	13.8	31.25
64	160	102	7	103	7	95.5	7	15.6
128	50	104	3.5	104.5	3.5	97	3.5	7.8
256	50	104.5	1.7	105.2	1.7	97.7	1.7	3.9

PADDING OVERSAMPLING

As shown in Figure 87, an internally generated clock triggers the samples to be averaged, and then the ADC remains idle until the following CONVST signal rising edge. In software mode, through the oversampling register (Address 0x08), the internal clock (OS_CLOCK) frequency can be changed such that idle time is minimized and sampling instants are equally spaced, as shown in Figure 88. As a result, the actual oversampling clock frequency depends on the OS_PAD bits configuration, as per the following equation:

$$OS\_CLOCK(kHz) = \frac{1}{1000 \times (1 + \frac{OS\_PAD}{16})}$$

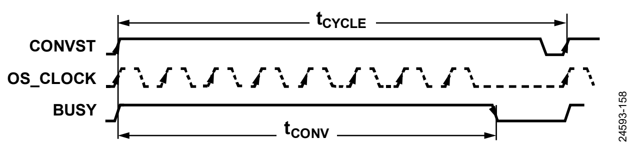


Figure 88. Oversampling by 8 Example, Oversampling Padding Enabled

EXTERNAL OVERSAMPLING CLOCK

In software mode, there is an option to apply an external clock through the CONVST pin when oversampling mode is enabled. Providing a low jitter external clock helps improve SNR performance for large oversampling ratios. By applying an external clock, the input is sampled at regular time intervals, which is optimum for antialiasing performance.

To enable the external oversampling clock, Bit 5 in the CONFIG register (Address 0x02, Bit 5) must be set. Then, the throughput rate is

$$Throughput = \frac{1}{t_{CYCLE} \times OSR}$$

That is, the sampling signal is provided externally through the CONVST pin, and after every OSR number of clocks, an output is averaged and provided, as shown in Figure 90. This feature is available using either the parallel interface or serial interface.

Simultaneous Sampling of Several AD7606C-18 Devices

In general, synchronizing several SAR ADCs is achieved by using a common CONVST signal. However, when oversampling is enabled, an internal clock is used to trigger the subsequent samples by default. Any deviation between these internal clocks may impede device to device synchronization. This deviation can be minimized by using external oversampling, as the CONVST signal of all the samples is managed externally.

A partial reset (t_{RESET} < 2 μs) interrupts the oversampling process and empties the data register. Therefore, if by any reason the different AD7606C-18 devices are not synchronized, issuing a partial reset resynchronizes the devices, as shown in Figure 89.

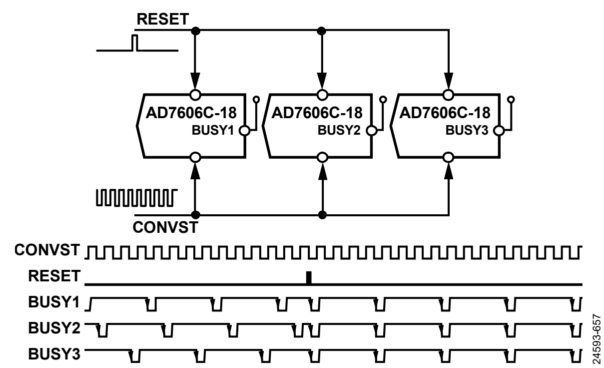


Figure 89. Synchronizing Several AD7606C-18 Devices When External Oversampling Clock Is Enabled

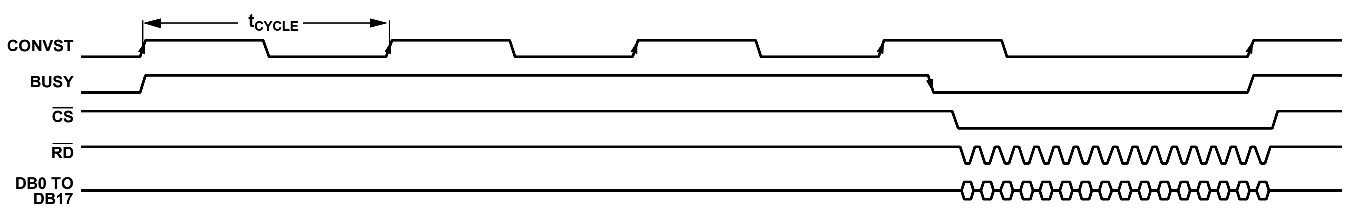


Figure 90. External Oversampling Clock Applied on the CONVST Pin (OSR = 4), Parallel Interface

SYSTEM CALIBRATION FEATURES

The following system calibration features are available in software mode by writing to corresponding registers in the memory map:

- Phase calibration
- Gain calibration
- Offset calibration
- Analog input open circuit detection

SYSTEM PHASE CALIBRATION

When using an external filter, as shown in Figure 92, any mismatch on the discrete components or in the sensor used can cause phase mismatch between channels. This phase mismatch can be compensated for in software mode, on a per channel basis, by delaying the sampling instant on individual channels.

The sampling instant on any particular channel can be delayed with regards to the CONVST signal rising edge, with a resolution of 1 µs, and up to 255 µs, by writing to the corresponding CHx_PHASE register (Address 0x19 through Address 0x20).

For example, if the CH4_PHASE register (Address 0x1C) is written with 10 decimal, Channel 4 is effectively sampled 10 µs after the CONVST signal rising edge, as shown in Figure 91.

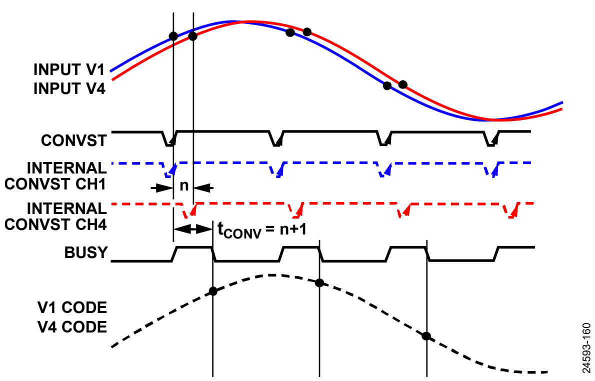


Figure 91. System Phase Calibration Functionality

Note that delaying any channel extends the BUSY signal high time, and t_{CONV} extends until $t_{CONV} = n + 1$ µs, with n as the CHx_PHASE register content of the most delayed channel. In the previously explained example, if only the CH4_PHASE register is programmed, t_{CONV} is 11 µs. Therefore, this scenario must be considered when running at higher throughput rates.

SYSTEM GAIN CALIBRATION

Using an external R_{FILTER}, which is a resistor placed in a series to the analog input front-end, see Figure 92, generates a system gain error. This gain error can be compensated for in software mode, on a per channel basis, by writing the series resistor value used on the corresponding register, Address 0x09 through Address 0x10. These registers can compensate up to 65 kΩ series resistors with a resolution of 1024 Ω.

Note that system gain calibration is only available on bipolar analog input ranges, both single-ended and differential. System gain calibration is not available in unipolar single-ended ranges.

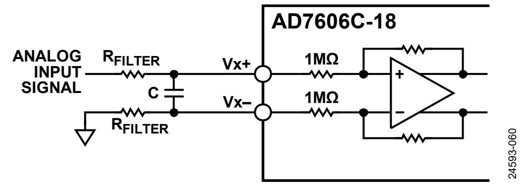


Figure 92. System Gain Error

For example, if a 27 kΩ resistor is placed in series to the analog input of Channel 5, the resistor generates about −2% positive full-scale error on the system (at ±10 V range), as seen in Figure 93. In software mode, this error is eliminated by writing 27 decimal to the CH5_GAIN register (Address 0x0D), which keeps the error within 0.05% of FSR, no matter the R_{FILTER} value of the series resistor, as shown in Figure 94

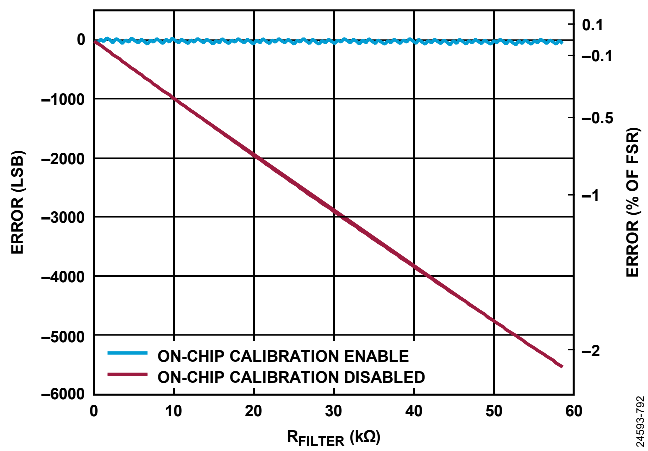


Figure 93. System Gain Calibration, with and Without Calibration, ±10 V Single-Ended Range

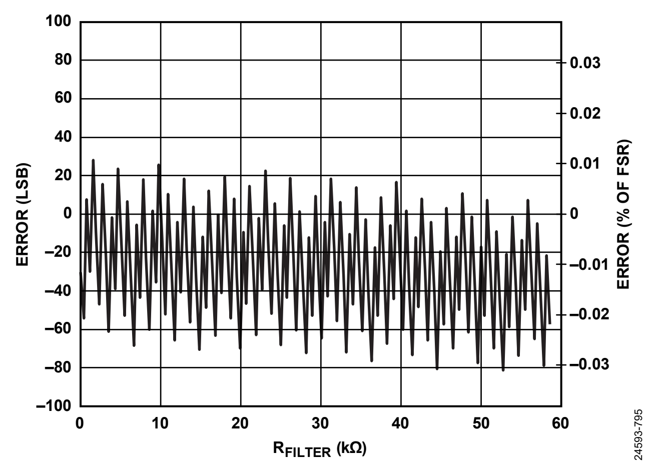


Figure 94. System Error with Gain Calibration Enabled

SYSTEM OFFSET CALIBRATION

A potential offset on the sensor, or any offset caused by a mismatch between the R_{FILTER} pair placed on a particular channel (as described in the Analog Front-End section), can be compensated in software mode on a per channel basis. The CHx_OFFSET registers (Address 0x11 through Address 0x18) allow the ability to add or subtract up to 512 LSBs to the ADC code automatically with a resolution of 4 LSB, as shown in Table 20.

For example, if the signal connected to Channel 3 has a 9 mV offset, and the analog input range is set to ±10 V range (where LSB size = 76.3 μV) to compensate for this offset, program −30 LSB to the corresponding register (that is, 9 mV/76.3 μV/4). Writing 128 decimal – 30 decimal = 0x80 − 0x1E = 0x62 into the CH3_OFFSET register (Address 0x13) removes such offset.

Table 20. CHx_OFFSET Register Bit Decoding

CHx_OFFSET Register Code	Offset Calibration (LSB)
0x00	−512
0x45	−236
0x80 (Default)	0
0x83	+12
0xFF	+508

ANALOG INPUT OPEN CIRCUIT DETECTION

The AD7606C-18 has an analog input open circuit detection feature available in software mode. To use this feature, an R_{PD} must be placed as shown in Figure 95. If the analog input is disconnected, for example, if a switch opens in Figure 95, the source impedance changes from the burden resistor (R_S) to R_{PD}, as long as $R_S < R_{PD}$. It is recommended to use R_{PD} = 20 kΩ so that the AD7606C-18 can detect changes in the source impedance by internally switching the PGA common-mode voltage. Analog input open circuit detection operates in manual mode or in automatic mode.

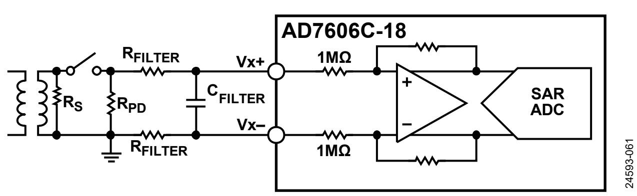


Figure 95. Analog Front End with R_{PD}

Note that analog input open circuit detection is only available on bipolar analog input ranges, both single-ended and differential. Analog input open circuit detection is not available in unipolar single-ended ranges.

Manual Mode

Manual mode is enabled by writing 0x01 to the OPEN_DETECT_QUEUE register (Address 0x2C). In manual mode, each PGA common-mode voltage is controlled by the corresponding CHx_OPEN_DETECT_EN bit on the OPEN_DETECT_ENABLE register (Address 0x23). Setting this bit high shifts up the PGA common-mode voltage. If there is an open circuit on the analog input, the ADC output changes proportionally to the R_{PD}, as shown in Figure 96. If there is not an open circuit, any change on the PGA common-mode voltage has no effect on the ADC output.

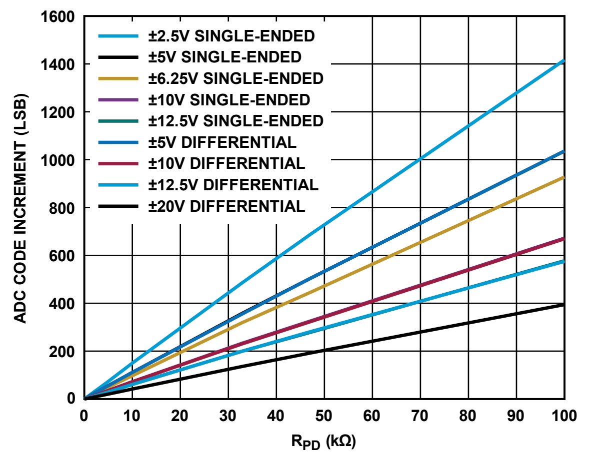


Figure 96. Open Circuit Code Error increment, Dependent of R_{PD}

Automatic Mode

Automatic mode is enabled by writing any value greater than 0x01 to the OPEN_DETECT_QUEUE register (Address 0x2C), as shown in Table 21. If the AD7606C-18 detects that the ADC reported a number (specified in the OPEN_DETECT_QUEUE register) of consecutive unchanged conversions, the analog input open circuit detection algorithm is performed internally and automatically. The analog input open circuit detection algorithm automatically changes the PGA common-mode voltage, checks the ADC output, and returns to the initial common-mode voltage, as shown in Figure 97. If the ADC code changes in any channel with the PGA common-mode change, this implies there is no input signal connected to that analog input, and the corresponding flag asserts within the OPEN_DETECTED register (Address 0x24). Each channel can be individually enabled or disabled through the OPEN_DETECT_ENABLE register (Address 0x23).

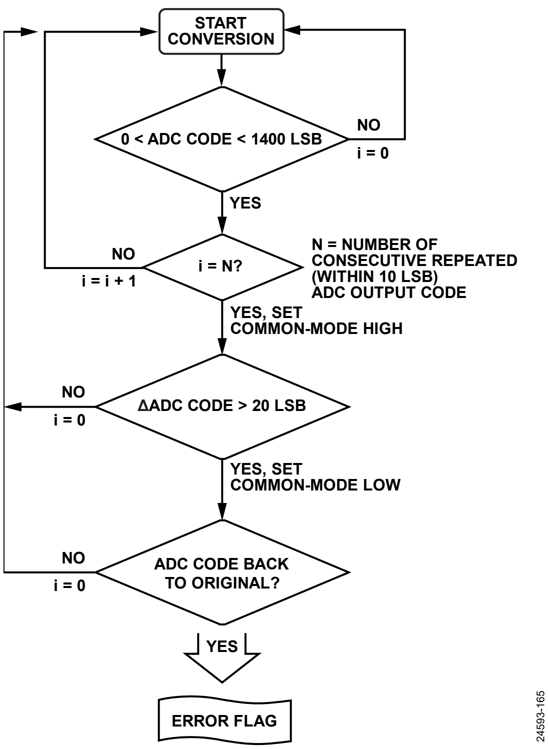


Figure 97. Automatic Analog Input Open Circuit Detect Flowchart

If no oversampling is used, the recommended minimum number of conversions to be programmed for the AD7606C-18 to automatically detect an open circuit on the analog input is

$$OPEN\_DETECT\_QUEUE =$$
$$10 \times f_{SAMPLE} \left(R_{PD} + 2 \times R_{FILTER}\right) \times (C_{FILTER} + 10\ pF)$$

However, when oversampling mode is enabled, the recommended minimum number of conversions to use is

$$OPEN\_DETECT\_QUEUE =$$
$$1 + \left(f_{SAMPLE} \times 2 \left(R_{PD} + 2 \times R_{FILTER}\right) \times (C_{FILTER} + 10\ pF) \times OSR\right)$$

Table 21. Analog Input Open-Circuit Detect Mode Selection and Register Functionality

OPEN_DETECT_QUEUE (Address 0x2C)	Open Detect Mode	OPEN_DETECT_ENABLE (Address 0x23)
0x00 (Default)	Disabled.	Not applicable.
0x01	Manual.	Sets common-mode voltage high or low on a per channel basis.
0x02[1] to 0xFF	Automatic. OPEN_DETECT_QUEUE is the number of consecutive conversions before asserting any CHx_OPENED flag.	Enables or disables automatic analog input open circuit detection on a per channel basis.

[1] It is recommended to write to OPEN_DETECT_QUEUE a value greater than 5.

DIGITAL INTERFACE

The AD7606C-18 provides two interface options: a parallel interface and a high speed serial interface. The required interface mode is selected via the $\overline{\text{PAR}}$/SER SEL pin.

Table 22. Interface Mode Selection

$\overline{\text{PAR}}$/SER SEL Setting	Interface Mode
0	Parallel interface
1	Serial interface

Operation of the interface modes is discussed in the Hardware Mode section and the Software Mode section.

Hardware Mode

In hardware mode, only ADC mode is available. ADC data can be read from the AD7606C-18 via the parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals or via the serial interface with standard $\overline{\text{CS}}$, SCLK, and two $D_{OUT}x$ signals.

See the Reading Conversion Results (Parallel ADC Mode) section and the Reading Conversion Results (Serial ADC Mode) section for more details on how the ADC mode operates.

Software Mode

In software mode, which is active only when all three OSx pins are tied high, both ADC mode and register mode are available. ADC data can be read from the AD7606C-18, and registers can also be read from and written to the AD7606C-18 via the parallel data bus with standard $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ signals or via the serial interface with standard $\overline{\text{CS}}$, SCLK, SDI, and $D_{OUT}A$ lines.

See the Parallel Register Mode (Writing Register Data) section and the Parallel Register Mode (Reading Register Data) section for more details on how register mode operates.

Pin functions differ depending on the interface selected (parallel or serial) and the operation mode (hardware or software), as shown in Table 23.

Table 23. Data Interface Pin Function per Mode of Operation

		Parallel Interface			Serial Interface		
			Software Mode			Software Mode	
Pin Mnemonic	Pin No.	Hardware Mode	ADC Mode	Register Mode	Hardware Mode	ADC Mode	Register Mode
DB2 to DB4	16 to 18	DB2 to DB4		Register data	N/A[1]	N/A	
DB5/$D_{OUT}E$	19	DB5		Register data	N/A	$D_{OUT}E$[2]	Unused
DB6/$D_{OUT}F$	20	DB6		Register data	N/A	$D_{OUT}F$[2]	Unused
DB7/$D_{OUT}G$	21	DB7		Register data	N/A	$D_{OUT}G$[2]	Unused
DB8/$D_{OUT}H$	22	DB8		Register data	N/A	$D_{OUT}H$[2]	Unused
DB9/$D_{OUT}A$	24	DB9		Register data (MSB)	$D_{OUT}A$	$D_{OUT}A$	$D_{OUT}A$
DB10/$D_{OUT}B$	25	DB10		ADD0	$D_{OUT}B$	$D_{OUT}B$[3]	Unused
DB11/$D_{OUT}C$	27	DB11		ADD1	N/A	$D_{OUT}C$[4]	Unused
DB12/$D_{OUT}D$	28	DB12		ADD2	N/A	$D_{OUT}D$[4]	Unused
DB13/SDI	29	DB13		ADD3	N/A	Unused	SDI
DB14	30	DB14		ADD4	N/A	N/A	
DB15	31	DB15		ADD5	N/A	N/A	
DB16/DB0	32	DB16/DB0[5]		ADD6	N/A	N/A	
DB17/DB1	33	DB17/DB1[5]		R/$\overline{\text{W}}$	N/A	N/A	

[1] N/A means not applicable. Tie all N/A pins to AGND.
[2] Only used if 8 $D_{OUT}x$ mode is selected on the CONFIG register, otherwise leave unconnected.
[3] Only used if 2 $D_{OUT}x$, 4 $D_{OUT}x$, or 8 $D_{OUT}x$ mode is selected on the CONFIG register, otherwise leave unconnected.
[4] Only used if 4 $D_{OUT}x$ or 8 $D_{OUT}x$ mode is selected on the CONFIG register, otherwise leave unconnected.
[5] Pin functionality depends on whether it is the first or second read frame during an ADC read operation, see Figure 100.

PARALLEL INTERFACE

To read ADC data, or to read and write the register content over the parallel interface, tie the $\overline{PAR}$/SER SEL pin low.

The rising edge of the $\overline{CS}$ input signal three-states the bus, and the falling edge of the $\overline{CS}$ input signal takes the bus out of the high impedance state. $\overline{CS}$ is the control signal that enables the data lines and it is the function that allows multiple AD7606C-18 devices to share the same parallel data bus.

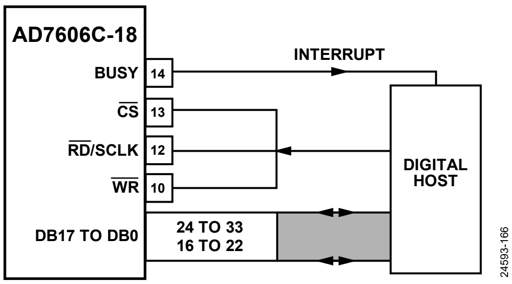


Figure 98. AD7606C-18 Interface Diagram—One AD7606C-18 Using the Parallel Bus with $\overline{CS}$ and $\overline{RD}$ Shorted Together

Reading Conversion Results (Parallel ADC Mode)

The falling edge of the $\overline{RD}$ pin reads data from the output conversion results register. Applying a sequence of $\overline{RD}$ pulses to the $\overline{RD}$ pin clocks the conversion results out from each channel onto the parallel bus, DB17 to DB0, in ascending order, from V1 to V8, as shown in Figure 99.

The parallel interface consists of 16 parallel lines on Pin 16 to Pin 22 and Pin 24 to Pin 33. Because the ADC data is 18 bit, two parallel frames are required as follows:

- 1st frame clocks out ADC data from Bit 2 to Bit 17 (MSB)
- 2nd frame clocks out ADC data from Bit 1 and Bit 0 (LSB)

The $\overline{CS}$ signal can be permanently tied low, and the $\overline{RD}$ signal can access the conversion results, as shown in Figure 3. A read operation of new data can take place after the BUSY signal goes low (see Figure 2). Alternatively, a read operation of data from the previous conversion process can take place while the BUSY pin is high.

When there is only one AD7606C-18 in a system and it does not share the parallel bus, data can be read using one control signal from the digital host. The $\overline{CS}$ and $\overline{RD}$ signals can be tied together, as shown in Figure 4. In this case, the falling edge of the $\overline{CS}$ and $\overline{RD}$ signals brings the data bus out of three-state and clocks out the data.

The FRSTDATA output signal indicates when the first channel, V1, is being read back, as shown in Figure 4. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes the FRSTDATA pin out of three-state. The falling edge of the $\overline{RD}$ signal corresponding to the result of V1 sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA pin returns to a logic low following the next falling edge of $\overline{RD}$.

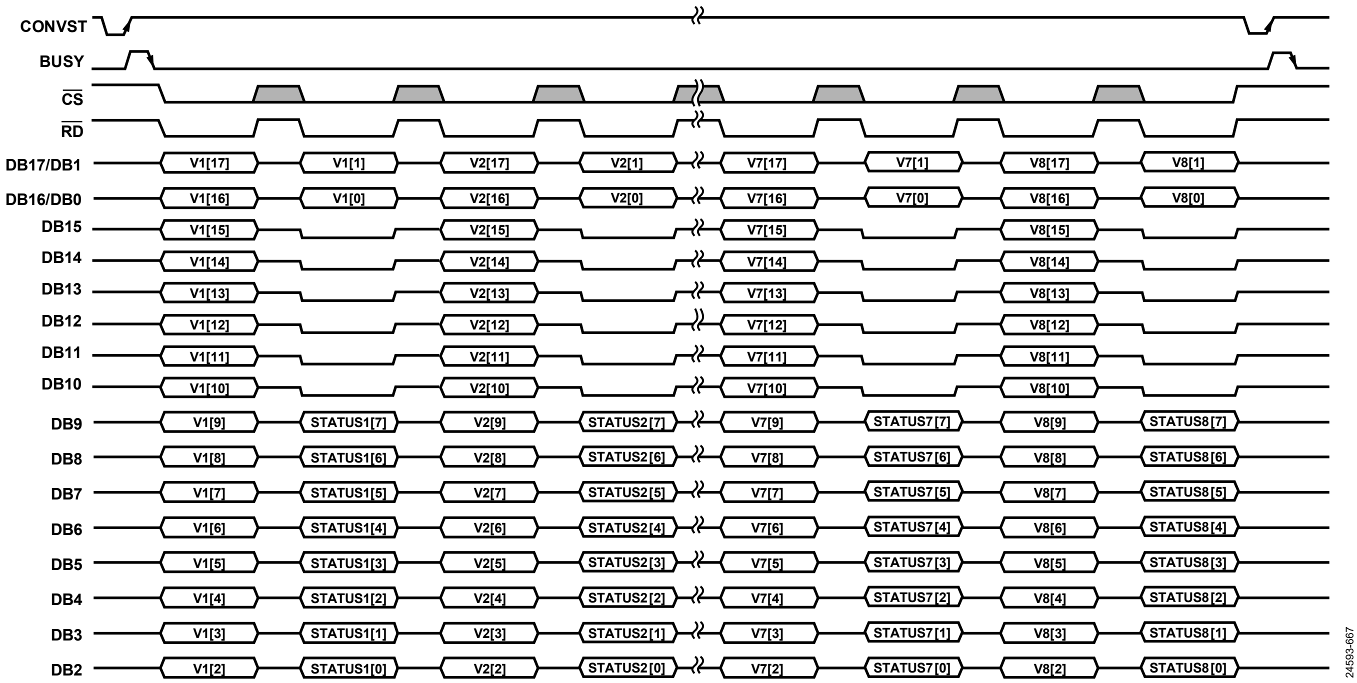


Figure 99. Parallel Interface, ADC Mode with Status Header Enabled

Reading During Conversion

Data read operations from the AD7606C-18, as shown in Figure 100, can occur in the following three scenarios:

- After a conversion while the BUSY line is low
- During a conversion while the BUSY line is high
- Starting while the BUSY line is low and ending while the following conversion is in progress, see Figure 2

Reading during conversions has little effect on the performance of the converter, and it allows a faster throughput rate to be achieved. Data can be read from the AD7606C-18 at any time other than on the falling edge of the BUSY signal because this is when the output data registers are updated with the new conversion data. Any data read while the BUSY signal is high must be completed before the falling edge of the BUSY signal.

Parallel ADC Mode with CRC Enabled

In software mode, the parallel interface supports reading the ADC data with the CRC appended, when enabled through the INT_CRC_ERR_EN bit (Address 0x21, Bit 2). The CRC is 16 bits, and it is clocked out after reading all eight channel conversions, as shown in Figure 101. The CRC calculation includes all data on the DBx pins: data, status (when appended), and zeros. See the Diagnostics section for more details on CRC.

Parallel ADC Mode with Status Enabled

In software mode, the 8-bit status header is enabled (see Table 25) by setting Bit 6 in the CONFIG register (Address 0x02, Bit 6), and each channel then takes the following two frames of data:

- The first frame clocks the ADC data out normally through DB17 to DB2 from the MSB to Bit 2.
- The second frame clocks out the status header of the channel on DB9 to DB2, DB9 being the MSB and DB2 being the LSB of the status header, while DB1 to DB0 clock out the two LSBs of the conversion result and the DB15 to DB10 pins clock out zeros.

This sequence is shown in Figure 99. Table 25 explains the status header content and describes each bit.

Table 24. CH.ID Bits Decoding in Status Header

CH.ID2	CH.ID1	CH.ID0	Channel Number
0	0	0	Channel 1 (V1)
0	0	1	Channel 2 (V2)
0	1	0	Channel 3 (V3)
0	1	1	Channel 4 (V4)
1	0	0	Channel 5 (V5)
1	0	1	Channel 6 (V6)
1	1	0	Channel 7 (V7)
1	1	1	Channel 8 (V8)

Table 25. Status Header, Parallel Interface

	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Content	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	RESERVED		CH. ID 2	CH. ID 1	CH. ID 0
Meaning[1]	Reset detected	Error flag on Address 0x22	The analog input of this channel is open			Channel ID (see Table 24)		

[1] See the Diagnostics section for more information.

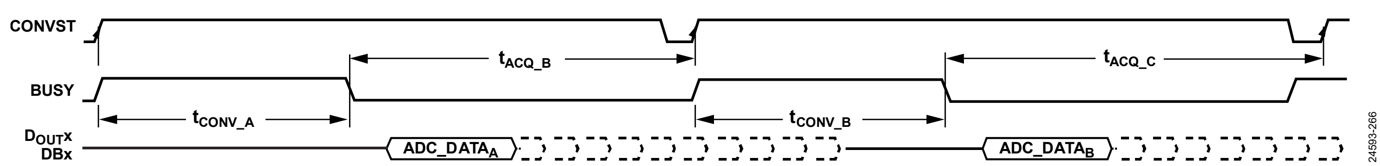


Figure 100. ADC Data Read Can Happen After Conversion and/or During the Following Conversion

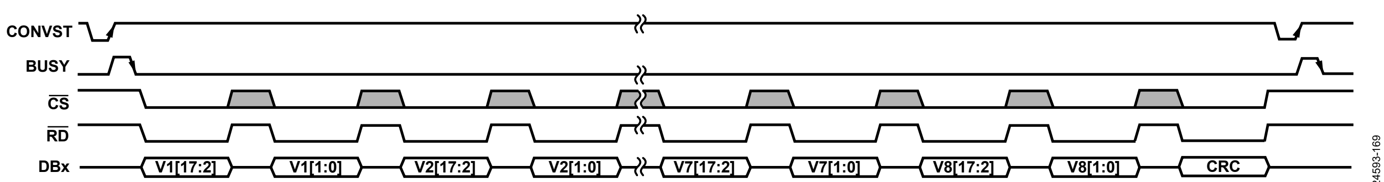


Figure 101. Parallel Interface, ADC Mode with CRC Enabled

Parallel Register Mode (Reading Register Data)

In software mode, all of the registers in Table 31 can be read over the parallel interface. Bits[DB17:DB2] leave a high impedance state when both the CS signal and RD signal are logic low for reading register content, or when both the CS signal and WR signal are logic low for writing register address and/or register content.

A register read is performed through two frames: first, a read command is sent to the AD7606C-18 and second, the AD7606C-18 clocks out the register content. The format for a register read command is shown in Figure 102. On the first frame, perform the following:

- Bit DB17 must be set to 1 to select a read command. The read command puts the AD7606C-18 into register mode.
- Bits[DB16:DB10] must contain the register address.
- The subsequent eight bits, Bits[DB9:DB2], are ignored.

The register address is latched on the AD7606C-18 on the rising edge of the WR signal. The register content can then be read from the latched register by bringing the RD line low on the following frame, as follows:

- Bit DB17 is pulled to 0 by the AD7606C-18.
- Bits[DB16: DB10] provide the register address being read.
- The subsequent eight bits, Bits[DB9: DB2], provide the register content.

To revert to ADC mode, keep all DBx pins low during one WR cycle, as shown in the Parallel Register Mode (Writing Register Data) section. No ADC data can be read while the device is in register mode.

Parallel Register Mode (Writing Register Data)

In software mode, all of the R/W registers in Table 31 can be written to over the parallel interface. To write a sequence of registers, exit ADC mode (default mode) by reading any register on the memory map. A register write command is performed by a single frame, via the parallel bus (Bits[DB17:DB2]), CS signal, and WR signal. The format for a write command, as shown in Figure 102, is structured as follows:

- Bit DB17 must be set to 0 to select a write command.
- Bits[DB16:DB10] contain the register address.
- The subsequent eight bits, Bits[DB9:DB2], contain the data to be written to the selected register.

Data is latched onto the device on the rising edge of the WR pin. To revert back to ADC mode, keep all DBx pins low during one WR cycle. No ADC data can be read while the device is in register mode.

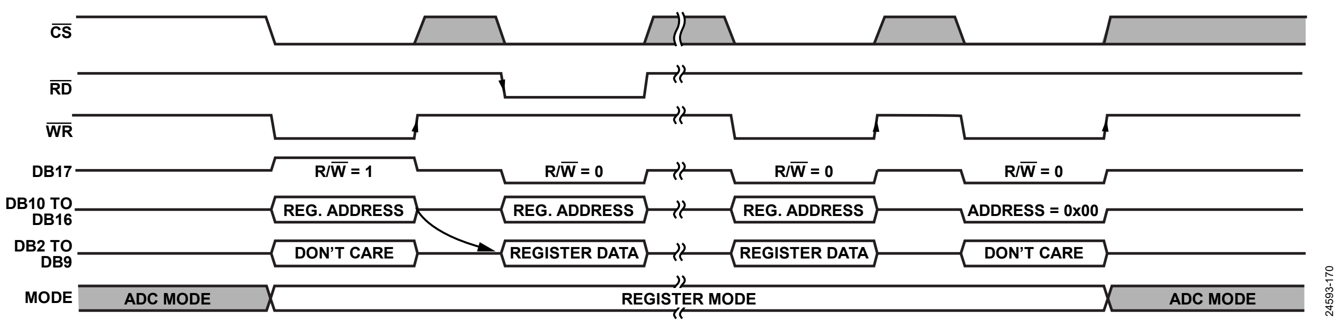


Figure 102. Parallel Interface Register Read Operation Followed by a Write Operation

SERIAL INTERFACE

To read ADC data or to read and write the register content over the serial interface, tie the $\overline{PAR}$/SER SEL pin high.

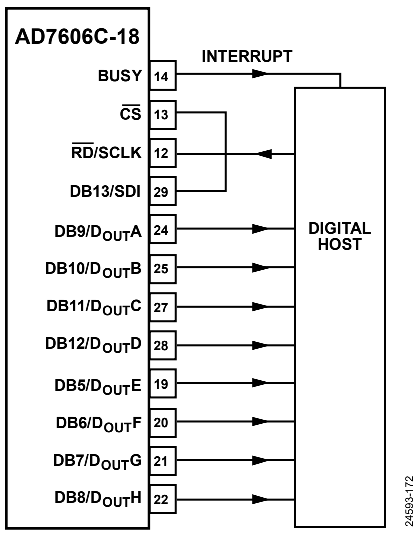


Figure 103. AD7606C-18 Interface Diagram—One AD7606C-18 Using the Serial Interface with Eight D_{OUT}x Lines

Reading Conversion Results (Serial ADC Mode)

The AD7606C-18 has eight serial data output pins, D_{OUT}A to D_{OUT}H. In software mode, data can be read back from the AD7606C-18 using either one (see Figure 107), two (see Figure 104), four (see Figure 105), or eight (see Figure 106) D_{OUT}x lines depending on the configuration set through the CONFIG register.

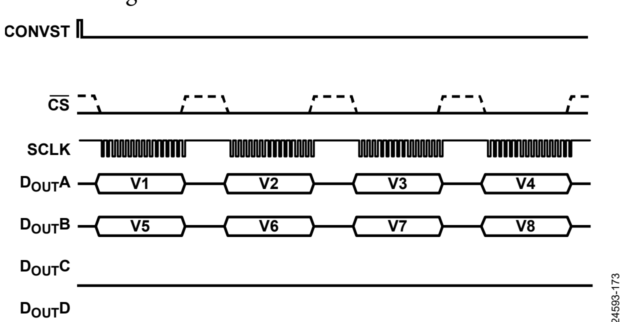


Figure 104. Serial Interface ADC Reading, Two D_{OUT}x Lines

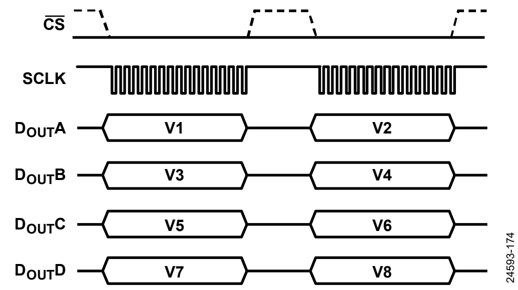


Figure 105. Serial Interface ADC Reading, Four D_{OUT}x Lines

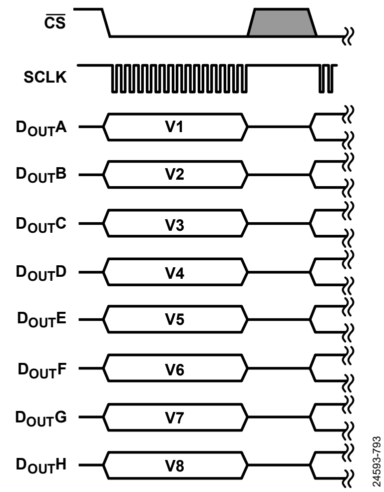


Figure 106. Serial Interface ADC Reading, Eight D_{OUT}x Lines

Table 26. D_{OUT}x Format Selection Using the CONFIG Register (Address 0x02)

D_{OUT}x Format	Address 0x02, Bit 4	Address 0x02, Bit 3
1 D_{OUT}x	0	0
2 D_{OUT}x	0	1
4 D_{OUT}x	1	0
8 D_{OUT}x	1	1

In hardware mode, only the 2 D_{OUT}x lines option is available. However, all channels can be read from D_{OUT}A by providing eight 18-bit SPI frames between two CONVST pulses.

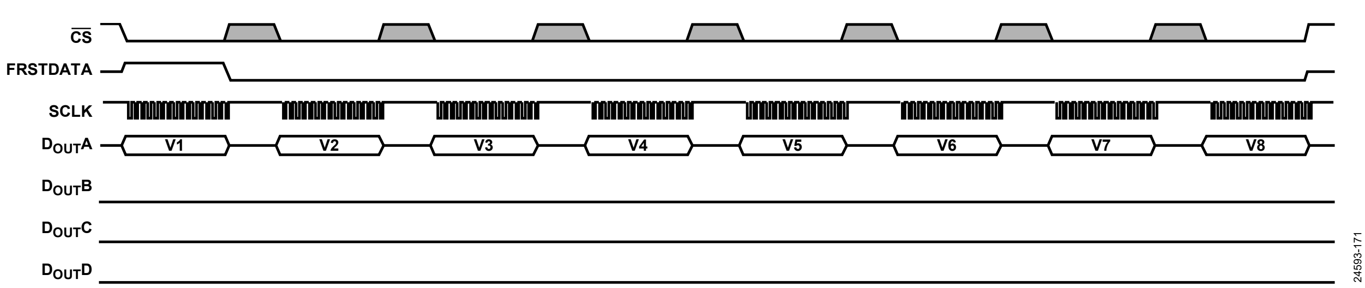


Figure 107. Serial Interface ADC Reading, One D_{OUT}x Line

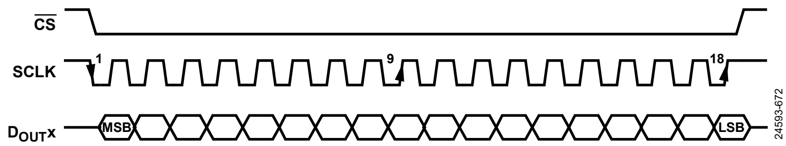


Figure 108. Serial Interface Data Read Back (One Channel)

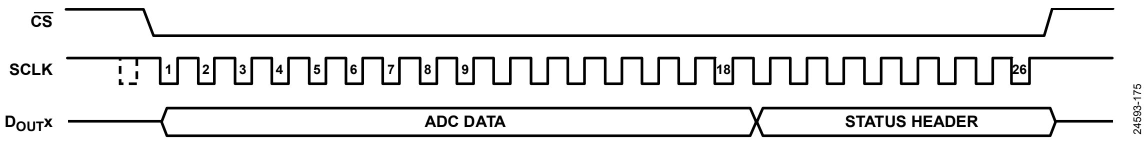


Figure 109. Serial Interface, ADC Mode, Status On

The $\overline{CS}$ falling edge takes the data output lines, $D_{OUT}x$, out of three-state and clocks out the MSB of the conversion result, as shown in Figure 108.

In 3-wire mode ($\overline{CS}$ tied low), instead of $\overline{CS}$ clocking out the MSB, the falling edge of the BUSY signal clocks out the MSB. The rising edge of the SCLK signal clocks all the subsequent data bits on the serial data outputs, $D_{OUT}x$, as shown in Figure 6. The $\overline{CS}$ input can be held low for the entire serial read operation, or it can be pulsed to frame each channel read of 24 SCLK cycles (see Figure 104). However, if $\overline{CS}$ is pulsed during a channel conversion result transmission, the channel that was interrupted retransmits on the next frame, completely starting from the MSB.

Data can also be clocked out using only the $D_{OUT}A$ pin, as shown in Figure 107. For the AD7606C-18 to access all eight conversion results on one $D_{OUT}x$ line, a total of 144 SCLK cycles is required. In hardware mode, these 144 SCLK cycles must be framed on groups of 18 SCLK cycles by the $\overline{CS}$ signal. The disadvantage of using just one $D_{OUT}x$ line is that the throughput rate is reduced if reading occurs after conversion. Leave the unused $D_{OUT}x$ lines disconnected in serial mode.

Figure 105 shows a read of eight simultaneous conversion results using four $D_{OUT}x$ lines on the AD7606C-18, available in software mode. In this case, a 36 SCLK transfer accesses data from the AD7606C-18, and $\overline{CS}$ is either held low to frame the entire 36 SCLK cycles or is pulsed between two 18-bit frames. This mode is only available in software mode, and it is configured through the CONFIG register (Address 0x02).

Figure 6 shows the timing diagram for reading one channel of data, framed by the $\overline{CS}$ signal, from the AD7606C-18 in serial mode. The SCLK input signal provides the clock source for the serial read operation. The $\overline{CS}$ signal goes low to access the data from the AD7606C-18.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. In serial mode, the falling edge of the $\overline{CS}$ signal takes the FRSTDATA pin out of three-state and sets the FRSTDATA pin high if the BUSY line is already deasserted, indicating that the result from V1 is available on the $D_{OUT}A$ output data line. The FRSTDATA output returns to a logic low following the 18^{th} SCLK falling edge. If the $\overline{CS}$ pin is tied permanently low (3-wire mode), the falling edge of the BUSY line sets the FRSTDATA pin high when the result from V1 is available on $D_{OUT}A$.

If the SDI is tied low or high, nothing is clocked to the AD7606C-18. Therefore, the device remains reading conversion results. When using the AD7606C-18 in 3-wire mode, keep the SDI at high level. While in ADC mode, single write operations can be performed, as shown in Figure 109. For writing a sequence of registers, switch to register mode, as described in the Serial Register Mode (Writing Register Data) section.

Reading During Conversion

Data read operations from the AD7606C-18, as shown in Figure 100, can occur in the following three scenarios:

- After a conversion while the BUSY line is low
- During a conversion while the BUSY line is high
- Starting while the BUSY line is low and ending while the following conversion is in progress, see Figure 2

Reading during conversions has little effect on the performance of the converter, and it allows a faster throughput rate to be achieved. Data can be read from the AD7606C-18 at any time other than on the falling edge of the BUSY signal because this is when the output data registers are updated with the new conversion data. Any data read while the BUSY signal is high must be completed before the falling edge of the BUSY signal.

Serial ADC Mode with CRC Enabled

In software mode, the CRC can be enabled by writing to the register map. In this case, the CRC is appended on each $D_{OUT}x$ line after the last channel is clocked out, as shown in Figure 115. See the Interface CRC section for more information on how the CRC is calculated.

Serial ADC Mode with Status Enabled

In software mode, the 8-bit status header (see Table 27) can be turned on when using the serial interface so that it is appended after each 18-bit data conversion, extending the frame size to 26 bits per channel, as shown in Figure 109.

Serial Register Mode (Reading Register Data)

All the registers in Table 31 can be read over the serial interface. The format for a read command is shown in Figure 110. It consists of two 16-bit frames. On the first frame, perform the following:

- The first bit clocked in SDI must be set to 0 to enable writing the address.
- The second bit clocked in SDI must be set to 1 to select a read command.
- Bits[3:8] clocked in SDI contain the register address to be clocked out on $D_{OUT}A$ on the following frame.
- The subsequent eight bits, Bits[9:16], clocked in SDI are ignored.

If the AD7606C-18 is in ADC mode, the $D_{OUT}x$ lines keep clocking ADC data on Bits[9:16], and then the AD7606C-18 switches to register mode.

If the AD7606C-18 is in register mode, the $D_{OUT}x$ lines read back the content from the previous addressed register, no matter if the previous frame was a read or a write command. To exit register mode, keep the SDI line low for 16 SCLK cycles, as shown in Figure 111.

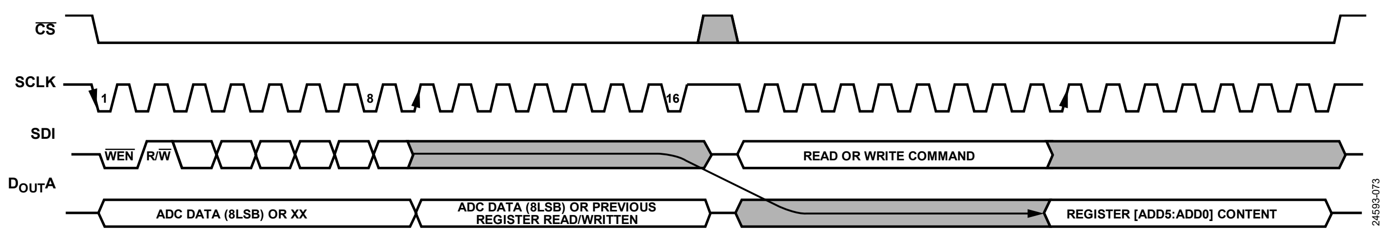


Figure 110. Serial Interface Read Command, First Frame Provides the Address, Second Frame Provides the Register Content

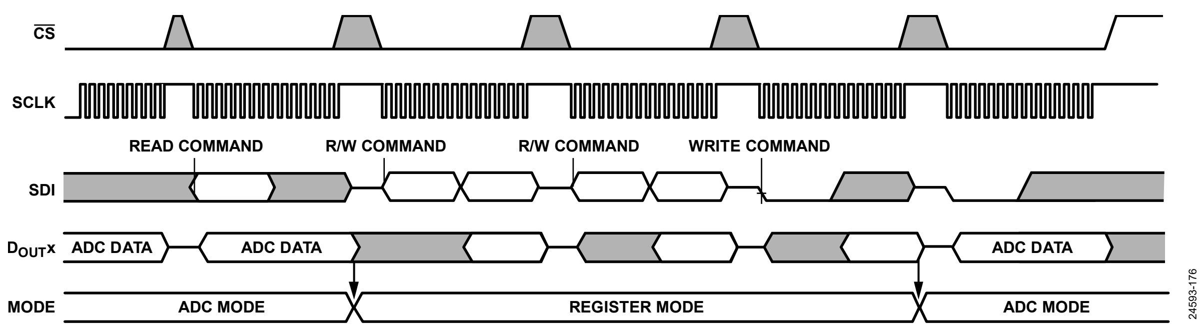


Figure 111. AD7606C-18 Register Mode

Table 27. Status Header, Serial Interface

	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Content	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	RESERVED		CH.ID 2	CH.ID 1	CH. ID 0
Meaning[1]	Reset detected	Error flag on Address 0x22	The analog input of this channel is open			Channel ID (see Table 24)		

[1] See the Diagnostics section for more information.

Serial Register Mode (Writing Register Data)

In software mode, all the read and write registers in Table 31 can be written to over the serial interface. To write a sequence of registers, exit ADC mode (default mode) by reading any register on the memory map. A register write command is performed by a single 16-bit SPI access. The format for a write command, as shown in Figure 112, is structured as follows:

- The first bit clocked in SDI must be set to 0 to enable a write command.
- The second bit clocked in SDI, the R/$\overline{W}$ bit, must be cleared to 0.
- Bit ADD5 to Bit ADD0 clocked in SDI contain the register address to be written.
- The subsequent eight bits (Bits[DIN7:DIN0]) clocked in SDI contain the data to be written to the selected register. Data is clocked in from SDI on the falling edge of SCLK, while data is clocked out on $D_{OUT}A$ on the rising edge of SCLK.

When writing continuously to the device, the data that appears on $D_{OUT}A$ is from the register address that was written to on the previous frame, as shown in Figure 112. The $D_{OUT}B$, $D_{OUT}C$, and $D_{OUT}D$ pins are kept low during the transmission.

While in register mode, no ADC data is clocked out because the $D_{OUT}x$ lines are used to clock out register content. After writing all required registers, keeping the SDI line low for 16 SCLK cycles returns the AD7606C-18 to ADC mode, where the ADC data is again clocked out on the $D_{OUT}x$ lines, as shown in Figure 111.

In software mode, when the CRC is turned on, eight additional bits are clocked in and out on each frame. Therefore, 24-bit frames are required.

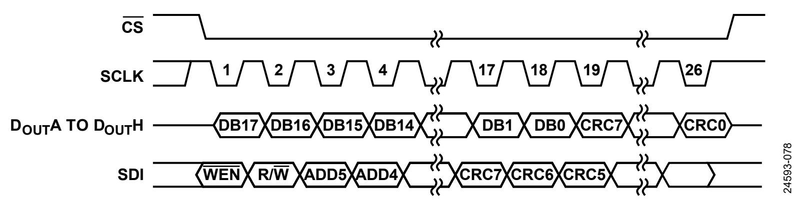


Figure 112. AD7606C-18 Serial Interface, Single Write Command, SDI Clocks in the Address Bit ADD5 to Bit ADD0 and the Register Content Bit DIN7 to Bit DIN0 During the Same Frame, $D_{OUT}A$ Provides Register Content Requested on the Previous Frame

Serial Register Mode with CRC

Registers can be written to and read from the AD7606C-18 with CRC enabled, in software mode, by asserting the INT_CRC_ERR_EN bit (Address 0x21, Bit 2).

When reading a register, the AD7606C-18 provides eight additional bits on the D_{OUT}A pin with the CRC resultant of the data shifted out previously on the same frame. The controller can then check whether the data received is correct by applying the following polynomial:

$$x^8 + x^2 + x + 1$$

With the CRC enabled, the SPI frames extend to 24 bits in length, as shown in Figure 113.

When writing a register, the controller must clock the data (register address plus register content) in the AD7606C-18 followed by an 8-bit CRC word, calculated from the previous 16 bits using the above polynomial. The AD7606C-18 reads the register address and the register content, calculates the corresponding 8-bit CRC word, and asserts the INT_CRC_ERR bit (Address 0x22, Bit 2) if the calculated CRC word does not match the CRC word received between the 17th and 24th bit through the SDI, as shown in Figure 114.

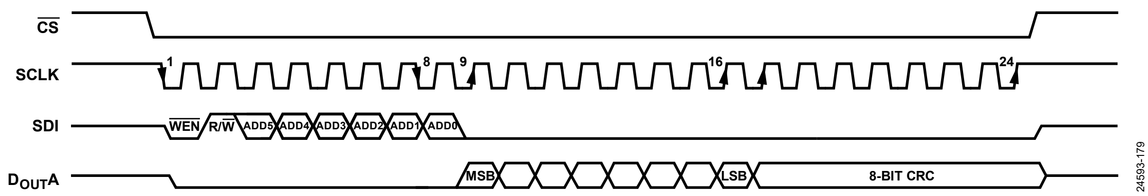


Figure 113. Reading Registers Through the SPI with CRC Enabled

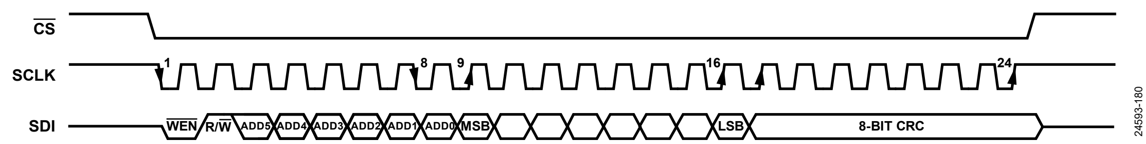


Figure 114. Writing Registers Through the SPI with CRC Enabled

DIAGNOSTICS

Diagnostic features are available in software mode to verify the correct operation of the AD7606C-18. The list of diagnostic monitors includes reset detection, overvoltage detection, undervoltage detection, analog input open circuit detection, and digital error detection.

If an error is detected, a flag asserts on the status header, if enabled, as described in the Digital Interface section. This flag points to the registers on which the error is located, as explained in the following sections.

In addition, a diagnostic multiplexer can dedicate any channel to verify a series of internal nodes, as explained in the Diagnostics Multiplexer section.

RESET DETECTION

The RESET_DETECT bit on the status register (Address 0x01, Bit 7) asserts if either a partial reset or full reset pulse is applied to the AD7606C-18. On power-up, a full reset is required. This reset asserts the RESET_DETECT bit, indicating that the power-on reset (POR) initialized properly on the device.

The POR monitors the REGCAP voltage and issues a full reset if the voltage drops under a certain threshold.

The RESET_DETECT bit can be used to detect an unexpected device reset or a large glitch on the RESET pin, or a voltage drop on the supplies.

The RESET_DETECT bit is only cleared by reading the status register.

DIGITAL ERROR

Both the status register and status header contain a DIGITAL_ERROR bit. This bit asserts when any of the following monitors trigger:

- Memory map CRC, read only memory (ROM) CRC, and digital interface CRC.
- SPI invalid read or write.
- BUSY stuck high.

To find out which monitor triggered the DIGITAL_ERROR bit, the DIGITAL_DIAG_ERR register (Address 0x22) has a bit dedicated for each of them, as explained in the ROM CRC, Memory Map CRC, Interface CRC Checksum, Interface Check, SPI Invalid Read and Write, and BUSY Stuck High sections.

ROM CRC

The ROM stores the factory trimming settings for the AD7606C-18. After power-up, the ROM content is loaded to registers during device initialization. After the load, a CRC is calculated on the loaded data and verified if the result matches the CRC stored in the ROM.

The AD7606C-18 uses the following 16-bit CRC polynomial to calculate the CRC checksum value on the memory map:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^8 + x^6 + x^4 + x^3 + x + 1 \quad (0xBAAD)$$

If the calculated and stored CRC values do not match, the error checking and correction (ECC) block can detect up to 3 bit errors (hamming distance of 4). Otherwise, the ROM_CRC_ERR (Address 0x22, Bit 0) asserts. When ROM_CRC_ERR asserts after power-up, it is recommended to issue a full reset to reload all factory settings.

This ROM CRC monitoring feature is enabled by default but can be disabled by clearing the ROM_CRC_ERR_EN bit (Address 0x21, Bit 0).

Memory Map CRC

The memory map CRC is disabled by default. After the AD7606C-18 is configured in software mode through writing the required registers, the memory map CRC can be enabled through the MM_CRC_ERR_EN bit (Address 0x21, Bit 1). When enabled, the CRC calculation is performed on the entire memory map and stored. Every 4 μs, the CRC on the memory map is recalculated and compared to the stored CRC value.

The AD7606C-18 uses the following 16-bit CRC polynomial to calculate the CRC checksum value on the memory map:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^8 + x^6 + x^4 + x^3 + x + 1 \quad (0xBAAD)$$

If the calculated and the stored CRC values do not match, the ECC block can detect up to 3 bit errors (hamming distance of 4). Otherwise, the memory map is corrupted and the MM_CRC_ERR bit (Address 0x22, Bit 1) asserts. Every time the memory map is written, the CRC is recalculated and the new value stored.

If the MM_CRC_ERR bit asserts, it is recommended to write the memory map to recalculate the CRC. If the MM_CRC_ERR bit persists, it is recommended to issue a full reset to restore the default contents of the memory map.

Interface CRC Checksum

The AD7606C-18 has a CRC checksum mode to improve interface robustness by detecting errors in data transmission. The CRC feature is available in both ADC modes (serial and parallel) and register mode (serial only).

The AD7606C-18 uses the following 16-bit CRC polynomial to calculate the CRC checksum value:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^8 + x^6 + x^4 + x^3 + x + 1 \quad (0xBAAD)$$

To replicate the polynomial division in the controller, the data shifts left by 16 bits to create a number ending in 16 Logic 0s. The polynomial is aligned so that the MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure repeats. This process repeats until the original data is reduced to a value less than the polynomial, which results in the 16-bit checksum.

An example of the CRC calculation for the 16-bit data is shown in Table 28. The CRC corresponding to the data 0x064E, using the previously described polynomial, is 0x2137.

The serial interface supports the CRC when enabled via the INT_CRC_ERR_EN bit (Address 0x21, Bit 2). The CRC is a 16-bit word that is appended to the end of each D_{OUT}x line in use after reading all the channels. An example using four D_{OUT}x lines is shown in Figure 115.

If using two D_{OUT}x lines (D_{OUT}A and D_{OUT}B), each 16-bit CRC word is calculated using data from four channels (72 bits), as shown in Figure 116. If using only one D_{OUT}x line, all eight channels are clocked out through D_{OUT}A, followed by the 16-bit CRC word calculated using data from the eight channels (144 bits).

Table 28. Example CRC Calculation for 16-Bit Data[1, 2]

Data	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Process Data	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Polynomial						1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1										
						0	1	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0									
							1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1									
							0	1	0	1	1	1	0	0	0	1	1	1	0	1	1	0	1	0								
								1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1								
								0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0		
														1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1		
														0	0	1	0	1	0	1	0	1	0	0	0	1	1	0	1	1	0	0
																1	0	1	1	1	0	1	0	1	0	1	0	1	1	0	1	1
CRC																	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1

[1] This table represents the division of the data. Blank cells are for formatting purposes.
[2] X = don't care.

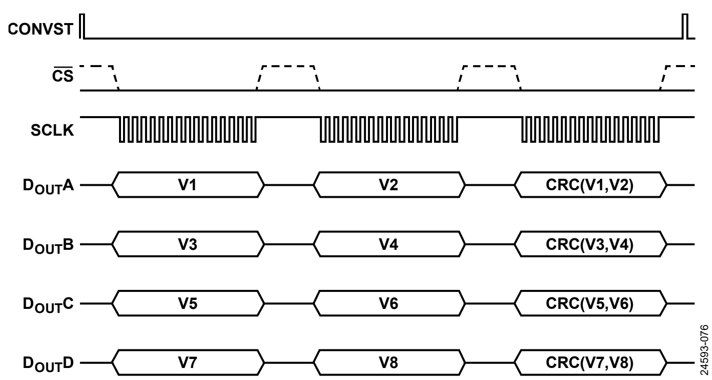


Figure 115. Serial Interface ADC Reading with CRC On, Four D_{OUT}x Lines

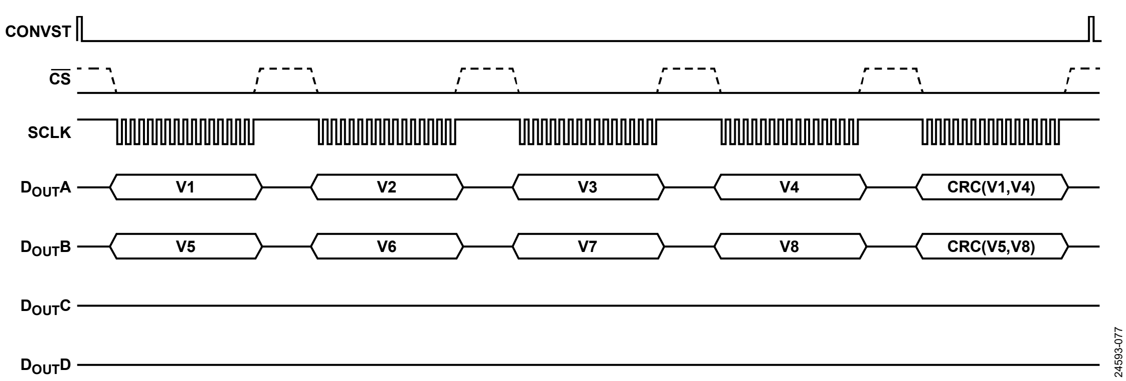


Figure 116. Serial Interface ADC Reading with CRC On, Two D_{OUT}x Lines

When the AD7606C-18 is in register mode and registers are being read or written, the CRC polynomial used is x8 + x2 + x + 1 (0x83). When reading a register, and CRC is enabled, each SPI frame is 26 bits long and the CRC 8-bit word is clocked out from the 17th to 24th SCLK cycle. Similarly, when writing a register, a CRC word can be appended on the SDI line, as shown in Figure 117. The AD7606C-18 checks and triggers an error, INT_CRC_ERR (Address 0x22, Bit 2), if the CRC word given and the CRC word internally calculated do not match.

The parallel interface also supports CRC in ADC mode only, and it is clocked out through DB17 to DB2 after Channel 8, as shown in Figure 101. The 16-bit CRC word is calculated using data from the eight channels (128 bits).

Interface Check

The integrity of the digital interface can be checked by setting the INTERFACE_CHECK_EN bit (Address 0x21, Bit 7). Selecting the interface check forces the conversion result registers to a known value, as shown in Table 29.

Verifying that the controller receives the data in Table 29 ensures that the interface between the AD7606C-18 and the controller operates properly. If the interface CRC is enabled because the data transmitted is known, this mode verifies that the controller performs the CRC calculation properly.

Table 29. Interface Check Conversion Results

Channel Number	Conversion Result Forced (Hex)
V1	0x2ACCA
V2	0x15CC5
V3	0x2A33A
V4	0x15335
V5	0x0CAAC
V6	0x0C55C
V7	0x33AA3
V8	0x33553

SPI Invalid Read and Write

When attempting to read back an invalid register address, the SPI_READ_ERR bit (Address 0x22, Bit 4) is set. The invalid readback address detection can be enabled by setting the SPI_READ_ERR_EN bit (Address 0x21, Bit 4). If an SPI read error is triggered, it is cleared by overwriting that bit or disabling the checker.

When attempting to write to an invalid register address or a read only register, the SPI_WRITE_ERR bit (Address 0x22, Bit 3) is set. The invalid write address detection can be enabled by setting the SPI_WRITE _ERR_EN bit (Address 0x21, Bit 3). If an SPI write error is triggered, it is cleared by overwriting that bit or disabling the checker.

BUSY Stuck High

BUSY stuck high monitoring is enabled by setting the BUSY_STUCK_HIGH_ERR_EN bit (Address 0x21, Bit 5). After this bit is enabled, the conversion time (t_{CONV} in Table 3) is monitored internally with an independent clock. If t_{CONV} exceeds 4 μs, the AD7606C-18 automatically issues a partial reset and asserts the BUSY_STUCK_HIGH_ERR bit (Address 0x22, Bit 5). To clear this error flag, the BUSY_STUCK_HIGH_ERR bit must be overwritten with a 1.

When oversampling mode is enabled, the individual conversion time for each internal conversion is monitored.

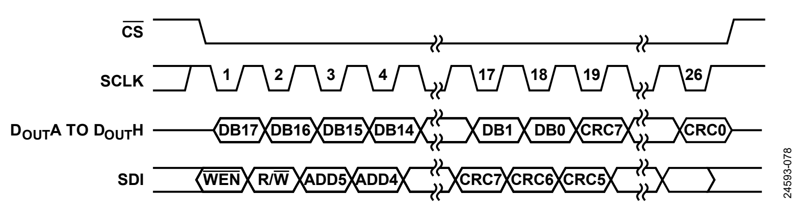


Figure 117. Register Write with CRC On

DIAGNOSTICS MULTIPLEXER

All eight input channels contain a diagnostics multiplexer in front of the PGA that monitors the internal nodes described in Table 30 to ensure the correct operation of the AD7606C-18. For accurate measurements, it is recommended to use Channel 8, where the offset and gain for diagnostic channels have been trimmed in production.

Table 30 shows the bit decoding for the diagnostic mux register on Channel 1 as an example. When an internal node is selected, the input voltage at the input pins is deselected from the PGA, as shown in Figure 118.

Each diagnostic multiplexer configuration is accessed in software mode through the corresponding register (Address 0x28 to Address 0x2B). To use the multiplexer on one channel, the ±10 V range must be selected on that channel.

Table 30. Channel 1 Diagnostic Mux Register Bit Decoding

Address 0x18			
Bit 2	**Bit 1**	**Bit 0**	**Signal on Channel 1**
0	0	0	V1
0	0	1	Temperature sensor
0	1	0	V_{REF}
0	1	1	ALDO
1	0	0	DLDO
1	0	1	V_{DRIVE}
1	1	0	AGND
1	1	1	AV_{CC}

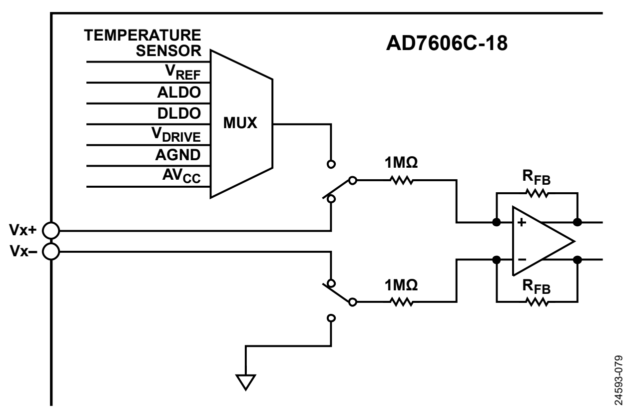


Figure 118. Diagnostic Multiplexer (Channel 1 Shown as an Example) (R_{FB} = Feedback Resistor)

Temperature Sensor

The temperature sensor can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 118. The temperature sensor voltage is measured and is proportional to the die temperature as per the following equation:

$$\text{Temperature}\,(°C) = \frac{ADC_{OUT}\,(V) - 0.19502\,(V)}{0.000618\,(V/°C)} + 25\,(°C)$$

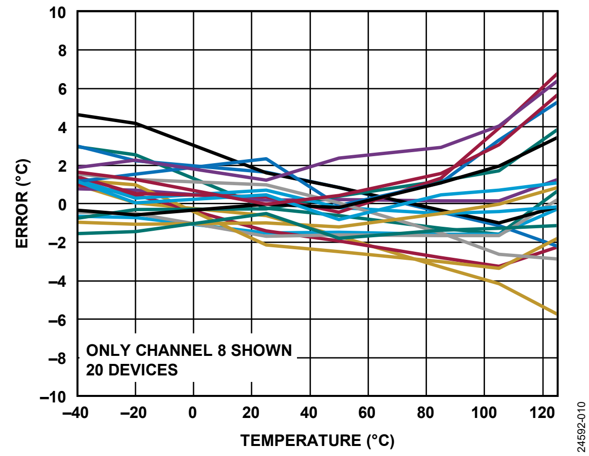


Figure 119. Temperature Sensor Error

Reference Voltage

The reference voltage can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 120. The internal or external reference is selected as an input to the diagnostic multiplexer based on the REF SELECT pin. Ideally, the ADC output follows the voltage reference level ratiometrically. Therefore, if the ADC output goes beyond the expected 2.5 V, either the reference buffer or the PGA is malfunctioning.

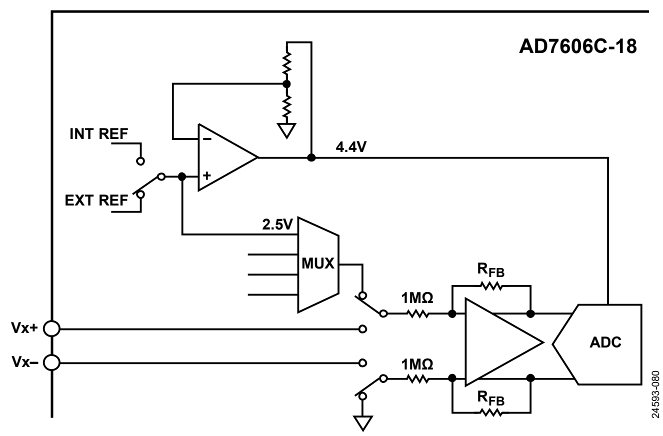


Figure 120. Reference Voltage Signal Path Through the Diagnostic Multiplexer

Internal LDOs

The analog and digital LDO (REGCAP pins) can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 118. The ADC output is four times the voltage on the REGCAP pins. This measurement verifies that each LDO is at the correct operating voltage so that the internal circuitry is biased correctly.

Supply Voltages

AV_{CC}, V_{DRIVE}, and AGND can be selected through the diagnostic multiplexer and converted with the ADC, as shown in Figure 118. This setup ensures the voltage and grounds are correctly applied to the device to ensure correct operation.

TYPICAL CONNECTION DIAGRAM

There are four AV_{CC} supply pins on the AD7606C-18 and it is recommended that each of the four pins are decoupled using a 100 nF capacitor at each supply pin and a 10 µF capacitor at the supply source. The AD7606C-18 can operate with the internal reference or an externally applied reference. When using a single AD7606C-18 device on the PCB, decouple the REFIN/REFOUT pin with a 100 nF capacitor. Refer to the Reference section when using an application with multiple AD7606C-18 devices. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The V_{DRIVE} voltage controls the voltage value of the output logic signals. For more information on layout, decoupling, and grounding, see the Layout Guidelines section.

After supplies are applied to the AD7606C-18, apply a full reset to the AD7606C-18 to ensure that it is configured for the correct mode of operation.

In Figure 120, the AD7606C-18 is configured in hardware mode and is operating with the internal reference because the REF SELECT pin is set to logic high. In this example, the device also uses the parallel interface because the $\overline{\text{PAR}}$/SER SEL pin is tied to AGND. The analog input range for all eight channels is ±10 V, provided the RANGE pin is tied to a high level and the oversampling ratio is controlled through the OSx pins by the controller.

In Figure 121, the AD7606C-18 is configured in software mode because the OSx pins are at logic level high. The oversampling ratio, as well as each channel range, are configured by accessing the memory map. In this example, the $\overline{\text{PAR}}$/SER SEL pin is at logic level high. Therefore, the serial interface is used for both reading the ADC data and reading and writing the memory map. The REF SELECT pin is tied to AGND. Therefore, the internal reference is disabled and an external reference is connected externally to the REFIN/REFOUT pin and decoupled through a 100 nF capacitor.

Figure 120 and Figure 121 are examples of typical connection diagrams. Other combinations of the reference, data interface, and operation mode are also possible, depending on the logic levels applied to each configuration pin.

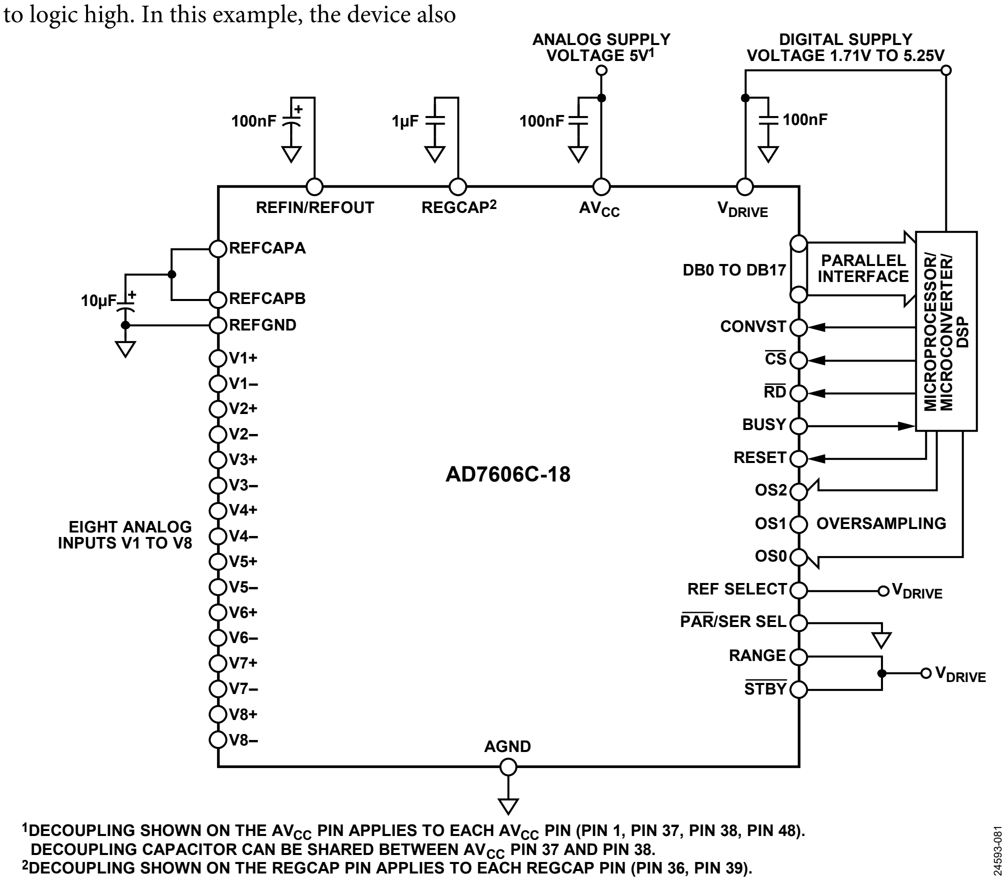


Figure 120. Typical Connection Diagram, Hardware Mode

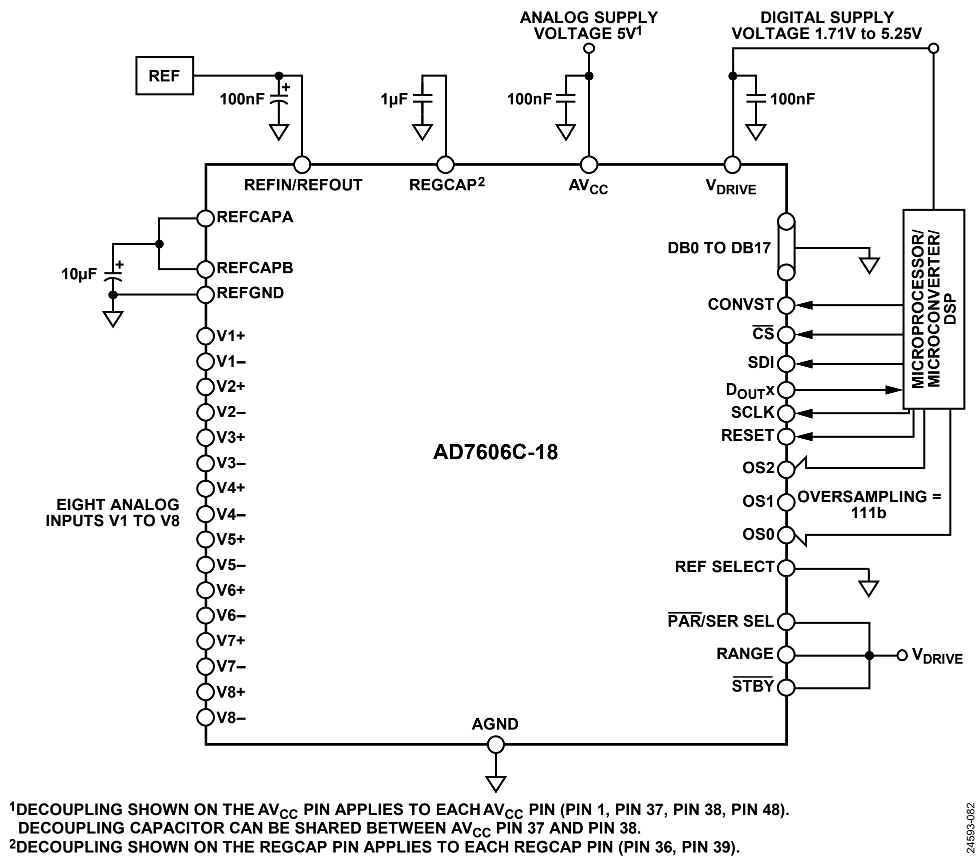


Figure 121. Typical Connection Diagram, Software Mode

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

The following layout guidelines are recommended to be followed when designing the PCB that houses the AD7606C-18:

- If the AD7606C-18 is in a system where multiple devices require analog-to-digital ground connections, use a solid ground plane (without splitting between analog and digital grounds).
- Make stable connections to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.
- Avoid running digital lines under the devices because doing so couples noise on the die. Allow the analog ground plane to run under the AD7606C-18 to avoid noise coupling.
- Shield fast switching signals like CONVST or clocks with digital ground to avoid radiating noise to other sections of the board and ensure that they do not run near analog signal paths.
- Avoid crossover of digital and analog signals.
- Ensure traces on layers in close proximity on the board run at right angles to each other to reduce the effect of feedthrough through the board.
- Ensure power supply lines to the AV_{CC} and V_{DRIVE} pins on the AD7606C-18 use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Where possible, use supply planes and make stable connections between the AD7606C-18 supply pins and the power tracks on the board. Use a single via or multiple vias for each supply pin.
- Place the decoupling capacitors close to (ideally, directly against) the supply pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA pin and REFCAPB pin as close as possible to their respective AD7606C-18 pins. Where possible, place the pins on the same side of the board as the AD7606C-18 device.

Figure 122 shows the recommended decoupling on the top layer of the AD7606C-18 PCB. Figure 123 shows bottom layer decoupling, which is used for the four AV_{CC} pins and the V_{DRIVE} pin decoupling. Where the ceramic 100 nF capacitors for the AV_{CC} pins are placed close to their respective device pins, a single 100 nF capacitor can be shared between Pin 37 and Pin 38.

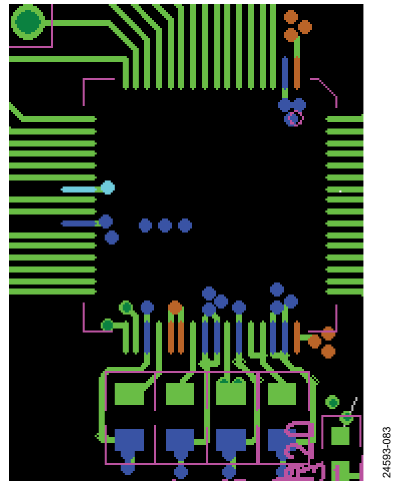


Figure 122. Top Layer Decoupling REFIN/REFOUT, REFCAPA, REFCAPB, and REGCAP Pins

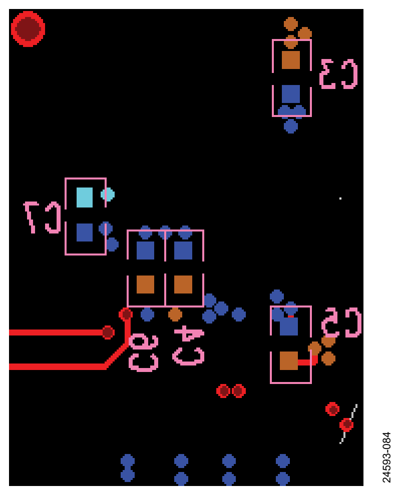


Figure 123. Bottom Layer Decoupling

To ensure stable device to device performance matching in a system that contains multiple AD7606C-18 devices, a symmetrical layout between the AD7606C-18 devices is important.

Figure 124 shows a layout with two AD7606C-18 devices. The AV_{CC} supply plane runs to the right of both devices, and the V_{DRIVE} supply track runs to the left of the two devices. The reference chip is positioned between the two devices, and the reference voltage track runs north to Pin 42 of U1 and south to Pin 42 of U2. A solid ground plane is used.

These symmetrical layout principles can also be applied to a system that contains more than two AD7606C-18 devices. The AD7606C-18 devices can be placed in a north to south direction, with the reference voltage located midway between the devices and the reference track running in the north to south direction, similar to Figure 124.

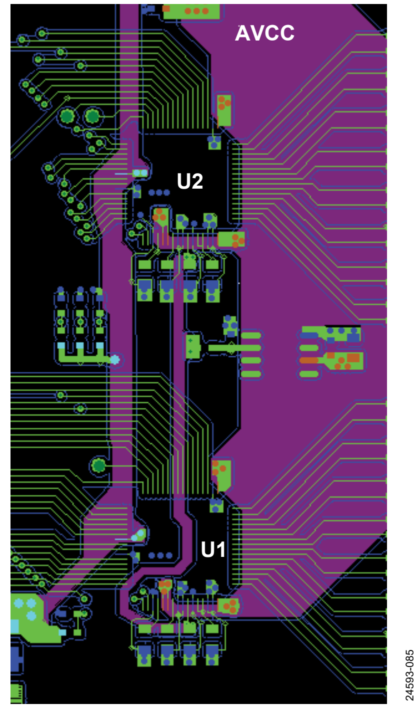


Figure 124. Layout for Multiple AD7606C-18 Devices—Top Layer and Supply Plane Layer

REGISTER SUMMARY

Table 31. AD7606C-18 Register Summary

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x01	STATUS	RESET_DETECT	DIGITAL_ERROR	OPEN_DETECTED	RESERVED					0x00	R
0x02	CONFIG	RESERVED	STATUS_HEADER	EXT_OS_CLOCK	DOUT_FORMAT		RESERVED	OPERATION_MODE		0x08	R/W
0x03	RANGE_CH1_ CH2	CH2_RANGE				CH1_RANGE				0x33	R/W
0x04	RANGE_CH3_ CH4	CH4_RANGE				CH3_RANGE				0x33	R/W
0x05	RANGE_CH5_ CH6	CH6_RANGE				CH5_RANGE				0x33	R/W
0x06	RANGE_CH7_ CH8	CH8_RANGE				CH7_RANGE				0x33	R/W
0x07	BANDWIDTH	CH8_BW	CH7_BW	CH6_BW	CH5_BW	CH4_BW	CH3_BW	CH2_BW	CH1_BW	0x00	R/W
0x08	OVERSAMPLING	OS_PAD				OS_RATIO				0x00	R/W
0x09	CH1_GAIN	RESERVED		CH1_GAIN						0x00	R/W
0x0A	CH2_GAIN	RESERVED		CH2_GAIN						0x00	R/W
0x0B	CH3_GAIN	RESERVED		CH3_GAIN						0x00	R/W
0x0C	CH4_GAIN	RESERVED		CH4_GAIN						0x00	R/W
0x0D	CH5_GAIN	RESERVED		CH5_GAIN						0x00	R/W
0x0E	CH6_GAIN	RESERVED		CH6_GAIN						0x00	R/W
0x0F	CH7_GAIN	RESERVED		CH7_GAIN						0x00	R/W
0x10	CH8_GAIN	RESERVED		CH8_GAIN						0x00	R/W
0x11	CH1_OFFSET	CH1_OFFSET								0x80	R/W
0x12	CH2_OFFSET	CH2_OFFSET								0x80	R/W
0x13	CH3_OFFSET	CH3_OFFSET								0x80	R/W
0x14	CH4_OFFSET	CH4_OFFSET								0x80	R/W
0x15	CH5_OFFSET	CH5_OFFSET								0x80	R/W
0x16	CH6_OFFSET	CH6_OFFSET								0x80	R/W
0x17	CH7_OFFSET	CH7_OFFSET								0x80	R/W
0x18	CH8_OFFSET	CH8_OFFSET								0x80	R/W
0x19	CH1_PHASE	CH1_PHASE								0x00	R/W
0x1A	CH2_PHASE	CH2_PHASE								0x00	R/W
0x1B	CH3_PHASE	CH3_PHASE								0x00	R/W
0x1C	CH4_PHASE	CH4_PHASE								0x00	R/W
0x1D	CH5_PHASE	CH5_PHASE								0x00	R/W
0x1E	CH6_PHASE	CH6_PHASE								0x00	R/W
0x1F	CH7_PHASE	CH7_PHASE								0x00	R/W
0x20	CH8_PHASE	CH8_PHASE								0x00	R/W
0x21	DIGITAL_ DIAG_ ENABLE	INTERFACE_ CHECK_EN	CLK_FS_OS_ COUNTER_EN	BUSY_STUCK_ HIGH_ERR_EN	SPI_READ _ERR_EN	SPI_ WRITE_ ERR_EN	INT_CRC_ ERR_EN	MM_CRC_ ERR_EN	ROM_ CRC_ ERR_EN	0x01	R/W
0x22	DIGITAL_ DIAG_ERR	RESERVED		BUSY_STUCK_ HIGH_ERR	SPI_ READ_ ERR	SPI_ WRITE_ ERR	INT_CRC_ ERR	MM_CRC_ ERR	ROM_ CRC_ ERR	0x00	R/W
0x23	OPEN_ DETECT_ ENABLE	CH8_OPEN_ DETECT_EN	CH7_OPEN_ DETECT_EN	CH6_OPEN_ DETECT_EN	CH5_ OPEN_ DETECT_ EN	CH4_ OPEN_ DETECT_ EN	CH3_OPEN_ DETECT_EN	CH2_OPEN_ DETECT_EN	CH1_ OPEN_ DETECT_ EN	0x00	R/W
0x24	OPEN_ DETECTED	CH8_OPEN	CH7_OPEN	CH6_OPEN	CH5_ OPEN	CH4_ OPEN	CH3_OPEN	CH2_OPEN	CH1_ OPEN	0x00	R/W
0x28	DIAGNOSTIC_ MUX_CH1_2	RESERVED		CH2_DIAG_MUX_CTRL			CH1_DIAG_MUX_CTRL			0x00	R/W
0x29	DIAGNOSTIC_ MUX_CH3_4	RESERVED		CH4_DIAG_MUX_CTRL			CH3_DIAG_MUX_CTRL			0x00	R/W
0x2A	DIAGNOSTIC_ MUX_CH5_6	RESERVED		CH6_DIAG_MUX_CTRL			CH5_DIAG_MUX_CTRL			0x00	R/W
0x2B	DIAGNOSTIC_ MUX_CH7_8	RESERVED		CH8_DIAG_MUX_CTRL			CH7_DIAG_MUX_CTRL			0x00	R/W
0x2C	OPEN_DETECT_ QUEUE	OPEN_DETECT_QUEUE								0x00	R/W
0x2D	FS_CLK_ COUNTER	CLK_FS_COUNTER								0x00	R
0x2E	OS_CLK_ COUNTER	CLK_OS_COUNTER								0x00	R
0x2F	ID	DEVICE_ID				SILICON_REVISION				0x31	R

REGISTER DETAILS

Address: 0x01, Reset: 0x00, Name: STATUS

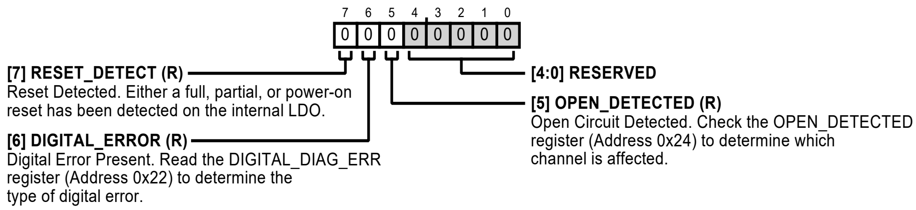


Table 32. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
7	RESET_DETECT	Reset Detected. Either a full, partial, or power-on reset has been detected on the internal LDO.	0x0	R
6	DIGITAL_ERROR	Digital Error Present. Read the DIGITAL_DIAG_ERR register (Address 0x22) to determine the type of digital error.	0x0	R
5	OPEN_DETECTED	Open Circuit Detected. Check the OPEN_DETECTED register (Address 0x24) to determine which channel is affected.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x02, Reset: 0x08, Name: CONFIG

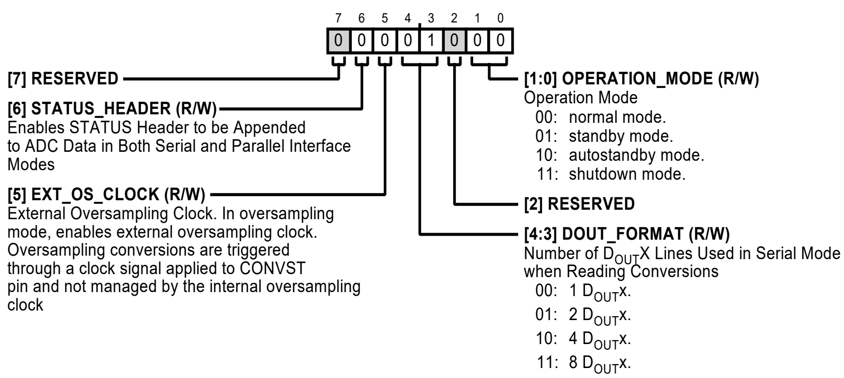


Table 33. Bit Descriptions for CONFIG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	STATUS_HEADER	Enables STATUS Header to be Appended to ADC Data in Both Serial and Parallel Interface Modes.	0x0	R/W
5	EXT_OS_CLOCK	External Oversampling Clock. In oversampling mode, enables external oversampling clock. Oversampling conversions are triggered through a clock signal applied to CONVST pin and not managed by the internal oversampling clock.	0x0	R/W
[4:3]	DOUT_FORMAT	Number of D_{OUT}x Lines Used in Serial Mode when Reading Conversions. 00: 1 D_{OUT}x. 01: 2 D_{OUT}x. 10: 4 D_{OUT}x. 11: 8 D_{OUT}x.	0x1	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	OPERATION_MODE	Operation Mode. 00: normal mode. 01: standby mode. 10: autostandby mode. 11: shutdown mode.	0x0	R/W

Address: 0x03, Reset: 0x33, Name: RANGE_CH1_CH2

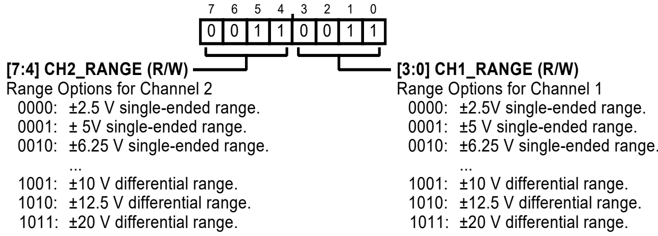


Table 34. Bit Descriptions for RANGE_CH1_CH2

Bits	Bit Name	Description	Reset	Access
[7:4]	CH2_RANGE	Range Options for Channel 2. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.	0x3	R/W
[3:0]	CH1_RANGE	Range Options for Channel 1. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.	0x3	R/W

Address: 0x04, Reset: 0x33, Name: RANGE_CH3_CH4

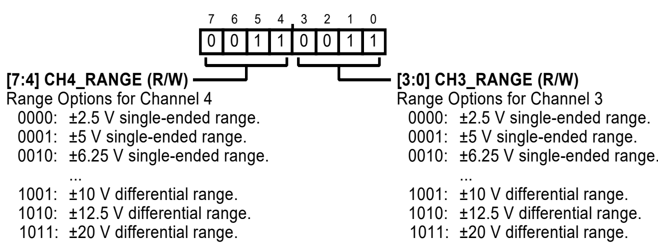


Table 35. Bit Descriptions for RANGE_CH3_CH4

Bits	Bit Name	Description	Reset	Access
[7:4]	CH4_RANGE	Range Options for Channel 4. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range.	0x3	R/W

Bits	Bit Name	Description	Reset	Access
		0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.		
[3:0]	CH3_RANGE	Range Options for Channel 3. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.	0x3	R/W

Address: 0x05, Reset: 0x33, Name: RANGE_CH5_CH6

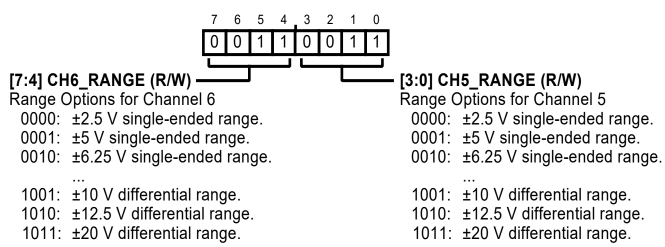


Table 36. Bit Descriptions for RANGE_CH5_CH6

Bits	Bit Name	Description	Reset	Access
[7:4]	CH6_RANGE	Range Options for Channel 6. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.	0x3	R/W
[3:0]	CH5_RANGE	Range Options for Channel 5. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range.	0x3	R/W

Bits	Bit Name	Description	Reset	Access
		0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.		

Address: 0x06, Reset: 0x33, Name: RANGE_CH7_CH8

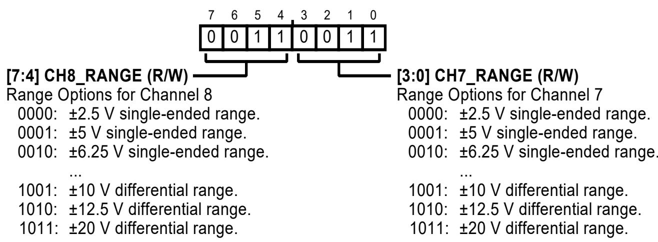


Table 37. Bit Descriptions for RANGE_CH7_CH8

Bits	Bit Name	Description	Reset	Access
[7:4]	CH8_RANGE	Range Options for Channel 8. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.	0x3	R/W
[3:0]	CH7_RANGE	Range Options for Channel 7. 0000: ±2.5 V single-ended range. 0001: ±5 V single-ended range. 0010: ±6.25 V single-ended range. 0011: ±10 V single-ended range. 0100: ±12.5 V single-ended range. 0101: 0 V to 5 V single-ended range. 0110: 0 V to 10 V single-ended range. 0111: 0 V to 12.5 V single-ended range. 1000: ±5 V differential range. 1001: ±10 V differential range. 1010: ±12.5 V differential range. 1011: ±20 V differential range.	0x3	R/W

Address: 0x07, Reset: 0x00, Name: BANDWIDTH

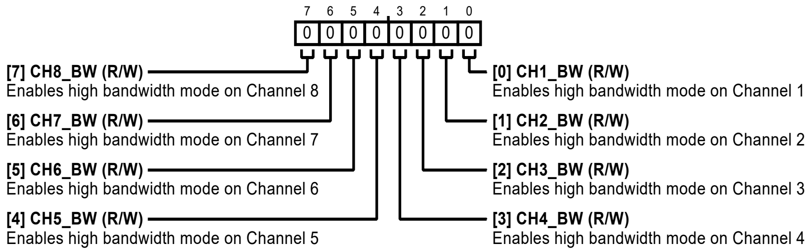


Table 38. Bit Descriptions for BANDWIDTH

Bits	Bit Name	Description	Reset	Access
7	CH8_BW	Enables high bandwidth mode on Channel 8.	0x0	R/W
6	CH7_BW	Enables high bandwidth mode on Channel 7.	0x0	R/W
5	CH6_BW	Enables high bandwidth mode on Channel 6.	0x0	R/W
4	CH5_BW	Enables high bandwidth mode on Channel 5.	0x0	R/W
3	CH4_BW	Enables high bandwidth mode on Channel 4.	0x0	R/W
2	CH3_BW	Enables high bandwidth mode on Channel 3.	0x0	R/W
1	CH2_BW	Enables high bandwidth mode on Channel 2.	0x0	R/W
0	CH1_BW	Enables high bandwidth mode on Channel 1.	0x0	R/W

Address: 0x08, Reset: 0x00, Name: OVERSAMPLING

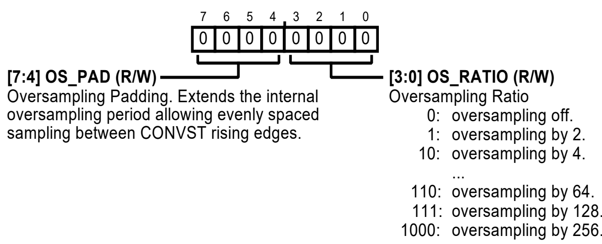


Table 39. Bit Descriptions for OVERSAMPLING

Bits	Bit Name	Description	Reset	Access
[7:4]	OS_PAD	Oversampling Padding. Extends the internal oversampling period allowing evenly spaced sampling between CONVST rising edges.	0x0	R/W
[3:0]	OS_RATIO	Oversampling Ratio. 0000: oversampling off. 0001: oversampling by 2. 0010: oversampling by 4. 0011: oversampling by 8. 0100: oversampling by 16. 0101: oversampling by 32. 0110: oversampling by 64. 0111: oversampling by 128. 1000: oversampling by 256.	0x0	R/W

Address: 0x09, Reset: 0x00, Name: CH1_GAIN

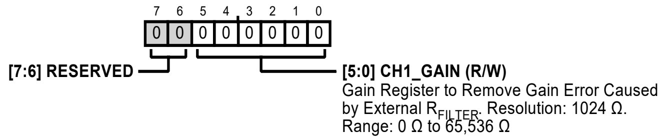


Table 40. Bit Descriptions for CH1_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH1_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0A, Reset: 0x00, Name: CH2_GAIN

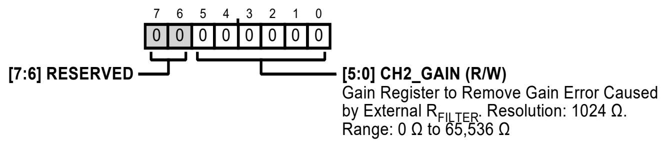


Table 41. Bit Descriptions for CH2_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH2_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0B, Reset: 0x00, Name: CH3_GAIN

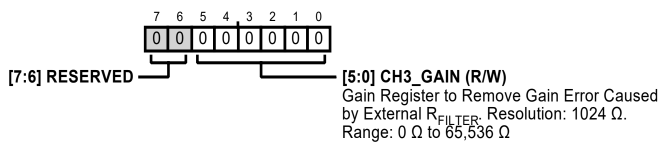


Table 42. Bit Descriptions for CH3_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH3_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0C, Reset: 0x00, Name: CH4_GAIN

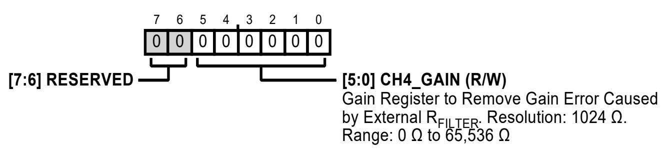


Table 43. Bit Descriptions for CH4_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH4_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0D, Reset: 0x00, Name: CH5_GAIN

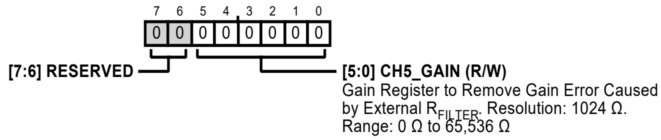


Table 44. Bit Descriptions for CH5_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH5_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0E, Reset: 0x00, Name: CH6_GAIN

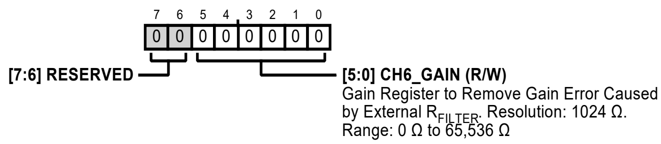


Table 45. Bit Descriptions for CH6_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH6_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x0F, Reset: 0x00, Name: CH7_GAIN

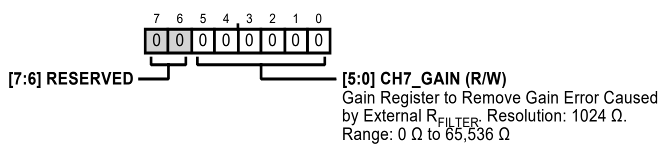


Table 46. Bit Descriptions for CH7_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH7_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x10, Reset: 0x00, Name: CH8_GAIN

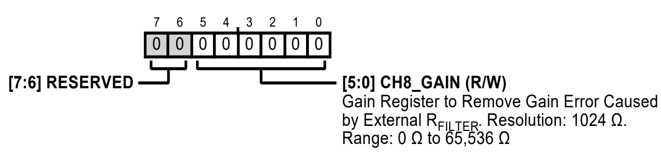


Table 47. Bit Descriptions for CH8_GAIN

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CH8_GAIN	Gain Register to Remove Gain Error Caused by External R_{FILTER}. Resolution: 1024 Ω. Range: 0 Ω to 65,536 Ω.	0x0	R/W

Address: 0x11, Reset: 0x80, Name: CH1_OFFSET

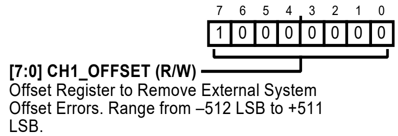


Table 48. Bit Descriptions for CH1_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x12, Reset: 0x80, Name: CH2_OFFSET

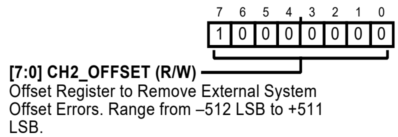


Table 49. Bit Descriptions for CH2_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH2_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x13, Reset: 0x80, Name: CH3_OFFSET

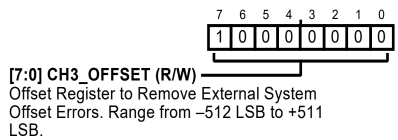


Table 50. Bit Descriptions for CH3_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH3_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x14, Reset: 0x80, Name: CH4_OFFSET

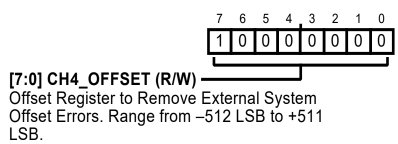


Table 51. Bit Descriptions for CH4_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH4_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x15, Reset: 0x80, Name: CH5_OFFSET

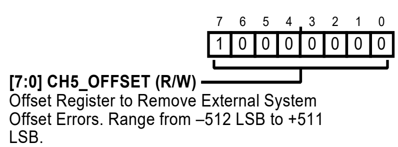


Table 52. Bit Descriptions for CH5_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH5_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x16, Reset: 0x80, Name: CH6_OFFSET

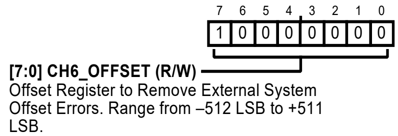


Table 53. Bit Descriptions for CH6_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH6_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x17, Reset: 0x80, Name: CH7_OFFSET

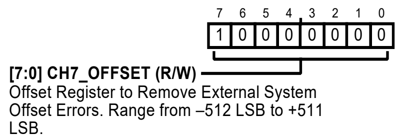


Table 54. Bit Descriptions for CH7_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH7_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x18, Reset: 0x80, Name: CH8_OFFSET

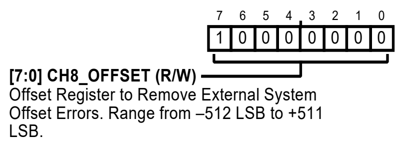


Table 55. Bit Descriptions for CH8_OFFSET

Bits	Bit Name	Description	Reset	Access
[7:0]	CH8_OFFSET	Offset Register to Remove External System Offset Errors. Range from −512 LSB to +511 LSB.	0x80	R/W

Address: 0x19, Reset: 0x00, Name: CH1_PHASE

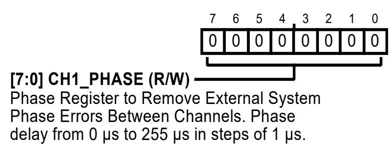


Table 56. Bit Descriptions for CH1_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x1A, Reset: 0x00, Name: CH2_PHASE

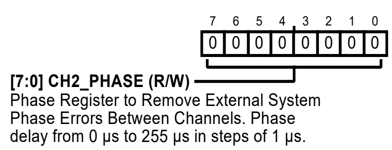


Table 57. Bit Descriptions for CH2_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH2_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x1B, Reset: 0x00, Name: CH3_PHASE

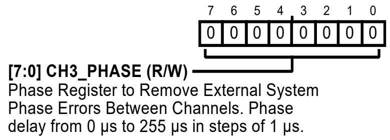


Table 58. Bit Descriptions for CH3_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH3_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x1C, Reset: 0x00, Name: CH4_PHASE

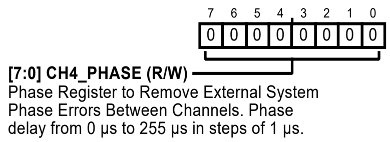


Table 59. Bit Descriptions for CH4_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH4_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: CH5_PHASE

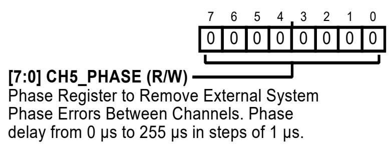


Table 60. Bit Descriptions for CH5_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH5_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x1E, Reset: 0x00, Name: CH6_PHASE

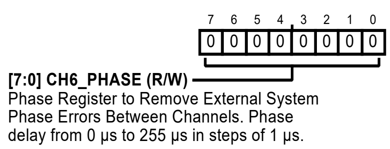


Table 61. Bit Descriptions for CH6_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH6_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: CH7_PHASE

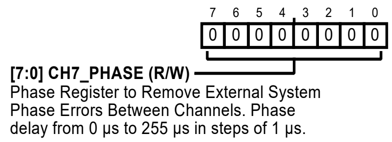


Table 62. Bit Descriptions for CH7_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH7_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x20, Reset: 0x00, Name: CH8_PHASE

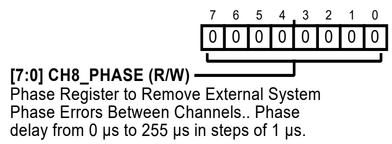


Table 63. Bit Descriptions for CH8_PHASE

Bits	Bit Name	Description	Reset	Access
[7:0]	CH8_PHASE	Phase Register to Remove External System Phase Errors Between Channels. Phase delay from 0 µs to 255 µs in steps of 1 µs.	0x0	R/W

Address: 0x21, Reset: 0x01, Name: DIGITAL_DIAG_ENABLE

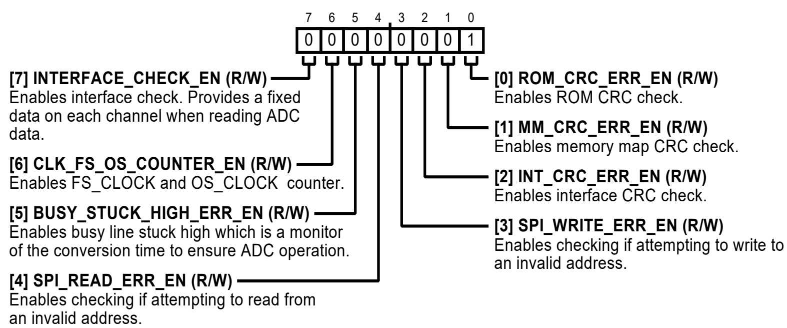


Table 64. Bit Descriptions for DIGITAL_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
7	INTERFACE_CHECK_EN	Enables interface check. Provides a fixed data on each channel when reading ADC data.	0x0	R/W
6	CLK_FS_OS_COUNTER_EN	Enables FS_CLOCK and OS_CLOCK counter.	0x0	R/W
5	BUSY_STUCK_HIGH_ERR_EN	Enables busy line stuck high which is a monitor of the conversion time to ensure ADC operation.	0x0	R/W
4	SPI_READ_ERR_EN	Enables checking if attempting to read from an invalid address.	0x0	R/W
3	SPI_WRITE_ERR_EN	Enables checking if attempting to write to an invalid address.	0x0	R/W
2	INT_CRC_ERR_EN	Enables interface CRC check.	0x0	R/W
1	MM_CRC_ERR_EN	Enables memory map CRC check.	0x0	R/W
0	ROM_CRC_ERR_EN	Enables ROM CRC check.	0x1	R/W

Address: 0x22, Reset: 0x00, Name: DIGITAL_DIAG_ERR

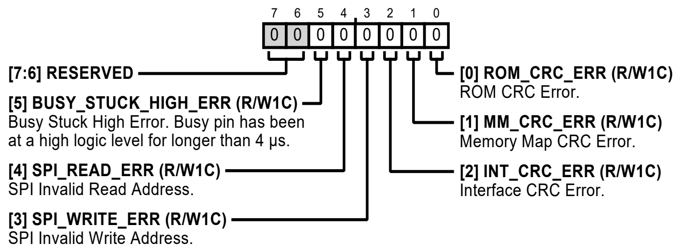


Table 65. Bit Descriptions for DIGITAL_DIAG_ERR

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	BUSY_STUCK_HIGH_ERR	Busy Stuck High Error. Busy pin has been at high logic level for longer than 4 µs.	0x0	R/W1C
4	SPI_READ_ERR	SPI Invalid Read Address.	0x0	R/W1C
3	SPI_WRITE_ERR	SPI Invalid Write Address.	0x0	R/W1C
2	INT_CRC_ERR	Interface CRC Error.	0x0	R/W1C
1	MM_CRC_ERR	Memory Map CRC Error.	0x0	R/W1C
0	ROM_CRC_ERR	ROM CRC Error.	0x0	R/W1C

Address: 0x23, Reset: 0x00, Name: OPEN_DETECT_ENABLE

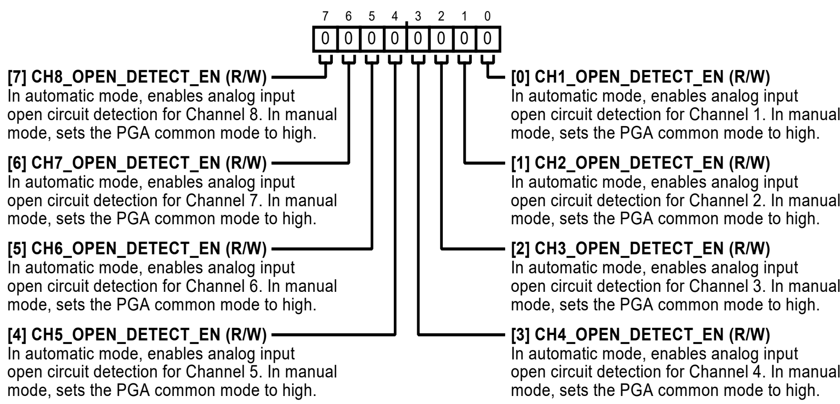


Table 66. Bit Descriptions for OPEN_DETECT_ENABLE

Bits	Bit Name	Description	Reset	Access
7	CH8_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 8. In manual mode, sets the PGA common mode to high.	0x0	R/W
6	CH7_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 7. In manual mode, sets the PGA common mode to high.	0x0	R/W
5	CH6_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 6. In manual mode, sets the PGA common mode to high.	0x0	R/W
4	CH5_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 5. In manual mode, sets the PGA common mode to high.	0x0	R/W
3	CH4_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 4. In manual mode, sets the PGA common mode to high.	0x0	R/W
2	CH3_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 3. In manual mode, sets the PGA common mode to high.	0x0	R/W
1	CH2_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 2. In manual mode, sets the PGA common mode to high.	0x0	R/W
0	CH1_OPEN_DETECT_EN	In automatic mode, enables analog input open circuit detection for Channel 1. In manual mode, sets the PGA common mode to high.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: OPEN_DETECTED

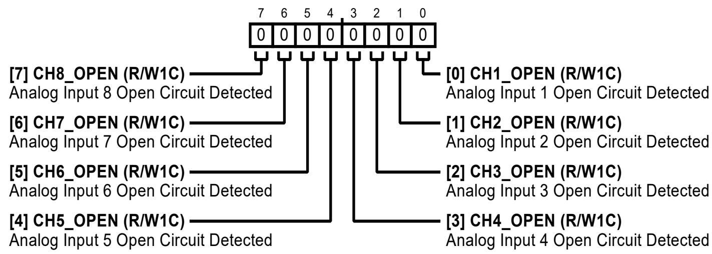


Table 67. Bit Descriptions for OPEN_DETECTED

Bits	Bit Name	Description	Reset	Access
7	CH8_OPEN	Analog Input 8 Open Circuit Detected.	0x0	R/W1C
6	CH7_OPEN	Analog Input 7 Open Circuit Detected.	0x0	R/W1C
5	CH6_OPEN	Analog Input 6 Open Circuit Detected.	0x0	R/W1C
4	CH5_OPEN	Analog Input 5 Open Circuit Detected.	0x0	R/W1C
3	CH4_OPEN	Analog Input 4 Open Circuit Detected.	0x0	R/W1C
2	CH3_OPEN	Analog Input 3 Open Circuit Detected.	0x0	R/W1C
1	CH2_OPEN	Analog Input 2 Open Circuit Detected.	0x0	R/W1C
0	CH1_OPEN	Analog Input 1 Open Circuit Detected.	0x0	R/W1C

Address: 0x28, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH1_2

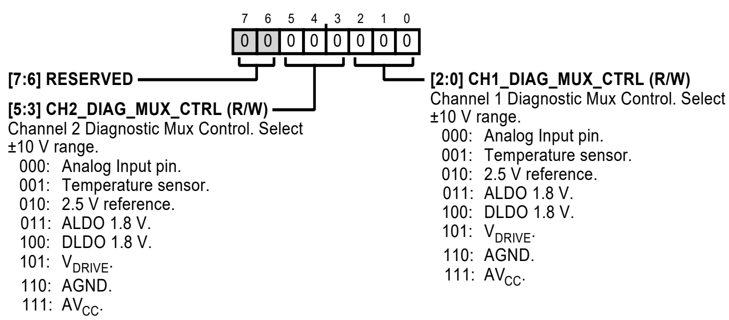


Table 68. Bit Descriptions for DIAGNOSTIC_MUX_CH1_2

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH2_DIAG_MUX_CTRL	Channel 2 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W
[2:0]	CH1_DIAG_MUX_CTRL	Channel 1 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x29, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH3_4

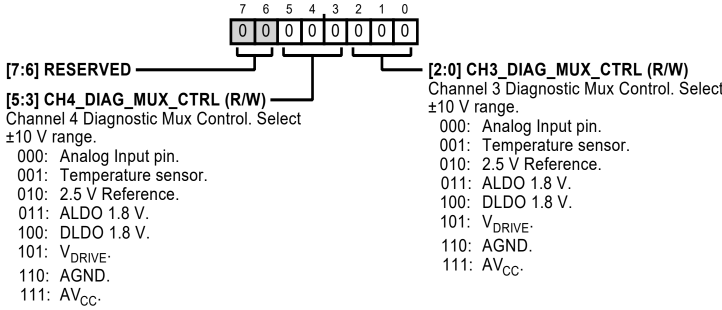


Table 69. Bit Descriptions for DIAGNOSTIC_MUX_CH3_4

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH4_DIAG_MUX_CTRL	Channel 4 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W
[2:0]	CH3_DIAG_MUX_CTRL	Channel 3 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x2A, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH5_6

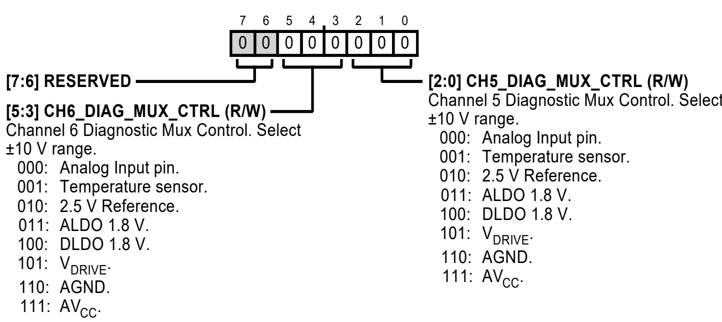


Table 70. Bit Descriptions for DIAGNOSTIC_MUX_CH5_6

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH6_DIAG_MUX_CTRL	Channel 6 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.		
[2:0]	CH5_DIAG_MUX_CTRL	Channel 5 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x2B, Reset: 0x00, Name: DIAGNOSTIC_MUX_CH7_8

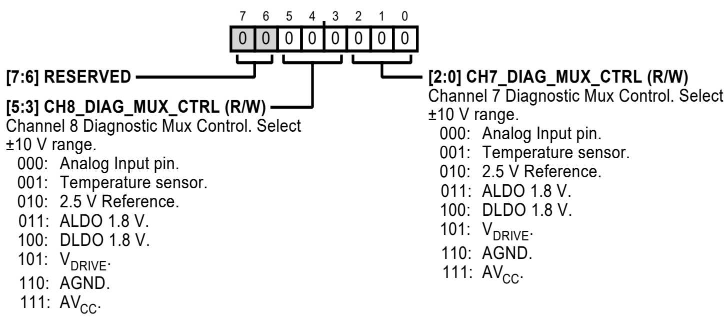


Table 71. Bit Descriptions for DIAGNOSTIC_MUX_CH7_8

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	CH8_DIAG_MUX_CTRL	Channel 8 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W
[2:0]	CH7_DIAG_MUX_CTRL	Channel 7 Diagnostic Mux Control. Select ±10 V range. 000: Analog input pin. 001: Temperature sensor. 010: 2.5 V reference. 011: ALDO 1.8 V. 100: DLDO 1.8 V. 101: V_{DRIVE}. 110: AGND. 111: AV_{CC}.	0x0	R/W

Address: 0x2C, Reset: 0x00, Name: OPEN_DETECT_QUEUE

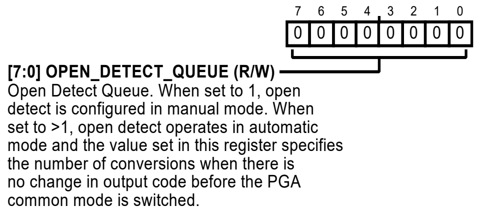


Table 72. Bit Descriptions for OPEN_DETECT_QUEUE

Bits	Bit Name	Description	Reset	Access
[7:0]	OPEN_DETECT_QUEUE	Open Detect Queue. When set to 1, open detect is configured in manual mode. When set to >1, open detect operates in automatic mode and the value set in this register specifies the number of conversions when there is no change in output code before the PGA common mode is switched.	0x0	R/W

Address: 0x2D, Reset: 0x00, Name: FS_CLK_COUNTER

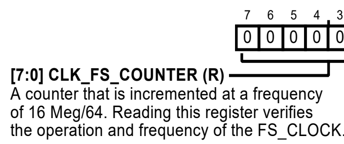


Table 73. Bit Descriptions for FS_CLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	CLK_FS_COUNTER	A counter that is incremented at a frequency of 16 Meg/64. Reading this register verifies the operation and frequency of the FS_CLOCK.	0x0	R

Address: 0x2E, Reset: 0x00, Name: OS_CLK_COUNTER

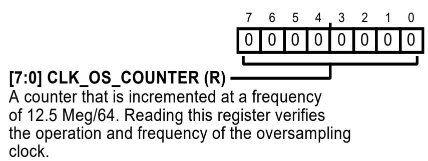


Table 74. Bit Descriptions for OS_CLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	CLK_OS_COUNTER	A counter that is incremented at a frequency of 12.5 Meg/64. Reading this register verifies the operation and frequency of the oversampling clock.	0x0	R

Address: 0x2F, Reset: 0x31, Name: ID

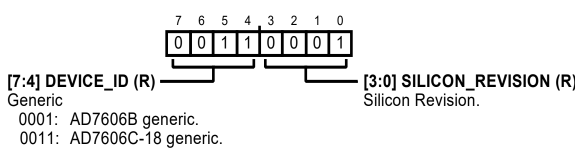


Table 75. Bit Descriptions for ID

Bits	Bit Name	Description	Reset	Access
[7:4]	DEVICE_ID	Generic. 0001: AD7606B generic. 0011: AD7606C-18 generic.	0x3	R
[3:0]	SILICON_REVISION	Silicon Revision.	0x1	R

OUTLINE DIMENSIONS

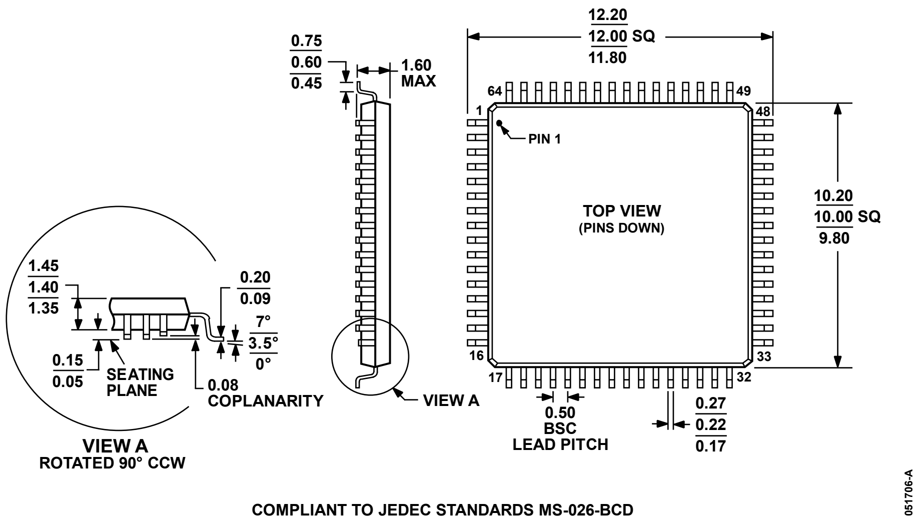


Figure 126. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7606C-18BSTZ	−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606C-18BSTZ-RL	−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7606C18FMCZ		Evaluation Board for the AD7606C-18	
EVAL-SDP-CH1Z		Evaluation Controller Board	

[1] Z = RoHS Compliant Part.