8-Channel, Li-Ion, Battery Monitoring System

Data Sheet

AD7284

FEATURES

- 8 analog input channels, integrated secondary monitor
  - ±3 mV maximum cell voltage accuracy, TUE, 14-bit ADC
- Very low measurement latency across 96 cells
- Stack voltage measurement
  - ±16 mV typical battery stack voltage (TUE) accuracy
- Cell balancing interface, with individually programmable on time
- 4 auxiliary analog input channels, 14-bit ADC
  - Suitable for thermistor inputs and external diagnostics
  - Buffered reference output for ratiometric measurements
- Internal temperature sensor
- V_{DD} operating range: 10 V to 40 V
- On-chip 5 V regulator
- Watchdog timer
- I_{DD} matching current: 100 µA
- Robust, proprietary daisy-chain interface
- SPI to host controller
- CRC protection on read and write commands
- 2 general-purpose outputs
- 64-lead low profile quad flat package, exposed pad (LQFP_EP)
- Junction temperature range: −30°C to +120°C
- Qualified for automotive applications

APPLICATIONS

- Li-Ion battery monitoring
- Electric and hybrid electric vehicles
- Stationary power applications

FUNCTIONAL BLOCK DIAGRAM

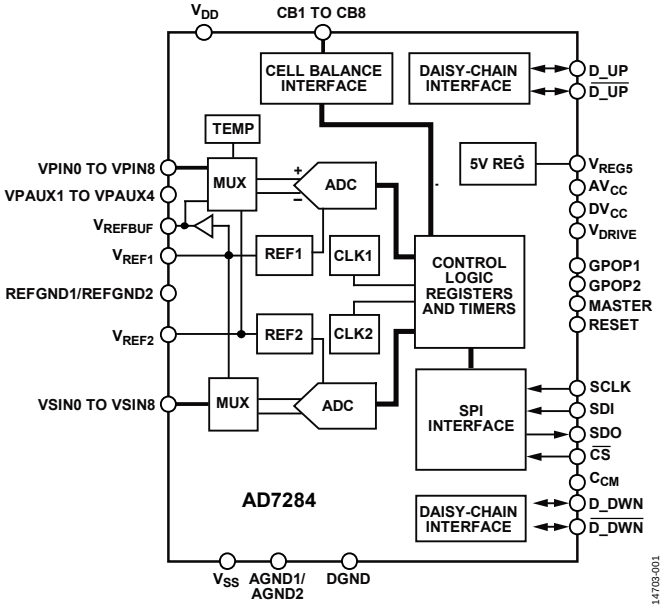

Figure 1.

GENERAL DESCRIPTION

The AD7284 contains all the functions required for the general-purpose monitoring of stacked Li-Ion batteries, as used in hybrid electric vehicles and battery backup applications.

The AD7284 has multiplexed cell voltage and auxiliary, analog-to-digital converter (ADC) measurement channels supporting four to eight cells of battery management. The device provides a maximum total unadjusted error, TUE, (cell voltage accuracy) of ±3 mV that includes all the internal errors from input to output. The primary ADC resolution is 14 bits.

The AD7284 also includes an integrated secondary measurement path that validates the data on the primary ADC. Other diagnostic features include the detection of open inputs, communication, and power supply related faults.

The AD7284 cell balancing interface outputs control the external field effect transistors (FETs) to allow discharging of individual cells.

There are two on-chip 2.5 V voltage references: one reference for the primary measurement path, and one for the secondary measurement path.

The AD7284 operates from one V_{DD} supply, ranging from 10 V to 40 V. The device provides eight differential analog input channels to accommodate large common-mode signals across the full V_{DD} range. Each channel allows an input signal range, VPINx − VPIN(x − 1) and VSINx − VSIN(x − 1), of 0 V to 5 V, where x = 0 to 8. The input pins assume a series stack of eight cells. The AD7284 includes four auxiliary ADC input channels that can be used for temperature measurement or system diagnostics.

The AD7284 has a differential daisy-chain interface that allows multiple devices to be stacked without the need for individual device isolation. By design, this interface allows both device to device communication within the same module and communication between devices on different modules.

Rev. C
Document Feedback

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4/2018—Rev. A to Rev. B

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5/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 10 V to 40 V, V_{SS} = 0 V, DV_{CC} = AV_{CC} = V_{REG5}, V_{DRIVE} = 3.0 V to 5.5 V, unless otherwise noted. T_J = −30°C to +120°C, where T_J is the junction temperature, unless otherwise noted. See the Thermal Data section for more details.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY ADC DC ACCURACY (VPIN0 to VPIN8)					
Resolution[1]	14			Bits	No missing codes, 305 µV/LSB
Integral Nonlinearity (INL)		±1.4		LSB	
Differential Nonlinearity (DNL)		±0.8		LSB	
ADC Unadjusted Error[1]		±1		mV	
TUE[2, 3]					
VPINx − VPIN(x − 1) Range					
2 V to 3.6 V		±1	±3	mV	10°C ≤ T_J ≤ 75°C
2 V to 4.3 V		±1	±5	mV	−10°C ≤ T_J ≤ +105°C
0 V to 5 V[1]		±1	±10	mV	7.5 V ≤ V_{DD} ≤ 40 V
PRIMARY ADC CELL VOLTAGE INPUTS (VPIN0 to VPIN8)					
Pseudo Differential Input Voltage Range					
VPINx − VPIN(x − 1)	0		5	V	
Static Leakage Current		±30	±100	nA	
Dynamic Leakage Current		±3		nA	Convert start command issued every 100 ms
Input Capacitance		15		pF	
PRIMARY ADC DC ACCURACY (VPAUX1 to VPAUX4)					
Resolution	14			Bits	No missing codes, 305 µV/LSB
INL[1]		±1.5		LSB	
DNL[1]		±0.8		LSB	
ADC Unadjusted Error[1]		±2		mV	
TUE[2]					
VPAUXx Range					
0 V to 2.5 V[1]		±2	±5	mV	−10°C ≤ T_J ≤ +105°C
0 V to 5 V[1]		±2	±10	mV	7.5 V ≤ V_{DD} ≤ 40 V
PRIMARY ADC AUXILIARY INPUTS (VPAUX1 to VPAUX4)					
Input Voltage Range[1]	0		5	V	
Static Leakage Current		±80	±100	nA	
Dynamic Leakage Current		±3		nA	Convert start command issued every 100 ms
Input Capacitance		15		pF	
PRIMARY ADC DC ACCURACY (VSTK[4])					
Resolution[1]	14			Bits	No missing codes, 4.88 mV/LSB
TUE[2]					
Battery Stack Voltage (VSTK) Range					
10 V to 28.8 V[1]		±16	±24	mV	10°C ≤ T_J ≤ 75°C
7.5 V to 40 V[1]		±16	±50	mV	
VSTK Voltage Accuracy					Relative to the sum of the cells
VSTK Range					
10 V to 28.8 V[1]		±2	±15	mV	10°C ≤ T_J ≤ 75°C
7.5 V to 40 V[1]		±2	±30	mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SECONDARY ADC DC ACCURACY (VSIN0 to VSIN8)					
Resolution	10			Bits	No missing codes, 4.88 mV/LSB
INL		±1		LSB	
DNL		±0.8		LSB	
TUE[2, 3]		±15	±25	mV	7.5 V ≤ V_{DD} ≤ 40 V
SECONDARY ADC CELL VOLTAGE INPUTS (VSIN0 to VSIN8)					
Pseudo Differential Input Voltage					
VSINx − VSIN(x − 1)	0		5	V	
Static Leakage Current		±5	±100	nA	
Dynamic Leakage Current		±3		nA	Convert start command issued every 100 ms
Input Capacitance		15		pF	
REFERENCE (V_{REF1}, V_{REF2})					
Reference Voltage		2.5		V	
Reference Temperature Coefficient		±3		ppm/°C	Included in the TUE specification
Output Voltage Hysteresis		160		ppm	
Long-Term Drift[5]		320		ppm/ 2000 hours	Primary reference
Turn On Settling Time		5		ms	C_{REF1} = 1 µF//100 nF, C_{REF2} = 1 µF//100 nF
REFERENCE BUFFER OUTPUT (V_{REFBUF})					
Output Voltage Accuracy	−4.5	±1	+4.5	mV	Relative to V_{REF1} output voltage
Output Current			1	mA	
Load Regulation		0.25		mV/mA	
Turn On Settling Time		5		ms	C_{REFBUF} = 1 µF
REGULATOR OUTPUT (V_{REG5})					
Output Voltage	4.8	5	5.2	V	
Output Current		2		mA	
Line Regulation		0.5		mV/V	
Load Regulation		0.5		mV/mA	
Internal Short-Circuit Protection Limit		30		mA	
CELL BALANCING OUTPUTS[6]					CB1 to CB8 output
Output Voltage					
High, V_{OH}	3.7	5	5.3	V	I_{SOURCE} = 20 µA
Low, V_{OL}		0	0.09	V	
Ramp-Up and Ramp-Down Time		100		µs	For a 80 pF load
INTERNAL TEMPERATURE SENSOR					Measures junction temperature
Accuracy[1]		±3		°C	−30°C ≤ T_J ≤ +120°C
Resolution		0.03125		°C/LSB	
LOGIC INPUTS (EXCEPT RESET)					
Input Voltage					
High, V_{INH}	V_{DRIVE} × 0.7			V	
Low, V_{INL}			V_{DRIVE} × 0.3	V	
Input Current, I_{IN}		10		µA	
Input Capacitance, C_{IN}		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output Voltage					
High, V_{OH}	V_{DRIVE} × 0.9			V	I_{SOURCE} = 200 µA
Low, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating State					
Leakage Current		1		µA	
Output Capacitance		5		pF	
RESET					
t_{RESET}	100			ns	Pulse width to reset or wake up the AD7284 (V_{DRIVE} high)
Leakage Current		60		µA	
POWER REQUIREMENTS					
V_{DD} Operating Range	10		40	V	
Current Consumption on the V_{DD} Pin (I_{DD})					Applies to master and slave configurations
I_{DD} During Conversion	14	15	17	mA	
I_{DD} During Conversion Data Readback	15	16.5	18	mA	Continuous readback
I_{DD} During Cell Balancing	13	14	16	mA	
		13	14	mA	Device in partial power-down
I_{DD} Idle	12	14	15	mA	To support transformer-based communications
I_{DD} Partial Power-Down Mode	11	12	14	mA	
I_{DD} Full Power-Down Mode	22	30	40	µA	
I_{DD} Matching Current		100		µA	Similar supply and temperature conditions across devices
TXIBAL	−3.9	−4.5	−4.9	mA	Bit D6 in Control Register 2
IDIODE	−0.39	−0.35	−0.32	mA	Bit D5 in Control Register 2
RXIBAL		0.12	0.56	mA	Bit D4 in Control Register 2
IMASTER	−3.5	−4.0	−4.5	mA	Bit D3 in Control Register 2
Master Configuration Only					
V_{DRIVE}	3.0		5.5	V	Typically 3.3 V or 5 V
V_{DRIVE} Threshold		0.8		V	To wake up the master device
I_{DRIVE}		15		µA	

[1] Guaranteed by design and/or characterization.
[2] TUE includes the INL of the ADC, the gain and offset errors of the input channels, as well as the reference error; that is, the difference between the ideal and actual reference voltage and the temperature coefficient of the reference.
[3] These specifications assume that all cells are in the same input voltage range, for example, VPINx – VPIN(x – 1) range = 2 V to 3.6 V.
[4] VSTK, the battery stack voltage, is scaled down internally by a factor of 16 before being applied to the ADC for measurement.
[5] Data generated from high temperature operating life (HTOL) reliability testing.
[6] For CB1 to CB5, the CBx output can be set to 0 V to 5 V with respect to the negative terminal of the cell being balanced. For CB6 to CB8, the CBx output can be set to 0 V to −5 V with respect to the positive terminal of the cell being balanced.

ADC TIMING SPECIFICATIONS

Table 2. ADC Timing for Three Devices in a Chain

Parameter[1]	Min	Typ	Max	Unit	Description
t_{CONV}		1040		ns	ADC conversion time
t_{ACQ}		400		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 00
		800		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 01
		1600		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 10
		3200		ns	ADC acquisition time, Bits[D1:D0] of Control Register 2 set to 11
t_{START}	32	33.6	35	µs	Delay from rising edge of $\overline{CS}$ (conversion command issued) to the first conversion
t_{DELAY}		100		ns	Propagation delay between two devices in the daisy chain

[1] All input signals are specified with $t_{RISE} = t_{FALL} = 5$ ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.

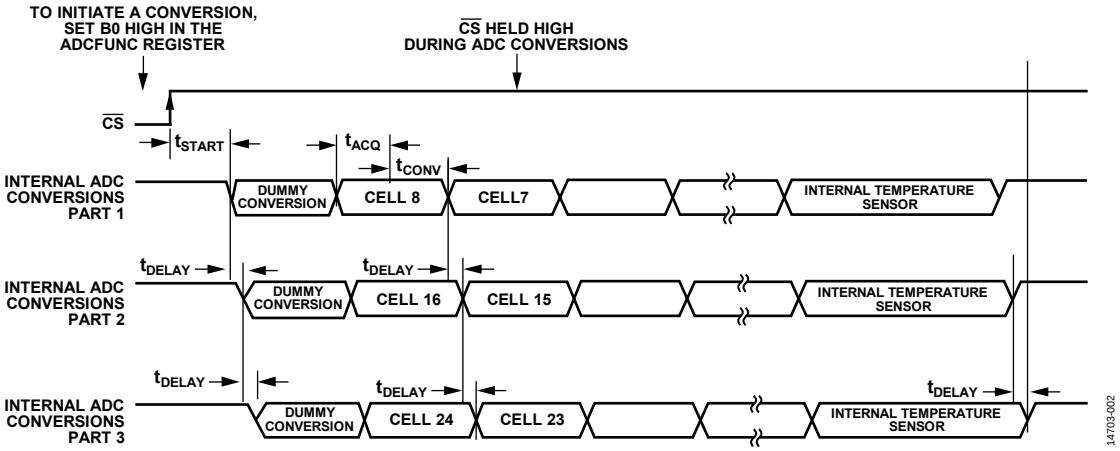


Figure 2. ADC Timing Diagram for Three Devices in a Chain

SERIAL PERIPHERAL INTERFACE (SPI) TIMING SPECIFICATIONS

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Description
f_{SCLK}		500		kHz	Frequency of the serial read clock on the SCLK pin for write and read registers
		725[2]		kHz	Frequency of the serial read clock on the SCLK pin for write registers only
		725[2]		kHz	Frequency of the serial read clock on the SCLK pin for read conversion data on slave devices
t_1	200			ns	$\overline{CS}$ falling edge to SCLK rising edge
t_2[3]			20	ns	Delay from $\overline{CS}$ falling edge to SDO active
t_3	10			ns	SDI setup time prior to SCLK falling edge
t_4	10			ns	SDI hold time after SCLK falling edge
t_5[4]			40	ns	Data access time after SCLK rising edge
t_6	20			ns	SCLK to data valid hold time
t_7	$0.5 \times t_{SCLK}$			ns	SCLK high pulse width
t_8	$0.5 \times t_{SCLK}$			ns	SCLK low pulse width
t_9	100			ns	$\overline{CS}$ rising edge to SCLK rising edge
t_{10}[5]			10	ns	$\overline{CS}$ rising edge to SDO high impedance
t_{11}	400			ns	$\overline{CS}$ high time
t_{12}		1.5		ns	Time from falling edge of last SCLK to rising edge of $\overline{CS}$

[1] All input signals are specified with $t_{RISE} = t_{FALL}$ = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications given are with a 25 pF load capacitance.
[2] Setting Bit D26 of the register address (see the Register Address section and Table 10) to 1 allows SCLK to increase to 725 kHz, as described in the Register Write and Register Read Operations section.
[3] Guaranteed by design and/or characterization.
[4] Time required for the output to cross 0.4 V or 2.4 V.
[5] t_{10} applies when using a continuous SCLK signal. Guaranteed by design.

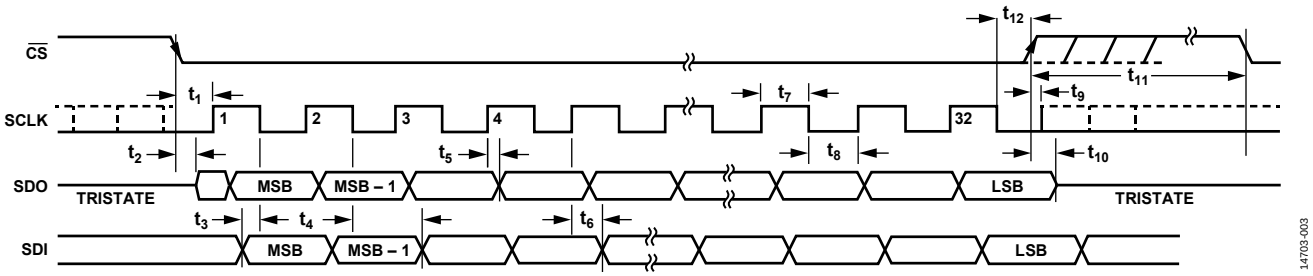


Figure 3. SPI Timing Diagram for a 32-Bit $\overline{CS}$ Frame

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are defined with respect to the normal operating specifications and not to other maximum rating specifications. The mnemonics listed in the rating column refer to the values as defined in the Specifications section only.

Table 4.

Parameter	Rating
V_{DD}	V_{SS}[1] − 0.3 V to V_{SS} + 48 V
MASTER	V_{SS} − 0.3 V to V_{DD} + 0.3 V
V_{DRIVE}, V_{REG5}[2]	V_{SS} − 0.3 V to V_{SS} + 6 V
ADCGND1 to ADCGND2 to V_{SS}	−0.3 V to +0.3 V
VPIN0, VSIN0	V_{SS} − 0.3 V to V_{SS} + 0.3 V
VPIN1 to VPIN7, VSIN1 to VSIN7	V_{SS} −0.3 V to V_{DD} + 0.3 V
VPIN8, VSIN8	V_{DD} −0.3 V to V_{DD} +1 V
Pseudo Differential Input Voltage[3]	
VPINx − VPIN(x − 1)	−0.3 V to +6 V
VPAUX1 to VPAUX4	V_{SS} − 0.3 V to V_{REG5} + 0.3 V
CB1	V_{SS} − 0.3 V to V_{REG5} + 0.3 V
CB2 to CB7	V_{SS} to V_{DD}
CB8	V_{DD} − 6 V to V_{DD}
Relative Input/Output Voltages	
CBx − VPINx − 1, x = 2 to 5	−0.3 V to +6 V
CBx − VPINx, x = 6 to 8	−6 V to +0.3 V
D_UP, $\overline{\text{D\_UP}}$	V_{SS} − 0.3 V to V_{DD} + 7 V
D_DWN, $\overline{\text{D\_DWN}}$	V_{SS} − 0.3 V to V_{REG5} + 0.3 V
Digital Input Voltage	V_{SS} − 0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage	V_{SS} − 0.3 V to V_{DRIVE} + 0.3 V
Analog Outputs (V_{REF1}, V_{REFBUF}, C_{CM})	V_{SS} − 0.3 V to V_{REG5} +0.3 V
ESD Human Body Model (HBM) Rating	
ANSI/ESDA/JEDEC JS-001-2010 (Standard HBM), All Pins	2.5 kV
Operating Junction Temperature Range	−40°C to +120°C
Absolute Maximum Junction Temperature	150°C
Storage Temperature	150°C
Reflow Profile	J-STD 20 (JEDEC)

[1] V_{SS}, DGND, AGND1, AGND2, REFGND1, and REFGND2 are internally shorted on chip and must be connected together on the printed circuit board (PCB). See the pin descriptions of these pins in the Pin Configuration and Function Descriptions section for additional information.
[2] V_{REG5}, AV_{CC}, and DV_{CC} are internally shorted on chip and must be connected together on the PCB. See the pin descriptions of these pins in the Pin Configuration and Function Descriptions section for additional information.
[3] Applies to primary and secondary analog voltage inputs; x = 1 to 8.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The IPC 2221 industrial standard recommends the use of conformal coating on high voltage pins.

THERMAL DATA

The junction temperature (T_J) refers to the temperature of the silicon die within the package of the device when the device is powered. The AD7284 parameters are specified over a junction temperature range of −30°C to +120°C.

The absolute maximum junction temperature of the AD7284 is 150°C. The AD7284 may be damaged when the junction temperature limit is exceeded. Monitoring of the junction temperature, or the ambient temperature in conjunction with an accurate thermal model, guarantees that T_J is within the specified temperature limits.

Measure the junction temperature using the internal temperature sensor.

Use the junction temperature (T_J) and the power dissipation (P_D) to calculate the ambient temperature (T_A) by

$$T_A = T_J - (P_D \times \theta_{JA})$$

where θ_{JA} is the junction to ambient thermal resistance of the package.

THERMAL RESISTANCE

The AD7284 is in a 64-lead LQFP_EP package with an exposed pad. The exposed pad is added for thermal performance purposes.

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance[1]

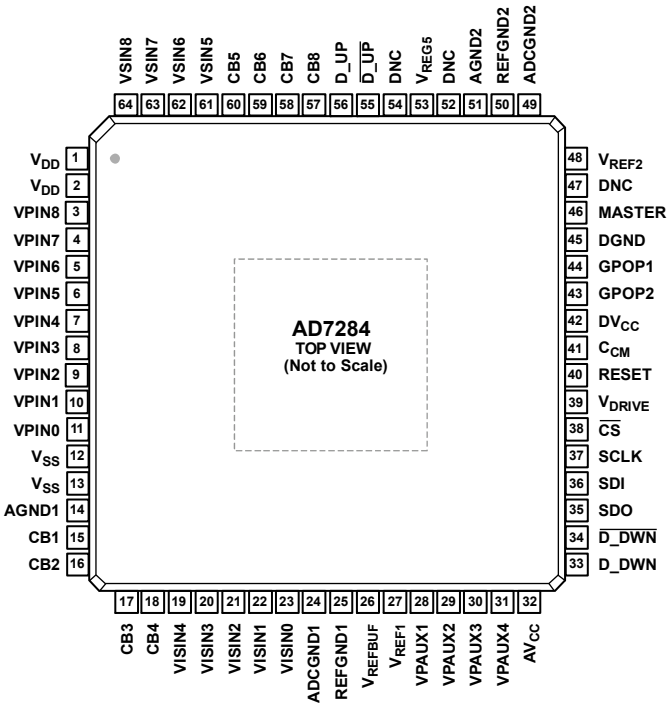
Package Type	θ_{JA}[2]	θ_{JC}[3]	Unit
SW-64-2	32	5	°C/W

[1] Thermal impedance values take into account the localized heat distribution on the die.
[2] Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 25 thermal vias. See the JEDEC51 standard.
[3] Estimated value based on measurements from similar packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
2. THE EXPOSED PAD IS PROVIDED FOR THERMAL PURPOSES AND MUST BE SOLDERED DOWN TO THE BOARD. THE EXPOSED PAD IS INTERNALLY CONNECTED TO V_{SS} ON THE DIE AND MUST BE CONNECTED TO THE V_{SS} PIN OF THE DEVICE ON THE PCB.

14703-004

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	V_{DD}	Positive Power Supply Voltage. These pins are connected to the top of the battery stack. Place 4.6 µF to 4.8 µF decoupling capacitors on the V_{DD} pins. It is also recommended that a current limiting resistor be connected between V_{DD} and the top of the stack.
3 to 11	VPIN8 to VPIN0	Primary Analog Voltage Inputs for Monitoring Up to Eight Cells. Connect VPIN0 to the base of the series of the connected battery cells and, therefore, to the bottom of Cell 1. Connect VPIN1 to the top of Cell 1, connect VPIN2 to the top of Cell 2, and so on.
12, 13	V_{SS}	Negative Power Supply Voltage. These pins are connected to the bottom of the battery stack. These inputs must be at the same potential as all the analog and digital grounds of the device.
14, 51	AGND1, AGND2	Analog Ground Pins. These pins are the ground reference point for most of the analog circuitry on the AD7284. These inputs must be at the same potential as V_{SS}.
15 to 18, 57 to 60	CB1 to CB8	Cell Balance Outputs for Balancing Up to Eight Cells. These pins provide a voltage output that can supply the gate drive of an external cell balancing transistor. The CB1 to CB5 outputs provide a 0 V to 5 V voltage output referenced to the absolute voltage of the negative terminal of the battery cell that is being balanced. The CB6 to CB8 outputs provide a 0 V to −5 V voltage output referenced to the absolute voltage of the positive terminal of the battery cell that is being balanced.
19 to 23,61 to 64	VSIN0 to VSIN8	Secondary Analog Voltage Inputs for Monitoring Up to Eight Cells. These pins can connect directly to the corresponding primary analog voltage inputs, or they can connect separately to the battery cells. If connected separately to the battery cells, connect VSIN0 to the base of the series connected battery cells and, therefore, to the bottom of Cell 1. Connect VSIN1 to the top of Cell 1, connect VSIN2 to the top of Cell 2, and so on.
24, 49	ADCGND1, ADCGND2	Analog Grounds for the Primary and Secondary ADCs. These pins must be at the same potential as V_{SS}.
25, 50	REFGND1, REFGND2	Reference Grounds. These pins are the ground reference points for the primary and secondary internal band gap references. These pins must be at the same potential as V_{SS}.
26	V_{REFBUF}	2.5 V Reference Buffer Output Voltage. A 1 µF decoupling capacitor connected to REFGND1 is recommended on this pin.

Pin No.	Mnemonic	Description
27	V_{REF1}	2.5 V Primary Reference Output Voltage. A 1 µF capacitor in parallel with a 100 nF decoupling capacitor connected to REFGND1 is recommended on this pin. V_{REF1} can be driven from an external reference, but it must not be used to drive any other circuit.
28 to 31	VPAUX1 to VPAUX4	Primary Auxiliary ADC Inputs (0 V to 5 V, Single-Ended). If any of these inputs are not required in the application, it is recommended that these pins be connected to V_{REG5} or V_{SS} through a 10 kΩ resistor.
32	AV_{CC}	Analog Supply Voltage. Decouple this supply pin to AGND1 with a 100 nF decoupling capacitor and connect this pin to the V_{REG5} output pin.
33, 34	$\overline{D\_DWN}$, D_DWN	Daisy-Chain Lower Interface Ports. On slave devices, terminate these pins with a 50 Ω resistor connected to the C_{CM} pin. These pins are connected to the D_UP and $\overline{D\_UP}$ pins on the AD7284 device below it in the daisy chain. On a master device, these pins are not used; connect these pins to V_{SS} via a 1 kΩ resistor instead.
35	SDO	Serial Data Output When Master Device. On a slave AD7284 device, this pin is not used and can be left unconnected.
36	SDI	Serial Data Input When Master Device. On a slave AD7284 device, this pin is not used and can be pulled low to DGND via a 1 kΩ resistor.
37	SCLK	Serial Clock Input When Master Device. On a slave AD7284 device, this pin is not used and can be pulled low to DGND via a 1 kΩ resistor.
38	$\overline{CS}$	Chip Select Input When Master Device. On a slave AD7284 device, this input is not used and can be connected to V_{SS} via a 1 kΩ resistor.
39	V_{DRIVE}	Digital Input/Output Supply Input. On a master device, connect an external voltage supply to the V_{DRIVE} pin. The voltage supplied at this pin determines the voltage at which the SPI interface operates. Decouple this pin to DGND with a 100 nF decoupling capacitor. On a master device, pulling V_{DRIVE} low powers down the device unless an active power-down timer is running. After the expiration of the power-down timer, the device powers down. On a slave device, connect the V_{DRIVE} pin to V_{REG5}.
40	RESET	Digital Input. An active high signal causes the device to reset to the power-on state. This input is internally pulled down. When this input is not used, an external 1 kΩ pull-down resistor to DGND is recommended.
41	C_{CM}	Common-Mode Decoupling Capacitor Port. This pin supplies a 2 V level used for the daisy-chain common mode. A 1 µF decoupling capacitor to V_{SS} is required on this pin.
42	DV_{CC}	Digital Supply Voltage. Connect the DV_{CC} supply pin to the V_{REG5} output pin. Decouple this digital supply to DGND with a 100 nF decoupling capacitor.
43, 44	GPOP2, GPOP1	General-Purpose Outputs. These pins provide a voltage output level of 0 V for a low signal and a voltage output level of V_{DRIVE} for a high signal.
45	DGND	Digital Ground. This pin is the ground reference point for all digital circuitry on the AD7284. This pin must be at the same potential as V_{SS}.
46	MASTER	Voltage Input. When the AD7284 acts as a master, connect this pin to the V_{DD} supply pin through a 10 kΩ resistor. When the AD7284 acts as a slave, connect this pin to the V_{SS} supply pin of the same AD7284 device through a 10 kΩ resistor.
47, 52, 54	DNC	Do Not Connect. Do not connect to these pins.
48	V_{REF2}	2.5 V Secondary Reference Output Voltage. A 1 µF capacitor in parallel with a 100 nF decoupling capacitor to REFGND2 is recommended on this pin. V_{REF2} can not be driven externally and must not be used to drive any other circuit.
53	V_{REG5}	5 V Analog Voltage Output. The internally generated V_{REG5} voltage provides the supply voltage for the ADC core. A 100 nF decoupling capacitor to AGND2 is required on the V_{REG5} pin.
55, 56	$\overline{D\_UP}$, D_UP	Daisy-Chain Upper Interface Ports. Terminate these pins with a 50 Ω resistor connected to the V_{DD} pin directly for configurations using transformer isolation or via a capacitor when using the direct coupled configuration. The $\overline{D\_UP}$ pin is connected to the $\overline{D\_DWN}$ pin of the AD7284 device above it in the daisy chain, and the D_UP pin is connected to the D_DWN pin of the AD7284 device above it in the daisy chain.
	Exposed Pad	Exposed Pad. The exposed pad is provided for thermal purposes and must be soldered down to the board. The exposed pad is internally connected to V_{SS} on the die and must be connected to the V_{SS} pin of the device on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

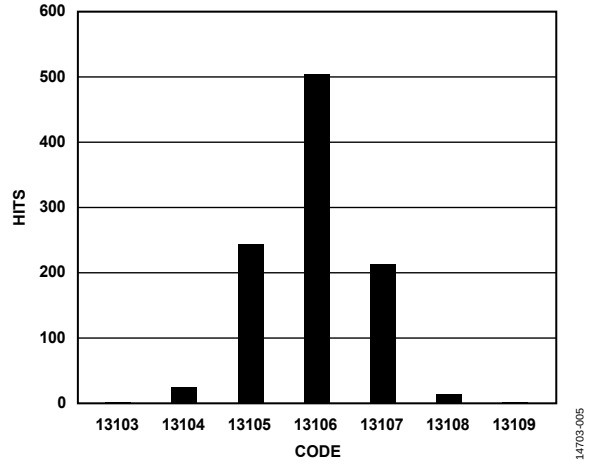


Figure 5. Typical Code Noise for VPIN1 Through VPIN8, V_{DD} = 32 V, T_J = 60°C

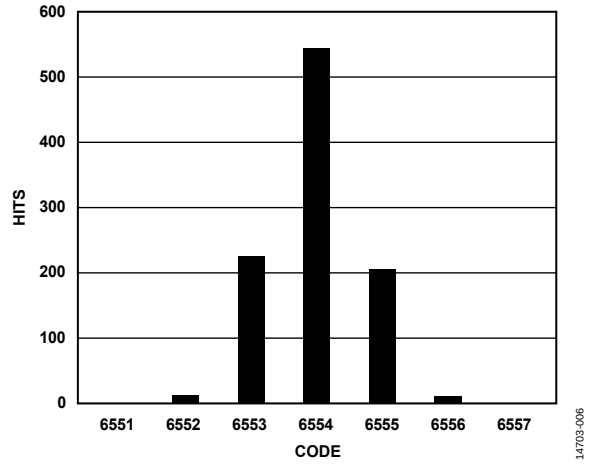


Figure 6. Typical Code Noise for VSTK, V_{DD} = 32 V, T_J = 60°C

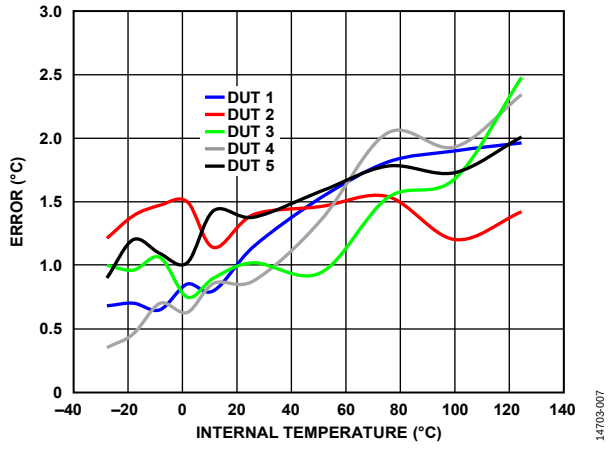


Figure 7. Error vs. Internal Temperature for Various Devices Under Test (DUT)

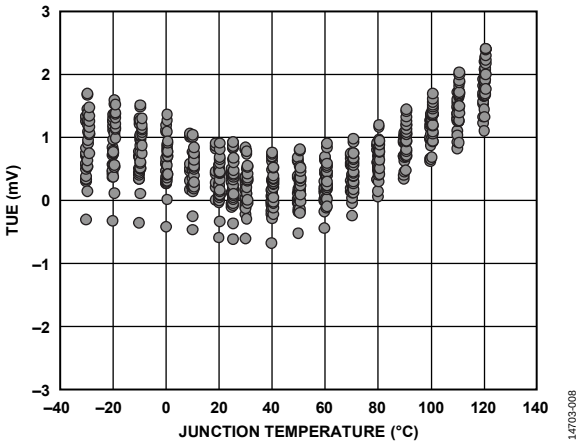


Figure 8. TUE vs. Junction Temperature, Preassembly, V_{DD} = 18 V

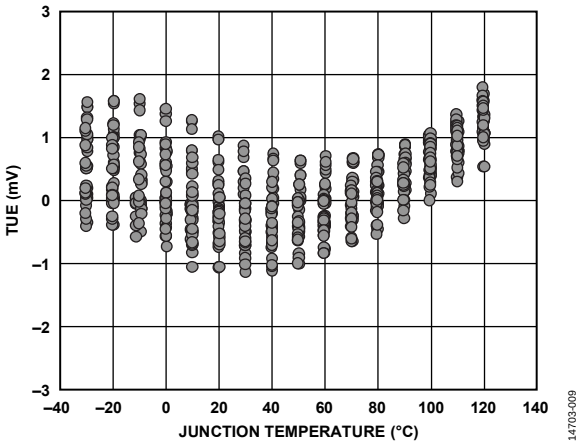


Figure 9. TUE vs. Junction Temperature, Postassembly, V_{DD} = 18 V

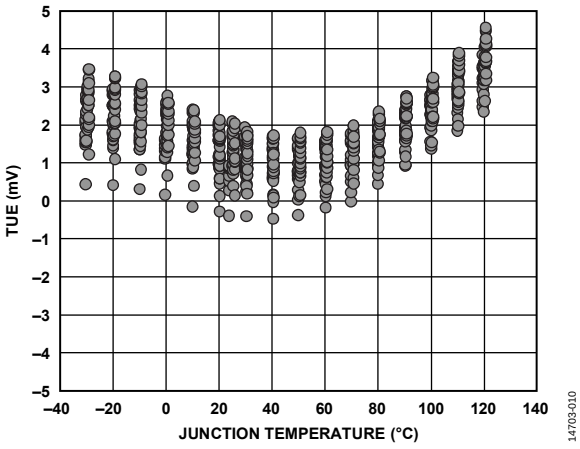


Figure 10. TUE vs. Junction Temperature, Preassembly, V_{DD} = 32 V

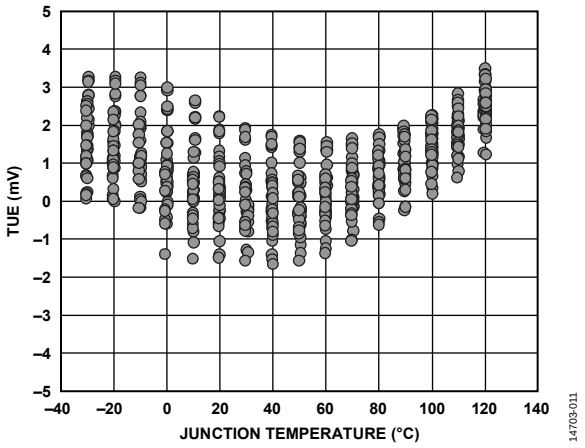


Figure 11. TUE vs. Junction Temperature, Postassembly, V_{DD} = 32 V

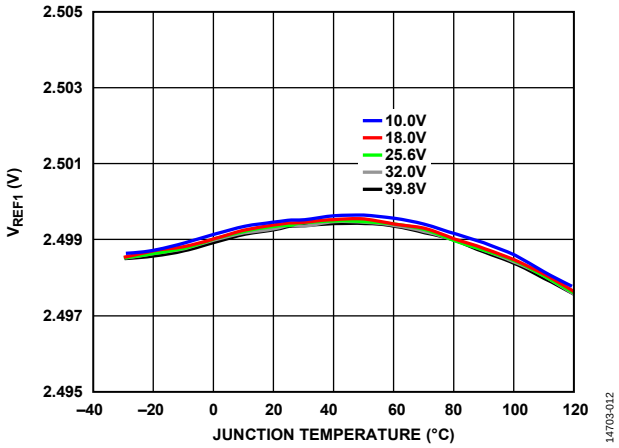


Figure 12. Preassembly Primary Voltage Reference, V_{REF1} vs. Junction Temperature

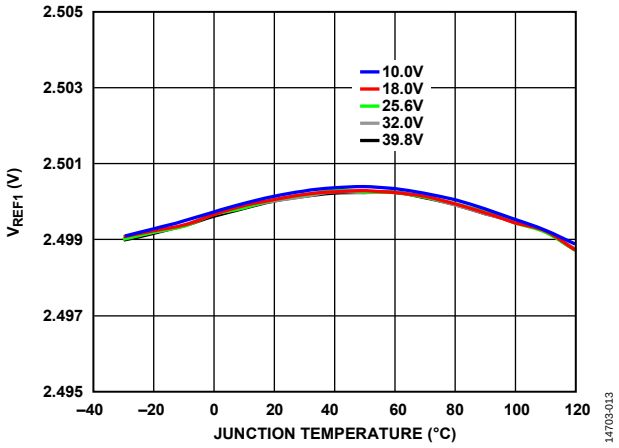


Figure 13. Postassembly Primary Voltage Reference, V_{REF1} vs. Junction Temperature

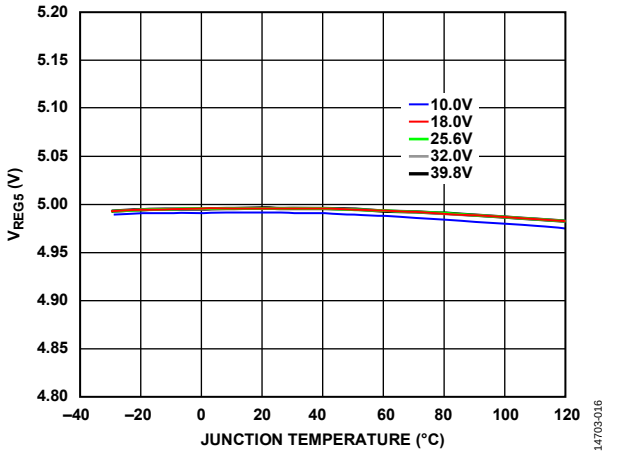


Figure 14. Preassembly 5 V Voltage Regulator Output (V_{REG5}) vs. Junction Temperature

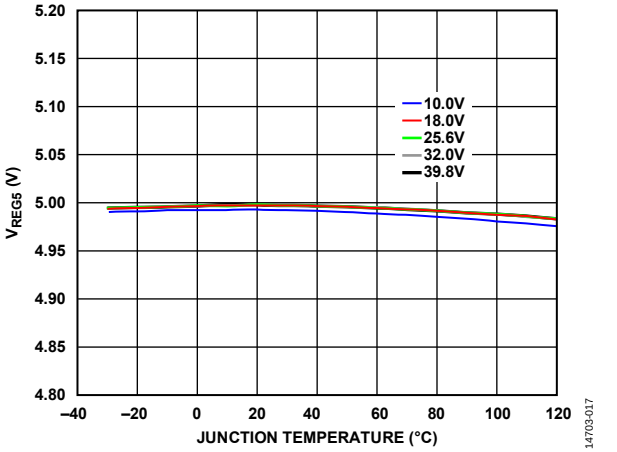


Figure 15. Postassembly 5 V Voltage Regulator Output (V_{REG5}) vs. Junction Temperature

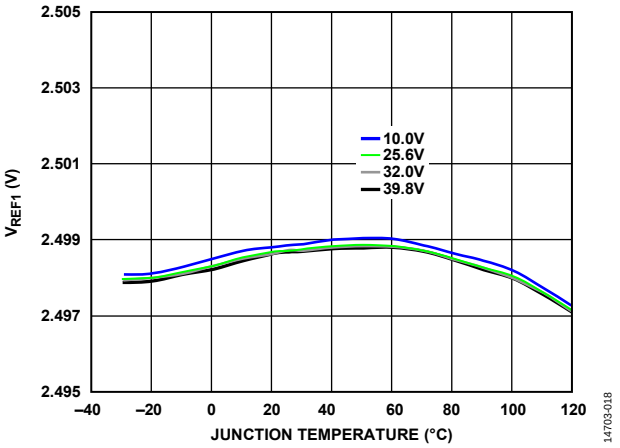


Figure 16. Preassembly Buffered Voltage Reference, V_{REF1} vs. Junction Temperature

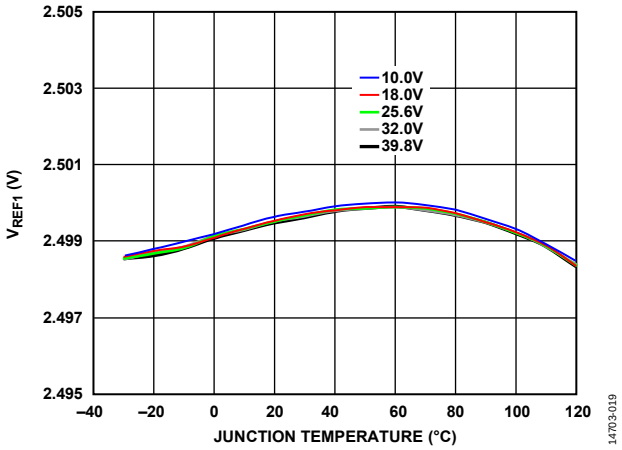


Figure 17. Postassembly Buffered Voltage Reference, V_{REF1} vs. Junction Temperature

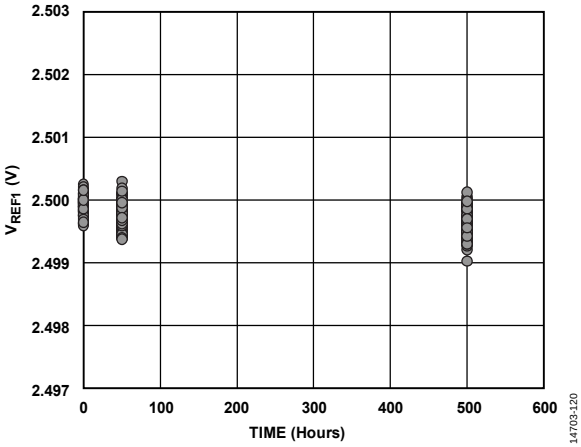


Figure 18. V_{REF1} vs. Time, 0 Hours to 500 Hours Accelerated Lifetime Drift (HTOL)

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Code Error
Offset code error applies to straight binary output coding. It is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal, that is, AGND + 1 LSB.

Gain Error
Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is $2 \times V_{REF1} - 1$ LSB) after adjusting for the offset error.

ADC Unadjusted Error
ADC unadjusted error includes INL errors, as well as offset and gain errors of the ADC and measurement channel.

Total Unadjusted Error (TUE)
TUE is the maximum deviation of the output code from the ideal. TUE includes INL errors, offset and gain errors, and reference errors. Reference errors include the difference between the actual and ideal reference voltage (that is, 2.5 V) and the reference voltage temperature coefficient.

Reference Voltage Temperature Coefficient
The reference voltage temperature coefficient (tempco) is derived from the maximum and minimum reference output voltage (V_{REF}) measured between T_{MIN} and T_{MAX}. It is expressed in ppm/°C using the following equation:

$$Tempco\ V_{REF}\ (\text{ppm/°C}) = \frac{V_{REF\ (MAX)} - V_{REF\ (MIN)}}{2.5\ \text{V} \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF\ (MAX)}$ is the maximum V_{REF} between T_{MIN} and T_{MAX}.
$V_{REF\ (MIN)}$ is the minimum V_{REF} between T_{MIN} and T_{MAX}.
T_{MAX} = 120°C.
T_{MIN} = −30°C.

Output Voltage Hysteresis
Output voltage hysteresis, or thermal hysteresis, is defined as the absolute maximum change of the reference output voltage after the device is cycled through temperature from either T_HYS+ or T_HYS−, where

T_HYS+ = 25°C to T_{MAX} to 25°C

T_HYS- = 25°C to T_{MIN} to 25°C

It is expressed in ppm using the following equation:

$$V_{HYS}\ (\text{ppm}) = \left| \frac{V_{REF_{(25°C)}} - V_{REF\ (T\_HYS)}}{V_{REF\ (25°C)}} \right| \times 10^6$$

where:
$V_{REF\ (25°C)}$ = V_{REF} at 25°C.
$V_{REF\ (T\_HYS)}$ is the maximum change of V_{REF} at T_HYS+ or T_HYS-.

Static Leakage Current
Static leakage current is the current that is measured on the cell voltage and/or the auxiliary ADC inputs when the device is static, that is, not converting.

Dynamic Leakage Current
Dynamic leakage current is the current measured on the cell voltage and/or the auxiliary ADC inputs, when converting, with the static leakage current subtracted. The dynamic leakage current is specified with a convert start command issued every 100 ms. Calculate the dynamic leakage current for a different conversion using the following equation:

$$I_{DYN\,(B)} = \left| \frac{I_{DYN\,(A)} \times f_{CNVST\,(B)}}{f_{CNVST\,(A)}} \right|$$

where:
$I_{DYN\,(B)}$ is the dynamic leakage at the desired convert start frequency, $f_{CNVST\,(B)}$.
$I_{DYN\,(A)}$ is the dynamic leakage at convert start frequency, $f_{CNVST\,(A)}$.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7284 is a Li-Ion battery monitoring device that can monitor eight series connected Li-Ion battery cells and four additional voltage inputs.

The AD7284 consists of a primary measurement path and a secondary measurement path, allowing the host microcontroller to perform a comparison of the two sets of acquired data.

Take the V_{DD} and V_{SS} supplies required by the AD7284 from the battery cells being monitored by the device. An internal V_{REG5} rail is generated to provide power for the internal AD7284 core.

The AD7284 includes two on-chip 2.5 V reference output voltages, V_{REF1} and V_{REF2}. Additionally, the V_{REFBUF} analog output voltage provides a buffered version of the V_{REF1} primary reference to allow the connection of external thermistors and to provide a ratiometric temperature measurement using the four primary auxiliary inputs, VPAUX1 to VPAUX4.

The primary measurement path consists of a voltage input multiplexer and a successive approximation register (SAR) ADC, providing 14 bits of resolution. The primary analog voltage inputs, VPIN0 to VPIN8, with a set of external filtering components, allow the individual voltage monitoring of eight cells, plus a stack voltage measurement. The primary auxiliary inputs, VPAUX1 to VPAUX4, can monitor temperatures or be used for external diagnostics. The primary measurement path also measures V_{REG5}, V_{REF2}, and the internal temperature sensor. The V_{REF2} measurement allows the host microcontroller to verify the operation of the primary measurement path.

The secondary measurement path consists of a voltage input multiplexer and a SAR ADC providing 10 bits of resolution. The secondary analog voltage inputs, VSIN0 to VSIN8, allow a second set of voltage measurements on the eight cells. The secondary analog voltage inputs can connect with a second set of external filtering components, or these inputs can connect directly to VPIN0 to VPIN8 on the primary measurement path to minimize the use of external components, if desired. The secondary measurement path also measures V_{REG5} and V_{REF1}. The V_{REF1} measurement allows the host microcontroller to verify the operation of the secondary measurement ADC.

The AD7284 provides eight outputs to control external transistors as part of a cell balancing circuit. The CB1 to CB5 outputs provide a 0 V to 5 V output voltage referenced to the absolute voltage of the negative terminal of the battery cell that is being balanced. The CB6 to CB8 outputs provide a 0 V to −5 V output voltage referenced to the absolute voltage of the positive terminal of the battery cell that is being balanced.

The AD7284 features a differential daisy-chain interface. A chain of AD7284 devices can monitor the cell voltages and temperatures of a larger number of cells, as shown in Figure 19. The conversion data from each AD7284 in the chain passes through the master device to the system controller via a single SPI interface. Control data can be similarly passed via the single SPI interface to the master AD7284 device and up the differential daisy-chain interface to each individual AD7284 device in the daisy chain.

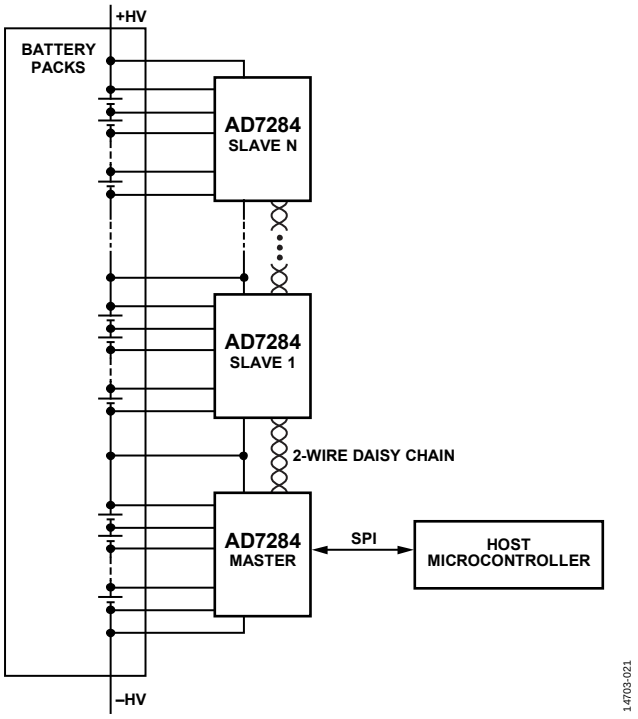


Figure 19. Simplified System Diagram with Multiple AD7284 Devices (Additional Circuitry Omitted for Clarity)

The AD7284 also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the AD7284 to interface to both the 3.3 V and the 5 V processors.

In the event of communication loss, a watchdog timer places the unresponsive devices in the chain into power-down mode.

CONVERTER OPERATION

The primary and secondary conversion paths of the AD7284 each consist of an input multiplexer and a SAR ADC.

Multiplexer Configuration

Each multiplexer selects a pair of analog inputs to convert: VPIN0 to VPIN8 for the primary path and VSIN0 to VSIN8 for the secondary path. The voltage of each individual cell is measured by converting the difference between the adjacent analog inputs, that is, VPIN1 − VPIN0, VPIN2 − VPIN1, and so on (see Figure 20 and Figure 21).

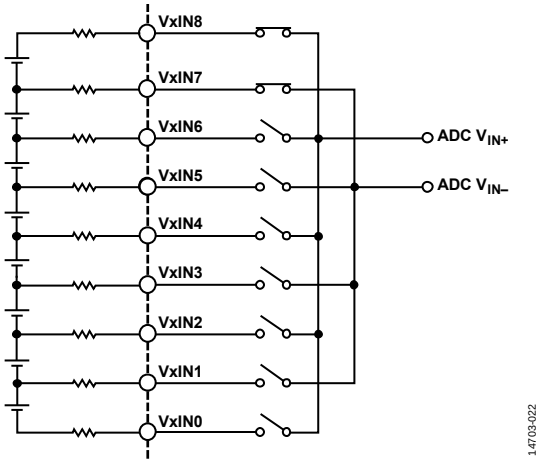


Figure 20. Multiplexer Configuration During VxIN8 to VxIN7 Sampling (Cell 8)

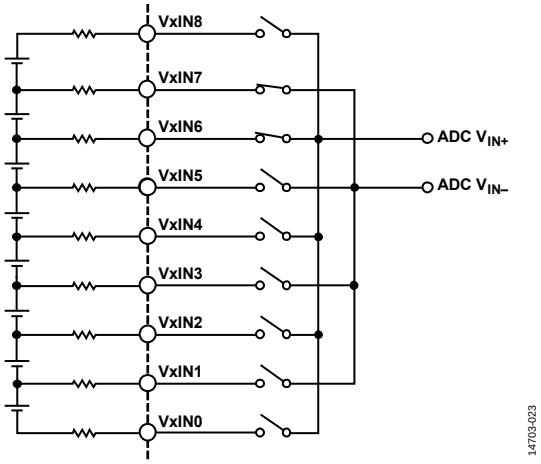


Figure 21. Multiplexer Configuration During VxIN7 to VxIN6 Sampling (Cell 7)

Converter Configurations

The two converters on the AD7284 are SAR ADCs. They are composed of a comparator, SAR control logic, and two capacitive digital-to-analog converters (DACs).

Figure 22 shows a simplified schematic of the SAR ADC. During the acquisition phase, the SW1, SW2, and SW3 switches are closed. The sampling capacitor array, C_S, acquires the signal on the input during this phase.

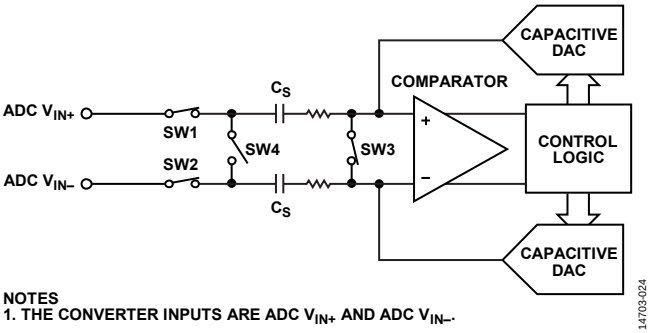


Figure 22. SAR ADC Configuration During the Acquisition Phase

When the ADC starts a conversion, SW1, SW2, and SW3 open, and SW4 closes, causing the comparator to become unbalanced (see Figure 23). The control logic and capacitive DACs add and subtract fixed amounts of charge to return the comparator to a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. This output code is then stored in the appropriate register for the converted input.

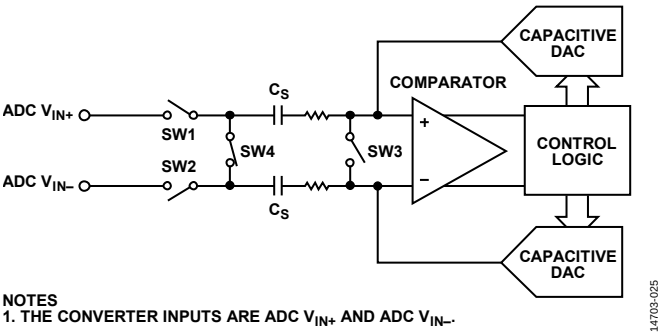


Figure 23. SAR ADC Configuration During the Conversion Phase

Transfer Function

The conversion data readback for each voltage measurement consists of 14 bits. The output coding of the AD7284 primary measurement path is in 14-bit, straight binary format. The output coding of the AD7284 secondary measurement path is in 10-bit, straight binary format. The result is inverted so that it is easily distinguished from the primary measurement and is preceded by four data bits set to 0000.

The LSB size is dependent on whether the primary measurement path or the secondary measurement is used. The analog input range of the voltage inputs is 0 V to 5 V. The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSBs, and so on). The ideal transfer characteristic is shown in Figure 24.

Table 7. LSB Size for the Analog Input Range

Measurement Path	Input Range	Full-Scale Range[1]	LSB Size
Primary	0 V to 5 V	5 V/16,384	305 µV
Secondary	0 V to 5 V	5 V/1,024	4.88 mV

[1] The 16,384 and 1,024 values in this column represent the number of codes available for each ADC.

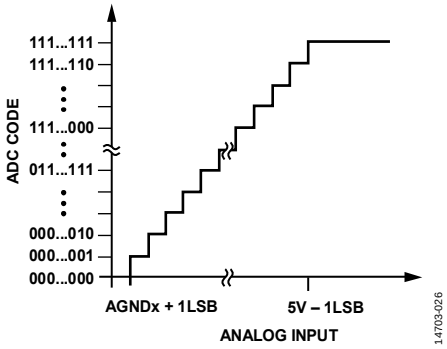


Figure 24. Ideal Transfer Characteristic

INTERNAL TEMPERATURE SENSOR

The AD7284 contains an on-chip temperature sensor. The temperature measurement updates with each conversion request and is provided as part of each conversion frame.

The temperature sensor measures the junction temperatures in the −30°C to +120°C range with a typical accuracy of ±3°C.

The output coding of the temperature sensor is twos complement, with a resolution of 32 LSB/°C. Code 0 corresponds to 25°C (junction temperature).

AUXILIARY ADC INPUTS

The AD7284 provides four single-ended analog inputs to the primary ADC, VPAUX1 to VPAUX4. The input voltage range is 0 V to 5 V with respect to V_{SS}. These inputs can convert other voltages within the system, such as converting the voltage output of a thermistor temperature measurement circuit.

VOLTAGE REFERENCES

The AD7284 contains two identical 1.2 V band gap voltage references. These references are internally buffered and gained to provide 2.5 V reference voltages to the primary (V_{REF1}) and secondary (V_{REF2}) ADCs, as shown in Figure 25.

The provision of two reference voltages is a diagnostic feature and enables validation of the behavior of the measurement paths and the references. For example, the secondary ADC measures the primary reference, V_{REF1}. Similarly, the primary ADC measures the secondary reference, V_{REF2}.

An external 2.5 V reference can overdrive the reference for the primary path, V_{REF1}. When an external reference is used, set Bit D4 of Control Register 1 to disable the V_{REF1} buffer. The secondary measurement path measures the external reference in this case.

The primary reference is further buffered and provided as a reference output, V_{REFBUF}, to bias external thermistors. This buffer is capable of driving currents up to 1 mA, allowing the user to connect up to four 10 kΩ thermistor circuits in parallel. The primary conversion includes a measure of this voltage level.

Decouple the V_{REFBUF} pin to ADCGND1 using a 1 µF capacitor. Decouple the V_{REF1} pin to ADCGND1 using a 1 µF capacitor with a 100 nF capacitor in parallel. Decouple the V_{REF2} pin to ADCGND2 using a 1 µF capacitor with 100 nF capacitor in parallel.

Larger decoupling capacitors can be used to decouple V_{REF1} and V_{REF2}; however, this results in the reference taking longer to power up. The turn on settling time is typically 5 ms with the recommended decoupling capacitor values.

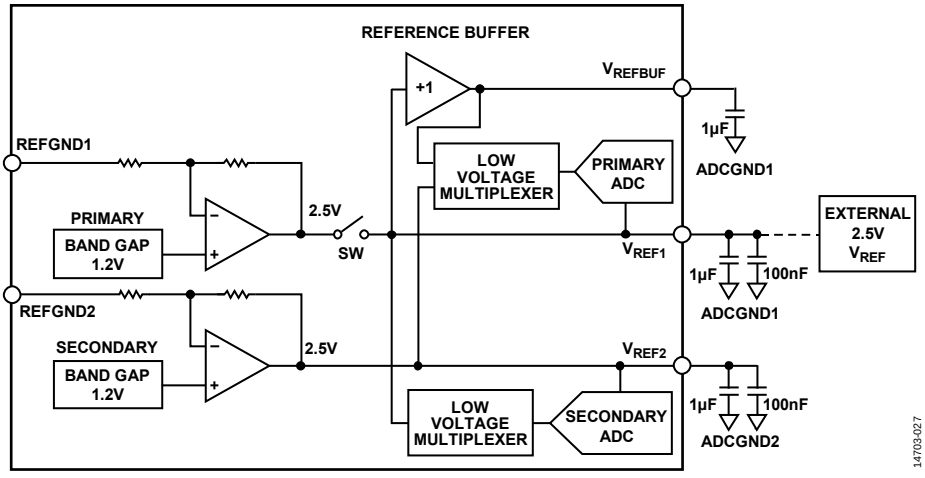


Figure 25. Internal References and Optional External Reference

CELL CONNECTIONS

The AD7284 can monitor four to eight battery cells connected in series.

Typical Eight Cell Configuration

Figure 26 shows the typical connections to the AD7284 supply and cell monitoring inputs in an eight cell configuration.

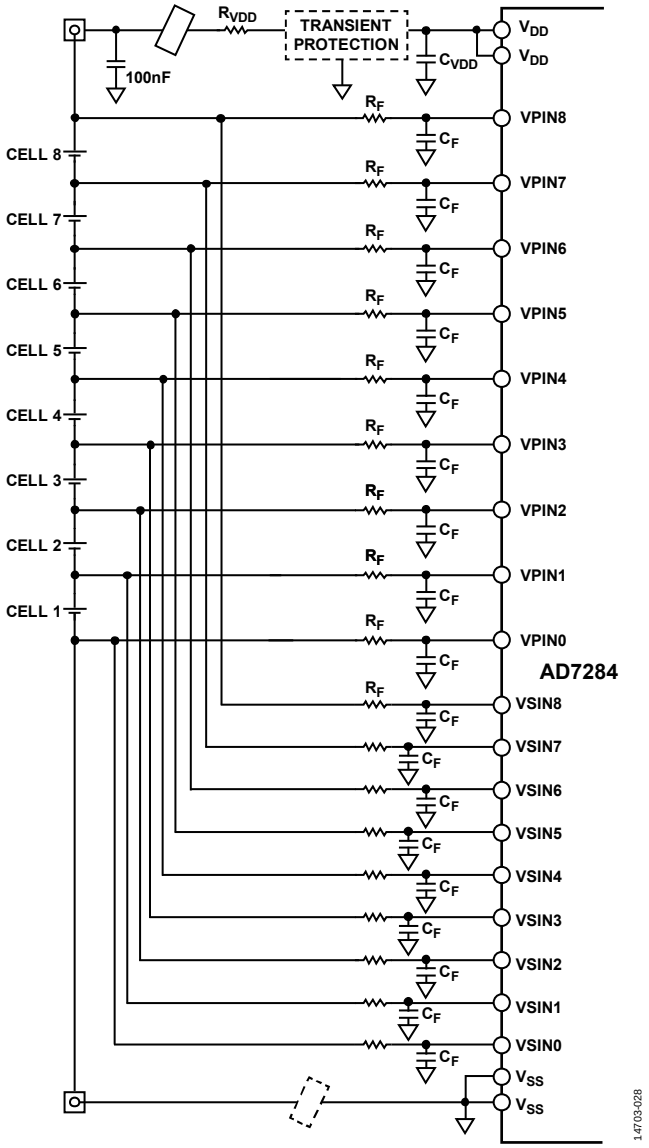


Figure 26. Typical Cells and Supply Connections (Additional Circuitry Omitted for Clarity)

A series resistor, R_{VDD} (10 Ω to 40 Ω), is recommended from the top of the battery into the V_{DD} supply pins. The total decoupling capacitors on the supply pins, C_{VDD}, must be 4.7 µF.

The analog voltage inputs must be filtered externally with a single-ended low-pass filter approach. The resistors, R_F, in series with the VPIN0 to VPIN8 and VSIN0 to VSIN8 inputs provide protection for the analog inputs in the event of an overvoltage or undervoltage condition on those inputs (for example, if any of the cell voltage inputs are incorrectly shorted to V_{DD} or V_{SS}). The resistors also provide protection during the initial connection of the daisy chain of AD7284 devices to the battery stack. The C_F capacitors, in conjunction with the R_F resistors, act as a low-pass filter. C_F capacitor values between 100 nF and 1 µF are recommended. The cutoff frequency of the low-pass filter when using an R_F of 1 kΩ and a C_F capacitor of 1 µF is 160 Hz. The cutoff frequency of the low-pass filter when using a C_F capacitor of 100 nF is 1600 Hz.

The time constant of the R_F and C_F filters on the primary and secondary paths must match the time constant on the V_{DD} pins fairly closely (for example, 100 nF (C_F) and 1 kΩ (R_F) on the inputs, and 4.7 µF (C_{VDD}) and 20 Ω (R_{VDD}) on V_{DD}).

Connection to Fewer Voltage Cells

While the AD7284 provides eight input channels for battery cell voltage measurement, it can also be used in applications that require fewer than eight cell voltage measurements. When used in this manner, ensure that the sum of the individual cell voltages still exceeds the minimum V_{DD} supply voltage (10 V).

The minimum number of cells connected to each AD7284 is four. Figure 27 shows the recommended connections to monitor four cells. The unused inputs are connected together and connected between Cell 2 and Cell 3 via a resistor. The resistor minimizes the leakage from the unused inputs.

Irrespective of how many cells are connected, the AD7284 acquires and converts all eight voltages. All conversion results are available for readback; results of the unused voltage channels are zero.

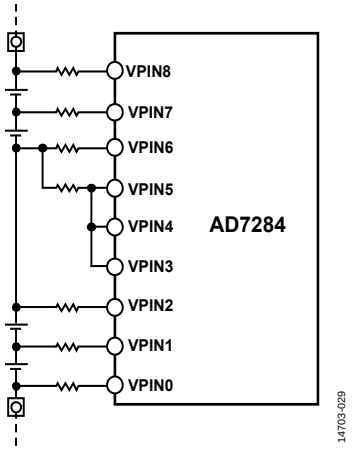


Figure 27. Typical Connection with Minimum Cells Connected (Additional Circuitry Omitted for Clarity)

Connection of Unused Secondary Channel Inputs

In applications where the secondary path is not used, connect the VSINx pins directly to the corresponding VPINx pins.

By default, the two ADCs convert simultaneously. To minimize the discharge of the C_F capacitor during the acquisition phase, enable the delay mode between conversions. The ADC delay mode is controlled by Control Register 3, Bit 6.

Acquisition Time

The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. This, in turn, depends on the input impedance and any external components placed on the analog inputs. The default acquisition time of the AD7284 on initial power-up is 400 ns. To accommodate the use of alternative input filter configurations, the acquisition time can be set to 400 ns, 800 ns, 1600 ns, or 3200 ns using Bits[D1:D0] in Control Register 2 (see Table 22).

Calculate the minimum acquisition time required, t_{ACQ}, by

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R) \times C)$$

where:
R_{SOURCE} includes any extra source impedance on the analog input between the external capacitors and the input pins. It does not include any extra source impedance, for example, the 1 kΩ series resistors, which are between the battery cells and the external capacitors.
R is the internal switch and path resistance, typically 620 Ω.
C is the sampling capacitance, typically 15 pF.

ADC CONVERSIONS SEQUENCE

Upon completion of a conversion sequence, the primary and secondary path measurements are available for read back. The primary path measurements must be read first. Reading the secondary path measurements is optional.

The primary path consists of 18 measurements available in the following order:

1. Cell Voltage 1 to Cell Voltage 8.
2. Stack voltage scaled down by 16.
3. Secondary path reference voltage.
4. V_{REG5} voltage scaled by 2/3.
5. Primary Auxiliary Input 1 to Primary Auxiliary Input 4.
6. Reference buffer output voltage.
7. Repeated V_{REG5} voltage scaled by 2/3.
8. Internal temperature sensor.

All 18 measurements must be read back on each device as described in the Conversion Data Readback section.

The secondary path consists of 10 measurements available in the following order:

1. Cell Voltage 1 to Cell Voltage 8.
2. Primary path reference voltage.
3. V_{REG5} voltage scaled by 4/5.

To read back one measurement from the secondary path, all 10 measurements must be read back for each device (see the Conversion Data Readback section).

The results are read back via the 4-wire SPI.

Internal Voltage Measurements

Table 8 and Table 9 show the range of the expected measured reference values that are returned on each measurement cycle. Detecting one of these values outside of the indicated range indicates a fault condition.

Table 8. Primary Internal Voltage Measurement

Parameter	Min	Max	Unit	Register
V_{REF2}	2.485	2.515	V	0x12
$V_{REG5} \times 2/3$	3.200	3.421	V	0x13
V_{REFBUF}	2.486	2.514	V	0x1C
$V_{REG5} \times 2/3$	3.200	3.421	V	0x1D

Table 9. Secondary Internal Voltage Measurement

Parameter	Min	Max	Unit	Register
V_{REF1}	2.475	2.525	V	0x31
$V_{REG5} \times 4/5$	3.865	4.135	V	0x34

CONVERTING WITH A SINGLE AD7284

Conversions are initiated on the AD7284 by setting Bit D0 high in the ADC functional control register. A single conversion command initiates conversions on all channels of the AD7284. The conversions on the primary measurement path and the secondary measurement path occur in parallel, as shown in Figure 28. As described in the Converter Operation section, the voltage of each individual battery cell is measured by converting the difference between the adjacent analog inputs. The first conversion starts t_{START} after the conversion start command. This conversion is a dummy conversion that has the same timing as a normal conversion and provides additional acquisition time for the first cell conversion. The first cell converted is Cell 8 (VPIN8 − VPIN7), then Cell 7 (VPIN7 − VPIN6), and so on, as shown in Figure 28.

Calculate the conversion time per channel by

$$Conversion\ Time\ per\ Channel = t_{ACQ} + t_{CONV}$$

Similarly, calculate the conversion time for eight cell voltages by

$$Conversion\ Time\ per\ Eight\ Primary\ Cells = (t_{ACQ} + t_{CONV}) \times 9$$

where the 9th conversion is the dummy conversion.

The device conversion time includes the internal temperature sensor channel, which requires a longer acquisition and conversion time (typically 276 µs). Therefore, calculate the conversion time per device by

$$Conversion\ Time\ per\ Device = t_{START} + ((t_{ACQ} + t_{CONV}) \times 18) + 276\ \mu s$$

where:

t_{START} is the time between the rising edge of $\overline{CS}$ to the dummy conversion. See Table 2.
t_{ACQ} is the analog input acquisition time. See Table 2.
t_{CONV} is the conversion time. See Table 2.
Factor 18 is the one dummy conversion plus seventeen measurements.

With an acquisition time set to 400 ns, the conversion time per device is typically 336 µs.

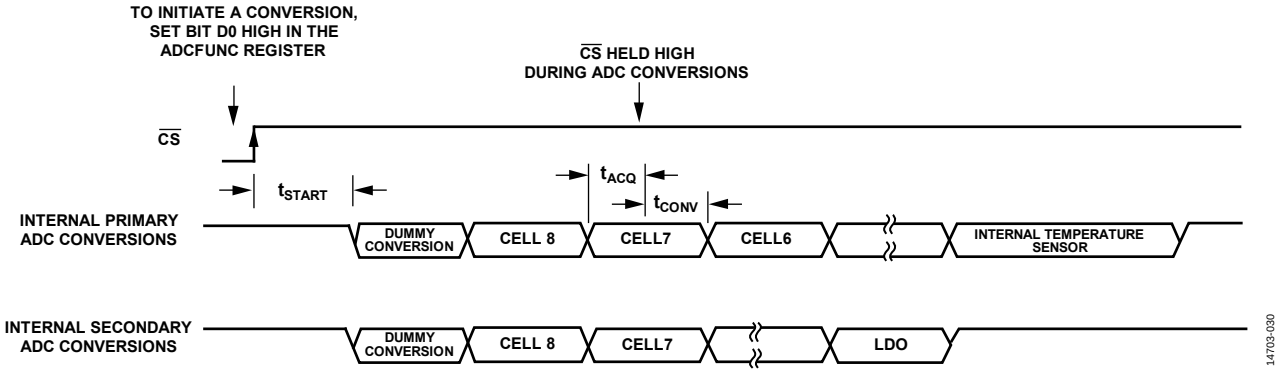


Figure 28. ADC Conversions with a Single Device

CONVERTING WITH A CHAIN OF AD7284 DEVICES

The AD7284 provides a daisy-chain interface that allows up to 30 AD7284 devices to stack. One feature of the daisy-chain interface is the ability to initiate conversions on all devices in the daisy-chain stack with a single convert start command. The convert start command transfers up the daisy chain from the master device to each AD7284 in turn. The delay time between each AD7284 is t_{DELAY}, as shown in Figure 29. Note that this diagram is simplified to show the primary measurement path only.

Calculate the total conversion time for all channels by

Total Conversion Time = (Conversion Time per Device) + ((N − 1) × t_{DELAY})

where:
N is the number of AD7284 devices in the daisy chain.
t_{DELAY} is the delay time when transferring the convert start command between adjacent AD7284 devices, as specified in Table 2.

The latency across all cells is the delay between the start of converting the first cell and the start of converting on the last cell of a battery stack, as shown in Figure 30. Calculate this latency by

Latency Across All Cells = (*Conversion Time of Seven Cells*) + ((*N* − 1) × t_{DELAY})

With an acquisition time set to 400 ns, the latency across 96 cells is typically 13 µs.

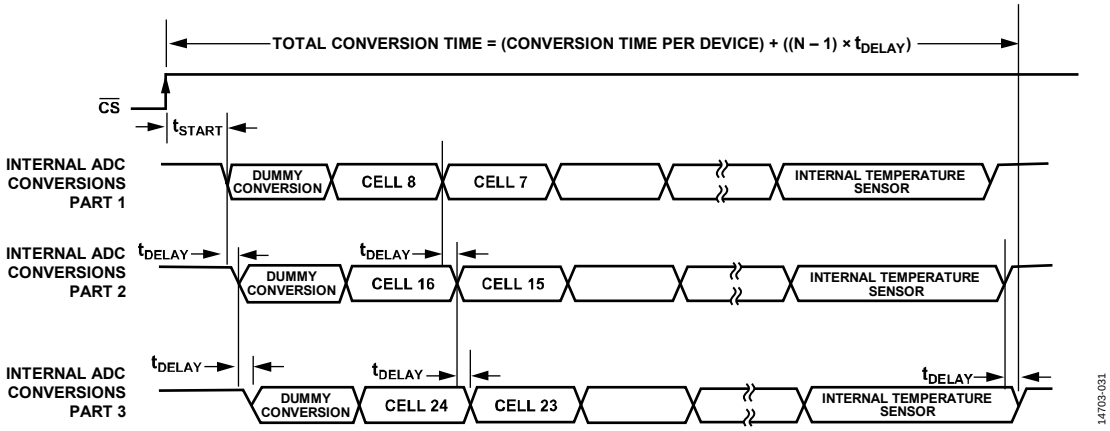


Figure 29. ADC Conversions with a Chain of Three Devices

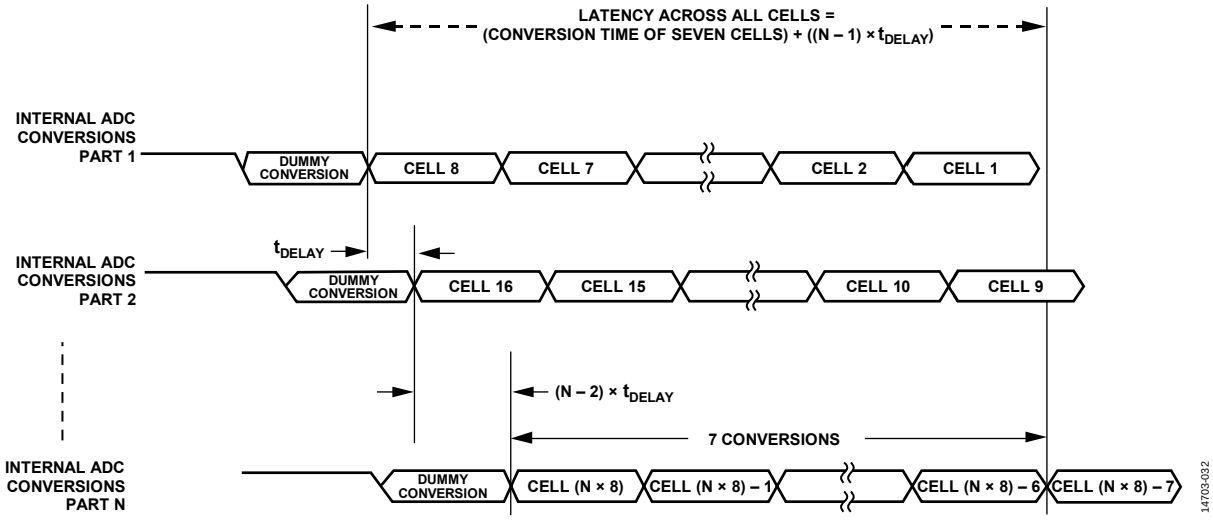


Figure 30. Latency Across All Cells

CONVERSION DATA READBACK

A sequence with ADC conversions and a readback operation is shown in Figure 31. The user issues a command to the device to start the conversion. The conversion data is available for read back when the channel acquisition and conversion times complete. The data returned from a conversion results readback operation is contained within multiple 64-bit packs, as described in the Conversion Data Readback Operation section.

Following a conversion, the primary conversion data for all devices in the daisy chain is available for readback. To enable secondary conversion data readback, a command is issued as shown in Figure 32. This is the only 32-bit command that can be issued while in 64-bit mode.

The sequence to read back primary and secondary data is described in the Example 5: Convert and Read All Conversion Data section.

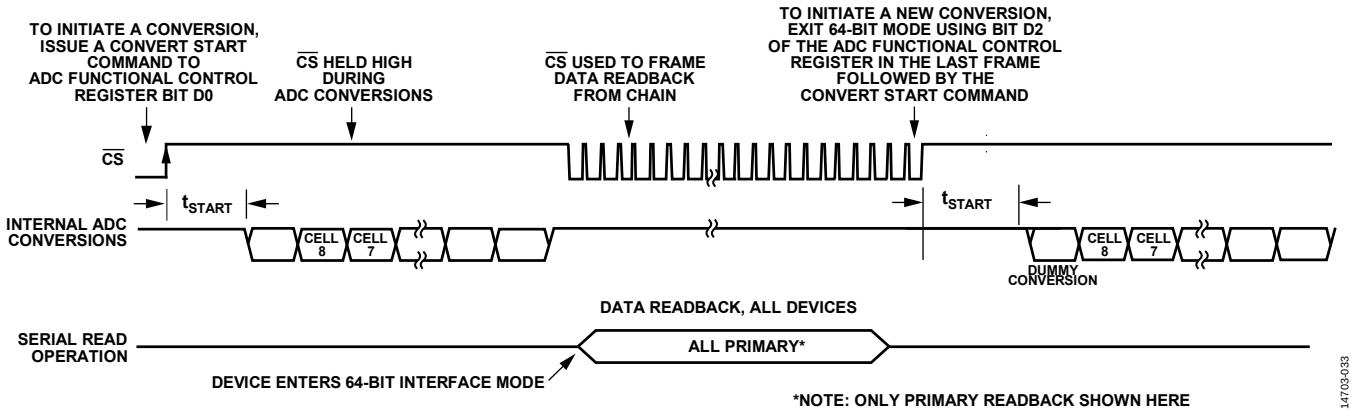


Figure 31. ADC Conversions and Readback of Primary Data and Initiation of a Second Conversion

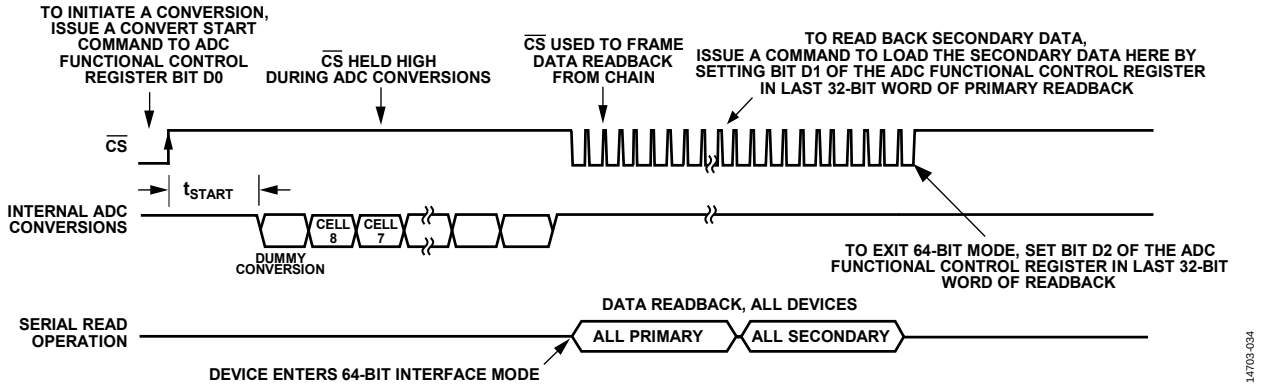


Figure 32. ADC Conversions and Readback of Primary and Secondary Data and Exit of 64-Bit Readback Mode

CELL BALANCING OUTPUTS

The AD7284 provides eight cell balance outputs that can drive the gates of the external transistors as part of a cell balancing circuit. The cell balance feature can be used while converting cell voltage measurements; however, the accuracy of the conversions degrades. Cell balancing is also available while the AD7284 is in partial power-down mode.

Cell Balance Connections

As shown in Figure 33, five of the cell balance outputs (CB1 to CB5) are capable of driving an N channel, metal oxide semiconductor field effect transistor (MOSFET), while the other three (CB6 to CB8) drive a P channel MOSFET. These outputs are designed to drive 20 µA (typical) into the external FET, enabling turn on within 100 µs.

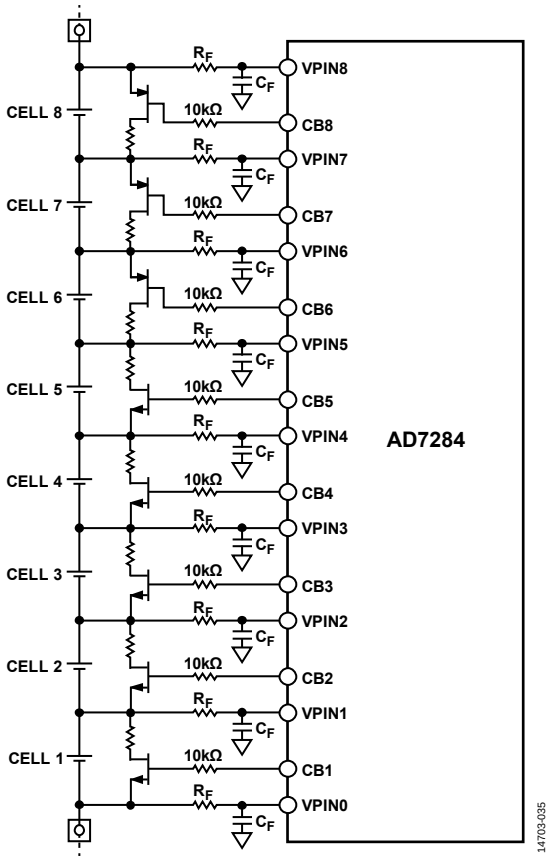


Figure 33. Cell Balancing Configuration

In an application with two or more AD7284 devices in a directly connected daisy chain, it is recommended to place 10 kΩ series resistors between the CBx outputs of the AD7284 and the gates of the external cell balancing transistors. These resistors, in conjunction with the internal 5 V clamps, help protect the CBx outputs and gates of the external cell balancing transistors during the initial connection of the monitoring circuitry to the battery stack.

The simplified internal configuration of the cell balance circuit (CB1 to CB5) is shown in Figure 34.

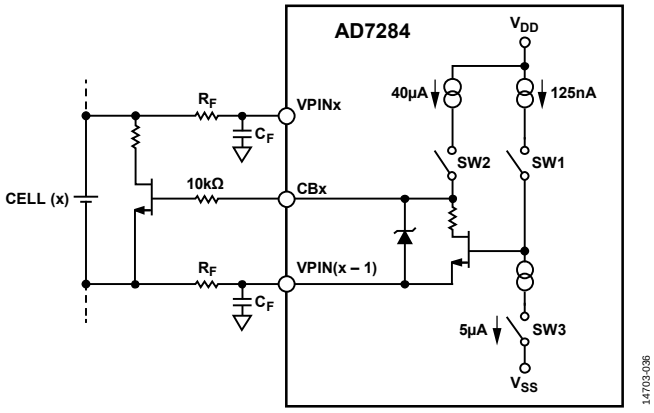


Figure 34. Simplified Internal Configuration of the Cell Balancing Circuit (CB1 to CB5)

When cell balancing is disabled, SW1 is closed, SW2 and SW3 are open, the negative channel metal oxide semiconductor (NMOS) switch is on, and the CBx pin is pulled to VPIN(x – 1). When enabled, SW1 is open, SW2 and SW3 are closed, the NMOS switch is off, and the CBx voltage increases as current charges the gate of an external FET. The internal clamp ensures that CBx stays within approximately 5 V of VPIN(x – 1) and provides a path for some of the 40 µA out of VPIN(x – 1), which causes a voltage drop on VPIN(x – 1). The voltage drop depends on the value of the input resistor. CB6 to CB8 use an equivalent positive channel metal oxide semiconductor (PMOS) circuit.

Cell Balance Outputs Interface

Three bits are used to control the cell balancing feature:

- The cell balance power-down bit, CBPDB, in Control Register 1 (see Table 21) controls the cell balance output drivers. The default value of this bit at power-up is 0, and the drivers are disabled. Turn off the drivers when cell balancing is not used to reduce power consumption and maintain accuracy on cell monitoring.
- The general output enable bit, GOE_CB, in Control Register 3 (see Table 24) allows the host microcontroller/DSP to control the state of all cell balance outputs with one write command while still maintaining the current state of the cell balance control register. The default value of this bit at power-up is 0, which corresponds to the cell balance outputs off state.
- The cell balance bits, CBx, in the cell balance control register (see Table 26) allow the user to individually configure the state of the cell balance output. The default value of this register at power-up is 0x00, and each of the cell balance outputs are disabled.

To enable cell balancing on one or multiple cells, the CBPDB bit, the GOE_CB bit, and the corresponding CBx bit(s) must be set to 1.

Programmable On Time

To enable individual programmable on times, activate the corresponding CBx output(s) as described in the Cell Balance Outputs Interface section. Programming an on time for a disabled CBx output has no effect.

The AD7284 offers eight cell balance timer (CBTx) registers to individually program the on time of the CBx output pins. On times of 0 minutes (the output stays turned on) to 8.5 hours can be programmed with a two minute resolution. All CBTx registers are 0x00 by default. The values programmed in the CBTx registers are compared with a single timer. The default value of the timer is 0x00. The current value of the timer is available in the current cell balance count state (CBCNT) register.

The timer starts from 0x00 when a CBTx register is written to. When the value in the timer reaches the value of any of the CBTx registers, the corresponding CBx output is switched off. The timer stops when the largest value programmed in the enabled CBTx registers is equal to the timer. CBTx registers settings are maintained following a timeout event.

The timer restarts from 0x00 on a write to any of the active CBTx registers. Writing zero causes the corresponding cell balance output to switch off and the timer to restart. A write to the CBCTRL register while the timer is active causes the timer to restart from 0x00. The CBCNT register can adjust the values of previously enabled cell balance timers. Individual or all CBx output(s) can be switched off before the timer reaches its or their programmed value(s) by disabling the CBx output(s) as described in the Cell Balance Outputs Interface section.

The cell balance timer is independent of the power-down timer. Use the power-down timer to allow cell balancing to occur for a set time before powering down the AD7284.

Note that the power-down timer can be used instead of the watchdog timer when using the cell balancing timer to prevent the need to service the watchdog timer.

OPEN INPUT DETECTION

Two methods are available to detect an open wire condition between the cell and an ADCs input pin: open input sense and cell balance sense. These methods require the use of the secondary path and independent filters on the ADC inputs.

The host controller initiates the diagnostic request. It then reads back conversion results from primary and secondary inputs from which it is possible to determine an open input condition.

Open Input Sense

The open input sense (OIS) technique allows the detection of an open wire at the board edge or at the device input.

When enabled, the OIS diagnostics cause a small current to sink (or source, in the case of VPIN0 and VSIN0) from the selected primary or secondary voltage sense pin. A delay is also introduced between the primary and secondary conversions. If an input wire disconnects, the OIS current sources from or sinks into the input filter capacitor, causing the input voltage to shift. This shift is seen as a difference between the primary and secondary measurements.

The size of the voltage shift depends on the size of the input filter capacitor, the delay between primary and secondary measurements (1000 µs), and the OIS current (100 µA).

For a 100 nF filter capacitor, a shift of 500 mV is expected. If the input pins are connected correctly, a voltage drop of approximately 100 mV is measured between the primary and secondary inputs when using a 1 kΩ input resistor, R_F.

Cell Balance Sense

An alternative method is using the cell balance function. This technique is useful for detecting board edge open wire conditions. When enabled, a cell balance FET that is off for the first conversion is switched on for the second conversion. If the input wire disconnects, the enabled FET causes the input that disconnected to pull toward the pin on the opposite side of the enabled FET.

Sequence of Operations

To perform an open wire diagnostic on an input, use the following procedure:

1. Enable the OISx bit for the cell connection under investigation using the OISCTRL control register and/or the OISGPOP control register, or set the appropriate cell balance enable bit in the cell balance control register.
2. In the Control 3 register, select the appropriate input sense function via the IN_SNSE bits, set the ADC delay bit (ADCDLY), and select the conversion order with the ADCORDR bit. If not in delay mode, the GOE_x bits gate the respective cell balance or the OISCTRL register settings.
3. Set the CBPDB bit in Control Register 1 for the cell balance method.
4. Initiate a conversion and read back the primary and secondary data.

POWER MANAGEMENT

AD7284 SUPPLIES

The AD7284 is powered from the cell stack. The device connects to the cell stack positive terminal (+HV) through the V_{DD} pin and the cell stack negative terminal (−HV) through the V_{SS} pin. An internal regulator generates a 5 V supply (V_{REG5}) for the internal core of the AD7284, as shown in Figure 35.

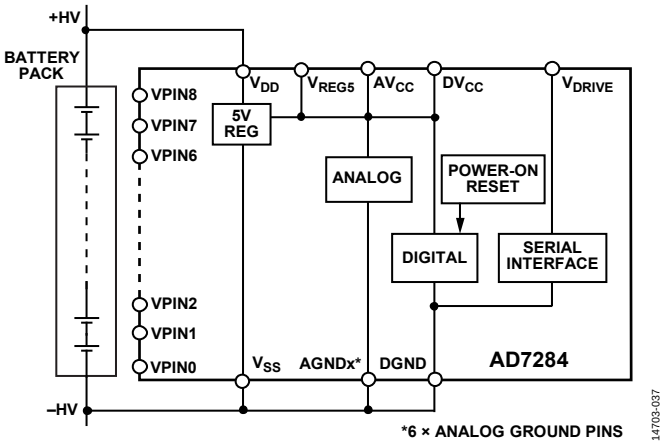


Figure 35. Power Supply Overview (External Circuitry Omitted for Clarity)

A total decoupling capacitance of 4.7 µF is recommended on the V_{DD} pins. Optionally, use 2.2 µF in parallel with 100 nF on each of the V_{DD} pins.

It is required that 100 nF be present on the regulator output pin, V_{REG5}, and on each of the low voltage supplies, AV_{CC} and DV_{CC}. Connect these three pins together on the PCB.

V_{DRIVE}

For the master device only, an external V_{DRIVE} supply is required to power the digital input/output pins to ensure interface compatibility with host supplies operating at 3.3 V or 5 V. Therefore, do not drive the digital input pins when V_{DRIVE} is low.

V_{DRIVE} is also an integral part of the power-up/power-down scheme within the AD7284, as described in the Active Mode, Power-Up section and the Power-Down section. Pulling V_{DRIVE} low places the AD7284 into the lowest power mode, unless an active power-down timer is running.

A 100 nF decoupling capacitor is recommended on the V_{DRIVE} pin for the master device only.

On slave devices, connect V_{DRIVE} directly to V_{REG5} at all times. In this configuration, all currents supplied by the low voltage pins, such as V_{REFBUF}, GPOP1, and GPOP2, are supplied by the internal regulator. This regulator delivers 2 mA typically for use external to the AD7284.

MODES OF OPERATION

The three modes of operation for the AD7284 include the following: active mode (power-up), software partial power-down mode, and hardware full power-down mode.

In active mode, the AD7284 can be idle or perform the following tasks:

- ADC conversions.
- Conversion data readback.
- Register read and write.
- Cell balancing (cell balancing and register reads or writes, can also be performed in partial power-down mode).

The current consumption is specified in Table 1.

ACTIVE MODE, POWER-UP

Connect the V_{DRIVE} pin on the AD7284 master device to an external voltage supply. A rising edge on the V_{DRIVE} supply signals the AD7284 master device to power up. If V_{DRIVE} is already held high, an alternate method of powering up the master is via a pulse of 100 ns minimum on the RESET pin.

Power-Up Time

The time required for an AD7284 master device to power up and to receive SPI communications is typically 200 µs with a total capacitance of 300 nF on V_{REG5} (100 nF on each pin). The time required to perform accurate ADC conversions is typically 5 ms. These figures apply when V_{REF1} and V_{REF2} are decoupled with a 1 µF in parallel with 100 nF.

The AD7284 slave devices power up through a slave wake-up signal that is automatically transmitted through the daisy chain. The master device transmits the slave wake-up signal to the first slave device, the first slave device transmits the wake-up signal to the device above it in the daisy chain, and so on. Each device transmits a slave wake-up signal typically within 100 µs of receiving its own wake-up signal. The time required for a slave device to power up and perform accurate ADC conversions is typically 5 ms (see Figure 36).

Calculate the total power-up time for a chain of AD7284 devices connected in the direct current configuration by

$$Total\ Power\text{-}Up\ Time = 5\ \text{ms} + ((N - 1) \times 100\ \mu\text{s})$$

where N is the number of AD7284 devices in the daisy chain.

Connect the V_{DRIVE} pin on each slave device to its own V_{REG5} pin.

Multiple dummy register writes are required to wake up the chain in a configuration with an isolated daisy chain.

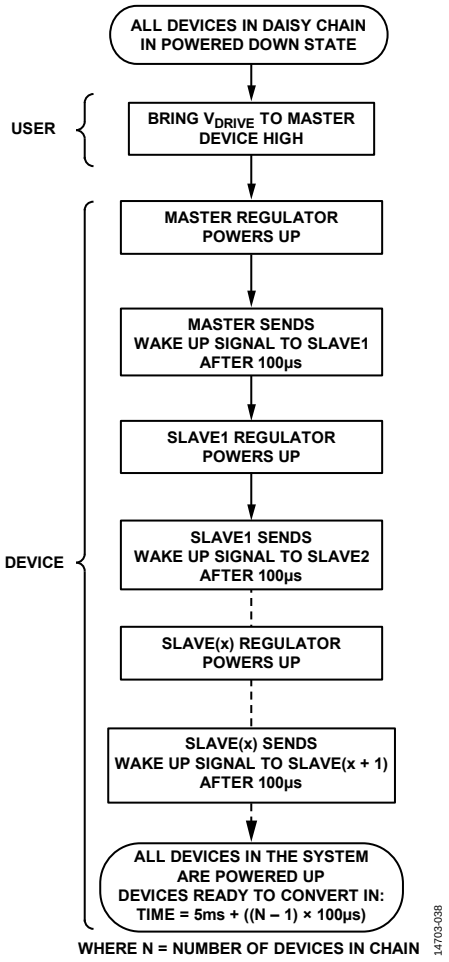


Figure 36. Power-Up Flowchart for a Direct Coupled Daisy Chain

RESET

An optional RESET input can reset the AD7284, which is an active high input and is provided primarily for use in resetting the master device. Resetting the master device reverts it to the default state on power-up. The hardware reset signal is not physically communicated to the slave devices. A software reset command to the slave devices is required to implement a full chain reset. Note that a software reset does not reset the device identification.

The RESET pin of a master device can wake up a chain of devices, as described in the Active Mode, Power-Up section.

For debug purposes, assert the RESET pin on an individual slave device to reset that device. Appropriate isolation is required.

POWER-DOWN

The following features are available to allow flexible power savings on the AD7284:

- A software (partial) power-down option.
- A hardware (full) power-down option.
- A power-down timer that controls when the device enters hardware power-down mode.

Software (Partial) Power-Down Mode

During software (partial) power-down mode, cell balancing and register reads or writes can be performed. The registers stay configured and the primary reference and LDO stay powered up to ensure accurate measurements can be performed immediately after wake up. Additionally, the watchdog timer remains active, as does the daisy chain so that communication is available to wake up the device.

Hardware (Full) Power-Down Mode

In hardware (full) power-down mode, the regulator powers off. When placing the device into full power-down mode, all digital inputs on the AD7284 master device must return to 0 V within a similar timescale to V_{DRIVE} going low.

Power-Down Timer

The power-down timer register allows the user to configure a set time after which the AD7284 enters hardware power-down mode.

The power-down timer can be set to 0 hours to 8.5 hours, with a resolution of two minutes, and the user can read back the current value of the power-down timer by reading the power-down counter register. The power-down timer starts to count up when the HWPD bit in Control Register 1 is set (and if the power-down timer register is not equal to 0x00). If the power-down timer register is written to after the counter starts, the counter is reset and then restarts automatically, counting to the new value in the power-down timer register. When the timer reaches the value in the power-down counter register, the device enters power-down mode after checking for the following conditions:

- For a master device, V_{DRIVE} must be low.
- For a slave device, the HWPD bit in Control Register 1 must be set.

See the Power-Down Entry Sequences section for more details.

The default value of the power-down timer register at power-up and reset is 0x00, or there is no timer delay.

Power-Down Entry Sequences

Enter power-down by using two methods: controlling the watchdog timer as described in the Watchdog Timer section, or by configuring the HWPD bit in Control Register 1 and the power-down timer, as described in this section.

Depending on whether the device is configured as a master or a slave, there are two methods for enabling the full power-down mode:

- A slave device is set to full power-down mode by configuring the power-down timer first (optional) and setting Bit D2 of Control Register 1, HWPD.
- A master device is set to full power-down mode by pulling the V_{DRIVE} pin low. Delay entry into full power-down mode by using the power-down timer and the HWPD bit. The master device enters full power-down mode immediately after V_{DRIVE} is pulled low if the timer value is 0. With the V_{DRIVE} pin held high, the HWPD bit only controls the start of the power-down timer.

Powering Down a Chain of Devices

Figure 37 shows a sequence to fully power down a chain of devices.

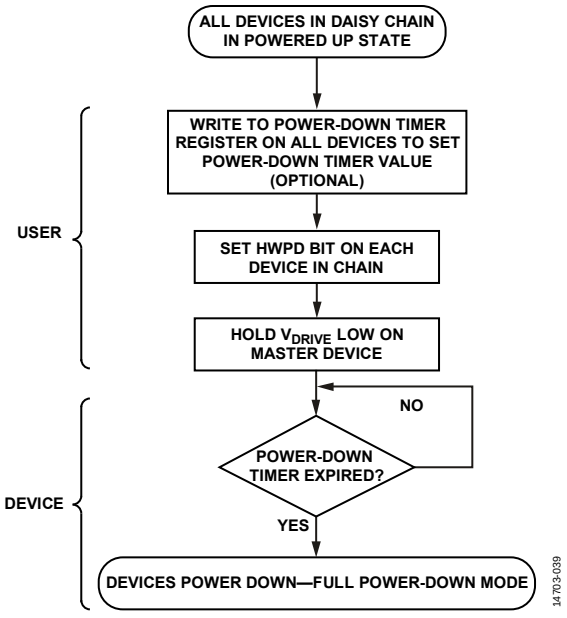


Figure 37. Entry in Full Power-Down Mode

To power down a chain of devices without using a timer, use the following procedure:

1. Set Bit D2 of Control Register 1 to 1 on all devices to select a hardware power-down.
2. Pull V_{DRIVE} low on the master device.

To power down a chain of devices using the power-down timer, use the following procedure:

1. Write to the power-down timer (PDT) register on all devices to set a power-down timer value.
2. Set Bit D2 of Control Register 1 to 1 on all devices to select a hardware power-down, which activates the power-down timer.
3. Pull V_{DRIVE} low on the master device.

All devices power down on the expiration of the power-down timer.

If V_{DRIVE} is not low when the power-down timer expires, set the HWPD bit of the master to 0 or reset the master device. The slave devices continue to power down following power-down timeout, as long as the HWPD bit is set high.

WATCHDOG TIMER

The watchdog timer (WDT) register allows the user to configure a set time after which the AD7284 is automatically powered down if communication to the device is lost.

The AD7284 allows the user to set the watchdog timer to a maximum value of 1040 ms and with a resolution of 8.192 ms. Service the watchdog timer by regularly writing a timeout value to the watchdog timer register before it expires to restart the timer and prevent the device from powering down.

At power-up, the watchdog timer is enabled with a default value of 0x0C (98.304 ms).

Disabling the watchdog timer may be required for a long cell balancing period, where the cell balancing timer and power-down timer are used. In this scenario, enable the power-down timer before disabling the watchdog timer.

The sequence to disable the watchdog timer involves three consecutive register write operations:

1. Write 0x00 to the watchdog timer register.
2. Write 0x5A to the watchdog key register.
3. Write 0x00 again to the watchdog timer register.

Any intermediate SPI command resets the process of disabling the watchdog timer, reducing the risk of disabling it unintentionally. See the Example 3: Disabling the Watchdog Timer section for more details.

If the watchdog timer is enabled and the device is placed in partial power-down mode, the device enters full power-down mode, unless a nonzero value is written to the watchdog timer register before the watchdog timer times out.

If the watchdog timer times out, the device (or the chain of devices) enters full power-down mode. The master stays in this mode until either V_{DRIVE} or RESET are toggled.

SERIAL PERIPHERAL INTERFACE (SPI)

The AD7284 SPI is Mode 1 SPI compatible, that is, the clock polarity (CPOL) is 0, and the clock phase (CPHA) is 1. The interface consists of four signals: $\overline{CS}$, SCLK, SDI, and SDO, as shown in Figure 3. The SDI line transfers data into the on-chip registers, and the SDO line reads the on-chip registers and conversion result registers. SCLK is the serial clock input for the device, and all data transfers, either on SDI or on SDO, take place with respect to SCLK. Data clocks into the AD7284 on the SCLK falling edge, and data clocks out of the AD7284 on the SCLK rising edge. The $\overline{CS}$ input frames the serial data being transferred to or from the device. The register data and the ADC conversion readback data can be framed by $\overline{CS}$ in 32-bit or 16-bit SCLK bursts, allowing the greatest flexibility for connecting to processors.

All register reads and writes are configured as 32 bits of data, while all conversion results are configured as 64-bits words.

The AD7284 powers up in 32-bit mode and automatically enters 64-bit mode when conversions initiate. The device remains in 64-bit mode until returned to 32-bit mode by writing 0x04 to the ADC functional control register. Conversion data cannot be reread from the AD7284; if an attempt is made to reread data, it reads as 0. The life counter value is identical to the previous read because it increments between conversion sets.

REGISTER WRITE AND REGISTER READ OPERATIONS

Up to 30 AD7284 devices can be daisy-chained together to allow monitoring up to 240 individual Li-Ion cell voltages. The AD7284 SPI interface, in combination with the daisy-chain interface, allows any register in the 30 AD7284 stack to be updated using one 32-bit write command.

All register write and read operations are performed via the SPI using a 32-bit data packet. The format of the 32-bit data packet is described in Table 10.

Each register access must include a device address and a register address, in addition to the data to be written. The AD7284 also requires a 12-bit cyclic redundancy check (CRC) to be included in each 32-bit write command.

Register Read Operation

To read back a register from a chain of AD7284 devices, write the address of the desired register to be read back to the read register (Register 0x3F).

Follow this with null frames (0x00000000) for each device in the daisy chain. For example, eight null frames for an eight device chain. Each of these frame returns the register content of each device, starting with the master. See the Examples of Interfacing with the AD7284 section for more details.

It is not possible to read one register from one device in the chain, that register in all devices in the chain must be read.

Device Address

The device address is a 5-bit address that allows each individual AD7284 in the battery monitoring stack to be uniquely identified. A maximum of 30 devices can be supported in one chain. On initial power-up, each AD7284 is configured with a default address of 0x00. A simple sequence of commands allows each AD7284 to recognize its unique device address in the stack (see the Example 1: Initialize All Devices in a Daisy Chain section). This device address can then be locked to the AD7284 and is used in subsequent read and write commands. A unique device address of 0x1F is used to address all devices in the stack.

Register Address

As shown in Table 10, D25 to D20 form a 6-bit register address. Register addresses can be found in Table 14.

Write and Write/Read

As shown in Table 10, Bit D26 controls the data transfer mode on the daisy chain, unidirectional (write) or bidirectional (write/read) communication.

With D26 high, the next communication in the chain is unidirectional, and the master transmits the SPI command to the slaves up the chain. D26 is typically high for register write operations. The maximum SCLK frequency is 725 kHz when the daisy chain operates in unidirectional mode.

With D26 low, the next communication in the chain is bidirectional. The master transmits the SPI command to the slaves and then switches to receive mode, expecting data back from the slaves. The slaves start in receive mode and switch to transmit mode after reception of the command.

A minimum delay of 50 µs is required prior to switching from bidirectional to unidirectional mode (not applicable for the master only setup). The maximum SCLK frequency is 500 kHz when the daisy chain operates in bidirectional mode.

Examples of register read and register write operations can be found in the Examples of Interfacing with the AD7284 section.

Register Data

As shown in Table 10, the register data field (Bits[D19:D12]) contains the data to be written into the register during a register write operation. All AD7284 registers are 8 bits wide and are listed in Table 14 in the Register Map section.

12-Bit CRC

The AD7284 includes a 12-bit CRC with a Hamming distance of six on all write commands to either individual devices or to a chain of devices. An AD7284 that receives an invalid CRC in the write command does not execute the command. The CRC on the write command is calculated based on Bits[D31:D12] of the write command, which includes the device address, the register address, and the register data. The CRC polynomial ((0xB41) in Koopman's notation) used when writing to or reading from the AD7284 is

$$x^{12} + x^{10} + x^9 + x^7 + x^1 + 1$$

CONVERSION DATA READBACK OPERATION

The data returned from a conversion result read operation is contained within a 64-bit packet. The data returned includes the device address, the channel addresses, a life counter, and a 16-bit CRC, in addition to the two conversions results, which are each 14 bits. The 64-bit read conversion result packet is shown in Table 11.

When reading back conversion data from a daisy chain of AD7284 devices, the conversion data is first read from the primary measurement path on the master device, followed by the primary measurement path from the first slave device, and so on. When all the conversion data is returned for the primary measurements, the device can then be configured to read back the secondary measurement data.

When reading conversion results from a chain of 12 devices monitoring 96 cells, the readback time is of the region of 9.5 ms when using the higher SCLK rate of 725 kHz (t_{SCLK} = 1.38 µs). For 12 devices, the total number of primary conversions is,

$$12 \times 18 = 216$$

Two conversion sets are packed into a 64-bit frame; therefore, the number of bits transferred is

$$216 \div 2 \times 64 = 6912$$

The transfer time is the number of bits transferred multiplied by the bit period defined by SCLK, 6912 Bits × t_{SCLK} = 9.5 ms.

Within a single device, the device converts all 18 primary and 10 secondary channels. All 18 primary conversions must be read back, which may be followed by optional read back of all 10 secondary conversions as required.

See the Example 5: Convert and Read All Conversion Data section for more details. The 64-bit conversion data packets can be read back in 4 × 16-bit or 2 × 32-bit frames.

Channel Addresses

The channel address allows individual measurement results to be uniquely identified. Each channel address is six bits wide and two channel addresses are contained within each 64-bit read cycle. The address for each channel is detailed in the register map for the AD7284 (see Table 14).

Life Counter

As shown in see Table 14, the life counter is a 3-bit counter that increments every time a successful sequence of conversions is completed. After the counter reaches 7, it wraps around and starts counting again from 0. This feature allows the detection of a conversion sequence that is not complete. The life counter is cleared on a software reset or hardware power-down.

Conversion Data

As shown in see Table 14, the conversion data readback consists of 14 bits. When reading back a conversion result from the primary measurement path, the 14-bit conversion result is included. When reading back a conversion result from the secondary measurement path, an inverted 10-bit conversion result plus 4 MSB data bits set to 0 make up the 14-bit data value returned.

Device Address

The device address is described in the Register Write and Register Read Operations section.

16-Bit CRC

The AD7284 includes a 16-bit CRC with a Hamming distance of six within the 64-bit pack and is calculated based on Bits[D63:D16] of the read conversion result cycle. The CRC calculations include Channel Address 1, the life counter, Channel Address 2, Conversion Data 1, the device address, and Conversion Data 2. The CRC polynomial ((0xC86C) in Koopman's notation) used when reading conversion data from the AD7284 is

$$x^{16} + x^{15} + x^{12} + x^7 + x^6 + x^4 + x^3 + 1$$

Table 10. 32-Bit Register Write/Read Operations

Device Address	Write and Write/Read	Register Address	Register Data	CRC
D31 to D27 5 bits	D26 1 bit	D25 to D20 6 bits	D19 to D12 8 bits	D11 to D0 12 bits

Table 11. 64-Bit Read Conversion Result Packet

Channel Address 1	Life Counter	Channel Address 2	Conversion Data 1	Device Address	Conversion Data 2	CRC
D63 to D58 6 bits	D57 to D55 3 bits	D54 to D49 6 bits	D48 to D35 14 bits	D34 to D30 5 bits	D29 to D16 14 bits	D15 to D0 16 bits

CRC PSEUDOCODE EXAMPLES

The following pseudocode examples show how to calculate the CRC for two types of data packets.

The following variables must first be declared:

- i is an integer variable.
- shft[xx] are an integer variables.
- data_in represents the data bits that the CRC is calculated on (Bits[D31:D12]). This data supplies the input to the first XOR gate.
- xor_0 is an integer variables. The outputs of the shift registers start at the leftmost shift register in the circuit implementation. With the exception of data_in, initialize all variables to 0.

12-Bit CRC

To calculate the CRC value from the preceding 20 bits of data, use the following pseudocode, where sfht[n] corresponds to CRC_x in Figure 38 and Figure 39:

```
for (i=31; i>=12; i--)
      {
      xor_0 = data_in[i] ^ shft[11];
      shft[11] = shft[10];
      shft[10] = shft[9] ^ xor_0;
      shft[9] = shft[8] ^ xor_0;
      shft[8] = shft[7];
      shft[7] = shft[6] ^ xor_0;
      shft[6] = shft[5];
      shft[5] = shft[4];
      shft[4] = shft[3];
      shft[3] = shft[2];
      shft[2] = shft[1];
      shft[1] = shft[0] ^ xor_0;
      shft[0] = xor_0;
      }
crc12calc = shft;
```

16-Bit CRC

To calculate the CRC value from the preceding 48 bits of data, use the following pseudocode:

```
for (i=63; i>=16; i--)
      {
      xor_0 = data_in[i] ^ shft[15] ;
      shft[15] = shft[14] ^ xor_0;
      shft[14] = shft[13];
      shft[13] = shft[12];
      shft[12] = shft[11] ^ xor_0;
      shft[11] = shft[10];
      shft[10] = shft[9];
      shft[9] = shft[8];
      shft[8] = shft[7];
      shft[7] = shft[6] ^ xor_0;
      shft[6] = shft[5] ^ xor_0;
      shft[5] = shft[4];
      shft[4] = shft[3] ^ xor_0;
      shft[3] = shft[2] ^ xor_0;
      shft[2] = shft[1];
      shft[1] = shft[0];
      shft[0] = xor_0;
      }
crc16calc = shft;
```

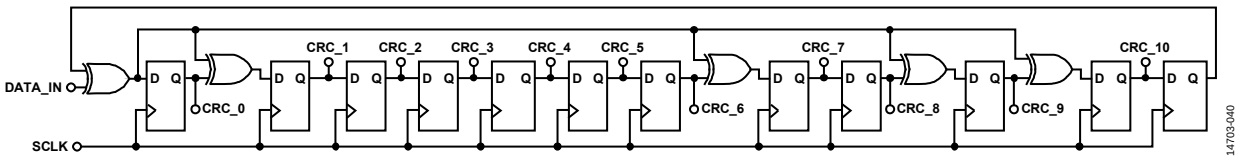


Figure 38. 12-Bit CRC Implementation

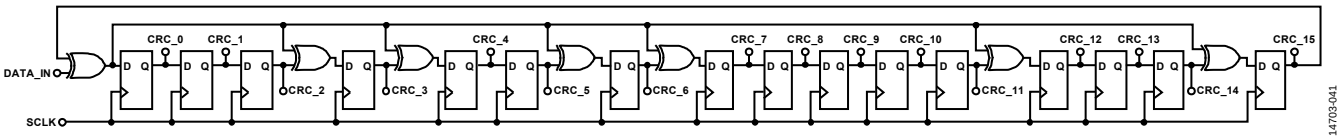


Figure 39. 16-Bit CRC Implementation

DAISY-CHAIN INTERFACE

To minimize isolation requirements and simplify the interface between the host processor and each battery monitoring device, the master AD7284 device is the only communication port to the host processor. All slave devices interface via the master device using a 2-wire daisy-chain interface.

Each AD7284 device is powered from the top and bottom terminals of the cell pack. The supply voltage of each device is offset from the adjacent device in the chain by as much as 40 V.

The AD7284 daisy-chain interface is a fully differential, 2-wire, half-duplex interface enabling minimal interconnects and robust communication between devices in a chain.

DAISY-CHAIN PHYSICAL INTERFACE

The daisy-chain interface consists of a differential daisy chain for up paths (D_UP/$\overline{\text{D\_UP}}$) and down paths (D_DWN/$\overline{\text{D\_DWN}}$). When multiple devices are configured in a chain, the up paths from the master are connected to the down paths of the adjacent slave. Similarly, the up paths on the other side of the slave device interfaces to the down path of the next adjacent slave device, and so on, as shown in Figure 40.

The internal common-mode amplifier provides a C_{CM} voltage of typically 2 V above the V_{SS} rail, which biases the daisy-chain paths. The C_{CM} pin requires a 1 µF capacitor to V_{SS}.

When communicating between devices located on the same board, the daisy chain requires a single pair of external termination resistors (50 Ω) connected to the C_{CM} pin.

When interfacing between devices across boards, pairs of 50 Ω terminations are required on each sides of the daisy chain. A low value capacitor (≤100 nF) is required from the termination center point to the V_{DD} rail.

Additional protection circuitry beyond what is shown in Figure 40 may be required on the daisy-chain pins for hot plug and service disconnect (see the Hot Plug section and the Service Disconnect (SD) section).

An alternative approach is using a transformer to provide isolation, as described in the Transformer Configuration section.

DAISY-CHAIN PROTOCOL

The daisy chain uses a proprietary protocol with a preamble or start condition, a Manchester encoded data packet, including a CRC and a stop condition. The data bit rate is 3.125 Mbps typical.

The daisy-chain interface operates in unidirectional mode for register write and conversion data readback operation, or in bidirectional mode for register read operation.

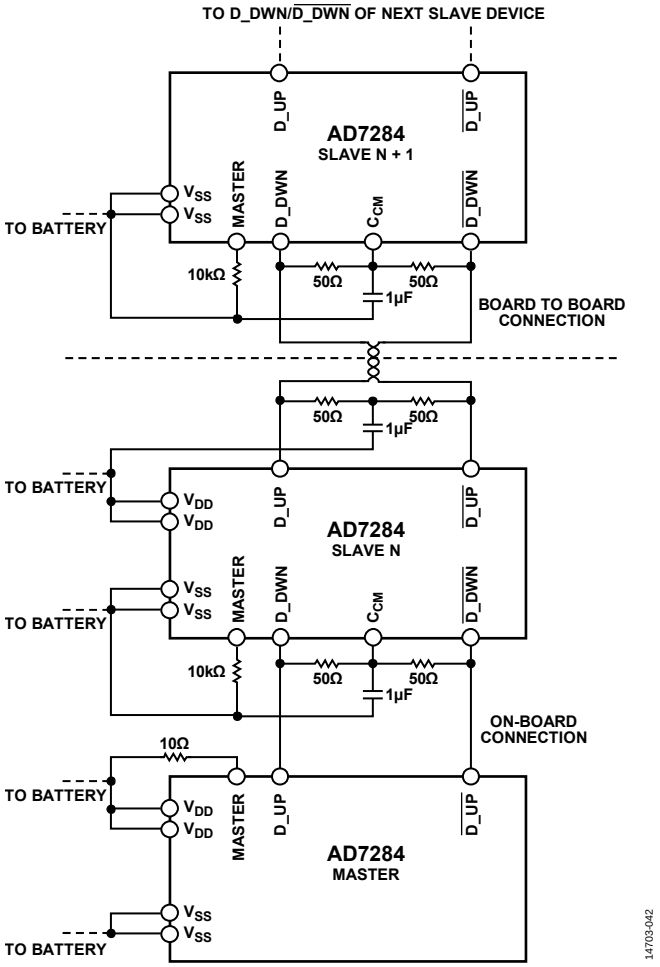


Figure 40. AD7284 Daisy-Chain Interconnection Examples (Additional Circuitry Omitted for Clarity)

DAISY-CHAIN DEBUG MODE

The AD7284 incorporates a debug feature using the two GPOPx pins (GPOP1 and GPOP2) that allow the user to monitor the daisy-chain communications between devices. The daisy chain is a current-based interface. The debug feature translates the daisy-chain communications into a single-ended voltage relative to the logic levels of the corresponding device.

Configuration of the debug feature involves setting Bit D0 (GPOP SEL) of the OISGPOP control register (see Table 28) to enable the feature.

Table 12. Daisy-Chain Debug Configuration

Device	GPOP1	GPOP2
Master	Commands transmitted to device above	Data received from device above
Slave	Commands received from device below	Data received from device above

REGISTER MAP

PAGE ADDRESSING

The AD7284 uses page addressing to maximize register addressing space. Page 0 is the default page on power-on.

Page 0 initiates a conversion and accesses primary or secondary ADC data. Page 1 contains all the configuration and diagnostic register space, see Table 14.

Throughout the register map, there is reserved register address space. This space does not provide any user functions; it is reserved space to support future software compatibility.

Page Register

To access a particular page, first write the relevant page number to the page register (Register 0x3E); this gives access to the registers contained within that page. To access further registers from the currently selected page, it is not necessary to rewrite the page selection.

Table 13. Page Register (Register 0x3E)

Bits	Name	Description
[D7:D2]	Not applicable	Reserved
[D1:D0]	Page	00: Page 0 01: Page 1

Table 14. Register Map

Page Number	Address	Register Description	Register Name[1]	Data Bits[1]	Access[1]	Power-On Default/Reset[1]
0	0x00	Null frame	N/A	N/A	N/A	N/A
0	0x01	Primary Cell Voltage 1	VPIN1	D13 to D0	Read	0x0000
0	0x02	Primary Cell Voltage 2	VPIN2	D13 to D0	Read	0x0000
0	0x03	Primary Cell Voltage 3	VPIN3	D13 to D0	Read	0x0000
0	0x04	Primary Cell Voltage 4	VPIN4	D13 to D0	Read	0x0000
0	0x05	Primary Cell Voltage 5	VPIN5	D13 to D0	Read	0x0000
0	0x06	Primary Cell Voltage 6	VPIN6	D13 to D0	Read	0x0000
0	0x07	Primary Cell Voltage 7	VPIN7	D13 to D0	Read	0x0000
0	0x08	Primary Cell Voltage 8	VPIN8	D13 to D0	Read	0x0000
0	0x09 to 0x10	Reserved	N/A	N/A	Reserved	0x0000
0	0x11	Stack voltage	VSTK	D13 to D0	Read	0x0000
0	0x12	V_{REF2} voltage	VREF2	D13 to D0	Read	0x0000
0	0x13	V_{REG5} Voltage 1	VREG5_1	D13 to D0	Read	0x0000
0	0x14	Primary Auxiliary ADC 1	AUXP1	D13 to D0	Read	0x0000
0	0x15	Primary Auxiliary ADC 2	AUXP2	D13 to D0	Read	0x0000
0	0x16	Primary Auxiliary ADC 3	AUXP3	D13 to D0	Read	0x0000
0	0x17	Primary Auxiliary ADC 4	AUXP4	D13 to D0	Read	0x0000
0	0x18 to 0x1B	Reserved	N/A	N/A	Reserved	0x0000
0	0x1C	Reference buffer	REFBUF	D13 to D0	Read	0x0000
0	0x1D	V_{REG5} Voltage 2	VREG5_2	D13 to D0	Read	0x0000
0	0x1E	Temperature sensor	TMPSNR	D13 to D0	Read	0x0000
0	0x1F to 0x20	Reserved	N/A	N/A	Reserved	0x0000
0	0x21	Secondary Cell Voltage 1	VSIN1	D9 to D0	Read	0x000
0	0x22	Secondary Cell Voltage 2	VSIN2	D9 to D0	Read	0x000
0	0x23	Secondary Cell Voltage 3	VSIN3	D9 to D0	Read	0x000
0	0x24	Secondary Cell Voltage 4	VSIN4	D9 to D0	Read	0x000
0	0x25	Secondary Cell Voltage 5	VSIN5	D9 to D0	Read	0x000
0	0x26	Secondary Cell Voltage 6	VSIN6	D9 to D0	Read	0x000
0	0x27	Secondary Cell Voltage 7	VSIN7	D9 to D0	Read	0x000
0	0x28	Secondary Cell Voltage 8	VSIN8	D9 to D0	Read	0x000
0	0x29 to 0x30	Reserved	N/A	N/A	Reserved	0x000
0	0x31	V_{REF1} voltage	VREF1	D9 to D0	Read	0x000
0	0x32 to 0x33	Reserved	N/A	N/A	Reserved	0x000
0	0x34	V_{REG5} Voltage 3	VREG5_3	D9 to D0	Read	0x000
0	0x35 to 0x3C	Reserved	N/A	N/A	Reserved	0x000
0	0x3D	ADC functional control	ADCFUNC	D7 to D0	Write/read	0x00
0	0x3E	Page register	Page	D7 to D0	Write/read	0x00
0	0x3F	Read register	RDREG	D7 to D0	Write/read	0xFF

Page Number	Address	Register Description	Register Name[1]	Data Bits[1]	Access[1]	Power-On Default/Reset[1]
1	0x00	Null frame	N/A	N/A	N/A	N/A
1	0x01	Fault register	Fault	D7 to D0	Read	0xFF
1	0x02	Current cell balance count state	CBCNT	D7 to D0	Read	0x00
1	0x03	Current power-down count state	PDCNT	D7 to D0	Read	0x00
1	0x04	Current watchdog count state	WDCNT	D7 to D0	Read	0x00
1	0x05 to 0x06	Reserved	N/A	N/A	Reserved	0x00
1	0x07	Control Register 1	CTRL1	D7 to D0	Write/read	0x00
1	0x08	Control Register 2	CTRL2	D7 to D0	Write/read	0x00
1	0x09	Control Register 3	CTRL3	D7 to D0	Write/read	0x00
1	0x0A	Control Register 4	CTRL4	D7 to D0	Write/read	0x00
1	0x0B	Cell balance control	CBCTRL	D7 to D0	Write/read	0x00
1	0x0C to 0x0D	Reserved	N/A	N/A	Reserved	0x00
1	0x0E	OIS control	OISCTRL	D7 to D0	Write/read	0x00
1	0x0F	OIS GPOPx control	OISGPOP	D7 to D0	Write/read	0x00
1	0x10	Power-down timer	PDT	D7 to D0	Write/read	0x00
1	0x11	CB Timer 1	CBT1	D7 to D0	Write/read	0x00
1	0x12	CB Timer 2	CBT2	D7 to D0	Write/read	0x00
1	0x13	CB Timer 3	CBT3	D7 to D0	Write/read	0x00
1	0x14	CB Timer 4	CBT4	D7 to D0	Write/read	0x00
1	0x15	CB Timer 5	CBT5	D7 to D0	Write/read	0x00
1	0x16	CB Timer 6	CBT6	D7 to D0	Write/read	0x00
1	0x17	CB Timer 7	CBT7	D7 to D0	Write/read	0x00
1	0x18	CB Timer 8	CBT8	D7 to D0	Write/read	0x00
1	0x19 to 0x20	Reserved	N/A	N/A	Reserved	0x00
1	0x21	Watchdog timer	WDT	D6 to D0	Write/read	0x0C
1	0x22	Watchdog key	WDKY	D7 to D0	Write/read	0x00
1	0x23	Storage Register 1	STRG1	D7 to D0	Write/read	0x00
1	0x24	Storage Register 2	STRG2	D7 to D0	Write/read	0x00
1	0x25 to 0x3D	Reserved	N/A	N/A	Reserved	0x00
1	0x3E	Page register	Page	D7 to D0	Write/read	0x00
1	0x3F	Read register	RDREG	D7 to D0	Write/read	0xFF

[1] N/A means not applicable.

PAGE 0 ADDRESSES

Primary Path Conversion Results Registers

Page 0 contains the 18 registers, as follows, for the primary path:

- The cell voltage registers (VPIN1 to VPIN8) store the conversion result from each cell input to the primary measurement path.
- The stack voltage register (VSTK) stores the conversion result from the battery stack input to the primary measurement path.
- The V_{REF2} voltage register (VREF2) stores the conversion result of the secondary reference input to the primary measurement path.
- The V_{REG5} Voltage 1 register (VREG5_1) stores the conversion result of the regulated LDO voltage input to the primary measurement path through an odd multiplexer channel. A scaling factor of 2/3 is applied to the conversion result.
- The auxiliary ADC registers (AUXP1 to AUXP4) store the conversion result of each auxiliary ADC input to the primary measurement path.
- The reference buffer register (REFBUF) stores the conversion result of the thermistor buffer voltage V_{REFBUF} supply, which can be used for the external thermistor circuitry.
- The V_{REG5} Voltage 2 register (VREG5_2) stores the conversion result of the regulated LDO voltage input to the primary measurement path through an even multiplexer channel. A scaling factor of 2/3 is applied to the conversion result.
- The temperature sensor register (TMPSNR) stores the conversion result of the internal temperature sensor input to the primary measurement path.

The conversion results are in 14-bit straight binary format, except for the conversion result of the temperature sensor, which is in 14-bit, twos complement format.

Code 0 of the temperature sensor corresponds to 25°C with 32 LSB/°C of resolution.

Table 15 shows examples of output codes and corresponding junction temperature.

Table 15. Internal Temperature Sensor Output Codes Examples

Junction Temperature (°C)	Binary Output Code
−30	11 1001 0010 0000
0	11 1100 1110 0000
+24.96875	11 1111 1111 1111
+25	00 0000 0000 0000
+25.03125	00 0000 0000 0001
+120	00 1011 1110 0000

Secondary Path Conversion Results Registers

Page 0 contains the 10 registers for the secondary path, as follows:

- The cell voltage registers (VSIN1 to VSIN8) store the conversion result from each cell input to the secondary measurement path.
- The V_{REF1} voltage register (VREF1) stores the conversion result of the primary reference input to the secondary measurement path.
- The LDO Voltage 3 register (VREG5_3) stores the conversion result of the regulated LDO voltage input to the secondary measurement path through an even multiplexer channel. A scaling factor of 4/5 is applied to the conversion result.

The conversion results are inverted and in 10-bit straight binary format with four leading zeros.

ADC Functional Control Register

The ADC functional control (ADCFUNC) register allows initiation of a conversion sequence and selection of primary or secondary data.

Table 16. ADCFUNC Register Settings (Register 0x3D)

Bits	Name	Description
[D7:D3]	Reserved	Reserved, set to 0.
D2	EXIT64	Set to 1 to exit 64-bit data packet mode.
D1	SPIRLD	Set to 1 to load the secondary ADC results.
D0	CONVST	Trigger convert start; set to 1 to initiate the trigger convert start.

PAGE 1 ADDRESSES

Fault Register

The fault register (fault) allows the user to read the stored operational fault flags. The fault register is updated at the end of every conversion sequence. The fault register is reset to 0x00 after the user reads back from it. The default value of the fault register on power-up is 0xFF.

Table 17. Fault Register Settings (Register 0x01)

Bits	Name	Description
D7	PORFLAG	Power-on reset flag. Set to 1 to indicate that a power-on reset (POR) has occurred.
D6	WDFAULT	Watchdog power-down fault. Set to 1 when the watchdog timer times out.
D5	LDOFAULT	Set to 1 if the internal LDO supply is out of range, typically <4.8 V or >5.2 V.
D4	Reserved	Reserved, set to 0.
D3	FUSECRC	Set to 1 when the fuse CRC does not match the programmed fuse CRC value.
D2	CCMFAULT	Set to 1 when the voltage on the C_{CM} pin exceeds the overvoltage threshold that is set to 2.5 V typically. Also, set this bit to 1 when the voltage on the C_{CM} pin exceeds the undervoltage threshold that is set to 1.5 V typically.
D1	CFGFAULT	Set to 1 if in an illegal configuration occurs. Issue a reset to restart the device in a user configuration state.
D0	OSCDRIFT	The AD7284 has two internal oscillators which are trimmed to the same frequency. The oscillators are compared to each other and, if they differ by more than 3.9%, this bit is set to 1.

Current Cell Balance Count State Register

The current cell balance count (CBCNT) register stores the current value of the cell balance timer. The default value is 0x00.

Table 18. CBCNT Register Setting (Register 0x02)

Bits	Name	Description
[D7:D0]	CBCOUNT	LSB = 2 minutes. This register contains a value between 0x00 and 0xFF. The maximum value is 510 minutes.

Current Power-Down Count State Register

The current power-down count state (PDCNT) register is used in conjunction with the power-down modes that use the power-down timer register. The power-down counter register stores the current value of the power-down counter. If the power-down counter register is zero and the power-down is set, the slave device powers down immediately. See the Power-Down section for more details.

Table 19. PDCNT Register Setting (Register 0x03)

Bits	Name	Description
[D7:D0]	PDCOUNT	LSB = 2 minutes. This register contains a value between 0x00 and 0xFF. The maximum value is 510 minutes.

Current Watchdog Count State Register

The current watchdog count state (WDCNT) register stores the current running value of the watchdog timer counter.

Table 20. WDCNT Register Settings (Register 0x04)

Bits	Name	Description
D7	Not applicable	Reserved.
[D6:D0]	WDCOUNT	LSB = 8.192 ms. This register contains a value between 0x00 and 0x7F. The maximum value is 1040.384 ms.

Control Register 1

Control Register 1 (CTRL1) gives the user control of the various power-down features of the AD7284, the software reset functionality, and over the primary reference to allow it to be overdriven by an external source.

Table 21. CTRL1 Register Settings (Register 0x07)

Bits	Name	Description
[D7:D5]	Reserved	Reserved, set to 0.
D4	PREF	Primary reference overdrive. 0: normal mode, no overdrive. 1: overdrive mode. The primary reference can be driven externally.
D3	CBPDB	Cell balance power-down. 0: cell balance powered down. 1: cell balance powered up.
D2	HWPD	Hardware (full) power-down. 0: do not enter full power-down mode when the power-down timer is 0x00 (default). 1: if a value other than 0x00 is in the power-down timer register, start the power-down timer. Enter full power-down mode when the power-down timer reaches its timeout (also dependent on V_{DRIVE} for the master). If the power-down timer register is already at 0x00, power down the device (also dependent on V_{DRIVE} for the master). The HWPD bit takes precedence over the SWPD bit.
D1	SWPD	Software (partial) power-down. 0: do not enter partial power-down mode (default). 1: enter partial power-down mode immediately.
D0	SWRST	Software reset. 0: bring out of reset (default). 1: reset.

Control Register 2

Control Register 2 (CTRL2) sets the acquisition time of the ADC and provides current matching control of the daisy chain. See Table 23 for the appropriate setting for Bits[D6:D3].

Table 22. CTRL2 Register Settings (Register 0x08)

Bits	Name	Description
D7	Reserved	Reserved, set to 0.
D6	TXIBAL	Additional current equivalent to the transmit bias current. 0: matching on. 1: marching off.
D5	IDIODE	An additional 400 µA forward bias current is used for the service disconnect (SD) diode. 0: bias current enabled. 1: bias current disabled.
D4	RXIBAL	A level shifting current is required for the data receive circuit (120 µA). 0: current enabled. 1: current disabled.
D3	IMASTER	Master mode. 0: enable the transceiver (4.5 mA) and the receiver (3 mA) bias currents. 1: disable the transceiver and the receiver bias currents.
D2	Reserved	Reserved, set to 0.
[D1:D0]	ACQTME	Set acquisition time. 00: 400 ns (default). 01: 800 ns. 10: 1600 ns. 11: 3200 ns.

Table 23. Recommended Configuration for Control Register 2, Bits[D6:D3]

Bits	Setting	Description
[D6:D3]	0000	Master in a dc-coupled chain; service disconnect diodes used
	0000	Master in a chain with mixed coupling; service disconnect diodes used
	0000	Slave in a mixed chain with a transformer coupled connection to the device directly below; service disconnect diodes used
	0100	Master in a dc-coupled chain; no service disconnect diodes
	0100	Master in a chain with mixed coupling; no service disconnect diodes
	0100	Slave in a mixed chain with a transformer coupled connection directly below; no service disconnect diodes
	1010	Slave in a dc coupled chain; service disconnect diodes used
	1010	Slave in a mixed chain with a dc connection directly below; service disconnect diodes used
	1110	Master in a transformer coupled chain; no service disconnect diodes
	1110	Slave in a dc-coupled chain; no service disconnect diodes
	1110	Slave in a transformer coupled chain; no service disconnect diodes
	1110	Slave in a mixed chain with a dc-coupled connection directly below; no service disconnect diodes
	1111	Master only; no daisy chain

Control Register 3

Control Register 3 (CTRL3) is used for input sense control and also provides the general output enabling functions on Bit D4, Bit D3, and Bit D2.

Table 24. CTRL3 Register Settings (Register 0x09)

Bits	Name	Description
D7	Reserved	Reserved, set to 0.
D6	ADCDLY	ADC delay mode. 0: normal mode, no delay. 1: delay mode. The primary and secondary measurements are delayed by 1000 µs, relative to each other, as dictated by Bit D5.
D5	ADCORDR	Sets the order of the ADC conversions in delay mode. 0: primary followed by secondary. 1: secondary followed by primary.
D4	GOE_CB	General output enable for cell balance. 0: disabled (default). 1: enabled.
D3	GOE_OSS	General output enable for open input sense on secondary path. 0: disabled. 1: enabled.
D2	GOE_OSP	General output enable for open input sense on primary path. 0: disabled. 1: enabled.
[D1:D0]	IN_SNSE	Selection of input sense function. These bits determine which outputs are turned on for the duration of the sense signal. 00: function off. 01: cell balance sense active. 10: primary open input sense active. 11: secondary open input sense active.

Control Register 4

The master device ID bits, Bits[D6:D2] in Control Register 4 (CTRL4), can configure the devices with unique IDs in a single daisy chain with the master having an address settable between 0 and 30. An address of 31 (0x1F) is not allowed by either master or slave and, if attempted, is ignored, with the existing address being kept. In the event the master is assigned an address of 30, any following slaves are assigned 0, 1, 2, and so on. Address 31 is reserved for the address all command and is not assigned to any single device.

On power-on, the user can configure the device IDs by first writing the appropriate ID to Bits[D6:D2] of the master device. These bits are set to zero by default.

Analog Devices, Inc., recommends programming the master device with an address other than 0 so that if a POR event occurs, it is detectable due to the master address reverting back to 0 on a reset.

Asserting Bit D0 (the device ID increment bit) initiates the device ID setup process, which assigns an ID to the devices in the chain that are incremented from the master ID. After the ID process completes, D0 clears and Bit D1 (the device ID lock bit) is internally set. The user can read back from the control register of each device to confirm the device ID has locked. Unlock the device ID by writing a 0 to D1; keep the device ID locked by writing 1 to D1 on any subsequent writes.

Bits[D0:D1] are mutually exclusive and, in the event that both bits are set in one command, the device ID lock bit, Bit D1, takes precedence over the increment bit, and the device does not start the increment sequence.

The device ID bits written to the control register of the master device are directly used as that device ID. The slave device IDs are stored in a different register. A readback of the control register of any slave device returns the master device ID. The actual device ID is the first five bits of each 32-bit SDO frame.

A 25 µs delay per device is required between initiating the device ID setup process and a new register write command. The device ID is not cleared by a software reset.

Table 25. CTRL4 Register Settings (Register 0x0A)

Bits	Name	Description
D7	Reserved	Reserved.
D6	DEVID, Bit 4	Master device ID, Bit 4.
D5	DEVID, Bit 3	Master device ID, Bit 3.
D4	DEVID, Bit 2	Master device ID, Bit 2.
D3	DEVID, Bit 1	Master device ID, Bit 1.
D2	DEVID, Bit 0	Master device ID, Bit 0.
D1	DEVIDLOCK	Device ID lock. Read this bit to check if device ID has locked. 0: device is not locked to its device address. If no device address is received, the device continues to operate with default device address, 0x0. 1: device is locked to its device address. It is set automatically by the device when the device ID setup is complete.
D0	DEVIDINC	Device ID increment. 0: do not initialize the assign ID setup process. 1: initialize the device ID setup process. Assigns and auto increments the device ID for all devices discovered on the daisy chain.

Cell Balance Control Register

The cell balance control (CBCTRL) register determines the state of each of the cell balance outputs (CB1 to CB8) individually. The default value of the cell balance control register on power-up is 0x00, and the cell balance outputs are off.

Table 26. CBCTRL Register Settings (Register 0x0B)

Bits	Name	Description
D7	CB8	This bit sets the CB8 output. 0: output off. 1: output on.
D6	CB7	This bit sets the CB7 output. 0: output off. 1: output on.
D5	CB6	This bit sets the CB6 output. 0: output off. 1: output on.
D4	CB5	This bit sets the CB5 output. 0: output off. 1: output on.
D3	CB4	This bit sets the CB4 output. 0: output off. 1: output on.
D2	CB3	This bit sets the CB3 output. 0: output off. 1: output on.
D1	CB2	This bit sets the CB2 output. 0: output off. 1: output on.
D0	CB1	This bit sets the CB1 output. 0: output off. 1: output on.

OIS Control Registers

The OIS control registers (OISCTRL and OISGPOP) control the switching of a current into each analog voltage input (100 µA). The nine OISx outputs can be individually enabled by setting an appropriate bit in the OIS control registers. Setting a bit to Logic 1 enables the current in conjunction with the open input sense GOE bits (D2 or D3), as detailed in Table 24.

Table 27. OISCTRL Register Settings (Register 0x0E)

Bits	Name	Description
D7	OIS8	OIS 8 control. Set this bit to 1 to pull current from either VPIN8 or VSIN8, depending on the CTRL3 setting, to V_{SS}.
D6	OIS7	OIS 7 control. Set this bit to 1 to pull current from Pin VPIN7 or Pin VSIN7 , depending on the CTRL3 setting, to V_{SS}.
D5	OIS6	OIS 6 control. Set this bit to 1 to pull current from Pin VPIN6 or Pin VSIN6, depending on the CTRL3 setting, to V_{SS}.
D4	OIS5	OIS 5 control. Set this bit to 1 to pull current from Pin VPIN5 or Pin VSIN5, depending on the CTRL3 setting, to V_{SS}.
D3	OIS4	OIS 4 control. Set this bit to 1 to pull current from Pin VPIN4 or Pin VSIN4, depending on the CTRL3 setting, to V_{SS}.
D2	OIS3	OIS 3 control. Set this bit to 1 to pull current from Pin VPIN3 or Pin VSIN3, depending on the CTRL3 setting, to V_{SS}.
D1	OIS2	OIS 2 control. Set this bit to 1 to pull current from Pin VPIN2 or VSIN2, depending on the CTRL3 setting, to V_{SS}.
D0	OIS1	OIS 1 control. Set this bit to 1 to pull current from Pin VPIN1 or Pin VSIN1, depending on the CTRL3 setting, to V_{SS}.

Table 28. OISGPOP Register Settings (Register 0x0F)

Bits	Name	Description
D7	OIS0	OIS 0 control. Set this bit to 1 to pull current from AV_{CC}.
[D6:D3]	Reserved	Reserved.
D2	GPOP2	User defined General-Purpose Output Signal 2.
D1	GPOP1	User defined General-Purpose Output Signal 1.
D0	GPOP SEL	GPOPx configuration. 0: user defined GPOPx. 1: GPOPx pins configured for daisy-chain debug, see the Daisy-Chain Debug Mode section for further details.

Power-Down Timer Register

The power-down timer (PDT) register allows the user to configure a set time after which the AD7284 is powered down. The AD7284 allows the user to set the power-down timer to a value from 0 hours to 8.5 hours (510 minutes, maximum). The resolution of the power-down timer is 2 minutes. When using the power-down timer in conjunction with the CBx timers, it is recommended that the value programmed to the power-down timer exceed the time programmed to the CBx timer by at least 2 minutes because the power-down timer takes priority over the CBx timers and the device powers down. The default value of the power-down timer register on power-up is 0x00.

The power-down timer does not begin counting until the HWPD bit in Control Register 1 is set. Clearing the HWPD bit does not stop the power-down timer; stop the power-down timer by writing 0x00 to the register.

During a count, a new value can be written to the power-down timer register. This causes the power-down timer to restart and count to the new value.

Table 29. PDT Register Setting (Register 0x10)

Bits	Name	Description
[D7:D0]	PD_T	LSB = 2 minutes. Selectable between 0x00 and 0xFF. The maximum value = 510 minutes.

CB Timer 1 to CB Timer 8 Registers

The CB Timer 1 to CB Timer 8 (CBT1 to CBT8) registers allow the user to program individual times for each of the eight cell balance outputs. The AD7284 allows the user to set the CBx timer to a value from 0 minutes to 8.5 hours. The resolution of the CBx timers is 2 minutes. The default value of the CBx timer registers on power-up is 0x00. When the CBx timer value is set to 0x00, the CBx timer is not activated; that is, the CBx outputs are all controlled by the contents of the cell balance register only.

Table 30. CBT1 Register to CBT8 Register Settings (Register 0x11 to Register 0x18)

Bits	Name	Description
[D7:D0]	CB_T	LSB = 2 minutes. Selectable between 0x00 and 0xFF. The maximum value is 510 minutes.

Watchdog Timer Register

The watchdog timer (WDT) register allows the user to configure a set time after which the AD7284 is automatically powered down if communications to the AD7284 is lost. The AD7284 allows the user to set the watchdog timer to a maximum value of 1040 ms with a resolution of 8.192 ms.

The default value of the watchdog timer register on power-up is 0x0C (98.304 ms).

Table 31. WDT Register Settings (Register 0x21)

Bits	Name	Description
D7	Reserved	Reserved; set this bit to 0.
[D6:D0]	WDT	LSB = 8.192 ms. Selectable between 0x00 and 0x7F. The maximum value is 1040 ms.

Watchdog Key Register

The watchdog key (WDKY) register allows the user to disable the watchdog timer. To disable the watchdog timer, write 0x00 to the watchdog timer register, then write 0x5A to the watchdog key register, and finally write 0x00 to the watchdog timer register. The default value of the watchdog key register on power-up is 0x00.

Table 32. WDKY Register Setting (Register 0x22)

Bits	Name	Description
[D7:D0]	WDKEY	Key = 0x5A

Storage Register 1 and Storage Register 2

Storage Register 1 and Storage Register 2 (STRG1 and STRG2) are available for user storage purposes. These registers are volatile.

Table 33. STRG1 Register Setting (Register 0x23)

Bits	Name	Description
[D7:D0]	STRG1	Storage Register 1

Table 34. STRG2 Register Setting (Register 0x24)

Bits	Name	Description
[D7:D0]	STRG2	Storage Register 2

REGISTERS COMMON TO PAGE 0 AND PAGE 1

Page Register

The page (page) register can be written to independently of the current page selection.

Read Register

The read (RDREG) register defines the read operation of the AD7284. The read register can be written to independently of the page addressing. To read back a register from a chain of AD7284 devices, first write the desired register to the read register on all devices. Issue a null write command (0x00000000) per device to read back the register contents of each device in the daisy chain. The readback starts with the master device, then the first slave device, and so on. The read register is not used for reading back conversion results. See the Example 5: Convert and Read All Conversion Data section for more details. The default value of the read register on power-up is 0xFF.

EXAMPLES OF INTERFACING WITH THE AD7284

REGISTER WRITE AND REGISTER READ OPERATIONS EXAMPLES

In this section, Example 1 and Example 3 illustrate register write operations. Example 2 illustrates a register read operation.

Example 1: Initialize All Devices in a Daisy Chain

See Table 35. By default, the device ID on the AD7284 is 0. This example demonstrates how to set the master ID to 2 and to increment the device ID of slaves up the chain. Changing the master device ID allows identification of each device in a system containing more than one master.

1. Write 1. Write 0x01 to the page register on all devices to give access to Control Register 4 in Page 1. The 32-bit write command is 0xFFE013B2.
2. Write 2. Write to the Control Register 4 at Address 0x0A. Set the master ID and increment the IDs up the chain. The master ID is set by writing a 5-bit code to Bits[D6:D2] (0x02 in this example). Set the device increment bit (D0) to 1 and the device lock bit (D1) to 0. The 32-bit write command is 0xFCA0983D.

Example 2: Reading the Device ID

See Table 36. This sequence is similar for any register read operation. To verify the device IDs are set and locked, take the following steps to read Control Register 4:

1. Write 1. Write 0x01 to the page register on all devices to give access to Control Register 4 in Page 1. The 32-bit write command is 0xFFE013B2.
2. Write 2. Write 0x0A into the read register (the address corresponding to Control Register 4). The 32-bit write command is 0xFBF0A43F. The write/write, read bit must be 0.
3. Write 3. Apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each slave in the chain to be read back. Verify in the register data field that the device ID is locked for each device in the daisy chain by ensuring Bit D1 (the device ID lock bit) is set high on each Control Register 4 readback. Also, in this example, a device ID of 2 is returned for the master device signified by the first five bits, a device ID of three for the first slave device by the first five bits, and so on. The 32-bit write command is 0x00000000. In Table 36, n is the number of devices in the chain.

Table 35. Example 1: Initializing All Devices in a Daisy Chain

Write Command	Device Address	Write/Write, Read	Register Address	Data	12-Bit CRC	32-Bit Write Command
Write 1	11111	1	111110	00000001	001110110010	0xFFE013B2
Write 2	11111	1	001010	00001001	100000111101	0xFCA0983D

Table 36. Example 2: Reading the Device ID for a Chain of Devices

Write Command	Device Address	Write/Write, Read	Register Address	Data	12-Bit CRC	32-Bit Write Command
Write 1	11111	1	111110	00000001	001110110010	0xFFE013B2
Write 2	11111	0	111111	00001010	010000111111	0xFBF0A43F
Write 3 (×n)	00000	0	000000	00000000	000000000000	0x00000000

Example 3: Disabling the Watchdog Timer

See Table 37.

1. Write 1. Write 0x01 to the page register on all devices to give access to the watchdog timer registers in Page 1. The 32-bit write command is 0xFFE013B2.
2. Write 2. To start the watchdog timer disable routine, write 0x00 to the watchdog timer register. The 32-bit write command is 0xFE100F8E.
3. Write 3. Write the correct key value, 0x5A, to the watchdog key register. The 32-bit write command is 0xFE25A8DC.
4. Write 4. Complete the routine by writing 0x00 to the watchdog timer register. The 32-bit write command is 0xFE100F8E.

CONVERSION DATA READBACK OPERATION EXAMPLES

Example 4: Convert and Read Primary Conversion Data

See Table 38.

1. Write 1. Write Data 0x00 to the page register on all devices. The 32-bit write command is 0xFFE00531.
2. Write 2. Initiate conversions through the software convert start bit by asserting the LSB of the ADC functional control register. The 32-bit write command is 0xFFD01420. Allow sufficient time for all conversions to be completed, as described in the Converting with a Chain of AD7284 Devices section. Note that, after conversions are initiated, the device automatically enters 64-bit read mode and remains in 64-bit mode until commanded to exit.
3. Write 3. Following the completion of all conversions, apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each primary conversion result to be read back. For a daisy chain of three devices with 18 primary measurements on each device, this equates to 54 frames in total. All frames, except the last one, input a 32-bit write command of 0x00000000. In the table, n is the number of devices in the chain.
4. Write 4. The last frame (the 54th frame for a daisy chain of three devices) inputs 0xFFD04E2C. This command writes the value of 0x04 to the ADC functional control register, returning the interface protocol back to 32-bit mode such that the devices are ready to receive configuration changes or further software convert start requests.

Table 37. Example 3: Disabling the Watchdog Timer

Write Command	Device Address	Write/Write, Read	Register Address	Data	12-Bit CRC	32-Bit Write Command
Write 1	11111	1	111110	00000001	001110110010	0xFFE013B2
Write 2	11111	1	100001	00000000	111110001110	0xFE100F8E
Write 3	11111	1	100010	01011010	100011011100	0xFE25A8DC
Write 4	11111	1	100001	00000000	111110001110	0xFE100F8E

Table 38. Example 4: Convert and Read Primary Conversion Data

Write Command	Device Address	Write/Write, Read	Register Address	Data	12-Bit CRC	32-Bit Write Command
Write 1	11111	1	111110	00000000	010100110001	0xFFE00531
Write 2	11111	1	111101	00000001	010000100000	0xFFD01420
Write $3 \times (n \times 18) - 1$	00000	0	000000	00000000	000000000000	0x00000000
Write 4	11111	1	111101	00000100	111000101100	0xFFD04E2C

Example 5: Convert and Read All Conversion Data

See Table 39.

1. Write 1. Write Data 0x00 to the page register on all devices. The 32-bit write command is 0xFFE00531.
2. Write 2. Initiate conversions through the software convert start bit by asserting the LSB of the ADC functional control register. The 32-bit write command is 0xFFD01420. Allow sufficient time for all conversions to be completed as described in the Converting with a Chain of AD7284 Devices section. Note that, after conversions are initiated, the device automatically enters 64-bit read mode and remains in 64-bit mode until commanded to exit.
3. Write 3. Following the completion of all conversions, apply a $\overline{CS}$ low pulse that frames 32 SCLKs for each primary and secondary conversion result to be read back. For a single device, with 18 primary and 10 secondary measurements, this equates to 28 frames in total. All frames, except for the 18th and 28th, input the 32-bit write command of 0x00000000. For a daisy chain of three devices with 18 primary and 10 secondary measurements on each device, this equates to 84 frames in total. In this case, all frames, except for the 54th and 84th, input a 32-bit write command of 0x00000000.
4. Write 4. During the last primary readback frame, input 0xFFD02FA5. This command writes the value of 0x02 to the ADC functional control register, selecting the secondary conversion data results. For a single device, this is the 18th frame. For a daisy chain of three devices, this is the 54th frame.
5. Write 5. During the last secondary read back frame, write 0xFFD04E2C. This command writes the value of 0x04 to the ADC functional control register, returning the interface protocol back to 32-bit mode such that the devices are ready to receive configuration changes or further software convert start requests. For a single device, this is the 28th frame. For a daisy chain of three devices, this is the 84th frame.

Table 39. Example 5: Convert and Read All Conversion Data

Write Command	Device Address	Write/Write-Read	Register Address	Data	12-Bit CRC	32-Bit Write Command
Write 1	11111	1	111110	00000000	010100110001	0xFFE00531
Write 2	11111	1	111101	00000001	010000100000	0xFFD01420
Write $3 \times (n \times 18) - 1$	00000	0	000000	00000000	000000000000	0x00000000
Write 4	11111	1	111101	00000010	111110100101	0xFFD02FA5
Write $3 \times (n \times 10) - 1$	00000	0	000000	00000000	000000000000	0x00000000
Write 5	11111	1	111101	00000100	111000101100	0xFFD04E2C

APPLICATIONS INFORMATION

The AD7284 can be used in many different system architectures, from a system with a single device, to a chain of devices connected with or without transformers, multiple devices on one board, or single devices on multiple boards. Each of these system architectures present different external components requirements.

TYPICAL CONNECTION DIAGRAMS

This section summarizes the different hardware recommendations from the previous sections, presents a typical diagram for a single device, and a typical diagram for a chain of three devices on separate boards.

Master Only

Figure 41 shows an example of components for a master device, monitoring eight cells using two independent filters (on the primary and secondary path), and monitoring temperature on four thermistors.

The following notes refer to the notes detailed in Figure 41 and Figure 42:

1. A 100 nF decoupling capacitor placed close to the battery cell connector.
2. A transient protection, rated appropriately, capable of limiting the voltage at the device to within the absolute maximum ratings.
3. Ferrite bead to filter supply noise. Typically, 1 kΩ ferrite (100 MHz) is recommend in the V_{DD} path. If a ferrite is required in the V_{SS} line, it is recommended to use a value <100 Ω (100 MHz). This note applies to the master or slave configurations. See Note 11 in Figure 41 and see Note 3 in Figure 42.
4. Current limiting resistor between 10 Ω and 40 Ω. This resistor also acts as a low-pass filter in conjunction with the decoupling capacitance on the V_{DD} pin. Take care with regard to the time constant of this filter, as described in the Cell Connections section.
5. Decoupling capacitors; 100 nF in parallel with 4.7 µF in total or 100 nF in parallel with 2.2 µF on each V_{DD} pin.
6. Primary path input filters comprised of R_F and C_F typically have values between 330 Ω to 1 kΩ and 100 nF to 1 µF.
7. 10 kΩ to protect the CBx pins and gate of the external cell balancing transistors during the initial connection of the monitoring circuitry to the battery stack.
8. Secondary path input filters comprised of R_F and C_F typically have values between 330 Ω to 1 kΩ and 100 nF to 1 µF.
9. Daisy-chain upper port is unused and terminated with 50 Ω.
10. Daisy-chain lower port is unused and connected to V_{SS} via a 1 kΩ resistor.

Note that the 1 µF capacitor on V_{DRIVE} shown in Figure 41 is an ADuM5401 requirement. It is recommended to add 100 nF decoupling on the V_{DRIVE} pin.

Three Devices on Separate Boards

Li-Ion battery applications require a significant number of individual cells to provide the required output voltage. Figure 42 shows the recommended configuration of a chain of AD7284 devices monitoring a larger battery stack. The daisy-chain interface of the AD7284 allows each AD7284 to communicate with the AD7284 immediately above and below it. The daisy-chain interface allows the AD7284 devices to be electrically connected to the battery management device without the need for individual isolation devices between each AD7284. One AD7284 acts as the master device, interfacing through the standard SPI interface to the host processor and to the chain of connected slave devices.

Figure 42 shows how a chain of three devices can be configured to operate on individual boards, if required; the same configuration can be used if all devices are mounted on the same board.

In general, Analog Devices recommends placing two to three AD7284 devices on a single board with a transformer coupling making the connection between boards.

More details on external components requirements are covered in the Daisy-Chain Interface section, the Hot Plug section, and the Service Disconnect (SD) section.

Note that external components are subject to change.

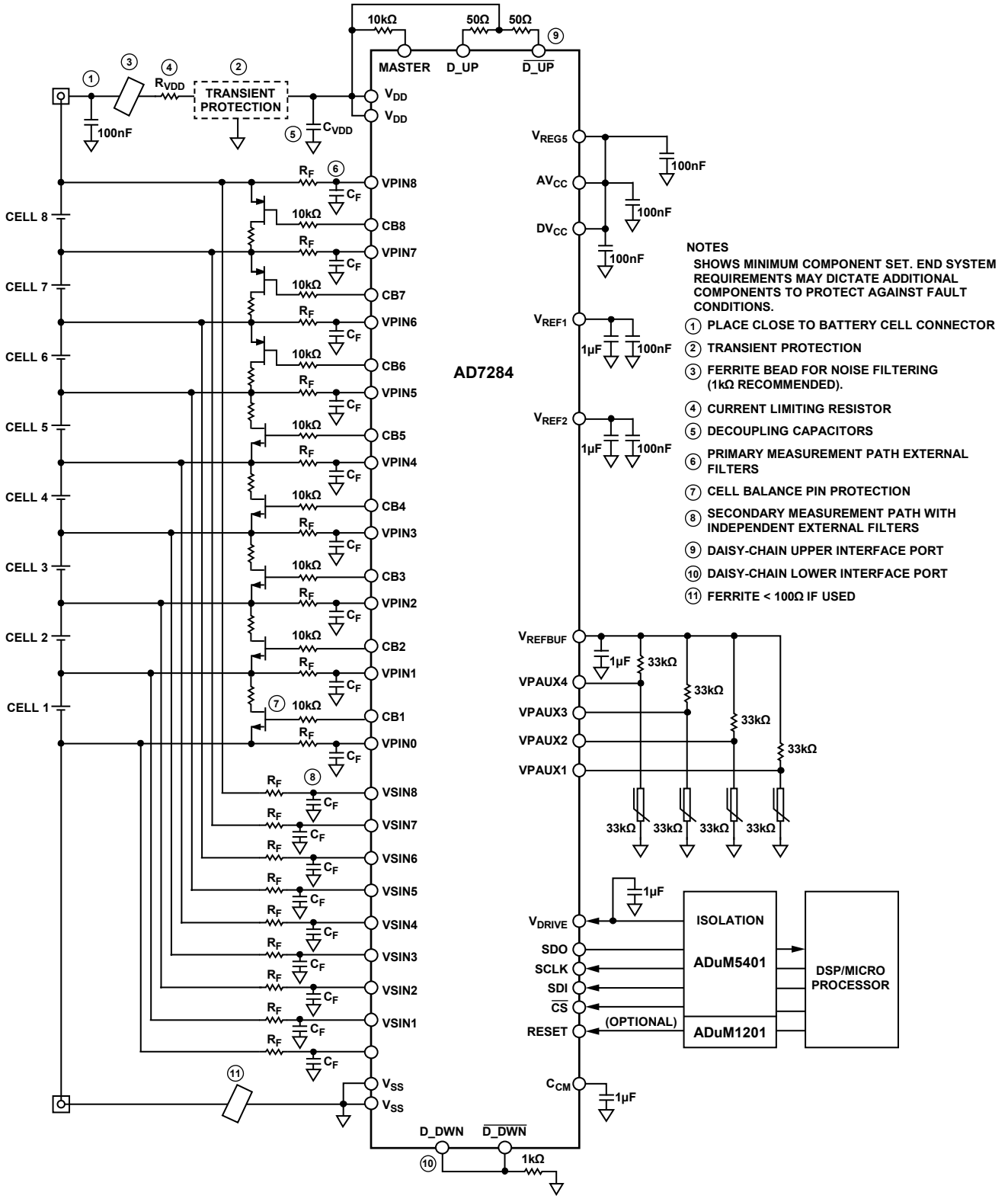


Figure 41. AD7284 Master Configuration Diagram for Eight Battery Cells

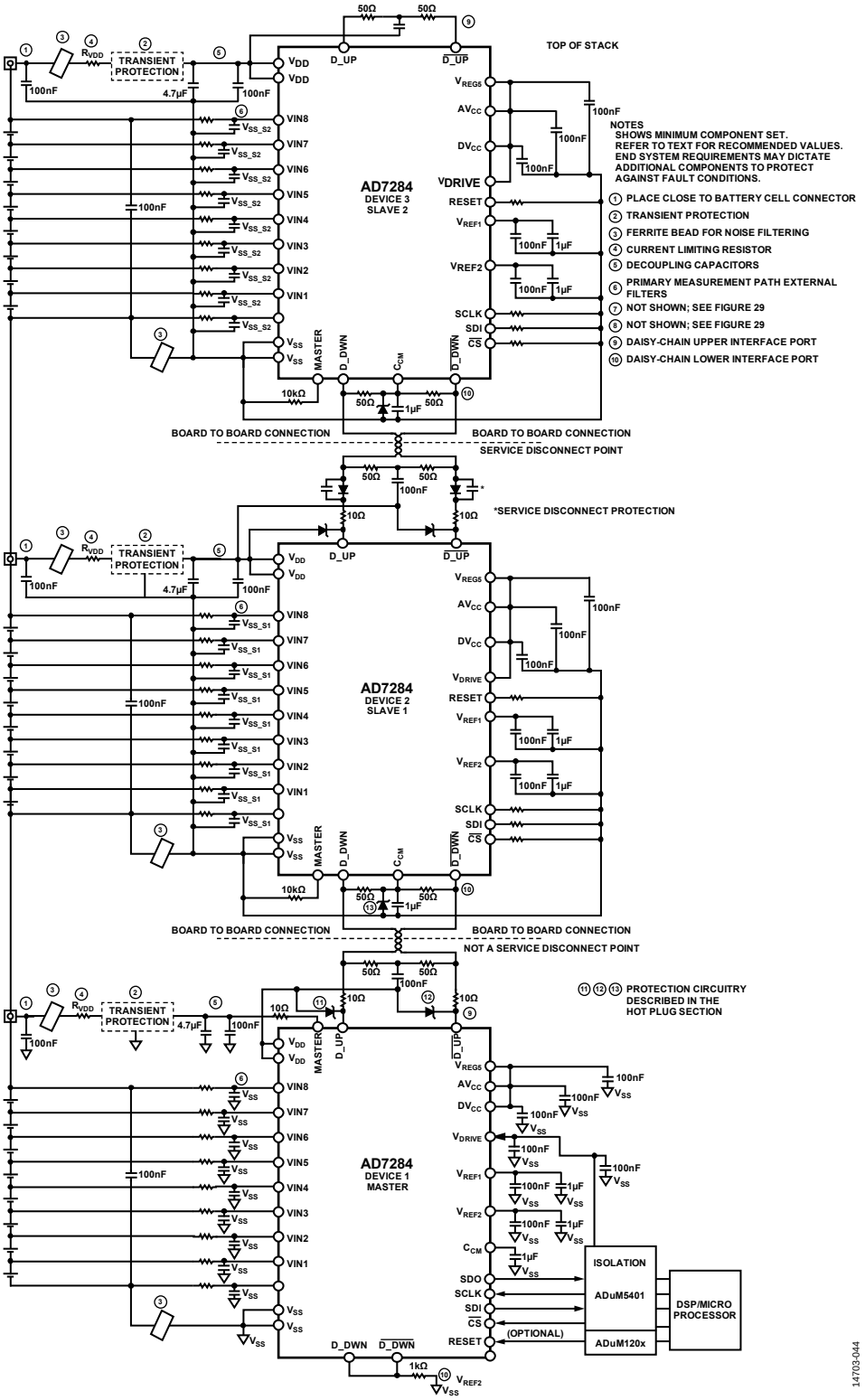


Figure 42. AD7284 Daisy-Chain Configuration with Three Devices, Where All Devices are on Separate Boards

HOT PLUG

A typical battery stack can have voltages in the range of 12 V to 400 V. For applications requiring flexibility in the order of connections of a daisy-chain interface, battery voltage, and battery stack connections, some additional external components are recommended at the board to board connection points to protect the AD7284 devices.

A protection diode placed across the supplies of each AD7284 acts to clamp the voltage across the device during initial connection to the battery stack, preventing an overvoltage damaging the AD7284. A clamp voltage rating of 40 V is suggested for these diodes, but lower values can also be used to suit the application where smaller cell counts are used. The diodes must limit the voltage to maximum of 48 V (AD7284 absolute maximum rating on V_{DD}). The Zener diode must withstand the voltage of the full stack.

Figure 43 shows the types of external components involved and includes low capacitance protection diodes (D1 and D2) to clamp the daisy-chain pin voltages close to the supply rails, and 10 Ω series resistors (R1 and R2) to limit current protecting the diodes. The daisy-chain pins can support capacitive loads up to 200 pF, typical. In addition, the D3 diode clamps the voltage on the C_{CM} pin.

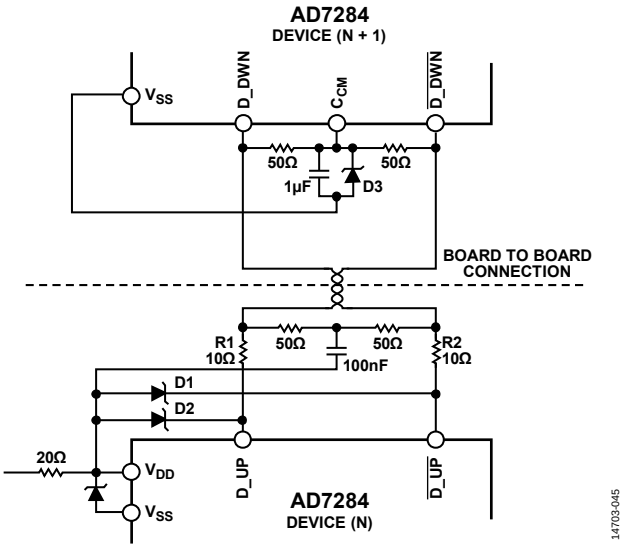


Figure 43. Suggested Hot Plug Components (Additional Circuitry Omitted for Clarity)

Other protection considerations are discussed in the Applications Information section, such as the inclusion of 1 kΩ resistors in series with the inputs, providing protection for the analog inputs in the event of an overvoltage or undervoltage on those inputs. At all times, ensure that the devices are not exposed to conditions outside the absolute maximum levels.

SERVICE DISCONNECT (SD)

At SD points, a series diode (SD diode) and small value parallel capacitor (3.9 nF) are necessary for each D_UP pin and $\overline{\text{D\_UP}}$ pin, as shown in Figure 44. Clamping diodes with low capacitance (pF) keep the daisy-chain pin voltages close to the supply rails. These components must be suitably rated to the stack voltage.

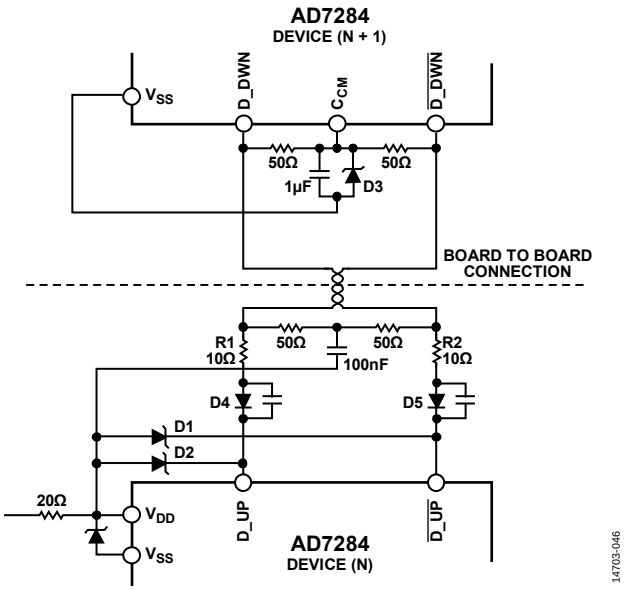


Figure 44. Suggested Hot Plug Components, Including Service Disconnect Components (Additional Circuitry Omitted for Clarity)

An alternative approach is to use transformers to provide isolation from device to device, which reduces some of the rating requirements on the external components.

TRANSFORMER CONFIGURATION

Figure 45 shows a typical configuration with transformers.

The center point of the isolated sides on the transformer can connect to the chassis or be left unconnected. If connected to the chassis, ESD protection diodes and an RC filter to filter noise from the chassis may be required.

R_T is the terminating resistor for the transformers; use values from 50 Ω to 200 Ω.

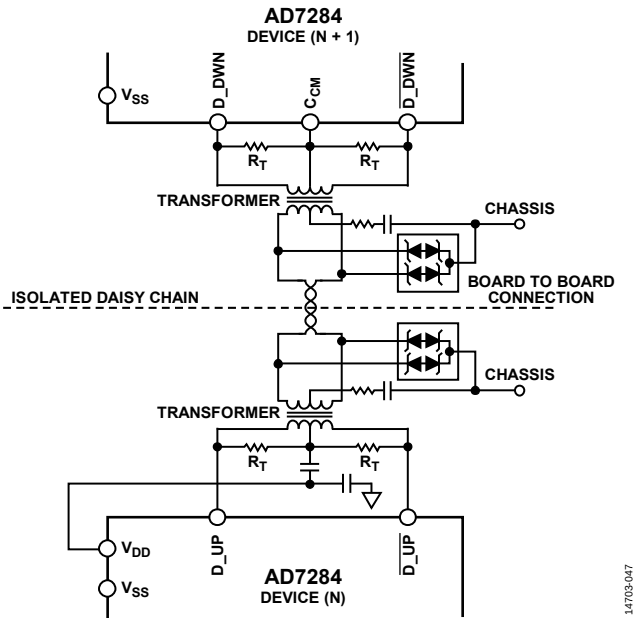


Figure 45. Transformer Configuration
(Additional Circuitry Omitted for Clarity)

OUTLINE DIMENSIONS

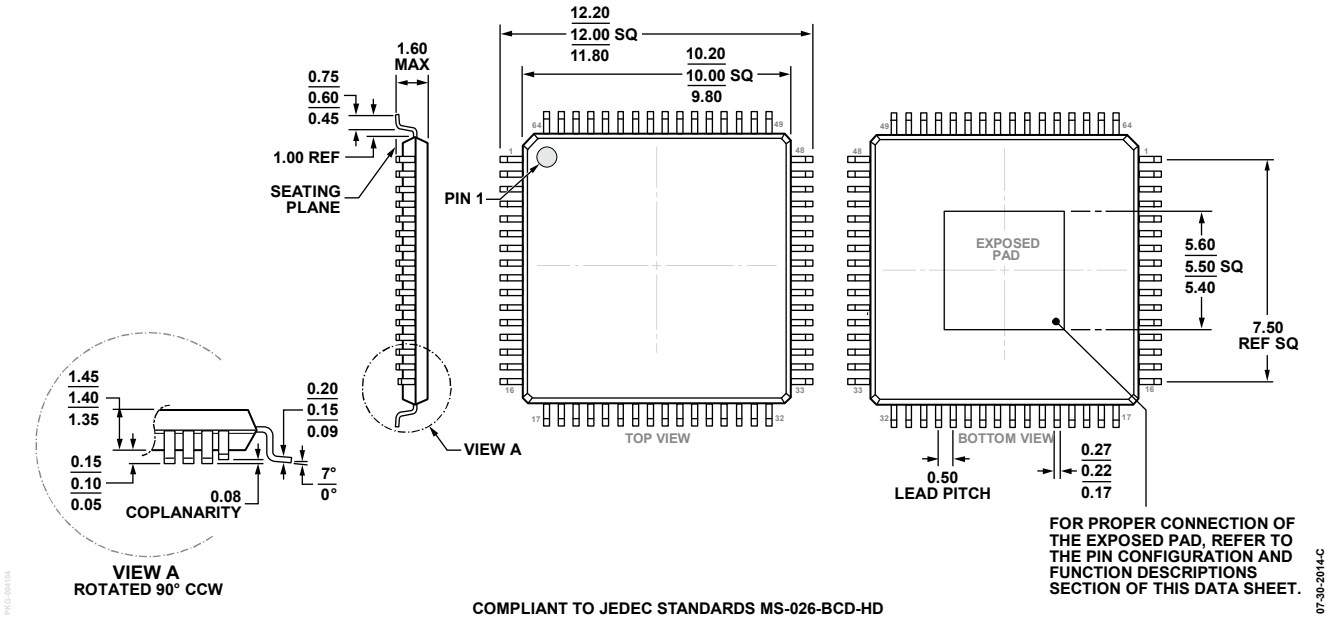


Figure 46. 64-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Junction Temperature Range	Package Description	Package Option
AD7284WBSWZ	−30°C to +120°C	64-Lead LQFP_EP with Exposed Pad, Tray	SW-64-2
AD7284WBSWZ-RL	−30°C to +120°C	64-Lead LQFP_EP with Exposed Pad, Tape and Reel	SW-64-2
EV-AD7284SSSDZ		Mini Transformer Isolated Slave Evaluation Kit	
EV-AD7284TMSDZ		Transformer Isolated Master Evaluation Kit	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD7284W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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