Octal, 12-/16-Bit *nano*DAC+ with 2 ppm/°C Reference, I²C Interface

Data Sheet

AD5671R/AD5675R

FEATURES

- **High performance**
  - **High relative accuracy (INL): ±3 LSB maximum at 16 bits**
  - **Total unadjusted error (TUE): ±0.14% of FSR maximum**
  - **Offset error: ±1.5 mV maximum**
  - **Gain error: ±0.06% of FSR maximum**
  - **Low drift 2.5 V reference: 2 ppm/°C typical**
- **Wide operating ranges**
  - **−40°C to +125°C temperature range**
  - **2.7 V to 5.5 V power supply**
- **Easy implementation**
  - **User selectable gain of 1 or 2 (GAIN pin/bit)**
  - **1.8 V logic compatibility**
- **400 kHz I²C-compatible serial interface**
- **20-lead, RoHS-compliant TSSOP and LFCSP**

APPLICATIONS

- **Optical transceivers**
- **Base station power amplifiers**
- **Process control (PLC input/output cards)**
- **Industrial automation**
- **Data acquisition systems**

GENERAL DESCRIPTION

The AD5671R/AD5675R are low power, octal, 12-/16-bit buffered voltage output digital-to-analog converters (DACs). They include a 2.5 V, 2 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design. The AD5671R/AD5675R are available in a 20-lead TSSOP and in a 20-lead LFCSP and incorporate a power-on reset circuit and a RSTSEL pin that ensures the DAC outputs power up to zero scale or midscale and remain there until a valid write. The AD5671R/AD5675R contain a power-down mode, reducing the current consumption to 1 µA typical while in power-down mode.

Table 1. Octal *nano*DAC+® Devices

Interface	Reference	16-Bit	12-Bit
SPI	Internal	AD5676R	AD5672R
	External	AD5676	Not applicable
I²C	Internal	AD5675R	AD5671R

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL)
   AD5671R (12-bit): ±1 LSB maximum
   AD5675R (16-bit): ±3 LSB maximum
2. Low Drift, 2.5 V On-Chip Reference

FUNCTIONAL BLOCK DIAGRAM

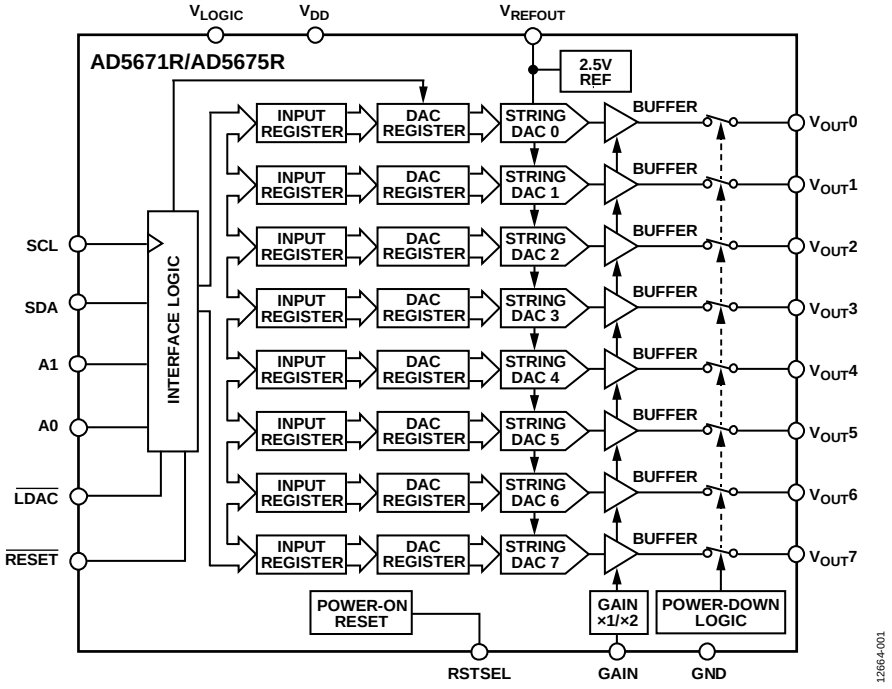

Figure 1.

Rev. C Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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10/2014—Revision 0: Initial Version

SPECIFICATIONS

AD5671R SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, resistive load (R_L) = 2 kΩ, capacitive load (C_L) = 200 pF, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	12			Bits	
Relative Accuracy (INL)		±0.12	±1	LSB	Gain = 1
		±0.12	±1	LSB	Gain = 2
Differential Nonlinearity (DNL)		±0.01	±0.1	LSB	Gain = 1
		±0.01	±0.1	LSB	Gain = 2
Zero Code Error		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error		−0.75	±2	mV	Gain = 1
		−0.1	±1.5	mV	Gain = 2
Full-Scale Error		−0.018	±0.14	% of full-scale range (FSR)	Gain = 1
		−0.013	±0.07	% of FSR	Gain = 2
Gain Error		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.06	% of FSR	Gain = 2
TUE		±0.03	±0.18	% of FSR	Gain = 1
		±0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift		±1		µV/°C	
DC Power Supply Rejection Ratio (PSRR)		0.25		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk		±2		µV	Due to single channel, full-scale output change
		±3		µV/mA	Due to load current change
		±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		2.5	V	Gain = 1
	0		5	V	Gain = 2
Output Current Drive (I_{OUT})			15	mA	
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 1 kΩ
Resistive Load[2]	1			kΩ	
Load Regulation		183		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −30 mA ≤ I_{OUT} ≤ +30 mA
		177		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[3]		40		mA	
Load Impedance at Rails[4]		25		Ω	
Power-Up Time		2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
REFERENCE OUTPUT					
Output Voltage[5]	2.4975		2.5025	V	
Reference Temperature Coefficient[6, 7]					See the Terminology section
20-Lead TSSOP		2	5	ppm/°C	
20-Lead LFCSP		5	10	ppm/°C	
Output Impedance		0.04		Ω	
Output Voltage Noise		13		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient, frequency (f) = 10 kHz, C_L = 10 nF, gain = 1 or 2
Load Regulation Sourcing		29		µV/mA	At ambient
Load Regulation Sinking		74		µV/mA	At ambient

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Current Load Capability		±20		mA	$V_{DD} \geq 3$ V
Line Regulation		43		µV/V	At ambient
Long-Term Stability/Drift		12		ppm	After 1000 hours at 125°C
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles
LOGIC INPUTS					
Input Current			±1	µA	Per pin
Input Voltage					
Low, V_{IL}			$0.3 \times V_{LOGIC}$	V	
High, V_{IH}	$0.7 \times V_{LOGIC}$			V	
Pin Capacitance		3		pF	
LOGIC OUTPUTS (SDA)					
Output Voltage					
Low, V_{OL}			0.4	V	I_{OL} = 200 µA
High, V_{OH}	$V_{LOGIC} - 0.4$			V	I_{OH} = −200 µA
Floating State Output Capacitance		4		pF	
POWER REQUIREMENTS					
V_{LOGIC}	1.62		5.5	V	
V_{LOGIC} Supply Current (I_{LOGIC})			3	µA	Power-on, −40°C + 105°C
			3	µA	Power-on, −40°C + 125°C
			3	µA	Power-down, −40°C + 105°C
			3	µA	Power-down, −40°C + 125°C
V_{DD}	2.7		5.5	V	Gain = 1
	$V_{REF} + 1.5$		5.5	V	Gain = 2
V_{DD} Supply Current (I_{DD})					$V_{IH} = V_{DD}$, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[8]		1.1	1.26	mA	Internal reference off, −40°C to +85°C
		1.8	2.0	mA	Internal reference on, −40°C to +85°C
		1.1	1.3	mA	Internal reference off
		1.8	2.1	mA	Internal reference on
All Power-Down Modes[9]		1	1.7	µA	Tristate to 1 kΩ, −40°C to +85°C
		1	1.7	µA	Power-down to 1 kΩ, −40°Cto +85°C
		1	2.5	µA	Tristate, −40°C to +105°C
		1	2.5	µA	Power-down to 1 kΩ, −40°C to +105°C
		1	5.5	µA	Tristate to 1 kΩ, −40°C to +125°C
		1	5.5	µA	Power-down to 1 kΩ, −40°C to +125°C

[1] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when the internal reference voltage (V_{REF}) = V_{DD} with gain = 1, or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 12 to 4080.
[2] Together, Channel 0, Channel 1, Channel 2, and Channel 3 can source/sink 40 mA. Similarly, together, Channel 4, Channel 5, Channel 6, and Channel 7 can source/sink 40 mA up to a junction temperature of 125°C.
[3] V_{DD} = 5 V. The devices include current limiting to protect the devices during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.
[4] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.
[5] Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See the Internal Reference and Amplifier Gain Selection section.
[6] Reference is trimmed and tested at two temperatures and is characterized from −40°C to +125°C.
[7] Reference temperature coefficient calculated as per the box method. See the Terminology section for further information.
[8] Interface inactive. All DACs active. DAC outputs unloaded.
[9] All DACs powered down.

AD5675R SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, R_L = 2 kΩ, C_L = 200 pF, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE[1]								
Resolution	16			16			Bits	
Relative Accuracy (INL)		±1.8	±8		±1.8	±3	LSB	Gain = 1
		±1.7	±8		±1.7	±3	LSB	Gain = 2
Differential Nonlinearity (DNL)		±0.7	±1		±0.7	±1	LSB	Gain = 1
		±0.5	±1		±0.5	±1	LSB	Gain = 2
Zero-Code Error		0.8	4		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error		−0.75	±6		−0.75	±2	mV	Gain = 1
		−0.1	±4		−0.1	±1.5	mV	Gain = 2
Full-Scale Error		−0.018	±0.28		−0.018	±0.14	% of FSR	Gain = 1
		−0.013	±0.14		−0.013	±0.07	% of FSR	Gain = 2
Gain Error		+0.04	±0.24		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.12		−0.02	±0.06	% of FSR	Gain = 2
TUE		±0.03	±0.3		±0.03	±0.18	% of FSR	Gain = 1
		±0.006	±0.25		±0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift		±1			±1		µV/°C	
DC PSRR		0.25			0.25		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk		±2			±2		µV	Due to single channel, full-scale output change
		±3			±3		µV/mA	Due to load current change
		±2			±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS								
Output Voltage Range	0		2.5	0		2.5	V	Gain = 1
	0		5	0		5	V	Gain = 2
Output Current Drive			15			15	mA	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 1 kΩ
Resistive Load[2]	1			1			kΩ	
Load Regulation		183			183		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −30 mA ≤ I_{OUT} ≤ +30 mA
		177			177		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[3]		40			40		mA	
Load Impedance at Rails[4]		25			25		Ω	
Power-Up Time		2.5			2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
REFERENCE OUTPUT								
Output Voltage[5]	2.4975		2.5025	2.4975		2.5025	V	
Reference Temperature Coefficient[6, 7]								See the Terminology section
20-Lead TSSOP		5	20		2	5	ppm/°C	
20-Lead LFCSP		5	20		2	10	ppm/°C	
Output Impedance		0.04			0.04		Ω	
Output Voltage Noise		13			13		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240			240		nV/√Hz	At ambient, f = 10 kHz, C_L = 10 nF, gain = 1 or 2
Load Regulation Sourcing		29			29		µV/mA	At ambient
Load Regulation Sinking		74			74		µV/mA	At ambient
Output Current Load Capability		±20			±20		mA	V_{DD} ≥ 3 V
Line Regulation		43			43		µV/V	At ambient

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
Long-Term Stability/Drift		12			12		ppm	After 1000 hours at 125°C
Thermal Hysteresis		125			125		ppm	First cycle
		25			25		ppm	Additional cycles
LOGIC INPUTS								
Input Current			±1			±1	μA	Per pin
Input Voltage								
Low, V_{INL}			0.3 × V_{LOGIC}			0.3 × V_{LOGIC}	V	
High, V_{INH}	0.7 × V_{LOGIC}			0.7 × V_{LOGIC}			V	
Pin Capacitance		3			3		pF	
LOGIC OUTPUTS (SDA)								
Output Voltage								
Low, V_{OL}			0.4			0.4	V	I_{SINK} = 200 μA
High, V_{OH}	V_{LOGIC} − 0.4			V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 μA
Floating State Output Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{LOGIC}	1.62		5.5	1.62		5.5	V	
I_{LOGIC}			3			3	μA	Power-on, −40°C + 105°C
			3			3	μA	Power-on, −40°C + 125°C
			3			3	μA	Power-down, −40°C + 105°C
			3			3	μA	Power-down, −40°C + 125°C
V_{DD}	2.7		5.5	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}								$V_{IH} = V_{DD}$, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[8]		1.1	1.26		1.1	1.26	mA	Internal reference off, −40°C to +85°C
		1.8	2.0		1.8	2.0	mA	Internal reference on, −40°C to +85°C
		1.1	1.3		1.1	1.3	mA	Internal reference off
		1.8	2.1		1.8	2.1	mA	Internal reference on
All Power-Down Modes[9]		1	1.7		1	1.7	μA	Tristate to 1 kΩ, −40°C to +85°C
		1	1.7		1	1.7	μA	Power-down to 1 kΩ, −40°C to +85°C
		1	2.5		1	2.5	μA	Tristate, −40°C to +105°C
		1	2.5		1	2.5	μA	Power-down to 1 kΩ, −40°C to +105°C
		1	5.5		1	5.5	μA	Tristate to 1 kΩ, −40°C to +125°C
		1	5.5		1	5.5	μA	Power-down to 1 kΩ, −40°C to +125°C

[1] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when $V_{REF} = V_{DD}$ with gain = 1, or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280.
[2] Together, Channel 0, Channel 1, Channel 2, and Channel 3 can source/sink 40 mA. Similarly, together, Channel 4, Channel 5, Channel 6, and Channel 7 can source/sink 40 mA up to a junction temperature of 125°C.
[3] V_{DD} = 5 V. The devices include current limiting to protect the devices during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.
[4] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.
[5] Initial accuracy presolder reflow is ±750 μV; output voltage includes the effects of preconditioning drift. See the Internal Reference and Amplifier Gain Selection section.
[6] Reference is trimmed and tested at two temperatures and is characterized from −40°C to +125°C.
[7] Reference temperature coefficient calculated as per the box method. See the Terminology section for further information.
[8] Interface inactive. All DACs active. DAC outputs unloaded.
[9] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
OUTPUT VOLTAGE SETTLING TIME[2]					
AD5671R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
AD5675R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
SLEW RATE		0.8		V/µs	
DIGITAL-TO-ANALOG GLITCH IMPULSE[2]		1.4		nV-sec	1 LSB change around major carry (internal reference, gain = 1)
DIGITAL FEEDTHROUGH[2]		0.13		nV-sec	
CROSSTALK[2]					
Digital		0.1		nV-sec	
Analog		−0.25		nV-sec	
		−1.3		nV-sec	Internal reference, gain = 2
DAC-to-DAC		−2.0		nV-sec	Internal reference, gain = 2
TOTAL HARMONIC DISTORTION (THD)[3]		−80		dB	At T_A, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
OUTPUT NOISE SPECTRAL DENSITY[2]		300		nV/√Hz	DAC code = midscale, 10 kHz; gain = 2
OUTPUT NOISE[2]		6		µV p-p	0.1 Hz to 10 Hz, gain = 1
SIGNAL-TO-NOISE RATIO (SNR)		90		dB	At T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SPURIOUS-FREE DYNAMIC RANGE (SFDR)		83		dB	At T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)		80		dB	At T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] The operating temperature range is −40°C to +125°C; T_A = 25°C.
[2] See the Terminology section. Measured using internal reference and gain = 1, unless otherwise noted.
[3] Digitally generated sine wave (f_{OUT}) at 1 kHz.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, all specifications −40°C to +125°C, unless otherwise noted.

Table 5.

Parameter[1]	Min	Max	Unit	Description
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD,STA}$, start/repeated start hold time
t_5	100		ns	$t_{SU,DAT}$, data setup time
t_6[2]	0	0.9	µs	$t_{HD,DAT}$, data hold time
t_7	0.6		µs	$t_{SU,STA}$, repeated start setup time
t_8	0.6		µs	$t_{SU,STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}[3]	0	300	ns	t_R, rise time of SCL and SDA when receiving
t_{11}[3]	20 + 0.1C_B	300	ns	t_F, fall time of SCL and SDA when transmitting/receiving
t_{12}	20		ns	$\overline{\text{LDAC}}$ pulse width
t_{13}	400		ns	SCL rising edge to $\overline{\text{LDAC}}$ rising edge
t_{14}	8		ns	$\overline{\text{RESET}}$ minimum pulse width low, 1.62 V ≤ V_{LOGIC} ≤ 2.7 V
	10		ns	$\overline{\text{RESET}}$ minimum pulse width low, 2.7 V ≤ V_{LOGIC} ≤ 5.5 V
t_{15}	90		ns	$\overline{\text{RESET}}$ activation time, 1.62 V ≤ V_{LOGIC} ≤ 2.7 V
	90		ns	$\overline{\text{RESET}}$ activation time, 2.7 V ≤ V_{LOGIC} ≤ 5.5 V
t_{SP}[4]	0	50	ns	Pulse width of suppressed spike
C_B		400	pF	Capacitive load for each bus line

[1] See Figure 2 and Figure 3.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the SCL falling edge.
[3] t_R and t_F are measured from 0.3 × V_{DD} to 0.7 × V_{DD}.
[4] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

Timing Diagrams

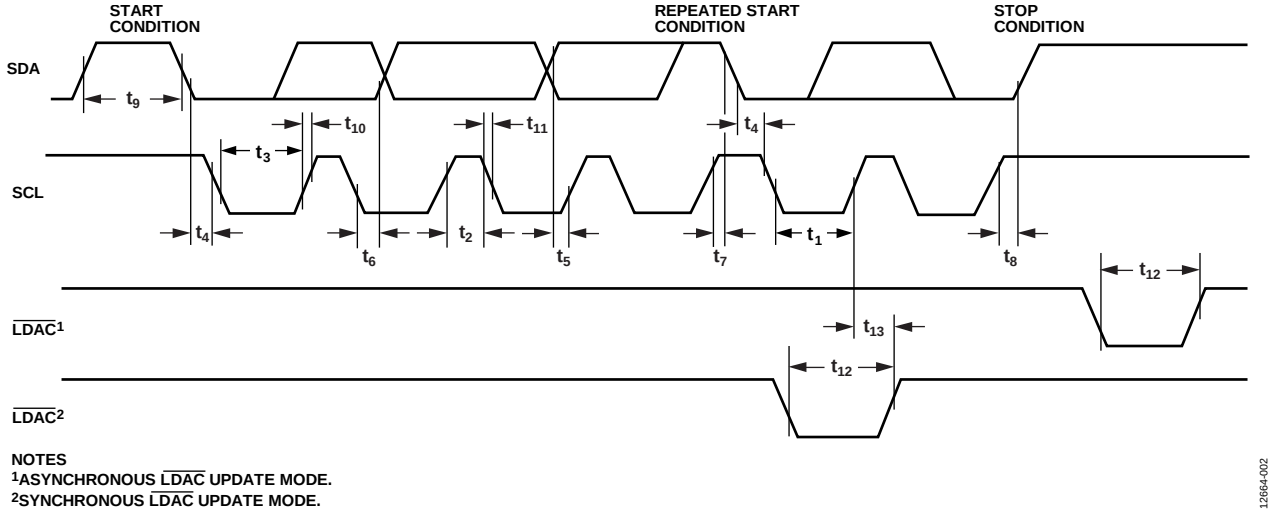


Figure 2. 2-Wire Serial Interface Timing Diagram

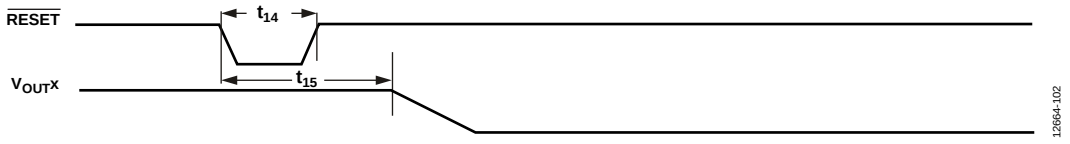


Figure 3. $\overline{\text{RESET}}$ Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT}x to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7.Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
20-Lead TSSOP (RU-20)[1]	98.65	44.39	17.58	1.77	43.9	°C/W
20-Lead LFCSP (CP-20-8)[2]	82	16.67	32.5	0.43	22	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51

[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

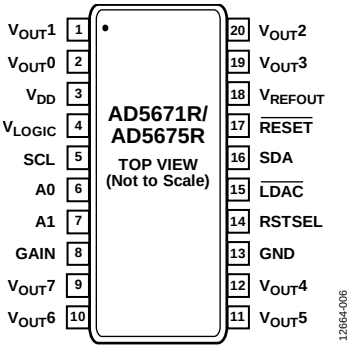


Figure 4. TSSOP Pin Configuration

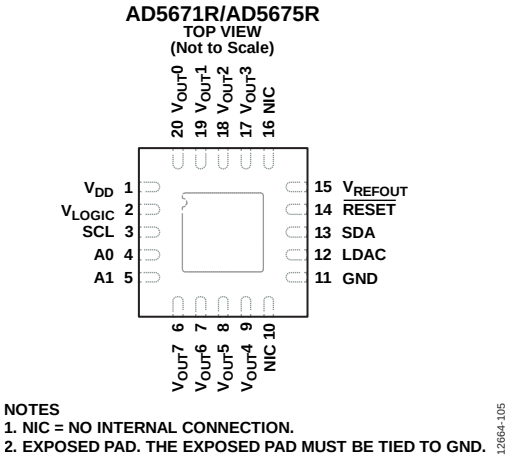


Figure 5. LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	$V_{OUT}1$	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
2	20	$V_{OUT}0$	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
N/A[1]	0	EPAD	Exposed Pad. The exposed pad must be tied to GND.
3	1	V_{DD}	Power Supply Input. These devices operate from 2.7 V to 5.5 V. Decouple the V_{DD} supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	2	V_{LOGIC}	Digital Power Supply. The voltage on this pin ranges from 1.62 V to 5.5 V.
5	3	SCL	Serial Clock Line. In conjunction with the SDA line, this pin clocks data into or out of the 24-bit input shift register.
6	4	A0	Address Input. Sets the first LSB of the 7-bit slave address.
7	5	A1	Address Input. Sets the second LSB of the 7-bit slave address.
8	N/A[1]	GAIN	Span Set Pin. When this pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}.
9	6	$V_{OUT}7$	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
10	7	$V_{OUT}6$	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
11	8	$V_{OUT}5$	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
12	9	$V_{OUT}4$	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
N/A[1]	10, 16	NIC	No Internal Connection.
13	11	GND	Ground Reference Point for All Circuitry on the Device.
14	N/A[1]	RSTSEL	Power-On Reset Pin. Tie this pin to GND to power up all eight DACs to zero scale. Tie this pin to V_{LOGIC} to power up all eight DACs to midscale. On models without RSTSEL, the outputs power up to zero scale.
15	12	$\overline{\text{LDAC}}$	Load DAC. $\overline{\text{LDAC}}$ operates in two modes, asynchronously and synchronously. Pulsing this pin low updates any or all DAC registers if the input registers have new data, which simultaneously updates all DAC outputs. This pin can also be tied permanently low.
16	13	SDA	Serial Data Input. In conjunction with the SCL line, this pin clocks data into or out of the 24-bit input shift register. SDA is a bidirectional, open-drain data line that must be pulled to the supply with an external pull-up resistor.
17	14	$\overline{\text{RESET}}$	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
18	15	V_{REFOUT}	Reference Output Voltage. When using the internal reference, this is the reference output pin. This pin is the reference output by default.
19	17	$V_{OUT}3$	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
20	18	$V_{OUT}2$	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

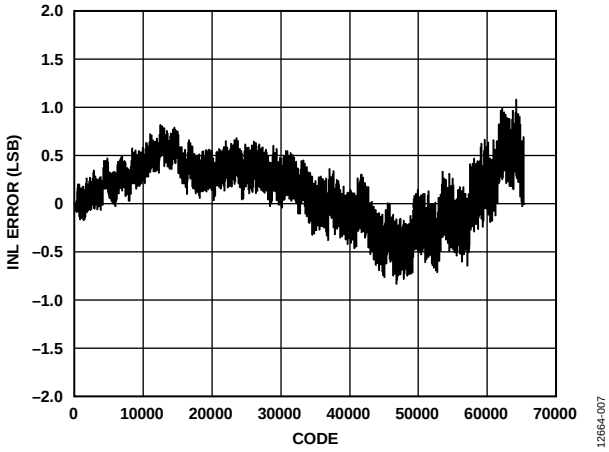


Figure 6. AD5675R INL Error vs. Code

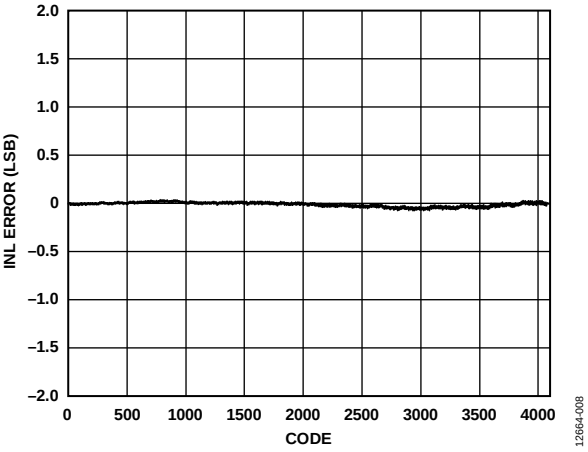


Figure 7. AD5671R INL Error vs. Code

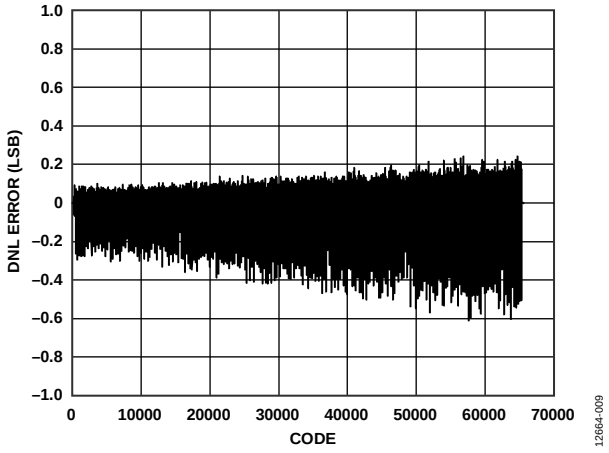


Figure 8. AD5675R DNL Error vs. Code

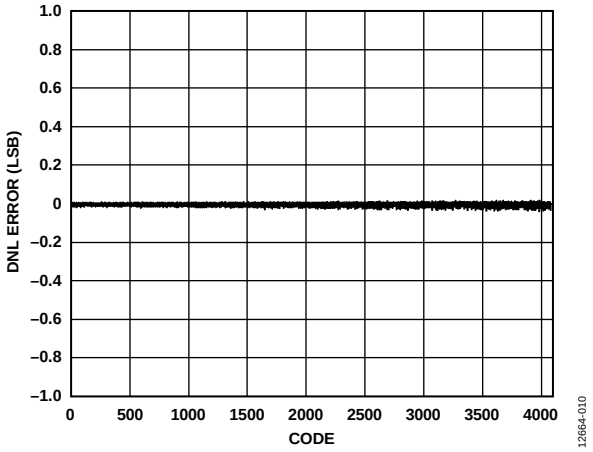


Figure 9. AD5671R DNL Error vs. Code

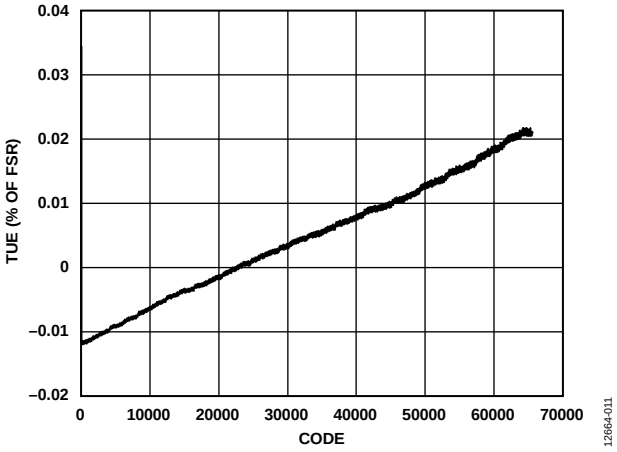


Figure 10. AD5675R TUE vs. Code

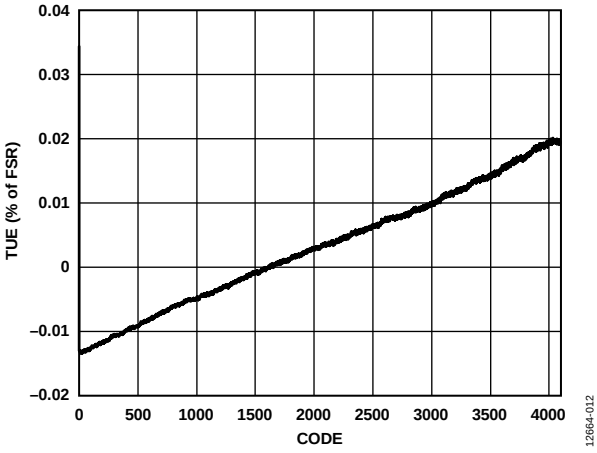


Figure 11. AD5671R TUE vs. Code

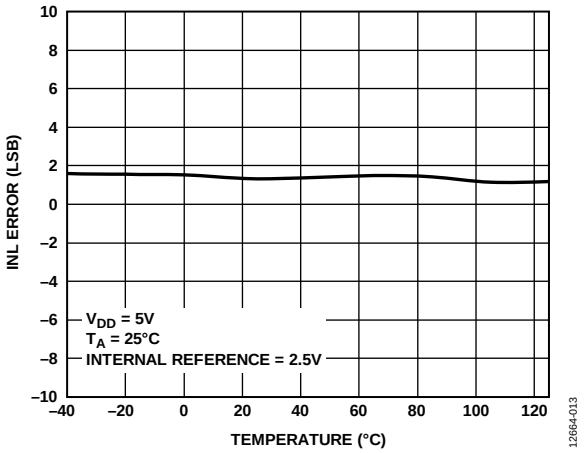


Figure 12. AD5675R INL Error vs. Temperature

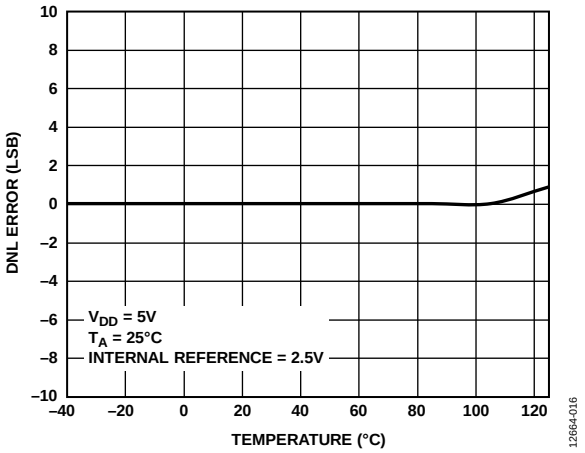


Figure 15. AD5671R DNL Error vs. Temperature

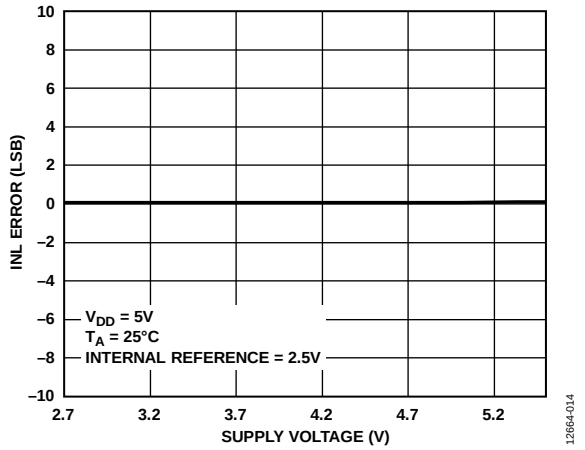


Figure 13. AD5671R INL Error vs. Supply Voltage

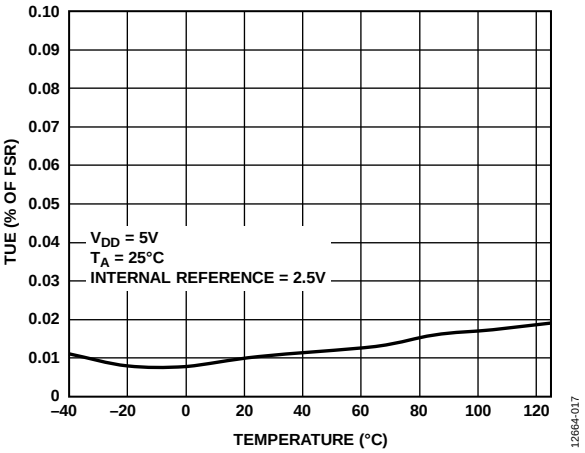


Figure 16. AD5675R TUE vs. Temperature

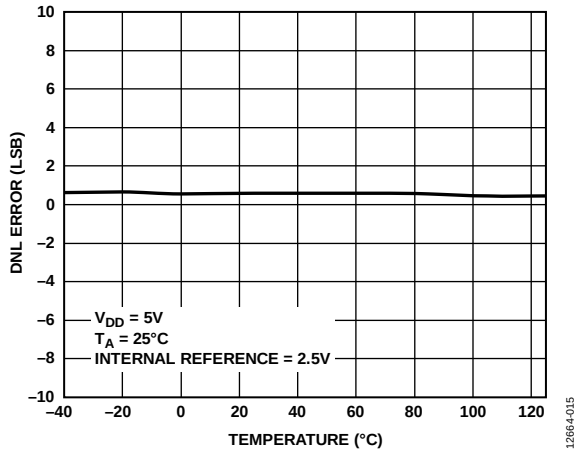


Figure 14. AD5675R DNL Error vs. Temperature

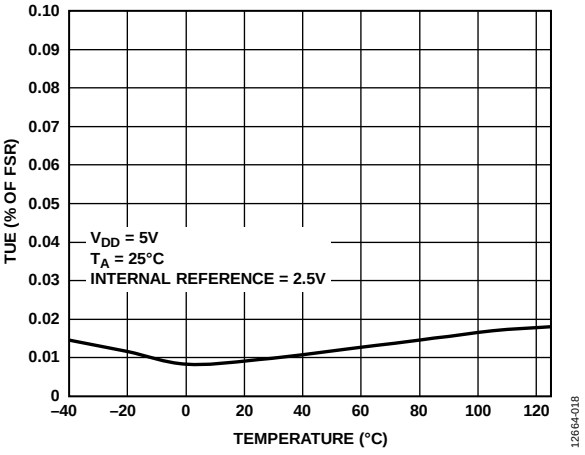


Figure 17. AD5671R TUE vs. Temperature

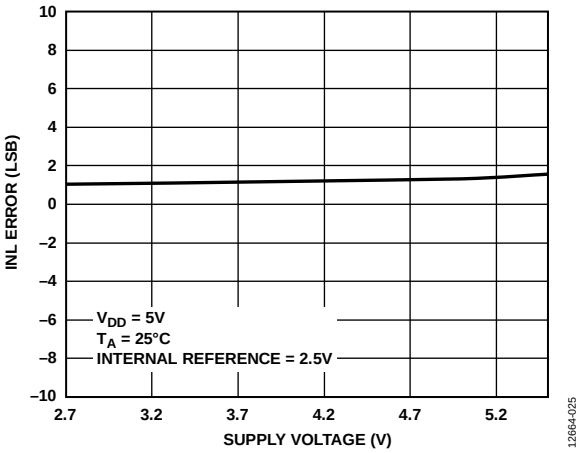


Figure 18. AD5675R INL Error vs. Supply Voltage

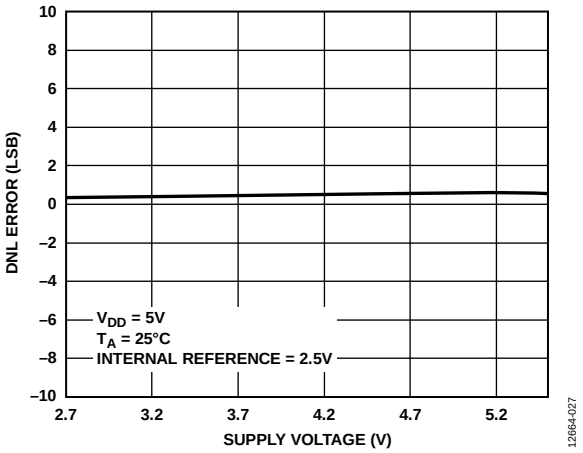


Figure 19. AD5675R DNL Error vs. Supply Voltage

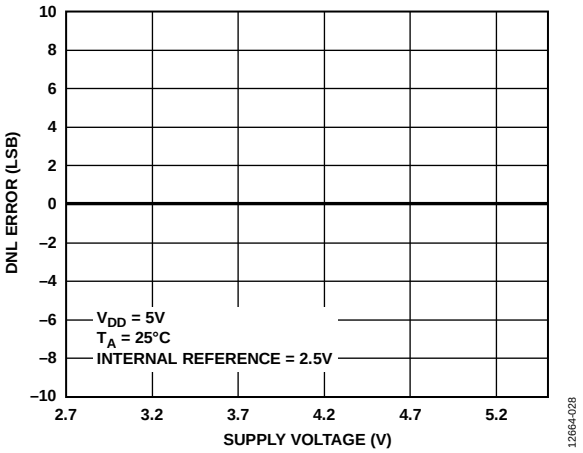


Figure 20. AD5671R DNL Error vs. Supply Voltage

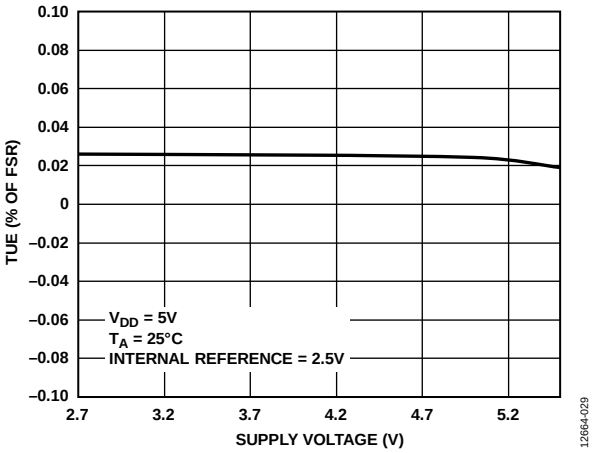


Figure 21. AD5675R TUE vs. Supply Voltage

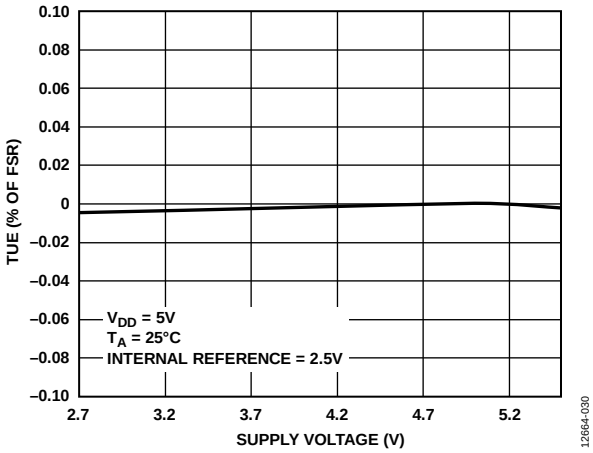


Figure 22. AD5671R TUE vs. Supply Voltage

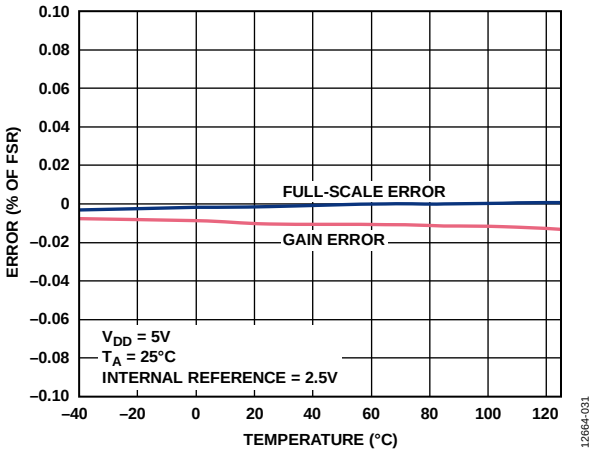


Figure 23. AD5675R Gain Error and Full-Scale Error vs. Temperature

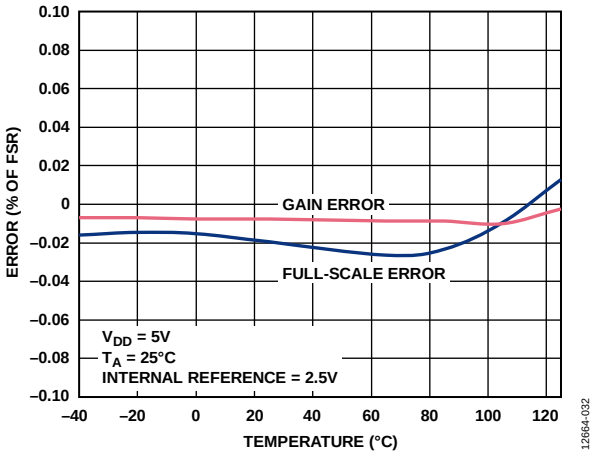


Figure 24. AD5671R Gain Error and Full-Scale Error vs. Temperature

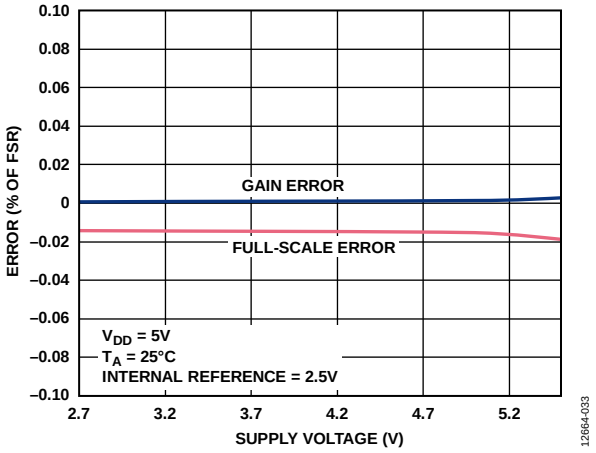


Figure 25. AD5675R Gain Error and Full-Scale Error vs. Supply Voltage

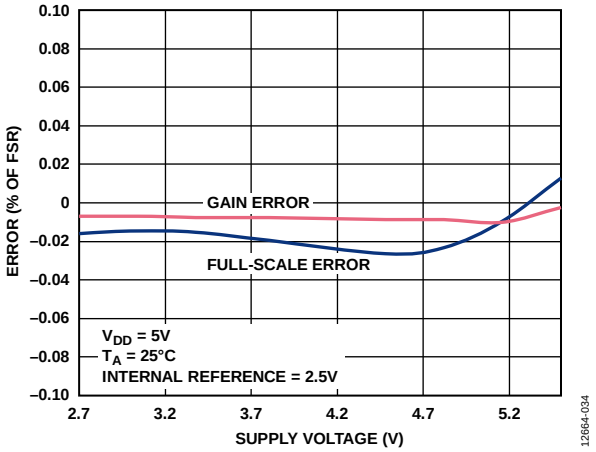


Figure 26. AD5671R Gain Error and Full-Scale Error vs. Supply Voltage

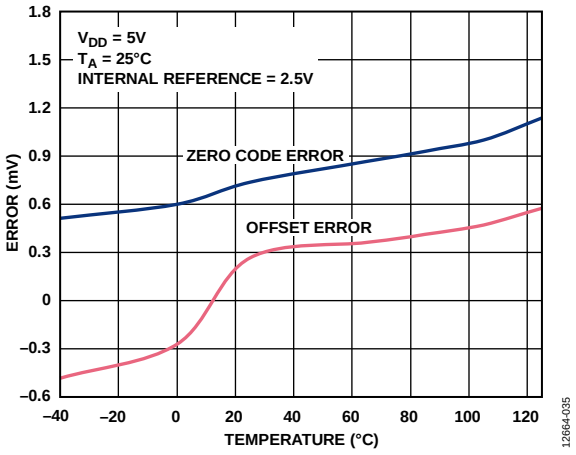


Figure 27. AD5675R Zero Code Error and Offset Error vs. Temperature

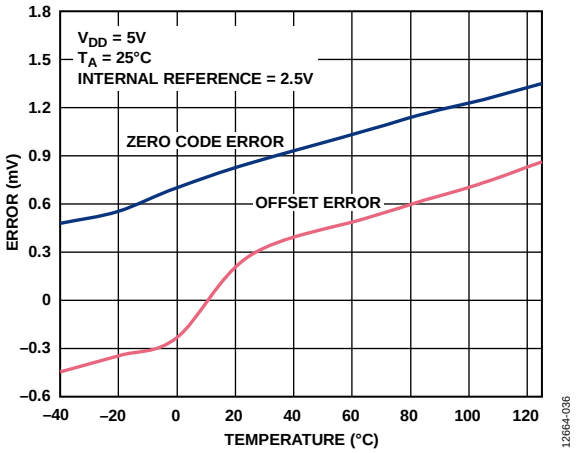


Figure 28. AD5671R Zero Code Error and Offset Error vs. Temperature

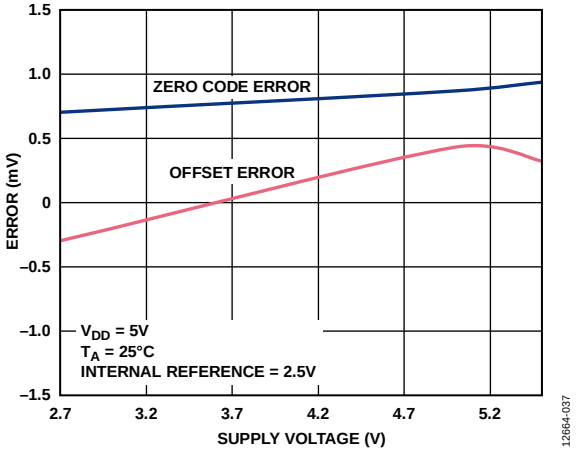


Figure 29. AD5675R Zero Code Error and Offset Error vs. Supply Voltage

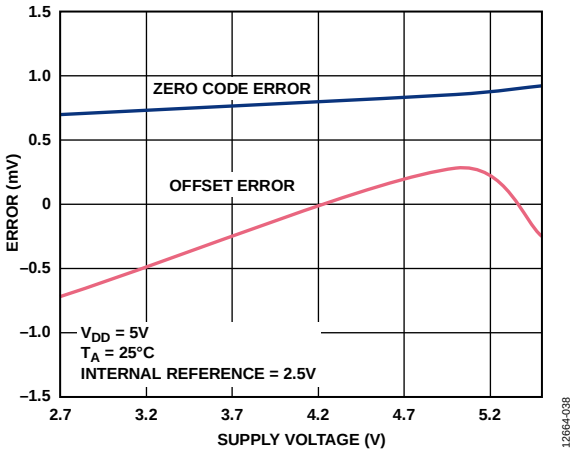


Figure 30. AD5671R Zero Code Error and Offset Error vs. Supply Voltage

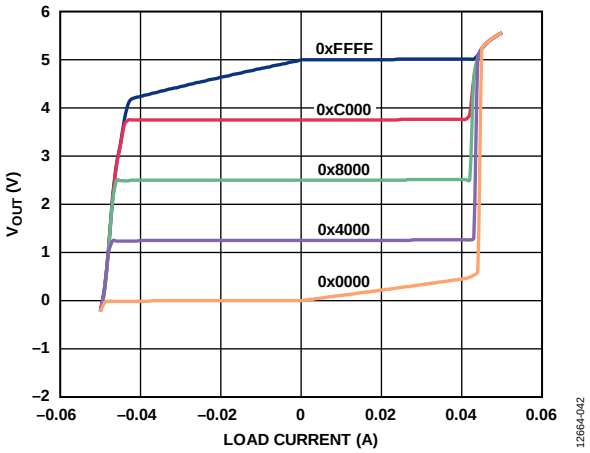


Figure 33. Source and Sink Capability at 5 V

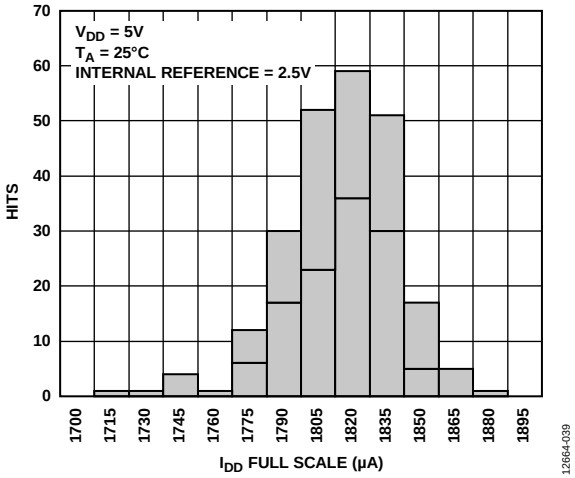


Figure 31. I_{DD} Histogram with Internal Reference

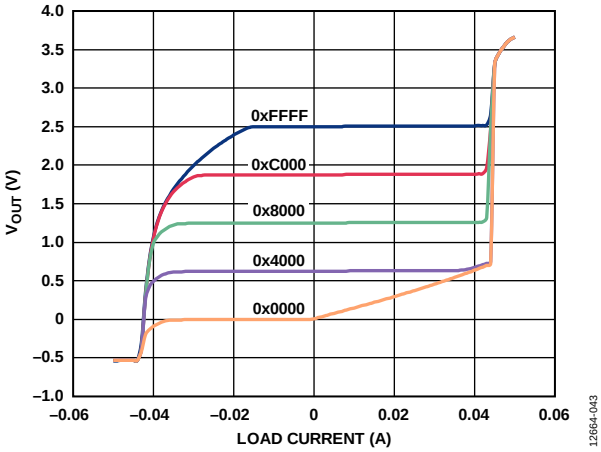


Figure 34. Source and Sink Capability at 3 V

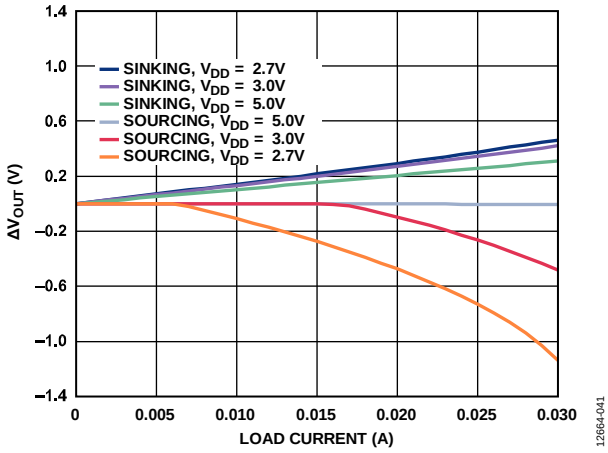


Figure 32. Output Voltage Change (ΔV_{OUT}) vs. Load Current

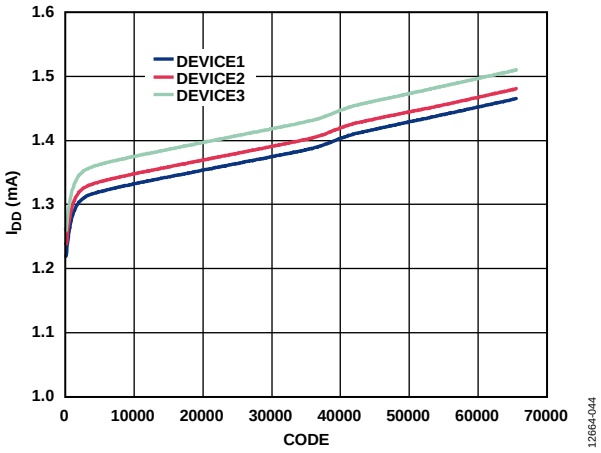


Figure 35. I_{DD} vs. Code

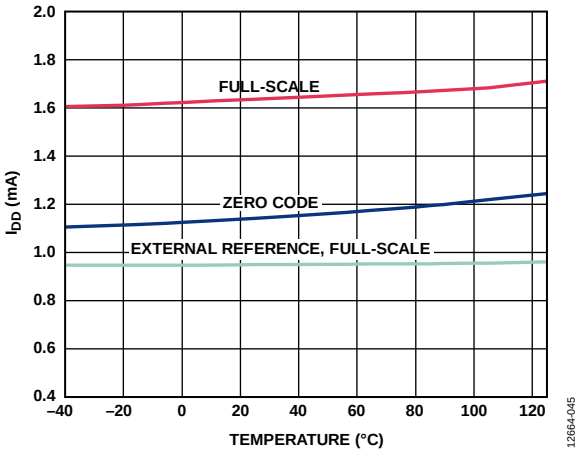


Figure 36. I_{DD} vs. Temperature

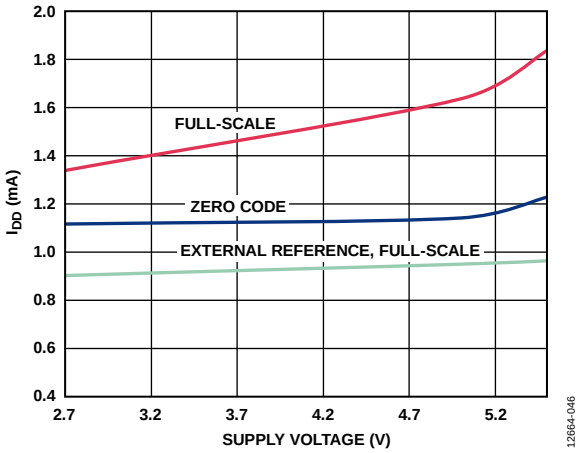


Figure 37. I_{DD} vs. Supply Voltage

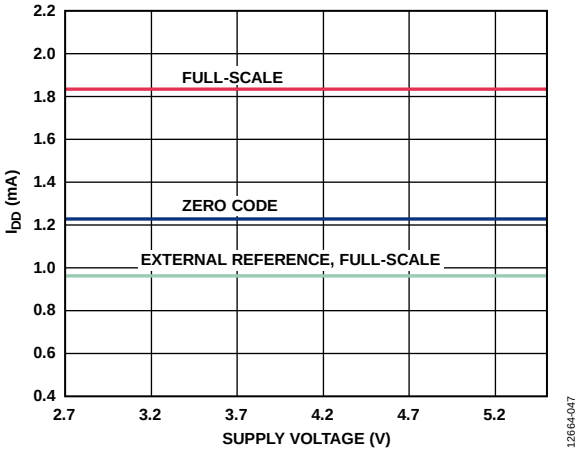


Figure 38. I_{DD} vs. Logic Input Voltage

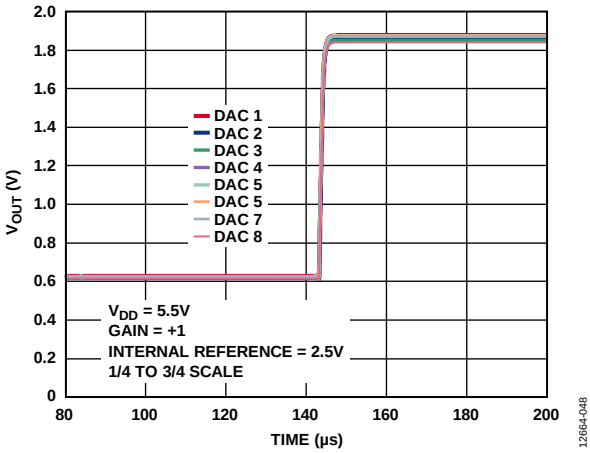


Figure 39. Full-Scale Settling Time

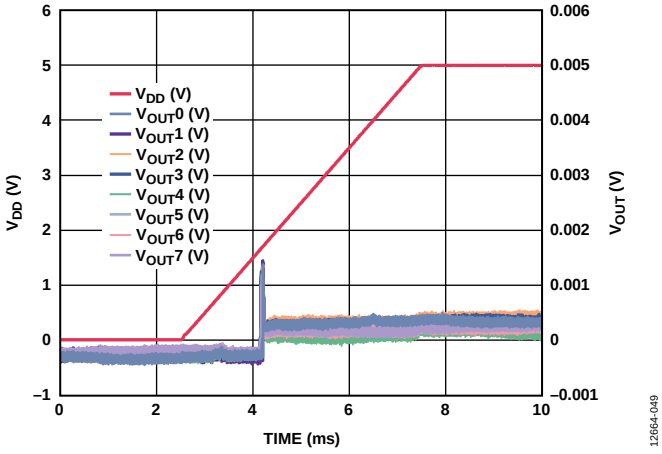


Figure 40. Power-On Reset to 0 V and Midscale

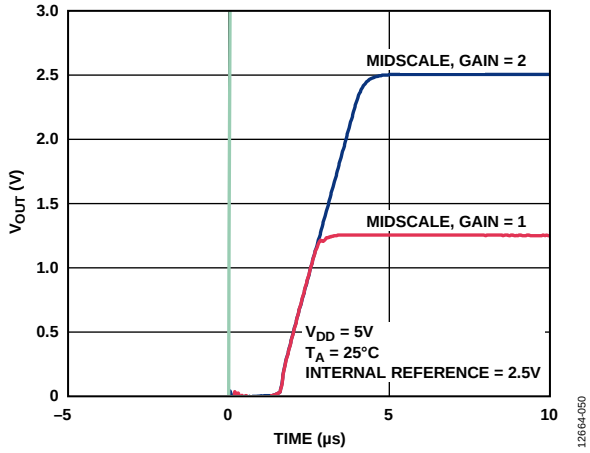


Figure 41. Exiting Power-Down to Midscale

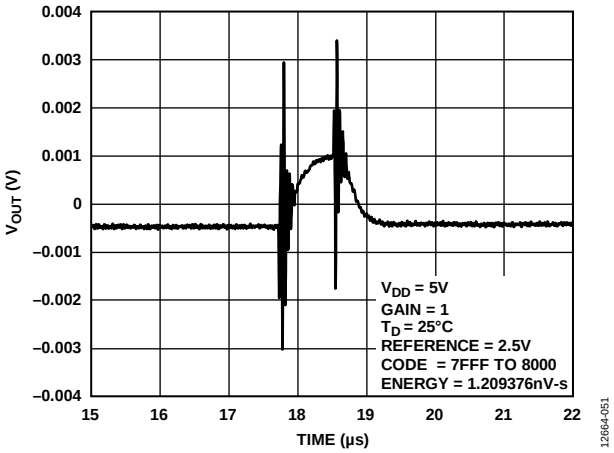


Figure 42. Digital-to-Analog Glitch Impulse

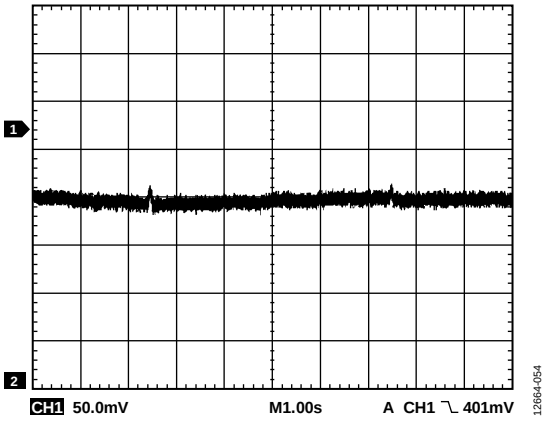


Figure 45. 0.1 Hz to 10 Hz Output Noise Plot

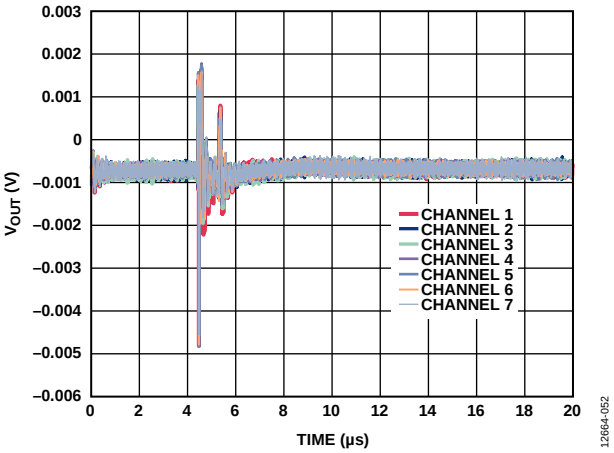


Figure 43. Analog Crosstalk

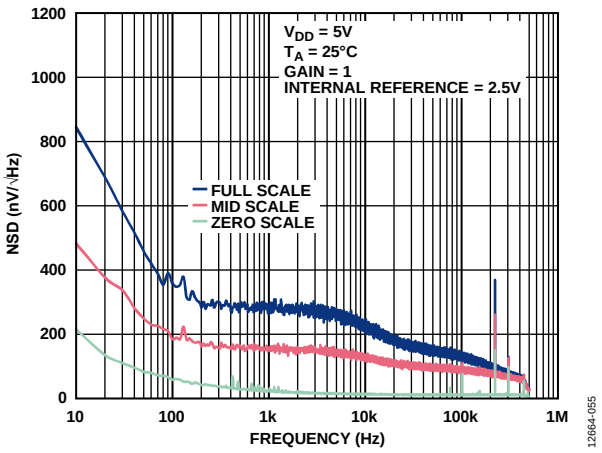


Figure 46. Noise Spectral Density (NSD)

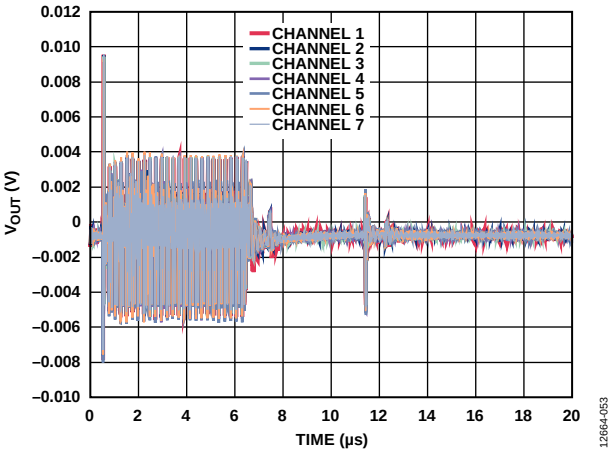


Figure 44. DAC-to-DAC Crosstalk

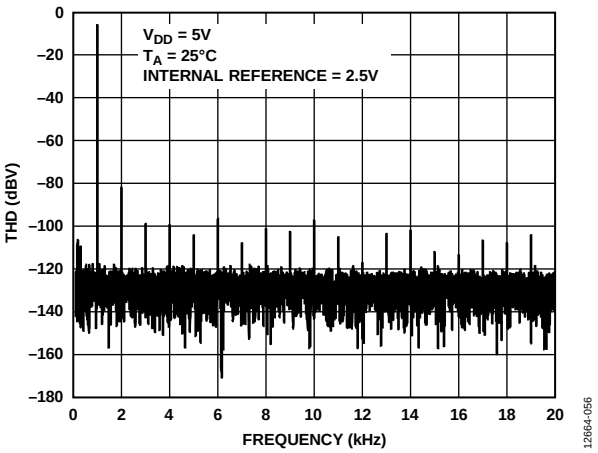


Figure 47. THD at 1 kHz

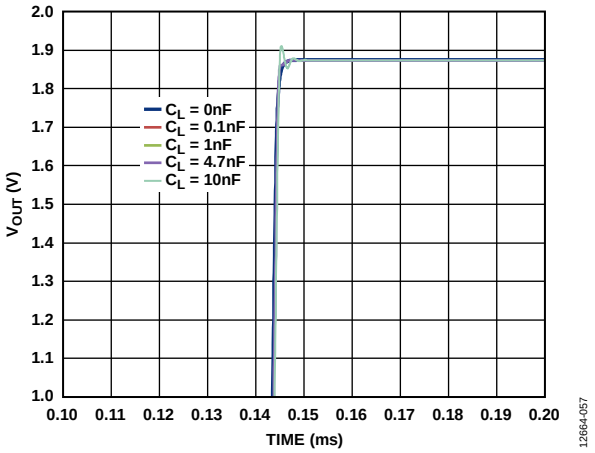


Figure 48. Settling Time at Various Capacitive Loads

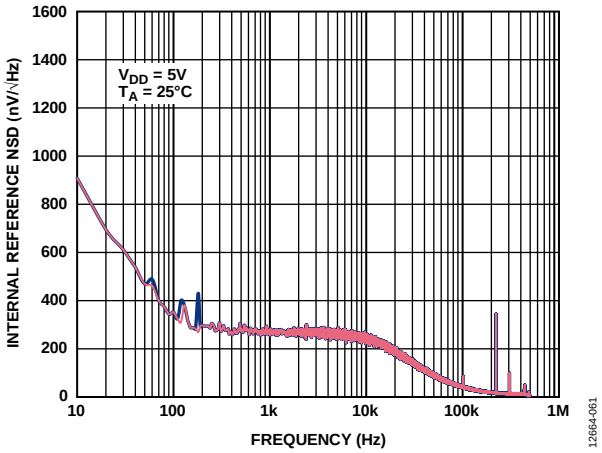


Figure 50. Internal Reference NSD vs. Frequency

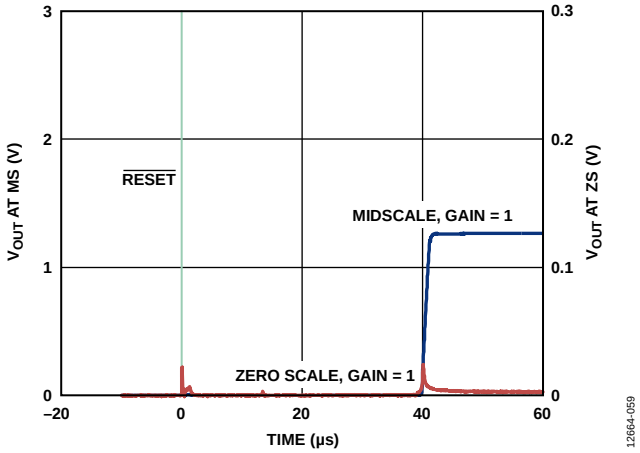


Figure 49. Hardware Reset

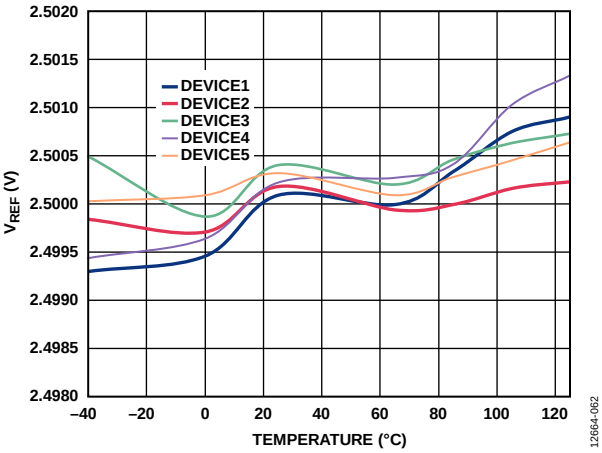


Figure 51. V_{REF} vs. Temperature (A Grade)

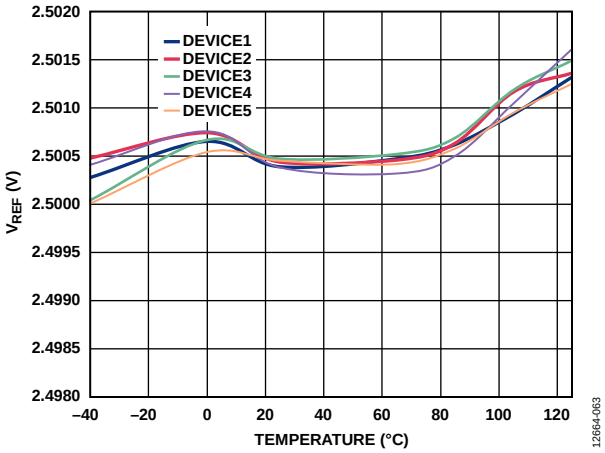


Figure 52. V_{REF} vs. Temperature (B Grade)

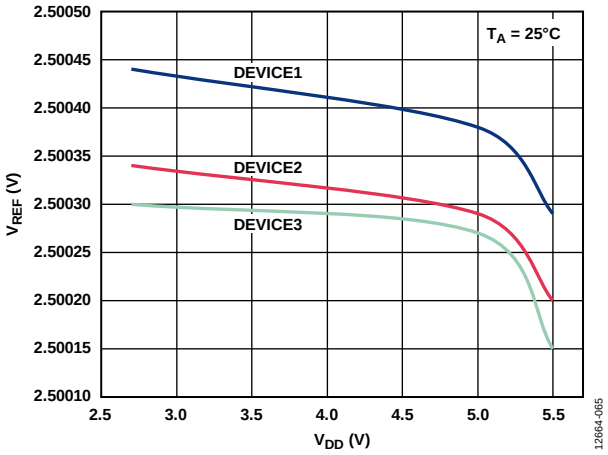


Figure 54. V_{REF} vs. V_{DD}

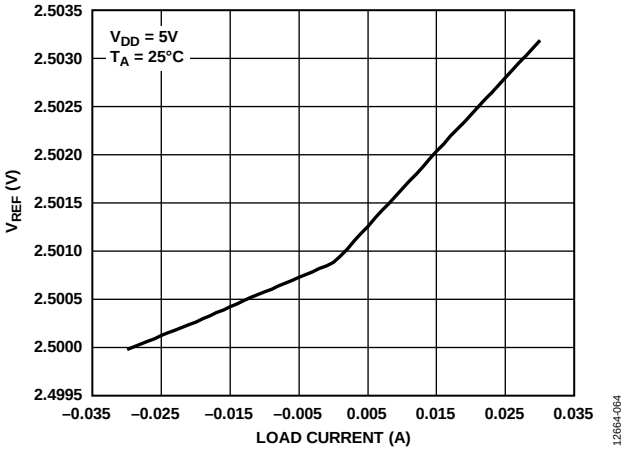


Figure 53. V_{REF} vs. Load Current and V_{DD}

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. These DACs are guaranteed monotonic by design.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. The ideal output is 0 V. The zero code error is always positive because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. The ideal output is V_{REF} − 1 LSB (Gain = 1) or 2 × V_{REF} (Gain = 2). Full-scale error is expressed in percent of full-scale range (% of FSR).

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 256 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
The dc power supply rejection ratio indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Noise Spectral Density (NSD)
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by first loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then, execute a software $\overline{\text{LDAC}}$ and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times TempRange} \right] \times 10^6$$

where:
$V_{REF\ (MAX)}$ is the maximum reference output measured over the total temperature range.
$V_{REF\ (MIN)}$ is the minimum reference output measured over the total temperature range.
$V_{REF\ (NOM)}$ is the nominal reference output voltage, 2.5 V.
TempRange is the specified temperature range of −40°C to +125°C.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The AD5671R/AD5675R are octal, 12-/16-bit, serial input, voltage output DACs with an internal reference. The devices operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5671R/AD5675R in a 24-bit word format via a 2-wire serial interface. The AD5671R/AD5675R incorporate a power-on reset circuit to ensure that the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to 1 μA.

TRANSFER FUNCTION

The internal reference is on by default.

Gain is the gain of the output amplifier and is set to 1 by default. This gain can be set to ×1 or ×2 using the gain select pin (GAIN). When this pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}.

DAC ARCHITECTURE

The AD5671R/AD5675R implement segmented string DAC architecture with an internal output buffer. Figure 55 shows the internal block diagram.

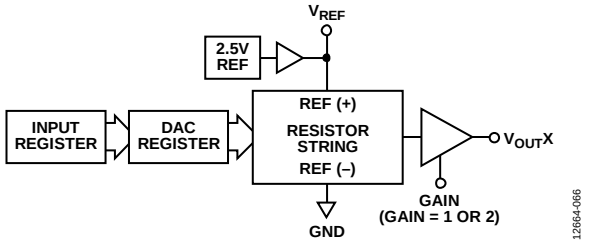


Figure 55. Single DAC Channel Architecture Block Diagram

The resistor string structure is shown in Figure 56. The code loaded to the DAC register determines the node on the string where the voltage is tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches and connecting the string to the amplifier. Because each resistance in the string has same value, R, the string DAC is guaranteed monotonic.

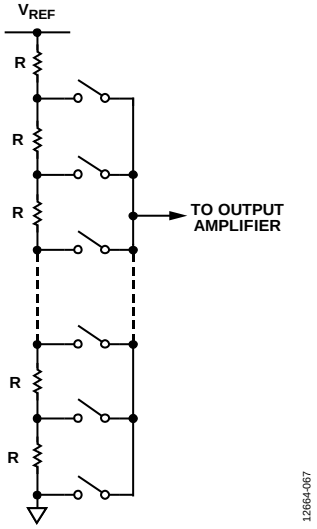


Figure 56. Resistor String Structure

Internal Reference

The AD5671R/AD5675R on-chip reference is enabled at power-up, but can be disabled via a write to the control register. See the Internal Reference and Amplifier Gain Selection section for details.

The AD5671R/AD5675R have a 2.5 V, 2 ppm/°C reference, giving a full-scale output of 2.5 V or 5 V, depending on the state of the GAIN pin. The internal reference associated with the device is available at the V_{REFOUT} pin. This buffered reference is capable of driving external loads of up to 15 mA.

Output Amplifiers

The output buffer amplifier generates rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The actual range depends on the value of V_{REF}, the GAIN pin, the offset error, and the gain error. The GAIN pin selects the gain of the output. If the GAIN pin is tied to GND, all eight outputs have a gain of 1, and the output range is 0 V to V_{REF}. If the GAIN pin is tied to V_{LOGIC}, all eight outputs have a gain of 2, and the output range is 0 V to 2 × V_{REF}.

These amplifiers are capable of driving a load of 1 kΩ in parallel with 10 nF to GND. The slew rate is 0.8 V/μs with a typical ¼ to ¾ scale settling time of 5 μs.

SERIAL INTERFACE

The AD5671R/AD5675R use a 2-wire, I²C-compatible serial interface. These devices can be connected to an I²C bus as a slave device under the control of the master devices. The AD5671R/AD5675R support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

Input Shift Register

The input shift register of the AD5671R/AD5675R is 24 bits wide. Data is loaded MSB first (DB23), and the first four bits are the command bits, C3 to C0 (see Table 9), followed by the 4-bit DAC address bits, A3 to A0 (see Table 10), and finally, the 16-bit data-word.

The data-word comprises 16-bit or 12-bit input code, followed by zero or four don't care bits for the AD5675R and AD5671R, respectively (see Figure 57 and Figure 58). These data bits are transferred to the input register on the 24 falling edges of SCL.

Commands execute on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected.

Table 9. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Hardware $\overline{\text{LDAC}}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference and gain setup register
1	0	0	0	Reserved
1	0	0	1	Set up the readback register (readback enable)
1	0	1	0	Update all channels of input register simultaneously with the input data
1	0	1	1	Update all channels of DAC register and input register simultaneously with the input data
1	1	0	0	Reserved
…	…	…	…	
1	1	1	1	Reserved

Table 10. Address Commands

Channel Address[3:0]				
A3	A2	A1	A0	Selected Channel
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7

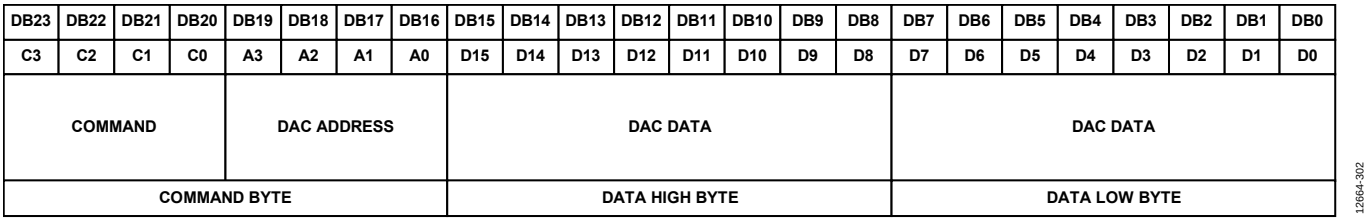


Figure 57. AD5675R Input Shift Register Content

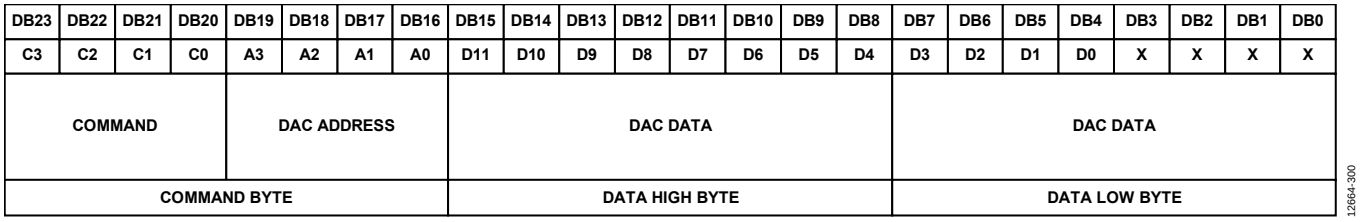


Figure 58. AD5671R Input Shift Register Content

WRITE AND UPDATE COMMANDS

Write to Input Register n (Dependent on $\overline{LDAC}$)

Command 0001 allows the user to write the dedicated input register of each DAC individually. When $\overline{LDAC}$ is low, the input register is transparent, if not controlled by the $\overline{LDAC}$ mask register.

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers and outputs with the contents of the input registers selected and updates the DAC outputs directly. Data Bit D7 to Bit D0 determine which DACs have data from the input register transferred to the DAC register. Setting a bit to 1 transfers data from the input register to the appropriate DAC register.

Write to and Update DAC Channel n (Independent of $\overline{LDAC}$)

Command 0011 allows the user to write to the DAC registers and updates the DAC outputs directly. The DAC address bits are used to select the DAC channel.

I²C SLAVE ADDRESS

The AD5671R/AD5675R have a 7-bit I²C slave address. The five MSBs are 00011, and the two LSBs (A1 and A0) are set by the state of the A1 and A0 address pins. The ability to make hardwired changes to A1 and A0 allows the user to incorporate up to four AD5671R/AD5675R devices on one bus (see Table 11).

Table 11. Device Address Selection

A1 Pin Connection	A0 Pin Connection	A1	A0
GND	GND	0	0
GND	V_{LOGIC}	0	1
V_{LOGIC}	GND	1	0
V_{LOGIC}	V_{LOGIC}	1	1

SERIAL OPERATION

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address.
2. The slave device with the transmitted address responds by pulling SDA low during the ninth clock pulse (this is called the acknowledge bit, or ACK). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its input shift register.
3. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). Transitions on the SDA line must occur during the low period of SCL; SDA must remain stable during the high period of SCL.
4. After all data bits are read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge (NACK) for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high again during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5671R/AD5675R, begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5671R/AD5675R require two bytes of data for the DAC, and a command byte that controls various DAC functions. Three bytes of data must therefore be written to the DAC with the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 59. All these data bytes are acknowledged by the AD5671R/AD5675R. A stop condition follows.

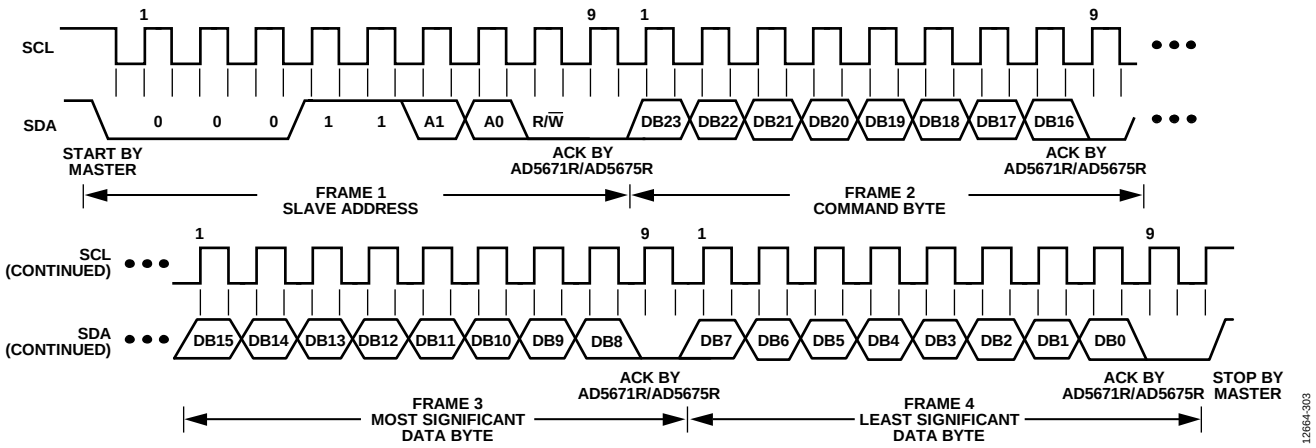


Figure 59. I²C Write Operation

READ OPERATION

When reading data back from the AD5671R/AD5675R, begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which determines both the read command that is to follow and the pointer address to read from; the command byte is also acknowledged by the DAC. The user configures the channel to read back the contents of one or more DAC input registers and sets the read back command to active using the command byte. The command byte must be followed by two dummy bytes of data.

Then, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 60. A NACK condition from the master, followed by a stop condition, completes the read sequence. If more than one DAC is selected, DAC 0 is read back by default.

MULTIPLE DAC READBACK SEQUENCE

When reading data back from multiple AD5671R/AD5675R DACs, the user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which is also acknowledged by the DAC. The user selects the first channel to read back using the command byte.

Following this sequence, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. The first two bytes of data are then read from DAC Input Register n (selected using the command byte), MSB first, as shown in Figure 60. The next two bytes read back are the contents of DAC Input Register n + 1, and the next bytes read back are the contents of DAC Input Register n + 2. Data is read from the DAC input registers in this autoincremented fashion until a NACK followed by a stop condition follows. If the contents of DAC Input Register 7 are read out, the next two bytes of data read are the contents of DAC Input Register 0.

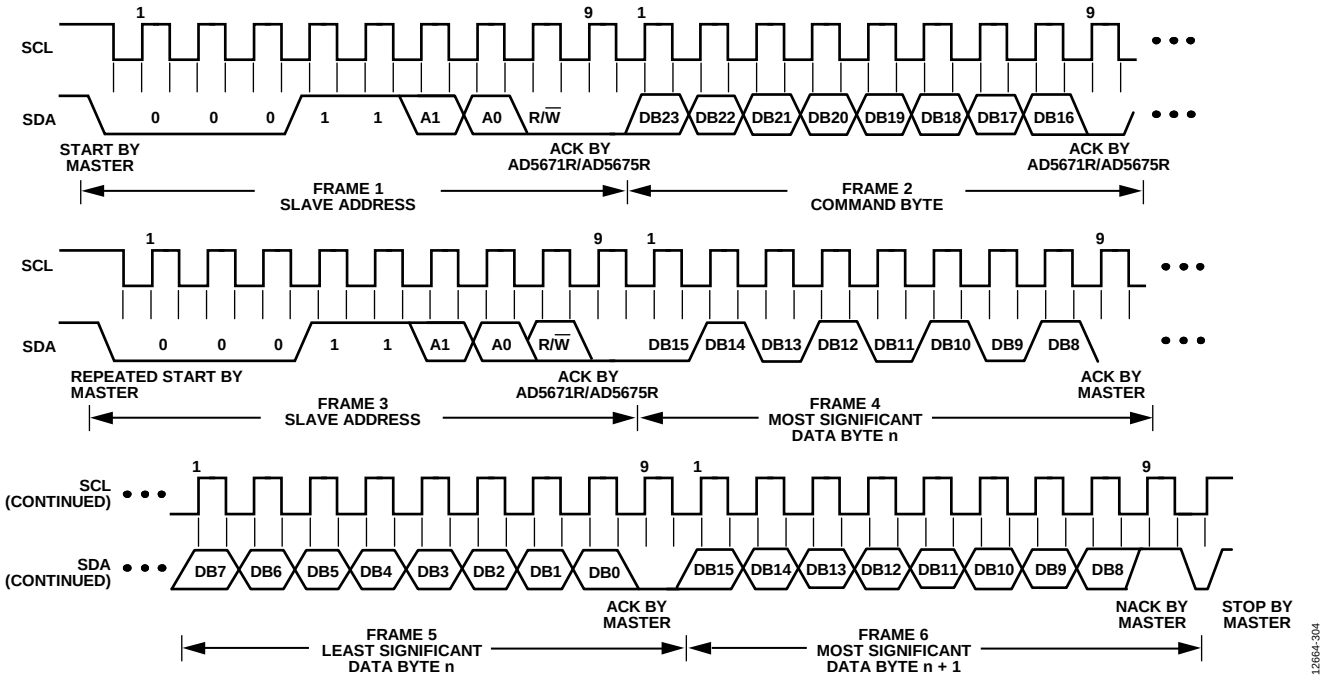


Figure 60. I²C Read Operation

POWER-DOWN OPERATION

The AD5671R/AD5675R contain two separate power-down modes. Command 0100 is designated for the power-down function (see Table 9). These power-down modes are software programmable by setting 16 bits, Bit DB15 to Bit DB0, in the input shift register. There are two bits associated with each DAC channel. Table 12 shows how the state of the two bits corresponds to the mode of operation of the device.

Any or all DACs (DAC 0 to DAC 7) power down to the selected mode by setting the corresponding bits. See Table 13 for the contents of the input shift register during the power-down/power-up operation.

Table 12. Modes of Operation

Operating Mode	PD1	PD0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
Tristate	1	1

When both Bit PD1 and Bit PD0 in the input shift register are set to 0, the device works normally with its normal power consumption of typically 1 mA at 5 V. However, for the two power-down modes, the supply current falls to typically 1 μA. In addition to this fall, the output stage switches internally from the amplifier output to a resistor network of known values. Therefore the DAC channel output impedance is defined when the channel is powered down. There are two different power-down options. The output is connected internally to GND through either a 1 kΩ resistor, or it is left open circuited (tristate). The output stage is shown in Figure 61.

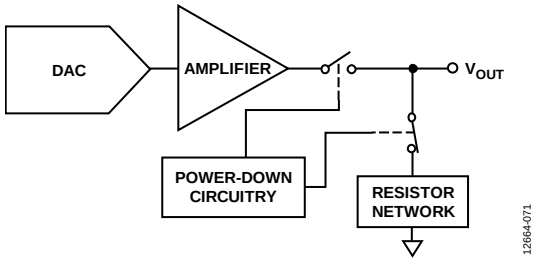


Figure 61. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC registers are unaffected in power-down mode, and the DAC registers can be updated while the device is in power-down mode. The time required to exit power-down is typically 2.5 μs for V_{DD} = 5 V.

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5671R/AD5675R DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC registers are controlled by the $\overline{\text{LDAC}}$ pin.

Instantaneous DAC Updating ($\overline{\text{LDAC}}$ Held Low)

For instantaneous updating of the DACs, $\overline{\text{LDAC}}$ is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the 24th clock, and the output changes immediately.

Deferred DAC Updating ($\overline{\text{LDAC}}$ is Pulsed Low)

For deferred updating of the DACs, $\overline{\text{LDAC}}$ is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by pulling $\overline{\text{LDAC}}$ low after the 24th clock. The update occurs on the falling edge of $\overline{\text{LDAC}}$.

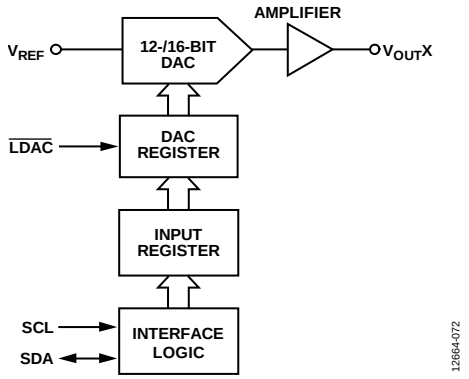


Figure 62. Simplified Diagram of Input Loading Circuitry for a Single DAC

Table 13. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation

			DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0
[DB23:DB20]	DB19	[DB18:DB16]	[DB15: B14]	[DB13: B12]	[DB11: B10]	[DB9:DB8]	[DB7:DB6]	[DB5:DB4]	[DB3:DB2]	[DB1:DB0]
0100	0	XXX[1]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

[1] X means don't care.

$\overline{\text{LDAC}}$ MASK REGISTER

Command 0101 is reserved for this software $\overline{\text{LDAC}}$ function. The address bits are ignored. Writing to the DAC using Command 0101 loads the 8-bit $\overline{\text{LDAC}}$ register (DB7 to DB0). The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the $\overline{\text{LDAC}}$ pin, regardless of the state of the hardware $\overline{\text{LDAC}}$ pin. This flexibility is useful in applications where the user wants to select which channels respond to the $\overline{\text{LDAC}}$ pin.

The $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (see Table 15). Setting the $\overline{\text{LDAC}}$ bits (DB0 to DB7) to 0 for a DAC channel means that this channel update is controlled by the hardware $\overline{\text{LDAC}}$ pin.

Table 14. $\overline{\text{LDAC}}$ Overwrite Definition

Load $\overline{\text{LDAC}}$ Register		
$\overline{\text{LDAC}}$ Bits (DB7 to DB0)	**$\overline{\text{LDAC}}$ Pin**	**$\overline{\text{LDAC}}$ Operation**
00000000	1 or 0	Determined by the $\overline{\text{LDAC}}$ pin.
11111111	X[1]	DAC channels update and override the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 1.

[1] X means don't care.

Table 15. Write Commands and $\overline{\text{LDAC}}$ Pin Truth Table[1]

Command	Description	Hardware $\overline{\text{LDAC}}$ Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update DAC Register n with contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high to low hardware $\overline{\text{LDAC}}$ pin transition always updates the contents of the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the $\overline{\text{LDAC}}$ mask register.
[2] When $\overline{\text{LDAC}}$ is permanently tied low, the LDAC mask bits are ignored.

HARDWARE RESET ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the RSTSEL pin. Keep $\overline{\text{RESET}}$ low for a minimum time (see Table 5) to complete the operation. When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the outputs cannot be updated with a new value. Any events on $\overline{\text{LDAC}}$ or $\overline{\text{RESET}}$ during power-on reset are ignored. If the $\overline{\text{RESET}}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5671R/AD5675R contain a power-on reset circuit that controls the output voltage during power-up. By connecting the RSTSEL pin low, the output powers up to zero scale. Note that this power-up is outside the linear region of the DAC; by connecting the RSTSEL pin high, V_{OUT} powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC.

SOFTWARE RESET

A software executable reset function is also available, which resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function. The DAC address bits must be set to 0x0 and the data bits set to 0x1234 for the software reset command to execute.

INTERNAL REFERENCE AND AMPLIFIER GAIN SELECTION

The on-chip reference is on at power-up by default. To reduce the supply current, turn off this reference by setting the software programmable bit, DB0, in the internal reference and gain setup register.

The state of Bit DB2 in the internal reference and gain setup register determines the output amplifier gain setting for the LFCSP package (see Table 16 and Table 17). Ignore Bit DB2 for the TSSOP package. Command 0111 is reserved for setting up the internal reference and amplifier gain.

Table 16. Internal Reference and Gain Setup Register

Bit	Description
DB2	Amplifier gain setting DB2 = 0; amplifier gain = 1 (default) DB2 = 1; amplifier gain = 2
DB1	Reserved; set to 0
DB0	Internal reference DB0 = 0; reference is on (default) DB1 = 1; reference is off

SOLDER HEAT REFLOW

As with all IC reference voltage circuits, the reference value experiences a shift induced by the soldering process. Analog Devices, Inc., performs a reliability test called precondition to mimic the effect of soldering a device to a board. The output voltage specification quoted previously includes the effect of this reliability test.

Figure 63 shows the effect of solder heat reflow (SHR) as measured through the reliability test (precondition).

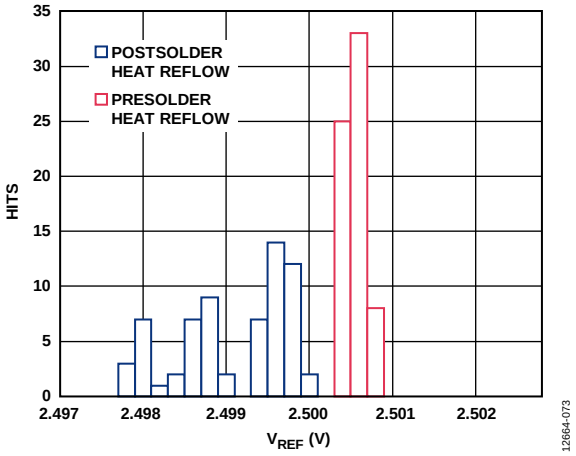


Figure 63. Solder Heat Reflow Reference Voltage Shift

LONG-TERM TEMPERATURE DRIFT

Figure 64 shows the change in V_{REF} value after 1000 hours in the life test at 150°C.

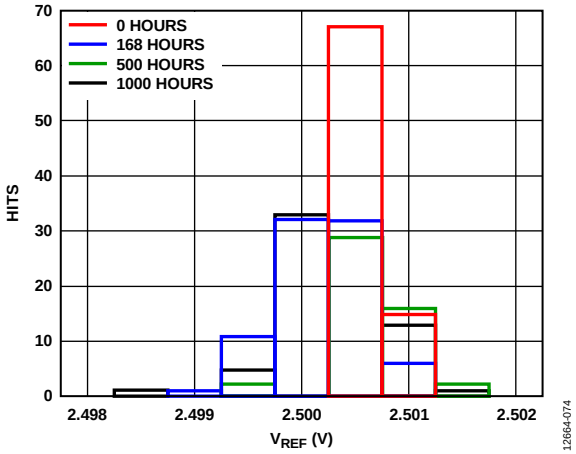


Figure 64. Reference Drift Through to 1000 Hours

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

Thermal hysteresis data is shown in Figure 65. It is measured by sweeping the temperature from ambient to −40°C, then to +125°C, and returning to ambient. The V_{REF} delta is then measured between the two ambient measurements and shown in blue in Figure 65. The same temperature sweep and measurements were immediately repeated, and the results are shown in red in Figure 65.

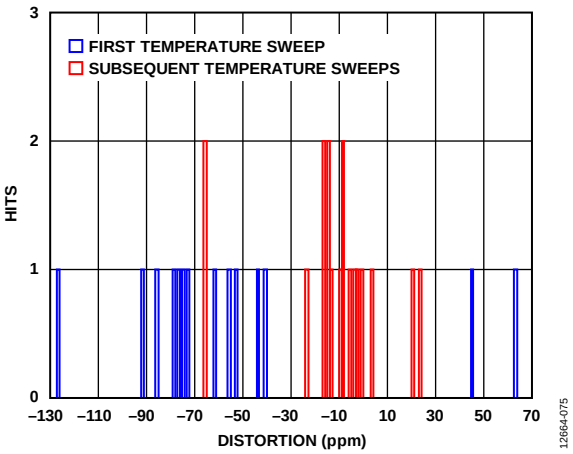


Figure 65. Thermal Hysteresis

Table 17. 24-Bit Input Shift Register Contents for Internal Reference and Amplifier Gain Setup Command[1]

DB23 (MSB)	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB1 to DB3	DB2	DB1	DB0 (LSB)
0	1	1	1	X	X	X	X	X	1/0	0	1/0
Command bits (C3 to C0)				Address bits (A3 to A0)				Don't care	Amplifier gain	Reserved	Reference setup register

[1] X means don't care.

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD5671R/AD5675R is typically powered by the following supplies: V_{DD} = 3.3 V and V_{LOGIC} = 1.8 V.

The ADP7118 can be used to power the V_{DD} pin. The ADP160 can be used to power the V_{LOGIC} pin. This setup is shown in Figure 66. The ADP7118 can operate from input voltages up to 20 V. The ADP160 can operate from input voltages up to 5.5 V.

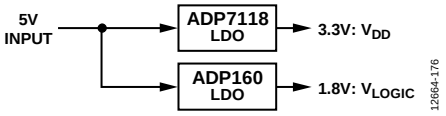


Figure 66. Low Noise Power Solution for the AD5671R/AD5675R

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5671R/AD5675R is done via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 2-wire interface consisting of a clock signal and a data signal.

AD5671R/AD5675R TO ADSP-BF531 INTERFACE

The I²C interface of the AD5671R/AD5675R is designed for easy connection to industry-standard DSPs and microcontrollers. Figure 67 shows the AD5671R/AD5675R connected to the Analog Devices, Inc., Blackfin® processor. The Blackfin processor has an integrated I²C port that can be connected directly to the I²C pins of the AD5671R/AD5675R.

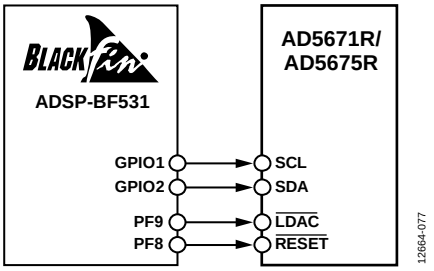


Figure 67. AD5671R/AD5675R to ADSP-BF531 Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5671R/AD5675R are mounted so that the devices lie on the analog plane.

The AD5671R/AD5675R must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The GND plane on the device can be increased (as shown in Figure 68) to provide a natural heat sinking effect.

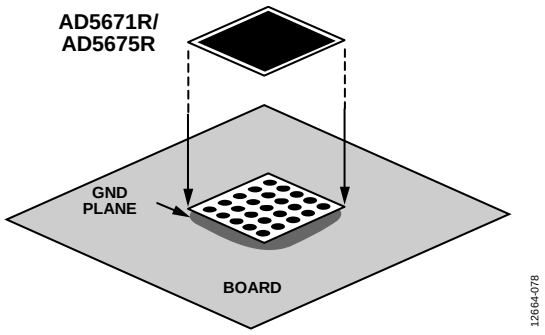


Figure 68. Pad Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5671R/AD5675R makes the devices ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 69 shows a 2-channel isolated interface to the AD5671R/AD5675R using an ADuM1251. For further information, visit www.analog.com/icoupler.

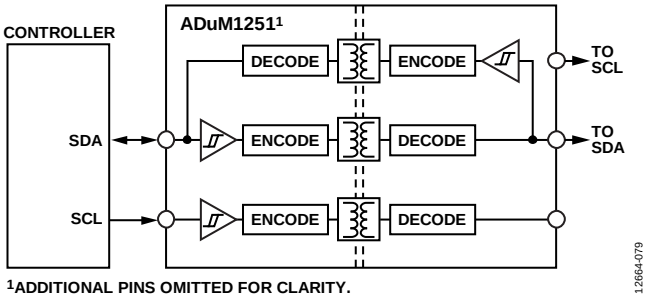
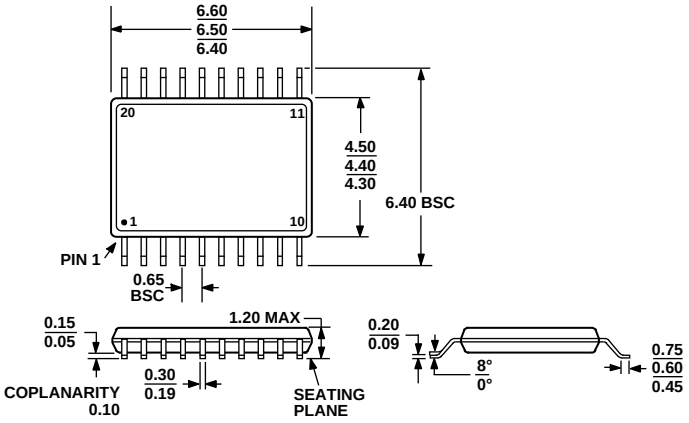


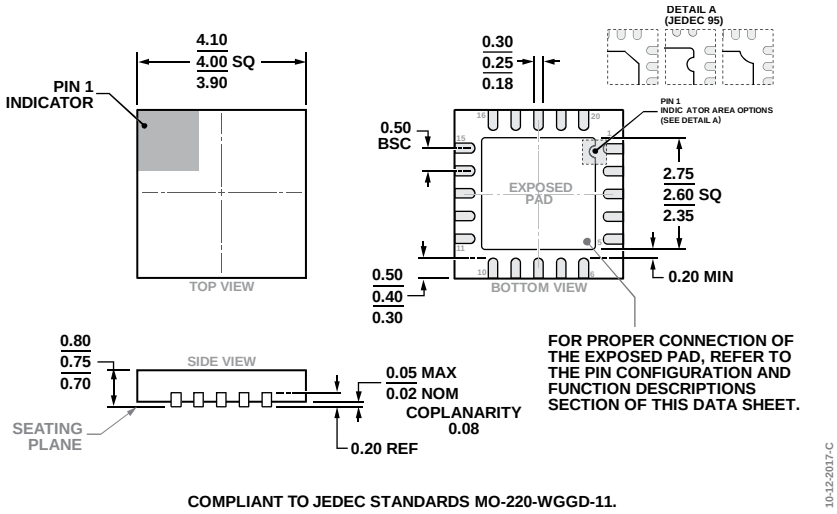
Figure 69. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 70. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 71. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Resolution	Temperature Range	Accuracy	Reference Temperature Coefficient (ppm/°C)	Package Description	Package Option
AD5671RBRUZ	12 Bits	−40°C to +125°C	±1 LSB INL	2 (typical)	20-Lead TSSOP	RU-20
AD5671RBRUZ-REEL7	12 Bits	−40°C to +125°C	±1 LSB INL	2 (typical)	20-Lead TSSOP	RU-20
AD5671RBCPZ-REEL7	12 Bits	−40°C to +125°C	±1 LSB INL	2 (typical)	20-Lead LFCSP	CP-20-8
AD5671RBCPZ-RL	12 Bits	−40°C to +125°C	±1 LSB INL	2 (typical)	20-Lead LFCSP	CP-20-8
AD5675RARUZ	16 Bits	−40°C to +125°C	±8 LSB INL	5 (typical)	20-Lead TSSOP	RU-20
AD5675RARUZ-REEL7	16 Bits	−40°C to +125°C	±8 LSB INL	5 (typical)	20-Lead TSSOP	RU-20
AD5675RBRUZ	16 Bits	−40°C to +125°C	±3 LSB INL	2 (typical)	20-Lead TSSOP	RU-20
AD5675RBRUZ-REEL7	16 Bits	−40°C to +125°C	±3 LSB INL	2 (typical)	20-Lead TSSOP	RU-20
AD5675RACPZ-REEL7	16 Bits	−40°C to +125°C	±8 LSB INL	5 (typical)	20-Lead LFCSP	CP-20-8
AD5675RACPZ-RL	16 Bits	−40°C to +125°C	±8 LSB INL	5 (typical)	20-Lead LFCSP	CP-20-8
AD5675RBCPZ-REEL7	16 Bits	−40°C to +125°C	±3 LSB INL	5 (typical)	20-Lead LFCSP	CP-20-8
AD5675RBCPZ-RL	16 Bits	−40°C to +125°C	±3 LSB INL	5 (typical)	20-Lead LFCSP	CP-20-8
EVAL-AD5675RSDZ					AD5675R Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5675RSDZ is used to evaluate the AD5671R and AD5675R.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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AD5671RBRUZ AD5671RBRUZ-REEL7 AD5675RARUZ AD5675RARUZ-REEL7 AD5675RBCPZ-REEL7 AD5675RACPZ-REEL7 AD5671RBCPZ-REEL7 AD5671RBCPZ-RL AD5675RBCPZ-RL AD5675RACPZ-RL AD5675RBRUZ AD5675RBRUZ-REEL7 EVAL-AD5675RARDZ