Data Sheet

AD4630-24/AD4632-24

24-Bit, 2 MSPS/500 kSPS, Dual Channel SAR ADCs

FEATURES

- High performance
  - Throughput: 2 MSPS (AD4630-24) or 500 kSPS (AD4632-24) per channel maximum
  - INL: ±0.9 ppm maximum from −40°C to +125°C
  - SNR: 105.7 dB typical
  - THD: −127 dB typical
  - NSD: −166 dBFS/Hz typical
- Low power
  - 15 mW per channel at 2 MSPS
  - 5 mW per channel at 500 kSPS
  - 1.5 mW per channel at 10 kSPS
- Easy Drive features reduce system complexity
  - Low 0.6 µA input current for dc inputs at 2 MSPS
  - Wide input common-mode range: −(1/128) × V_{REF} to +(129/128) × V_{REF}
- Flexible external reference voltage range: 4.096 V to 5 V
  - Accurate integrated reference buffer with 2 µF bypass capacitor
- Programmable block averaging filter with up to 2^{16} decimation
  - Extended sample resolution to 30 bits
  - Overrange and synchronization bits
- Flexi-SPI digital interface
  - 1, 2, or 4 SDO lanes per channel allows slower SCK
  - Echo clock mode simplifies use of digital isolator
  - Compatible with 1.2 V to 1.8 V logic
- 7 mm × 7 mm 64-Ball CSP_BGA package with internal supply and reference capacitors to help reduce system footprint

APPLICATIONS

- Automatic test equipment
- Digital control loops
- Medical instrumentation
- Seismology
- Semiconductor manufacturing
- Scientific instrumentation

FUNCTIONAL BLOCK DIAGRAM

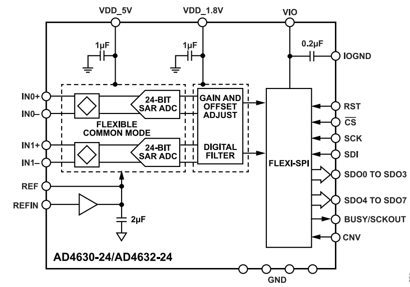

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD4630-24/AD4632-24 are two-channel, simultaneous sampling, Easy Drive™, 2 MSPS or 500 kSPS successive approximation register (SAR) analog-to-digital converters (ADCs). With a guaranteed maximum ±0.9 ppm INL and no missing codes at 24 bits, the AD4630-24/AD4632-24 achieve unparalleled precision from −40°C to +125°C. Figure 1 shows the functional architecture of the AD4630-24/AD4632-24.

A low drift, internal precision reference buffer eases voltage reference sharing with other system circuitry. The AD4630-24/AD4632-24 offer a typical dynamic range of 106 dB when using a 5 V reference. The low noise floor enables signal chains requiring less gain and lower power. A block averaging filter with programmable decimation ratio can increase dynamic range up to 153 dB. The wide differential input and common-mode ranges allow inputs to use the full voltage reference (±V_{REF}) range without saturating, simplifying signal conditioning requirements and system calibration. The improved settling of the Easy Drive analog inputs broadens the selection of analog front-end components compatible with the AD4630-24/AD4632-24. Both single-ended and differential signals are supported.

The versatile Flexi-SPI serial peripheral interface (SPI) eases host processor and ADC integration. A wide data clocking window, multiple SDO lanes, and optional dual data rate (DDR) data clocking can reduce the serial clock to 10 MHz while operating at a sample rate of 2 MSPS or 500 kSPS. Echo clock mode and ADC host clock mode relax the timing requirements and simplify the use of digital isolators.

The 64-ball chip scale package ball grid array (CSP_BGA) of the AD4630-24/AD4632-24 integrates all critical power supply and reference bypass capacitors, reducing the footprint and system component count, and lessening sensitivity to board layout.

Rev. B

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

5/2023—Rev. A to Rev. B

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VDD_5V = 5.4 V, VDD_1.8V = 1.8 V, VIO = 1.8 V, REFIN = 5 V, input common mode = 2.5 V, sampling frequency (f_S) = 2 MSPS and 500 kSPS for the AD4630-24/AD4632-24, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		24			Bits
ANALOG INPUT					
Voltage Range	INx+ voltage (V_{INx+}) − INx− voltage (V_{INx-})	−(65/64) × V_{REF}		+(65/64) × V_{REF}	V
Absolute Input Voltage	V_{INx+}, V_{INx-} to GND	−(1/128) × V_{REF}		+(129/128) × V_{REF}	V
Common-Mode Input Range	(V_{INx+} + V_{INx-})/2	−(1/128) × V_{REF}		+(129/128) × V_{REF}	V
Common-Mode Rejection Ratio (CMRR)	Input frequency (f_{IN}) = 10 kHz		132		dB
Analog Input Current	Acquisition phase, T_A = 25°C		0.4		nA
	Converting any dc input at 2 MSPS		0.6		µA
Analog Input Capacitance (C_{IN})	Acquisition phase		60		pF
	Outside acquisition phase (pin capacitance (C_{PIN}))		2		pF
THROUGHPUT					
Complete Cycle					
AD4630-24		500			ns
AD4632-24		2000			ns
Conversion Time		264	282	300	ns
Acquisition Phase[1]					
AD4630-24		244	260	275	ns
AD4632-24		1744	1760	1775	ns
Throughput Rate					
AD4630-24		0		2	MSPS
AD4632-24		0		500	kSPS
DC ACCURACY					
No Missing Codes		24			Bits
Integral Nonlinearity (INL) Error		−0.9	±0.1	+0.9	ppm
Differential Nonlinearity (DNL) Error			±0.5		LSB
Transition Noise			29.7		LSB rms
Zero Error		−90	0	+90	µV
Zero Error Drift			±0.007		ppm/°C
Gain Error	Buffer disabled, REF = 5 V	−0.004	±0.0002	+0.004	%FS
	Buffer enabled, REFIN = 5 V	−0.008	±0.0006	+0.008	%FS
Gain Error Temperature Drift	Buffer disabled, REF = 5 V		±0.025		ppm/°C
	Buffer enabled, REFIN = 5 V		±0.07		ppm/°C
Power Supply Sensitivity	VDD_5V = 5.4 V ± 0.1 V		±0.1		ppm
	VDD_1.8V = 1.8 V ± 5%		±0.2		ppm
Low Frequency Noise[2]	Bandwidth = 0.1 Hz to 10 Hz		1.8		µV p-p
AC ACCURACY					
Dynamic Range			106		dB
Noise Spectral Density (NSD)			−166		dBFS/Hz
Total RMS Noise			17.7		µV rms
Signal to Noise Ratio (SNR)	f_{IN} = 1 kHz, −0.5 dBFS	103.3	105.7		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz, −0.5 dBFS		127		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz, −0.5 dBFS		−127	−115	dB
Signal-to-Noise-and-Distortion (SINAD) Ratio	f_{IN} = 1 kHz, −0.5 dBFS	103.3	105.7		dB
Oversampled Dynamic Range	Averaging = 2		109		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Averaging = 256		130		dB
	Averaging = 65536		152.7		dB
SNR	VDD_5V = 5.0 V, f_{IN} = 1 kHz, −0.5 dBFS, REFIN = 4.096 V		104		dB
SFDR	VDD_5V = 5.0 V, f_{IN} = 1 kHz, −0.5 dBFS, REFIN = 4.096 V		130		dB
THD	VDD_5V = 5.0 V, f_{IN} = 1 kHz, −0.5 dBFS, REFIN = 4.096 V		−130		dB
SINAD	VDD_5V = 5.0 V, f_{IN} = 1 kHz, −0.5 dBFS, REFIN = 4.096 V		104		dB
SNR	f_{IN} = 100 kHz, −0.5 dBFS		105.6		dB
THD	f_{IN} = 100 kHz, −0.5 dBFS		−113		dB
SINAD	f_{IN} = 100 kHz, −0.5 dBFS		104.9		dB
−3 dB Input Bandwidth			74		MHz
Aperture Delay			0.7		ns
Aperture Jitter			1.4		ps rms
CHANNEL-TO-CHANNEL CROSSTALK	f_{IN} = 1 kHz, 1.3 kHz		−135		dB
INTERNAL REFERENCE BUFFER	External reference drives REFIN				
REFIN Voltage Range	5.3 V ≤ VDD_5V ≤ 5.5 V	4.95	5	5.05	V
	4.8 V ≤ VDD_5V ≤ 5.25 V		4.5		V
	4.75 V ≤ VDD_5V ≤ 5.25 V	4.046	4.096	4.146	V
REFIN Bias Current		−50	5	+50	nA
REFIN Input Capacitance			40		pF
Reference Buffer Offset Error	REFIN = 5 V, T_A = 25°C	−100	±25	+100	μV
	REFIN = 4.5 V, T_A = 25°C		±25		μV
	REFIN = 4.096 V, T_A = 25°C	−100	±25	+100	μV
Reference Buffer Offset Drift			±0.3		μV/°C
Power-On Settling Time			3		ms
EXTERNALLY OVERDRIVEN REFERENCE	External reference drives REF (REFIN = 0 V)				
REF Voltage Range	5.3 V ≤ VDD_5V ≤ 5.5 V	4.95	5	5.05	V
	4.8 V ≤ VDD_5V ≤ 5.25 V		4.5		V
	4.75 V ≤ VDD_5V ≤ 5.25 V	4.046	4.096	4.146	V
REF Current					
AD4630-24	f_S = 2 MSPS		1.8		μA
AD4632-24	f_S = 500 kSPS		0.5		μA
REF Input Capacitance			2		μF
DIGITAL INPUTS	1.14 V ≤ VIO ≤ 1.89 V				
Logic Levels					
Input Voltage Low (V_{IL})		−0.3		+0.35 × VIO	V
Input Voltage High (V_{IH})		0.65 × VIO		VIO + 0.3	V
Input Current Low (I_{IL})		−10		+10	μA
Input Current High (I_{IH})		−10		+10	μA
Input Pin Capacitance			2		pF
DIGITAL OUTPUTS	1.14 V ≤ VIO ≤ 1.89 V				
Pipeline Delay		Conversion results available immediately after completed conversion			
Output Voltage Low (V_{OL})	Sink current (I_{SINK}) = 2 mA			0.25 × VIO	V
Output Voltage High (V_{OH})	Source current (I_{SOURCE}) = 2 mA	0.75 × VIO			V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES					
VDD_5V	REF = 5 V	5.3	5.4	5.5	V
	REF = 4.5 V	4.8	5	5.25	V
	REF = 4.096 V	4.75	5	5.25	V
VDD_1.8V		1.71	1.8	1.89	V
VIO[3]		1.14		1.89	V
Standby Current					
VDD_5V			500		µA
VDD_1.8V			90		µA
VIO			<1		µA
Shutdown Current					
VDD_5V			5		µA
VDD_1.8V			5		µA
VIO			<1		µA
Operating Current, AD4630-24	Both channels active, 2 MSPS				
VDD_5V	VDD_5V = 5.4 V		2.7	3.2	mA
VDD_1.8V	VDD_1.8V = 1.8 V		8.2	11.2	mA
VIO	VIO = 1.8 V, 1-lane SDO		0.6		mA
Operating Current, AD4632-24	Both channels active, 500 kSPS				
VDD_5V	VDD_5V = 5.4 V		1.1	1.5	mA
VDD_1.8V	VDD_1.8V = 1.8 V		2.1	3.1	mA
VIO	VIO = 1.8 V, 1-lane SDO		0.15		mA
Power Dissipation	Both channels active, 2 MSPS		30	39	mW
	Both channels active, 500 kSPS		10	14.2	mW
t_{RESET_DELAY}	After power-on, delay from VDD_5V and VDD_1.8V valid to $\overline{RST}$ assertion	3			ms
t_{RESET_PW}	$\overline{RST}$ pulse width	50			ns
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

1 The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS for the AD4630-24 and 500 kSPS for the AD4632-24.

2 See the low frequency noise plot in Figure 24. 1/f noise is canceled internally by auto-zeroing. Noise spectral density is substantially uniform from dc to $f_S/2$.

3 When VIO < 1.4V, Bit IO2X must be set to 1. See the Output Driver Register section.

TIMING SPECIFICATIONS

VDD_5V = 5.4 V, VDD_1.8V = 1.8 V, VIO = 1.8 V, REFIN = 5 V, input common mode = 2.5 V, f_S = 2 MSPS and 500 kSPS for the AD4630-24/AD4632-24, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C. See Figure 2 for the timing voltage levels. For VIO < 1.4 V, Bit IO2X must be set to 1.

Table 2. Digital Timing Interface

Parameter[1]	Symbol	Min	Typ	Max	Unit
Conversion Time—CNV Rising Edge to Data Available	t_{CONV}	264	282	300	ns
Acquisition Phase[2]					
AD4630-24	t_{ACQ}	244	260	275	ns
AD4632-24	t_{ACQ}	1744	1760	1775	ns
Time Between Conversions					
AD4630-24	t_{CYC}	500			ns
AD4632-24	t_{CYC}	2000			ns

SPECIFICATIONS

Table 2. Digital Timing Interface (Continued)

Parameter[1]	Symbol	Min	Typ	Max	Unit
CNV High Time	t_{CNVH}	10			ns
CNV Low Time	t_{CNVL}	20			ns
Internal Oscillator Frequency	f_{OSC}	75.1	80	84.7	MHz

[1] Timing specifications assume a 5 pF load capacitance on digital output pins. t_{CONV}, t_{CYC}, t_{SCK}, and t_{SCKOUT} are production tested. All other timing specifications are guaranteed by characterization and design.

[2] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS for the AD4630-24 and 500 kSPS for the AD4632-24.

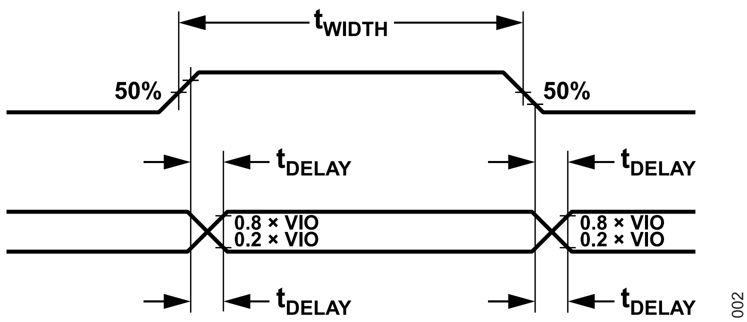


Figure 2. Voltage Levels for Timing

Table 3. Register Read/Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Pulse Width	t_{CSPW}	10			ns
SCK Period	t_{SCK}				
VIO > 1.71 V		11.6			ns
VIO > 1.14 V		12.3			ns
SCK Low Time	t_{SCKL}	5.2			ns
SCK High Time	t_{SCKH}	5.2			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	2.1			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 1.71 V				9.4	ns
VIO > 1.14 V				11.8	ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns
SDI Valid Setup Time to SCK Rising Edge	t_{SSDI}	1.5			ns
SDI Valid Hold Time from SCK Rising Edge	t_{HSDI}	1.5			ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}				
VIO > 1.71 V		11.6			ns
VIO > 1.14 V		12.3			ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	5.2			ns

SPECIFICATIONS

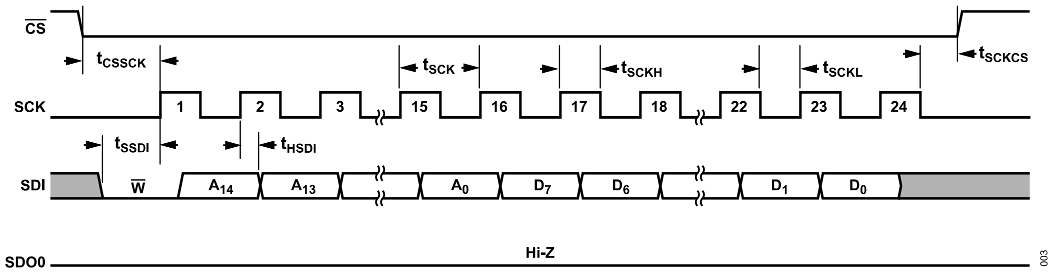


Figure 3. Register Configuration Mode Write Timing

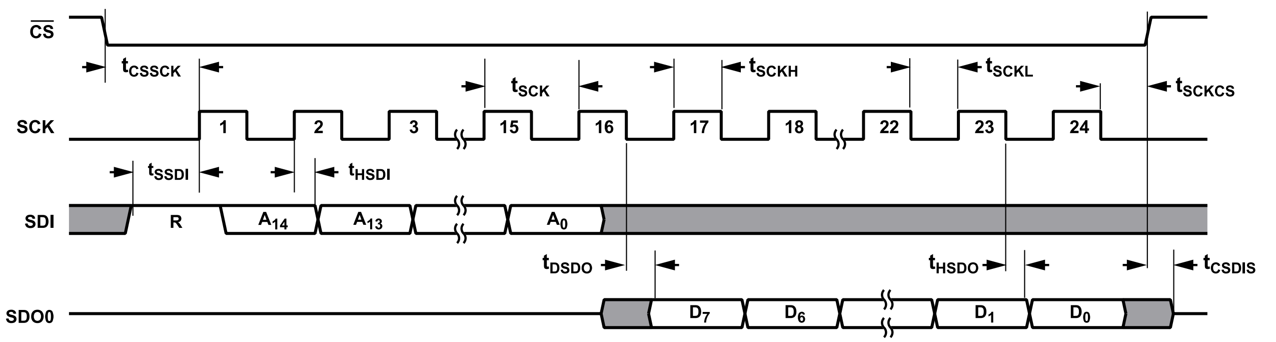


Figure 4. Register Configuration Mode Read Timing

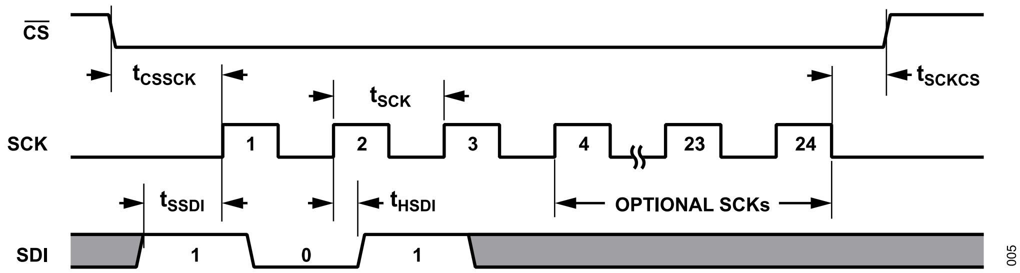


Figure 5. Register Configuration Mode Command Timing

Table 4. SPI Compatible Mode Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCK}				
VIO > 1.71 V		9.8			ns
VIO > 1.14 V		12.3			ns
SCK Low Time	t_{SCKL}				
VIO > 1.71 V		4.2			ns
VIO > 1.14 V		5.2			ns
SCK High Time	t_{SCKH}				
VIO > 1.71 V		4.2			ns
VIO > 1.14 V		5.2			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	1.4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 1.71 V				5.6	ns
VIO > 1.14 V				8.1	ns
$\overline{CS}$ Falling Edge to SDO Valid	t_{CSEN}				ns
VIO > 1.71 V				6.8	ns

SPECIFICATIONS

Table 4. SPI Compatible Mode Timing (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
VIO > 1.14 V				9.3	ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}				
VIO > 1.71 V		9.8			ns
VIO > 1.14 V		12.3			ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	4.2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns
$\overline{CS}$ Falling Edge to BUSY Rising Edge	t_{CSBUSY}		6		ns

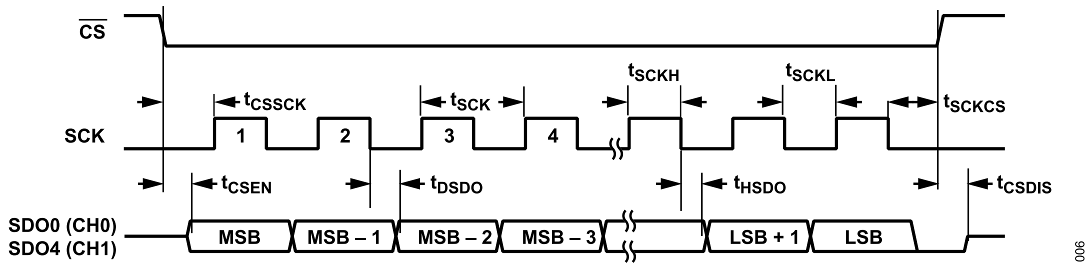


Figure 6. SPI Clocking Mode 1-Lane SDR Timing

Table 5. Echo Clock Mode Timing, SDR, 1-Lane

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCK}				
VIO > 1.71 V		9.8			ns
VIO > 1.14 V		12.3			ns
SCK Low Time, SCK High Time	t_{SCKL}, t_{SCKH}				
VIO > 1.71 V		4.2			ns
VIO > 1.14 V		5.2			ns
SCK Rising Edge to Data/SCKOUT Remains Valid	t_{HSDO}	1.1			ns
SCK Rising Edge to Data/SCKOUT Valid Delay	t_{DSDO}				
VIO > 1.71 V				5.6	ns
VIO > 1.14 V				8.1	ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}				
VIO > 1.71 V		9.8			ns
VIO > 1.14 V		12.3			ns
Skew Between Data and SCKOUT	t_{SKEW}	−0.4	0	+0.4	ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	4.2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns

SPECIFICATIONS

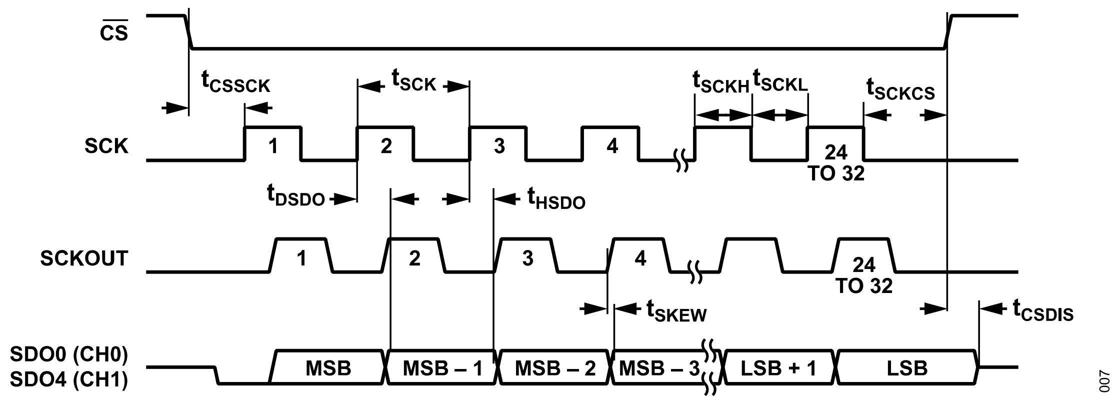


Figure 7. Echo Clock Mode Timing, SDR, 1-Lane

Table 6. Echo Clock Mode Timing, DDR, 1-Lane

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCK}	12.3			ns
SCK Low Time, SCK High Time	t_{SCKL}, t_{SCKH}	5.2			ns
SCK Edge to Data/SCKOUT Remains Valid	t_{HSDO}	1.1			ns
SCK Edge to Data/SCKOUT Valid Delay	t_{DSDO}				
VIO > 1.71 V				6.2	ns
VIO > 1.14 V				8.7	ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}	12.3			ns
Skew Between Data and SCKOUT	t_{SKEW}	−0.4	0	+0.4	ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	9			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns

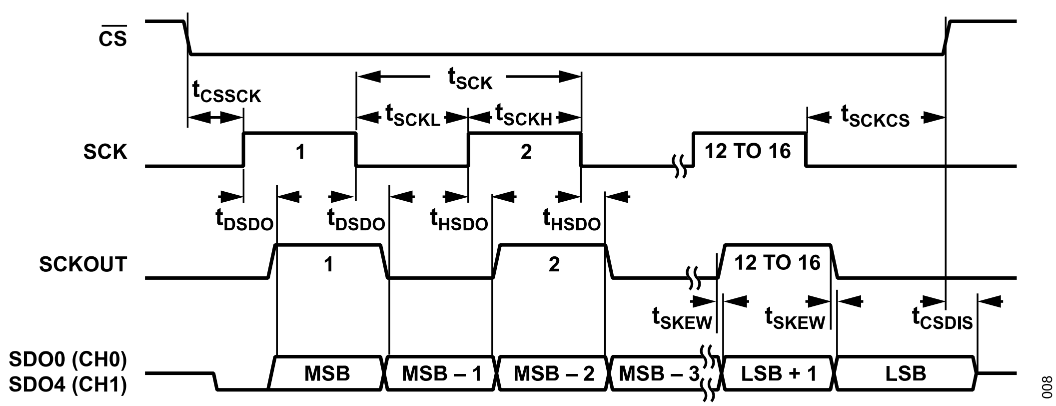


Figure 8. Echo Clock Mode Timing, DDR, 1-Lane

Table 7. Host Clock Mode Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCKOUT}				
OSC_DIV = No Divide		11.8	12.5	13.3	ns
OSC_DIV = Divide by 2		23.6	25	26.6	ns
OSC_DIV = Divide by 4		47.4	50	53.2	ns
SCK Low Time	$t_{SCKOUTL}$	0.45 × t_{SCKOUT}		0.55 × t_{SCKOUT}	ns
SCK High Time	$t_{SCKOUTH}$	0.45 × t_{SCKOUT}		0.55 × t_{SCKOUT}	ns
$\overline{CS}$ Falling Edge to First SCKOUT Rising Edge	$t_{DSCKOUT}$				

SPECIFICATIONS

Table 7. Host Clock Mode Timing (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
VIO > 1.71 V		10	13.6	19	ns
VIO > 1.14 V		10	15	21	ns
Skew Between Data and SCKOUT	t_{SKEW}	−0.4	0	+0.4	ns
Last SCKOUT Edge to $\overline{CS}$ Rising Edge	$t_{SCKOUTCS}$	5.2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns

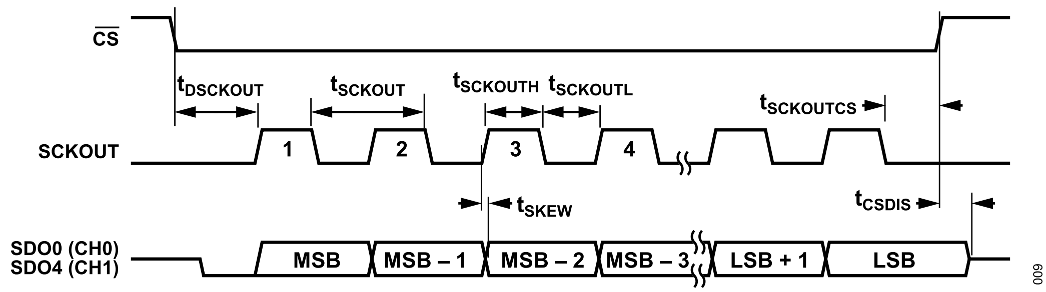


Figure 9. Host Clock Mode Timing, SDR, 1-Lane

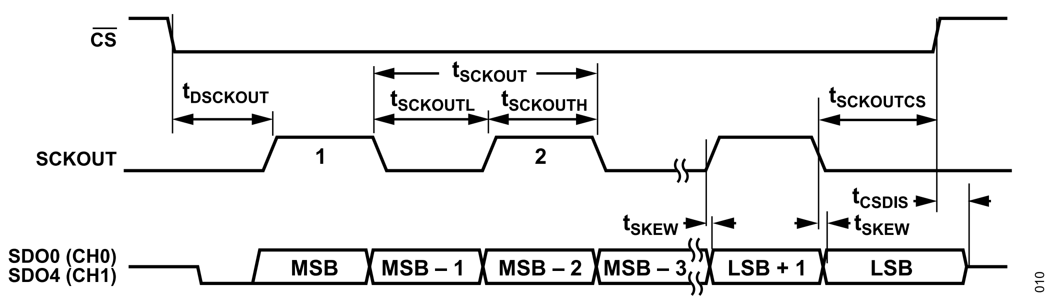


Figure 10. Host Clock Mode Timing, DDR, 1-Lane

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
IN1+, IN1−, IN0+, IN0−, REFIN to GND	−0.3 V to VDD_5V + 0.3 V
Supply Voltage	
VDD_5V, REF to GND	−0.3 V to +6.0 V
VDD_1.8V, VIO to GND	−0.3 V to +2.1 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
CNV to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−55°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Maximum Reflow (Package Body) Temperature	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
05-08-1797	35	16	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

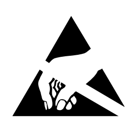
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4630-24/AD4632-24

Table 10. AD4630-24/AD4632-24, 64-Ball CSP_BGA

ESD Model	Withstand Threshold (kV)	Class
HBM	4	3A
FICDM	1.25	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

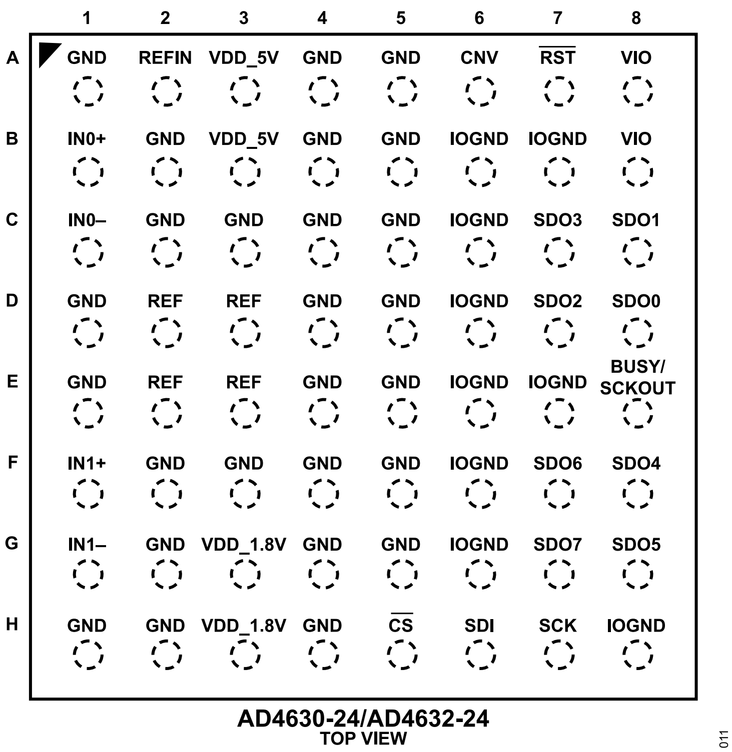


Figure 11. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, D1, E1, H1, B2, C2, F2, G2, H2, C3, F3, A4, B4, C4, D4, E4, F4, G4, H4, A5, B5, C5, D5, E5, F5, G5	GND	P	Power Supply Ground.
A2	REFIN	AI	Buffered Reference Input. When using the internal reference buffer, drive REFIN with 4.096 V to 5 V (referred to GND). To disable the reference buffer, tie REFIN to GND and drive REF with 4.096 V to 5 V.
A3, B3	VDD_5V	P	5 V Power Supply. The range of VDD_5V depends on the reference value: 5.3 V to 5.5 V for a 5 V reference, and 4.75 V to 5.25 V for a 4.096 V reference. This pin has a 1 µF bypass capacitor inside the package.
A6	CNV	DI	Convert Input. A rising edge on this input powers up the device and initiates a new conversion. This signal must have low jitter to achieve the specified performance of the ADC. The logic levels are determined by VIO.
A7	$\overline{\text{RST}}$	DI	Reset Input (Active Low). Asynchronous device reset.
A8, B8	VIO	P	Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8 V, 1.5 V, or 1.2 V). This pin has a 0.2 µF bypass capacitor inside the package. For VIO < 1.4 V, Bit IO2X of the output driver register must be set to 1.
B1	IN0+	AI	Channel 0 Positive Analog Input.
B6, B7, C6, D6, E6, E7, F6, G6, H8	IOGND	P	VIO Ground. Connect to the same ground plane as GND.
C1	IN0−	AI	Channel 0 Negative Analog Input.
C7	SDO3	DO	Channel 0 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
C8	SDO1	DO	Channel 0 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
D2, D3, E2, E3	REF	AI	Optional Unbuffered Reference Input. Drive REF with 4.096 V to 5 V (referred to GND). This pin has a 2 µF bypass capacitor inside the package. When using the internal reference buffer, do not connect REF.
D7	SDO2	DO	Channel 0 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
D8	SDO0	DO	Channel 0 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
E8	BUSY/SCKOUT	DO	BUSY Indicator in SPI Clocking Mode. This pin goes high at the start of a new conversion and returns low when the conversion finishes. The logic levels are determined by VIO. When SCKOUT is enabled, this pin function is either an echo of the incoming SCK from the host controller or a clock sourced by the internal oscillator.
F1	IN1+	AI	Channel 1 Positive Analog Input.
F7	SDO6	DO	Channel 1 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
F8	SDO4	DO	Channel 1 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
G1	IN1−	AI	Channel 1 Negative Analog Input.
G3, H3	VDD_1.8V	P	1.8 V Power Supply. The range of VDD_1.8V is 1.71 V to 1.89 V. This pin has a 1 µF bypass capacitor inside the package.
G7	SDO7	DO	Channel 1 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
G8	SDO5	DO	Channel 1 Serial Data Output. The conversion result outputs on this pin. It is synchronized to SCK.
H5	$\overline{CS}$	DI	Chip Select Input (Active Low).
H6	SDI	DI	Serial Data Input.
H7	SCK	DI	Serial Data Clock Input. When the device is selected ($\overline{CS}$ = low), the conversion result is shifted out by this clock.

[1] AI is analog input, P is power, DI is digital input, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD_5V = 5.4 V, VDD_1.8V = 1.8 V, VIO = 1.8 V, REFIN = 5 V, input common mode = 2.5 V, f_S = 2 MSPS, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C.

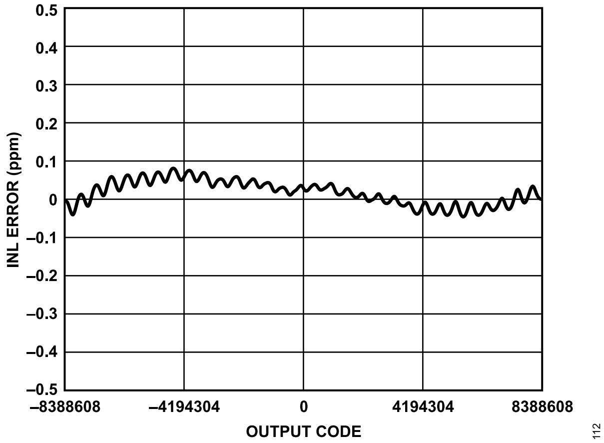


Figure 12. INL Error vs. Output Code, Differential Input

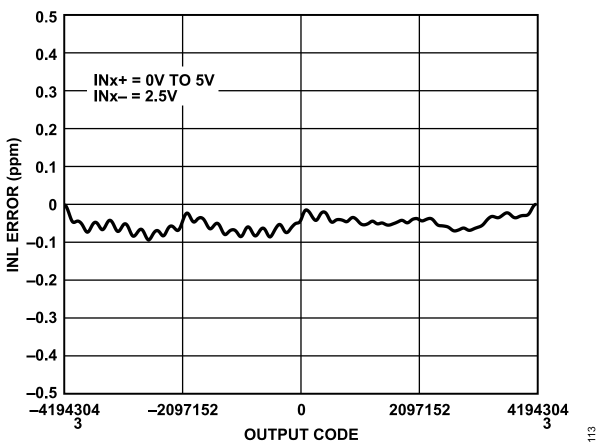


Figure 13. INL Error vs. Output Code, Single-Ended Input

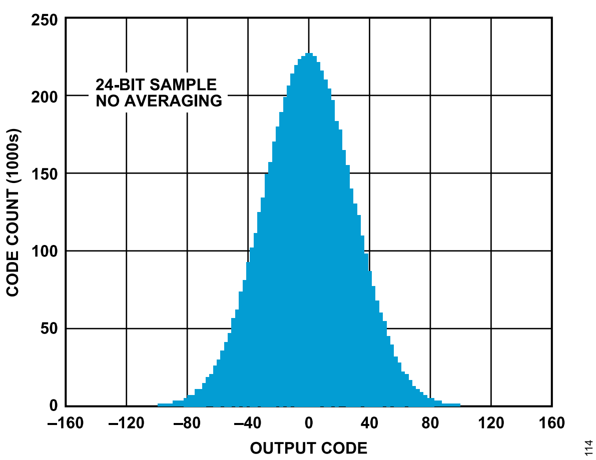


Figure 14. Code Histogram for Shorted Inputs

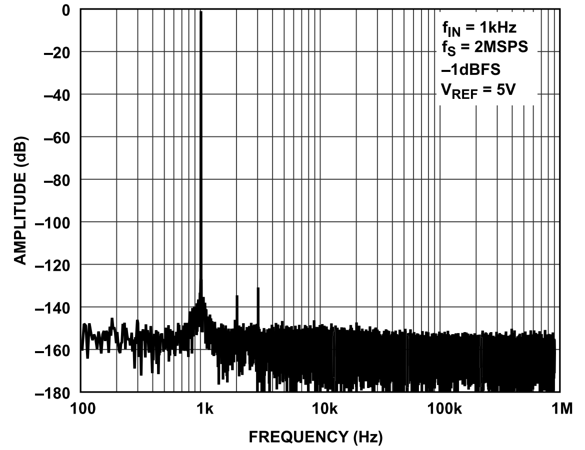


Figure 15. FFT, 2 MSPS, f_{IN} = 1 kHz, V_{REF} = 5 V

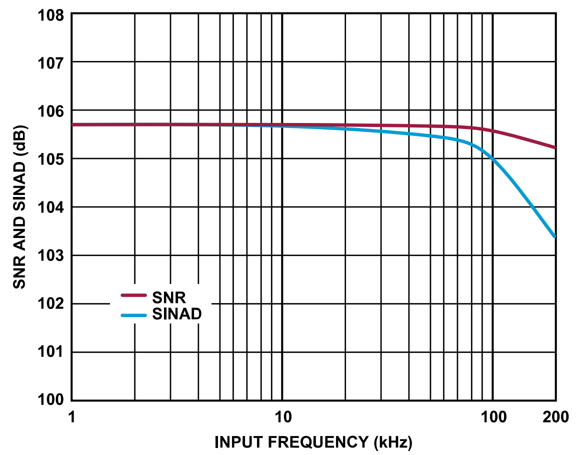


Figure 16. SNR and SINAD vs. Input Frequency

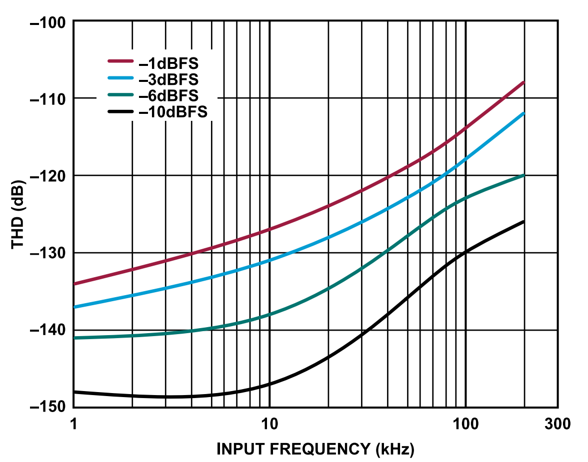


Figure 17. THD vs. Input Frequency and Amplitude

TYPICAL PERFORMANCE CHARACTERISTICS

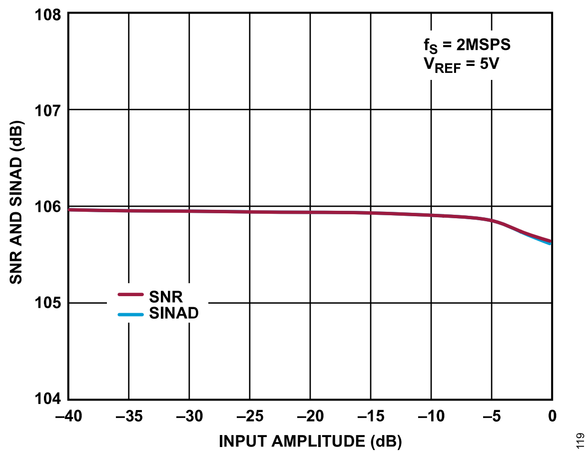


Figure 18. SNR and SINAD vs. Input Amplitude, f_{IN} = 1 kHz

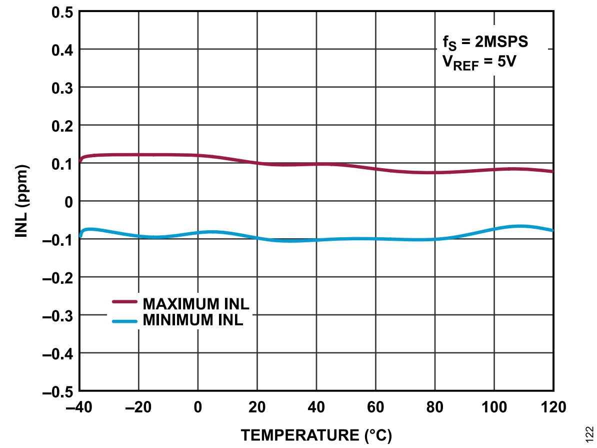


Figure 21. INL vs. Temperature

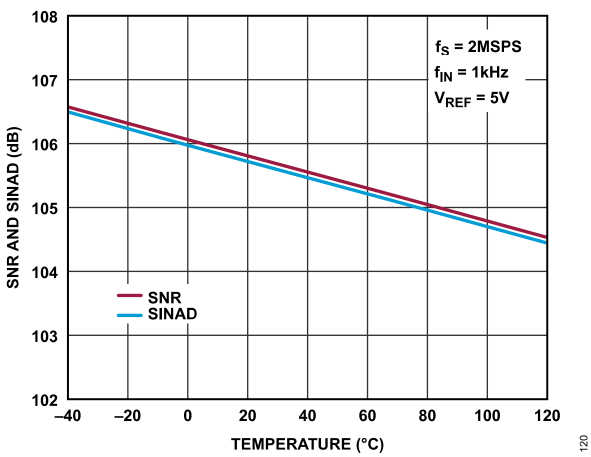


Figure 19. SNR and SINAD vs. Temperature, f_{IN} = 1 kHz

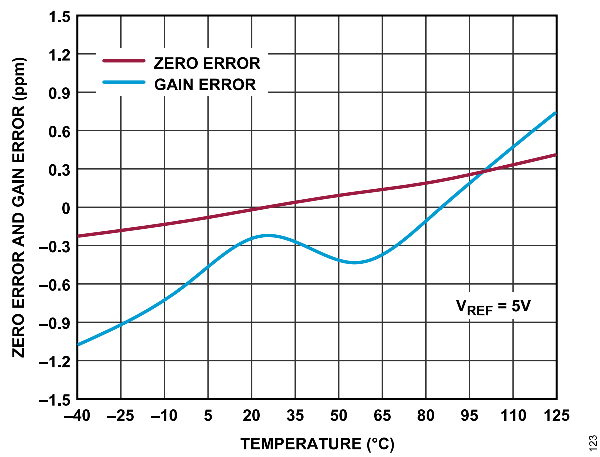


Figure 22. Zero Error and Gain Error vs. Temperature

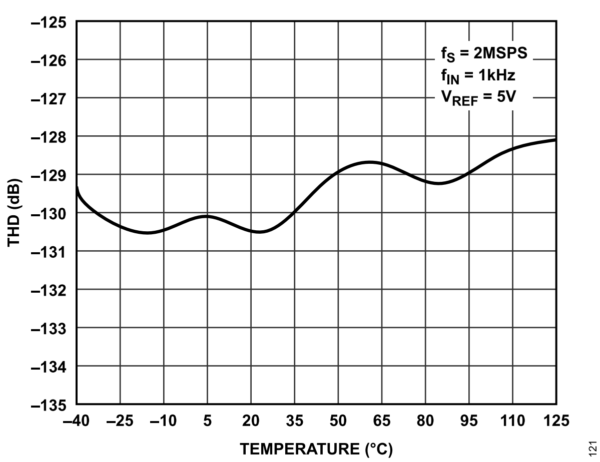


Figure 20. THD vs. Temperature, f_{IN} = 1 kHz

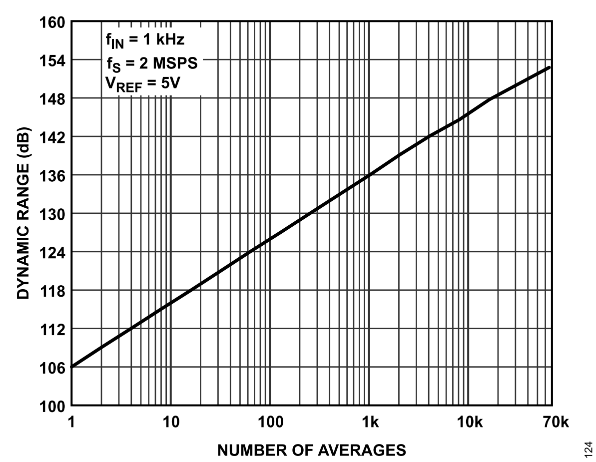


Figure 23. Dynamic Range vs. Number of Averages

TYPICAL PERFORMANCE CHARACTERISTICS

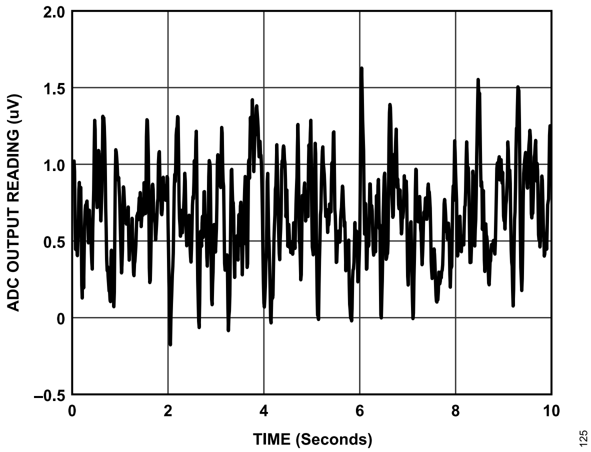


Figure 24. Low Frequency Noise (Output Data Rate = 19.5 SPS After Averaging Blocks of 2048 Samples)

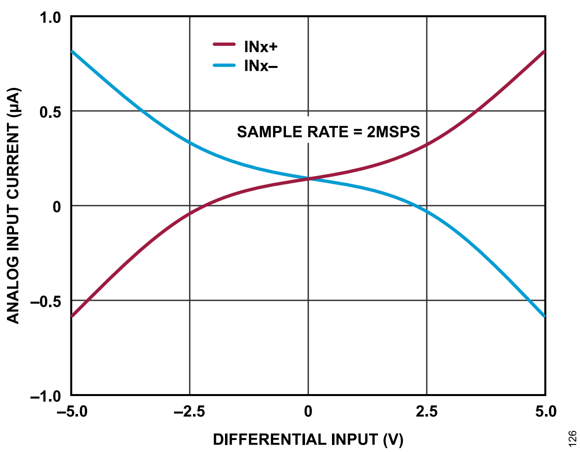


Figure 25. Analog Input Current vs. Differential Input, AD4630-24, 2 MSPS

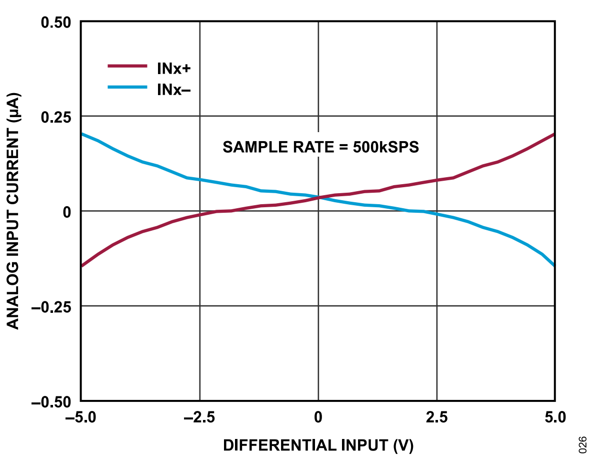


Figure 26. Analog Input Current vs. Differential Input, AD4632-24, 500 kSPS

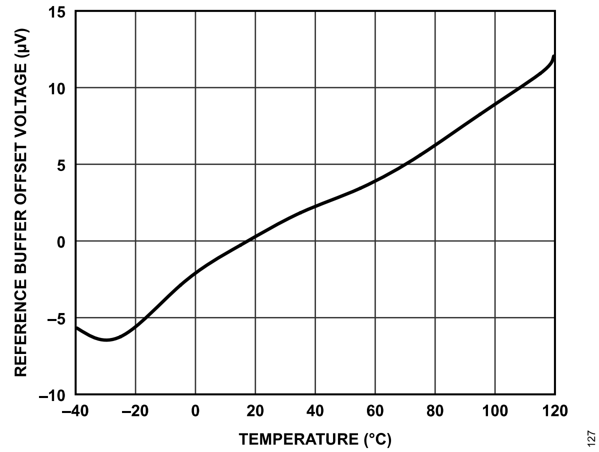


Figure 27. Reference Buffer Offset Voltage vs. Temperature

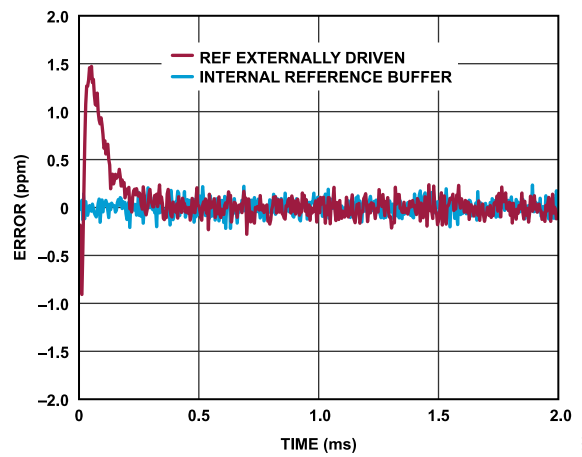


Figure 28. Error During Conversion Burst After Long Idle Time

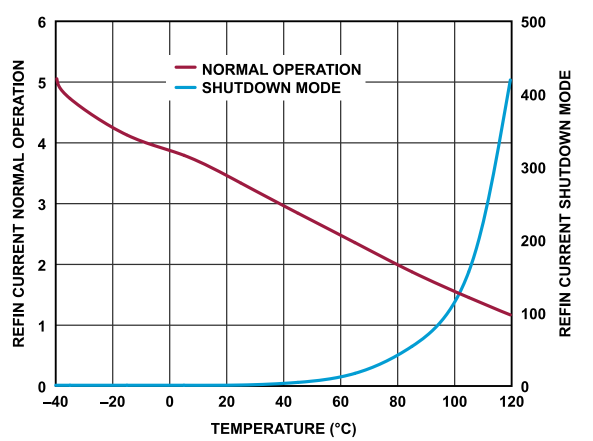


Figure 29. REFIN Current Normal Operation and REFIN Current Shutdown Mode vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

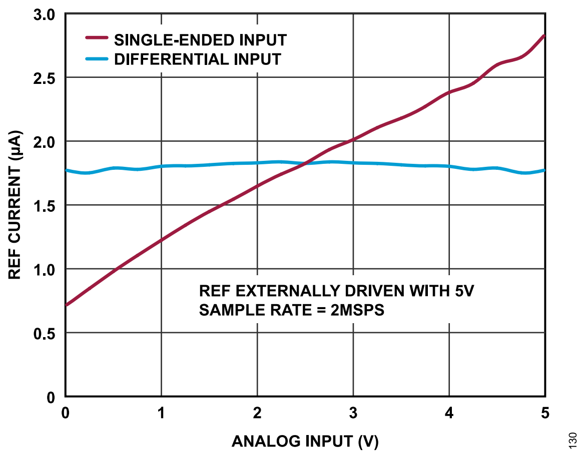


Figure 30. REF Current vs. Analog Input, AD4630-24, 2 MSPS

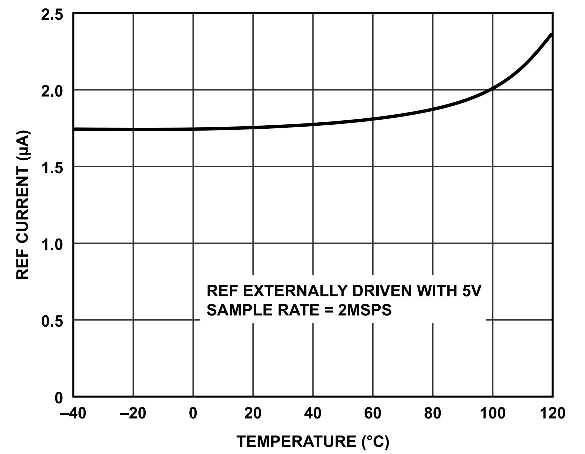


Figure 33. REF Current vs. Temperature

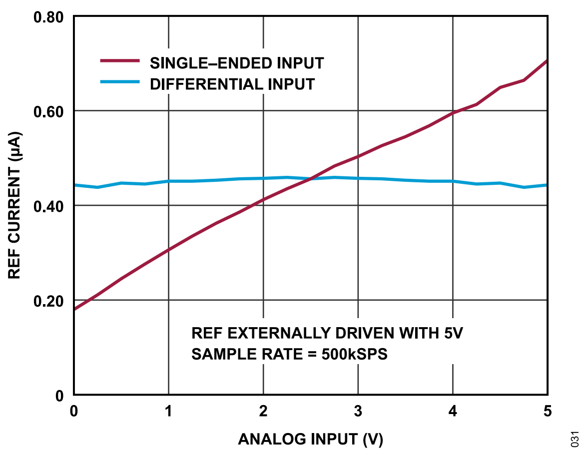


Figure 31. REF Current vs. Analog Input, AD4632-24, 500 kSPS

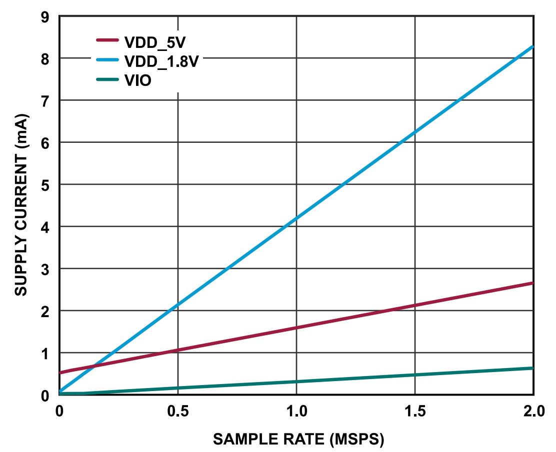


Figure 34. Supply Current vs. Sample Rate

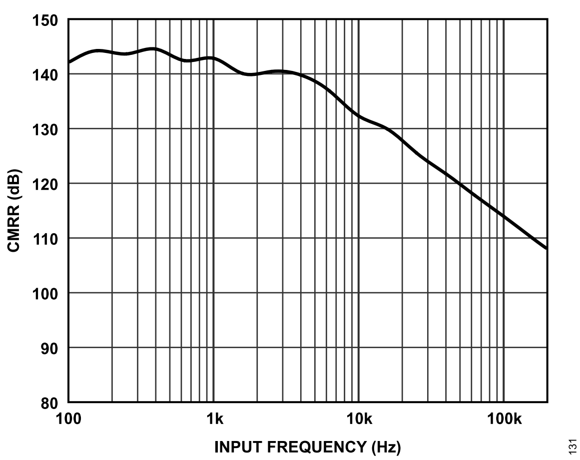


Figure 32. CMRR vs. Input Frequency

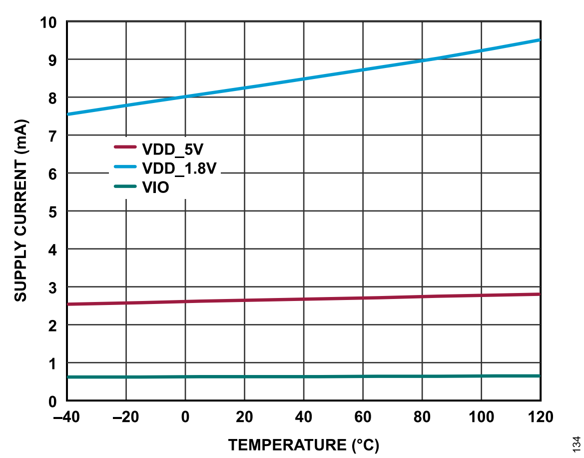


Figure 35. Supply Current vs. Temperature, AD4630-24, 2 MSPS

TYPICAL PERFORMANCE CHARACTERISTICS

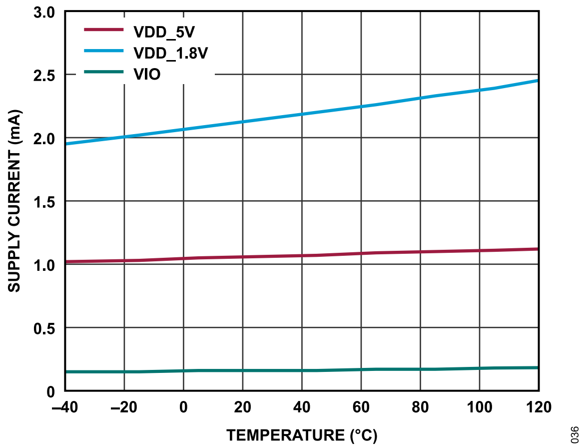


Figure 36. Supply Current vs. Temperature, AD4632-24, 500 kSPS

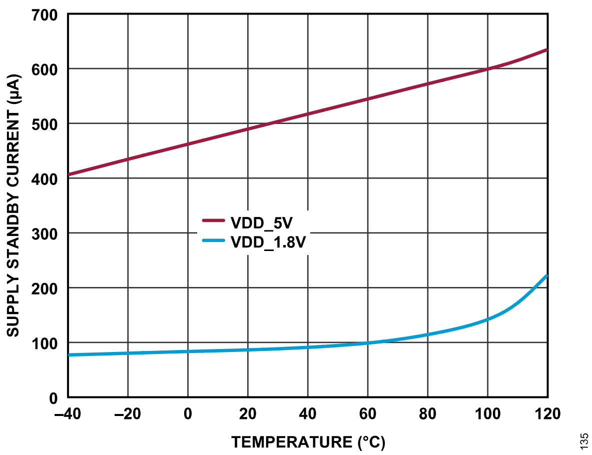


Figure 37. Supply Standby Current vs. Temperature

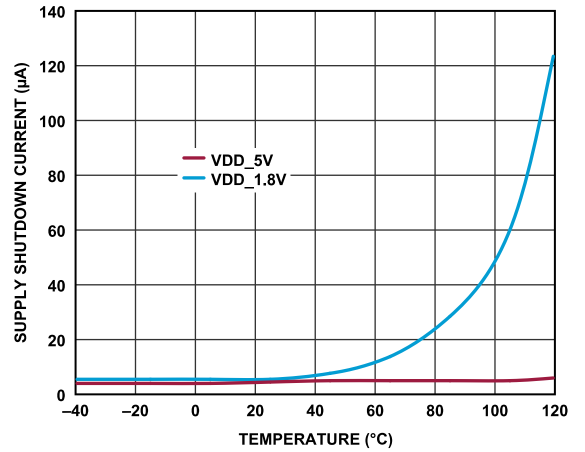


Figure 38. Supply Shutdown Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL) Error

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 40).

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error (ZE)

Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

Gain Error (GE)

The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of a full-scale input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD as follows: ENOB = (SINAD dB − 1.76)/ 6.02. ENOB is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range (DR)

Dynamic range is the rms voltage of a full-scale sine wave to the total rms voltage of the noise measured. The value for dynamic range is expressed in decibels. Dynamic range is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms voltage of a full-scale sine wave to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms voltage of a full-scale sine wave to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 4.5 V p-p sine wave applied to the input common-mode voltage of frequency, f.

$$CMRR(dB) = 10 \times \log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:
P_{ADC_IN} is the common-mode power at the frequency, f, applied to the inputs.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

THEORY OF OPERATION

Figure 39 shows the basic functions of the AD4630-24/AD4632-24.

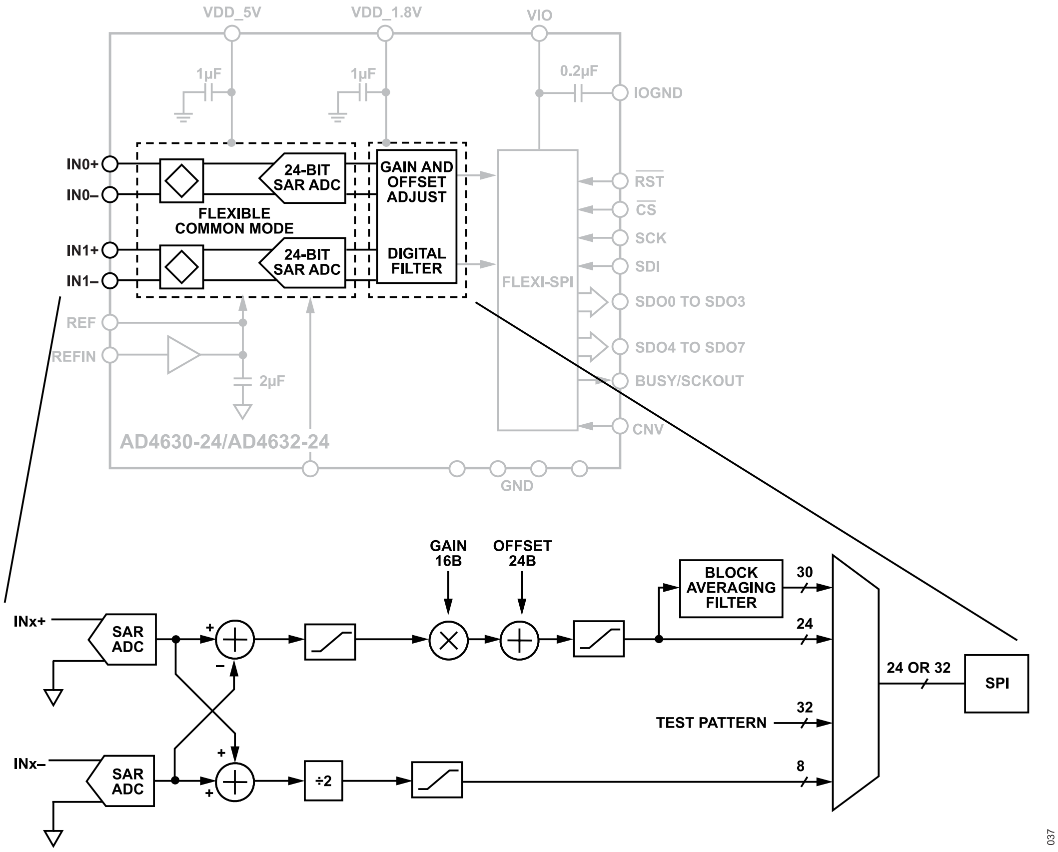


Figure 39. Functional Block Diagram and Channel Architecture

OVERVIEW

The AD4630-24/AD4632-24 are low noise, low power, high speed, dual 24-bit SAR ADCs. The AD4630-24 is capable of converting 2,000,000 samples per second (2 MSPS), and the AD4632-24 is capable of converting 500,000 samples per second (500 kSPS). The AD4630-24/AD4632-24 offer several analog and digital features to ease system design. The analog features include a wide common-mode range, which eases level shifting requirements, as well as an extended fully differential input range of ±(65/64) × V_{REF}, which eases the margin requirements on signal conditioning.

The AD4630-24/AD4632-24 have an integrated reference buffer with an integrated decoupling capacitor to minimize the external components on board. The on-chip track-and-hold circuitry does not exhibit any pipeline delay or latency, making this circuitry ideal for control loops and high speed applications. The digital features include offset correction, gain adjustment, and averaging, which offload the host processor. The user can configure the device for one of several output code formats (see the Summary of Selectable Output Data Formats section).

The AD4630-24/AD4632-24 uses a Flexi-SPI, allowing the data to be accessed via multiple SPI lanes, which relaxes clocking requirements for the host SPI controller. An echo clock mode is also available to assist in data clocking, simplifying the use of isolated data interfaces. The AD4630-24/AD4632-24 have a valid first conversion after exiting power-down mode. The architecture achieves ±0.9 ppm INL maximum, with no missing codes at 24 bits and 105.7 dB SNR. The AD4630-24 dissipates only 15 mW per channel at 2 MSPS.

CONVERTER OPERATION

The AD4630-24/AD4632-24 operate in two phases: acquisition phase and conversion phase. In the acquisition phase, the internal track-and-hold circuitry is connected to each input pin (INx+, INx−) and samples the voltage on each pin independently. Issuing a rising edge pulse on the CNV pin initiates a conversion. The rising edge pulse on the CNV pin also asserts the BUSY signal to indicate a conversion in progress. At the end of conversion, the BUSY signal deasserts. The conversion result is a 24-bit code or a 16-bit code representing the input voltage difference and an 8-bit code representing the input common-mode voltage. Depending on the device configuration, this conversion result can be processed digitally and latched into the output register. The acquisition circuit on each input pin is also precharged to the previous sample voltage, which minimizes the kickback charge to the input driver. The host

THEORY OF OPERATION

processor retrieves the output code via the SDOx pins that are internally connected to the output register.

TRANSFER FUNCTION

In the default configuration, the AD4630-24/AD4632-24 digitize the full-scale difference voltage of 2 × V_{REF} into 2^{24} levels, resulting in an LSB size of 0.596 µV with V_{REF} = 5 V. Note that 1 LSB at 24 bits is approximately 0.06 ppm. The ideal transfer function is shown in Figure 40. The differential output data is in twos complement format. Table 12 summarizes the mapping of input voltages to differential output codes.

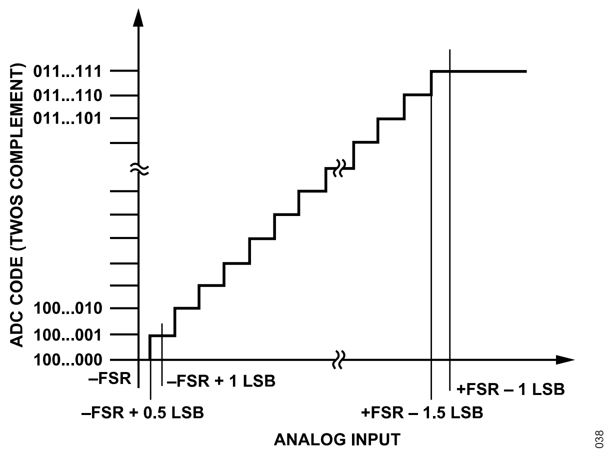


Figure 40. ADC Ideal Transfer Function for the Differential Output Codes (FSR Is Full-Scale Range)

Table 12. Input Voltage to Output Code Mapping

Description	Analog Input Voltage Difference	Digital Output Code (Twos Complement, Hex)
FSR − 1 LSB	(8388607 × V_{REF})/(8388608)	0x7FFFFF
Midscale + 1 LSB	V_{REF}/(8388608)	0x000001
Midscale	0 V	0x000000
Midscale − 1 LSB	−V_{REF}/(8388608)	0xFFFFFF
−FSR + 1 LSB	−(8388607 × V_{REF})/(8388608)	0x800001
−FSR	−V_{REF}	0x800000

ANALOG FEATURES

The common-mode voltage is not restricted except by the absolute voltage range for each input (from −1/128 × V_{REF} to 129/128 × V_{REF}). The analog inputs can be modeled by the equivalent circuit shown in Figure 41. In the acquisition phase, each input sees approximately 58 pF (C_{IN}) from the sampling capacitor in series with 37 Ω on resistance (R_{ON}) of the sampling switch. During the conversion phase, each input sees C_{PIN}, which is about 2 pF. Any signal that is common to both inputs is reduced by the common-mode rejection of the ADC. During the conversion, the analog inputs draw only a small leakage current.

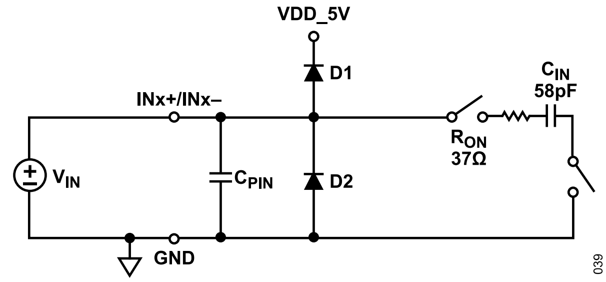


Figure 41. Equivalent Circuit for the AD4630-24/AD4632-24 Differential Analog Input

Each input is sampled independently. The conversion results do not saturate, assuming each input is within the specified full-scale input range. Note that digital domain saturation does occur if the digital offset and digital gain parameters are configured to map the conversion result to numeral values that exceed the full-scale digital range (-2^{23} to $+2^{23}-1$ for the 24-bit word). An input voltage difference up to ±(65/64) × V_{REF} can be captured and converted without saturation by setting the digital gain parameter to a value < 1.

The slew rate at the analog input pins must be less than 400 V/µs during the acquisition phase and less than 30 V/µs at the sampling moment to ensure good performance. This rate can be ensured by choosing values for the external RC circuit such that the RC time constant is more than 12.5 ns (R × C > 12.5e-9).

DIGITAL SAMPLE PROCESSING FEATURES

The AD4630-24/AD4632-24 support several digital and data processing features that can be applied to the signal samples. These features are enabled and disabled via the control registers of the AD4630-24/AD4632-24. Figure 39 contains an ADC channel architecture block diagram showing the digital and data processing features available for each input channel.

Full-Scale Saturation

The conversion results saturate digitally (before any postprocessing) when either or both inputs exceed the specified analog limits. After applying offset and gain scaling, the results are truncated to 24-bit representation (saturating at maximum 0x7FFFFF and minimum 0x800000). Take care to avoid unintentional saturation, especially when applying digital offset and/or gain scaling. See the Digital Offset Adjust and Digital Gain sections for more details on the use of these features.

THEORY OF OPERATION

Common-Mode Output

When the host controller writes 0x1 or 0x2 to the OUT_DATA_MD bit field of the modes register (see the Modes Register section), an 8-bit code representing the input common-mode voltage is appended to the 16-bit or 24-bit code representing the input voltage difference. The LSB size of the 8-bit code is $V_{REF}/256$. The 8-bit code saturates at 0 and 255 when the common-mode input voltage is 0 V and V_{REF}, respectively. The 8-bit code is not affected by digital offset and gain scaling, which is applied only to the code representing the input voltage difference.

Block Averaging

The AD4630-24/AD4632-24 provides a block averaging filter (SINC1) with programmable block length 2^N, where N = 1, 2, 3, …, 16. The filter is reset after processing each block of 2^N samples. The filter is enabled by writing 0x3 to the OUT_DATA_MD bit field of the modes register (see the Modes Register section) as well as a value (1 ≤ N ≤ 16) to the AVG_VAL bit field in the averaging mode register (see the Averaging Mode Register section). In this configuration, the output sample word is 32 bits. The 30 MSBs represent the numerical value of the 24-bit codes averaged in blocks of 2^N samples. The 24 MSBs of the 30-bit code are equal to the 24-bit codes when averaging blocks of constant values. The 31st bit (OR) is an overrange warning bit, which is high when one or more samples in the block are subject to saturation. The 32nd bit (SYNC) is high once every 2^N conversion cycles to indicate when the average values are updated at the end of each block of samples. See the Summary of Selectable Output Data Formats section for the data format when the filter is enabled.

The effective data rate in averaging mode is CNV frequency $(f_{CNV})/2^N$. The reset value of N in the AVG_VAL bit field is 0x00 (no averaging). Figure 62 shows an example timing diagram in averaging mode. Figure 42 shows the frequency response of the filter for N = 1, 2, 3, 4, and 5.

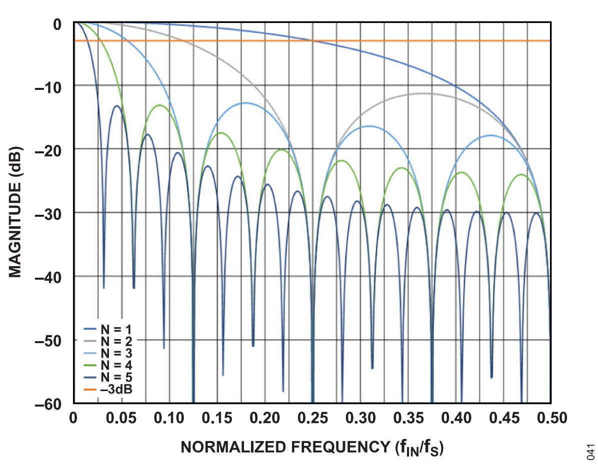


Figure 42. Frequency Response Examples for the Block Averaging Filter

Digital Offset Adjust

Each ADC channel can be independently programmed to add a 24-bit signed offset value to the sample data (see the Register Details section). When adding an offset to the samples, it is possible to cause the sample data to saturate numerically. Take this into account when using the offset feature. The default value is 0x000000. See the Channel 0 Offset Registers section or Channel 1 Offset Registers section in the AD4630-24/AD4632-24 register map for more details.

Digital Gain

Each ADC channel can be programmed independently to apply a 16-bit unsigned digital gain (CHx_USER_GAIN) to the digital samples (see the Register Details section). The gain is applied to each sample based on the following equation:

$$Code_{OUT} = Code_{IN} \times (CHx\_USER\_GAIN/0x8000)$$

where 0x0000 ≤ CHx_USER_GAIN ≤ 0xFFFF.

The effective gain range is 0 to 1.99997. Note that applying gain to the samples can cause numerical saturation. The default value is 0x8000 (gain = 1). To measure input voltage differences exceeding $\pm V_{REF}$, set the gain below unity to avoid the numerical saturation of the 24-bit/16-bit/30-bit output differential codes. See the Channel 0 Gain Registers section or Channel 1 Gain Registers section in the AD4630-24/AD4632-24 register map for more details.

Test Pattern

To facilitate functional testing and debugging of the SPI, the host controller can write a 32-bit test pattern to the AD4630-24/AD4632-24 (see the Test Pattern Registers section). The value written to the test pattern registers applies to both ADC channels, and is output using the normal sample cycle timing on each channel. The 32-bit test pattern output mode is enabled by writing 0x4 to the OUT_DATA_MD bit field of the modes register (see the Modes Register section). The default value stored in the test pattern registers is 0x5A5A0F0F.

THEORY OF OPERATION

Summary of Selectable Output Data Formats

Figure 43 summarizes the output data formats that are available on the AD4630-24/AD4632-24, which are selected in the modes register (see the Modes Register section). Note that the selected mode is applied to both channels. The OR and SYNC flags are each 1 bit.

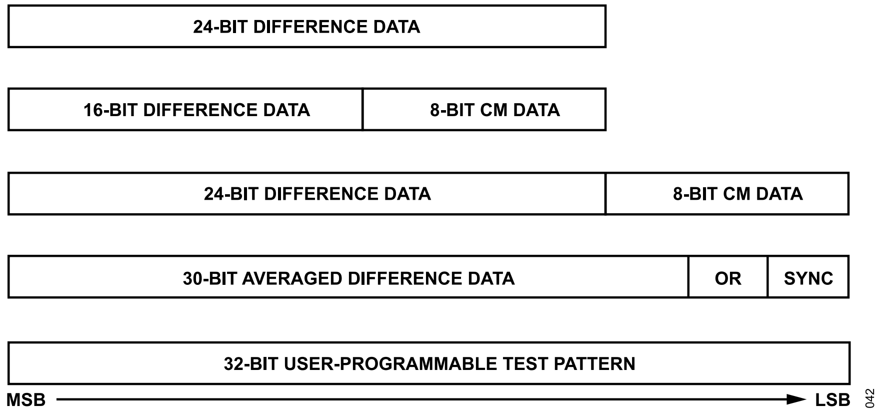


Figure 43. Summary of Selectable Output Sample Formats

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAMS

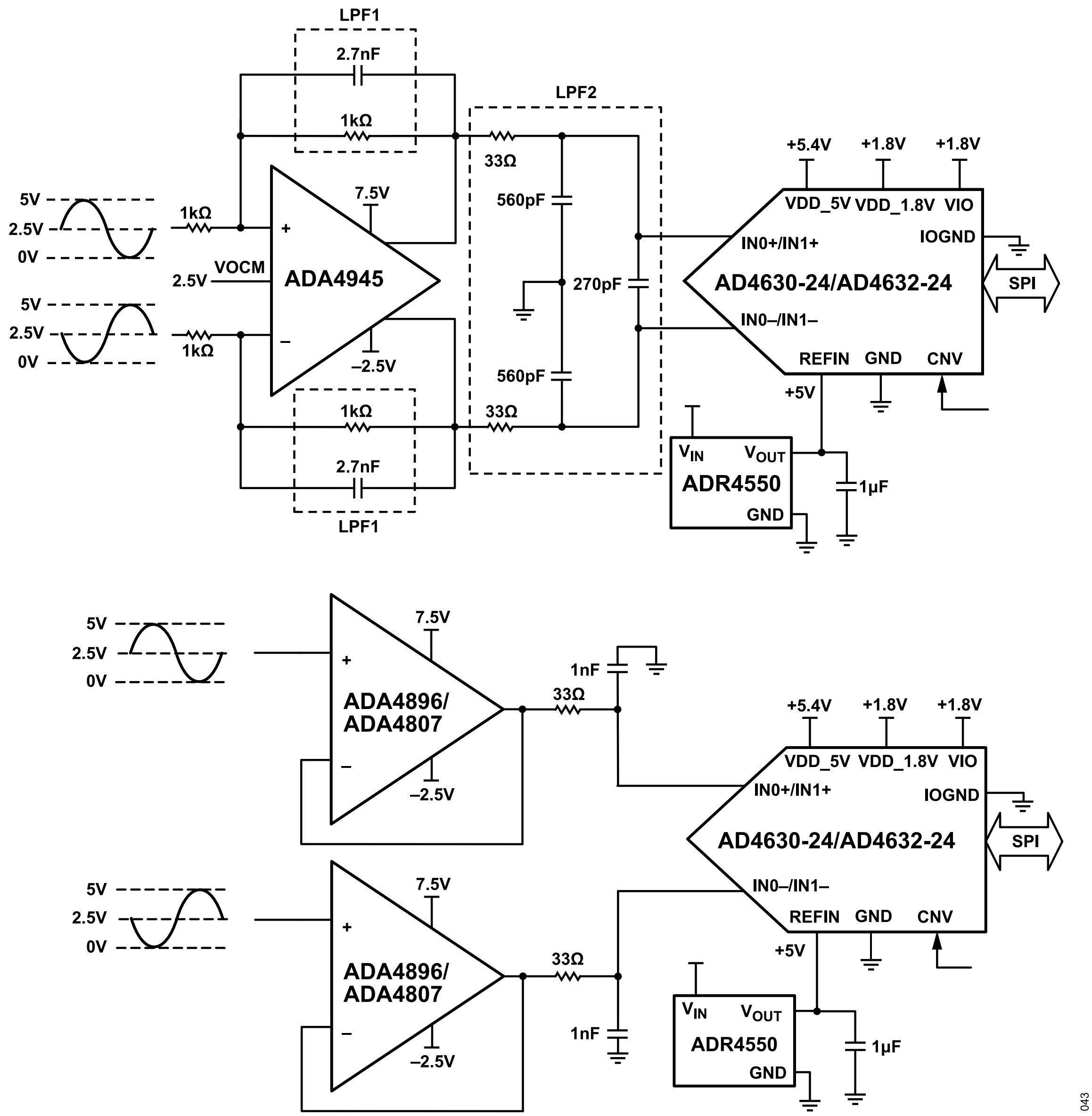


Figure 44. Typical Application Circuit Diagrams

APPLICATIONS INFORMATION

ANALOG FRONT-END DESIGN

Easy Drive Features

A combination of a long acquisition phase and a precharging circuit of the AD4630-24/AD4632-24 family lessens the design challenges associated with the ADC driver stage and increases the flexibility in ADC driver selection. The AD4630-24/AD4632-24 uniquely combine high performance with ease of use features that enable ease of drive, lower overall system power, simplified signal chain bill of materials (BOM), reduced performance sensitivity to external circuitry, and shorter design cycles.

Precharge Buffer

The AD4630-24/AD4632-24 have a precharging circuit as a part of the internal track-and-hold circuitry, which charges the internal sampling capacitors to the previously sampled input voltage. This circuit reduces the charge kickback, making it easier to drive than other conventional SAR ADCs. The reduced kickback, combined with a longer acquisition phase, reduces settling requirements on the driving amplifier. This combination also allows the use of larger resistor values, which are beneficial for improving amplifier stability. Furthermore, the bandwidth of the RC filter is reduced, resulting in lower noise and/or power consumption of the signal chain.

Long Acquisition Phase

The AD4630-24/AD4632-24 also feature a fast conversion time that results in a long acquisition phase. A long acquisition phase reduces the settling requirement on the driving amplifier, and a lower power and lower bandwidth amplifier can be chosen. The longer acquisition phase means that a lower RC input filter cutoff can be used, which means a noisier amplifier can also be tolerated. A larger value of R can be used in the RC filter with a corresponding smaller value of C, reducing amplifier stability concerns without affecting distortion performance significantly. A larger value of R also results in reduced dynamic power dissipation in the amplifier.

Driver Amplifier Choice

Although the AD4630-24/AD4632-24 use easy to drive technology, which broadens the range of companion circuitry that is capable of driving this ADC, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept low enough to preserve the SNR and transition noise performance of the AD4630-24/AD4632-24. The noise from the driver is filtered by the single-pole, low-pass filter of the analog input circuit made by R_{ON} and C_{IN}, or by the external filter, if one is used. Because the typical noise of the AD4630-24/AD4632-24 is 17.7 µVrms, the SNR degradation due to the amplifier is the following:

$$SNR_{LOSS} = 20 \times \log_{10}\left(\frac{17.7 \times 10^{-6}\text{V}}{\sqrt{\left(17.7 \times 10^{-6}\text{V}\right)^2 + \frac{\pi}{2} \times f_{-3\ \text{dB}}\left(N \times e_N\right)^2}}\right) \quad (1)$$

  where:
  $f_{-3\ dB}$ is the input bandwidth, in hertz, of the AD4630-24 (74 MHz) or the cutoff frequency of the input filter, if one is used (see Figure 45).
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the operational amplifier, in V/√Hz.

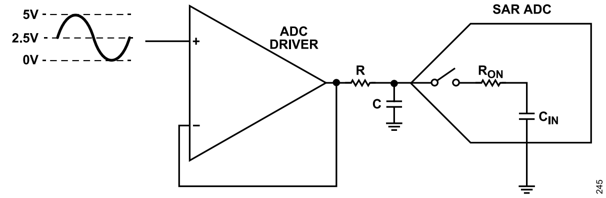


Figure 45. External Filter Example

- For AC applications, the driver must have a THD performance commensurate with the AD4630-24/AD4632-24.
- For multichannel multiplexed applications, the driver amplifier and the analog input circuit of the AD4630-24/AD4632-24 must settle for a full-scale step onto the capacitor array at a 24-bit level. In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. Settling at 0.1% to 0.01% may differ significantly from the settling time at a 24-bit level and must be verified prior to driver selection.

Figure 44 shows two examples for driving the AD4630-24/AD4632-24. Either amplifier can be combined with an upstream stage that provides additional signal conditioning. Both amplifiers can accommodate single-ended or differential inputs. To take advantage of the excellent SNR and THD performance of the AD4630-24/AD4632-24, choose a driver amplifier that has low noise and THD sufficient to meet the application requirements. In addition to the amplifiers shown in Figure 44, the LTC6227 is another driver option.

Analog Devices, Inc., offers several companion driver amplifiers that can be found on the Differential Amplifiers and ADC Drivers web page. The Precision ADC Driver Tool can be used to model the settling behavior and estimate the ac performance of the AD4630-24 with a selected driver amplifier and RC filter. Once the Precision ADC Driver Tool has modeled a specific circuit, the circuit can be exported for simulation in LTspice.

MULTIPLEXED APPLICATIONS

The AD4630-24/AD4632-24 significantly reduce system complexity for multiplexed applications that require superior performance in terms of noise, power, and throughput. Figure 46 shows a simplified block diagram of a multiplexed data acquisition system including a multiplexer, an ADC driver, and a precision SAR ADC.

Switching multiplexer channels typically results in large voltage steps at the ADC inputs. To ensure an accurate conversion result, the step must be given adequate time to settle before the ADC samples its inputs (on the rising edge of CNV). The settling time

APPLICATIONS INFORMATION

error is dependent on the drive circuitry (multiplexer and ADC driver), RC filter values, and the time when the multiplexer channels are switched.

Switch the multiplexer channels just after the conversion phase has elapsed to maximize settling time and to prevent corruption of the conversion result. To avoid conversion corruption, do not switch the channels during conversion time (BUSY high) and quiet time ($t_{QUIET\_CNV\_AVD}$). If the analog inputs are multiplexed during conversion time or quiet time, the current conversion is possibly corrupted.

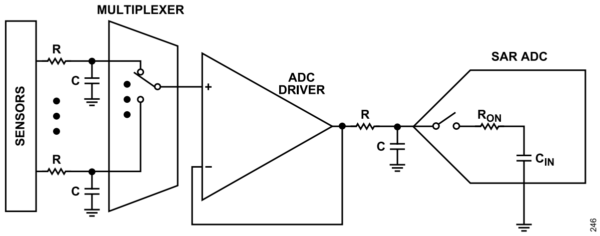


Figure 46. Multiplexed Data Acquisition Signal Using the AD4630-24/ AD4632-24

REFERENCE CIRCUITRY DESIGN

The AD4630-24/AD4632-24 require an external reference to define the input range. This reference must be 4.096 V to 5 V. An optimal choice for the reference is the ADR4550 or ADR4540. The ADC has several features that reduce the charge pulled from the reference, making the AD4630-24/AD4632-24 easier to use than other ADCs. For most applications, the reference can drive the REFIN pin, which has an internal precision buffer that isolates the reference from the ADC circuitry. The buffer has a high input impedance and small input current (5 nA typical) that allows multiple ADCs to share a common reference. An RC circuit between the reference and REFIN can be used to filter reference noise (see Figure 47). The suggested values are 100 Ω < R < 1 kΩ, and C ≥ 10 µF.

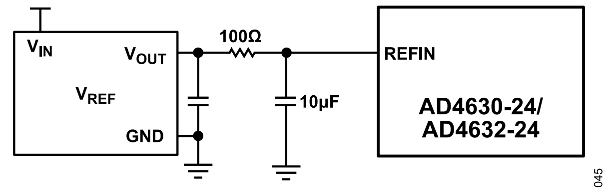


Figure 47. Reference with Noise Filter

For the best possible gain error, the internal buffer can be disabled (REFIN = 0 V) and an external reference used to drive the REF pin. The current drawn by the REF pin is small (<2 µA) and depends on the sample rate and output code (see Figure 30). An internal 2 µF capacitor on the REF pin provides optimal reference bypassing and simplifies PCB design by reducing component count and layout sensitivity.

In applications where a burst of samples is taken after idling for long periods, as shown in Figure 48, the reference current (I_{REF}) quickly goes from approximately 0 µA to a maximum of 1.8 µA at 2 MSPS on the AD4630-24 or a maximum of 0.5 µA at 500 kSPS on the AD4632-24. This step in dc current draw triggers a transient response in the reference that must be considered because any deviation in the reference output voltage affects the accuracy of the output code. If the reference is driving the REFIN pin, the internal buffer is able to handle these transitions (see Figure 28). When the REF pin is being driven with no external buffer, and the transient response of the reference is important, the fast settling LTC6655LN-5 reference is recommended.

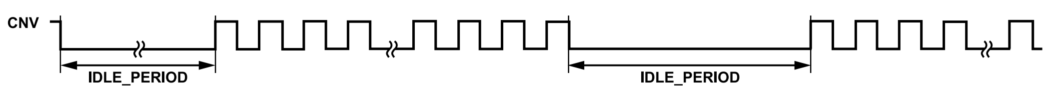


Figure 48. CNV Waveform Showing Burst Sampling

APPLICATIONS INFORMATION

DEVICE RESET

The AD4630-24/AD4632-24 provide two options for performing a device reset using the serial interface. A hardware reset is initiated by pulsing the voltage on the $\overline{RST}$ pin low. A software reset is initiated by setting both the SW_RESET and SW_RESETX bits in the Interface Configuration A register to 1 in the same write instruction (see the Interface Configuration A Register section).

Performing a hardware or software reset asserts the RESET_OCCURRED bit in the digital diagnostics register (see the Digital Diagnostics Register section). The RESET_ OCCURRED bit is cleared by writing it with a 1. RESET_ OCCURRED can be used by the digital host to confirm the AD4630-24/AD4632-24 executed a device reset.

The AD4630-24/AD4632-24 are designed to generate a power-on reset (POR) when VDD_5V and VDD_1.8V are first applied. A POR resets the state of the user configuration registers and asserts the RESET_ OCCURRED bit. If VDD_5V or VDD_1.8V drops below its specified operating range, a POR occurs. Perform a hardware or software reset after a POR.

Figure 49 shows the timing diagram for performing a device reset using the $\overline{RST}$ input. The minimum $\overline{RST}$ pulse width is 50 ns, represented by t_{RESET_PW} in Figure 49 and Table 1. Perform a reset no sooner than 3 ms after the power supplies are valid and stable (this delay is represented by t_{RESET_DELAY} in Figure 49 and Table 1).

After a hardware or software reset, no SPI commands or conversions can be started for 750 µs.

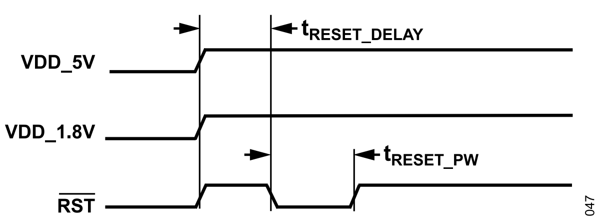


Figure 49. Power-On Reset (POR) Timing

POWER SUPPLIES

The AD4630-24/AD4632-24 do not have any specific power supply sequencing requirements. Take care to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The voltage range for the VDD_5V supply depends on the chosen reference voltage (see the internal reference buffer or externally overdriven reference specifications in Table 1). Figure 50 shows the minimum and maximum values for VDD_5V with respect to REFIN and REF for maximum performance.

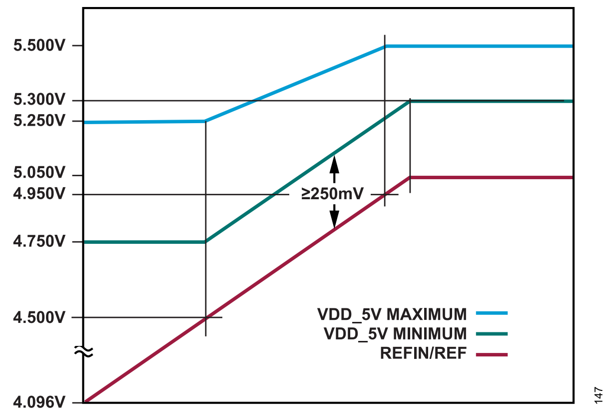


Figure 50. VDD_5V Minimum and Maximum Values for REFIN/REF

The AD4630-24/AD4632-24 have a POR circuit that resets the AD4630-24/AD4632-24 at initial power-up or whenever VDD_5V or VDD_1.8V drops below the specified operating range.

Note that the VDD_5V and the VDD_1.8V supplies have internal 1 µF bypass capacitors inside the package, whereas VIO has an internal 0.2 µF bypass capacitor. These internal capacitors reduce the BOM count and solution size. If the bulk supply bypass capacitors are not close to the ADC, external capacitors can be added next to the ADC. The minimum rise time for all supplies is 100 µs.

Power Consumption States

During a conversion, the power consumption rate of the AD4630-24/AD4632-24 is at its highest. When the conversion completes, the AD4630-24/AD4632-24 enter a standby state and much of the internal circuitry is powered down, and current consumption drops to less than 20% relative to the conversion state. To ensure full accuracy, some circuitry, including the reference buffer, remains powered on during the standby state.

The devices can be placed into a lower power shutdown state during periods when the convert clock is idle by writing 0x3 to the OPERATING_MODES bit field of the device configuration register (see the Device Configuration Register section). The default value of this bit field is 00 for normal operating mode. In the shutdown state, the current consumption typically drops to less than 10 µA.

Shutdown Mode

When the user enters shutdown mode, the internal reference buffer is disabled and a 500 Ω switch connects REFIN to REF (unless REFIN is grounded and REF is externally driven). This functionality keeps the 2 µF capacitor on REF charged up to allow fast recovery when the user leaves shutdown mode. Because of this keep alive switch, some charge is injected to REFIN when the user enters shutdown mode (400 pC) and leaves shutdown mode (5 pC). When leaving shutdown mode, REF is accurate after 30 µs.

SERIAL INTERFACE

The AD4630-24/AD4632-24 support a multilane SPI for each channel with a common bit clock (SCK). The flexible VIO supply allows the AD4630-24/AD4632-24 to communicate with any digital logic operating between 1.2 V and 1.8 V. However, for VIO levels below 1.4 V, Bit IO2X in the output driver register must be set to 1 (see the Output Driver Register section). The serial output data is clocked out on up to four SDO lanes per channel (see Figure 51). An echo clock mode that is synchronous with the output data is available to ease timing requirements when using isolation on the digital interface. A host clock mode is also available and uses an internal oscillator to clock out the data bits. The SPI Signals section describes the operation of the AD4630-24/AD4632-24 SPI.

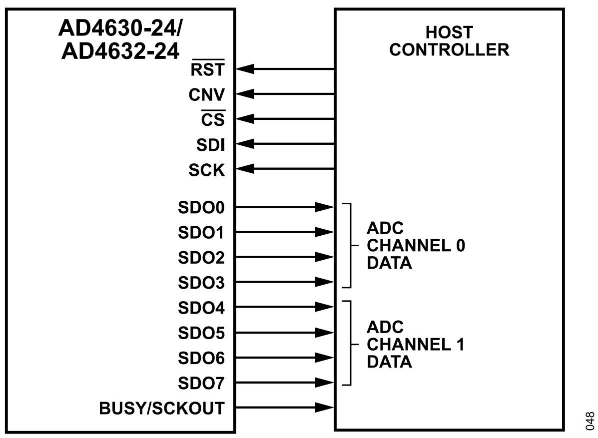


Figure 51. Multilane SPI

SPI SIGNALS

The SPI is a multilane interface that is used to both configure the ADC as well as retrieve sampled data. The SPI consists of the following signals:

- $\overline{CS}$ (input). Chip select. $\overline{CS}$ must be set low to initiate and enable a data transfer to or from the SDI pin or SDOx pins of the ADC. $\overline{CS}$ timing for reading sample data can be moderated by observing the state of the BUSY pin. For echo clock mode and host clock mode, $\overline{CS}$ timing must be controlled by the host processor because the BUSY pin is used as the bit clock output for these clocking modes.
- SDI (input). Serial data input stream from the host controller to ADC. SDI is only used when writing data into one of the user registers of the AD4630-24/AD4632-24.
- CNV (input). The CNV signal is sourced by the host controller and initiates a sample conversion. The frequency of the CNV signal determines the sampling rate of the AD4630-24/AD4632-24. The maximum frequency of the CNV clock is 2 MSPS.
- SCK (input). Serial data clock sourced by the host controller. The maximum supported SCK rate for output data transfer is 100 MHz. For register reads and writes, the maximum SCK rate is 86 MHz for VIO > 1.71 V, and 81 MHz for 1.14 V ≤ VIO < 1.71 V.
- SDO0 through SDO7 (outputs). Data lanes to the host controller. The SDO0 to SDO3 lanes are allocated to ADC Channel 0, whereas the SDO4 to SDO7 lanes are allocated to ADC Channel 1. The number of data lanes configured for each channel can be either 1, 2, or 4 lanes (see the output data modes in the Table 14 section). The number of data lanes is configured in the modes register. Note that the selected number of data lanes is applied to both ADC channels. The channels cannot be configured independently.
- BUSY/SCKOUT (output). The behavior of the BUSY/SCKOUT pin is dependent on selected clocking mode. Table 13 defines its behavior for each clocking mode.

Table 13. BUSY/SCKOUT Pin Behavior vs. Clocking Mode

Clocking Mode	Behavior
SPI	Valid BUSY signal for the ADC conversion status. BUSY goes high when a conversion is triggered by the CNV signal. BUSY goes low when the conversion completes.
Echo	Bit clock. BUSY/SCKOUT is a delayed version of SCK input.
Host	Bit clock. BUSY/SCKOUT sources the clock from the internal oscillator.

Register Access Mode

The AD4630-24/AD4632-24 offer programmable user registers to configure the device as outlined in the Registers section. By default, at power-up, the device is in conversion mode. Therefore, to access the user registers, a special access command must be sent by the host controller over the SPI, as shown in Figure 52. When this register access command is sent over the SPI, the device enters the register configuration mode. To read back the values from one of the user registers listed in the Registers section, the host controller must send the pattern shown in Figure 53. To write to one of the user registers, the host controller must send the pattern shown in Figure 54. In either case (read/write), the host controller must always issue 24 clock pulses on the SCK line and pull $\overline{CS}$ low for the entire transaction.

After writing to or reading from the appropriate user registers, the host controller must exit the register configuration mode by writing 0x01 to Register Address 0x0014 as detailed in the exit configuration mode register. An algorithm for register read/write access is as follows:

1. Perform a readback from dummy Register Address 0x3FFF to enter the register configuration mode.
2. Readback from or write to the desired user register addresses.
3. Exit the register configuration mode by writing 0x01 to Register Address 0x0014. Exiting register configuration mode causes the register updates to take effect.

SERIAL INTERFACE

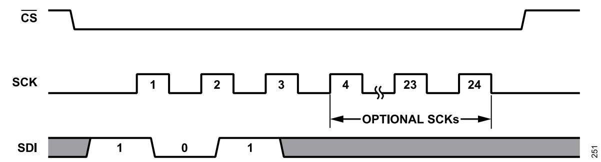


Figure 52. Register Configuration Mode Command

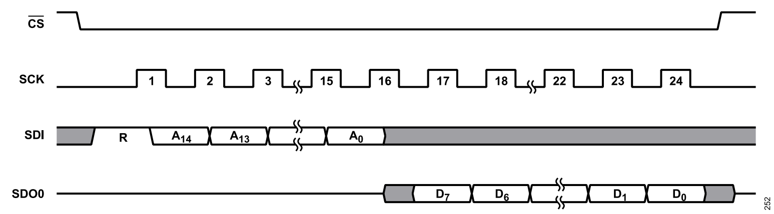


Figure 53. Register Configuration Mode Read

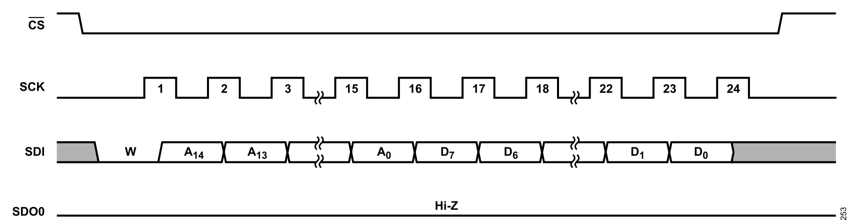


Figure 54. Register Configuration Mode Write

SERIAL INTERFACE

Stream Mode

The AD4630-24/AD4632-24 also offer a way to perform bulk register read/write transactions while the AD4630-24/AD4632-24 is in register configuration mode. To perform bulk read/write registers transactions, keep $\overline{CS}$ low and issue SCK pulses in multiples of 8 because each register is only one byte (8 bits) wide. In stream mode, only address decrementing is allowed, meaning that the user can read back from or write to the initial register address and register addresses that are directly below the initial register address. Apply register accesses in stream mode to register blocks with contiguous addresses. However, it is possible to address registers that are not present in the register map. To do so, write all zeros to these registers, or, when reading back, discard the contents read from these registers because it is random data. See the Registers section to see which register address is valid and continuous. For example, to read back a 24-bit offset value in one shot, the user must issue 24 SCK pulses staring from Register Address 0x0018. Figure 55 shows the timing diagram for a bulk read starting at a given address.

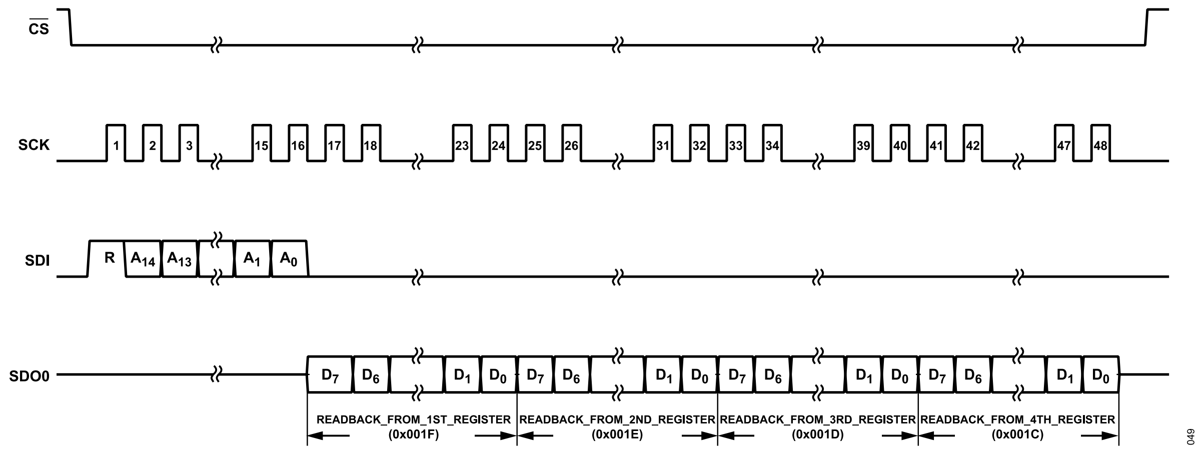


Figure 55. Stream Mode Bulk Register Read Back Operation

SERIAL INTERFACE

SAMPLE CONVERSION TIMING AND DATA TRANSFER

A conversion starts on the rising edge of the CNV signal, as shown in Figure 56. Once the conversion completes, $\overline{CS}$ can be asserted, which causes the current conversion result to load into the output shift register.

Referring to Figure 56, there are two optional data transfer zones for Sample N. Zone 1 represents the use case where $\overline{CS}$ is asserted immediately following the deassertion of the BUSY signal for the Sample N conversion (in SPI conversion mode), or after 300 ns for echo and host clock modes. For Zone 1, the available time to read out Sample N is given by:

Zone 1 Data Read Window = $t_{CYC} - t_{CONV} - t_{QUIET\_CNV\_ADV}$

For example, if f_{CNV} is 2 MSPS (t_{CYC} = 500 ns) and the typical value of t_{CONV} (282 ns) is used, the available window width is 198.4 ns (500 ns – 282 ns – 19.6 ns).

Zone 2 represents the case where an assertion of $\overline{CS}$ to read Sample N is delayed until after the conversion for Sample N + 1 initiates.

To prevent data corruption, a quiet zone must be observed before and after each rising edge of the CNV signal, as shown in Figure 56 and Figure 57. The quiet zone immediately before the rising edge of CNV is labeled as $t_{QUIET\_CNV\_ADV}$, and is equal to 19.6 ns. The quiet zone immediately after the rising edge of CNV is labeled $t_{QUIET\_CNV\_DELAY}$, and is equal to 9.8 ns. Assuming that the $\overline{CS}$ asserts immediately after the quiet zone around the rising edge of CNV, the amount of time available to clock out the data is:

Zone 2 Data Read Window = $t_{CYC} - t_{QUIET\_CNV\_DELAY} - t_{QUIET\_CNV\_ADV}$

For example, if f_{CNV} is 2 MSPS (t_{CYC} = 500 ns) and the typical value of t_{CONV} (282 ns) is used, the available window width is 470.6 ns (500 ns – 9.8 ns – 19.6 ns). The Zone 2 transfer window is longer than the Zone 1 window, which can enable the use of a slower SCK on the SPI and ease the timing requirements for the interface. When using Zone 2 for the data transfer, assert $\overline{CS}$ immediately after the quiet zone. $\overline{CS}$ must be asserted at least 25 ns before the falling edge of BUSY for Sample N + 1. If not, Sample N is overwritten with Sample N + 1.

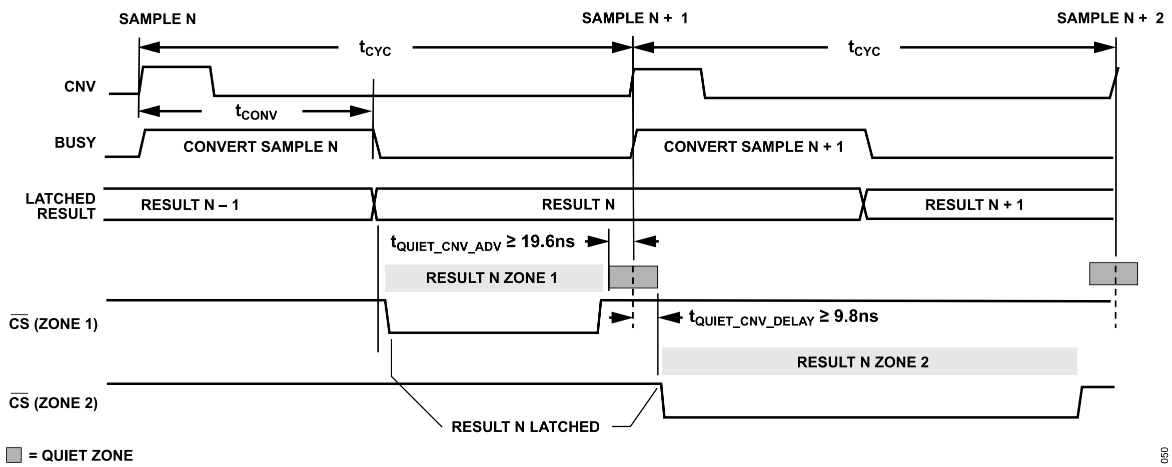


Figure 56. Example Timing for Data Transfer Zones

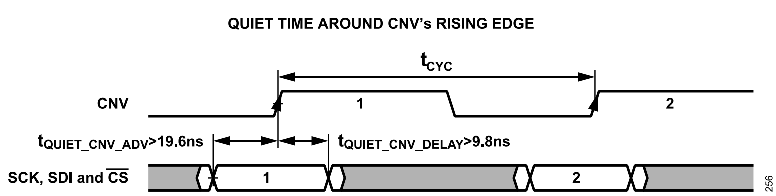


Figure 57. Quiet Zones

SERIAL INTERFACE

CLOCKING MODES

This section covers the various clocking modes supported by the AD4630-24/AD4632-24 SPI. These modes are available for 1-lane, 2-lane, 4-lane, and interleaved configurations. The clocking mode is configured in the modes register (see Table 16 for register descriptions). Note that the selected clocking mode applies to both ADC channels. The channels cannot be configured independently.

SPI Clocking Mode

SPI clocking mode is the default clocking mode of the AD4630-24/AD4632-24 and is equivalent to a host sourced bit clock (SCK), in which the host controller uses its own clock to latch the output data.

The SPI compatible clocking mode is enabled by writing 0x0 to the CLK_MD bit field of the modes register (see the Modes Register section). The interface connection is as shown in Figure 51. In this mode, the BUSY signal is valid and indicates the completion of a conversion (high to low transition of BUSY). A simplified sample cycle is shown in Figure 58. When not in averaging mode, if the host controller does not use the BUSY signal to detect the completion of a conversion, and instead uses an internal timer to retrieve the data, the host controller must wait at least 300 ns after the rising edge of the CNV pulse before asserting $\overline{CS}$ low. When operating in block averaging mode, the host controller must assert $\overline{CS}$ low no sooner than 300 ns after the rising edge of the CNV pulse for the last sample in the block.

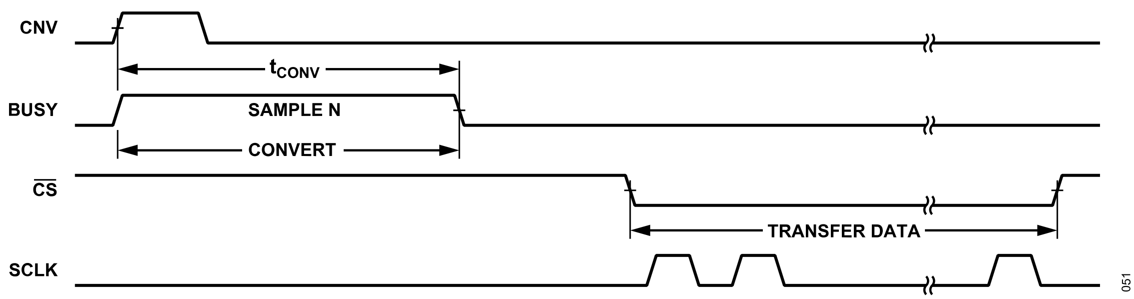


Figure 58. Typical Sample Cycle for SPI Clocking Mode

SERIAL INTERFACE

Echo Clock Mode

Figure 59 shows the signal connections for the echo clock mode. Echo clock mode is enabled by writing 0x1 to the CLK_MD bit field of the modes register (see the Modes Register section). In this mode, the BUSY/SCKOUT pin cannot be used to detect a conversion completion. The BUSY/SCKOUT pin becomes a bit clock output and is sourced by looping through the SCK of the host controller to the BUSY/SCKOUT pin (with some fixed delay, 5.4 ns to 7.9 ns, depending on VIO). To begin retrieving the conversion data in nonaveraging mode, the host controller must assert $\overline{CS}$ low no sooner than 300 ns after the rising edge of the CNV pulse. When the ADC is configured for block averaging mode, the host controller must assert $\overline{CS}$ low no sooner than 300 ns after the rising edge of the CNV pulse for the last sample in the block. Example timing diagrams are shown in the Data Clocking Requirements and Timing section. When echo clock mode is enabled, SCKOUT is aligned with SDOx transitions, making the data and clock timing insensitive to asymmetric propagation delays in the SDOx and SCK paths.

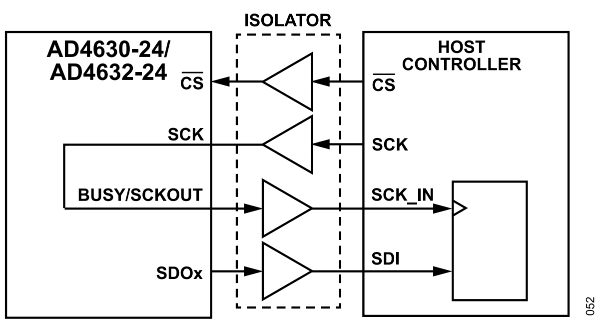


Figure 59. Echo Clock Mode Signal Path Diagram

Host Clock Mode

When enabled, host clock mode uses the internal oscillator as the bit clock source. The host clock mode is enabled by writing 0x2 to the CLK_MD bit field of the modes register. The bit clock frequency can be programmed in the OSC_DIV bit field in the internal oscillator register, with available divisor values of 1, 2, or 4 (see the Internal Oscillator Register section). Figure 60 shows the signal connections for the host clock mode. In this mode, the BUSY/SCKOUT pin provides the bit clock output and cannot be used to detect a conversion completion. The AD4630-24/AD4632-24 automatically calculate the number of clock pulses required to clock out the conversion data based on word size, number of active lanes, and choice of single data rate or DDR mode. The number of clock pulses can be read from the OSC_LIMIT bit field of the internal oscillator register. The SCK from the host must not be active. When retrieving the conversion data in nonaveraging mode, the host must not assert $\overline{CS}$ low sooner than 300 ns after the rising edge of the CNV pulse. When the ADC is configured in averaging mode for 2^N averages, the host must not assert $\overline{CS}$ low sooner than 300 ns after the rising edge of CNV pulse for the last sample in the block.

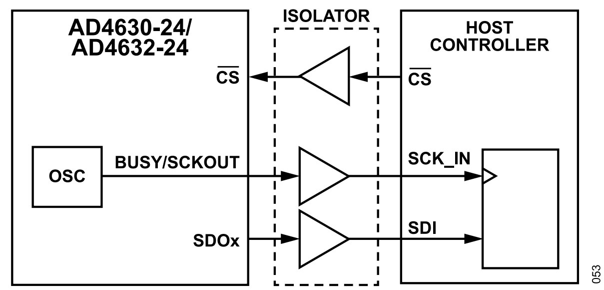


Figure 60. Host Clock Mode Signal Path Example

Single Data Rate

Single data rate (SDR) clocking in which one bit (per active lane) is clocked out during a single clock cycle, is supported for all output configurations and sample formats (see Table 14). The SDR clocking mode is enabled by default at power-up or can be enabled by writing 0 to the DDR_MD bit of the modes register (see the Modes Register section).

Dual Data Rate

DDR mode (two data bit transitions per clock cycle per active lane) is available only for host clock mode and echo clock mode.

Note that the selected data rate mode is applied to both ADC channels. DDR clocking mode is enabled by writing 1 to the DDR_MD bit of the modes register (see the Modes Register section). DDR mode uses half the number of SCK pulses to clock out conversion data in comparison to SDR mode.

1-Lane Output Data Clocking Mode

1-lane output data clocking mode is the default output data clocking mode at power-up. 1-lane output data clocking mode is enabled by writing 0x0 to the LANE_MD bit of the modes register (see the Modes Register section). The active lane for ADC Channel 0 is SDO0. The active lane for ADC Channel 1 is SDO4. Example timing diagrams for 1-lane output data clocking mode using SPI clocking mode, echo clock mode, and host clock mode are shown in the Data Clocking Requirements and Timing section.

2-Lane Output Data Clocking Mode

When 2-lane output data clocking mode is enabled, the sample word bits are split between two SDO lanes. Figure 66 shows how the bits are allocated between the lanes for 2-lane output data clocking mode. The bit arrangement is the same for SPI clocking mode, echo clock mode, and host clock mode. 2-lane output data clocking mode is enabled by writing 0x1 to the LANE_MD bit of the modes register (see the Modes Register section). The host controller must recombine the data coming from the SDO lanes to reconstruct the original sample word. The number of SCK pulses required to clock out the conversion data is reduced by one half with respect to 1-lane output data clocking mode. Table 14 lists the active SDO lanes for 2-lane output data clocking mode. Example

SERIAL INTERFACE

timing diagrams for 2-lane output data clocking mode using SPI clocking mode, echo clock mode, and host clock mode are shown in the Data Clocking Requirements and Timing section.

4-Lane Output Data Clocking Mode

When 4-lane output data clocking mode is enabled, the sample word bits are split between four SDO lanes. Figure 67 shows how the bits are allocated between the lanes for 4-lane mode. The bit arrangement is the same for SPI clocking mode, echo clock mode, and host clock mode. 4-lane output data clocking mode is enabled by writing 0x2 to the LANE_MD bit of the modes register (see the Modes Register section). The host controller must recombine the data coming from the SDO lanes to reconstruct the original sample word. The number of SCK pulses required to clock out the conversion data is reduced by one fourth with respect to 1-lane output data clocking mode. The active SDO lanes for 4-lane output data clocking mode are shown in Table 14. Example timing diagrams for 4-lane output data clocking mode using SPI clocking mode, echo clock mode, and host clock mode are shown in the Data Clocking Requirements and Timing section.

Interleaved Lane Output Data Clocking Mode

In interleaved lane output data clocking mode, the Channel 0 and Channel 1 conversion data is interleaved on SDO0. The bit arrangement is shown in Figure 68. The bit arrangement is the same for SPI clocking mode, echo clock mode, and host clock mode. Interleaved lane output data clocking mode is enabled by writing 0x3 to the LANE_MD bit of the modes register (see the Modes Register section). The host controller must demultiplex the data on SDO0 to reconstruct the original sample words. The number of SCK pulses required to clock out the conversion data is increased by 2× with respect to 1-lane output data clocking mode. The data transfer can occur in either Zone 1 or Zone 2 (see Figure 56). Using the interleaved lane output data clocking mode allows the host controller to use a single SDO lane to retrieve data from both ADC channels, reducing I/O requirements for the digital interface. Examples of interleaved lane mode timing are shown in the Data Clocking Requirements and Timing section.

Data Output Modes Summary

Table 14 is a summary of the supported data output modes of the AD4630-24/AD4632-24.

Table 14. Supported Data Output Modes

Number of Lanes (per Channel)	Active SDO Lanes		Clock Mode	Supported Data Clocking Mode	Output Sample Data-Word Length
	Channel 0	Channel 1			
1	SDO0	SDO4	SPI	SDR only	24 or 32
			Echo	SDR and DDR	24 or 32
			Host	SDR and DDR	24 or 32
2	SDO0, SDO1	SDO4, SDO5	SPI	SDR only	24 or 32
			Echo	SDR and DDR	24 or 32
			Host	SDR and DDR	24 or 32
4	SDO0, SDO1, SDO2, SDO3	SDO4, SDO5, SDO6, SDO7	SPI	SDR only	24 or 32
			Echo	SDR and DDR	24 or 32
			Host	SDR and DDR	24 or 32
Interleaved	SDO0		SPI	SDR only	48 or 64
			Echo	SDR and DDR	48 or 64
			Host	SDR and DDR	48 or 64

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DATA CLOCKING REQUIREMENTS AND TIMING

Basic and Averaging Conversion Cycles

Figure 61 shows the basic conversion cycle for a single sample. This cycle applies to SPI clocking mode. When echo clock mode and host clock modes are used, the BUSY function is disabled and the bit clock is sourced on the BUSY pin. The data transfer must meet the requirements described in the Sample Conversion Timing and Data Transfer section.

Table 15 contains the minimum and maximum values for the conversion timing parameters, which apply to all clocking modes.

Table 15. Conversion Cycle Timing Parameters

Parameter	Minimum (ns)	Maximum
t_{CNVH}	10	No specific maximum
t_{CNVL}	20	No specific maximum
t_{CNV}	264	300 ns

The duration of the data transfer period is dependent on the sample resolution, number of active lanes, SCK frequency, and data clocking mode (SDR or DDR). The nominal value of the transfer duration is given by:

$$Data\ \ Transfer\ \ Function = t_{TRANS} = \frac{N_{BITS}}{M_{LANES}} \times \frac{1}{f_{SCK}} \times \frac{1}{K}\ \ \text{seconds}$$

where:
t_{TRANS} is the transition time.
N_{BITS} = number of bits to clock out.
M_{LANES} = number of lanes used to clock out the data (1, 2, or 4).
f_{SCK} = SCK clock frequency in Hz.
K = 1 (SDR only, DDR not available for SPI clocking mode).

For a given f_{SCK}, number of data lanes, sample word size, and SDR or DDR mode, the minimum sample period when using Zone 1 for the data transfer is as follows:

Minimum Zone 1 Sample Period:

$$t_{CYC} \geq \left(\frac{N_{BITS}}{M_{LANES} \times f_{SCK} \times K}\right) + t_{CONV} + t_{QUIET\_CNV\_ADV}$$

The minimum sample period when using Zone 2 for data transfer is as follows:

$$t_{CYC} \geq \left(\frac{N_{BITS}}{M_{LANES} \times f_{SCK} \times K}\right) + t_{QUIET\_CNV\_DELAY} + t_{QUIET\_CNV\_ADV}$$

Figure 62 shows a typical conversion cycle when the averaging mode is active and SPI clocking mode is used. The BUSY signal is asserted for a number of CNV clock periods that is equal to the configured number of samples to be averaged. The averaged sample is then available when the BUSY signal is deasserted. Like nonaveraged mode, if the configured clocking mode is either echo clock or host clock, the BUSY signal is replaced by the output bit clock (SCKOUT). The host controller must manage the timing for asserting $\overline{CS}$.

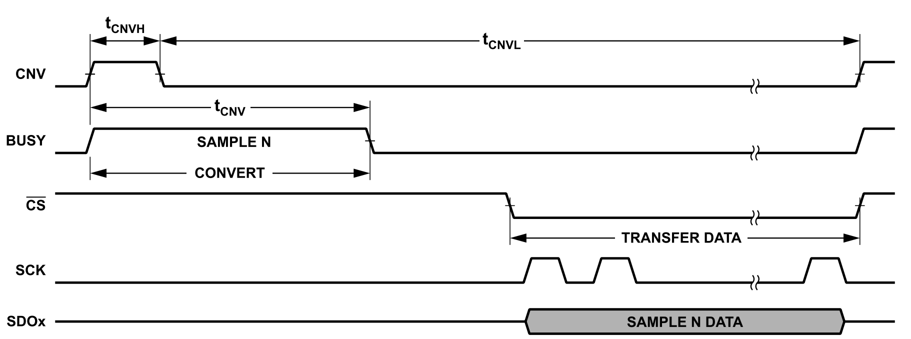

Figure 61. Basic Single Sample Conversion Cycle

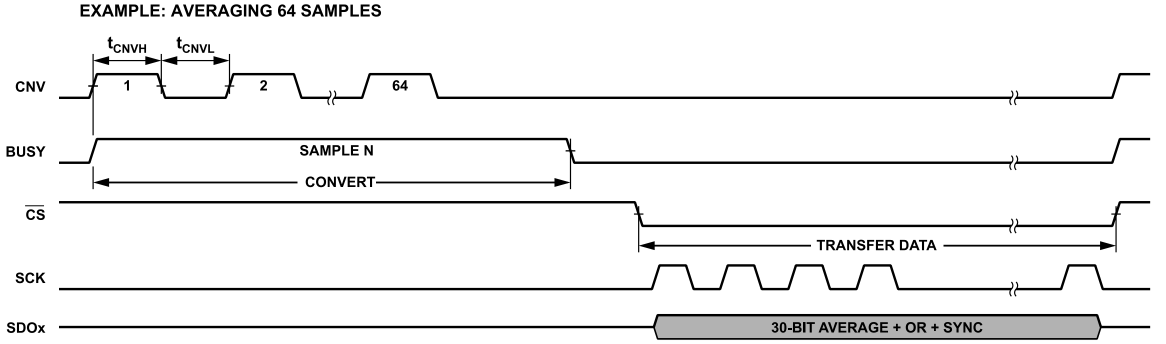

Figure 62. Example Conversion Cycle for Averaging Mode

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The two transfer zones that exist in nonaveraging mode also exist in averaging mode (see Figure 63, Figure 64, and Figure 65). To prevent data corruption, it is necessary to avoid SPI rising and falling edges signals taking place during quiet zones.

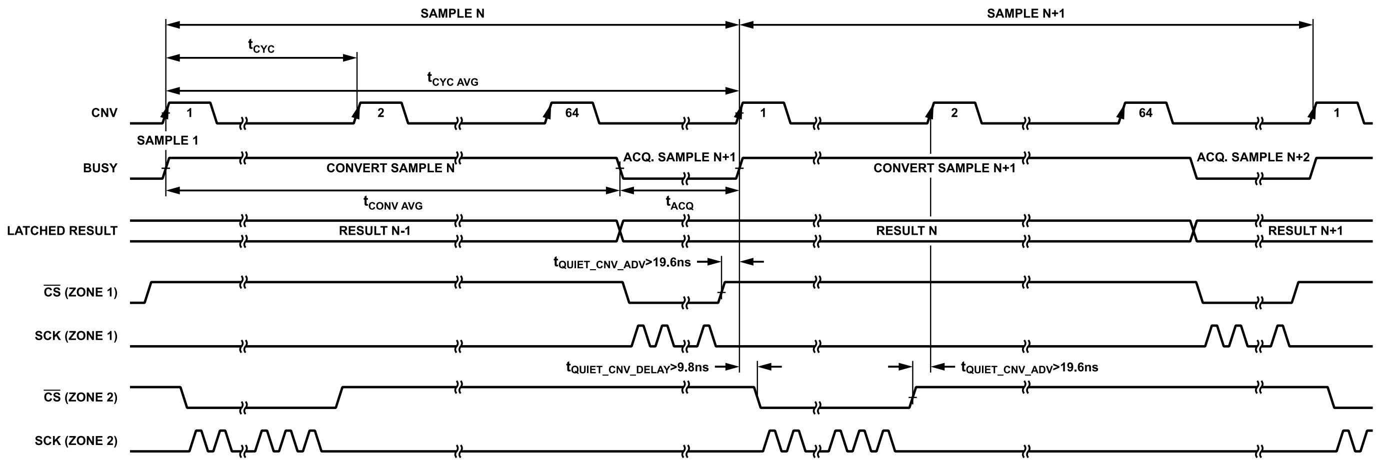

Figure 63. Example of Different Zones in Averaging Mode (64 Samples Averaged)

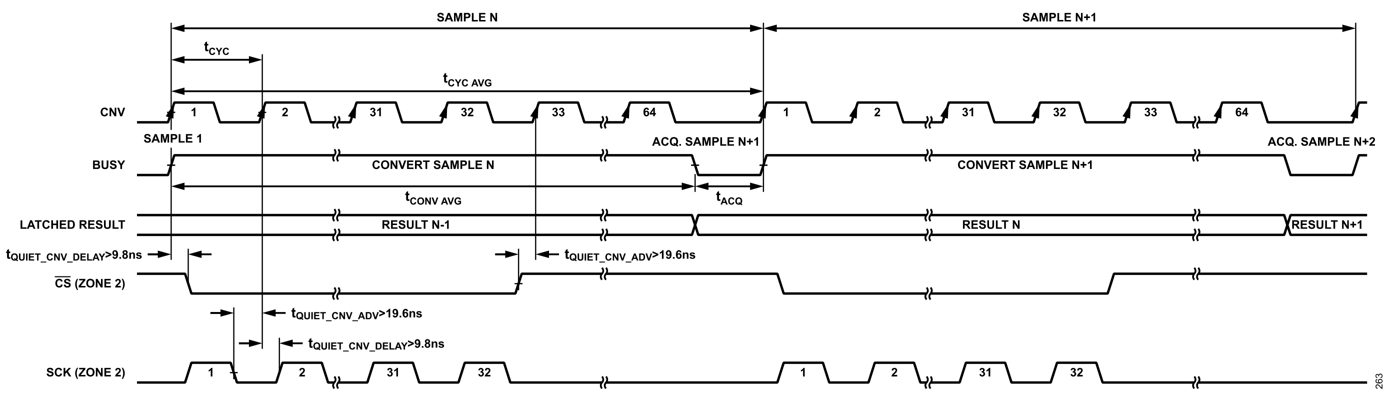

Figure 64. Example of Zone 2 in Averaging Mode (1 Bit per Sample)

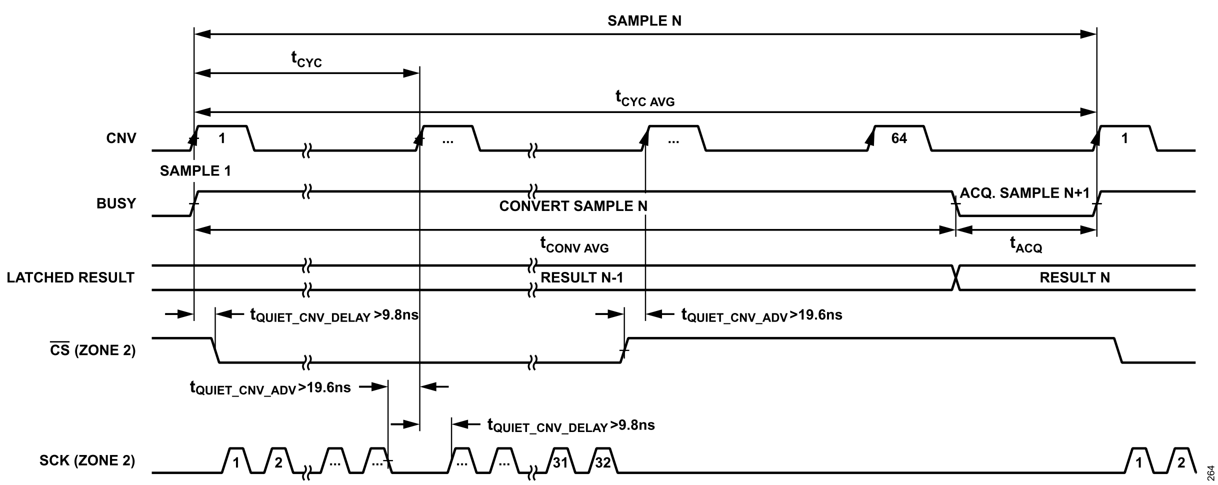

Figure 65. Example of Zone 2 in Averaging Mode (N Bits per Cycle)

SERIAL INTERFACE

SPI Clocking Mode Timing Diagrams

1-Lane, SDR Mode

Figure 6 shows a conversion cycle for 1-lane data output using SDR clocking mode (1-bit transitions per clock cycle). This cycle timing is the same for both ADC channels.

2-Lane, SDR Mode

Figure 66 shows a conversion cycle for 2-lane data output using SDR clocking mode. Figure 66 shows the timing for Channel 0, but this diagram also applies to Channel 1. See the 2-Lane Output Data Clocking Mode section for a detailed explanation.

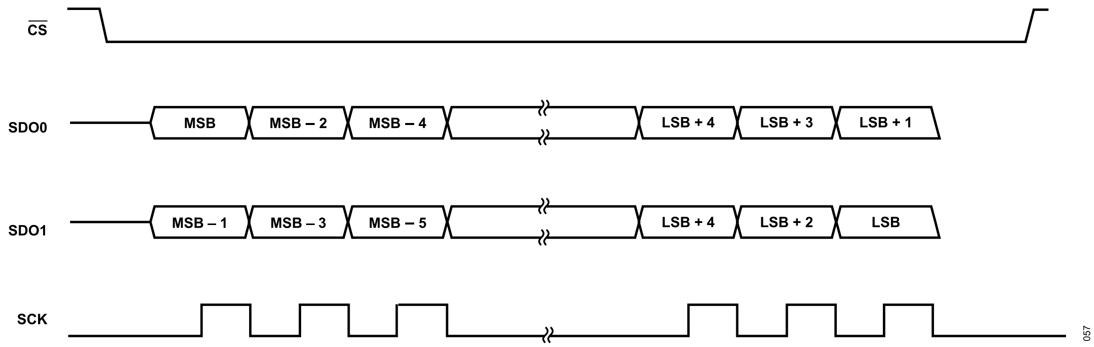

Figure 66. 2-Lane Mode, SDR Timing Diagram

SERIAL INTERFACE

4-Lane, SDR Mode

Figure 67 shows a conversion cycle for 4-lane data output using SDR clocking mode. Figure 67 shows the timing for Channel 0, but this diagram also applies for Channel 1. See the 4-Lane Output Data Clocking Mode section for a detailed explanation.

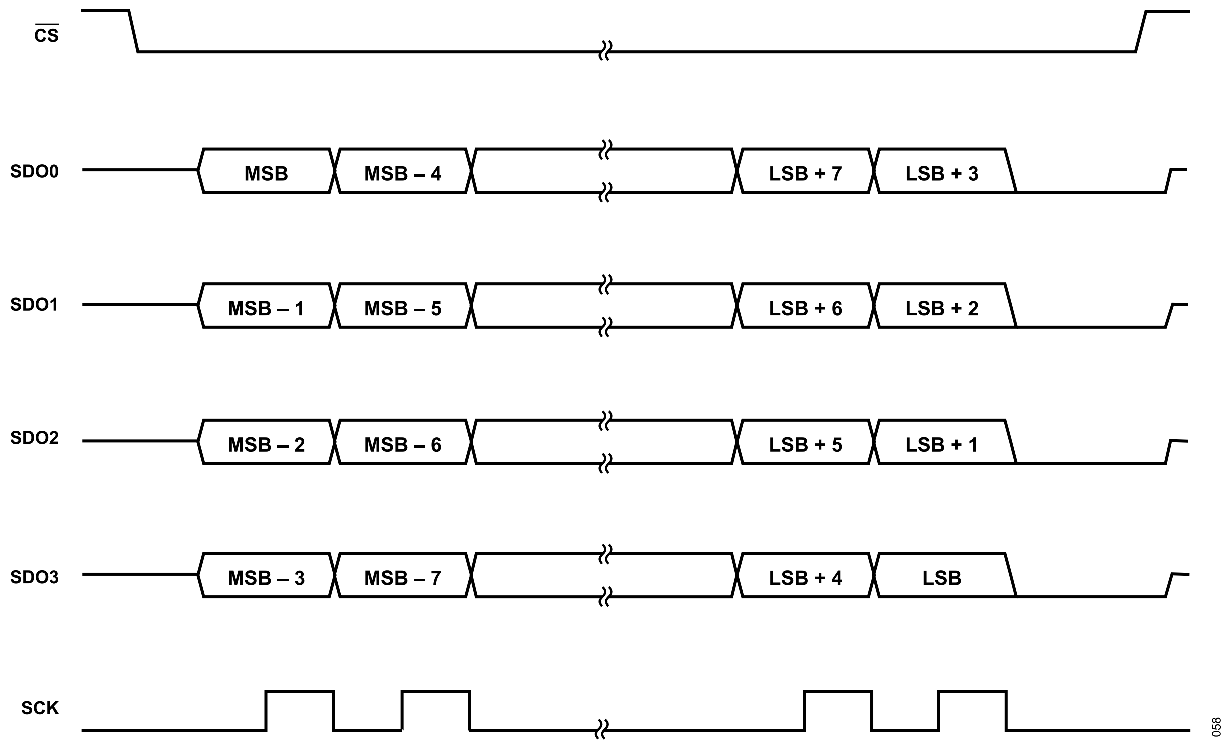

Figure 67. 4-Lane, SDR Timing Diagram

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Interleaved Mode Timing, SDR Mode

Figure 68 shows a conversion cycle for interleaved data output using SDR clocking mode. See the Interleaved-Lane Output Data Clocking Mode section for a detailed explanation.

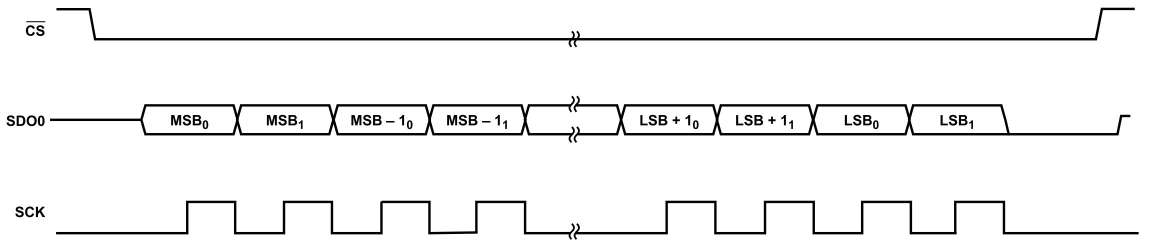

Figure 68. Interleaved Mode, SDR Timing Diagram

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Echo Clock Timing Diagrams

1-Lane, SDR Mode, Echo Clock Mode

Figure 7 shows the timing relationships for SDR mode (1-bit transitions per SCK period) in 1-lane echo clock mode. The timing relationships between the signals apply to both 24-bit and 32-bit sample word formats.

SCKOUT is a delayed version of the incoming SCK. The delay (t_{DSDO}) has a maximum value of 5.6 ns (at VIO > 1.71 V). Changes the in SDOx logic states are aligned to the rising edges of SCKOUT. The clock and data edge alignments are the same for 1-lane, 2-lane, and 4-lane output data modes.

1-Lane, DDR Mode, Echo Clock Mode

Figure 8 shows the timing relationships for DDR mode (2-bit transitions per SCKOUT period) in 1-lane echo clock mode. The timing relationships between the signals apply to both 24-bit and 32-bit sample word formats.

Similar to SDR mode, SCKOUT is a delayed version of the incoming SCK. Changes in the SDOx logic states are aligned to both the rising and falling edges of SCKOUT.

Host Clock Mode Timing

1-Lane, Host Clock Mode, SDR

Figure 9 shows the timing relationships for host clock mode when using SDR mode and 1-lane output data clocking mode. Similar to echo clock mode, the clock rising edges are aligned to the data bit transitions. The frequency of the SCKOUT signal is controlled by the OSC_DIV value programmed in the internal oscillator register (see the Internal Oscillator Register section).

1-Lane, Host Clock Mode, DDR

Figure 10 shows the timing relationships for host clock mode when using DDR mode. Similar to echo clock mode, the rising and falling clock edges are aligned to the data bit transitions. The frequency of the SCKOUT signal is controlled by the OSC_DIV value programmed in the internal oscillator register (see the Internal Oscillator Register section).

LAYOUT GUIDELINES

The following layout guidelines are recommended to achieve maximum performance out of the AD4630-24/AD4632-24:

- The AD4630-24/AD4632-24 contains internal 1 µF bypass capacitors for VDD_5V and VDD_1.8V, while VIO contains an internal 0.2 µF capacitor. Therefore, no external bypass capacitors are required, saving board space and reducing BOM count and layout sensitivity.
- Have all the analog signals flow in from the left side of the AD4630-24/AD4632-24 and all the digital signals to flow in and out from the right side of AD4630-24/AD4632-24 because this helps isolate analog signals from digital signals.
- Use a solid ground plane under the AD4630-24/AD4632-24 and connect all the analog ground (GND) pins and digital ground (IOGND) pins to the shared ground plane to avoid the formation of ground loops.
- Traces routed to either the REFIN pin or REF pins must be isolated/shielded from other signals. Avoid routing signals beneath the reference trace (REFIN or REF). The REF pins are connected to an internal 2 µF capacitor, eliminating the need to place a decoupling capacitor on the output of the external reference buffer. If a noise reduction filter is placed between the output of the reference (or buffer) and the chosen reference input, the filter must be placed as close as possible to the AD4630-24/AD4632-24.

REGISTERS

The AD4630-24/AD4632-24 has programmable user registers that are used to configure the device. These registers can be accessed while the AD4630-24/AD4632-24 are in register configuration mode. Table 16 details the AD4630-24/AD4632-24 user registers and the bit fields in the registers. The Register Details section details the functions of each of the bit fields. The access mode specifies whether the register is comprised only of read-only bits (R) or a mix of read-only and read/write bits (R/W). Read-only bits cannot be overwritten by a SPI write transaction, whereas read/write bits can be overwritten.

Table 16. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			SW_RESETX	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	STALLING	RESERVED		SHORT_INSTRUCTION	RESERVED			0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED						OPERATING_MODES		0x00	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED [7:4]				CHIP_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x20	R
0x06	CHIP_GRADE	[7:0]	GRADE					DEVICE_REVISION			0x01	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x81	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x10	INTERFACE_CONFIG_C	[7:0]	RESERVED								0x00	R/W
0x11	INTERFACE_STATUS_A	[7:0]	RESERVED			CLOCK_COUNT_ERR	RESERVED				0x00	R/W
0x14	EXIT_CFG_MD	[7:0]	RESERVED							EXIT_CONFIG_MD	0x00	R/W
0x15	AVG	[7:0]	AVG_SYNC	RESERVED		AVG_VAL					0x00	R/W
0x16	OFFSET_CH0_LB	[7:0]	CH0_USER_OFFSET[7:0]								0x00	R/W
0x17	OFFSET_CH0_MB	[7:0]	CH0_USER_OFFSET[15:8]								0x00	R/W
0x18	OFFSET_CH0_HB	[7:0]	CH0_USER_OFFSET[23:16]								0x00	R/W
0x19	OFFSET_CH1_LB	[7:0]	CH1_USER_OFFSET[7:0]								0x00	R/W
0x1A	OFFSET_CH1_MB	[7:0]	CH1_USER_OFFSET[15:8]								0x00	R/W
0x1B	OFFSET_CH1_HB	[7:0]	CH1_USER_OFFSET[23:16]								0x00	R/W
0x1C	GAIN_CH0_LB	[7:0]	CH0_USER_GAIN[7:0]								0x00	R/W
0x1D	GAIN_CH0_HB	[7:0]	CH0_USER_GAIN[15:8]								0x80	R/W
0x1E	GAIN_CH1_LB	[7:0]	CH1_USER_GAIN[7:0]								0x00	R/W
0x1F	GAIN_CH1_HB	[7:0]	CH1_USER_GAIN[15:8]								0x80	R/W
0x20	MODES	[7:0]	LANE_MD		CLK_MD		DDR_MD	OUT_DATA_MD			0x00	R/W
0x21	OSCILLATOR	[7:0]	OSC_LIMIT				OSC_DIV				0x00	R/W
0x22	IO	[7:0]	RESERVED							IO2X	0x00	R/W
0x23	TEST_PAT_BYTE0	[7:0]	TEST_DATA_PAT[7:0]								0x0F	R/W
0x24	TEST_PAT_BYTE1	[7:0]	TEST_DATA_PAT[15:8]								0x0F	R/W
0x25	TEST_PAT_BYTE2	[7:0]	TEST_DATA_PAT[23:16]								0x5A	R/W
0x26	TEST_PAT_BYTE3	[7:0]	TEST_DATA_PAT[31:24]								0x5A	R/W
0x34	DIG_DIAG	[7:0]	POWERUP COMPLETED	RESET_OCCURRED	RESERVED					FUSE_CRC_EN	0x40	R/W
0x35	DIG_ERR	[7:0]	RESERVED							FUSE_CRC_ERR	0x00	R/W

REGISTER DETAILS

INTERFACE CONFIGURATION A REGISTER

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

Interface configuration settings.

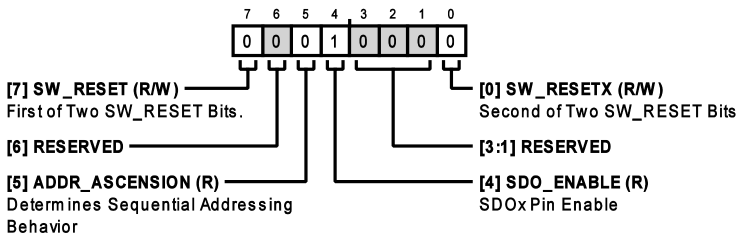


Table 17. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET	First of Two SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the device. All registers except for this register are reset to their default values.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_ASCENSION	Determines sequential addressing behavior. 0: address accessed is decremented by one for each data byte when streaming. 1: not a valid option.	0x0	R
4	SDO_ENABLE	SDOx Pin Enable.	0x1	R
[3:1]	RESERVED	Reserved.	0x0	R
0	SW_RESETX	Second of Two SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the device. All registers except for this register are reset to their default values.	0x0	R/W

INTERFACE CONFIGURATION B REGISTER

Address: 0x01, Reset: 0x00, Name: INTERFACE_CONFIG_B

Additional interface configuration settings.

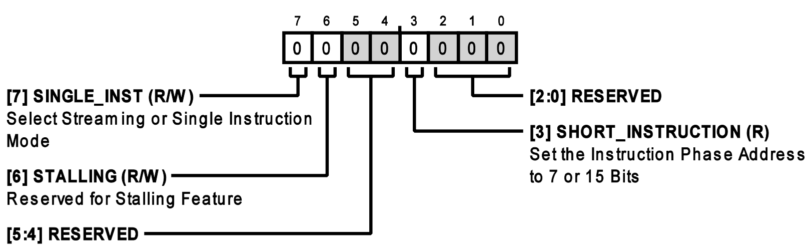


Table 18. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Select streaming or single instruction mode. 0: streaming mode is enabled. The address decrements as successive data bytes are received. 1: single instruction mode is enabled.	0x0	R/W
6	STALLING	Reserved for Stalling Feature.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R
3	SHORT_INSTRUCTION	Set the instruction phase address to 7 or 15 bits. 0: 15-bit addressing. 1: 7-bit addressing.	0x0	R

REGISTER DETAILS

Table 18. Bit Descriptions for INTERFACE_CONFIG_B (Continued)

Bits	Bit Name	Description	Reset	Access
[2:0]	RESERVED	Reserved.	0x0	R

DEVICE CONFIGURATION REGISTER

Address: 0x02, Reset: 0x00, Name: DEVICE_CONFIG

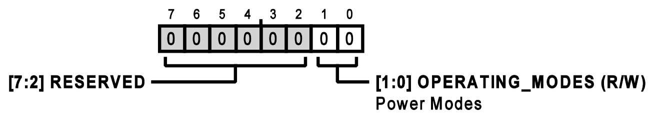


Table 19. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	OPERATING_MODES	Power Modes. 00: normal operating mode. 11: shutdown mode.	0x0	R/W

CHIP TYPE REGISTER

Address: 0x03, Reset: 0x07, Name: CHIP_TYPE

The chip type is used to identify the family of Analog Devices products a given device belongs to. Use the chip type with the product ID to uniquely identify a given product.

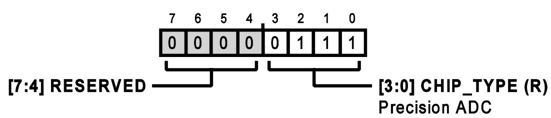


Table 20. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision ADC.	0x7	R

PRODUCT ID LOW REGISTER

Address: 0x04, Reset: 0x00, Name: PRODUCT_ID_L

Low byte of the product ID.

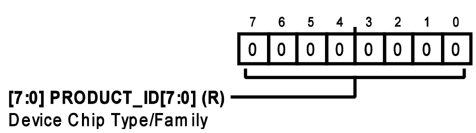


Table 21. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID, Bits[7:0]	Device Chip Type/Family. Use the product ID with the chip type to identify a product.	0x0	R

REGISTER DETAILS

PRODUCT ID HIGH REGISTER

Address: 0x05, Reset: 0x20, Name: PRODUCT_ID_H

High byte of the product ID.

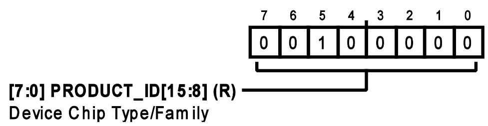


Table 22. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID, Bits[15:8]	Device Chip Type/Family. Use the product ID with the chip type to identify a product.	0x20	R

CHIP GRADE REGISTER

Address: 0x06, Reset: 0x01, Name: CHIP_GRADE

Identifies product variations and device revisions.

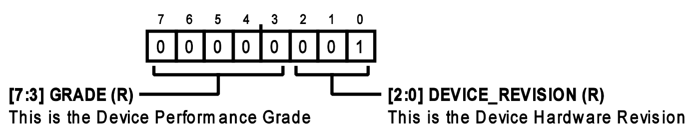


Table 23. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:3]	GRADE	This is the device performance grade. AD4630-24: 0b00000 AD4632-24: 0b00010	 0x0 0x2	R
[2:0]	DEVICE_REVISION	This is the device hardware revision.	0x1	R

SCRATCHPAD REGISTER

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

This register can be used to test writes and reads.

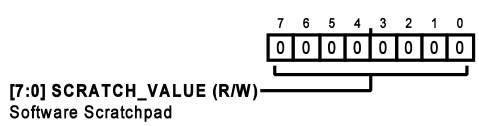


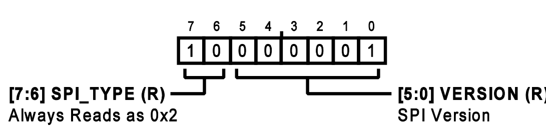
Table 24. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

SPI REVISION REGISTER

Address: 0x0B, Reset: 0x81, Name: SPI_REVISION

Indicates the SPI revision.



REGISTER DETAILS

Table 25. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	Always reads as 0x2.	0x2	R
[5:0]	VERSION	SPI Version. 01: draft	0x1	R

VENDOR ID LOW REGISTER

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

Low byte of the vendor ID.

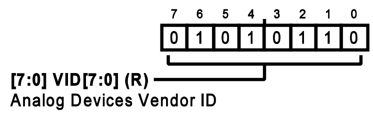


Table 26. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Analog Devices Vendor ID.	0x56	R

VENDOR ID HIGH REGISTER

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

High byte of the vendor ID.

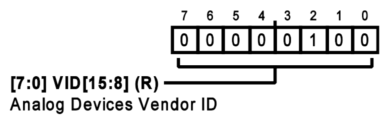


Table 27. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Analog Devices Vendor ID.	0x4	R

STREAM MODE REGISTER

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

Defines the length of the loop when streaming data.

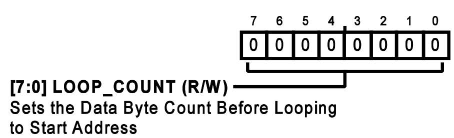


Table 28. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Sets the data byte count before looping to start address. When streaming data, a nonzero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes can be written using this approach. A value of 0x00 disables the loop back so that addressing wraps around at the upper and lower limits of the memory. After writing this register, the loop value applies only to the following SPI instruction and auto clears upon the end of that instruction.	0x0	R/W

REGISTER DETAILS

INTERFACE CONFIGURATION C REGISTER

Address: 0x10, Reset: 0x00, Name: INTERFACE_CONFIG_C

Additional interface configuration settings.

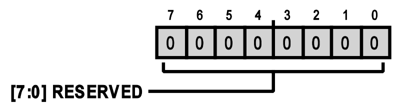


Table 29. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

INTERFACE STATUS A REGISTER

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

Status bits are set to 1 to indicate an active condition. The status bits can be cleared by writing a 1 to the corresponding bit location.

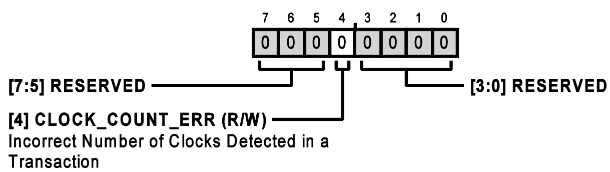


Table 30. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	CLOCK_COUNT_ERR	Incorrect Number of Clocks Detected in a Transaction.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R

EXIT CONFIGURATION MODE REGISTER

Address: 0x14, Reset: 0x00, Name: EXIT_CFG_MD

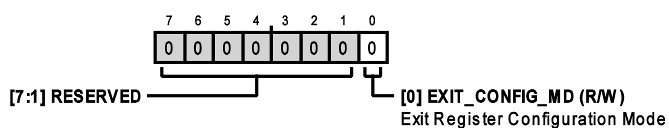


Table 31. Bit Descriptions for EXIT_CFG_MD

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	EXIT_CONFIG_MD	Exit Register Configuration Mode. Write 1 to exit register configuration mode. Self clearing upon $\overline{CS}$ = 1.	0x0	R/W

REGISTER DETAILS

AVERAGING MODE REGISTER

Address: 0x15, Reset: 0x00, Name: AVG

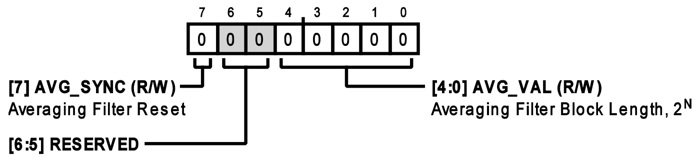


Table 32. Bit Descriptions for AVG

Bits	Bit Name	Description	Reset	Access
7	AVG_SYNC	Averaging Filter Reset. 1 = reset, self clearing.	0x0	R/W
[6:5]	RESERVED	Reserved.	0x0	R
[4:0]	AVG_VAL	Averaging Filter Block Length, 2^N. 0x00 = no averaging. 0x01 = 2^1 samples. 0x02 = 2^2 samples. 0x03 = 2^3 samples. 0x04 = 2^4 samples. 0x05 = 2^5 samples. … 0x0F = 2^{15} samples. 0x10 = 2^{16} samples. 0x11 through 0x1F = invalid.	0x0	R/W

CHANNEL 0 OFFSET REGISTERS

Address: 0x16, Reset: 0x00, Name: OFFSET_CH0_LB

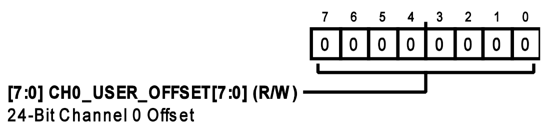


Table 33. Bit Descriptions for OFFSET_CH0_LB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH0_USER_OFFSET[7:0]	24-Bit Channel 0 Offset. Twos complement (signed). 1 LSB = ($V_{REF}/2^{23}$)/Gain. See the Channel 0 Gain Registers section for a description of the gain parameter.	0x0	R/W

Address: 0x17, Reset: 0x00, Name: OFFSET_CH0_MB

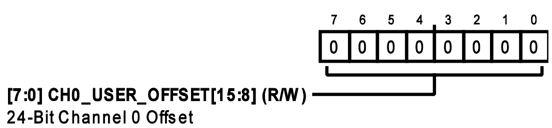


Table 34. Bit Descriptions for OFFSET_CH0_MB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH0_USER_OFFSET[15:8]	24-Bit Channel 0 Offset. Twos complement (signed). 1 LSB = ($V_{REF}/2^{23}$)/Gain. See the Channel 0 Gain Registers section for a description of the gain parameter.	0x0	R/W

REGISTER DETAILS

Address: 0x18, Reset: 0x00, Name: OFFSET_CH0_HB

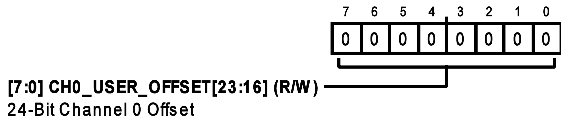


Table 35. Bit Descriptions for OFFSET_CH0_HB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH0_USER_OFFSET[23:16]	24-Bit Channel 0 Offset. Twos complement (signed). 1 LSB = ($V_{REF}/2^{23}$)/Gain. See the Channel 0 Gain Registers section for a description of the gain parameter.	0x0	R/W

CHANNEL 1 OFFSET REGISTERS

Address: 0x19, Reset: 0x00, Name: OFFSET_CH1_LB

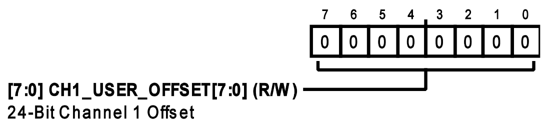


Table 36. Bit Descriptions for OFFSET_CH1_LB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_USER_OFFSET[7:0]	24-Bit Channel 1 Offset. Twos complement (signed). 1 LSB = ($V_{REF}/2^{23}$)/Gain. See the Channel 1 Gain Registers section for a description of the gain parameter value.	0x0	R/W

Address: 0x1A, Reset: 0x00, Name: OFFSET_CH1_MB

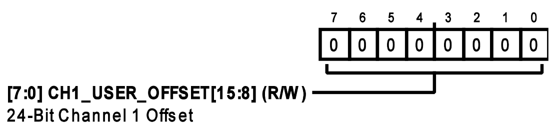


Table 37. Bit Descriptions for OFFSET_CH1_MB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_USER_OFFSET[15:8]	24-Bit Channel 1 Offset. Twos complement (signed). 1 LSB = ($V_{REF}/2^{23}$)/Gain. See the Channel 1 Gain Registers section for a description of the gain parameter value.	0x0	R/W

Address: 0x1B, Reset: 0x00, Name: OFFSET_CH1_HB

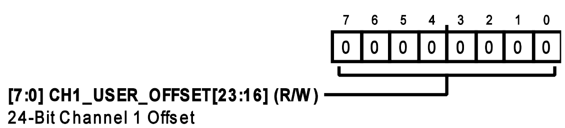


Table 38. Bit Descriptions for OFFSET_CH1_HB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_USER_OFFSET[23:16]	24-Bit Channel 1 Offset. Twos complement (signed). 1 LSB = ($V_{REF}/2^{23}$)/Gain. See the Channel 1 Gain Registers section for a description of the gain parameter value.	0x0	R/W

REGISTER DETAILS

CHANNEL 0 GAIN REGISTERS

Address: 0x1C, Reset: 0x00, Name: GAIN_CH0_LB

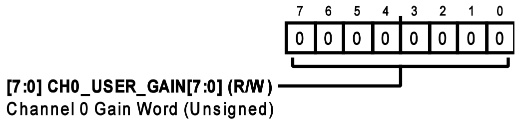


Table 39. Bit Descriptions for GAIN_CH0_LB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH0_USER_GAIN[7:0]	Channel 0 Gain Word (Unsigned). Multiplier output = input × gain word/0x8000. Maximum effective gain = 0xFFFF/0x8000 = 1.99997.	0x00	R/W

Address: 0x1D, Reset: 0x80, Name: GAIN_CH0_HB

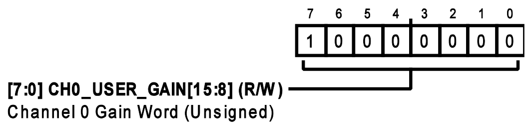


Table 40. Bit Descriptions for GAIN_CH0_HB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH0_USER_GAIN[15:8]	Channel 0 Gain Word (Unsigned). Multiplier output = input × gain word/0x8000. Maximum effective gain = 0xFFFF/0x8000 = 1.99997.	0x80	R/W

CHANNEL 1 GAIN REGISTERS

Address: 0x1E, Reset: 0x00, Name: GAIN_CH1_LB

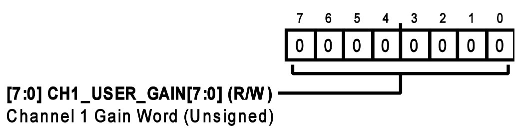


Table 41. Bit Descriptions for GAIN_CH1_LB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_USER_GAIN[7:0]	Channel 1 Gain Word (Unsigned). Multiplier output = input × gain word/0x8000. Maximum effective gain = 0xFFFF/0x8000 = 1.99997.	0x00	R/W

Address: 0x1F, Reset: 0x80, Name: GAIN_CH1_HB

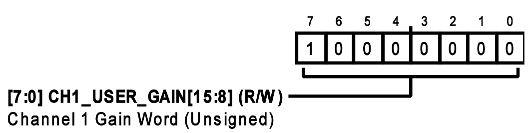


Table 42. Bit Descriptions for GAIN_CH1_HB

Bits	Bit Name	Description	Reset	Access
[7:0]	CH1_USER_GAIN[15:8]	Channel 1 Gain Word (Unsigned). Multiplier output = input × gain word/0x8000. Maximum effective gain = 0xFFFF/0x8000 = 1.99997.	0x80	R/W

REGISTER DETAILS

MODES REGISTER

Address: 0x20, Reset: 0x00, Name: MODES

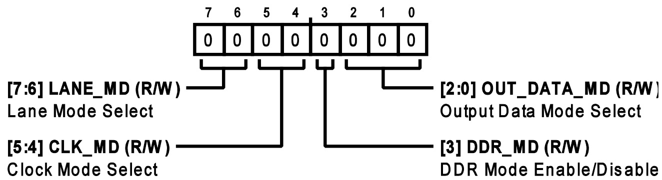


Table 43. Bit Descriptions for MODES

Bits	Bit Name	Description	Reset	Access
[7:6]	LANE_MD	Lane Mode Select. 00 = one lane per channel. 01 = two lanes per channel. 10 = four lanes per channel. 11 = Channel 0 and Channel 1 interleaved on SDO0.	0x0	R/W
[5:4]	CLK_MD	Clock Mode Select. 00 = SPI clocking mode. 01 = echo clock mode. 10 = host clock mode. 11 = invalid setting.	0x0	R/W
3	DDR_MD	DDR Mode Enable/Disable. 0 = SDR. 1 = DDR (only valid for echo clock and host clock modes).	0x0	R/W
[2:0]	OUT_DATA_MD	Output Data Mode Select. 000 = 24-bit differential data. 001 = 16-bit differential data + 8-bit common mode data. 010 = 24-bit differential data + 8-bit common mode data. 011 = 30-bit averaged differential data + OR bit + SYNC bit. 100 = 32-bit test data pattern (see the Test Pattern Registers section).	0x0	R/W

INTERNAL OSCILLATOR REGISTER

Address: 0x21, Reset: 0x00, Name: OSCILLATOR

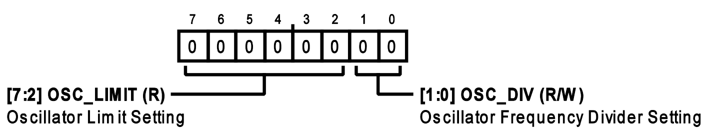


Table 44. Bit Descriptions for OSCILLATOR

Bits	Bit Name	Description	Reset	Access
[7:2]	OSC_LIMIT	Oscillator Limit Setting. Oscillator is limited to this number of clock pulses plus one. Automatically calculated by the AD4630-24/AD4632-24 based on the data-word size, number of active SDO lanes, and data rate mode (SDR or DDR).	0x0	R
[1:0]	OSC_DIV	Oscillator Frequency Divider Setting. 00 = no divide (divide by 1). 01 = divide by 2. 10 = divide by 4. 11 = invalid setting.	0x0	R/W

REGISTER DETAILS

OUTPUT DRIVER REGISTER

Address: 0x22, Reset: 0x00, Name: IO

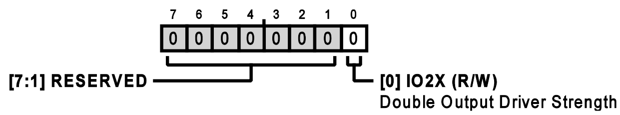


Table 45. Bit Descriptions for IO

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	IO2X	Double Output Driver Strength. 1 = double output driver strength. 0 = normal output driver strength.	0x0	R/W

TEST PATTERN REGISTERS

Address: 0x23, Reset: 0x0F, Name: TEST_PAT_BYTE0

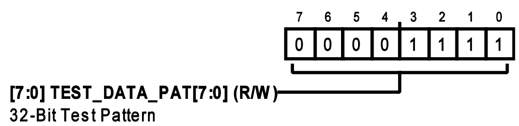


Table 46. Bit Descriptions for TEST_PAT_BYTE0

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[7:0]	32-Bit Test Pattern. Applied to both channels when OUT_DATA_MD = 4 (see the Modes Register section).	0xF	R/W

Address: 0x24, Reset: 0x0F, Name: TEST_PAT_BYTE1

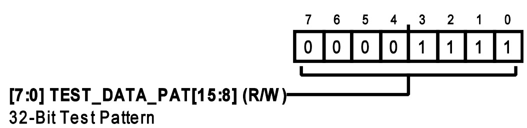


Table 47. Bit Descriptions for TEST_PAT_BYTE1

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[15:8]	32-Bit Test Pattern. Applied to both channels when OUT_DATA_MD = 4 (see the Modes Register section).	0xF	R/W

Address: 0x25, Reset: 0x5A, Name: TEST_PAT_BYTE2

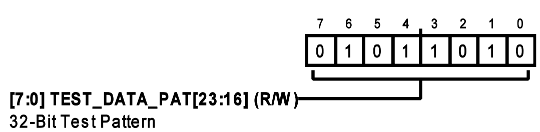


Table 48. Bit Descriptions for TEST_PATBYTE2

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[23:16]	32-Bit Test Pattern. Applied to both channels when OUT_DATA_MD = 4 (see the Modes Register section).	0x5A	R/W

REGISTER DETAILS

Address: 0x26, Reset: 0x5A, Name: TEST_PAT_BYTE3

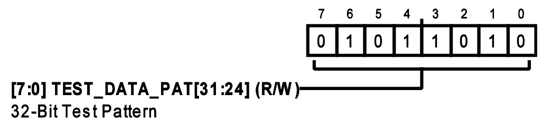


Table 49. Bit Descriptions for TEST_PAT_BYTE3

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[31:24]	32-Bit Test Pattern. Applied to both channels when OUT_DATA_MD = 4 (see the Modes Register section).	0x5A	R/W

DIGITAL DIAGNOSTICS REGISTER

Address: 0x34, Reset: 0x40, Name: DIG_DIAG

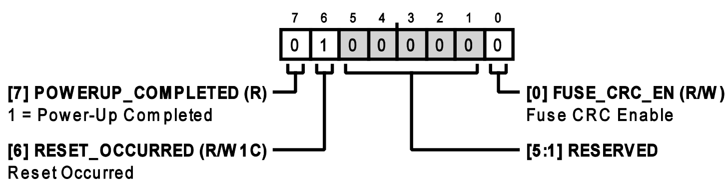


Table 50. Bit Descriptions for DIG_DIAG

Bits	Bit Name	Description	Reset	Access
7	POWERUP_COMPLETED	1 = Power-Up Completed.	0x0	R
6	RESET_OCCURRED	Reset Occurred. This bit is set to 1 upon a reset event. Write 1 to clear (useful for detecting brownouts).	0x1	R/W1C
[5:1]	RESERVED	Reserved.	0x0	R
0	FUSE_CRC_EN	Fuse CRC Enable. Write a 1 to force recheck of CRC.	0x0	R/W

DIGITAL ERRORS REGISTER

Address: 0x35, Reset: 0x00, Name: DIG_ERR

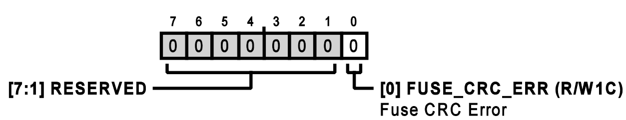
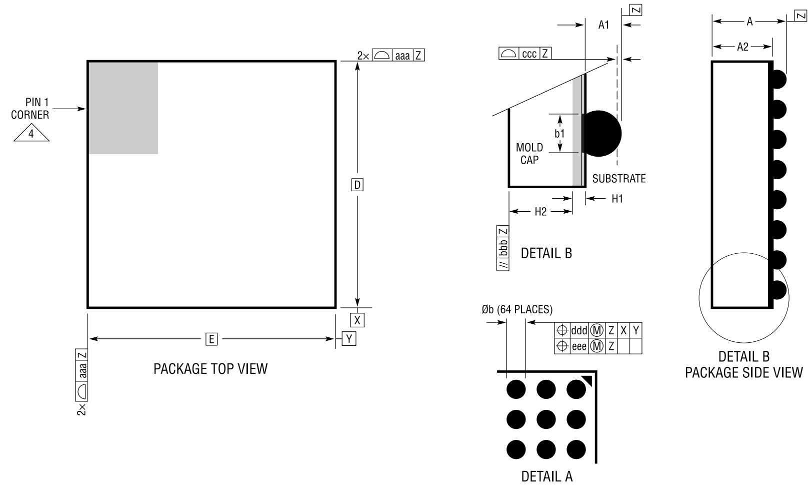
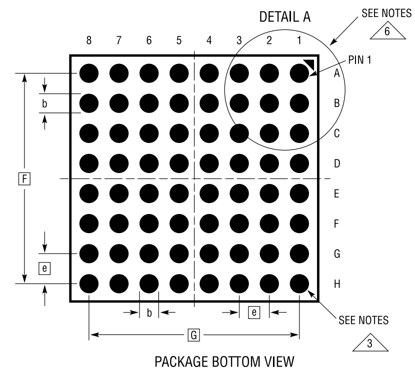


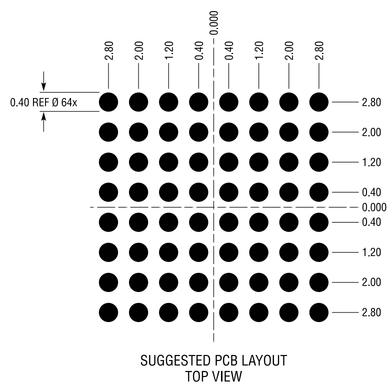
Table 51. Bit Descriptions for DIG_ERR

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FUSE_CRC_ERR	Fuse CRC Error. This bit is set to 1 upon a fuse CRC error. Write 1 to clear.	0x0	R/W1C

OUTLINE DIMENSIONS







SYMBOL	MIN	NOM	MAX	NOTES
	DIMENSIONS			
A	1.52	1.72	1.92	
A1	0.30	0.40	0.50	BALL HT
A2	1.22	1.32	1.42	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.00		
E		7.00		
e		0.80		
F		5.60		
G		5.60		
H1		0.32	REF	SUBSTRATE THK
H2		1.00	REF	MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 64				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG μModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

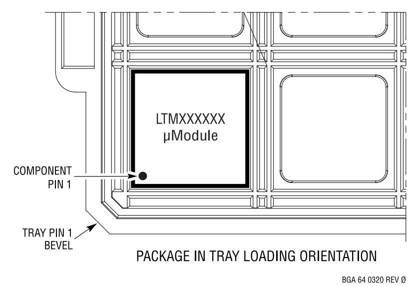


Figure 69. 64-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(05-08-1797)
Dimensions shown in millimeters

Updated: May 11, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4630-24BBCZ	-40°C to +125°C	64-Lead BGA (7 mm x 7 mm x 1.72 mm)		05-08-1797
AD4630-24BBCZ-RL	-40°C to +125°C	64-Lead BGA (7 mm x 7 mm x 1.72 mm)	Reel, 2000	05-08-1797
AD4632-24BBCZ	-40°C to +125°C	64-Lead BGA (7 mm x 7 mm x 1.72 mm)		05-08-1797
AD4632-24BBCZ-RL	-40°C to +125°C	64-Lead BGA (7 mm x 7 mm x 1.72 mm)	Reel, 2000	05-08-1797

1 Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1, 2]	Description
EVAL-AD4630-24-KTZ	Evaluation Kit
EVAL-AD4630-24FMCZ	Evaluation Board

1 Z = RoHS Compliant Part.

2 The EVAL-AD4630-24-KTZ and EVAL-AD4630-24FMCZ can be used to evaluate the AD4632-24.