

## Single Channel, 12-/16-Bit, 16 MUPS, Multispan, Multi-IO SPI DAC

### **FEATURES**

- 12-/16-bit resolution
- 16 MUPS single channel rate in fast mode
- 11 MUPS single channel rate in precision mode
- ▶ 78 ns small signal settling time to 0.1% accuracy
- ▶ 100 ns large signal settling time to 0.1% accuracy
- Ultrasmall glitch: <50 pV×s</p>
- Ultralow latency: 5 ns
- THD: -105 dB at 1 kHz for AD3541R-16 and -95 dB at 1 kHz for AD3541R-12
- ► 5 selectable output voltage ranges
- ▶ 1.2 V and 1.8 V logic level compatible
- Single (classic) and dual SPI modes
- Multiple error detectors, both analog and digital domains
- 2.5 V internal voltage reference, 10 ppm/°C maximum TC
- Small package: 4 mm × 4 mm LFCSP

### **APPLICATIONS**

- Instrumentation
- Hardware in the loop
- Process control equipment
- Medical devices
- Automated test equipment
- Data acquisition system
- Programmable voltage sources
- Optical communications

### FUNCTIONAL BLOCK DIAGRAM

### **GENERAL DESCRIPTION**

The AD3541R is a low drift, single channel, ultra-fast, 12-/16-bit accuracy, voltage output digital-to-analog converter (DAC) that can be configured in multiple voltage span ranges. The AD3541R operates with a fixed 2.5 V reference.

Each DAC incorporates three drift compensating feedback resistors for the internal transimpedance amplifier (TIA) that scales the output voltage. The device has five preconfigured output voltage ranges: 0 V to 2.5 V, 0 V to 5 V, 0 V to 10 V, -5 V to +5 V, and -2.5 V to +7.5 V.

The AD3541RBCPZ16 (hereafter referred to as AD3541R-16) can operate in fast mode for maximum speed or precision mode for maximum accuracy. The AD3541RBCPZ12 (hereafter referred to as AD3541R-12) has a single operation mode.

The serial peripheral interface (SPI) can be configured in dual SPI and single SPI (classic SPI) mode with single date rate (SDR) or double data rate (DDR), with logical levels from 1.2 V to 1.8 V.

The AD3541R is specified over the extended industrial temperature range ( $-40^{\circ}$ C to  $+105^{\circ}$ C).

#### Table 1. Related Devices

Part No.	Description
LTC6655	0.25 ppm noise, low drift precision reference
ADR4525	Ultralow noise, high accuracy, 2.5 V voltage reference
AD3552R	Dual channel, 16-bit, 33 MUPS, multispan, multi-IO SPI DAC
AD3551R	Single channel, 16-bit, 33 MUPS, multispan, multi-IO SPI DAC
AD3542R	Single channel, 12-/16-bit, 16 MUPS, multispan, multi-IO SPI DAC



Figure 1. Functional Block Diagram

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. A



Information furnished by Analog Devices is believed to be accurate and reliable "as is". However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

### TABLE OF CONTENTS

1
1
1
1
1
1
3
3
)
)
)
1
2
1
5
5
5
5
5
5
5

V <sub>RFF</sub>	26
SPI Register Map Access	26
Serial Interface	
DAC Update Modes	34
Power-Down	35
Reset	
Error Detection	35
ALERT Pin	
Device ID	37
Summary of Interface Access Modes	37
Registers	38
Register Summary	38
Interface Register Details	41
DAC Register Details	50
Applications Information	58
Power Supply Recommendations	58
Layout Guidelines	58
Outline Dimensions	59
Ordering Guide	59
Evaluation Boards	59

## **REVISION HISTORY**

### 5/2023—Rev. 0 to Rev. A

Changed Single Channel, 16-Bit, 16 MUPS, Multispan, Multi-IO SPI DAC to Single Channel, 12-/16-Bit,	
16 MUPS, Multispan, Multi-IO SPI DAC	1
Changes to Features Section	1
Changes to General Description Section and Table 1	1
Changes to Figure 1	1
Changes to Relative Accuracy (INL) Parameter, Differential Nonlinearity (DNL) Parameter, V <sub>LOGIC</sub> Pin	
Parameter, and DV <sub>DD</sub> Dynamic Current Parameter, Table 2	4
Changes to Table 3	6
Change to Table 5	10
Changes to Figure 9 and Table 7	11
Changes to Figure 10 Caption to Figure 13 Caption	. 12
Added Figure 14; Renumbered Sequentially	12
Change to Figure 15 Caption	12
Changes to Figure 16 Caption to Figure 18 Caption	. 13
Added Figure 19	. 13
Changes to Figure 20 Caption and Figure 21 Caption	. 13
Changes to Figure 22 Caption and Figure 23 Caption	. 14
Change to Figure 32 Caption	15
Added Figure 33	. 15
Changes to Figure 34 Caption to Figure 36 Caption	. 16
Added Figure 37	. 16
Change to Figure 38 Caption	16
Added Figure 39	. 16
Change to Figure 68 Caption	21

### TABLE OF CONTENTS

Added Figure 69	21
Changes to Figure 70 and Figure 72 Caption	22
Added Figure 73	22
Changes to Relative Accuracy or Integral Nonlinearity (INL) Section	24
Changes to Differential Nonlinearity (DNL) Section	24
Changes to DC PSRR and AC PSRR Section	24
Changes to Output Voltage Settling Time Section	24
Changes to Digital-to-Analog Glitch Impulse Section	24
Changes to Digital Feedthrough Section	24
Changes to Output Noise Spectral Density Section	24
Changes to Total Harmonic Distortion (THD) Section	24
Changes to Product Description Section	25
Changes to DAC Architecture Section and Figure 77	25
Changes to Output Voltage Spans Section and Table 8	25
Changes to Transfer Function Section	25
Changes to TIA Power Consumption Section	25
Change to Figure 82	27
Changes to Streaming Mode Section	28
Changes to Figure 84 Caption and Figure 85	29
Changes to Serial Interface Section	32
Change to Figure 92	34
Changes to SDIO Drive Strength Section and Figure 93	34
Changes to DAC Update Modes Section and Figure 94	34
Changes to Table 13	35
Changes to Power-Down Section	35
Changes to Table 16	38
Changes to Table 17	39
Change to Product ID Low Register Section	43
Changes to Power Supply Recommendations Section and Figure 96	58
Changes to Layout Guidelines Section	58
Changes to Ordering Guide	59

## 5/2022—Revision 0: Initial Version

## **ELECTRICAL CHARACTERISTICS**

 $\begin{array}{l} {\sf AV}_{DD} = 5.0 \; V \pm 5\%, \; DV_{DD} = 1.8 \; V \pm 5\%, \; 1.1 \; V \leq V_{LOGIC} \leq 1.9 \; V, \; V_{REF} = 2.5 \; V, \; 4.75 \; V \leq PV_{DD} - PV_{SS} \leq 10.6 \; V, \; 4.75 \; V \leq PV_{DD} \leq 10.6 \; V, \; -5.3 \; V \leq PV_{SS} \leq 0 \; V, \; \text{and} \; -40^{\circ}\text{C} \leq \text{T}_{A} \leq +105^{\circ}\text{C}, \; \text{unless otherwise noted}. \end{array}$ 

Table 2.						
Parameter <sup>1</sup>	Symbol	Min	Тур	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE						
Resolution		16			Bits	
Relative Accuracy (INL)		-2		+2	LSB	AD3541R-16, 5 V range only
		-4		+4	LSB	AD3541R-16, all other ranges <sup>2</sup>
		-1		+1	LSB	AD3541R-12, all ranges
Differential Nonlinearity (DNL)		-1		+1	LSB	AD3541R-16, precision mode: -40°C to +105°C, fast mode: 0°C to 85°C
		-2		+2	LSB	AD3541R-16, fast mode: -40°C to +105°C
		-2		+2	LSB	AD3541R-16. 0 V to 2.5 V range, fast or precision mode <sup>2</sup>
		-0.5		+0.5	LSB	AD3541R-12, all ranges
Offset Frror		-0.15	+0.03	+0.15	%FSR	Midscale (MS), 25°C
Offset Error Drift <sup>2</sup>		0.10	2	7	ppm FSR/°C	0  V to $5  V$ $0  V$ to $10  V$ and $-25  V$ to $+75  V$ ranges
			4	11	ppm FSR/°C	$0 \vee to 2 5 \vee and -5 \vee to +5 \vee ranges$
Full-Scale Error		-0.3	+0.03	+0.3	%FSR	25°C
Full-Scale Error Drift <sup>2</sup>		0.0	20.00	7	nnm ESR/°C	$0 \vee t_0 5 \vee 0 \vee t_0 10 \vee and -25 \vee t_0 +75 \vee ranges$
			2	8	ppm FSR/°C	$0 \vee to 2 5 \vee and -5 \vee to +5 \vee ranges$
Zero Scale Error <sup>3</sup>		-0.35	-0.03	+0 35	%ESP	25°C
Zero-Scale Error Driff <sup>2</sup>		0.00	3	7		0.1 to $5.1$ 0.1 to $10.1$ and $-2.5.1$ to $+7.5.1$ ranges
			5	1 10	ppm FSB/°C	0.7 to $2.5$ V and $-5$ V to $+5$ V ranges
Total Upadiustad Error (TUE)		0.5	5	12		
DC Dewer Supply Dejection Datis (DSDD)		-0.5	0.6	+0.5	%F3R	DAC code - mideoele
			0.0		111V/V	
	V <sub>OUTx_ZS</sub>					All US loaded into the DAC register, 25°C
0 V to 2.5 V Range			-0.198		V	
0 V to 5 V Range			-0.077		V	
0 V to 10 V Range			-0.163		V	
−5 V to +5 V Range			-5.163		V	
-2.5 V to +7.5 V Range			-2.666		V	
Full-Scale Voltage <sup>4</sup>	V <sub>OUTx_FS</sub>					All 1s loaded into the DAC register, 25°C
0 V to 2.5 V Range			2.697		V	
0 V to 5 V Range			5.076		V	
0 V to 10 V Range			10.163		V	
−5 V to +5 V Range			5.166		V	
−2.5 V to +7.5 V Range			7.662		V	
Short-Circuit Current			73 and 85		mA	Sourcing and sinking
Load Regulation			10		μV/mA	
Capacitive Load Stability			200		pF	2 kΩ in parallel with capacitor
REFERENCE OUTPUT						
Output Voltage		2.492	2.5	2.508	V	At 25°C, over lifetime
Voltage Reference Temperature Coefficient (TC) <sup>5</sup>			3 3	10 15	ppm/°C ppm/°C	0°C to 105°C -40°C to +105°C
Output Impedance			50		mΩ	
Output Voltage Noise			3.2		μV rms	0.1 Hz to 10 Hz, no load on V <sub>REF</sub>

### Table 2. (Continued)

Parameter <sup>1</sup>	Symbol	Min	Тур	Max	Unit	Test Conditions/Comments
Output Voltage Noise Density			173		nV/√Hz	f = 1 kHz, no load on V <sub>REF</sub>
			167		nV/√Hz	f = 10 kHz, no load on V <sub>REF</sub>
Capacitive Load Stability <sup>2</sup>			4.7		μF	
Load Regulation			50		µV/mA	At 25°C
Output Current Load Capability			±8		mA	
Line Regulation			142		μV/V	At 25°C
REFERENCE INPUT						
Reference Current			1		μA	
Reference Input Range <sup>2</sup>	V <sub>REF</sub>	2.4	2.5	2.6	V	
Reference Input Impedance			3		MΩ	
LOGIC INPUTS						
Input Current	li li	-1		+1	μA	Per pin
Input Low Voltage	V <sub>IL</sub>			0.35 × V <sub>LOGIC</sub>	V	
Input High Voltage	V <sub>IH</sub>	0.65 × V <sub>LOGIC</sub>			V	
Pin Capacitance	CI		4		pF	
LOGIC OUTPUTS						
Output Low Voltage	V <sub>OL</sub>			0.20 × V <sub>LOGIC</sub>	V	I <sub>SINK</sub> = 100 μA
Output High Voltage	V <sub>OH</sub>	0.80 × VLOGIC			V	I <sub>SOURCE</sub> = 100 μA
Pin Capacitance	Co	20010	4		pF	
POWER REQUIREMENTS						
V <sub>LOGIC</sub> Pin		1.1	1.8	1.89	V	
V <sub>LOGIC</sub> Current	ILOGIC		1	7.5	μA	$V_{IH} = V_{LOGIC} \times 0.9, V_{IL} = V_{LOGIC} \times 0.1$
V <sub>LOGIC</sub> Dynamic Current	ILOGIC_DYNAMIC		2	3.2	mA	SCLK = 66 MHz, dual SPI DDR, $V_{IH}$ = $V_{LOGIC} \times 0.65$ , $V_{IL}$ = $V_{LOGIC} \times 0.35$
DV <sub>DD</sub> Pin		1.71	1.8	1.89	V	
DV <sub>DD</sub> Current	I <sub>DVDD</sub>		0.5	0.8	mA	
DV <sub>DD</sub> Dynamic Current	IDVDD_DYNAMIC		24	26	mA	AD3541R-16, SCLK = 66 MHz, dual SPI DDR
			15	18	mA	AD3541R-12, SCLK = 66 MHz, dual SPI DDR
AV <sub>DD</sub> Pin		4.75	5	5.25	V	
AV <sub>DD</sub> Current	I <sub>DD</sub>		12	15	mA	
AV <sub>DD</sub> Power-Down Current	I <sub>DD</sub>		0.6		mA	After reset, DACs powered down
AV <sub>DD</sub> Reset Current	I <sub>DD</sub>		120		μA	RESET asserted
PV <sub>DD</sub> Pin		4.75		10.6	V	
PV <sub>DD</sub> Current	I <sub>PVDD</sub>		4.5		mA	10 V range full scale, load current not included
PV <sub>DD</sub> Power-Down Current	I <sub>PVDD</sub>		32	40	μA	Channel power-down bit set
PV <sub>SS</sub> Pin		PV <sub>DD</sub> - 10.6		0	V	
PV <sub>SS</sub> Current <sup>6</sup>	I <sub>PVSS</sub>		3.8		mA	±5 V range zero scale, load current not included
PV <sub>SS</sub> Power-Down Current	I <sub>PVSS</sub>		32	40	μA	Channel power-down bit set
Recommended Headroom and Footroom			200		mV	See Figure 51

<sup>1</sup> See the Terminology section.

<sup>2</sup> Guaranteed by design and characterization, not production tested.

<sup>3</sup> Measured at zero code.

<sup>4</sup> See the Output Voltage Spans section.

<sup>5</sup> Reference temperature coefficient is calculated as per the box method.

 $^{\rm 6}$   $\,$  Measured as current sourced from the  $\rm PV_{SS}$  pin.

## **AC CHARACTERISTICS**

 $AV_{DD} = 5.0 \text{ V} \pm 5\%, \text{ DV}_{DD} = 1.8 \text{ V} \pm 5\%, 1.1 \text{ V} \le \text{V}_{\text{LOGIC}} \le 1.9 \text{ V}, 4.75 \text{ V} \le \text{PV}_{\text{DD}} - \text{PV}_{\text{SS}} \le 10.6 \text{ V}, 4.75 \text{ V} \le \text{PV}_{\text{DD}} \le 10.6 \text{ V}, -5.3 \text{ V} \le \text{PV}_{\text{SS}} \le 0 \text{ V}, \text{ and } -40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +105^{\circ}\text{C}, \text{ unless otherwise noted.}$ 

Table 3.

Parameter <sup>1</sup>	Min Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Output Voltage Settling Time	100		ns	2 V step, 0.1% error, 0 V to 5 V range
	85		ns	2 V step, 1% error, 0 V to 5 V range
	78		ns	60 mV step, 0.1% error, 0 V to 5 V range
	22		ns	60 mV step, 1% error, 0 V to 5 V range
Slew Rate	100		V/µs	Full-scale step, 0 V to 2.5 V range, −40 °C to +105°C
	140		V/µs	Full-scale step, all other ranges, −40 °C to +105 °C
Digital-to-Analog Glitch Impulse	50		pV×s	0 V to 5 V range, ±1 LSB change around major carry
Digital Feedthrough	12		pV×s	50 MHz clock, R <sub>FB</sub> 2_x
AC PSRR	80		dB	1 kHz, R <sub>FB</sub> 1_x
	43		dB	1 MHz, R <sub>FB</sub> 1_x
Output Noise Spectral Density	20		nV/√Hz	DAC code = midscale, external reference, 10 kHz, R <sub>FB</sub> 1_x
	40		nV/√Hz	R <sub>FB</sub> 2_x
Output Noise	3.8		μV <sub>RMS</sub>	DAC code = midscale, external reference, 1 Hz to 10 kHz, R <sub>FB</sub> 1_x
	7.6		μV <sub>RMS</sub>	R <sub>FB</sub> 2_x
Total Harmonic Distortion (THD)	-105		dB	AD3541R-16, 0 V to 5 V range, f <sub>OUT</sub> = 1 kHz
	-101		dB	AD3541R-16, f <sub>OUT</sub> = 10 kHz
	-90		dB	AD3541R-12, f <sub>OUT</sub> = 1 kHz to 10 kHz
	-84		dB	f <sub>OUT</sub> = 100 kHz
Spurious-Free Dynamic Range (SFDR)	-105		dB	AD3541R-16, 0 V to 5 V range, f <sub>OUT</sub> = 1 kHz
	-92		dB	AD3541R-12

<sup>1</sup> See the Terminology section.

## TIMING CHARACTERISTICS

 $AV_{DD} = 5.0 \text{ V} \pm 5\%, \text{ DV}_{DD} = 1.8 \text{ V} \pm 5\%, 1.1 \text{ V} \le \text{V}_{\text{LOGIC}} \le 1.9 \text{ V}, 4.75 \text{ V} \le \text{PV}_{\text{DD}} - \text{PV}_{\text{SS}} \le 10.6 \text{ V}, 4.75 \text{ V} \le \text{PV}_{\text{DD}} \le 10.6 \text{ V}, -5.3 \text{ V} \le \text{PV}_{\text{SS}} \le 0 \text{ V}, \text{ and } -40^{\circ}\text{C} \le \text{T}_{\text{A}} \le +105^{\circ}\text{C}, \text{ unless otherwise noted.}$ 

Table 4.						
Parameter <sup>1, 2</sup>	Description	Min	Тур	Мах	Unit	Test Conditions/Comments
f <sub>SCLK</sub>	SCLK frequency			66	MHz	
t <sub>1</sub>	SCLK cycle time	15.2			ns	
t <sub>SCLK/2</sub>	SCLK half period	7.6			ns	
t <sub>2</sub>	CS falling edge to first SCLK rising edge	5			ns	
t <sub>3</sub>	Last SCLK sampling edge <sup>3</sup> to CS rising edge	10			ns	
t <sub>4</sub>	CS falling edge from SCLK sampling edge ignored	5			ns	
t <sub>5</sub>	CS rising edge to SCLK rising edge ignored	5			ns	
t <sub>6</sub>	Minimum CS high time	10			ns	
t <sub>7</sub>	Data setup time	2			ns	
t <sub>8</sub>	Data hold time	2			ns	
t <sub>9</sub>	SCLK falling edge to SDO data valid			15	ns	1.7 < V <sub>LOGIC</sub> < 1.9

#### Table 4. (Continued)

Parameter <sup>1, 2</sup>	Description	Min	Тур	Max	Unit	Test Conditions/Comments
				25	ns	1.1 < V <sub>LOGIC</sub> < 1.7
t <sub>10</sub>	SCLK sampling edge to LDAC falling edge	7.6			ns	
t <sub>11</sub>	LDAC pulse width low	7.6			ns	
t <sub>12</sub>	CS rising edge to SDO disabled		50		ns	
t <sub>13</sub>	$\overline{\text{LDAC}}$ rising edge to $\overline{\text{CS}}$ falling edge	5			ns	
t <sub>14</sub>	RESET pulse width low	10			ns	t <sub>14</sub> to t <sub>19</sub> shown in Figure 8
t <sub>15</sub>	RESET pulse activation time			100	ns	
t <sub>16</sub>	V <sub>OUTx</sub> update from CHx_DAC register write		12.6		ns	
t <sub>17</sub>	V <sub>OUT</sub> update from LDAC falling edge		5		ns	
t <sub>18</sub> 4	Wait time before DAC register access	100			ms	
t <sub>19</sub> 5	Shutdown exit time		5		ms	
Update Rate	Dual SPI mode, DDR and streaming enabled, precision mode			11	MUPS <sup>6</sup>	
	Dual SPI mode, DDR and streaming enabled, fast mode			16.5	MUPS <sup>6</sup>	

<sup>1</sup> All input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  (10% to 90%) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

<sup>2</sup> Guaranteed by design and characterization, not production tested.

<sup>3</sup> The SCLK sampling edge refers to the SCLK edge where the data is read in (sampled).

 $^4$   $\,$  Same timing must be expected at power-up from the instant that AV\_{DD} = 4 V or DV\_{DD} = 0.8 V.

<sup>5</sup> Time required to exit power-down to normal mode.

<sup>6</sup> MUPS is mega updates per second.

### Timing Diagrams



#### Figure 2. Classic SPI Write Operation with Single Data Rate



Figure 3. Classic SPI Read Operation with Single Data Rate



Figure 4. Classic SPI Write Operation with Double Data Rate



Figure 5. Dual SPI Write Operation with Single Data Rate



Figure 6. Dual SPI Read Operation with Single Data Rate







Figure 8. Start-Up Sequence Timing

### **ABSOLUTE MAXIMUM RATINGS**

 $T_A = 25^{\circ}C$ , unless otherwise noted.

#### Table 5.

Parameter	Rating
AV <sub>DD</sub> to AGND	-0.3 V to +6 V
DV <sub>DD</sub> to DGND	-0.3 V to +2.1 V
AGND to DGND	-0.3 V to +0.3 V
V <sub>LOGIC</sub> to DGND	-0.3 V to DV <sub>DD</sub> + 0.3 V or
	+2.1 V (whichever is less)
PV <sub>DD</sub> to PV <sub>SS</sub>	-0.3 V to +11 V
V <sub>REF</sub> to AGND	-0.3 V to +3 V
R <sub>FB</sub> x_y to AGND	-18 V to +18 V
Digital Input Voltage to DGND	-0.3 V to V <sub>LOGIC</sub> + 0.3 V or +2.1 V (whichever is less)
Operating Temperature Range	
Industrial	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature (T <sub>J</sub> )	125°C
Power Dissipation	(Maximum Τ <sub>J</sub> – Τ <sub>A</sub> )/θ <sub>JA</sub>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

 $\theta_{JA}$  is the natural convection junction to ambient thermal resistance.

 $\theta_{JC}$  is the junction to case thermal resistance. Both  $\theta_{JA}$  and  $\theta_{JC}$  are defined by the JEDEC JESD51 standard, and their values are dependent on the test board and test environment.

#### Table 6. Thermal Resistance<sup>1</sup>

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
CP-28-15	54	12	°C/W

<sup>1</sup> Simulation values on JEDEC 2S2P board, still air (0 m/sec airflow).

### **ESD CAUTION**



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 9. Pin Configuration

#### Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1	DV <sub>DD</sub>	S	Digital Core Power Supply. 1.8 V ± 5%.
2	V <sub>LOGIC</sub>	S	Digital Interface Power Supply. 1.2 V to 1.8 V.
3	CS	DI	Chip Select, Active Low Logic Input. This is the frame synchronization signal for the input data.
4	SCLK	DI	Serial Clock Input.
5	SDI/SDIO0	DI/O	Serial Data Input in Classic SPI Mode.
			Serial Bidirectional Input/Output Bit 0 in Dual SPI Mode.
6	SDO/SDIO1	DI/O	Serial Data Output in Classic SPI Mode.
			Serial Bidirectional Input/Output Bit 1 in Dual SPI Mode.
7	LDAC	DI	Load DAC, Active Low Logic Input. <u>LDAC</u> can be operated in two modes: synchronous or asynchronous. Pulsing this pin low causes the DAC register to update if the input register has new data. If this pin is tied permanently low, the DAC automatically updates when new data is written to the input register.
8	RESET	DI	Asynchronous Reset Input. Active low logic input. When $\overline{\text{RESET}}$ is low, all registers are reset to their default values and the activity on the digital interface is ignored. The AD3541R incorporates a power-on reset (POR) circuit. If this pin is not used, it must be tied to V <sub>LOGIC</sub> .
9	ALERT	DO	Alert Pin. Active low logic output. This pin is driven low if an alert condition is detected and it is not masked by the corresponding bit in the mask register. This pin has an internal configurable pull-up resistor.
10, 26	AGND	S	Analog Ground Reference. It is recommended to connect DGND and AGND to the same ground plane under the device.
11 to 15, 28	DNC		Do Not Connect. Leave these pins floating.
16	PV <sub>DD</sub>	S	Positive Supply Voltage for Output Amplifier.
17	AV <sub>DD</sub>	S	Analog Power Supply. 5 V ± 5%.
18	V <sub>REF</sub>	AI/O	Voltage Reference, 2.5 V. Input when using the external reference, and output or floating when using the internal reference.
19	CV <sub>REF</sub>	AI/O	Decoupling Capacitor for Internal Reference, Optional.
20	V <sub>OUT</sub> 0	AI/O	Analog Output Voltage for Channel 0.
21	R <sub>FB</sub> 4_0	AI/O	Hardware Gain Selection for Channel 0, Gain = 4.
22	R <sub>FB</sub> 2_0	AI/O	Hardware Gain Selection for Channel 0, Gain = 2.
23	R <sub>FB</sub> 1_0	AI/O	Hardware Gain Selection for Channel 0, Gain = 1.
24	CAP0	AI/O	Amplifier Feedback Capacitor for Channel 0. Connect a capacitor (NP0 recommended) between this pin and V <sub>OUT0</sub> to adjust the amplifier bandwidth.
25	PV <sub>SS</sub>	S	Negative Rail for Output Amplifier.
27	DGND	S	Digital Ground Reference. It is recommended to connect DGND and AGND to the same ground plane under the device.

<sup>1</sup> S = supply, DI = digital input, DO = digital output, and AI/O = analog input/output.

AVDD = 5 V,  $DV_{DD} = V_{LOGIC} = 1.8$  V, 4.75 V  $\leq PV_{DD} - PV_{SS} \leq 10.6$  V, 4.75 V  $\leq PV_{DD} \leq 10.6$  V, -5.3 V  $\leq PV_{SS} \leq 0$  V, external voltage reference, temperature = 25°C (ambient), and decoupling as outlined in the Power Supply Recommendations section, unless otherwise noted.



Figure 10. AD3541R-16 DNL vs. Code, 0 V to 5 V Range, -40°C, Fast Mode and Precision Mode



Figure 11. AD3541R-16 DNL vs. Code, 0 V to 5 V Range, 25°C, Fast Mode and Precision Mode



Figure 12. AD3541R-16 DNL vs. Code, 0 V to 5 V Range, 85°C, Fast Mode and Precision Mode



Figure 13. AD3541R-16 DNL vs. Code, 0 V to 5 V Range, 105°C, Fast Mode and Precision Mode



Figure 14. AD3541R-12 DNL vs. Code vs. Temperature, 0 V to 5 V Range



Figure 15. AD3541R-16 INL vs. Code, 0 V to 5 V Range, -40°C, Fast Mode and Precision Mode



Figure 16. AD3541R-16 INL vs. Code, 0 V to 5 V Range, 25°C, Fast Mode and Precision Mode



Figure 17. AD3541R-16 INL vs. Code, 0 V to 5 V Range, 85°C, Fast Mode and Precision Mode



Figure 18. AD3541R-16 INL vs. Code, 0 V to 5 V Range, 105°C, Fast Mode and Precision Mode



Figure 19. AD3541R-12 INL vs. Code vs. Temperature, 0 V to 5 V Range



Figure 20. AD3541R-16 DNL vs. Range, Fast Mode and Precision Mode



Figure 21. AD3541R-16 INL vs. Range, Fast Mode and Precision Mode







Figure 23. AD3541R-16 INL vs. Temperature



Figure 24. TUE vs. Temperature



Figure 25. TUE vs. Range



Figure 26. Offset Error vs. Range



Figure 27. Offset Error vs. Temperature



Figure 28. Zero-Scale Error vs. Temperature



Figure 29. Full-Scale Error vs. Temperature



Figure 30. Output Noise Spectral Density (NSD) vs. Frequency



Figure 31. Output Load Stability (C<sub>FB</sub> Is Feedback Capacitor)



Figure 32. AD3541R-16 THD vs. Tone Frequency



Figure 33. AD3541R-12 THD vs. Tone Frequency







Figure 35. AD3541R-16 THD vs. Range



Figure 36. AD3541R-16 Spectral Noise Density with 1 kHz Sine Wave Playback (HD2 Is Second Harmonic Distortion, HD3 Is Third Harmonic Distortion, HD4 Is Fourth Harmonic Distortion)



Figure 37. AD3541R-12 Spectral Noise Density with 1 kHz Sine Wave Playback



Figure 38. AD3541R-16 Fast Fourier Transform (FFT) with 1 kHz Sine Wave, 12.5 MUPS



Figure 39. AD3541R-12 Fast Fourier Transform (FFT) with 1 kHz Sine Wave, 12.5 MUPS



Figure 40. Zero-Scale Voltage Distribution, 0 V to 2.5 V Range



Figure 41. Zero-Scale Voltage Distribution, 0 V to 5 V Range



Figure 42. Zero-Scale Voltage Distribution, 0 V to 10 V Range



Figure 43. Zero-Scale Voltage Distribution, -5 V to +5 V Range



Figure 44. Zero-Scale Voltage Distribution, -2.5 V to +7.5 V Range



Figure 45. Full-Scale Voltage Distribution, 0 V to 2.5 V Range



Figure 46. Full-Scale Voltage Distribution, 0 V to 5 V Range



Figure 47. Full-Scale Voltage Distribution, 0 V to 10 V Range



Figure 48. Full-Scale Voltage Distribution, -5 V to +5 V Range



Figure 49. Full-Scale Voltage Distribution, -2.5 V to +7.5 V Range



Figure 50. Source and Sink Capability, 5 V Range



Figure 51. Headroom and Footroom vs. Load Current







Figure 53. Digital-to-Analog Glitch Energy Histogram



Figure 54. Digital Feedthrough



Figure 55. Small Signal Settling Time, 0 V to 5 V Range (R<sub>LOAD</sub> Is Load Resistance)



Figure 56. Small Signal Settling Time, 0 V to 10 V Range



Figure 57. Small Signal Settling Time, -5 V to +5 V Range



Figure 58. Large Signal Settling Time, 0 V to 5 V Range



Figure 59. Large Signal Settling Time, 0 V to 10 V Range



Figure 60. Large Signal Settling Time, -5 V to +5 V Range



Figure 61. Slew Rate vs. Temperature



Figure 62. AC PSRR vs. Frequency



Figure 63. Reference Voltage (V<sub>REF</sub>) NSD vs. Frequency, Load Impedance











Figure 66. Reference Voltage Spread



Figure 67. V<sub>REF</sub> vs. Temperature



Figure 68. AD3541R-16 DV<sub>DD</sub> Dynamic Current vs. SPI Clock Frequency, SPI Mode



Figure 69. AD3541R-12 DV<sub>DD</sub> Dynamic Current vs. SPI Clock Frequency, SPI Mode











Figure 72. AD3541R-16 DV<sub>DD</sub> Dynamic Current vs. Temperature



Figure 73. AD3541R-12 DV<sub>DD</sub> Dynamic Current vs. Temperature







Figure 75. PV<sub>SS</sub> Current vs. Temperature



Figure 76.  $\text{PV}_{\text{DD}}$  and  $\text{PV}_{\text{SS}}$  Current vs. Range

## TERMINOLOGY

### **Relative Accuracy or Integral Nonlinearity (INL)**

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

### **Differential Nonlinearity (DNL)**

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes.

### **Offset Error**

Offset error is the vertical deviation from the ideal transfer function after the gain error has been compensated. Offset error is expressed in mV. In the AD3541R, offset error is measured at midscale. The comparison between the ideal output and the actual output is performed at midscale.

### **Offset Error Drift**

The offset error drift is a measurement of the relative variation of the offset with temperature. It is expressed in ppm/°C. Total offset at a given temperature is calculated as

$$Offset_{T} = Offset_{25^{\circ}C} + \frac{TC \times (T - 25) \times V_{RANGE}}{10^{6}}$$

### Full-Scale and Zero-Scale Error

These errors measure the deviation from the ideal value at full scale and zero scale, at 25°C. The error is expressed as % of full-scale range (FSR). In the case of the AD3541R, the ideal value is calculated as the average of a sufficiently high number of samples.

### Full-Scale and Zero-Scale Error Drift

These parameters measure the variation of the zero-scale and full-scale voltage as a function of the temperature, relative to the ideal zero-scale and full-scale voltages. They are expressed in ppm/°C. The total deviation over temperature is calculated using the same formula used for the offset.

### **DC PSRR and AC PSRR**

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V<sub>OUT</sub> to a change in the supplies for midscale output of the DAC. DC PSRR is measured in mV/V, and AC PSRR is measured in dB. V<sub>REF</sub> is held at 2.5 V, and the supplies are varied by ±200 mV p-p.

## **Output Voltage Settling Time**

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level within a given accuracy for a given step change. Typically, it is evaluated for a small step and a large step to account for the effect of amplifier slewing.

## Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV × sec and is measured when the digital input code is changed by 1 LSB.

### **Digital Feedthrough**

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. Digital feedthrough is specified in nV × sec and measured with a full-scale code change on the data bus, which means from all 0s to all 1s and vice versa.

### **Output Noise Spectral Density**

Noise spectral density is a measurement of the internally generated random noise. Noise is measured at the DAC output when it is loaded with the midscale code and using an ideal external reference. Noise is also measured at the output of the internal reference, if available. Noise density is expressed in  $nV/\sqrt{Hz}$ . Figure 30 depicts the spectral density of the noise in the 1/f region and the flat (broadband) region, whereas the specification quoted in Table 2 pertains to the flat region.

### **Total Harmonic Distortion (THD)**

THD is the difference between the sine wave played by the DAC and an ideal sine wave of the same frequency and amplitude. The deviation from an ideal sine wave is due to time and amplitude discretization and nonlinear distortion. THD is measured as the power ratio of the sum of harmonic components to the fundamental component. It is expressed in dB.

# Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as shown in the following equation:

$$TC = \left(\frac{V_{REF}MAX - V_{REF}MIN}{V_{REF}NOM \times TEMP_RANGE}\right) \times 10^{6}$$
(1)

where:

*V<sub>REF\_MAX</sub>* is the maximum reference output measured over the total temperature range.

*V<sub>REF\_MIN</sub>* is the minimum reference output measured over the total temperature range.

 $V_{REF, NOM}$  is the nominal reference output voltage, 2.5 V. TEMP\_RANGE is the specified temperature range, -40°C to +105°C.

### **PRODUCT DESCRIPTION**

The AD3541R is a single channel, 16 MUPS voltage output DAC with programmable output ranges and a 2.5 V internal reference. This device is available in 16-bit and 12-bit resolutions.

The AD3541R-16 has two update modes.

- Fast mode: data written in this mode is 16 bits long, resulting in a single-channel update rate of 16 MUPS. The DNL specification is valid for the reduced temperature range defined in Table 2. The data for this mode is written in the registers ending in \_16B.
- Precision mode: data written in this mode is 24 bits long, resulting in a single-channel update rate of 11 MUPS. The DNL specification is guaranteed over the full operating temperature range. The data for this mode is written in the registers ending in \_24B.

The AD3541R-12 supports fast mode only. The \_24B registers are not accessible. 12-bit data must be written to the \_16B registers, leaving the four LSBs set to 0.

The AD3541R offers a versatile SPI interface capable of operating in classic and dual SPI modes with single or double data rate. The AD3541R features multiple error checkers, both in the analog and digital domains to guarantee a safe operation.

### DAC ARCHITECTURE

The AD3541R uses a current steering DAC architecture with a  $V_{\text{REF}}$  voltage of 2.5 V. The DAC current is converted to voltage by means of an internal TIA.

Figure 77 shows the internal block diagram.



Figure 77. DAC Channel Architecture Block Diagram

The TIA feedback loop is closed by hardwiring the V<sub>OUT</sub>x pin to any of the available R<sub>FB</sub>x\_y pins. The R<sub>FB</sub>x\_y value sets the maximum voltage span that can be achieved. The R<sub>FB</sub>x\_y pin used for each voltage range is specified in the Output Voltage Spans section.

### **OUTPUT VOLTAGE SPANS**

The AD3541R offers five voltage spans that are selected using the CH0\_OUTPUT\_RANGE register. The selected span must be in accordance with the feedback resistor being used, as shown in Table 8. Setting a voltage span that is not achievable with the current  $R_{FB}x_y$  resistor results in an incorrect voltage value.

The supply levels on  $\mathsf{PV}_{\mathsf{DD}}$  and  $\mathsf{PV}_{\mathsf{SS}}$  must also be adjusted to guarantee enough headroom and footroom for each range.

There is approximately a 3% overrange equally split on each end of the span to ensure that the nominal range is covered in any condition.

Table 8. Output Spar	Ranges and	Corresponding	Feedback	Resistor
----------------------	------------	---------------	----------	----------

		Output Span		
R <sub>FB</sub> x_y	CH0_OUTPUT_RANGE	(V)	V <sub>ZS</sub> (V)	V <sub>FS</sub> (V)
R <sub>FB</sub> 1_y	0x000	0 to 2.5	-0.197	2.701
	0x001	0 to 5	-0.077	5.077
R <sub>FB</sub> 2_y	0x010	0 to 10	-0.162	10.164
	0x011	-5 to +5	-5.164	5.162
	0x100	-2.5 to +7.5	-2.663	7.663

### TRANSFER FUNCTION

The conversion of the digital code to the DAC output current follows a linear relation with the code in plain binary. The ideal output voltage is given by the following equation:

$$V_{OUT} = (V_{FS} - V_{ZS}) \times \frac{D}{2^{16}} + V_{ZS}$$

where:

*D* is the decimal equivalent of the binary code that is loaded in the DAC register. For the AD3541R-12, *D* is still a 16-bit number where the lower four bits are 0, that is, the 12-bit code multiplied by 16.  $V_{ZS}$  and  $V_{FS}$  are according to the values given in the Output Voltage Spans section.

### INTERNAL TIA

The internal TIA is capable of operating at 20 mV from the supply rails,  $PV_{DD}$  and  $PV_{SS}$ . The supplies of the internal TIA must be adapted to accommodate the desired output range while observing the minimum headroom, footroom, and maximum supply voltage.

### **TIA POWER CONSUMPTION**

The static power consumption of the internal TIA depends on the output voltage, the feedback resistor, and the load resistance. The following formulas approximate the current drawn by a single amplifier on  $PV_{DD}$  and  $PV_{SS}$  as a function of these parameters, as long as the amplifier is not in saturation. Current values in mA are:

$$I_{PVDD} = 0.65 + max \left( 0, \frac{V_{OUT} - 2.5}{R_{FB}} + \frac{V_{OUT}}{R_L} \right)$$
  
$$I_{PVSS} = -0.65 + min \left( 0, \frac{V_{OUT} - 2.5}{R_{FB}} + \frac{V_{OUT}}{R_L} \right)$$

where:

 $V_{OUT}$  is the output voltage in volts.  $R_{FB}$  is the value of the feedback resistor in k $\Omega$ .

 $R_{l}$  is the load resistance in k $\Omega$ .

The first term of the equations is the quiescent current of an individual amplifier. Amplifiers are active at power up and can be disabled setting the CHx\_CHANNEL\_POWERDOWN bit in POW-

analog.com

ERDOWN\_CONFIG register. In AD3541R, channel 1 amplifier is present and active at power up. Unless disabled, its quiescent current is present so the first term of the equation is double.

### V<sub>REF</sub>

The AD3541R has an internal 2.5 V voltage reference with a 3 ppm/°C temperature coefficient that is enabled at power-up. The  $V_{REF}$  pin is in high impedance at power-up to avoid electrical problems. If the internal reference must be used externally, the REFERENCE\_VOLTAGE\_SEL bits in the REFERENCE\_CONFIG register must be written to enable the  $V_{REF}$  output as described in Table 9.

When the external reference is selected, the  $V_{\text{REF}}\xspace$  pin behaves as an input.

#### Table 9. Voltage Reference Selection

REFERENCE_VOLTAGE_SEL	Source	V <sub>REF</sub> I/O
00	Internal	Floating
01	Internal	2.5 V
10	External	Input
11	External	Input

### SPI REGISTER MAP ACCESS

### SPI Frame Synchronization

The  $\overline{CS}$  signal frames data during an SPI transaction. A falling edge on  $\overline{CS}$  enables the digital interface and initiates an SPI transaction. Each SPI transaction consists of at least one instruction phase and data phase, as described in the Instruction Phase section and the Data Phase section. For all SPI transactions, data is aligned MSB first. Deasserting  $\overline{CS}$  during an SPI transaction terminates part or all of the data transfer and disables the digital interface. If  $\overline{CS}$  is deasserted (returned high) after one or more register addresses are issued, those registers are written or read, but any partially addressed register is ignored. Figure 78 and Figure 79 outline the stages of a basic SPI write and read frame, respectively, for the AD3541R in register mode.

Detailed timing diagrams for register read and write operations are shown in Figure 2 through Figure 7. The timing specification is given in the Timing Characteristics section.

The AD3541R SPI protocol is flexible and can be configured to suit the needs of a variety of digital hosts. Data from multiple registers can be accessed in a single SPI frame, enabling efficient device configuration. All the different access modes are described in the Single Instruction Mode section and the Streaming Mode section.

### **Instruction Phase**

Every SPI frame starts with an instruction phase. The instruction phase immediately follows the falling edge of  $\overline{CS}$  that initiates the SPI transaction.

The instruction phase consists of a read/write bit (R/W) followed by a register address word. Setting R/W low initiates a write instruction, whereas setting R/W high initiates a read instruction. The register address word specifies the address of the register to be accessed. The register address word is 7 bits in length (7-bit addressing) by default. If required, 15-bit addressing can be enabled by setting the SHORT\_INSTRUCTION bit to 0 in the INTER-FACE\_CONFIG\_B register. If the user is using single instruction mode, each register read or write transaction in a single SPI frame also begins with an instruction phase. If the user is using streaming mode, only one instruction phase is required per SPI frame to access a set of consecutive registers. See the Single Instruction Mode section and the Streaming Mode section for instructions on selecting and using these modes.

### Data Phase

The data phase immediately follows the instruction phase, as shown in Figure 78 and Figure 79. The data phase can include the data for a single-byte register, a multibyte register, or multiple registers depending on the selected registers and access modes. See the Single Instruction Mode section, Streaming Mode section, and Address Direction section for descriptions of how these modes affect the read and write data in the data phase.

In a write operation, the content of the addressed register is updated immediately after the SCLK edge, which shifts in the last bit of the register data, regardless if it is a one-byte, two-byte, or three-byte register. Multibyte registers cannot be written partially, as explained in the Multibyte Registers section.

In a read operation, the content of the addressed register starts shifting out on the first SCLK edge of the data phase.

Data must be written to the AD3541R configuration registers in full bytes to ensure they are updated. If the data phase of an SPI write transaction does not include the entire byte of data for the register being updated, the contents of the register are not updated, and the CLOCK\_COUNTING\_ERROR bit in the INTERFACE\_STATUS\_A register is set.



Figure 79. Basic SPI Read Frame

### **Multibyte Registers**

Some AD3541R registers consist of 2 or 3 bytes of data stored in adjacent addresses and are referred to as multibyte registers. Multibyte registers end with a 16B or 24B suffix when they are 2 bytes or 3 bytes, respectively.

When writing to a multibyte register of the AD3541R, all bytes must be transferred in a single SPI transaction. For this reason, the STRICT\_REGISTER\_ACCESS bit in the INTERFACE\_CONFIG\_C register is read only and set to 1. If an SPI write transaction to a multibyte register is attempted on a per byte basis, the register contents are not updated and the PARTIAL\_REGISTER\_ACCESS bit in the INTERFACE\_STATUS\_A register is set. A write transaction to a multibyte register of the AD3541R takes effect after the 24<sup>th</sup> or 16<sup>th</sup> SCLK edge of the data phase, which shifts in the last bit of the register data.





The address of a multibyte register always depends on the ADDR\_DIRECTION bit in the INTERFACE\_CONFIG\_A register (see the Address Direction section for more details). With descending addressing, the first byte accessed in the data phase must be the most significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next lower address. With ascending addressing, the first byte accessed in the data phase must be the least significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next lower address. With ascending addressing, the first byte accessed in the data phase must be the least significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next higher address.

Multibyte registers can be read in a single SPI transaction or each byte can be addressed separately. If an SPI read transaction to a multibyte register is attempted on a per byte basis, the PARTI-AL\_REGISTER\_ACCESS bit in the INTERFACE\_STATUS\_A register is set. For example, the VENDOR\_ID register is 2 bytes long, and the addresses of its least significant byte and most significant byte are 0x0C and 0x0D, respectively. Figure 80 and Figure 81 show write and read transactions to a multibyte register (2 bytes) for address ascending and descending mode, respectively. See the Address Direction section for more information on selecting address descending (auto-decrementing) or ascending (auto-incrementing).

### Address Direction

The address direction option is used to control whether the register address is set to automatically increment (address ascending) or decrement (address descending) when transferring multiple bytes of data in a single data phase (for example, when accessing multibyte registers, as shown in Figure 80 and Figure 81, or when accessing multiple registers with streaming mode, as shown in Figure 83).

Address direction is selected with the ADDR\_DIRECTION bit in the INTERFACE\_CONFIG\_A register. If ADDR\_DIRECTION is set to 0, the address decrements after each byte is accessed. If ADDR\_DIRECTION is set to 1, the address increments after each byte is accessed.

When accessing multibyte registers, use descending addresses to shift in the most significant byte first.

Multibyte registers from Address 0x29 onwards can only be accessed in descending mode.

### Single Instruction Mode

When the SINGLE\_INSTRUCTION bit in the INTERFACE\_CON-FIG\_B register is set to 1, streaming mode is disabled, and single instruction mode is enabled. In single instruction mode, the data phase only contains data for a single register, and each data phase must be followed by a new instruction phase, even if  $\overline{CS}$  remains low. Single instruction mode allows the digital host to quickly read from and write to registers with nonadjacent addresses in a single SPI frame, whereas streaming mode only allows either reading or writing to contiguous registers without pulsing  $\overline{CS}$  high to initiate a new instruction phase.

Figure 82 shows an example of an SPI transaction in single instruction mode with the following register accesses:

- ▶ Sets the output range.
- ▶ Enables the output stage.
- ▶ Reads the CHIP\_TYPE register.



Figure 82. Single Instruction Mode Register Access Example with Address Descending

### **Streaming Mode**

When the SINGLE\_INSTRUCTION bit in the INTERFACE\_CON-FIG\_B register is set to 0, single instruction mode is disabled and streaming mode is enabled. In streaming mode, multiple registers with adjacent addresses can be accessed with a single instruction phase and data phase, allowing efficient access of contiguous regions of memory (for example, during initial device configuration). The AD3541R is configured in streaming mode by default.

When in streaming mode, each SPI frame consists of a single instruction phase and the following data phase contains data for multiple registers with adjacent addresses. A starting register address is specified by the digital host in the instruction phase, and this address is automatically incremented or decremented (based on the address direction setting) after each byte of data is accessed. The data phase can, therefore, be multiple bytes long, and each consecutive byte of read or write data corresponds to the next higher or lower register address (for ascending and descending address direction, respectively).

When writing or reading from a multibyte register in streaming mode with address ascending, the user must address the least significant byte of the register in the instruction phase. The data phase starts transferring data from the least significant byte in first place.

When writing or reading from a multibyte register in streaming mode with the address descending, the user must start addressing the most significant byte of the register in the instruction phase. The data phase starts transferring the most significant byte in first place.

Figure 83 shows the instruction and data phase when using streaming mode with address descending to write some registers of the AD3541R starting from Address 0x16. The length of the data phase determines the number of data bytes to be transferred to consecutive addresses.  $\overline{CS}$  is brought high at the end of the write transaction (in Figure 83, the end of the write transaction occurs after Address 0x02).

Figure 84 shows the instruction and data phase when using streaming mode with address descending to read some registers of the AD3541R starting from Address 0x16. The length of the data phase determines the number of data bytes to be transferred to consecutive addresses.  $\overline{CS}$  is brought high at the end of the read

transaction (in Figure 84, the end of the read transaction occurs after Address 0x02).

The STREAM\_MODE register can be used to specify a range of consecutive registers to loop through in the data phase. Looping allows the digital host to repeatedly read from or write to a set of registers (for example, CHx\_DAC\_16B register at Address 0x29 to Address 0x2C) as efficiently as possible. When accessing register addresses after and including Address 0x29, the address direction must always be set as descending.

If STREAM\_MODE is set to 0, looping is disabled and the following occurs:

- If address direction is set to descending, the address decrements until it reaches 0x00. On the subsequent byte accesses, the address is set to the top of the addressable space (Address 0x4B). Note that restrictions may apply in terms of SPI mode access depending on the register address.
- If address direction is set to ascending, the address increments until it reaches the top of the addressable space (Address 0x4B). On the subsequent byte access, the address is reset to 0x00. Note that restrictions may apply in terms of SPI mode access depending on the register address. Multibyte registers greater than 0x29 do not update in ascending mode.

If STREAM\_MODE is set to a value other than 0, looping is enabled and the value corresponds to the number of bytes to be accessed in the data phase before the address loops back to the value specified in the address phase. An example is shown in Figure 85, where the CH0\_DAC\_16B register is accessed twice using the looping feature.

The value of the STREAM\_MODE register can be preserved or reset to 0 at the end of the transaction (when CS returns high) depending on the value of the STREAM\_LENGTH\_KEEP\_VALUE bit in the TRANSFER\_REGISTER, as shown in Table 10. This feature allows writing the same range of registers continuously within the same transaction, which is useful for waveform playback.

|--|

STREAM_LENGTH_KEEP_VALUE	STREAM_MODE Register
0	Autoreset
1	Keeps previous value



Figure 83. Streaming Mode Register Write with Address Descending



#### Figure 84. Streaming Mode Register Read with Address Descending



Figure 85. Looping Enabled with Address Descending and STREAM\_MODE = 2

### **CRC Error Detection**

The AD3541R features an optional CRC to provide error detection for SPI transactions between the digital host (master) and the AD3541R (slave).

CRC error detection allows SPI masters and slaves to detect bit transfer errors with significant reliability. The CRC algorithm involves using a seed value and polynomial division to generate a CRC code. The master and slave both calculate the CRC code independently and compare it to determine the validity of the transferred data.

The AD3541R uses the CRC-8 standard with the following polynomial:

$$x^8 + x^2 + x + 1 \tag{2}$$

CRC error detection is enabled with the CRC\_EN and CRC\_EN\_B bits in the INTERFACE\_CONFIG\_C register. The value of CRC\_EN is only updated if CRC\_EN\_B is set to the CRC\_EN inverted value in the same register write instruction. Therefore, to enable the CRC, CRC\_EN must be set to 0b01 while CRC\_EN\_B is set to 0b10 in the same write transaction.

To disable the CRC, CRC\_ENABLE must be set to 0b00 while CRC\_ENABLE\_B is set to 0b11 in the same write transaction. Writing inverted values to two separate fields reduces the chances of CRC being enabled by mistake. CS must be brought high at the end of the enable or disable write. The transaction following the enabling of the CRC must already include the CRC byte, regardless if it is a write or read operation. A register write transaction that disables CRC must still include the CRC code at the end, but the transaction following the disabling of the CRC does not have to include the CRC byte.

Figure 86 and Figure 87 show how a CRC code is appended at the end of a write or read transaction, respectively, in single SPI mode (classic mode). For register writes, the digital host must generate the CRC by performing the calculation described in Equation 2 on the seed, the address, and the data. The AD3541R performs the

**SPI Transaction Type** Streaming Mode, Subsequent Data Phases Pin Single Instruction Mode Streaming Mode, First Data Phase SDI Read No CRC sent 0xA5, instruction phase, padding 0xA5, instruction phase, padding SDO 0xA5, instruction phase, read data 0xA5, instruction phase, read data Least significant byte of address, read data Write SDI Least significant byte of address, write data 0xA5, instruction phase, write data 0xA5, instruction phase, write data SDO 0xA5, instruction phase, write data 0xA5, instruction phase, write data Least significant byte of address, write data

Table 11. CRC Seed Values and Extent of CRC Calculation

same calculation and shifts out the CRC code on SDO at the same time as the host. The transaction is free of error if both CRC codes match. For register reads, the host calculates the CRC on the seed, the address, and a zero padding while the AD3541R calculates the CRC on the seed, the address, and the readout data. Both nodes then shift out the CRC code at the same time so that it can be checked on both sides.



Figure 87. Basic SPI Read Frame with CRC

DATA PHASE

INSTRUCTION PHASE

When accessing multibyte registers with CRC error detection enabled, the CRC code is placed after all of the bytes of register data.

When CRC error detection is enabled, the AD3541R does not update its register contents in response to a register write transaction unless it receives a valid CRC code at the end of the register data. If the CRC code is invalid, or if the digital host fails to transmit the CRC code, the AD3541R does not update its register contents, and the INVALID\_OR\_NO\_CRC flag in the INTERFACE\_STATUS\_A register is set. The INVALID\_OR\_NO\_CRC flag is cleared when 1 is written to this bit, and the correct CRC is required for the write to clear the bit to take effect.

 Table 11 shows the seed value used in the CRC code calculation

 and how it is calculated for both single instruction mode and

 streaming mode.

When using single instruction mode, every CRC code in an SPI frame uses 0xA5 as the seed value to prevent stuck at fault conditions for Address 0x00.

When using streaming mode, the first CRC code in an SPI frame also uses 0xA5 as the seed value, but subsequent CRC codes in the same frame are calculated using the least significant byte of the register address being accessed in the SPI transaction as the seed value.

Because enabling the CRC in single SPI (classic) mode requires that the SDO pin shifts out the CRC calculated by the AD3541R,

the transaction must respect the limitations of a read operation, which is that DDR is disabled.

In dual SPI modes, the CRC is appended at the end of the byte or multibyte register transaction but the CRC is generated only by the controller (write) or by the AD3541R (read), as shown in Figure 88.

When CRC error detection is enabled, do not use streaming mode, including looping, if the range of registers being addressed includes unused or reserved registers.

<del>cs</del>		
SCLK		
SDI/SDIO0	X R/W X ADDR6 X ADDR5 X ADDR4 X ADDR3 X ADDR2 X ADDR1 X ADDR0 X D14 X D12 X D10 X D8 X D6 X D4 X D2 X D0 X	
SDO/SDIO1	<u> </u>	990

Figure 88. Dual SPI Transaction with CRC

### SERIAL INTERFACE

The AD3541R implements a versatile serial interface that is compatible with several SPI modes. The interface is configured in single SPI (classic SPI) mode by default and can be switched to dual SPI by acting on the configuration registers. DDR can be enabled in any of the modes to duplicate the transfer speed in the data phase.

Clock polarity (CPOL) can be 1 or 0, but clock phase (CPHA) must be always 0. These combinations correspond to SPI Mode 0 and Mode 3, which are applicable when the SPI interface is in single data rate (SDR) mode.

### Single SPI (Classic) Mode

In single SPI (classic) mode, the SDI/SDIO0 and SDO/SDIO1 data lines are unidirectional. The SDI signal behaves as an input to transfer data from master to slave and the SDO signal behaves as an output to transfer data from slave to master, as shown in Figure 89. Single SPI (classic) mode is compatible with SPI Mode 0 and Mode 3, as well as with completely synchronous interfaces, such as synchronous serial port (SPORT<sup>™</sup>). See Figure 2 for a timing diagram of a typical write sequence. See the AN-1248 Application Note, *SPI Interface*, for more information about the classic SPI mode.

> CS SCLK

SDI00



Figure 89. Single SPI (Classic SPI) Connection

### **Dual SPI Mode**

In dual SPI mode, the SDI/SDIO0 and SDO/SDIO1 data lines are bidirectional, as shown in Figure 90. During the data phase, the  $R/\overline{W}$  bit of the instruction phase defines the direction of the data lines. During the instruction phase, the data lines are always configured as inputs. In dual SPI mode, consecutive bits are serialized in groups of two, as shown in Figure 91.



D0

D1

D12 D10

D11...)

D15 D13

Figure 91. Dual SPI Mode

R/W / ADDR6 & ADDR5 & ADDR4 & ADDR3 & ADDR2 & ADDR1 & ADDR0 & D14 &

### **Double Data Rate (DDR)**

Irrespective of the SPI mode being used, DDR can be enabled by setting the SPI\_CONFIG\_DDR bit in the INTERFACE\_CONFIG\_D register, which allows sampling data during the data phase on both clock edges, as shown in Figure 4 and Figure 7. After this mode is enabled, all data must be written using DDR.

DDR is only usable in the data phase during write operations. In readback operations, the SPI CONFIG DDR bit is ignored, and

#### Table 12. SPI Mode Combinations

data is transferred from the AD3541R to the controller in single data rate, as shown in Figure 2 and Figure 6.

After changing the SPI mode or the SPI\_CONFIG\_DDR bit,  $\overline{CS}$  must be brought high and a new access cycle must be started in the appropriate mode.

All valid SPI mode combinations are listed in Table 12.

SPI Mode	MULTI_IO_MODE	SPI_CONFIG_DDR
Single SPI SDR	00	0
Single SPI DDR	00	1
Dual SPI SDR	01	0
Dual SPI DDR	01	1

## **Register Map SPI Access Modes**

The register map is divided in two regions, primary and secondary.

The registers related to interface configuration, DAC configuration, and error flags are comprised in the primary region from Address 0x0 to Address 0x1E. This region can only be accessed in classic SPI mode with or without DDR, regardless of the value of MUL-TI\_IO\_MODE in the TRANSFER\_REGISTER.

The registers affecting the output value of the DAC are comprised in the secondary region from Address 0x28 to Address 0x4B. This region can be accessed in any of the SPI modes, with or without DDR.



Figure 92. Register Access Modes

### **SDIO Drive Strength**

The driving strength of the SDIO lines on the SDO/SDIO1, and SDI/SDIO0 pins can be configured to four different levels by setting the SDIO\_DRIVE\_STRENGTH bits in the INTERFACE\_CONFIG\_D register.

Higher drive strength value corresponds to a faster signal slew rate, as shown in Figure 93. However, higher slew rate means higher peak current and higher digital noise in the system. The default value is medium low strength.



Figure 93. Driving Strength Options

## DAC UPDATE MODES

There are several ways to update the DAC output, synchronously or asynchronously, directly or indirectly.

A synchronous update occurs when the change of the DAC output is triggered by an external signal, such as  $\overline{\text{LDAC}}$ , which can be common to many devices. In this case, the controller loads a value in the input register that is later transferred to the DAC register on the falling edge of the  $\overline{\text{LDAC}}$  signal, causing the simultaneous update of all V<sub>OUT</sub> signals.

To update the DAC using the  $\overline{\text{LDAC}}$  signal, the HW\_LDAC\_MASK\_CH0 bit in the HW\_LDAC\_16B or HW\_LDAC\_24B register, depending on the precision mode, must be set to 0.

An asynchronous update occurs when the change of the DAC output follows an operation on the register set. In this case, the change is aligned with the SCLK edge that shifts the last register bit in. The several combinations to update the DAC output are described in Table 13.

Page mask registers are provided for compatibility with the multichannel devices, AD3552R and AD3542R. To update the DAC using the page registers, the value of the SEL\_CH0 bit in the CH\_SELECT\_16B or CH\_SELECT\_24B register must be set to 1. Writing to the DAC\_PAGE register transfers the data to the CH0\_DAC register and writing to the INPUT\_PAGE register transfers the data to the CH0\_INPUT register. The data flow between registers is summarized in Figure 94.



Figure 94. DAC Data Flow Between Registers

#### Table 13. DAC Update Modes

SPI Mode	Register Written	LDAC Pin	Synchronous	Notes
Dual and Single SPI	CH0_INPUT	Falling edge	Yes	LDAC mask applied, HW_LDAC register.
Dual and Single SPI	CH0_INPUT	High	No	Write to SW_LDAC triggers the update.
Dual and Single SPI	CH0_INPUT	Low	No	Output updates automatically.
Dual and Single SPI	CH0_DAC	Not applicable	No	Output updates immediately.
Dual and Single SPI	DAC_PAGE	Not applicable	No	Page mask applied, according to CH_SELECT register. Output updates immediately.
Dual and Single SPI	INPUT_PAGE	Not applicable	No	Page mask applied, according to CH_SELECT register. Data copied to input register.

### POWER-DOWN

Each of the two DAC coresThe DAC core in the AD3541R can be disabled to reduce power consumption when the channel is not in use. Control is performed using the CH0\_DAC\_POWERDOWN bit in the POWERDOWN\_CONFIG register. The DAC core is powered down after reset and becomes active on the first update.

In addition, the internal TIA can be disabled by setting the CHx\_CHANNEL\_POWERDOWN bit in the POWERDOWN\_CON-FIG register. The TIA is powered up by default after reset.

### RESET

The AD3541R implements three different ways to reset the device. All three methods trigger the same reset procedure internally, except for the difference explained in the Software Reset section.

### **Power-On Reset**

The device integrates a power-on reset (POR) circuit that monitors  $AV_{DD}$  and  $DV_{DD}$ . Whenever  $AV_{DD}$  falls below 4 V or  $DV_{DD}$  falls below 1.3 V, an internal reset pulse is generated. This circuit ensures that the chip is correctly initialized at power-up or after a power dip.

### **RESET** Pin

A low level on the RESET pin sets the chip in default mode, clearing the values of all registers, setting the  $V_{OUT}$ 0 outputs to 0 V, and keeping the SPI lines in high impedance. When the RESET line is released (returns high), the device starts executing the initialization procedure that can take up to 100 ms ( $t_{18}$  time).

Table 14. Alarm Mask Register and Corresponding Error Source

After reset, the DAC core is in power-down mode and the  $V_{\text{OUT}}$  outputs are still at 0 V.

During reset, the internal transimpedance amplifier is still powered up and it may produce some glitch in the  $V_{OUT}$  signal, depending on the sequencing of the supplies.

### Software Reset

The device can be reset from the SPI interface by setting the SW\_RESET\_MSB and SW\_RESET\_LSB bits in the INTER-FACE\_CONFIG\_A register. The main difference between the software reset and the hardware reset using the RESET pin is that the former does not affect the INTERFACE\_CONFIG\_A register. The SW\_RESET\_MSB and SW\_RESET\_LSB bits clear after the reset operation has concluded.

### ERROR DETECTION

The AD3541R can detect abnormal conditions both in the analog and digital domains. These errors are reported in the INTER-FACE\_STATUS\_A and ERR\_STATUS registers. The list of the errors mapped to the ERR\_ALARM\_MASK register and its corresponding source is shown in Table 14. The errors listed in Table 14 can assert the ALERT pin if it is not masked in the ERR\_ALARM\_MASK register. The ALERT pin is also asserted after reset and in case of initialization failure.

The error bits in the INTERFACE\_STATUS\_A and ERR\_STATUS registers are sticky and keep their value until cleared with a write 1 operation. That is, to clear an error bit, write 1 on that specific bit location.

Bit Number	Alarm Mask Register Bit Name	Error Source Register Name	Error Source Bit Name
6	REF_RANGE_ALARM_MASK	ERR_STATUS	REF_RANGE_ERR_STATUS
5	CLOCK_COUNT_ALARM_MASK	INTERFACE_STATUS_A	CLOCK_COUNTING_ERROR
4	MEM_CRC_ALARM_MASK	ERR_STATUS	MEM_CRC_ERR_STATUS
3	SPI_CRC_ERR_ALARM_MASK	INTERFACE_STATUS_A	INVALID_OR_NO_CRC
2	WRITE_TO_READ_ONLY_ALARM_MASK	INTERFACE_STATUS_A	WRITE_TO_READ_ONLY_REGISTER
1	PARTIAL_REGISTER_ACCESS_ALARM_MASK	INTERFACE_STATUS_A	PARTIAL_REGISTER_ACCESS
0	REGISTER_ADDRESS_INVALID_ALARM_MASK	INTERFACE_STATUS_A	REGISTER_ADDRESS_INVALID

## ERR\_STATUS Register

### V<sub>REF</sub> Detection

The REF\_RANGE\_ERR\_STATUS bit in the ERR\_STATUS register is set when the reference voltage drops below 1 V for more than 5 ms. The error is detected irrespective of the reference voltage source, whether it is generated internally or provided externally via the V<sub>REF</sub> pin. This feature is useful to detect an interruption in the external reference voltage or an overload condition on the V<sub>REF</sub> pin when the internal reference is shared with another device.

### **SPI Mode Error**

The SPI mode error is produced during streaming when the address pointer crosses the boundary between the secondary and the primary region with the SPI interface configured in dual SPI mode because this region can only be accessed in classic SPI mode. The DUAL\_SPI\_STREAM\_EXCEEDS\_DAC\_ERR\_STATUS bit is set in the ERR\_STATUS register.

### **Register CRC**

The AD3541R includes an internal CRC for the register map and the read only memory (ROM). The CRC is executed every 4.1 µs, and only includes the primary region of the register map because the secondary region is expected to be continuously written. The CRC can be disabled by clearing the MEM\_CRC\_EN bit in the INTERFACE\_CONFIG\_D register. If a CRC error is detected, the MEM\_CRC\_ERR\_STATUS bit is set in the ERR\_STATUS register. It is advisable to reset the device if this error occurs.

### **Reset Status**

The RESET\_STATUS bit in the ERR\_STATUS register indicates that the AD3541R has been reset, either internally (POR or SW reset) or externally (via the RESET pin). The RESET\_STATUS bit is set when the POR completes correctly. It is useful to detect unexpected reset conditions, such as a dip in power supply, and take corrective actions.

The RESET\_STATUS bit causes the assertion of the ALERT pin and it is not maskable. Therefore, it must be cleared after reset or power-up to be able to detect new events via the ALERT signal.

## INTERFACE\_STATUS\_A Register

### **Device Busy**

The INTERFACE\_NOT\_READY bit in the INTERFACE\_STATUS\_A register is not an error, but a status bit. This bit can be polled to know when the device is ready to receive data from the controller.

### **SPI Clock Counter**

The error reported in the CLOCK\_COUNTING\_ERR bit is produced when the number of SCLK cycles is not in accordance AD3541R

with the amount required to shift a multiple of 8 bits, taking into account the SPI mode (dual or single) and the DDR mode. The CLOCK\_COUNTING\_ERR bit is set in the ERR\_STATUS register.

Valid combinations are shown in Table 15.

	•	
SPI Mode	DDR	Clock Cycles for 1 Byte
Single SPI	No	8
Single SPI	Yes	4
Dual SPI	No	4
Dual SPI	Yes	2

### SPI CRC

The INVALID\_OR\_NO\_CRC bit in the INTERFACE\_STATUS\_A register is set when the CRC is enabled and the CRC byte in the SPI transaction is missing or it does not match the calculated value. To clear this error, write 1 to this bit. Note that because CRC is enabled, this SPI transaction must have a valid CRC code to succeed.

### Write to Read Only Register

If the host tries to write to a read only register, the WRITE\_TO\_READ\_ONLY\_REGISTER bit field is asserted in the INTERFACE\_STATUS\_A register. To clear this error, write 1 to the WRITE\_TO\_READ\_ONLY\_REGISTER bit.

### **Partial Register Access**

The PARTIAL\_REGISTER\_ACCESS bit in the INTERFACE\_STA-TUS\_A register is set when a multibyte register is accessed for read or write partially, which means that the transaction ends before all the bytes of a multibyte register have been accessed. To clear this error, write 1 to the PARTIAL\_REGISTER\_ACCESS bit.

### Invalid Access

When the host tries to access an invalid register address, the REG-ISTER\_ADDRESS\_INVALID bit is set in the INTERFACE\_STA-TUS\_A register. To clear this error, write 1 to this bit.

### **ALERT** PIN

When one of the errors listed in Table 14 is detected and its corresponding bit in the ERR\_ALARM\_MASK register is set to 0, the ALERT pin is asserted. This pin can be used as an interrupt line for the CPU to take action when an error condition arises.

In addition, the ALERT pin is asserted when the RESET\_STATUS bit is asserted in the ERR\_STATUS register. This condition is not maskable. Therefore, the RESET\_STATUS bit must be cleared after initialization to use the ALERT pin. If the pin remains asserted after clearing all the error sources, it means that there has been an error during the initialization of the device and it must be power cycled.

analog.com

The ALERT pin requires a pull-up resistor that can be provided externally or internally. The chip incorporates an internal 2.5 k $\Omega$  pull-up resistor that can be enabled by setting the ALERT\_ENABLE\_PULLUP bit in the INTERFACE\_CONFIG\_D register.

The ALERT pin is deasserted when all the errors are cleared in their corresponding registers.

### **DEVICE ID**

The AD3541R includes numerous registers providing silicon related information. The following registers can be used to identify that the correct chip type and version are assembled:

- ▶ CHIP TYPE
- ▶ PRODUCT\_ID\_L

- ▶ PRODUCT\_ID\_H
- ▶ CHIP GRADE
- ▶ SPI REVISION
- ► VENDOR L
- ▶ VENDOR H

### SUMMARY OF INTERFACE ACCESS MODES

Finding the correct SPI mode can be difficult given the number of modes and the restrictions on specific registers or memory regions. To facilitate the implementation of the driver in the CPU, a decision tree is presented in Figure 95. Figure 95 depicts how the driver must proceed depending on the configuration of the interface and the registers being accessed.



Figure 95. Register Access Modes

## **REGISTER SUMMARY**

## **Register List**

### Table 16. Register Summary

Address	Name	Description	Reset	Access
0x00	INTERFACE_CONFIG_A	Interface Configuration A Register.	0x10	R/W
0x01	INTERFACE_CONFIG_B	Interface Configuration B Register.	0x08	R/W
0x02	DEVICE_CONFIG	Device Configuration Register.	0x00	R
0x03	CHIP_TYPE	Chip Type Register.	0x04	R
0x04	PRODUCT_ID_L	Product ID Low Register.	0x0B	R
0x05	PRODUCT_ID_H	Product ID High Register.	0x40	R
0x06	CHIP_GRADE	Chip Grade Register.	0x05	R
0x0A	SCRATCH_PAD	Scratch Pad Register.	0x00	R/W
0x0B	SPI_REVISION	SPI Revision Register.	0x83	R
0x0C	VENDOR_L	Vendor ID Low Register.	0x56	R
0x0D	VENDOR_H	Vendor ID High Register.	0x04	R
0x0E	STREAM_MODE	Stream Mode Register.	0x00	R/W
0x0F	TRANSFER_REGISTER	Transfer Configuration Register.	0x00	R/W
0x10	INTERFACE_CONFIG_C	Interface Configuration C Register.	0x23	R/W
0x11	INTERFACE_STATUS_A	Interface Status A Register.	0x00	R/W
0x14	INTERFACE_CONFIG_D	Interface Configuration D Register.	0x04	R/W
0x15	REFERENCE_CONFIG	Reference Configuration Register.	0x00	R/W
0x16	ERR_ALARM_MASK	Error Alarm Mask Register.	0x00	R/W
0x17	ERR_STATUS	Error Status Register.	0x01	R/W
0x18	POWERDOWN_CONFIG	Power-Down Configuration Register.	0x00	R/W
0x19	CH0_OUTPUT_RANGE	Output Range Register.	0x00	R/W
0x28	HW_LDAC_16B	Hardware LDAC Mask Register, Fast Mode.	0x00	R/W
0x29	CH0_DAC_16B	DAC Register for Channel 0, Fast Mode.	0x0000	R/W
0x2D	DAC_PAGE_16B	DAC Page Register, Fast Mode.	0x0000	R/W
0x2F	CH_SELECT_16B	Channel Select for Page Registers, Fast Mode.	0x00	R/W
0x30	INPUT_PAGE_16B	Input Page Register, Fast Mode.	0x0000	R/W
0x32	SW_LDAC_16B	Software LDAC Register, Fast Mode.	0x00	W
0x33	CH0_INPUT_16B	Input Register for Channel 0, Fast Mode.	0x0000	R/W
0x37	HW_LDAC_24B <sup>1</sup>	Hardware LDAC Mask Register, Precision Mode.	0x00	R/W
0x38	CH0_DAC_24B1	DAC Register for Channel 0, Precision Mode.	0x000000	R/W
0x3E	DAC_PAGE_24B <sup>1</sup>	DAC Page Register, Precision Mode.	0x000000	R/W
0x41	CH_SELECT_24B1	Channel Select for Page Registers, Precision Mode.	0x00	R/W
0x42	INPUT_PAGE_24B1	Input Page Register, Precision Mode.	0x000000	R/W
0x45	SW_LDAC_24B1	Software LDAC Register, Precision Mode.	0x00	W
0x46	CH0_INPUT_24B1	Input Register for Channel 0, Precision Mode.	0x000000	R/W

<sup>1</sup> Not available in the AD3541R-12.

## **Detailed Register Map**

## Table 17. Detailed Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	INTERFACE_ CONFIG_A	[7:0]	SW_RESET _MSB	RESERVED	ADDR_ DIRECTION	SDO_ ACTIVE		RESERVED		SW_RESET _LSB	0x10	R/W
0x01	INTERFACE_ CONFIG_B	[7:0]	SINGLE_IN STRUCTION		RESERVED		SHORT_INS TRUCTION		RESERVED		0x08	R/W
0x02	DEVICE_CONFIG	[7:0]	DEVICE_ STATUS_3	DEVICE_ STATUS_2	DEVICE_ STATUS_1	DEVICE_ STATUS_0	CUSTON	I_MODES	OPERATIN	IG_MODES	0x00	R
0x03	CHIP_TYPE	[7:0]		RESE	RVED			CL	ASS		0x04	R
0x04	PRODUCT_ID_L	[7:0]				PRODUC	DT_ID[7:0]				0x0B	R
0x05	PRODUCT_ID_H	[7:0]				PRODUC	T_ID[15:8]				0x40	R
0x06	CHIP_GRADE	[7:0]		DEVICE	GRADE			DEVICE_REVISION			0x05	R
0x0A	SCRATCH_PAD	[7:0]				VA	LUE				0x00	R/W
0x0B	SPI_REVISION	[7:0]				VER	SION				0x83	R
0x0C	VENDOR_L	[7:0]				VID	[7:0]				0x56	R
0x0D	VENDOR_H	[7:0]				VID	[15:8]				0x04	R
0x0E	STREAM_MODE	[7:0]				LEN	IGTH				0x00	R/W
0x0F	TRANSFER_ REGISTER	[7:0]	MULTI_I	O_MODE		RESERVED		STREAM_ RESERVED LENGTH_ KEEP_ VALUE		RVED	0x00	R/W
0x10	INTERFACE_ CONFIG_C	[7:0]	CRC_E	NABLE	STRICT_ REGISTER_ ACCESS		RESERVED CRC_ENABLE_B		NABLE_B	0x23	R/W	
0x11	INTERFACE_ STATUS_A	[7:0]	INTERFACE _NOT_ READY	RESERVED	CLOCK_ COUNTING ERROR	RESERVED	INVALID_ OR_NO_ CRC	WRITE_TO_ READ_ ONLY_ REGISTER	PARTIAL_ REGISTER_ ACCESS	REGISTER_ ADDRESS_ INVALID	0x00	R/W
0x14	INTERFACE_ CONFIG_D	[7:0]	RESERVED	ALERT_ ENABLE_ PULLUP	RESERVED	MEM_CRC_ EN	SDIO_DRIVE	_STRENGTH	RESERVED	SPI_ CONFIG_ DDR	0x04	R/W
0x15	REFERENCE_ CONFIG	[7:0]	RESERVED	IDUMP_ FASTMODE		RESE	RVED		REFERENCI	E_VOLTAGE_ EL	0x00	R/W
0x16	ERR_ALARM_ MASK	[7:0]	RESERVED	REF_ RANGE_ ALARM_ MASK	CLOCK_ COUNT_ ERR_ ALARM_ MASK	MEM_CRC_ ERR_ ALARM_ MASK	SPI_CRC_ ERR_ ALARM_ MASK	WRITE_TO_ READ_ ONLY_ ALARM_ MASK	PARTIAL_ REGISTER_ ACCESS_ ALARM_ MASK	REGISTER_ ADDRESS_ INVALID_ ALARM_ MASK	0x00	R/W
0x17	ERR_STATUS	[7:0]	RESERVED	REF_ RANGE_ ERR_ STATUS	DUAL_SPI_ STREAM_ EXCEEDS_ DAC_ERR_ STATUS	MEM_CRC_ ERR_ STATUS		RESERVED		RESET_ STATUS	0x01	R/W
0x18	POWERDOWN_ CONFIG	[7:0]	RESE	RVED	RESERVED	CH0_DAC_ POWERDO WN	RESE	RVED	RESERVED	CH0_ CHANNEL_ POWERDO WN	0x00	R/W
0x19	CH0_OUTPUT_ RANGE	[7:0]		RESE	RVED			CH0_OUTPUT	RANGE_SEL		0x00	R/W
0x28	HW_LDAC_16B	[7:0]			RESE	RVED			RESERVED	HW_LDAC_ MASK_CH0	0x00	R/W
0x2A	CH0_DAC_16B	[15:8]				DAC_DA	TA0[15:8]				0x00	R/W

### Table 17. Detailed Register Summary (Continued)

Reg	Name	Bits	Bit 7 Bi	it6 E	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x29		[7:0]				DAC_D	ATA0[7:0]				0x00	
0x2E	DAC_PAGE_16B	[15:8]				DAC_P	AGE[15:8]				0x00	R/W
0x2D	-	[7:0]				DAC_F	AGE[7:0]				0x00	
0x2F	CH_SELECT_16B	[7:0]			RESE	RVED			RESERVED	SEL_CH0	0x00	R/W
0x31	INPUT_PAGE_ 16B	[15:8]		INPUT_PAGE[15:8]						0x00	R/W	
0x30		[7:0]		INPUT_PAGE[7:0]					0x00	1		
0x32	SW_LDAC_16B	[7:0]			RESE	RVED			RESERVED	SW_LDAC_ CH0	0x00	W
0x34	CH0_INPUT_16B	[15:8]				INPUT_C	ATA0[15:8]				0x00	R/W
0x33		[7:0]				INPUT_I	DATA0[7:0]				0x00	
0x37	HW_LDAC_24B <sup>1</sup>	[7:0]			RESE	RVED			RESERVED	HW_LDAC_ MASK_CH0	0x00	R/W
0x3A	CH0_DAC_24B1	23:16]				DAC_D/	ATA0[15:8]				0x00	R/W
0x39		[15:8]				DAC_D	ATA0[7:0]				0x00	
0x38		[7:0]				RESI	ERVED				0x00	
0x40	DAC_PAGE_24B1	[23:16]				DAC_P	AGE[15:8]				0x00	R/W
0x3F		[15:8]				DAC_F	AGE[7:0]				0x00	
0x3E		[7:0]				RESI	ERVED				0x00	
0x41	CH_SELECT_ 24B <sup>1</sup>	[7:0]			RESE	RVED			RESERVED	SEL_CH0	0x00	R/W
0x44	INPUT_PAGE_ 24B <sup>1</sup>	[23:16]				INPUT_F	PAGE[15:8]				0x00	R/W
0x43		[15:8]				INPUT_	PAGE[7:0]				0x00	
0x42		[7:0]				RESI	ERVED				0x00	
0x45	SW_LDAC_24B <sup>1</sup>	[7:0]			RESE	RVED			RESERVED	SW_LDAC_ CH0	0x00	W
0x48	CH0_INPUT_24B1	[23:16]				INPUT_D	ATA0[15:8]				0x00	R/W
0x47		[15:8]				INPUT_I	DATA0[7:0]				0x00	
0x46		[7:0]				RESI	ERVED				0x00	

<sup>1</sup> Not available in the AD3541R-12.

### INTERFACE REGISTER DETAILS

### Interface Configuration A Register

#### Address: 0x00, Reset: 0x10, Name: INTERFACE\_CONFIG\_A

Interface configuration settings.



#### Table 18. Bit Descriptions for INTERFACE\_CONFIG\_A

Bits	Bit Name	Settings	Description	Reset	Access
7	SW_RESET_MSB	0	First of Two Software Reset Bits. Setting both software reset bits (SW_RESET_MSB and SW_RESET_LSB) in a single SPI write performs a software device reset, returning all registers (except the INTERFACE_CONFIG_A register) to the default power-up state.	0x0	R/W
		1	Initiates a software reset if the SW_RESET_LSB bit is also set to 1 in the same register write transaction.		
6	RESERVED		Reserved.	0x0	R
5	ADDR_DIRECTION	0	Address Direction Bit. Determines sequential addressing behavior when performing register reads and writes on multiple bytes of data in a single data phase. Address descending. Address accessed is automatically decremented by one for each data byte when streaming or addressing multibyte registers. Address ascending. Address accessed is automatically incremented by one for	0x0	R/W
			each data byte when streaming or addressing multibyte registers.		
4	SDO_ACTIVE		SDO Pin Enabled.	0x1	R
[3:1]	RESERVED		Reserved.	0x0	R
0	SW_RESET_LSB		Second of Two Software Reset Bits. Setting both software reset bits (SW_RESET_MSB and SW_RESET_LSB) in a single SPI write performs a software device reset, returning all registers (except the INTERFACE_CONFIG_A register) to the default power-up state.	0x0	R/W
		0	Do nothing.		
		1	Initiates a software reset if the SW_RESET_LSB bit is also set to 1 in the same register write transaction.		

### Interface Configuration B Register

#### Address: 0x01, Reset: 0x08, Name: INTERFACE\_CONFIG\_B

Additional interface configuration settings.



#### Table 19. Bit Descriptions for INTERFACE\_CONFIG\_B

Bits	Bit Name	Settings	Description	Reset	Access
7	SINGLE_INSTRUCTION		Access Mode Bit. Select streaming mode or single instruction mode.	0x0	R/W
		0	Streaming mode. The address increments/decrements as successive data bytes are received according to the ADDR_DIRECTION bit setting in the INTERFACE_CONFIG_A register and the LENGTH bits setting in the STREAM_MODE register.		
		1	Single instruction mode.		
[6:4]	RESERVED		Reserved.	0x0	R
3	SHORT_INSTRUCTION		Short Instruction Bit. Sets the length of the address in the instruction phase to 7 bits or 15 bits.	0x1	R/W
		0	15-bit addressing.		
		1	7-bit addressing.		
[2:0]	RESERVED		Reserved.	0x0	R

#### **Device Configuration Register**

#### Address: 0x02, Reset: 0x00, Name: DEVICE\_CONFIG

This register is intended for compatibility with the standardized register map and it has no effect on this device.



#### Table 20. Bit Descriptions for DEVICE CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
7	DEVICE_STATUS_3		Device Status Bit 3.	0x0	R
6	DEVICE_STATUS_2		Device Status Bit 2.	0x0	R
5	DEVICE_STATUS_1		Device Status Bit 1.	0x0	R
4	DEVICE_STATUS_0		Device Status Bit 0.	0x0	R
[3:2]	CUSTOM_MODES		Modes of Operation.	0x0	R
[1:0]	OPERATING_MODES		Power Modes.	0x0	R
		0	Normal operating mode.		

### Chip Type Register

### Address: 0x03, Reset: 0x04, Name: CHIP\_TYPE

The chip type register contains the identifier of the precision DAC family, which includes the AD3541R. This register must be used in conjunction with the product ID to uniquely identify the AD3541R.



#### Table 21. Bit Descriptions for CHIP\_TYPE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:0]	CLASS		Precision DAC.	0x4	R

### **Product ID Low Register**

### Address: 0x04, Reset: 0x0B, Name: PRODUCT\_ID\_L

Low byte of the product ID.



[7:0] PRODUCT\_ID[7:0] (R) — Product Identification Number.

#### Table 22. Bit Descriptions for PRODUCT\_ID\_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]		Product Identification Number.	0xB	R

### **Product ID High Register**

### Address: 0x05, Reset: 0x40, Name: PRODUCT\_ID\_H

High byte of the product ID.

 7
 6
 5
 4
 3
 2
 1
 0

 0
 1
 0
 0
 0
 0
 0
 0

[7:0] PRODUCT\_ID[15:8] (R) -Product Identification Number.

#### Table 23. Bit Descriptions for PRODUCT\_ID\_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]		Product Identification Number.	0x40	R

### **Chip Grade Register**

### Address: 0x06, Reset: 0x05, Name: CHIP\_GRADE

Identifies product variations and device revisions. The device revision refers to the version of the silicon and the device grade refers to the version of the test procedure.

[7:4] DEVICE\_GRADE (R) This is the Device Performance Grade.  $\begin{bmatrix} 7 & 6 & 5 & 4 & 3 & 2 & 1 & 0 \\ \hline 0 & 0 & 0 & 1 & 0 & 1 \\ \hline 0 & 0 & 0 & 1 & 0 & 1 \\ \hline 1 & 0 & 1 & 0 & 1 \\ \hline 0 & 1 & 0 & 1 \\ \hline 0 & 1 & 0 & 1 \\ \hline 1 & 0 & 0 \\ \hline 1$ 

#### Table 24. Bit Descriptions for CHIP GRADE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DEVICE_GRADE		This is the Device Performance Grade.	0x0	R
[3:0]	DEVICE_REVISION		This is the Device Hardware Revision.	0x5	R

#### Scratch Pad Register

#### Address: 0x0A, Reset: 0x00, Name: SCRATCH\_PAD

This register has no functional purpose. It is provided to test write and read operations.



#### Table 25. Bit Descriptions for SCRATCH PAD

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VALUE		Software Scratchpad.	0x0	R/W

#### **SPI Revision Register**

#### Address: 0x0B, Reset: 0x83, Name: SPI\_REVISION

Indicates the SPI interface revision.

[7:0] VERSION (R) ——— ADI SPI Standard Version.

#### Table 26. Bit Descriptions for SPI\_REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VERSION		ADI SPI Standard Version.	0x83	R

### Vendor ID Low Register

### Address: 0x0C, Reset: 0x56, Name: VENDOR\_L

Low byte of the vendor ID.



[7:0] VID[7:0] (R) Analog Devices Vendor ID.

#### Table 27. Bit Descriptions for VENDOR\_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID[7:0]		Analog Devices Vendor ID.	0x56	R

### Vendor ID High Register

### Address: 0x0D, Reset: 0x04, Name: VENDOR\_H

High byte of the vendor ID.



[7:0] VID[15:8] (R) — Analog Devices Vendor ID.

#### Table 28. Bit Descriptions for VENDOR\_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID[15:8]		Analog Devices Vendor ID.	0x4	R

### **Stream Mode Register**

#### Address: 0x0E, Reset: 0x00, Name: STREAM\_MODE

Defines the length of the loop when streaming data.



#### Table 29. Bit Descriptions for STREAM\_MODE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	LENGTH		Data Byte Loop Count. Specifies the data byte count before looping back to the start address. Only valid in streaming mode. A nonzero value sets the number of data bytes written or read before the address loops back to the start address. A maximum of 255 bytes can be transmitted using this approach. A value of 0x00 disables the loopback so that addressing wraps around at the upper and lower limits of memory.	0x0	R/W

### **Transfer Configuration Register**

### Address: 0x0F, Reset: 0x00, Name: TRANSFER\_REGISTER

This register configures the SPI mode used to transfer data and enables looping over the same register section when streaming data.



#### 1: LENGTH bit field keeps the same value.

#### Table 30. Bit Descriptions for TRANSFER REGISTER

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	MULTI_IO_MODE		Controls the SPI.	0x0	R/W
		00	Single SPI.		
		01	Dual SPI.		
[5:3]	RESERVED		Reserved.	0x0	R
2	STREAM_LENGTH_KEEP_VALUE		This bit controls the reset of the LENGTH bit field value in the STREAM_MODE register.	0x0	R/W
		0	LENGTH bit field is reset to 0 at the end of the transaction.		
		1	LENGTH bit field keeps the same value.		
[1:0]	RESERVED		Reserved.	0x0	R

### Interface Configuration C Register

### Address: 0x10, Reset: 0x23, Name: INTERFACE\_CONFIG\_C

Additional interface configuration settings.



#### Table 31. Bit Descriptions for INTERFACE\_CONFIG\_C

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CRC_ENABLE	00	CRC Enable. This field is written to enable/disable the use of the CRC error detection on the interface (when the device is in register mode). The CRC_ENABLE_B bits must also be written with the inverted value of the CRC_ENABLE bits in the same SPI write transaction for the CRC status to be changed.		R/W
		00	CRC disabled.		
		01	CRC enabled.		
5	STRICT_REGISTER_ACCESS		Access Mode to Multibyte Registers. This bit is read only. Register write transactions to multibyte registers must include data for each of its individual bytes for the register to be updated. Failure	0x1	R

Table 31. Bit Descriptions for INTERFACE\_CONFIG\_C (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
			to write data to the entire multibyte register (entity) results in the register contents not being updated in memory, and the PARTIAL_REGISTER_ACCESS flag in the INTERFACE_STATUS_A register being set.		
		1	Strict access mode. Multibyte registers require all bytes to be read/ written in full to avoid the PARTIAL_REGISTER_ACCESS bit being flagged.		
[4:2]	RESERVED		Reserved.	0x0	R
[1:0]	CRC_ENABLE_B		Inverted CRC Enable. This field must be written with the complementary value of the CRC_ENABLE field.	0x3	R/W
		11	CRC disabled.		
		10	CRC enabled.		

### Interface Status A Register

### Address: 0x11, Reset: 0x00, Name: INTERFACE\_STATUS\_A

This register flags several error conditions related to SPI communication and register addressing.



Bits	Bit Name	Settings	Description	Reset	Access
7	INTERFACE_NOT_READY		Interface Not Ready Error Flag. Indicates if the device interface was not ready for a transaction when an SPI read or write transaction was requested by the digital host (master). This flag bit is set if an SPI frame begins before the device is ready after a power-on reset. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit).	0x0	R/W1C
		0	Interface not ready error not detected.		
		1	Interface not ready error detected.		
6	RESERVED		Reserved.	0x0	R
5	CLOCK_COUNTING_ERROR		Clock Count Error Flag. Indicates if the incorrect number of serial clock edges was detected in an SPI read or write transaction (for example, if the transaction was terminated in the middle of a byte). This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit).	0x0	R/W1C

#### Table 32. Bit Descriptions for INTERFACE\_STATUS\_A

Table 32. Bit Descriptions for INTERFACE\_STATUS\_A (Continued)

Bits	Bits Bit Name		Description	Reset	Access
		0	Clock count error not detected.		
		1	Clock count error detected.		
4	RESERVED		Reserved.	0x0	R
3	INVALID_OR_NO_CRC	0	Invalid CRC or No CRC Received. This is set when the master fails to send a CRC or when the device calculates and checks the CRC and finds its value is incorrect. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit). CRC error not detected. CRC error detected.	0x0	R/W1C
2	WRITE_TO_READ_ONLY_REGISTER	0	Write to Read-Only Register Attempted. This bit indicates if the digital host attempts an SPI write to a register that contains exclusively read only fields. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit). No error. Write to read-only register detected.	0x0	R/W1C
1	PARTIAL_REGISTER_ACCESS	0	Partial Register Access Error Flag. This bit is asserted when there are not enough bytes of data in a transaction addressed to a multibyte register. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit). Partial access error not detected. Partial access error detected.	0x0	R/W1C
0	REGISTER_ADDRESS_INVALID	0	Register Invalid Address Error Flag. Indicates if an SPI read or write transaction was attempted on an invalid register address. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit). Invalid address error not detected. Invalid address error detected.	0x0	R/W1C

### Interface Configuration D Register

### Address: 0x14, Reset: 0x04, Name: INTERFACE\_CONFIG\_D

This register contains miscellaneous configuration bits affecting SPI communication and electrical parameters of digital signals.





Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R

Table 33. Bit Descriptions for INTERFACE\_CONFIG\_D (Continued)

Bits Bit Name		Settings	Description		Access
6	ALERT_ENABLE_PULLUP		ALERT Pin Control. Enable internal 2.5 k $\Omega$ pull-up resistor.	0x0	R/W
		0	Internal pull-up disabled. An external pull-up is required.		
		1	Internal pull-up enabled.		
5	RESERVED		Reserved.	0x0	R
4	MEM_CRC_EN		Memory CRC Enable. This bit controls the continuous checking of the primary register set and the ROM memory.	0x0	R/W
		0	Memory CRC checking disabled.		
		1	Memory CRC checking enabled.		
[3:2]	SDIO_DRIVE_STRENGTH		SDIO Drive Strength. These two bits allow for the increase in SDIO drive strength.	0x1	R/W
		00	Low SDIO drive strength.		
		01	Medium low SDIO drive strength.		
		10	Medium high SDIO drive strength.		
		11	High SDIO drive strength.		
1	RESERVED		Reserved.	0x0	R
0	SPI_CONFIG_DDR		SPI Configuration DDR. This bit controls the use of DDR for data transfers.	0x0	R/W
		0	DDR mode disabled.		
		1	DDR mode enabled.		

## DAC REGISTER DETAILS

### **Reference Configuration Register**

### Address: 0x15, Reset: 0x00, Name: REFERENCE\_CONFIG

This register controls the source and driving of the voltage reference.



#### Table 34. Bit Descriptions for REFERENCE\_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	IDUMP_FASTMODE		$I_{\text{DUMP}}$ Buffer Fast Mode. Set this bit to increase the $I_{\text{DD}}$ of the $I_{\text{DUMP}}$ buffer of the amplifier to allow for a greater gain bandwidth.	0x0	R/W
[5:2]	RESERVED		Reserved.	0x0	R
[1:0]	REFERENCE_VOLTAGE_SEL		Reference Voltage Selection. These two bits are used to select the configuration of the reference voltage circuit.	0x0	R/W
		00	Reference voltage generated internally. The $V_{\text{REF}}$ pin is floating.		
		01	Reference voltage generated internally and output on the $V_{REF}$ pin.		
		10	Reference voltage provided externally and input on the $V_{REF}$ pin.		
		11	Reference voltage provided externally and input on the $V_{REF}$ pin.		

#### **Error Alarm Mask Register**

#### Address: 0x16, Reset: 0x00, Name: ERR\_ALARM\_MASK

This register selects which error conditions cause the assertion of the ALERT pin.



#### Table 35. Bit Descriptions for ERR ALARM MASK

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R

Table 35. Bit Descriptions for ERR\_ALARM\_MASK (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
6	REF_RANGE_ALARM_MASK		Reference Alarm Mask. When set, the user can ignore alarms due to the reference dipping below 2 V.	0x0	R/W
5	CLOCK_COUNT_ERR_ALARM_MASK		Clock Count Error Alarm Mask. When set, the user can ignore alarms due to an insufficient number of clock periods for a user write.	0x0	R/W
4	MEM_CRC_ERR_ALARM_MASK		Memory CRC Error Alarm Mask. When set, the user can ignore alarms due to a memory CRC error.	0x0	R/W
3	SPI_CRC_ERR_ALARM_MASK		SPI CRC Error Alarm Mask. When set, the user can ignore alarms due to the SPI CRC checker.	0x0	R/W
2	WRITE_TO_READ_ONLY_ALARM_MASK		Write to Read-Only Alarm Mask. When set, the user can ignore alarms due to the user writing to a read-only register.	0x0	R/W
1	PARTIAL_REGISTER_ACCESS_ALARM_MASK		Partial Register Access Alarm Mask. When set, the user can ignore alarms due to the user not completing the write to a register.	0x0	R/W
0	REGISTER_ADDRESS_INVALID_ALARM_MASK		Register Address Invalid Alarm Mask. When set, the user can ignore alarms due to the user writing to an invalid register address.	0x0	R/W

### **Error Status Register**

#### Address: 0x17, Reset: 0x01, Name: ERR\_STATUS

This register signals a combination of errors in the analog and digital domains. All the bits are sticky and can be cleared by writing 1.



#### Table 36. Bit Descriptions for ERR\_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	REF_RANGE_ERR_STATUS		Reference Alarm Error Status. This bit indicates an alarm if the reference dips below 2 V.	0x0	R/W1C
5	DUAL_SPI_STREAM_EXCEEDS_DAC_ERR_STATUS		Dual SPI Exceeds DAC Memory Map During Streaming. This bit indicates an alarm when in dual SPI and streaming access goes beyond the DAC memory map.	0x0	R/W1C
4	MEM_CRC_ERR_STATUS		Memory Map Background CRC Error. This bit indicates an alarm when the background CRC detects	0x0	R/W1C

#### Table 36. Bit Descriptions for ERR\_STATUS (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
			bit corruption within the memory		
			map.		
[3:1]	RESERVED		Reserved.	0x0	R
0	RESET_STATUS		Reset Occurred. This bit indicates that the device has just completed initialization following a reset. This bit asserts the ALERT pin and it is nonmaskable. Therefore, it must be cleared right after initialization.	0x1	R/W1C

### **Power-Down Configuration Register**

#### Address: 0x18, Reset: 0x00, Name: POWERDOWN\_CONFIG

This register controls the individual power-down of the DAC channels.



#### Table 37. Bit Descriptions for POWERDOWN\_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	CH0_DAC_POWERDOWN		Channel 0 DAC Power-Down.	0x0	R/W
		0	Channel 0 DAC in normal operating mode.		
		1	Channel 0 DAC is in power-down mode.		
[3:1]	RESERVED		Reserved.	0x0	R
0	CH0_CHANNEL_POWERDOWN		Channel 0 Output Amplifier Power-Down.	0x0	R/W
		0	Channel 0 output amplifier is powered on.		
		1	Channel 0 output amplifier is in power-down mode.		

#### **Output Range Register**

#### Address: 0x19, Reset: 0x00, Name: CH0\_OUTPUT\_RANGE

This register sets the output range of the DAC channels to one of the preconfigured ranges listed in Table 8. In addition to setting this register, the corresponding R<sub>FBx 0</sub> resistor must be connected to obtain the expected result.



#### Table 38. Bit Descriptions for CH0\_OUTPUT\_RANGE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R

Table 38. Bit Descriptions for CH0\_OUTPUT\_RANGE (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	CH0_OUTPUT_RANGE_SEL		Channel 0 Output Range Select. The user can select which voltage output range is desired.	0x0	R/W
		000	0 V to 2.5 V range. Requires R <sub>FB1_0</sub> connection.		
		001	0 V to 5 V range. Requires R <sub>FB1_0</sub> connection.		
		010	0 V to 10 V range. Requires R <sub>FB2_0</sub> connection.		
		011	−5 V to +5 V range. Requires R <sub>FB2_0</sub> connection.		
		100	-2.5 V to +7.5 V range. Requires R <sub>FB2 0</sub> connection.		

### Hardware LDAC Mask Register, Fast Mode

### Address: 0x28, Reset: 0x00, Name: HW\_LDAC\_16B

This register controls the masking of the external LDAC signal to latch data into the DAC register.



#### Table 39. Bit Descriptions for HW\_LDAC\_16B

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	HW_LDAC_MASK_CH0		Hardware LDAC Mask for Channel 0. This bit controls the latching of data into the DAC register when the $\overline{\text{LDAC}}$ signal is asserted.	0x0	R/W
		0	Data is latched in DAC Register 0 when the LDAC pin is asserted.		
		1	LDAC signal masked for Channel 0. DAC register is not updated when LDAC is asserted.		

### **DAC Register for Channel 0, Fast Mode**

#### Address: 0x29, Reset: 0x0000, Name: CH0\_DAC\_16B

This register contains the data currently played on DAC Channel 0.



#### Table 40. Bit Descriptions for CH0 DAC 16B

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DAC_DATA0		Channel 0 DAC Data.	0x0	R/W

### DAC Page Register, Fast Mode

### Address: 0x2D, Reset: 0x0000, Name: DAC\_PAGE\_16B

This register is provided for compatibility with multichannel chips of this family.

#### 15 14 13 12 11 10 9 8 7 6 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

[15:0] DAC\_PAGE (R/W) DAC Page Data.

#### Table 41. Bit Descriptions for DAC\_PAGE\_16B

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DAC_PAGE		DAC Page Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register if the SEL_CH0 bit is set in the CH_SELECT_16B register.	0x0	R/W

### Channel Select for Page Registers, Fast Mode

### Address: 0x2F, Reset: 0x00, Name: CH\_SELECT\_16B

This register is provided for compatibility with multichannel chips of this family.



#### Table 42. Bit Descriptions for CH\_SELECT\_16B

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	SEL_CH0		Select Channel 0. When this bit is set, data written to the INPUT_PAGE_16B register is copied to the CH0_INPUT_16B register and data written to the DAC_PAGE_16B register is copied to the CH0_DAC_16B register.	0x0	R/W
		0	No operation.		
		1	Copy to corresponding register in Channel 0.		

#### Input Page Register, Fast Mode

#### Address: 0x30, Reset: 0x0000, Name: INPUT\_PAGE\_16B

This register is provided for compatibility with multichannel chips of this family.



Input Page Data.

#### Table 43. Bit Descriptions for INPUT PAGE 16B

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	INPUT_PAGE		Input Page Data. Following a write to this register, the DAC code loaded into this register is copied into the input register if the SEL_CH0 bit is set in the CH_SELECT_16B register.	0x0	R/W

#### Software LDAC Register, Fast Mode

#### Address: 0x32, Reset: 0x00, Name: SW\_LDAC\_16B

This register is used to trigger a data transfer between the input register and the DAC register. It is the software equivalent of pulsing the LDAC line low.



#### Table 44. Bit Descriptions for SW\_LDAC\_16B

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	SW_LDAC_CH0		Software LDAC for Channel 0. Setting this bit transfers contents from the CH0_INPUT_16B register to the CH0_DAC_16B register. This bit automatically resets after being written.	0x0	W
		0	No operation.		
		1	Load DAC 0.		

#### Input Register for Channel 0, Fast Mode

#### Address: 0x33, Reset: 0x0000, Name: CH0\_INPUT\_16B

This register contains the data to be transferred to the DAC register using one of the various trigger options, hardware LDAC, software LDAC, or automatic transfer.



[15:0] INPUT\_DATA0 (R/W) Channel 0 Input Data.

#### Table 45. Bit Descriptions for CH0 INPUT 16B

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	INPUT_DATA0		Channel 0 Input Data.	0x0	R/W

### Hardware LDAC Mask Register, Precision Mode

#### Address: 0x37, Reset: 0x00, Name: HW\_LDAC\_24B

This register controls the masking of the external <u>LDAC</u> signal to latch data into the DAC register.



#### Table 46. Bit Descriptions for HW LDAC 24B

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	HW_LDAC_MASK_CH0		Hardware LDAC Mask for Channel 0. This bit controls the latching of data into the DAC register when the $\overline{\text{LDAC}}$ signal is asserted.	0x0	R/W
		0	Data is latched in DAC Register 0 when the LDAC pin is asserted.		
		1	LDAC signal masked for Channel 0. DAC register is not updated when LDAC is asserted.		

## DAC Register for Channel 0, Precision Mode

### Address: 0x38, Reset: 0x000000, Name: CH0\_DAC\_24B

This register contains the data currently played on DAC Channel 0.



[23:8] DAC\_DATA0 (R/W) Channel 0 DAC Data.

#### Table 47. Bit Descriptions for CH0\_DAC\_24B

Bits	Bit Name	Settings	Description	Reset	Access
[23:8]	DAC_DATA0		Channel 0 DAC Data.	0x0	R/W
[7:0]	RESERVED		Reserved.	0x0	R

### **DAC Page Register, Precision Mode**

#### Address: 0x3E, Reset: 0x000000, Name: DAC\_PAGE\_24B

This register is provided for compatibility with multichannel chips of this family.



#### Table 48. Bit Descriptions for DAC\_PAGE\_24B

Bits	Bit Name	Settings	Description	Reset	Access
[23:8]	DAC_PAGE		DAC Page Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register if the SEL_CH0 bit is set in the CH_SELECT_24B register.	0x0	R/W
[7:0]	RESERVED		Reserved.	0x0	R

### Channel Select for Page Registers, Precision Mode

#### Address: 0x41, Reset: 0x00, Name: CH\_SELECT\_24B

This register is provided for compatibility with multichannel chips of this family.



#### Table 49. Bit Descriptions for CH\_SELECT\_24B

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	SEL_CH0		Select Channel 0. When this bit is set, data written to the INPUT_PAGE_24B register is copied to the CH0_INPUT_24B register and data written to the DAC_PAGE_24B register is copied to the CH0_DAC_24B register.	0x0	R/W
		0	No operation.		
		1	Copy to corresponding register in Channel 0.		

## Input Page Register, Precision Mode

### Address: 0x42, Reset: 0x000000, Name: INPUT\_PAGE\_24B

This register is provided for compatibility with multichannel chips of this family.



[23:8] INPUT\_PAGE (R/W) Input Page Data.

### Table 50. Bit Descriptions for INPUT\_PAGE\_24B

Bits	Bit Name	Settings	Description	Reset	Access
[23:8]	INPUT_PAGE		Input Page Data. Following a write to this register, the DAC code loaded into this register is copied into the input register if the SEL_CH0 bit is set in the CH_SELECT_24B register.	0x0	R/W
[7:0]	RESERVED		Reserved.	0x0	R

### Software LDAC Register, Precision Mode

### Address: 0x45, Reset: 0x00, Name: SW\_LDAC\_24B

This register is used to trigger a data transfer between the input register and the DAC register. It is the software equivalent of pulsing the LDAC line low.



#### Table 51. Bit Descriptions for SW\_LDAC\_24B

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	SW_LDAC_CH0		Software LDAC for Channel 0. Setting this bit transfers contents from the CH0_INPUT_24B register to the CH0_DAC_24B register. This bit automatically resets after being written.	0x0	W
		0	No operation.		
		1	Load DAC 0.		

### Input Register for Channel 0, Precision Mode

#### Address: 0x46, Reset: 0x000000, Name: CH0\_INPUT\_24B

This register contains the data to be transferred to the DAC register using one of the various trigger options, hardware LDAC, software LDAC, or automatic transfer.



#### Table 52. Bit Descriptions for CH0 INPUT 24B

Bits	Bit Name	Settings	Description	Reset	Access
[23:8]	INPUT_DATA0		Channel 0 Input Data.	0x0	R/W
[7:0]	RESERVED		Reserved.	0x0	R

### **APPLICATIONS INFORMATION**

## POWER SUPPLY RECOMMENDATIONS

The AD3541R does not have any restriction for power supply sequencing. The chip incorporates a power monitor for AV<sub>DD</sub> and DV<sub>DD</sub> that releases the internal reset when both rails are within specification. Nevertheless, the recommended sequence to turn on the supply rails is GND, AV<sub>DD</sub>, DV<sub>DD</sub>, V<sub>LOGIC</sub> because it minimizes the power-up glitch. PV<sub>DD</sub> and PV<sub>SS</sub> are independent of the three previous supplies and can be switched on at any time. A small glitch (<100 mV) appears when PV<sub>DD</sub> reaches 2 V.

It is recommended to connect AGND and DGND together and have a single solid ground plane.

 $AV_{DD}$  has a constant power consumption that is independent of the update rate. The main caution for this rail is ensuring that noise level is low in the high frequencies, where AC PSRR is lower.

 $\rm DV_{\rm DD}$  has a variable power consumption that depends on the update rate and the SPI bus mode. Dynamic current has fast variations that cause the rail to be noisy. If  $\rm DV_{\rm DD}$  is derived from AV\_{\rm DD}, a filter is recommended in addition to the LDO to completely remove the effect on the DAC output.

 $V_{\text{LOGIC}}$  has very low current demand that depends on the SPI bus mode and clock rate. Power consumption is maximum in readout operations in dual SPI mode.

The recommended decoupling for the supply rails and the analog lines is shown in Figure 96.



Figure 96. Recommended Application Circuit

The decoupling capacitors on  $CV_{REF}$  can be adjusted to achieve the desired trade-off between noise corner frequency and power-up glitch amplitude.

The  $C_{FB0}$  and  $C_{FB1}$  capacitors are used to adjust the bandwidth of the internal TIA to achieve the optimal step response with the minimum overshoot.

Use capacitors with NP0 dielectric for the feedback capacitors and any other capacitors on the path of the output voltage to avoid the derating caused by low frequency voltage variations. The decoupling capacitors for the supply rails and  $CV_{REF}$  can use materials with high dielectric constant because the voltage on these lines is constant.

## LAYOUT GUIDELINES

The pin configuration of the AD3541R, shown in Figure 9, is arranged in a way that facilitates the layout of the EVAL-AD3542R. Note that the EVAL-AD3542R can be used to evaluate the AD3541R. Most digital high speed lines are located on one side of the chip, with the analog functions of the DAC distributed along the other three sides. This arrangement allows routing the digital lines straight away from the analog functions, leaving space for analog parts to be placed around the other three sides, as shown in Figure 97.



Figure 97. EVAL-AD3542R Component Arrangement and Layout

The following list is a few recommendations to observe to obtain the best performance:

- Keep the C<sub>FB</sub>x capacitors close to the AD3541R with short traces to minimize noise pickup because it is connected to a high impedance node internally.
- Keep switching regulators and fast dV/dt signals away from the feedback loops of the DAC. Any μA induced on these lines becomes a mV at the output of the DAC.
- Do not overlap analog and digital signals. If a crossing cannot be avoided, it must be done at 45° or 90°.
- ▶ Route digital lines using traces with a constant characteristic impedance to avoid signal integrity problems that result in timing violations in DDR mode and crosstalk between signals. The traces must have a continuous ground plane in an adjacent layer. When changing layers, ensure that the destination layer is referred to another ground plane and the traces have the same characteristic impedance. Place a via connecting both ground planes near the via of the digital line. If the destination layer is referred to a power plane, it must be continuous along the path of the line and a decoupling capacitor between power and ground must be placed close to the via of the digital line.

### **OUTLINE DIMENSIONS**



Figure 98. 28-Lead Lead Frame Chip Package [LFCSP] 4 mm × 4 mm Body and 0.95 mm Package Height (CP-28-15) Dimensions shown in millimeters

Updated: May 05, 2023

### **ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
AD3541RBCPZ12-RL7	-40°C to +105°C	28-Lead LFCSP (4mm x 4mm x 0.95 mm)	Reel, 1500	CP-28-15
AD3541RBCPZ16-RL7	-40°C to +105°C	28-Lead LFCSP (4mm x 4mm x 0.95 mm)	Reel, 1500	CP-28-15

<sup>1</sup> Z = RoHS Compliant Part.

### **EVALUATION BOARDS**

Model <sup>12</sup>	Description
EVAL-AD3542RFMCZ	AD3542R Evaluation Board
EVAL-SDP-CH1Z	SDP High Speed Controller Board

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> The EVAL-AD3542RFMCZ can be used to evaluate AD3541R.



# **Mouser Electronics**

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD3541RBCPZ16-RL7 AD3541RBCPZ12-RL7