ANALOG DEVICES

2 ×10 W Filterless Class-D Stereo Audio Amplifier

Data Sheet

SSM3302

FEATURES

Filterless stereo Class-D amplifier with Σ-Δ modulation
2 × 10 W into 4 Ω load and 2 × 8 W into 8 Ω load at 12 V supply with <1% total harmonic distortion plus noise (THD + N)
91% efficiency at 12 V, 8 W into 8 Ω speaker
98 dB signal-to-noise ratio (SNR)
Single-supply operation from 7 V to 18 V
Flexible gain adjustment pin from 9 dB to 24 dB
Fixed input impedance of 40 kΩ
Mono output mode pin for 1 × 20 W output power into 2 Ω
10 μA shutdown current
Short-circuit and thermal protection
Available in a 40-lead, 6 mm × 6 mm LFCSP
Pop-and-click suppression
User-selectable ultralow EMI emissions mode
Thermal warning indicator
Power-on reset

APPLICATIONS

Mobile computing
Flat panel televisions
Media docking stations
Portable electronics
Sound bars

GENERAL DESCRIPTION

The SSM3302 is a fully integrated, high efficiency, stereo Class-D audio amplifier. The application circuit requires minimal external components and operates from a single 7 V to 18 V supply. The device is capable of delivering 2 × 10 W of continuous output power into a 4 Ω load (or 2 × 8 W into 8 Ω) with <1% THD + N from a 12 V supply. In addition, while mono mode is activated, the user can drive a load as small as 2 Ω up to 20 W continuous output power by stacking the stereo output terminals.

The SSM3302 features a high efficiency, low noise modulation scheme that requires no external LC output filters. This scheme continues to provide high efficiency even at low output power. The SSM3302 operates with 90% efficiency at 7 W into an 8 Ω load or with 82% efficiency at 10 W into 4 Ω from a 12 V supply, and it has an SNR of >98 dB.

Spread spectrum pulse density modulation (PDM) is used to provide lower EMI radiated emissions compared with other Class-D architectures. The SSM3302 includes an optional modulation select pin (ultralow EMI emission mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. The SSM3302 can pass FCC Class-B emissions testing with an unshielded 20 inch cable using common-mode choke-based filtering.

The fully differential input of the SSM3302 provides excellent rejection of common-mode noise on the input. The device also includes a highly flexible gain select pin that only requires one series resistor to choose a gain between 9 dB and 24 dB, with no change to the input impedance. The benefit of this is to improve gain matching between multiple SSM3302 devices within a single application compared with using external resistors to set gain.

The SSM3302 includes an integrated voltage regulator that generates a 5 V rail.

The SSM3302 has a micropower shutdown mode with a typical shutdown current of 10 μA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin. The device also includes pop-and-click suppression circuitry that minimizes voltage glitches at the output during turn on and turn off, reducing audible noise during activation and deactivation.

Other included features to simplify system level integration of the SSM3302 are input low-pass filtering to suppress out-of-band DAC noise interference to the pulse density modulator, fixed input impedance to simplify component selection across multiple platform production builds, and a thermal warning indicator pin.

The SSM3302 is specified over the commercial temperature range (−40°C to +85°C). It has built-in thermal shutdown and output short-circuit protection. It is available in a halide-free, 40-lead, 6 mm × 6 mm lead frame chip scale package (LFCSP).

Rev. A Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

5/13—Rev. 0 to Rev. A

Changed Voltage Rating from 6.3 V to 35 V in Bootstrap Capacitors Section ... 17

2/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

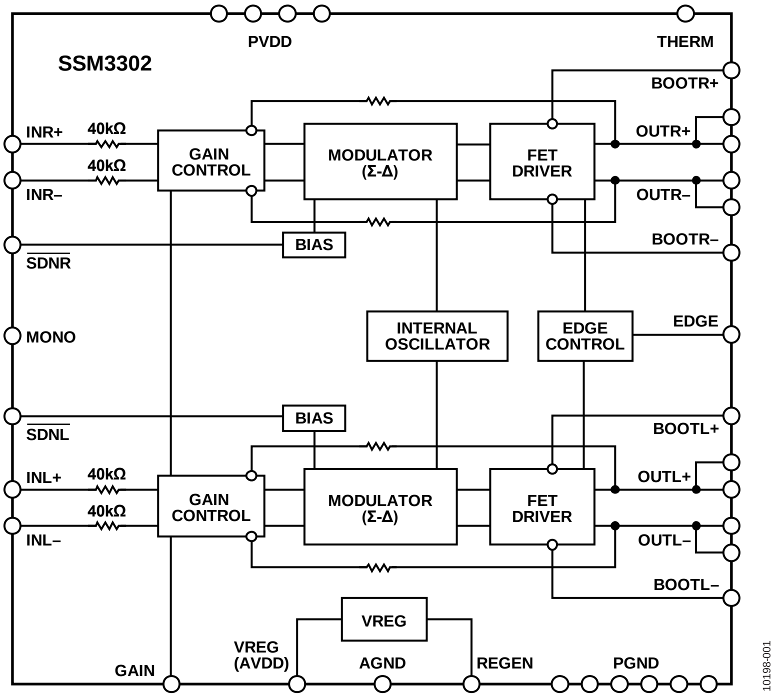


Figure 1.

SPECIFICATIONS

PVDD = 12 V, T_A = 25°C, R_L = 8 Ω + 64 μH, EDGE = AGND, gain = 9 dB, VREG = off, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power/Channel	P_O	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		12[1]		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		8		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		2.7		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		15[1]		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		10		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		3.2		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		20[1]		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		13[1]		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		4.8		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 15 V		24[1]		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 12 V		16[1]		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 7 V		5.7		W
		R_L = 2 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 12 V (mono mode)		29[2]		W
		R_L = 2 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, PVDD = 7 V (mono mode)		9.4[2]		W
		R_L = 2 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 12 V (mono mode)		36.6[2]		W
		R_L = 2 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, PVDD = 7 V (mono mode)		12.7[2]		W
Efficiency	η	P_O = 7 W, 8 Ω, PVDD = 12 V, EDGE = low (normal operation)		91.5		%
		P_O = 7 W, 8 Ω, PVDD = 12 V, EDGE = AVDD (ultralow EMI mode)		82		%
Total Harmonic Distortion + Noise	THD + N	P_O = 5 W into 8 Ω, f = 1 kHz, PVDD = 12 V		0.01		%
Input Common-Mode Voltage Range	V_{CM}		1.0		AVDD – 1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 2.5 V ± 100 mV at 1 kHz, output referred		43		dB
Channel Separation	X_{TALK}	P_O = 0.5 W, f = 1 kHz		80		dB
Average Switching Frequency	f_{SW}			300		kHz
Differential Output Offset Voltage	V_{OOS}	Gain = 9 dB			3.0	mV
POWER SUPPLY						
Supply Voltage Range	PVDD	Guaranteed from PSRR test	7		18	V
Power Supply Rejection Ratio	$PSRR_{DC}$	PVDD = 7 V to 15 V, dc input floating		70		dB
	$PSRR_{AC}$	V_{RIPPLE} = 100 mV at 1 kHz, inputs are ac grounded, C_{IN} = 0.1 μF		80		dB
Supply Current (Stereo)	I_{SYPVDD}	V_{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 15 V, V_{REGEN} = AVDD (internal V_{REG} active)		12.2		mA
		V_{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 15 V, V_{REGEN} = AGND (internal V_{REG} disabled)		6.2		mA
		V_{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 12 V, V_{REGEN} = AGND (internal V_{REG} disabled)		5		mA
		V_{IN} = 0 V, load = 8 Ω + 68 μH, PVDD = 7 V, V_{REGEN} = AGND (internal V_{REG} disabled)		3		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
	I_{SYAVDD}	V_{IN} = 0 V, load = 8 Ω + 68 µH, PVDD = 15 V, V_{REGEN} = AGND (internal V_{REG} disabled)		5.85		mA
		V_{IN} = 0 V, load = 8 Ω + 68 µH, PVDD = 12 V, V_{REGEN} = AGND (internal V_{REG} disabled)		5.8		mA
		V_{IN} = 0 V, load = 8 Ω + 68 µH, PVDD = 7 V, V_{REGEN} = AGND (internal V_{REG} disabled)		5.6		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = AGND		10		µA
ANALOG SUPPLY						
External Supply Voltage	AVDD	Permissible range for external AVDD, V_{REGEN} = AGND	4.5		5.5	V
On-Board Regulator	V_{VREG}			5		V
Regulator Current	I_{VREG}			20		mA
Regulator Power Supply Rejection	$PSRR_{VREG}$			70		dB
GAIN CONTROL						
Closed-Loop Voltage Gain	A_V	See Table 5 for gain options	9		24	dB
Input Impedance	Z_{IN}			40		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}		1.35			V
Input Voltage Low	V_{IL}				0.35	V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from AGND to AVDD		40		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from AVDD to AGND		500		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		56		kΩ
AMPLIFIER PROTECTION						
Overcurrent Threshold	I_{OC}			6		A
Overtemperature Warning	T_{WARN}			120		°C
Overtemperature Shutdown	T_{SD}			145		°C
Recovery Temperature	T_{REC}			85		°C
NOISE PERFORMANCE						
Output Voltage Noise	e_n	PVDD = 12 V, f = 20 Hz to 20 kHz, inputs are ac grounded, gain = 9 dB, A-weighted		100		µV rms
Signal-to-Noise Ratio	SNR	P_O = 10 W, R_L = 8 Ω		98		dB

[1] Although the SSM3302 has good audio quality above 2 × 10 W into 4 Ω, continuous output power beyond 2 × 10 W into 4 Ω must be avoided due to device packaging limitations.
[2] Mono mode. Output power beyond 20 W needs special care for thermally considered printed circuit board (PCB) design.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Power Supply Voltage (PVDD)	−0.3 V to +25 V
Analog Supply Voltage (AVDD)	−0.3 V to +6 V
Input Voltage	−0.3 V to +6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

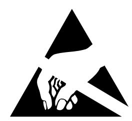
THERMAL RESISTANCE

θ_{JA} (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JA} and θ_{JC} are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling.

Table 3. Thermal Resistance

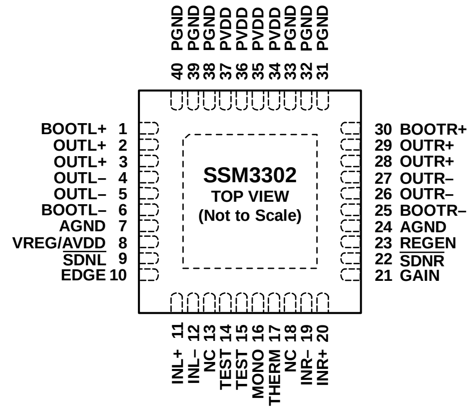
Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead, 6 mm × 6 mm LFCSP	31	2.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. USE MULTIPLE VIAS TO CONNECT THE EXPOSED PAD TO THE GROUND PLANE.
2. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10198-002

Figure 2. Pin Configuration (Top Side View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BOOTL+	Bootstrap Input/Output for Left Channel, Noninverting Output.
2, 3	OUTL+	Noninverting Output for Left Channel.
4, 5	OUTL−	Inverting Output for Left Channel.
6	BOOTL−	Bootstrap Input/Output for Left Channel, Inverting Output.
7	AGND	Analog Ground.
8	VREG/AVDD	5 V Regulator Output (if REGEN = high)/AVDD Input (if REGEN = low).
9	$\overline{\text{SDNL}}$	Shutdown, Left Channel. Active low digital input.
10	EDGE	Edge Control (Low Emission Mode). Active high digital input.
11	INL+	Noninverting Input for Left Channel.
12	INL−	Inverting Input for Left Channel.
13, 18	NC	This pin is not connected internally (see Figure 2).
14, 15	TEST	Test Pins. Tie to AGND.
16	MONO	Mono Output Mode Enable.
17	THERM	Overtemperature Warning (Open Collector).
19	INR−	Inverting Input for Right Channel.
20	INR+	Noninverting Input for Right Channel.
21	GAIN	Gain Select from 9 dB to 24 dB.
22	$\overline{\text{SDNR}}$	Shutdown, Right Channel. Active low digital input.
23	REGEN	5 V Regulator Enable, Active High.
24	AGND	Analog Ground.
25	BOOTR−	Bootstrap Input/Output for Right Channel, Inverting Output.
26, 27	OUTR−	Inverting Output for Right Channel.
28, 29	OUTR+	Noninverting Output for Right Channel.
30	BOOTR+	Bootstrap Input/Output for Right Channel, Noninverting Output.
31, 32, 33, 38, 39, 40	PGND	Power Stage Ground.
34, 35, 36, 37	PVDD	Power Stage Power Supply.
	Exposed Pad	Thermal Exposed Pad. Use multiple vias to connect this pad to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise stated, all data at PVDD = 12 V, EDGE = low, MONO = low, REGEN = high, and GAIN = 9 dB.

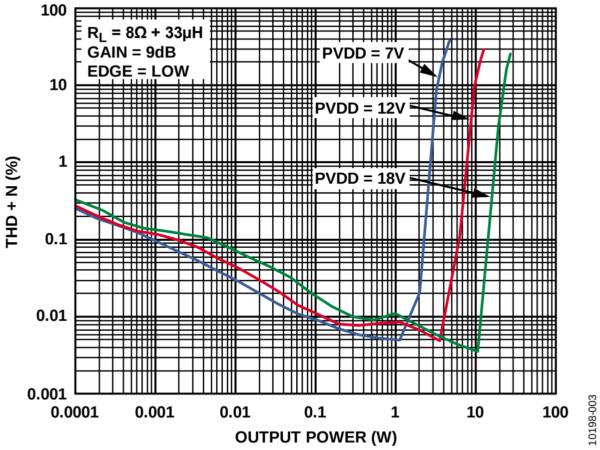


Figure 3. THD + N vs. Output Power into 8 Ω; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

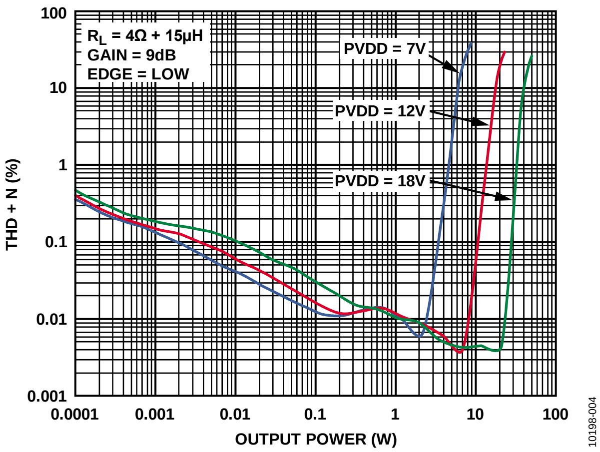


Figure 4. THD + N vs. Output Power into 4 Ω; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

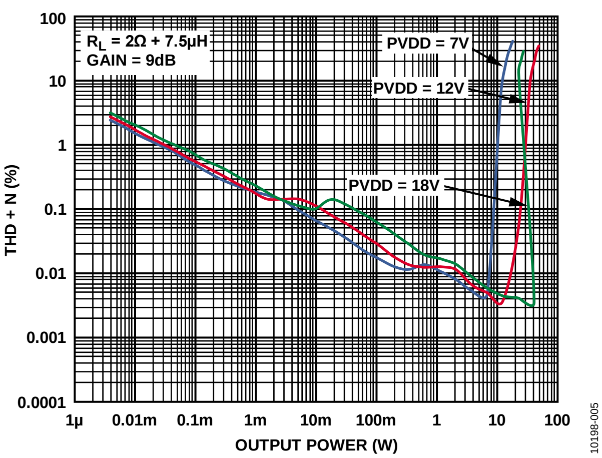


Figure 5. THD + N vs. Output Power into 2 Ω; Mono Mode; Gain = 9 dB; PVDD = 7 V, PVDD = 12 V, 1 PVDD = 8 V

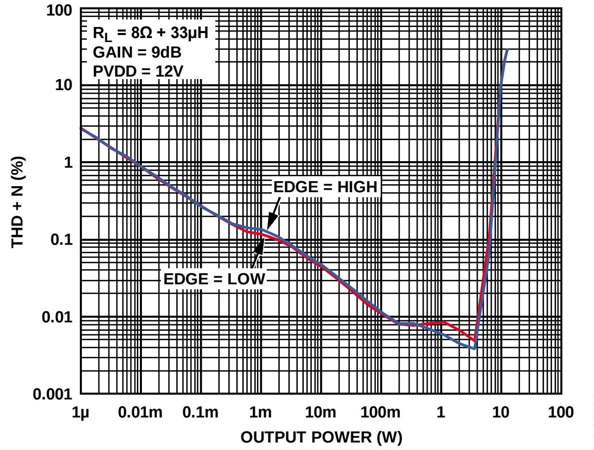


Figure 6. THD + N vs. Output Power into 8 Ω; EDGE = High, EDGE = Low

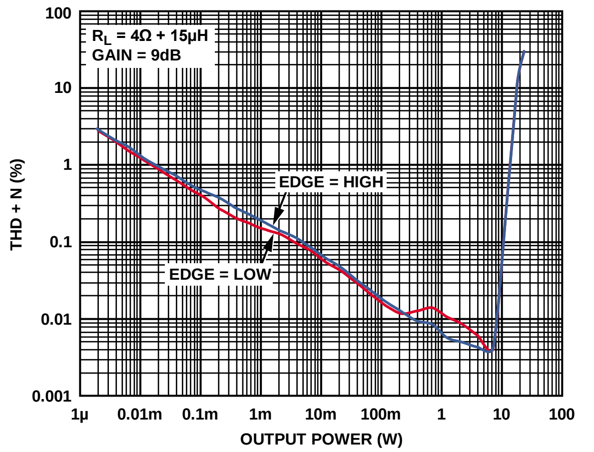


Figure 7. THD + N vs. Output Power into 4 Ω; EDGE = High, EDGE = Low

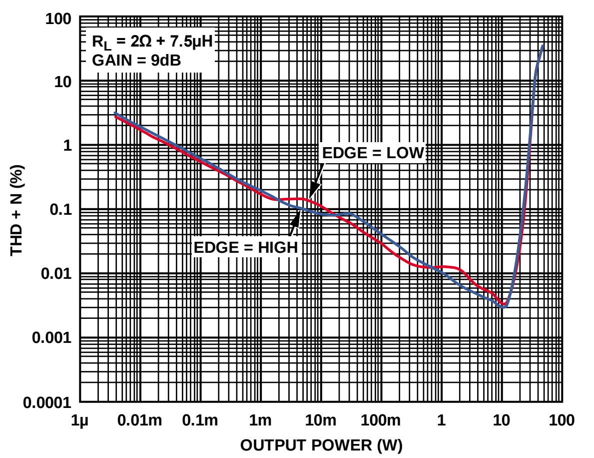


Figure 8. THD + N vs. Output Power into 2 Ω; EDGE = High, EDGE = Low

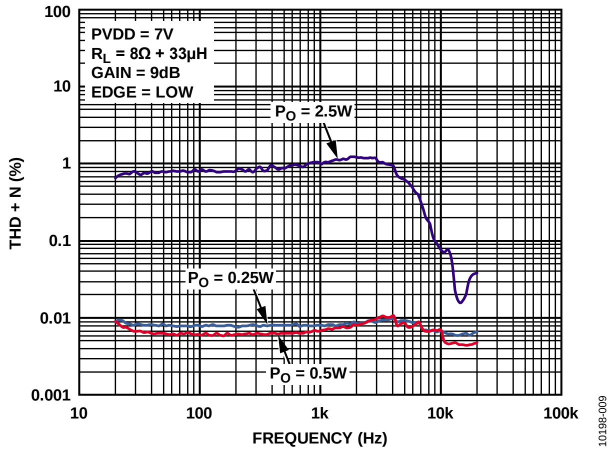


Figure 9. THD + N vs. Frequency;
R_L = 8 Ω; PVDD = 7 V; P_O = 0.25 W, P_O = 0.5 W, P_O = 2.5 W

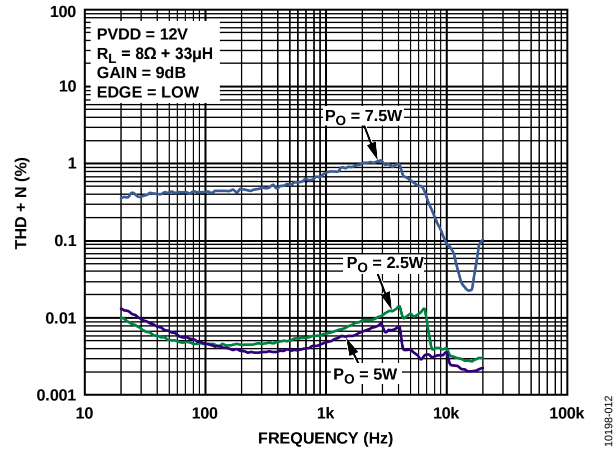


Figure 12. THD + N vs. Frequency;
R_L = 8 Ω; PVDD = 12 V; P_O = 2.5 W, P_O = 5 W, P_O = 7.5 W

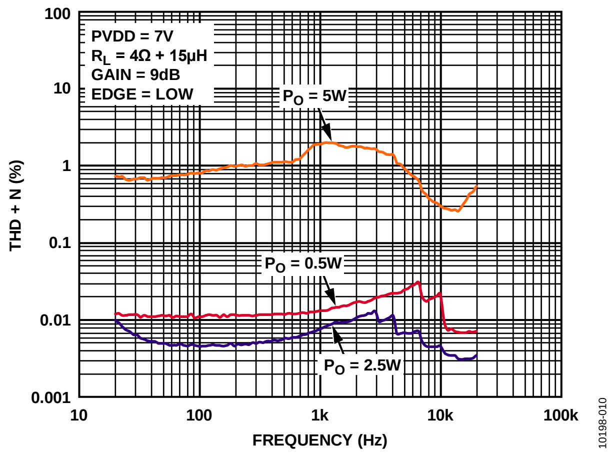


Figure 10. THD + N vs. Frequency;
R_L = 4 Ω; PVDD = 7 V; P_O = 0.5 W, P_O = 2.5 W, P_O = 5 W

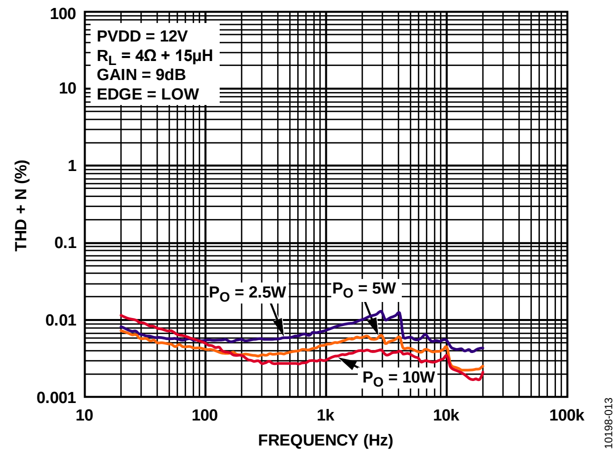


Figure 13. THD + N vs. Frequency;
R_L = 4 Ω; PVDD = 12 V; P_O = 2.5 W, P_O = 5 W, P_O = 10 W

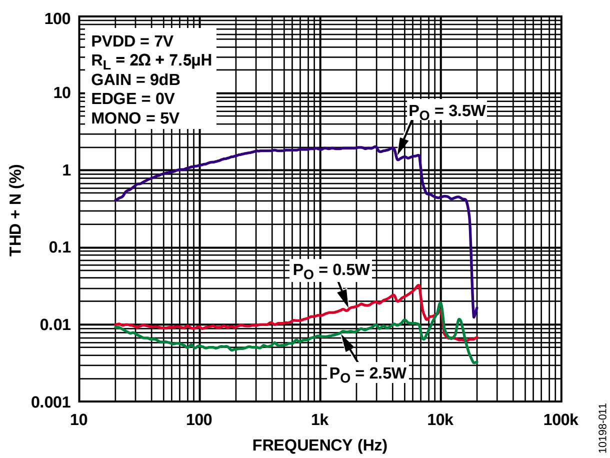


Figure 11. THD + N vs. Frequency;
R_L = 2 Ω; Mono Mode; PVDD = 7 V; P_O = 0.5 W, P_O = 2.5 W, P_O = 3.5 W

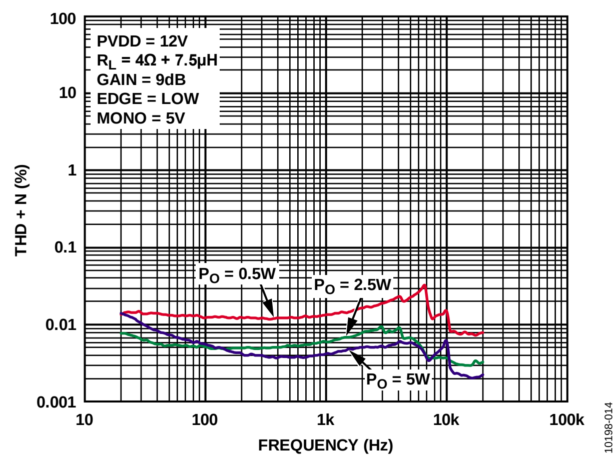


Figure 14. THD + N vs. Frequency;
R_L = 2 Ω; Mono Mode; PVDD = 12 V; P_O = 0.5 W, P_O = 2.5 W, P_O = 5 W

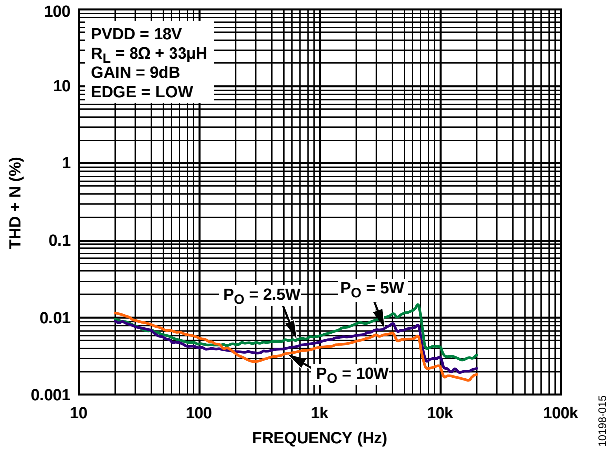


Figure 15. THD + N vs. Frequency;
R_L = 8 Ω; PVDD = 18 V; P_O = 2.5 W, P_O = 5 W, P_O = 10 W

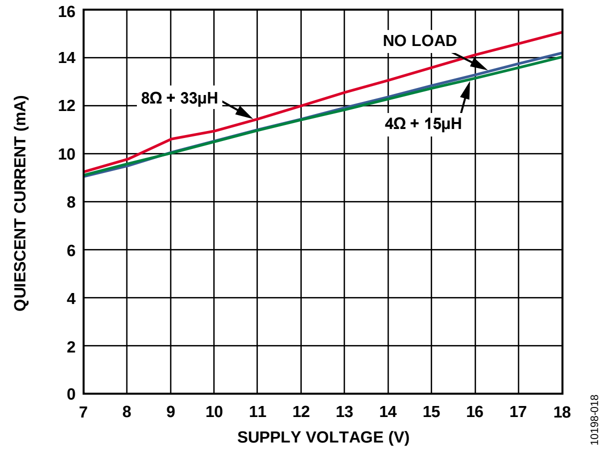


Figure 18. Quiescent Current vs. Supply Voltage,
R_L = 8 Ω + 33 µH, No Load, , R_L = 4 Ω + 15 µH

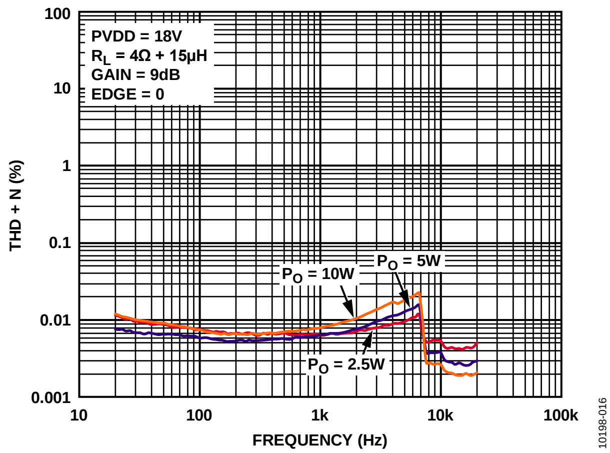


Figure 16. THD + N vs. Frequency;
R_L = 4 Ω; PVDD = 18 V; P_O = 2.5 W, P_O = 5 W, P_O = 10 W

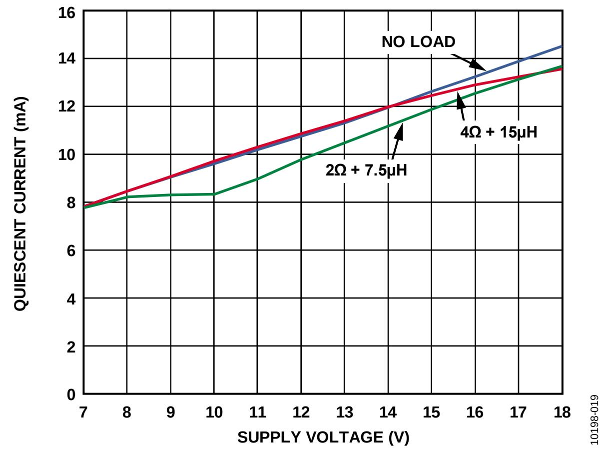


Figure 19. Quiescent Current vs. Supply Voltage,
Mono Mode, No Load, R_L = 4 Ω + 15 µH, R_L = 2 Ω + 7.5 µH

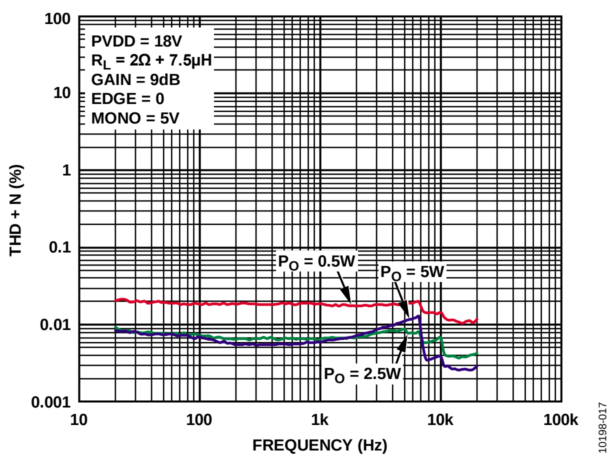


Figure 17. THD + N vs. Frequency;
R_L = 2 Ω; Mono Mode; PVDD = 18 V; P_O = 0.5 W, P_O = 2.5 W, P_O = 5 W

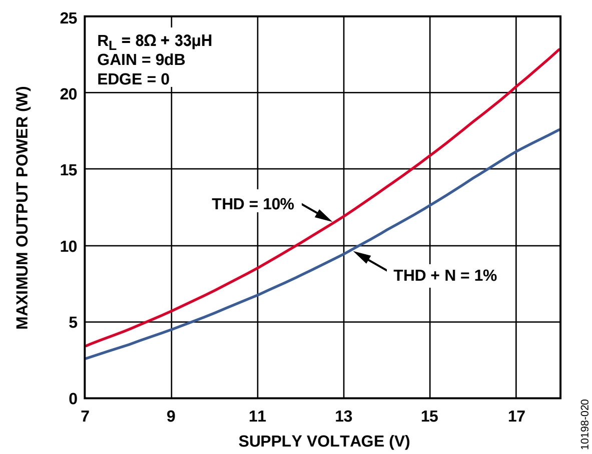


Figure 20. Maximum Output Power vs. Supply Voltage;
R_L = 8 Ω; THD + N = 1%, THD + N = 10%

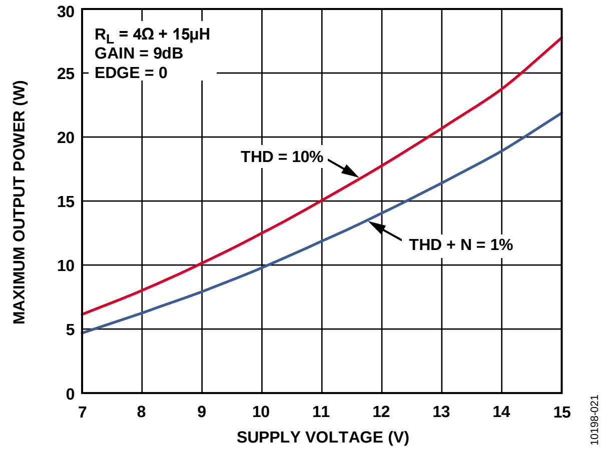


Figure 21. Maximum Output Power vs. Supply Voltage; R_L = 4 Ω; THD + N = 1%, THD + N = 10%

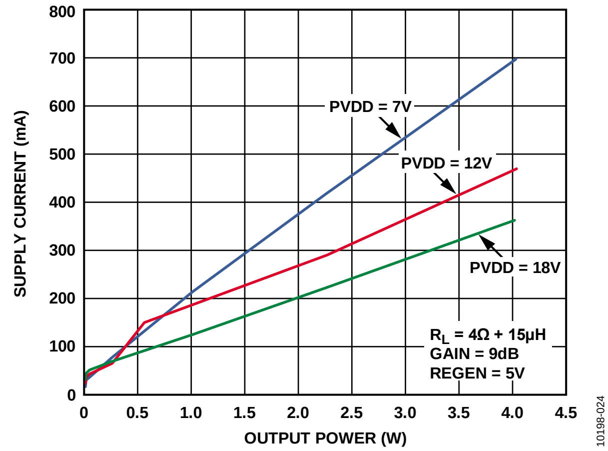


Figure 24. Supply Current vs. Output Power into 4 Ω; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

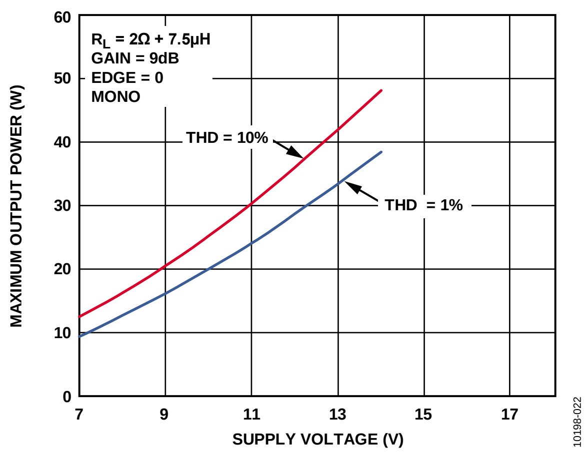


Figure 22. Maximum Output Power vs. Supply Voltage; R_L = 2 Ω; Mono Mode; THD + N = 1%, THD + N = 10%

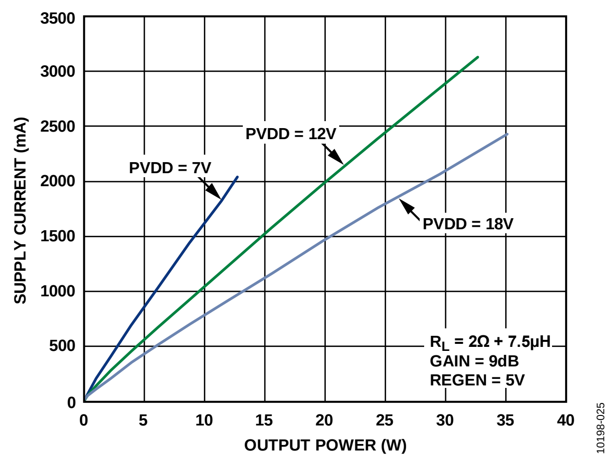


Figure 25. Supply Current vs. Output Power into 2 Ω; Mono Mode; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

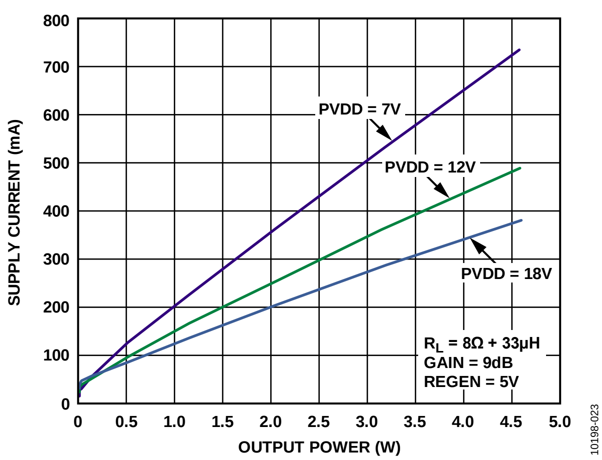


Figure 23. Supply Current vs. Output Power into 8 Ω; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

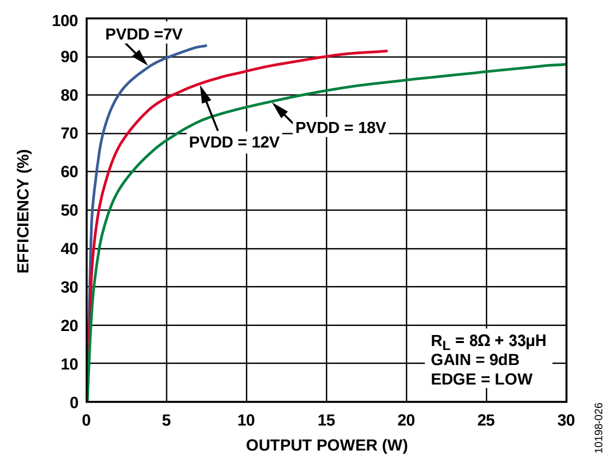


Figure 26. Efficiency vs. Output Power into 8 Ω; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

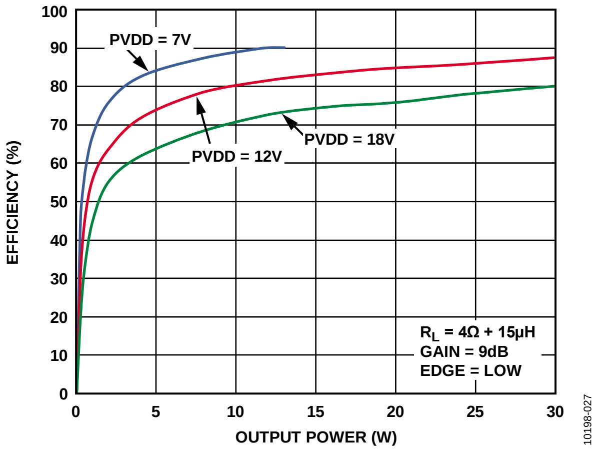


Figure 27. Efficiency vs. Output Power into 4 Ω; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

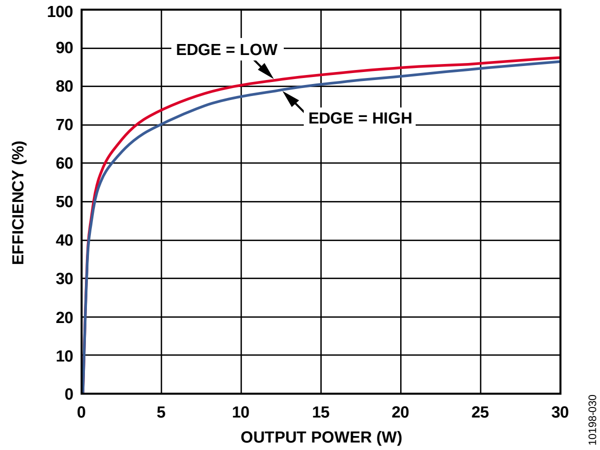


Figure 30. Efficiency vs. Output Power into 4 Ω; PVDD = 12 V; EDGE = High, EDGE = Low

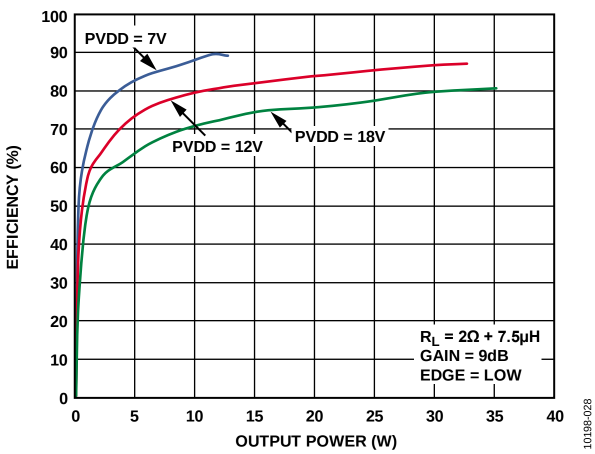


Figure 28. Efficiency vs. Output Power into 2 Ω; Mono Mode; PVDD = 7 V, PVDD = 12 V, PVDD = 18 V

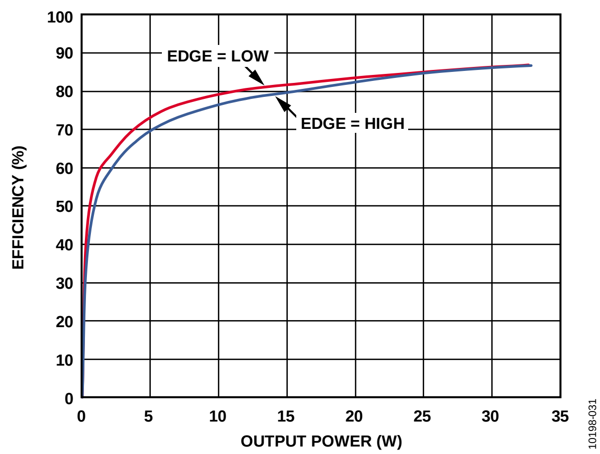


Figure 31. Efficiency vs. Output Power into 2 Ω; Mono Mode; PVDD = 12 V; EDGE = High, EDGE = Low

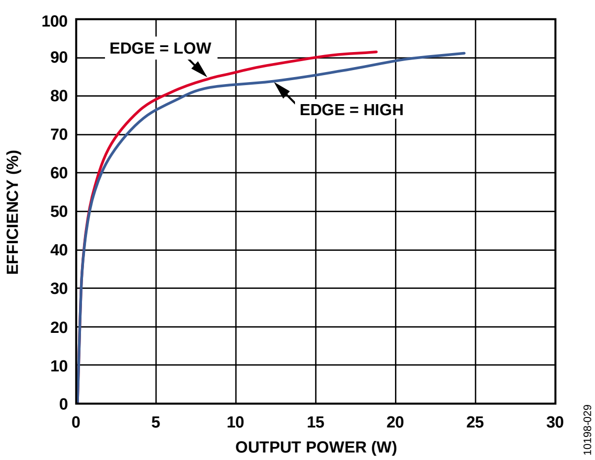


Figure 29. Efficiency vs. Output Power into 8 Ω; PVDD = 12 V; EDGE = High, EDGE = Low

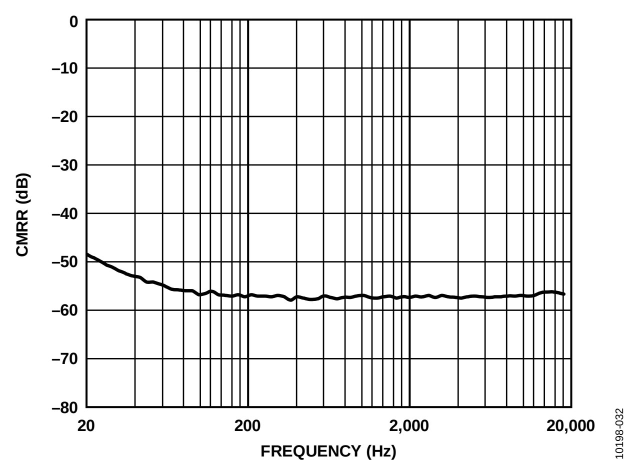


Figure 32. CMRR vs. Frequency, V_{RIPPLE} = 100 mV rms, AC-Coupled

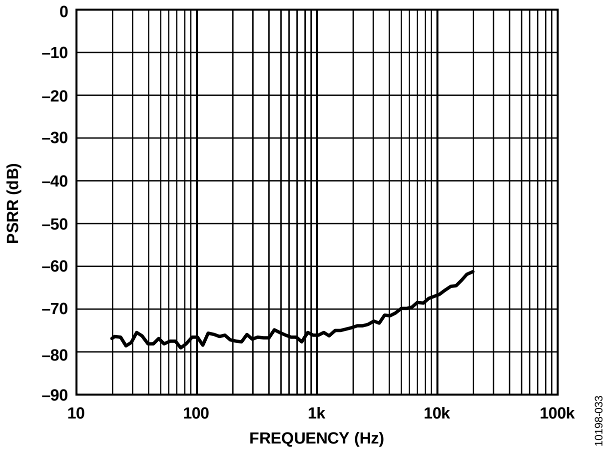


Figure 33. PSRR vs. Frequency, V_{RIPPLE} = 100 mV rms

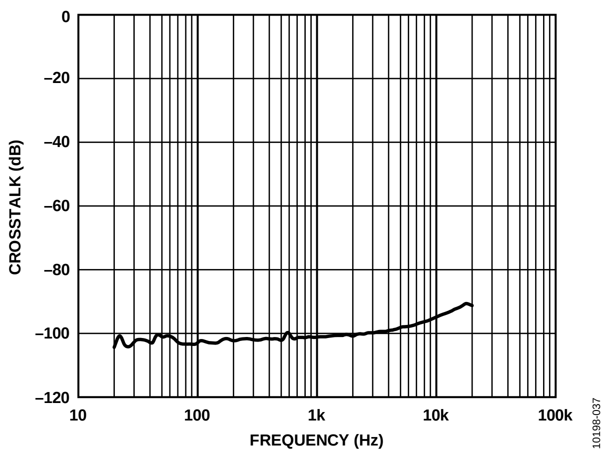


Figure 34. Crosstalk vs. Frequency, P_O = 0.5 W, R_L = 8 Ω

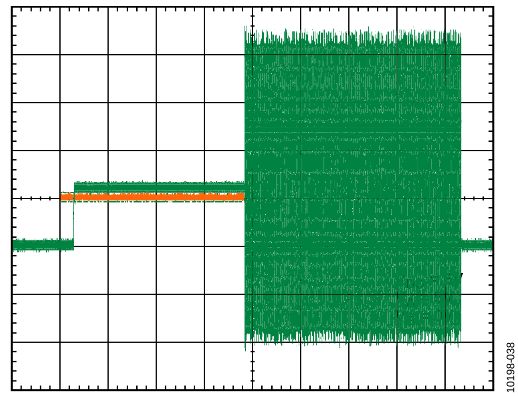


Figure 35. Turn-On Response (Showing $\overline{SDNL}$ Pin or $\overline{SDNR}$ Pin Rising Edge and Output)

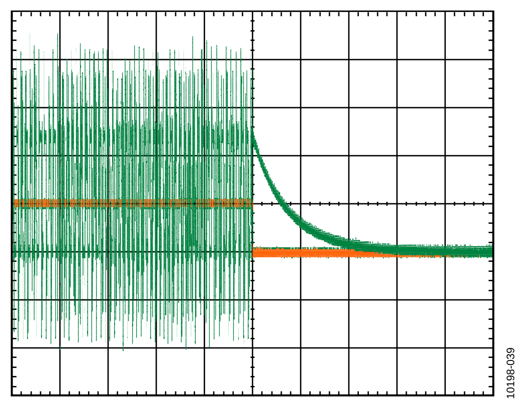


Figure 36. Turn-Off Response (Showing $\overline{SDNL}$ Pin or $\overline{SDNR}$ Pin Falling Edge and Output)

TYPICAL APPLICATION CIRCUITS

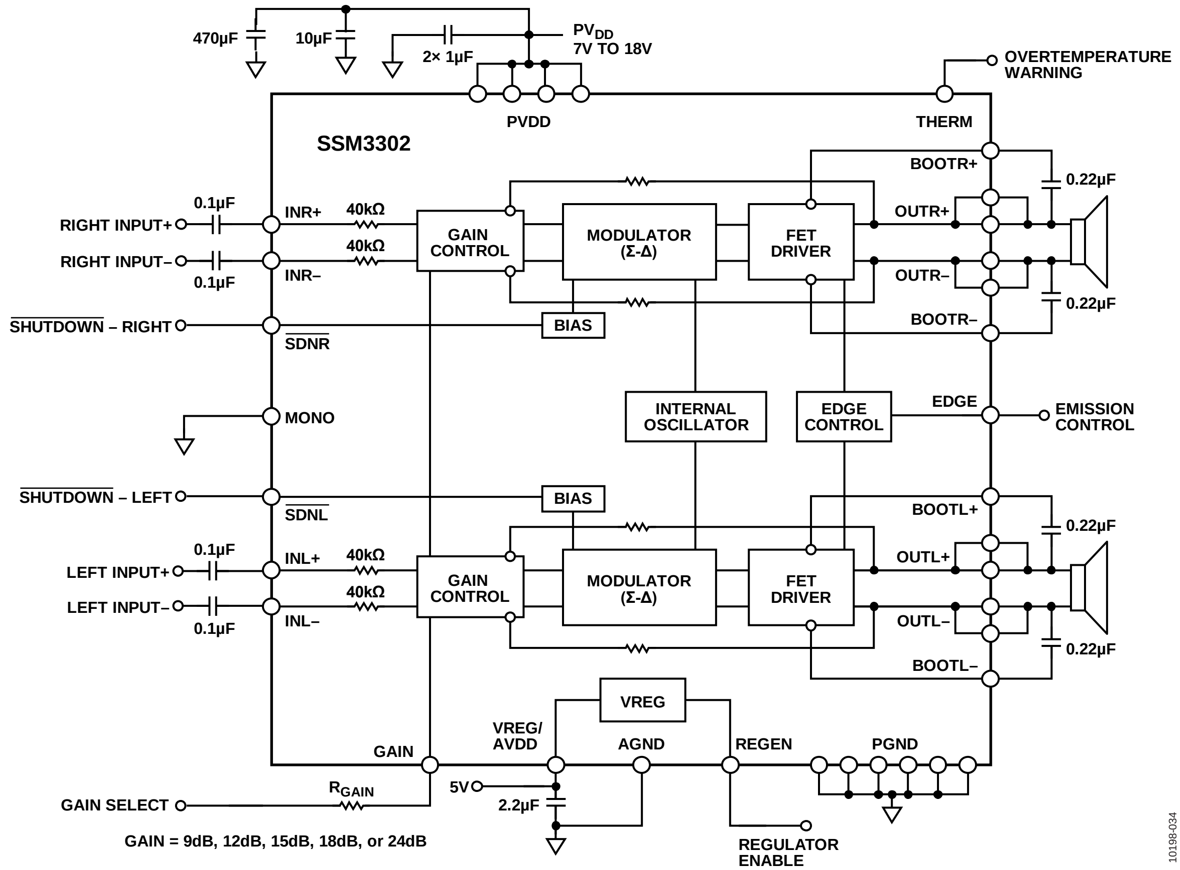


Figure 37. Stereo Mode Configuration

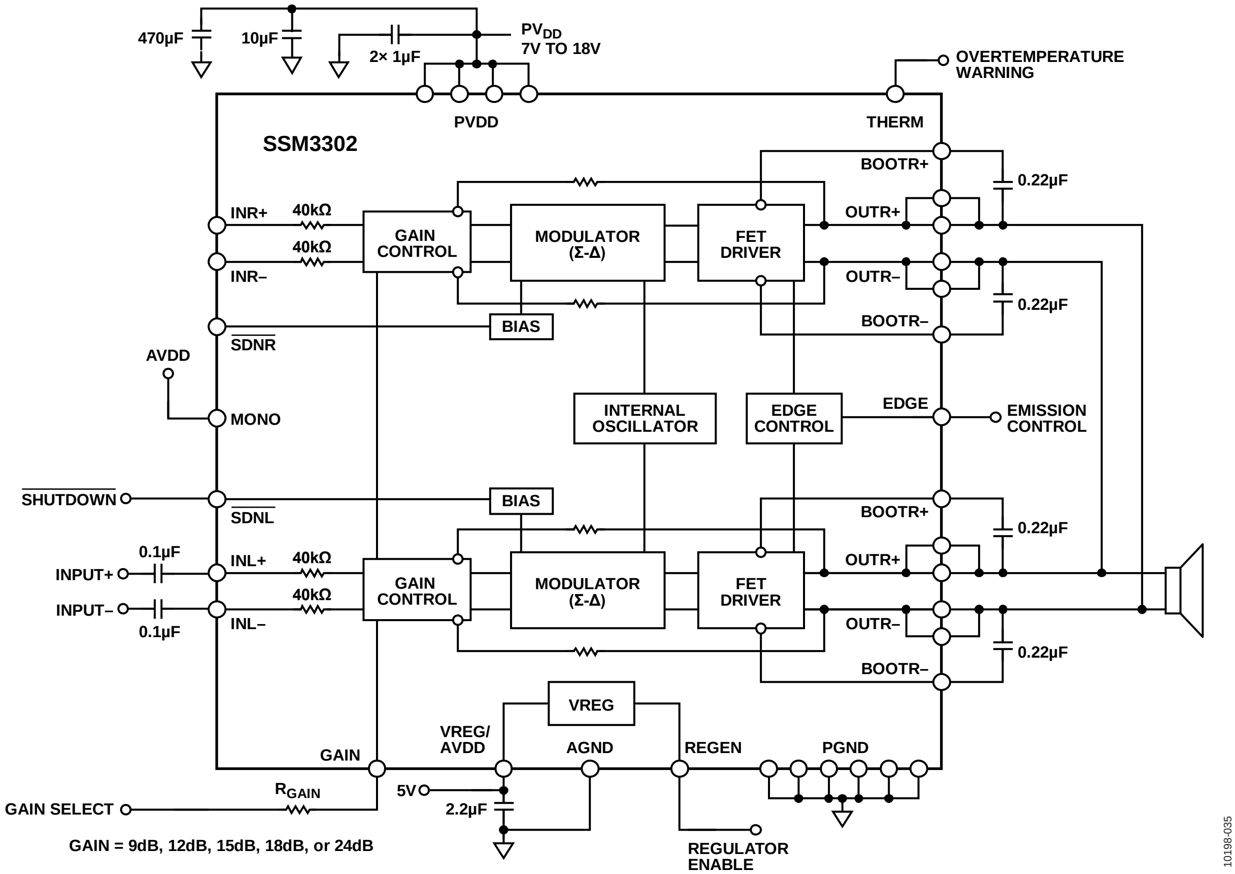


Figure 38. Mono Mode Configuration

APPLICATIONS INFORMATION

OVERVIEW

The SSM3302 stereo Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and reducing system cost. The SSM3302 does not require an output filter; it relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM3302 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in several important benefits. Unlike pulse-width modulators, Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM broadcast band. In addition, Σ-Δ modulation reduces the amplitude of spectral components at high frequencies, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. Due to the inherent spread spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM3302 amplifiers.

The SSM3302 also integrates overcurrent and overtemperature protection, as well as an overtemperature warning indicator pin.

ANALOG SUPPLY

The SSM3302 includes an integrated low dropout (LDO) linear regulator to generate a 5 V supply for the input stage. This regulator can be enabled using the REGEN pin. This analog supply voltage is available at the VREG/AVDD pin. Connect a 2.2 µF decoupling capacitor from this pin to the AGND pin.

Alternatively, an external 5 V analog supply can be connected to the AVDD pin. In this case, tie REGEN low to disable the internal regulator.

The internal 5 V regulator can supply up to 20 mA of current to the VREG pin if other analog circuits use the same supply. The regulator includes short-circuit protection, but no current limiter or other protection is provided.

GAIN SELECTION

The preset gain of SSM3302 can be selected between 9 dB and 24 dB with one external resistor and no change to the input impedance. Gain can be further adjusted to a user-defined setting by inserting series external resistors at the inputs. A major benefit of fixed input impedance is that there is no need to recalculate the input corner frequency (f_c) when gain is adjusted. The same input coupling components can be used for all gain settings.

Table 5. Gain Function Descriptions

Gain Setting (dB)	GAIN Pin Configuration
24	Tie to AVDD
18	Tie to AVDD through 47 kΩ
15	Open
12	Tie to AGND through 47 kΩ
9	Tie to AGND

AMPLIFIER PROTECTION

The SSM3302 includes protection circuitry to prevent damage in case of overcurrent and overtemperature conditions. Shorts across the output terminals, or between either terminal and PVDD or PGND, are also detected; in this case, the output transistors do not switch until the fault is removed.

If the temperature exceeds the threshold temperature (approximately 145°C), the chip is disabled until the temperature drops below the recovery threshold (85°C). This hysteresis prevents rapid cycling of the output at high temperatures.

Additionally, a temperature warning signal is available on the THERM pin. If the die temperature rises above 120°C, a logic high is output on this pin.

POP-AND-CLICK SUPPRESSION

Voltage transients at the outputs of the audio amplifiers may occur when shutdown is activated or deactivated. Voltage transients as small as 10 mV can be heard as an audible pop in the speaker. Clicks and pops are defined as undesirable audible transients generated by the amplifier system that do not come from the system input signal.

Such transients may be generated when the amplifier system changes its operating mode. For example, system power-up and power-down can be sources of audible transients.

The SSM3302 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

EMI NOISE

The SSM3302 uses a proprietary modulation and spread spectrum technology to minimize EMI emissions from the device. The SSM3302 can pass FCC Class-B emissions testing with unshielded 20 inch cable using ferrite bead-based filtering. For applications that have difficulty passing FCC Class-B emission tests, the SSM3302 includes a modulation select pin (ultralow EMI emission mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. Note that reducing the supply voltage greatly reduces radiated emissions.

MONO MODE

The SSM3302 can also be configured to stack its stereo outputs into a monaural amplifier configuration by enabling the mono output mode using the MONO pin. The user can drive a load as small as 2 Ω up to 20 W continuous output power—a particularly useful feature for driving the subwoofer in a 2.1 audio system.

To activate this operation, pull up the MONO pin to the level of VREG/AVDD. In mono mode, OUTL+ and OUTR+ (Pin 2/Pin 3 and Pin 28/Pin 29) provide the noninverting output, and OUTL− and OUTR− (Pin 4/Pin 5 and Pin 26/Pin 27) provide the inverting output. While the device is in mono mode, audio input is taken only from the left channel set of inputs: INL+ and INL− (Pin 11 and Pin 12).

Because the mono mode uses output sense circuitry attached to the left channel outputs, run PCB traces directly from the speaker to the left channel outputs and then extend the PCB traces to the right channel outputs.

OUTPUT MODULATION DESCRIPTION

The SSM3302 uses three-level, Σ-Δ output modulation. Each output can swing from PGND to PVDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, however, there are always noise sources present.

Due to this constant presence of noise, a differential pulse is occasionally generated in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated. However, most of the time, the output differential voltage is 0 V. This feature ensures that the current flowing through the inductive load is small.

When the user sends an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 39 depicts three-level, Σ-Δ output modulation with and without input stimulus.

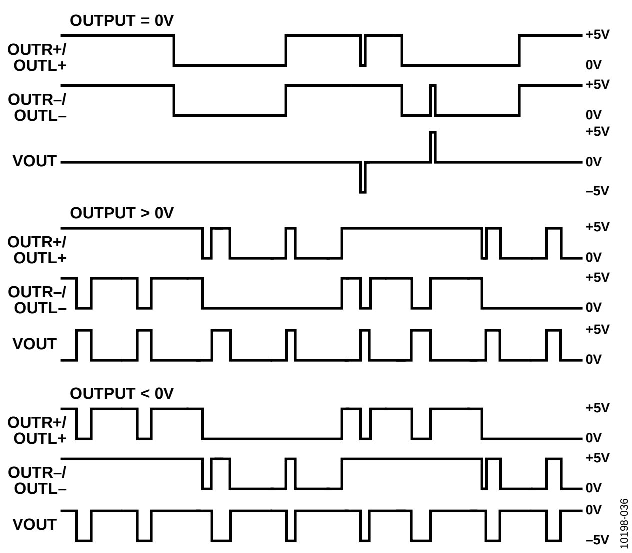


Figure 39. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply; a poor layout increases voltage drops, consequently decreasing efficiency. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. For lowest DCR and minimum inductance, ensure that track widths are at least 200 mil for every inch of length and use 1 oz. or 2 oz. copper. Use large traces for the power supply inputs and amplifier outputs. Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal.

To maintain high output swing and high peak output power, ensure that the PCB traces that connect the output pins to the load and supply pins are as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances. In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate ground planes for small signal and high power connections, there should be no overlap between these planes. Stitch the power plane to the SSM3302 exposed pad using multiple vias. Proper layout improves heat conduction into the board, allowing operation at larger output power levels without overtemperature issues.

INPUT CAPACITOR SELECTION

Input capacitors are required if the input signal is not biased within the recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the SSM3302 form a high-pass filter with a corner frequency determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Failure to use input capacitors degrades the output offset of the amplifier.

BOOTSTRAP CAPACITORS

The output stage of the SSM3302 uses a high-side NMOS driver, rather than PMOS driver. To generate the gate drive voltage for the high-side NMOS driver, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Using 0.22 µF ceramic capacitors with a voltage rating of 35 V or greater is recommended.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion, and high power supply rejection ratio, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. Decouple the power supply input with a good quality, low ESL, low ESR bulk capacitor larger than 220 μF. This capacitor bypasses low frequency noises to the ground plane.

For high frequency transient noises, place two separate 1 μF capacitors as close as possible to the PVDD pins of the device. Connect one of the 1 μF capacitors between the left-side PVDD terminals and PGND terminals, and connect the other 1 μF capacitor between the right-side PVDD terminals and PGND terminals. Placing the decoupling capacitor as close as possible to the SSM3302 helps to achieve the best performance.

OUTLINE DIMENSIONS

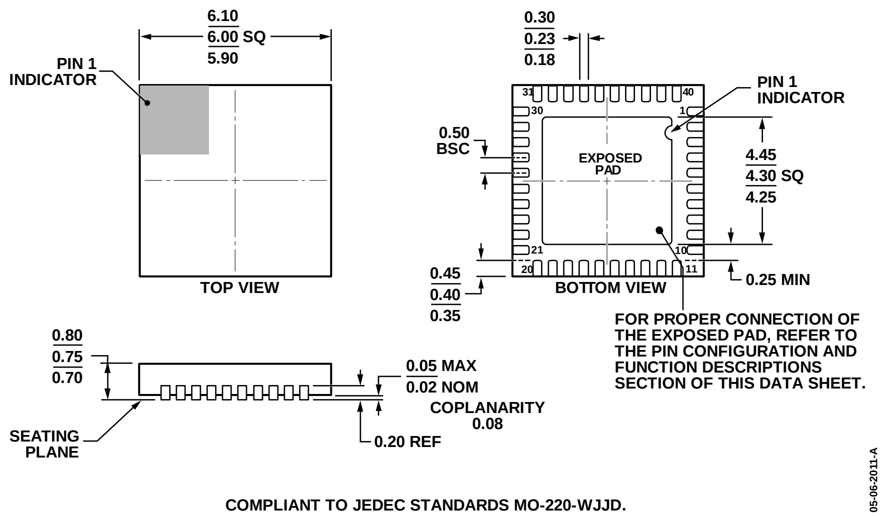


Figure 40. 40-Lead Lead Free Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM3302ACPZ	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP_WQ]	CP-40-10
SSM3302ACPZ-RL	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP_WQ]	CP-40-10
SSM3302ACPZ-R7	−40°C to +85°C	40-Lead Lead Free Chip Scale Package [LFCSP_WQ]	CP-40-10
EVAL-SSM3302Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES