

### FEATURES

- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

### APPLICATIONS

- Multiple Path Timing Deskew for ATE
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

### GENERAL DESCRIPTION

The SMP08 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP08 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to  $\pm 1/2$  LSB in less than 7 microseconds. The SMP08's output swing includes the negative supply in both single and dual supply operation.

The SMP08 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP08 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

### FUNCTIONAL BLOCK DIAGRAM



The SMP08 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP08s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP08 offers significant cost and size reduction over discrete designs. It is available in a 16-pin plastic DIP, or surface-mount SOIC package.

### REV. D

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# SMP08—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_{DD} = +5\text{ V}$ , $V_{SS} = -5\text{ V}$ , $DGND = 0\text{ V}$ , $R_L = \text{No Load}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for SMP08F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		$-3\text{ V} \leq V_{IN} \leq +3\text{ V}$		0.01		%
Buffer Offset Voltage	$V_{OS}$	$T_A = +25^\circ\text{C}$ , $V_{IN} = 0\text{ V}$		2.5	10	mV
Hold Step	$V_{HS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $V_{IN} = 0\text{ V}$		3.5	20	mV
		$V_{IN} = 0\text{ V}$ , $T_A = +25^\circ\text{C}$ to $+85^\circ\text{C}$		2.5	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	$V_{IN} = 0\text{ V}$ , $T_A = -40^\circ\text{C}$			5	mV
		$T_A = +25^\circ\text{C}$ , $V_{IN} = 0\text{ V}$		2	20	mV/s
Output Source Current	$I_{SOURCE}$	$V_{IN} = 0\text{ V}^1$	1.2			mA
Output Sink Current	$I_{SINK}$	$V_{IN} = 0\text{ V}^1$	0.5			mA
Output Voltage Range		$R_L = 20\text{ k}\Omega$	-3.0		+3.0	V
<b>LOGIC CHARACTERISTICS</b>						
Logic Input High Voltage	$V_{INH}$		2.4			V
Logic Input Low Voltage	$V_{INL}$				0.8	V
Logic Input Current	$I_{IN}$	$V_{IN} = 2.4\text{ V}$		0.5	1	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE<sup>2</sup></b>						
Acquisition Time <sup>3</sup>	$t_{AQ}$	$T_A = +25^\circ\text{C}$ , $-3\text{ V}$ to $+3\text{ V}$ to 0.1%		3.6	7	$\mu\text{s}$
Hold Mode Settling Time	$t_H$	To $\pm 1\text{ mV}$ of Final Value		1		$\mu\text{s}$
Channel Select Time	$t_{CH}$			90		ns
Channel Deselect Time	$t_{DCS}$			45		ns
Inhibit Recovery Time	$t_{IR}$			90		ns
Slew Rate	SR			3		V/ $\mu\text{s}$
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		$-3\text{ V}$ to $+3\text{ V}$ Step		-72		dB
<b>SUPPLY CHARACTERISTICS</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{ V}$ to $\pm 6\text{ V}$	60	75		dB
Supply Current	$I_{DD}$	$T_A = +25^\circ\text{C}$		4	7.5	mA
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		5	9.5	mA

## ELECTRICAL CHARACTERISTICS (@ $V_{DD} = +12\text{ V}$ , $V_{SS} = 0\text{ V}$ , $DGND = 0\text{ V}$ , $R_L = \text{No Load}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for SMP08F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		$60\text{ mV} \leq V_{IN} \leq 10\text{ V}$		0.01		%
Buffer Offset Voltage	$V_{OS}$	$T_A = +25^\circ\text{C}$ , $V_{IN} = 6\text{ V}$		2.5	10	mV
Hold Step	$V_{HS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $V_{IN} = 6\text{ V}$		3.5	20	mV
		$V_{IN} = 6\text{ V}$ , $T_A = +25^\circ\text{C}$ to $+85^\circ\text{C}$		2.5	4	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	$V_{IN} = 6\text{ V}$ , $T_A = -40^\circ\text{C}$			5	mV
		$T_A = +25^\circ\text{C}$ , $V_{IN} = 6\text{ V}$		2	20	mV/s
Output Source Current	$I_{SOURCE}$	$V_{IN} = 6\text{ V}^1$	1.2			mA
Output Sink Current	$I_{SINK}$	$V_{IN} = 6\text{ V}^1$	0.5			mA
Output Voltage Range		$R_L = 20\text{ k}\Omega$	0.06		10.0	V
		$R_L = 10\text{ k}\Omega$	0.06		9.5	V
<b>LOGIC CHARACTERISTICS</b>						
Logic Input High Voltage	$V_{INH}$		2.4			V
Logic Input Low Voltage	$V_{INL}$				0.8	V
Logic Input Current	$I_{IN}$	$V_{IN} = 2.4\text{ V}$		0.5	1	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE<sup>2</sup></b>						
Acquisition Time <sup>3</sup>	$t_{AQ}$	$T_A = +25^\circ\text{C}$ , $0\text{ V}$ to $10\text{ V}$ to 0.1%		3.5	4.25	$\mu\text{s}$
Hold Mode Settling Time	$t_H$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		3.75	6.00	$\mu\text{s}$
		To $\pm 1\text{ mV}$ of Final Value		1		$\mu\text{s}$
Channel Select Time	$t_{CH}$			90		ns
Channel Deselect Time	$t_{DCS}$			45		ns
Inhibit Recovery Time	$t_{IR}$			90		ns
Slew Rate	SR			4		V/ $\mu\text{s}$
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		$0\text{ V}$ to $10\text{ V}$ Step		-72		dB
<b>SUPPLY CHARACTERISTICS</b>						
Power Supply Rejection Ratio	PSRR	$10.8\text{ V} \leq V_{DD} \leq 13.2\text{ V}$	60	75		dB
Supply Current	$I_{DD}$	$T_A = +25^\circ\text{C}$		6.0	8.0	mA
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		8.0	10.0	mA

### NOTES

<sup>1</sup>Outputs are capable of sinking and sourcing over 20 mA but offset is guaranteed at specified load levels.

<sup>2</sup>All input control signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

<sup>3</sup>This parameter is guaranteed without test.

<sup>4</sup>Slew rate is measured in the sample mode with 0 V to 10 V step from 20% to 80%.

Specifications subject to change without notice.

# SMP08

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to DGND	-0.3 V, 17 V
$V_{DD}$ to $V_{SS}$	-0.3 V, 17 V
$V_{LOGIC}$ to DGND	-0.3 V, $V_{DD}$
$V_{IN}$ to DGND	$V_{SS}$ , $V_{DD}$
$V_{OUT}$ to DGND	$V_{SS}$ , $V_{DD}$
Analog Output Current	$\pm 20$ mA

(Not Short-Circuit Protected)

## Operating Temperature Range

FP, FS	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

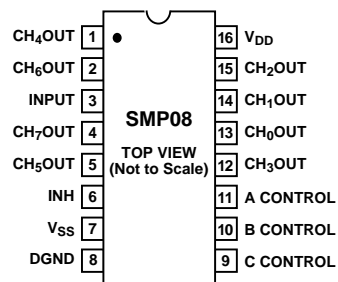
Package Type	$\theta_{JA}^*$	$\theta_{JC}$	Units
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	27	°C/W

\* $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for plastic DIP package;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SMP08FP	-40°C to +85°C	Plastic DIP	N-16
SMP08FS	-40°C to +85°C	SO-16	R-16A

## PIN CONNECTIONS



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SMP08 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# SMP08—Typical Performance Characteristics



Figure 1. Droop Rate vs. Temperature



Figure 2. Droop Rate vs. Input Voltage

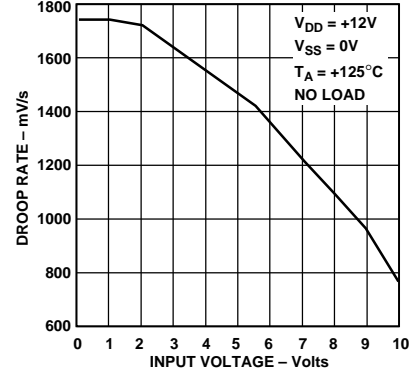


Figure 3. Droop Rate vs. Input Voltage



Figure 4. Hold Step vs. Input Voltage



Figure 5. Hold Step vs. Temperature

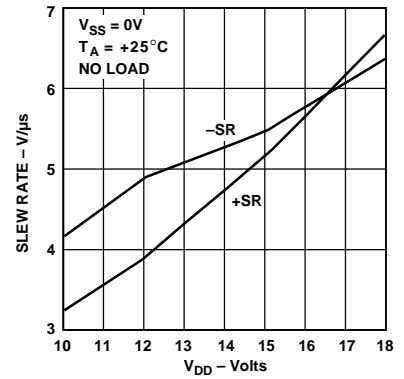


Figure 6. Slew Rate vs.  $V_{DD}$



Figure 7. Offset Voltage vs. Input Voltage



Figure 8. Offset Voltage vs. Input Voltage

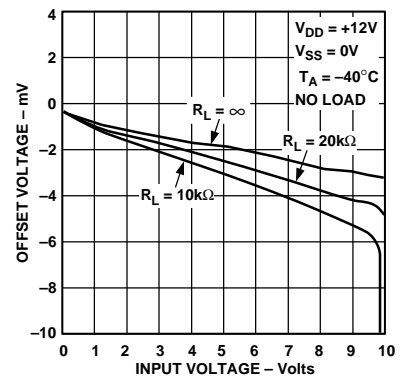


Figure 9. Offset Voltage vs. Input Voltage

# Typical Performance Characteristics—SMP08



Figure 10. Offset Voltage vs. Temperature

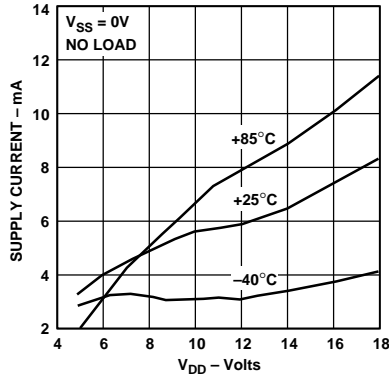


Figure 11. Supply Current vs.  $V_{DD}$

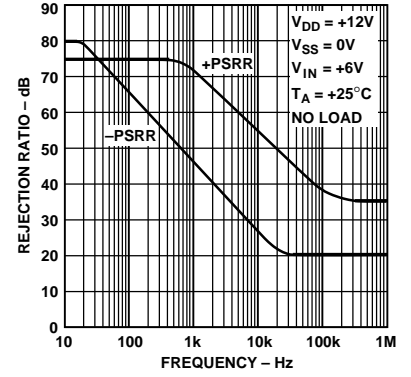


Figure 12. Sample Mode Power Supply Rejection

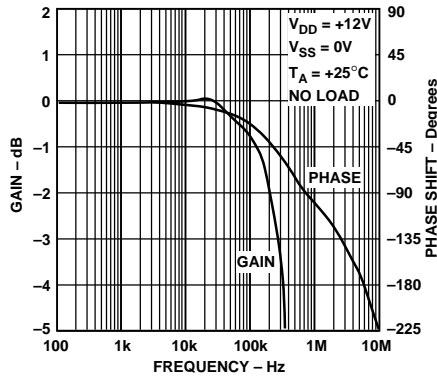


Figure 13. Gain, Phase Shift vs. Frequency

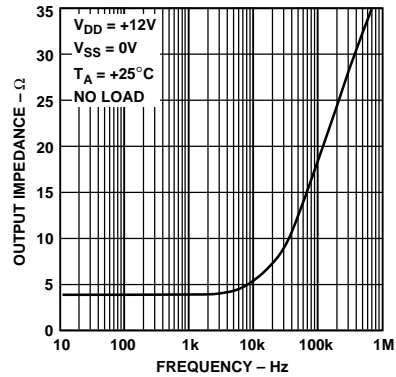


Figure 14. Output Impedance vs. Frequency



Figure 15. Maximum Output Voltage vs. Frequency

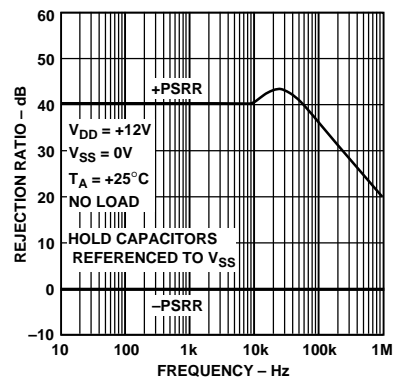


Figure 16. Hold Mode Power Supply Rejection

# SMP08



Figure 17. Burn-In Circuit

## APPLICATIONS INFORMATION

The SMP08, a multiplexed octal S/H, minimizes board space in systems requiring cycled calibration or an array of control voltages. When used in conjunction with a low cost 16-bit D/A, the SMP08 can easily be integrated into microprocessor based systems. Since the SMP08 features break-before-make switching and an internal decoder, no external logic is required. The SMP08 has an internally regulated TTL supply so that TTL/CMOS compatibility is maintained over the full supply range. See Figure 18 for channel decode address information.

## POWER SUPPLIES

The SMP08 is capable of operating with either single or dual supplies, over a voltage range of 7 volts to 15 volts. Based on the supply voltages chosen,  $V_{DD}$  and  $V_{SS}$  establish the input and output voltage range, which is:

$$(V_{SS} + 0.06 V) \leq V_{OUT/IN} \leq (V_{DD} - 2 V)$$

Note that several specifications, including acquisition time, offset and output voltage compliance, will degrade for supply voltages of less than 7 V.

If split supplies are used, the negative supply should be bypassed with a 0.1  $\mu$ F capacitor in parallel with a 10  $\mu$ F to ground. The internal hold capacitors are connected to this supply pin and any noise will appear at the outputs.

In single supply applications, it is extremely important that the  $V_{SS}$  (negative supply) pin is connected to a clean ground. The hold capacitors are internally tied to the  $V_{SS}$  (negative) rail. Any ground noise or disturbance will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. The analog and digital ground traces on the circuit board should be physically separated to reduce digital switching noise from entering the analog circuitry.

## POWER SUPPLY SEQUENCING

$V_{DD}$  should be applied to the SMP08 before the logic input signals. The SMP08 has been designed to be immune to latchup, but standard precautions should still be taken.

## OUTPUT BUFFERS (Pins 1, 2, 4, 5, 12, 13, 14, 15)

The buffer offset specification is 10 mV; this is less than 1/2 LSB of an 8-bit DAC with 10 V full scale. The hold step (magnitude of step caused in the output voltage when switching from sample-to-hold mode, also referred to as the pedestal error or sample-to-hold offset), is about 2.5 mV with little variation over the full output voltage range,  $T_A = +25^\circ\text{C}$  to  $+85^\circ\text{C}$ . The droop rate of a held channel is 2 mV/s typical and 20 mV/s maximum.

The buffers are designed to drive loads connected to ground. The outputs can source more than 20 mA, over the full voltage range, but have limited current sinking capability near  $V_{SS}$ . In split supply operation, symmetrical output swings can be obtained by restricting the output range to 2 V from either supply.

On-chip SMP08 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to 500 pF. However, since the SMP08's buffer outputs are not short-circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

## SIGNAL INPUT (Pin 3)

The signal input should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SMP08's acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ( $V_{SS} \leq V_{IN} < V_{DD}$ ) to avoid the possibility of latchup. If single supply operation is desired, op amps such as the OP183 or AD820 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as  $\pm 7.5$  V, can be used with the SMP08.

## APPLICATION TIPS

All unused digital inputs should be connected to logic LOW and unused analog inputs connected to analog ground. For connector-driven analog inputs that may become temporarily disconnected, a resistor to  $V_{DD}$ ,  $V_{SS}$  or analog ground should be used with a value ranging from 200 k $\Omega$  to 1 M $\Omega$ .



Figure 18. 8-Channel Multiplexed D/A Converter

Do not apply signals to the SMP08 with power off unless the input current is limited to less than 10 mA.

### TYPICAL APPLICATIONS

#### AN 8-CHANNEL MULTIPLEXED D/A CONVERTER

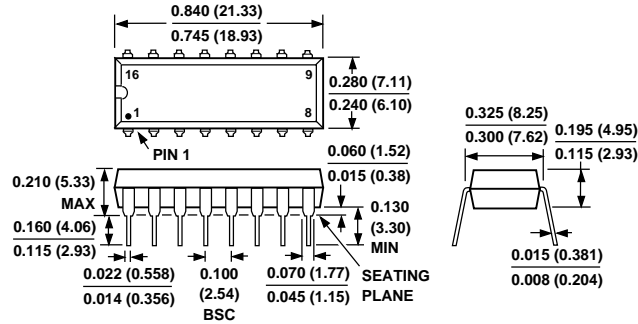
Figure 18 illustrates a typical demultiplexing function of the SMP08. It is used to sample-and-hold eight different output voltages corresponding to eight different digital codes from a D/A converter. The SMP08's droop rate of 20 mV/s requires a refresh once every 500 ms, before the voltage drifts beyond

1/2 LSB accuracy (1 LSB of an 8-bit DAC is equivalent to 19.5 mV out of a full-scale voltage of 5 V). For a 10-bit DAC the refresh rate must be less than 120 ms, and, for a 12-bit system, 31 ms. This implementation is very cost effective compared to using multiple DACs as the number of output channels increases.

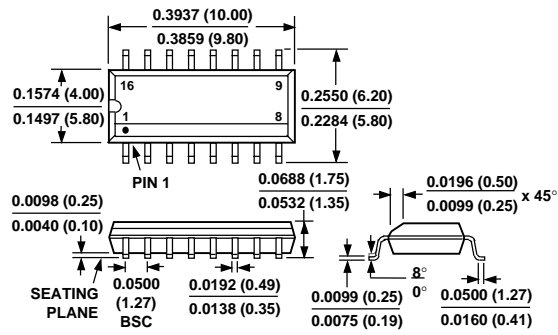
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**16-Lead Plastic DIP  
(N-16)**



**16-Lead SOIC (Narrow Body)  
(SO-16)**





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